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Non-equilibrium hole transport in deep sub-micron Well-Tempered Si p-MOSFETs

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When MOSFETs are scaled to deep submicron dimensions, the non-equilibrium, near ballistic transport in the channel becomes increasingly important. These effects are studied in detail using Monte Carlo (MC) simulations in *n*-channel MOSFETs where, due to the lower electron effective mass and associated scattering rates, the non-equilibrium transport starts to affect the device performance earlier than in *p*-channel devices. Very little has been done in order to study the corresponding effects in *p*-channel devices, partially because of the complicated hole band structure in Si, which requires a detailed model of the bandstructure and substantial computational resources. However recent experimental data [1] show that when MOSFETs are scaled to sub 0.1 μm dimensions, the performance gap, as measured in terms of intrinsic transconductance, between *n*-channel and *p*-channel devices shrinks from 2.5 times at 0.5 μm gate length to no more than 0.4 times at 0.05 μm gate length. Detailed MC simulations are needed to properly understand this phenomenon.

In addition to this, in recent years there has been considerable interest in the possibility to further enhance the performance of sub-micron *p*-channel MOSFETs by introducing a strained SiGe channel, which leads to a substantial increase in the hole mobility. This may reduce the asymmetry of the *n* and *p*-channel gate lengths in CMOS devices. However, industry has yet to take up the challenge of introducing SiGe into MOS devices, as this would not only require a massive retooling, but also because it has been able to meet the requirements of the Silicon Road Map by the aggressive scaling of conventional Si *p*-MOSFETs. Therefore, if SiGe is to make a commercial impact it must be able to out perform the best standard Si *p*–channel MOSFETs in deep submicron regime, where non-equilibrium transport becomes more important than the mobility itself.

In this work, using 2D full-band MC simulations we study non-equilibrium transport effects and the performance potential of *'Well Tempered'* Si *p*-channel MOSFETs covering gate lengths ranging from 90nm to 25nm (which corresponds to the period from 2002 to 2014 in the Silicon Roadmap). These devices, are a mirror reflection in terms of doping in the channel and in the polysilicon gate, of the *'Well Tempered' n*-channel MOSFETs advanced in [2]. They represent the current perception for the best that conventional Si MOSFET technology can, and will, be able to achieve, taking into account the fully scaled oxide thickness and junction depth amongst other design parameters. These devices are also an excellent basis with which to compare future designs for SiGe and other advanced *p*-MOSFET architectures. Figure 1 shows the bulk velocity-field characteristics obtained from our Monte Carlo simulator, which includes an approximation for the Bloch overlap integrals. Figure 2 shows drain current characteristics for a 50nm *'Well Tempered'* Si *p*-MOSFET, obtained from Monte Carlo simulations. The velocity distribution in the channel of the device is given in Figure 3.

By comparing MC simulations with carefully calibrated Drift Diffusion (DD) simulations of the same devices, we will provide a quantitative estimate of the importance and the influence of non-equilibrium transport on the device performance. This in turn may provide an explanation for the closing gap between the *n*- and *p*- channel MOSFETs in the deep submicron area. In addition we are aiming to present results from hydrodynamic (HD) and energy balance (EB) simulations of the well tempered *p*-channel MOSFETs, using energy dependent relaxation times extracted from MC simulations. This will provide an insight as to what extent the HD and EB simulations can be used with confidence in the design of deep submicron p-channel devices.

References

[1] A. Hori and B. Mizuno, International Electron Devices Meeting (Washington DC) 1999, 27.1.1-27.1.4

[2] "Well-Tempered" Bulk-Si n-MOSFET Device Home Page *http://www-mtl.mit.edu/Well/*

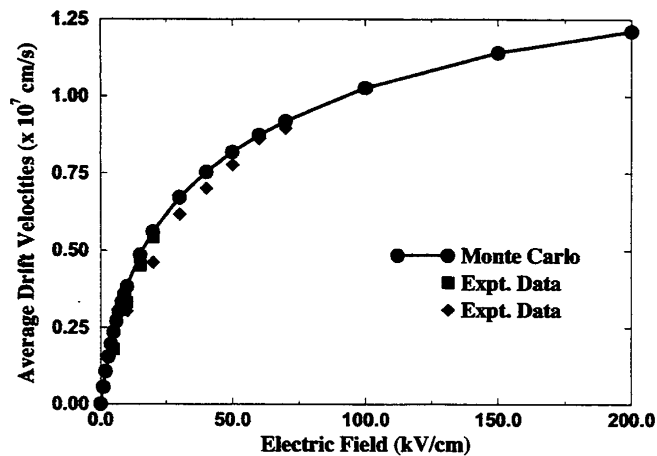

Figure 1: Velocity-field characteristics for holes in Si.

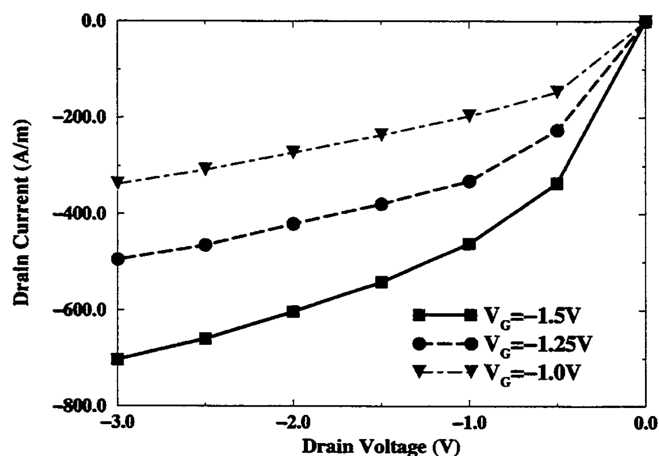

Figure 2: Drain current characteristics of 50nm *'Well-Tempered'* Si p-MOSFET.

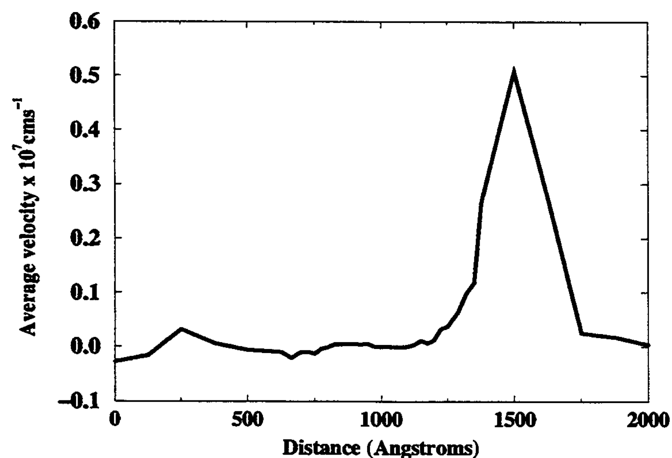

Figure 3: Hole velocities along the channel of the 50nm *'Well-Tempered'* Si p-MOSFET,

V_G=-1.5V, V_D=-2.5V