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Indication of Non-equilibrium Transport in SiGe *p*-MOSFETs

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Abstract

We have investigated the high field transport in CMOS compatible $Si_{0.64}Ge_{0.36}$ p-MOSFETs with various gate lengths for two different Si cap thicknesses. Using a fully calibrated Drift Diffusion and Energy Transport models, we have obtained good agreement with measurements across the entire range of voltages and gate lengths. Our results clearly indicate the presence of non-equilibrium transport in SiGe channels, which results from larger energy relaxation times in pseudomorphic SiGe layers in comparison with Si.

1. Introduction

The operational efficiency of CMOS circuits is limited by the poor performance of *p*-MOSFETs due to a 2.5 times smaller hole mobility as compared with electrons. Consequently, Si *p*-MOSFETs must be designed with a wider gate than their *n*-channel counterparts. Incorporation of a buried pseudomorphic SiGe layer into a *p*-MOSFET leads to improvements in hole mobility and may result in higher packing densities [1]. The improvement results from changes in the strained SiGe band-structure and reduction in scattering due to roughness and trapped charge at the Si/SiO_2 interface [2].

We have recently shown [3], using SiGe *p*-MOSFETs especially designed for high field measurements, that non-equilibrium transport may play an important role in deep-submicron SiGe devices. In this work we have successfully used numerical simulations to analyse the high field transport in fabricated *p*-MOSFETs with conventional architecture. It is found that non-equilibrium transport and related velocity overshoot may be important in evaluating device performance in devices with effective gate lengths as large as 0.38°µm The calibrated DD simulations are compared with energy transport (ET) results to validate the importance of non-equilibrium conditions. We also indicate the importance of parallel conduction in SiGe *p*-MOSFETs with varying Si cap thickness.

2. Device Structure

A schematic of the structure of devices analysed in this work is shown in figure 1. Active layers are MBE grown on a n^+ doped ($2\times10^{17}cm^{-3}$) Si substrate to reduce short channel effects. The SiGe strained channel is isolated from the substrate with a 100 nm undoped Si buffer layer.

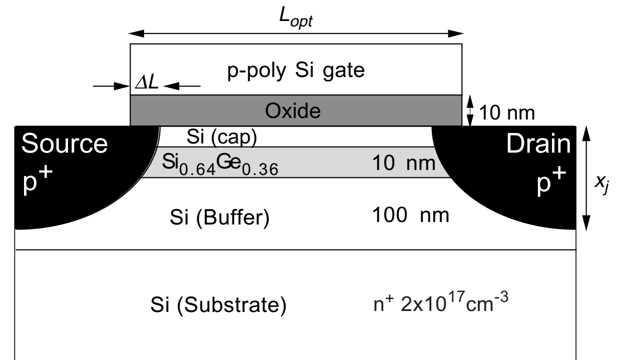

Figure 1 Simulated device structure

The channel doping is background limited (~$5\times10^{15}cm^{-3}$) to maximise the mobility. We have considered two different Si cap thicknesses: 2nm (wafer 1) and 8nm (wafer 2). The devices with drawn gate lengths (L_{opt}) 3, 1.8, 1.3 and 0.5 µm for wafer 1, and 3, 2, 1 and 0.5 µm for wafer 2 are fabricated using standard CMOS processes flow. Using a process simulator (TSUPREM4^{TM} [4]), we evaluated the final doping profile in these devices, resulting in a junction depth (x_j) of 0.3 µm. The gate width is 40 µm and gate oxide is 10 nm for all devices. Total thermal budget is kept to a minimum (800°C) to avoid degradation of the strained channel.

3. Simulation based analysis

We use DD simulations to analyse the operation of the devices and to deduce information about the transport in the SiGe channel. The calibration procedure starts by obtaining reliable estimates for the source R_S and drain resistances R_D, the sub-diffusion length (ΔL), as well as the low field hole mobility μ_{PO} and threshold voltage V_{TH}, using the method described by Laux [5]. Our analysis yields values of 90 Ω for the series source and drain resistance and values of 0.08 µm and 0.12 µm for ΔL in wafers 1 and 2 respectively. In our DD simulations [4], we consider vertical and longitudinal mobilites with the dependence on electric field described by:

$$\mu_{p\perp} = \frac{\mu_{po}}{\sqrt{1+\frac{E_\perp}{E_C}}}$$

and

$$\mu_p = \frac{\mu_{p\perp}}{\left[1+\left(\frac{\mu_{p\perp}E_{\|}}{v_{sat}}\right)^{\beta}\right]^{1/\beta}}$$

where $E_\perp$ and $E_{//}$ are the perpendicular and parallel components of the local electric field respectively, E_c is the critical field, v_{sat} is the saturation velocity, and § is a fitting parameter. Taking extracted parameters as initial values, we proceed to determine μ_{PO}, E_C, R_S and R_D by adjusting them to obtain the best fit to experimental I_D-V_{GS} data at a low drain bias (-50mV) for each channel length. These parameters are then kept constant, while we tune v_{sat} and §, to obtain the closest agreement with the measured I_D-V_D characteristics for different gate voltages. Further details of the calibration procedure is given elsewhere [3].

At the end of calibration, any increase in v_{sat} with reduction of gate length may be attributed to the effects of non-equilibrium carrier transport. In order to confirm the presence of such effect, finally, we employ the ET simulations, which properly take non-equilibrium transport into account. The relaxation times required for the ET model are obtained from our full band Monte Carlo (FBMC) bulk simulator [6,7].

4. Results and discussion

Employing the calibration procedure described in section 3, we have obtained very good agreement between the measured and simulated characteristics for both wafers, as can be seen in figures 2-4. The two most important figures of merit ($_{PO}$ and v_{sat}) for different channel lengths, are given in table 1, for both wafers. The first (second) parameter in each table cell refers to the SiGe (Si) layer. Note that the low field mobility parameters in table 1 are consistent for each wafer. The $Si_{0.64}Ge_{0.36}$ channel exhibits a ~70% improvement in wafer 1 whereas wafer 2 sports an impressive 230% increment in mobility. The lower mobility in wafer 1 is speculated to be due to the influence of Si/SiO_2 interface on the scattering in the SiGe channel, enhanced as a result of the very thin Si cap layer [8].

Table 1. Calibration parameters obtained.

Wafer	*L(µm)*	*µ(cm²/Vs)*	*v_{sat}(10⁷cm/s)*
1	3.0	340/200	0.35/1
1	1.3	340/200	0.45/1
1	0.5	340/200	0.50/1
2	3.0	550/240	0.60/1
2	1.0	550/240	0.65/1
2	0.5	550/240	0.70/1

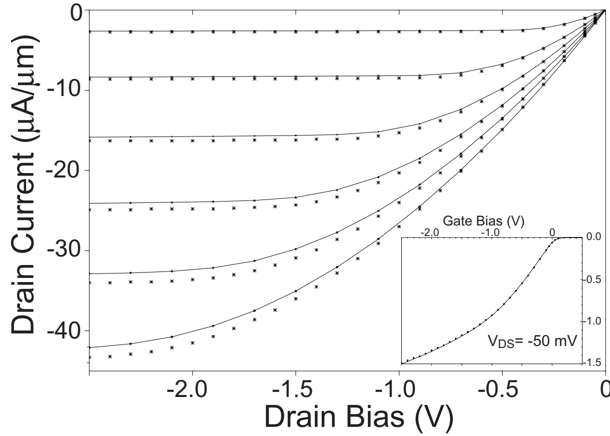

Figure 2. Measured (•) and simulated (—) I-V data for wafer 2, L_{opt}=3µm.

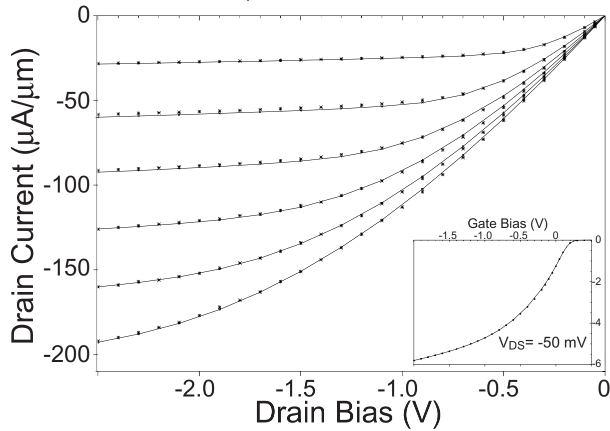

Figure 3. Measured (•) and simulated (—) I-V data for wafer 2, L_{opt}=0.5µm.

The implications of the calibration procedure are summarised in figure 5, where we plot the longitudinal field versus hole velocity curves corresponding to values given in table 1 for both wafers. It is evident from our calibration that the average hole velocity in the channel increases as L_{opt} is scaled down to an effective channel length of 0.38 µm. It must be noted that, strictly within the calibration context, v_{sat} is different from the bulk saturation velocity and gives an indication of average carrier velocity in the channel. We believe that non-equilibrium transport conditions in short channel devices (where the longitudinal electric field rapidly increases) are responsible for the increase in v_{sat}, required by the calibration process for good agreement with experiment. We found that velocity overshoot is expected to be more significant in SiGe *p*-MOSFET than in Si devices, due to a larger relaxation time in the former as compared to the latter

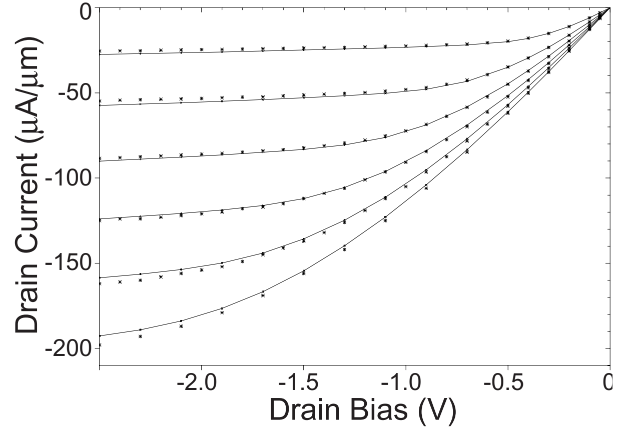

Figure 4. Measured (•) and simulated (—) I-V data for wafer 1, L_{opt}=0.5µm..

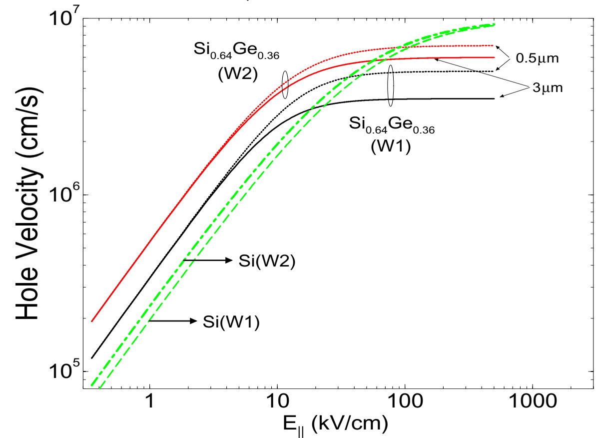

Figure 5. Velocity-field characteristics obtained from the calibration procedure

[6]. Hence, even though v_{sat} in strained SiGe is lower than bulk Si, non-equilibrium transport occur in the former earlier.

At this point, it is useful to independently demonstrate the presence of non-equilibrium conditions in our devices. The ET model of MEDICI™ is used to this end, taking the energy relaxation times generated by our FBMC module. As shown in figure 6, for the shortest channel length the ET simulations agree with the experimental data and calibrated DD model. If, however, we repeat the DD simulation of the same device with v_{sat} obtained from the calibration of the long (3 µm) channel device, the current is underestimated (figure 6). This confirms the accuracy of our calibration procedure and attest to the presence of non-equilibrium transport in the shortest device. Additional insight can be gained from the inset in figure 6, where we plot the hole velocity profiles along the SiGe channel obtained

from different models. Firstly, ET velocity curves reach velocities above the saturation limit in the bulk [9] confirming the presence of non-equilibrium transport. Secondly, the DD velocities obtained using long channel (L_{opt}=3 µm) calibration parameters in the short channel (L_{opt}=0.5 µm) limit fails to reproduce the ET curve, in marked contrast with the calibrated DD simulations.

Finally, we would also like to indicate that the thickness of Si cap has an important influence on the performance of SiGe *p*-MOSFETs. Although the devices with a thin Si cap have a lower mobility as discussed earlier, we observe that the drain currents in figures 3 and 4 are almost equal at V_{GS}=-3V and V_{DS}=-2.5V, for a channel length of 0.5 µm. This seemingly contradictory situation can be clarified, if we consider the Si cap mobility for both wafers in table 1 together with the parallel conduction observed in the thicker cap layers [10]. For a thick cap with a higher Si mobility, SiGe *p*-MOSFETs have significant parallel conduction with a populated 2DHG at the Si/SiO_2 interface. Consequently, the parallel conduction significantly reduces the drain current, along with the performance of these devices

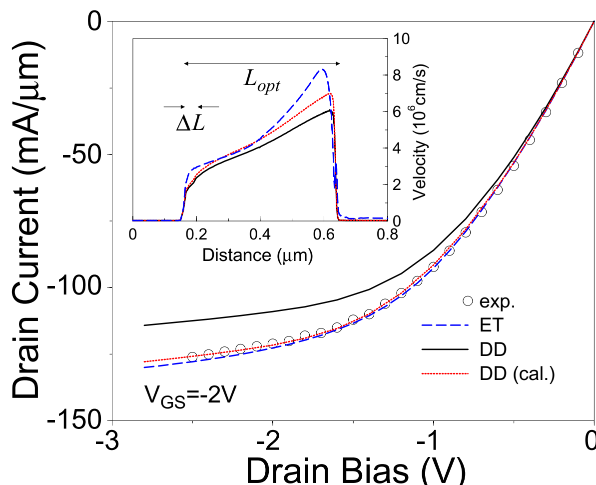

Figure 6. Comparison of DD and ET transport models in 0.5 µm p-MOSFETs. (wafer 2) V_{DS}=-2.5V in the inset

5. Conclusions

$Si_{0.64}Ge_{0.36}$ *p*-channel MOSFETs fabricated with a CMOS compatible process in varying gate lengths and two different cap thickness have been investigated using a calibrated drift diffusion model. Enhanced low field mobility in $Si_{0.64}Ge_{0.36}$ layers compared to Si control devices is observed. In addition, it is found that the effective saturation velocity for strained channel devices increases as the channel length decreases, which may be interpreted as an early indication of velocity overshoot. Simulations based on a Energy Transport model, which includes approximations for non-equilibrium transport effects, confirms the calibration procedure and results. The influence of the thickness of the Si cap layer in SiGe *p*-MOSFET architecture is also indicated.

Acknowledgements

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