Enhanced Velocity Overshoot and Transconductance in $Si/Si_{0.64}Ge_{0.36}/Si$ pMOSFETs - Predictions for Deep Submicron Devices

M. J. Palmer, G. Braithwaite, M. J. Prest, E. H. C. Parker and T. E. Whall
Dept of Physics, University of Warwick, Coventry CV4 7AL, England
E-mail: Martin.Palmer@warwick.ac.uk

Y. P. Zhao, S. Kaya, J. R. Watling, A. Asenov and J. R. Barker
Device Modelling Group, University of Glasgow, G12 8LA, Scotland

A. M. Waite and A. G. R. Evans
Department of Electronics and Computer Science, University of Southampton, Highfield, Southampton, SO17 1BJ, England

Abstract

Electrical measurements have been carried out on $Si/Si_{0.64}Ge_{0.36}/Si$ pMOS devices and it is demonstrated that enhanced low field carrier mobilities lead to concomitant and substantial enhancements in velocity overshoot and transconductance at deep submicron channel lengths. This provides considerable motivation for incorporating SiGe into Si MOS technology.

1. Introduction

There is much interest in fully pseudomorphic Si/SiGe/Si structures for Si-CMOS applications with a major objective of realising symmetrical CMOS with matching p-channel/n-channel performance [1]. However, whereas performance enhancements are impressive - factors of two or more at large channel lengths (>3 μm) [2], they are only modest for channel lengths of about 0.5 μm [3,4]. CMOS channel lengths are now, of course, approaching 0.1 μm but there are only a few reports on SiGe devices of this geometry. Whereas current drive enhancements of about a factor of two have been demonstrated at deep submicron compared to silicon controls, [5,6] the absolute values of current fall short of state-of-the-art silicon. There is therefore an urgent need for more work. The present paper puts the disappointing results at 0.5 μm into perspective and provides strong motivation for further investigations at 0.1 μm and below. Electrical measurements have been carried out at 77K in order to access higher (but realistic) mobilities, which otherwise would have to be obtained by the much more challenging route of maintaining materials quality in a fully processed pseudomorphic device. Alternatively, high mobilities may be achieved by the use of high-germanium

content layers grown pseudomorphically on SiGe virtual substrates. However, the production of virtual substrates of sufficient quality for MOS technologies remains a major challenge and the subject of much study. At this stage their use can only be anticipated. The current investigation follows those of Kaya *et al*. [7] and Zhao *et al.* [8], in which we reported enhanced velocity overshoot as compared to silicon in $Si/Si_{0.8}Ge_{0.2}/Si$ structures [7] and in the present devices [8] at 300K. It provides further support for the analysis given there.

The previous works extend the analysis to include energy transfer and Monte-Carlo simulations. They show that the origin of the velocity overshoot enhancement derives essentially from increased energy relaxation times in SiGe coupled with improved low field mobilities.

2. Fabrication, Measurement and Modelling

We have measured and modelled the drain characteristics of nominal $Si/Si_{0.64}Ge_{0.36}/Si$ pMOS devices of different effective channel lengths $0.35 < L_{eff} < 10$ μm and nominal silicon cap thicknesses $2\text{ nm} \le t_{cap} \le 8$ nm. The detailed specifications, fabrication and effective mobilities of those devices at 300K have been previously discussed [9].

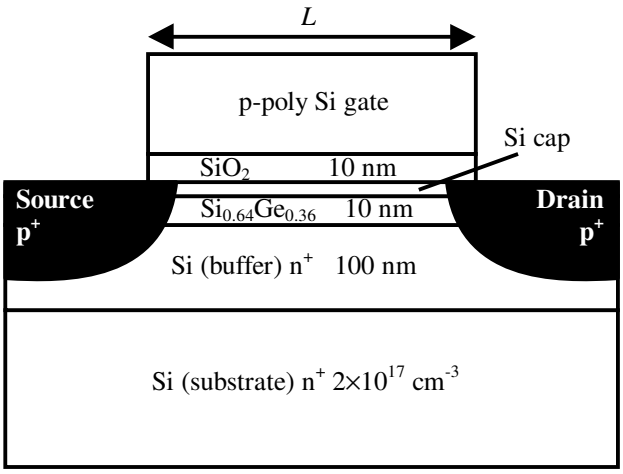

Figure 1. Schematic of the MOSFET structure

A schematic of the MOSFET structure is shown in figure 1 and the measured characteristics of a 8 nm silicon cap device are shown in figure 2. Using a commercial 2D device simulator [10] and empirical expressions for the vertical and horizontal field dependence of the carrier drift velocity we have obtained good fits to the data, also shown in figure 2.

3. Results and Discussion

From the model we have extracted the apparent saturation drift velocities, $\tilde{v}_{sat}$, given in figure 3. We note first of all that the long channel value of $\tilde{v}_{sat}$ in SiGe is less than that of silicon. In previous papers we have argued [9,11,12] that the low field room temperature mobility in these heterostructures is limited by interface roughness scattering. However, it has been shown [13,14] that alloy scattering increases by orders of magnitude in high horizontal fields and this is a possible explanation of the low value of $\tilde{v}_{sat}$ in the alloy. The small value of $\tilde{v}_{sat}$ means that the current drive/transconductance at 0.5μm

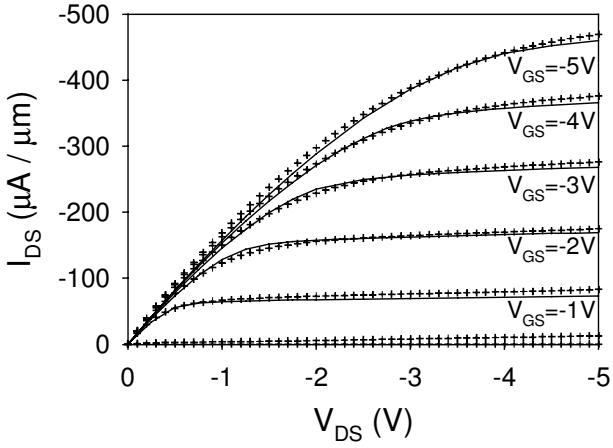

Figure 2. Example measured (+) and simulated (—) current characteristics: SiGe, 8 nm Si cap, L_{eff} = 0.35 μm.

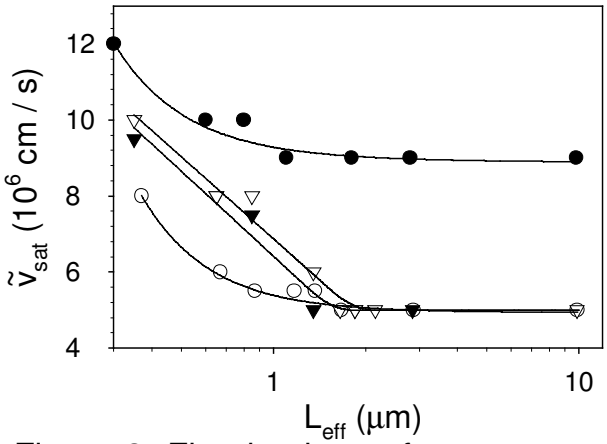

Figure 3. Fitted values of $\tilde{v}_{sat}$ versus gate length for SiGe samples with 2 nm (O) 5 nm (▼) and 8 nm (▽) caps and Si control (●).

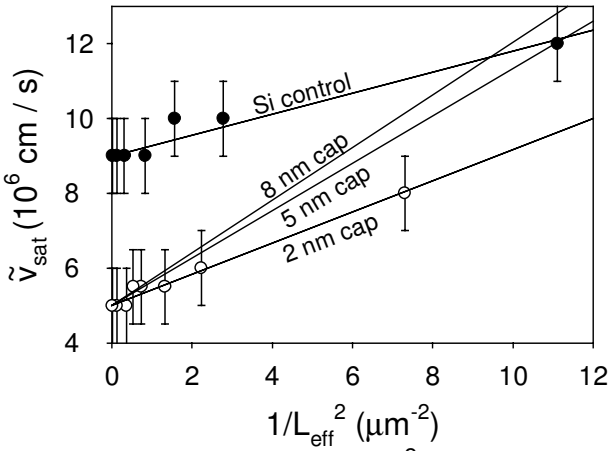

Figure 4. $\tilde{v}_{sat}$ versus $1/L_{eff}^2$ for SiGe samples and Si control. The 5 and 8 nm data points are omitted for clarity. The trend is similar but with more scatter.

is not substantially enhanced compared to silicon, in spite of the higher mobility [4]. However, as the channel length decreases, we observe a dramatic increase in $\tilde{v}_{sat}$ in the SiGe devices, substantially larger than in the silicon controls, which is attributed to velocity overshoot.

Following the analysis of Roldan *et al.* [15], we fit the drift velocity data to:

$$\tilde{v}_{sat} = v_{sat} + \lambda\, dE_{\parallel}/dx$$
$$\approx v_{sat} + \lambda_a V_{DS}/L^2$$

where v_{sat} is the velocity in a homogeneous field, $dE_{\parallel}/dx$ is the gradient of the electric field parallel to the surface and λ and λ_a are fitting parameters. Figure 4 shows $\tilde{v}_{sat}$ versus $1/L^2$ for the various devices. Using the λ_a values obtained from figure 4 we can predict the saturation transconductance enhancement from the form [15]

$$g_m = \frac{W}{L} C_{GC} V_{DS} \left[\frac{\mu}{1 + \frac{\mu}{v_{sat}} \frac{V_{DS}}{L}} + \frac{\lambda_a}{L} \right]$$

where C_{GC} is the gate to channel capacitance and μ is the low lateral field mobility corresponding to the average vertical field in the device with V_{GS}=-1V (to restrict transport to the SiGe channel) and V_{DS}=-3.3V. Table 1 shows a comparison of the

Table 1. Peak low field mobility at 300K [9] and 77K.

Sample	μ_{77K} (cm^2/Vs)	μ_{300K} (cm^2/Vs)
2 nm cap	569	162
5 nm cap	796	217
8 nm cap	1454	305
Si control	322	128

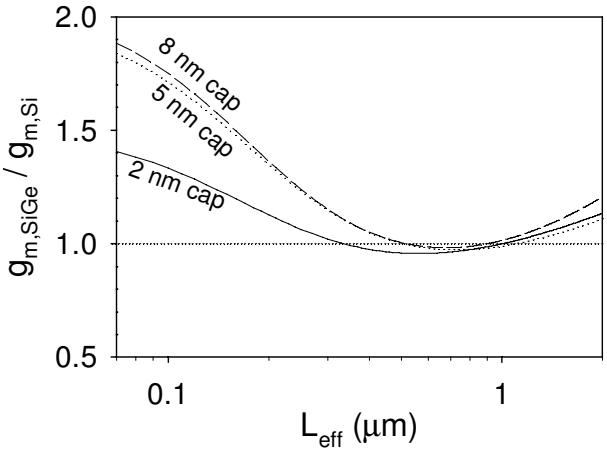

Figure 5. Predicted enhancement of saturation transconductance for SiGe samples compared to silicon control.

peak values of measured mobility at 77K and at room temperature. The ratios between the intrinsic transconductances of the SiGe samples and the Si control, taking account of the variation of C_{GC} with vertical architecture, are plotted against channel length in figure 5. The model predicts up to a factor of 1.9 improvement at L_{eff} = 0.07 μm.

4 Conclusions

$Si_{0.64}Ge_{0.36}$ p-channel MOSFETs operating at 77K have been investigated in an attempt to probe a high-mobility region of operation. An enhanced apparent saturation velocity at short channel lengths indicates velocity overshoot. The results are extrapolated to deep submicron gate lengths, predicting significant improvements in the transconductances of devices containing a SiGe channel. We expect similar enhancements at room temperature, especially as the low field mobilities can be improved. Even with existing devices, a rough estimate using the same extrapolation with the room temperature analysis [8] predicts a factor of 1.4 enhancement at L_{eff} = 0.07 μm. Notwithstanding the limitations of the present simulation methods [7,15,16], the enhancements predicted for $L_{eff} \leq 0.07$ μm should provide considerable encouragement for those seeking to fabricate SiGe MOS devices at small geometries.

5. References

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