High Performance III-V MOSFETs: a Dream Close to Reality?

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Abstract

We have studied the performance potential of sub 100 *nm* compound MOSFETs with InGaAs channel and high-*k* gate insulator, using ensemble Monte Carlo simulations. The results show that such devices could deliver 200-300% increase in the drive current compared to conventional MOSFETs with analogous channel lengths and device structure. This improvement is much higher than the 20-30% drive current increase in similar devices with strained Si channels on virtual SiGe substrates. As a viable solutions to the constant drive current bottleneck anticipated in the International Roadmap for Semiconductors for the next generations of Si MOSFETs it advocates further research in respect of the manufacturability of compound MOSFETs.

1. Introduction

The semiconductor industry is ready to adopt non-orthodox materials, technologies and devices in the silicon end-game. These already include the introduction of exotic high-*k* dielectrics in the gate stack of silicon MOSFETs to replace the native silicon dioxide [1]; the declared intention of leading manufacturers like IBM [2] and Intel to integrate the epitaxial SiGe in conventional CMOS; and the exhaustive research in alternative device architectures, including thin SOI [3], double [4] and FIN gate [5] MOSFETs. The availability of 12 inch silicon wafers with GaAs on top of $SrTiO_3$ buffers [6] offers new scenarios for integrating in an economic way very fast digital compound MOSFETs with less demanding Si blocks on a single chip, see Fig. 1. Both MESFETs [6] and HEMTs [7] with characteristics similar to those devices fabricated on traditional GaAs wafers have been demonstrated using EPIGEN™ technology. The enormous potential for the speed and drive current improvements in GaAs/InGaAs MOSFETs derives from the extremely high electron mobility and reduced phonon scattering compared to the conventional and strained silicon devices. At the same time, the development of suitable high-*k* gate dielectrics may prove to be less problematic compared to silicon [8]. Indeed, in September 2002, Motorola reported a self-aligned GaAs *p*-channel MOSFET with good properties of the Ga_2O_3/AlGaAs interface [9].

Using ensemble Monte Carlo simulations we have studied the potential performance of sub-100 *nm* *n*-type strained $In_{0.2}Ga_{0.8}As$ channel MOSFETs with a high-*k* gate dielectric utilising GaAs on 12 inch Si EPIGEN™ technology. The simulated performances of equivalent device geometries have been compared to the measured performances of *n*-type 67 *nm* conventional and strained Si channel MOSFETs reported by IBM [2] and 35 *nm* conventional MOSFETs reported by Toshiba [10].

2. Simulation Approach

The simulations of the III-V MOSFETs have been carried out using our ensemble Monte Carlo (MC) compound semiconductor simulator H2F/MC described in detail elsewhere [11, 12]. The MC module includes electron scattering with polar optical phonons; inter- and intra-valley optical phonons; non-polar optical phonons and acoustic phonons, as

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well as ionized and neutral impurity scattering. The strain effects on bandgaps, electron effective masses, phonon deformation potentials and energies and alloy scattering have been taken into account in the InGaAs channel. The use of MC simulations is essential due to extremely non-equilibrium nature of the carrier transport in the InGaAs channel at sub 100 *nm* channel lengths. The time step of 0.1 *fs* has been adopted in this work in order to deal with the instabilities due to the high doping in the source/drain regions of the compound MOSFETs. At this stage we have not included the effect of interface roughness scattering in our simulations as we speculate that the epitaxially grown vertical layer structure possesses a good interface and possibly the introduction of very thin AlGaAs spacer above the InGaAs channel and below the gate dielectric in the compound MOSFETs will further reduce the interface roughness scattering when compared to the Si/SiO_2 interface in conventional MOSFETs. Therefore we consider that the results presented in this paper represent the upper limits of device performance.

The simulator has been carefully calibrated against the 120 *nm* pHEMTs fabricated and measured in the Nanoelectronics Research Centre at the University of Glasgow. The device structure is illustrated schematically in Fig. 2. The devices have a 22 *nm* gate-to-channel separation; a strained $In_{0.2}Ga_{0.8}As$ channel and a delta-doped layer separated from the channel by a 5 *nm* spacer. We report very good agreement between the measured and the simulated output characteristics if contact resistances are correctly introduced in the Monte Carlo simulations at the post processing stage [13].

Being confident with the results of the calibration, we have decided to study the $In_{0.2}Ga_{0.8}As$ channel MOSFET as it has the same channel composition as the calibration device. Here we have replicated the structure, the equivalent oxide thickness and the doping profiles in the source/drain as well as in the channel of the reference IBM [2] and Toshiba [10] devices. The doping profiles in the reference devices have been deduced from comprehensive calibrations using MEDICI [14]. The excellent agreement between measured and simulated device characteristics in both cases, as depicted in Fig. 4 and Fig. 5 respectively, justifies our approach. The 67 *nm* effective channel length strained Si IBM MOSFET is among the shortest devices demonstrating a drive current improvement compared to the conventional Si MOSFET. Such an improvement of 30% according to IBM justifies the introduction of this complex technology into CMOS. The 35 *nm* gate length Toshiba MOSFET was chosen as one of the best high performance device readily developed for the 90 *nm* technology node and reported at IEDM 2001.

3. Results and Discussions

The measured I_d-V_g characteristics of the conventional and strained Si IBM MOSFETs with a 67 *nm* effective channel length and the simulated characteristics of the strained InGaAs channel MOSFET with a similar structure and doping profile are compared in Fig. 6. For proper comparison the characteristics are aligned in respect of the threshold voltage to give an indication of the expected drive current under equivalent V_g-V_t conditions. The InGaAs channel devices show a 200% improvement in the drive current compared to the control silicon devices. Even when one considers all the uncertainties associated with our simulation at this stage, this improvement is very much larger than the 30% improvement observed in the strained Si channel MOSFET. The I_d-V_d characteristics of the InGaAs channel MOSFET are illustrated in Fig. 7. The significant statistical noise in the simulated current is associated with plasma instabilities in the heavily doped source/drain regions of the device. Fig. 8 illustrates the velocity profile along the channel of the InGaAs and the conventional Si MOSFET, the latter obtained also from MC simulations. It is clear that the

substantial improvement in the drive current is associated with a much higher carrier velocity in the InGaAs channel MOSFET compared to that in the channel of Si devices.

Figure 9 compares the measured I_d-V_g characteristics of the conventional Si Toshiba MOSFET with a 35 *nm* physical gate length and the simulated characteristics of the strained InGaAs channel MOSFET with similar structure and doping. In this case we observe an increase in the drain current of approximately 300% compared to the reference Si device. This shows that the InGaAs MOSFET has a greater potential for improvement with scaling compared to the conventional Si. We are currently pursuing the MC simulation of the 35 *nm* Si MOSFET in order to investigate the performance improvement due to scaling. The I_d-V_d characteristics of the 35 *nm* InGaAs channel MOSFET are illustrated in Fig. 10. Due to the smaller device dimensions and smaller number of particles we were able to carry out longer MC simulations and thus accumulate better statistics resulting in smoother curves. Finally, Fig. 11 illustrates the velocity distribution along the channel of the 35 *nm* InGaAs channel MOSFET. It can be seen by comparing with Fig. 8 the further improvement in device performance with scaling is related to the increase of the nonequilibrium channel velocity.

4. Conclusions

Using carefully calibrated ensemble Monte Carlo simulations we have demonstrated that compound MOSFETs with a InGaAs channel can deliver up to a 200% improvement in the drive current for MOSFETs with channel lengths corresponding to the present status of the CMOS technology. Also from our simulations, a further improvement in the performance could be expected with the scaling of the compound MOSFETs to dimensions corresponding to the 90 *nm* technology node and beyond.

Acknowledgements

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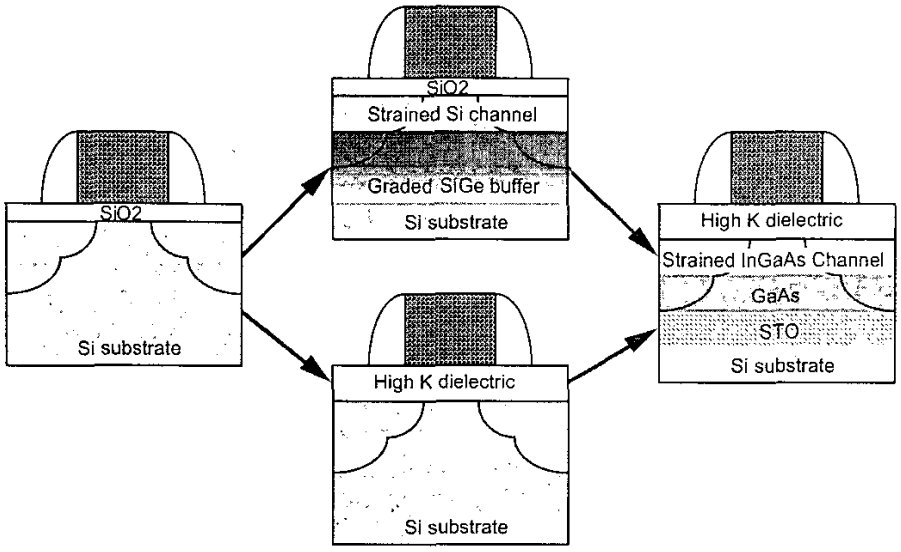

Fig. 1 Conceptual structure of a strained InGaAs channel MOSFET with high-k gate dielectric utilising GaAs on 12" Si EPIGEN™ technology.

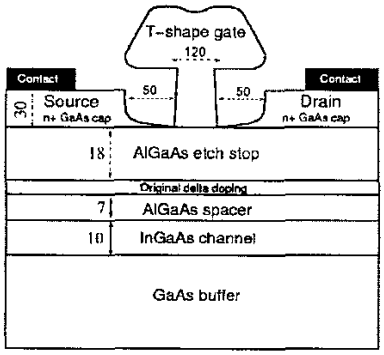

Fig. 2 120 nm gate length PHEMT used in the calibration of the Monte Carlo simulator.

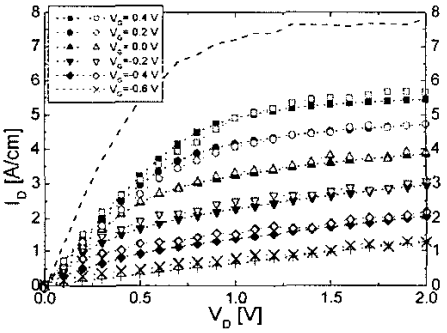

Fig. 3 Measured and simulated I_d-V_d characteristics of the PHEMT from Fig. 2.

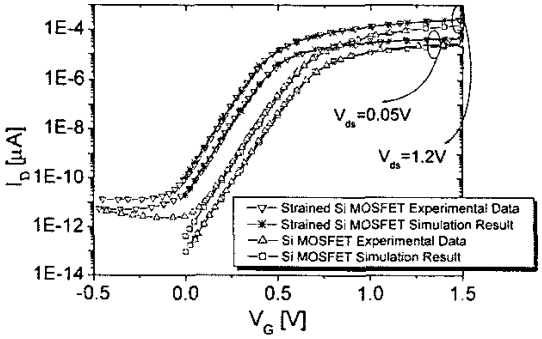

Fig. 4 Simulations of the conventional and strained Si IBM MOSFETs with a 67 nm effective channel length used to deduce the device structure and doping profiles.

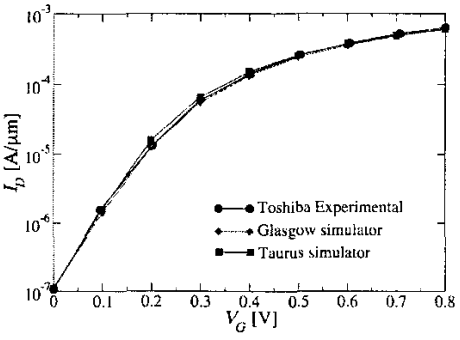

Fig. 5 Simulations of the conventional Si Toshiba MOSFET with a 35 nm physical channel length used to deduce the device structure and doping profiles.

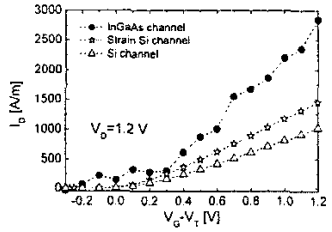

Fig. 6 Comparison of the I_d-V_g characteristics of the measured conventional and strained Si IBM MOSFETs with a 67 nm effective channel length and the simulated strained InGaAs channel MOSFET with similar structure and doping.

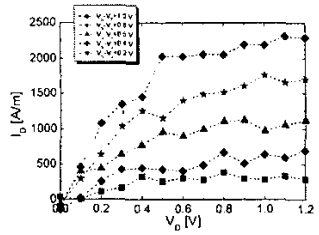

Fig. 7 I_d-V_d characteristics of the simulated strained InGaAs channel MOSFET with a 67 nm effective channel length.

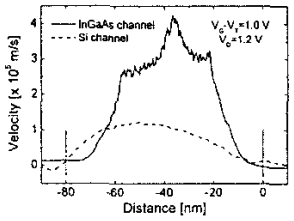

Fig. 8 Comparison of the velocity profile along the channel in the InGaAs channel and conventional Si MOSFETs with a 67 nm effective channel length.

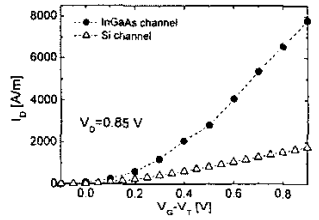

Fig. 9 Comparison of the I_d-V_g characteristics of the measured conventional Toshiba Si MOSFET with a 35 nm physical gate length and the simulated strained InGaAs channel MOSFET with similar structure and doping.

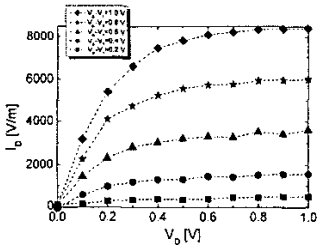

Fig. 10 I_d-V_d characteristics of the simulated strained InGaAs channel MOSFET with a 35 nm physical gate length.

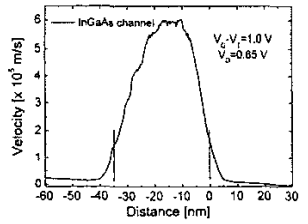

Fig. 11 Velocity profile along the channel in the InGaAs MOSFET with a 35 nm physical gate length. The position of the gate is again depicted by arrows.