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Scaling study of Si/SiGe MODFETs for RF applications

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Abstract

Based on the successful calibration on a $0.25\mu m$ strained Si/SiGe *n*-type MODFET, this paper presents a gate length scaling study of double-side doped Si/SiGe MODFETs. Our simulations show that gate length scaling improves device RF performance. However, the short channel effects (SCE) along with the parasitic delays limit the device performance improvements. We find that it is necessary to consider scaling (dimensions and doping) of both the lateral and vertical architecture in order to optimize the device design.

1. Introduction

The enhanced carrier transport in the Si/SiGe heterostructure has lead to improved device performance. Heterostructure modulation doped field effect transistor (MODFETs) with *n*-type strained Si or *p*-type Ge channels have demonstrated maximum oscillation frequencies, f_{max}, of 158GHz and 135GHz, respectively [1,2]. Compared to the conventional surface channel MOSFET, Si/SiGe MODFETs have the potential to achieve better linearity and reduced noise due to a higher quality of the channel/spacer interface. In this paper, we use an RF extraction methodology based on MEDICI [3] transient simulations to study the gate length scaling of *n*-type strained Si channel double-side doped MODFETs. Our simulations are calibrated against a $0.25\mu m$ device fabricated by Daimler Chrysler.

2. Simulation approach and calibration

2.1. RF Simulation Methodology

We use a time domain approach to extract the RF performance from numerical simulations (MEDICI). Fourier transforming the transient terminal currents provides the complex *y*-parameters [4,5], from which we may obtain the cut-off frequency f_T and, after a further transformation to *s*-parameters, the maximum frequency of oscillation, f_{max} [6]. To obtain figures of merit for a 'real' device – the raw *z*-parameters are augmented with gate and contact pad impedances (R_g, L_g, R_c, L_d and L_s). From these augmented Z^{real} an equivalent set of retransformations gives Y^{real} and hence S^{real} from which the figures of merit f_T and f_{max} can be extracted.

2.2 Calibration

Our scaling study is based on the comprehensive calibration of a $0.25\mu m$ strained Si channel *n*-type depleted MODFET using the drift-diffusion device simulator MEDICI [3]. Fig. 1 illustrates the device layer structure. The layer sequence is: a p^- substrate with ρ>1000Ωcm; a relaxed SiGe buffer with linearly graded Ge content up to 45%; a 4*nm* SiGe supply layer with a dopant concentration of $4\times10^{18}cm^{-3}$; a 3*nm* SiGe spacer; the 9*nm* strained Si channel; a 3*nm* SiGe spacer; a 3.5*nm* SiGe supply layer with a doping level of $1.5\times10^{19}cm^{-}$

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[3]; a $3nm$ SiGe cap layer and a $4nm$ Si cap layer. The T-shape Au/Pt gate is located asymmetrically with source-gate distance L_{sg}=0.2μm while total drain-source distance L_{ds}=1.5μm.

The effects of strain on the Silicon layers have been considered in the calculation of the material parameters in the MEDICI simulations: the strain causes the bands of Silicon to shift and creates splitting in the conduction and valence bands, which decreases the bandgap of the strained Silicon [7]. Consequently the electron density of states of strained Si is about 1/3 of relaxed Si due to the lowered 2-fold conduction band minima within the splitting; the calculated conduction band offset between the strain Si and the relaxed $Si_{0.55}Ge_{0.45}$ layers is approximately 170meV, providing good quantum confinement in the 2-DEG channel.

The calibration commences by extracting the low electric-field mobility parameters from I_d-V_g simulations at a low drain voltage. This is then followed by extracting the high drain I_d-V_g and I_d-V_d characteristics which enables us to determine the high-field transport parameters. Both the parallel and transverse electric field dependent mobility models have been used in this calibration and the calibrated low field mobility in the 2-DEG is 1500$cm^2/V\cdot s$. Figures 2 and 3 show the I_D-V_G and I_D-V_D characteristics (simulated and experimental) respectively and demonstrate the good agreement between measurements and simulations. However, slight discrepancies are observed at high V_G and V_D which may be attributable to self-heating [8,9]. Our simulations predict a current gain cutoff frequency, f_T, of ~24GHz, as indicated in fig. 4, also in agreement with experimental data. However, leakage in the buffer in this device causes the I_{on}/I_{off} ratio to be less than 10.

3. Scaling Study

3.1 Lateral only Scaling

Since the speed of an FET is traditionally limited by the electron transit time, the most obvious approach to improve the device speed is to reduce the gate length. However, 2-D effects due to lateral dimension scaling, *e.g.*, DIBL, affect the threshold voltage and subthreshold slope and increase the off-state current, see Fig. 5. It is also found that when the gate length is aggressively scaled (<100nm [10]), the gate begins to lose control over the channel and parasitic conduction layers which causes a saturation and possibly a reduction in transconductance and an increased drain conductance g_{ds}, see Fig. 5. These effects decrease the cutoff frequency f_T and the voltage gain G (defined as $v_{out}/v_{in}=g_m/g_{ds}$). Following the modulation efficiency (ME) definition as proposed by Foisy *et al* [11], which indicates the efficiency of the gate control on the 2-DEG, figure 6 indicates that scaling the gate-length has little effect on the ME, whereas the sheet carrier density in the channel increases due to the gate length scaling.

To achieve higher speed, the source and drain resistances, R_s and R_d, and the gate to source/drain capacitances, C_{gs} and C_{gd}, must be minimized [12]. Small R_s and R_d are also beneficial to achieve a low noise figure NF [13]. However, R_s and R_d have two major contributions, one arising from the source/drain access resistances and the second is the contact resistance. The source-drain distance L_{ds} is crucial in reducing R_s and R_d. However, reducing L_{ds} also decreases the voltage gain G due to increased drain conductance g_{ds}. It has been suggested that raising the source/drain junctions may compensate for this [10]. Scaling L_{ds} may also increase C_{gs} and C_{gd} and induce a second pronounced peak in the transconductance characteristics, see fig. 7. This is due to the increase in the current density within the Si cap layer between the source/drain and the gate at high gate bias when scaling L_{sg} and L_{ds} [14].

Figure 8 shows the effects of changing the L_{sg}/L_{ds} ratio and source-drain distance L_{ds}. It is found that for a given L_{ds}, decreasing the L_{sg}/L_{ds} ratio increases the C_{gs}/C_{gd} ratio, which will generally tend to increase f_{max}. However, in this work we find that the decrease in L_{sg}/L_{ds} also tends to increase the output (drain) conductance, g_{ds}. This increase in g_{ds} will reduce f_{max} by decreasing the effect of C_{gs}/C_{gd} on f_{max}. This effect is particular evident for the layer structures considered in this work due to their relatively high g_{ds}. The RF characteristics as a function of gate length scaling, with a L_{sg}/L_{ds} ratio $0.5\mu m/1.5\mu m$, are shown in figure 9. We have also studied the RF performance improvements with different saturation velocities as shown in figure 9. This provides an indication that the effect of velocity overshoot may also lead to an improvement in the RF performance.

3.2 The Optimization of the Vertical Structure

The optimization of the vertical structure may help to improve device performance and suppress some 2-D effects due to gate length scaling. The layer thickness and supply layer doping levels affect the ME; the layer thicknesses associated with the 2-DEG are crucial to the quantum confinement in the channel. The gate to channel distance requires careful consideration to improve the control the SCE effects introduced by scaling. Optimization of the vertical structure is also required to suppress parasitic conduction which makes it difficult to keep good linearity at high gate bias.

Figure 10 illustrates the effect of channel thickness on the sheet carrier density, obtained from 1-D Poisson-Schrödinger solutions, and the ME (inset). Although the peak concentration increases with decreasing channel thickness, the sheet carrier density reduces. It is also found that too large a channel thickness causes carriers to move away from the gate, which increases output conductance g_{ds}.

Reducing the Si and SiGe cap layer thicknesses improves the control of the gate on the device. However, reducing the SiGe cap layer thickness leads to an increase in parasitic conduction within the Si cap. Shrinking the SiGe spacer layer increases the ME and the sheet carrier density in the channel, but also reduces the mobility within the channel due to an increase in remote ionized impurity scattering [14].

The ME, threshold voltage shift and the sheet carrier density are sensitive to the doping concentration and layer thickness of the front supply layer [15], this is illustrated in figure 11 for ME and sheet carrier density. The RF characteristics versus gate length with a reduced gate-to-channel distance is presented in figure 12. Here we observe that the reduction of the extracted intrinsic capacitance (the sum of C_{gs} and C_{gd}) offsets the negative effect of the DIBL induced reduction of g_m on f_T [10]. Such reductions in g_m limit f_T during the gate length scaling.

4. Conclusions

Gate length scaling of *n*-channel RF Si/SiGe MODFETs, along with the lateral and vertical structure optimization have been studied. It is necessary to optimize both the lateral and vertical architectures in order to achieve RF performance improvements in sub-100nm devices. Parasitic effects are becoming increasingly important with gate length scaling, which together with the 2-D effects, limit the device performance improvements. The velocity overshoot in an aggressively scaled device is expected to overwhelm the parasitic effects [16] to the device performance; further studies will be required to confirm this.

Acknowledgements
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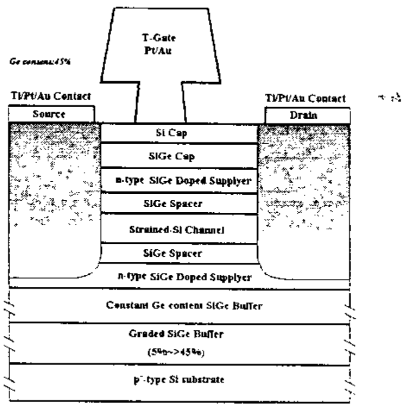

Figure 1: Schematic illustration of the 0.25μm MODFET studied in this work.

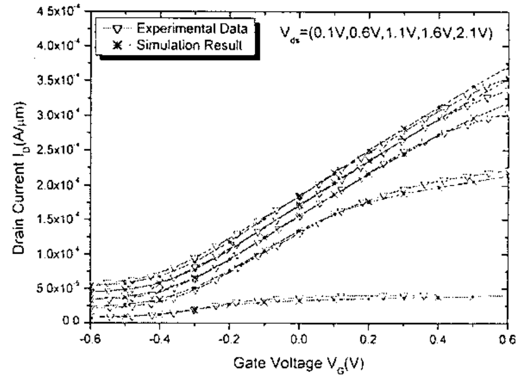

Figure 2: I_D-V_G current characteristics, both experimental (triangles) and simulated (stars) for the 0.25μm MODEFT.

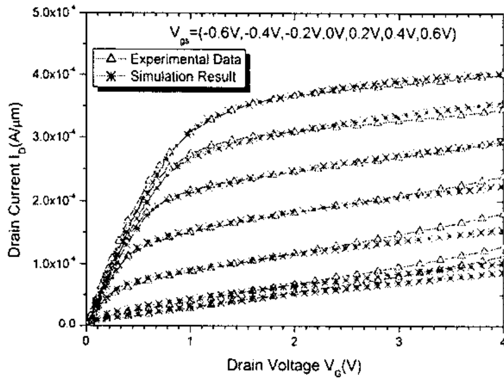

Figure 3: I_D-V_D current characteristics, both experimental (triangles) and simulated (stars) for the 0.25μm MODEFT.

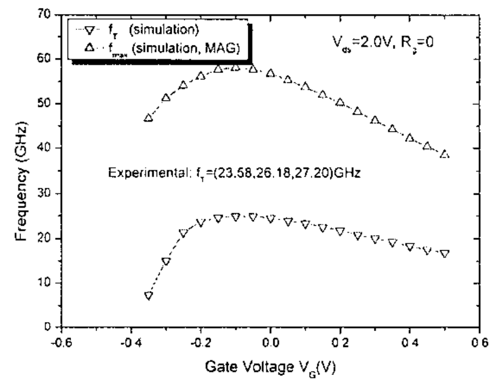

Figure 4: RF characteristics, f_T and f_{max} (maximum available gain) obtained from our simulations. The available experimental data is given in brackets.

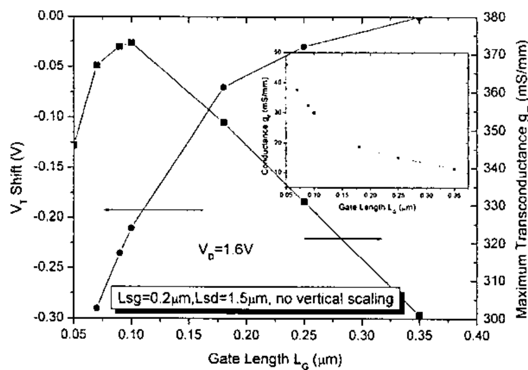

Figure 5: Threshold voltage shift and transconductance characteristics versus the gate length; the inset is the output conductance characteristic.

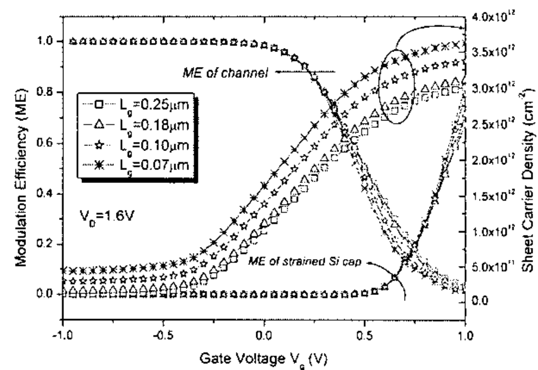

Figure 6: Effects of gate length scaling on the modulation efficiency and the sheet carrier density in the channel.

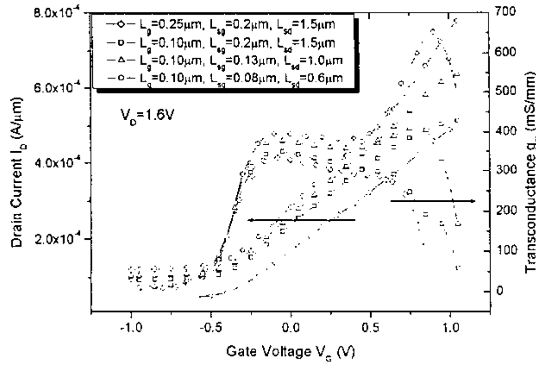

Figure 7: Current and transconductance characteristics with different lateral scaling strategy (no vertical scaling).

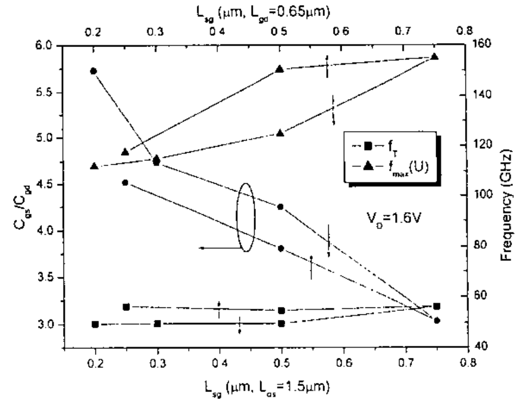

Figure 8: Effects of different L_{sg}/L_{ds} ratios on the device characteristics (L_g=0.1*μm*; all values are extracted from the MEDICI transient simulation without R_g, R_d and R_s).

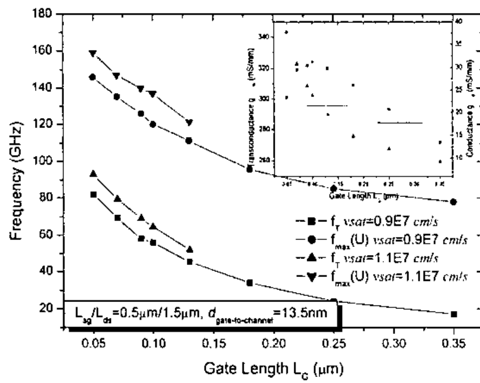

Figure 9: Intrinsic RF characteristics versus the gate length at V_{ds}=1.6V, the gate-to-channel distance=13.5*nm*; the inset is the transconductance and output conductance versus the gate length.

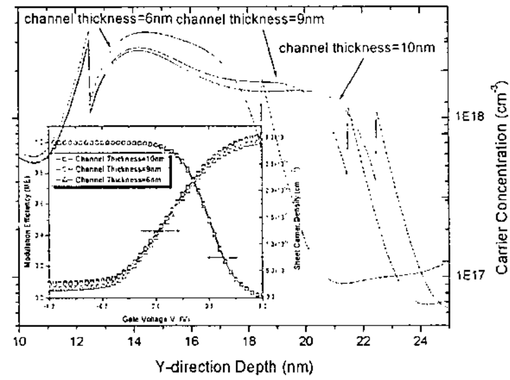

Figure 10: Effect of channel thickness on the carrier concentration (from Poisson-Schrödinger solution); the inset is the effect on the modulation efficiency and the sheet carrier density in the channel.

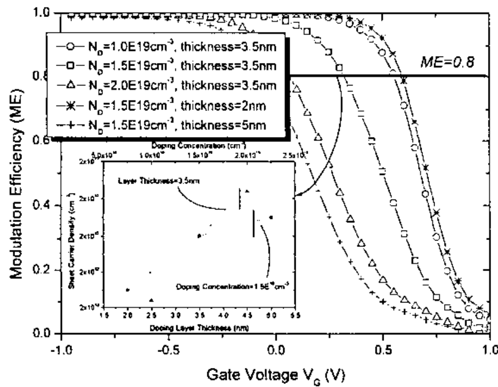

Figure 11: Effects of front supply layer thickness and doping concentration on the modulation efficiency and the sheet carrier density in the channel.

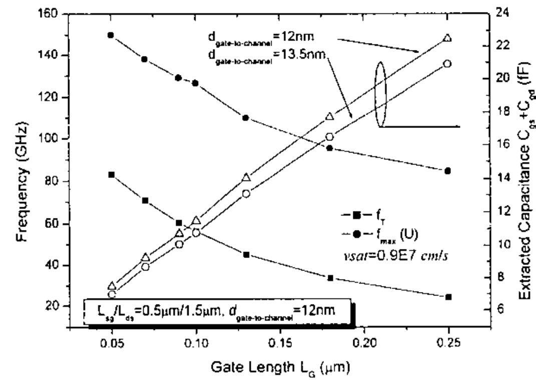

Figure 12: Extracted intrinsic RF characteristics and capacitance (C_{gs}+C_{gd}) versus the gate length at V_{ds}=1.6V, the gate-to-channel distance=12*nm*.