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Integrating 'atomistic', intrinsic parameter fluctuations into compact model circuit analysis.

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Abstract:

MOSFET parameter fluctuations resulting from the 'atomistic' granular nature of matter, are predicted to be a critical roadblock to the scaling of devices in future electronic systems. A methodology is presented which allows compact model based circuit analysis tools to exploit the results of 'atomistic' device simulation, allowing investigation of the effects of such fluctuations on circuits and systems. The methodology is applied to a CMOS inverter, ring oscillator, and analogue NMOS current mirror as simple initial examples of its efficacy.

1. Introduction

There is considerable interest in intrinsic parameter fluctuations, caused by differences between otherwise macroscopically identical devices. A growing body of research is aimed at predicting the nature and magnitude of these 'atomistic' fluctuations due to, amongst other things, channel dopant number and position variation, oxide thickness variation, and line edge roughness [1,2]. Such fluctuations, for example in V_t and I_{off}, will become steadily more pronounced as devices continue to scale. Although channel engineering methods have been presented as a short term palliative to restrain these fluctuations, some of the suggested solutions work against device short channel performance [3]. In circuits, parameter fluctuations ultimately lead to component mismatch and it is now widely realised that this problem may constitute a critical roadblock to the future performance and yield of both analogue and digital CMOS systems [4-6]. Figure 1 clearly illustrates potential variations in a MOSFET due to random dopant position in the channel, source and drain, which may lead to such macroscopic fluctuations between devices.

To create circuits which are efficient, and remain robust in the presence of intrinsic fluctuations, designers require more than a worst-case estimate of fluctuation magnitude. Ideally, they require a device model which integrates naturally with present circuit analysis and electronic design automation (EDA) tools, and describes the effect of fluctuations over the whole range of device operation – i.e. a set of compact models encompassing the appropriate physics of fluctuations, but reducing calculation time in an EDA tool by several orders of magnitude from that which would be required using present statistical, 3D device simulations.

2. 'Atomistic' Parameter Fluctuations

In addition, intrinsic fluctuations resulting from the microscopic sources, may have a quite different nature to the traditional process related parameter fluctuations. For instance, differing channel dopant configurations will have a marked effect in sub-threshold, but relatively minor effect in saturation. Thus it is vital to have a methodology specifically tailored to study the impact of different sources of intrinsic parameter fluctuations at circuit analysis level. This will allow us to investigate their effect, both separately and in combination, on the operation of circuits and systems.

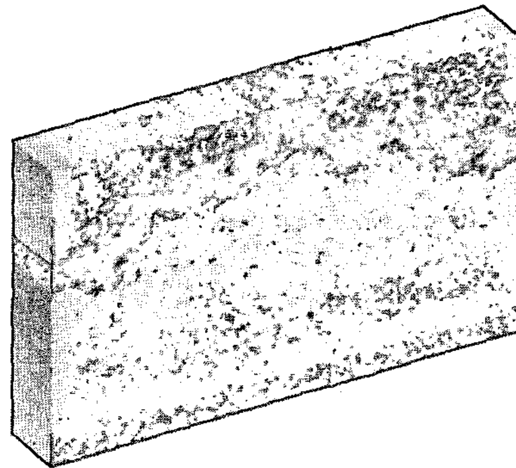

Fig. 1 Variation in potential in a 35 nm MOSFET due to detailed positions of dopants in the channel, source and drain. After [7].

In order to better understand the implications of intrinsic 'atomistic' fluctuations independent of experimental process variations, an ensemble of 100 macroscopically identical, but microscopically different devices is created and simulated using the Glasgow 'atomistic' device simulator – which can correctly account for fluctuations introduced by discrete random doping distributions in the MOSFET channel, source and drain. The ensemble, which is used as source data for the rest of the extraction methodology, is based on the continuous doping profile of a 35 nm nMOSFET [8], to which the simulator is rigorously calibrated. The details of this calibration are

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presented elsewhere [7]. Figure 2 shows typical I_D-V_G characteristics selected from the ensemble.

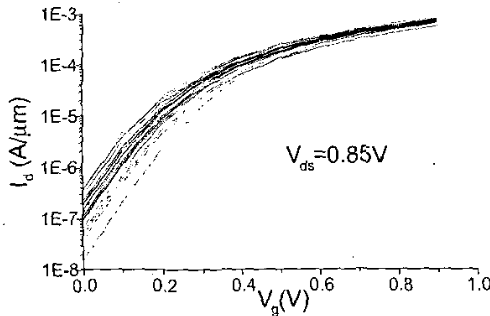

Fig. 2 Gate characteristics from 100 macroscopically identical 35 nm nMOSFETs, obtained by 'atomistic' device simulation.

We present, in section 3, an optimised methodology for extracting an ensemble of compact model parameters from statistical data produced by either experiment or device simulation.. In sections 4 and 5 we apply the methodology to analyse the performance of foundational circuits for both digital and analogue applications.

3. Methodology

The extraction process is completed in two phases. Firstly, a complete set of BSIM3v3 model parameters is extracted from the IV characteristics of a typical device with a continuous doping profile, and the parameters divided into two groups: those sensitive to 'atomistic' fluctuations, and those insensitive to 'atomistic' fluctuations, which are fixed after this phase. A combination of local optimisation and a group extraction strategy is employed to extract the whole set of BSIM3v3 parameters using the Synopsys tool AURORA, focussing on those critical to long channel behaviour, the threshold voltage in the short channel regime, and drain current response in the presence of high fields. Figures 3 and 4 show the quality of the BSIM3v3 parameter extraction results obtained for a typical 35 nm nMOSFET. The symbols are experimental results [8].

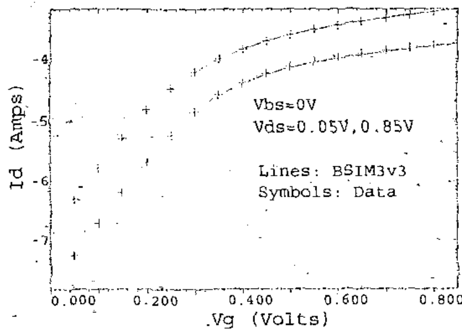

Fig. 3 Compact model calibration of gate characteristics for single 35 nm nMOSFET.

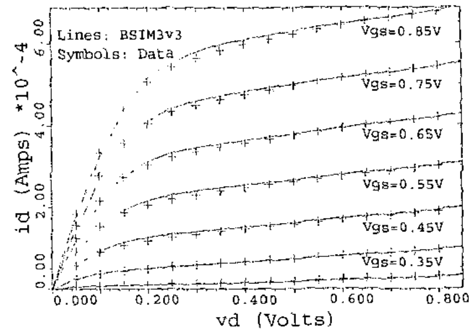

Fig. 4 Compact model calibration of drain characteristics for single 35 nm nMOSFET.

From the device operation point of view, 'atomistic' dopant fluctuations in the channel, source and drain have three crucial effects. They cause significant drain current and sub-threshold slope variation in the weak inversion regime. They cause significant threshold voltage fluctuations, and they introduce some I_{on} variation. Although the BSIM3v3 model does not directly consider these effects, it does introduce a number of empirical parameters to model different process conditions. Through careful parameter extraction, these parameters may be tuned to model the results of random doping effects. In principle, therefore, we can use BSIM3v3 in a second phase of analysis by choosing a basis set of model parameters and modelling each member of the statistical ensemble with extracted values for these parameters. In this work, seven key BSIM3v3 model parameters are chosen to represent the effect of random discrete dopants; N_{ch}, N_{factor}, V_{off}, a_0, a_1, a_2, and d_{sub}. Figure 5 shows the variation of the three most important of these parameters. N_{ch} is the effective channel doping, which will affect the model's threshold voltage, V_{off} will significantly affect the sub-threshold slope, and a_0 directly affects the drain saturation voltage.

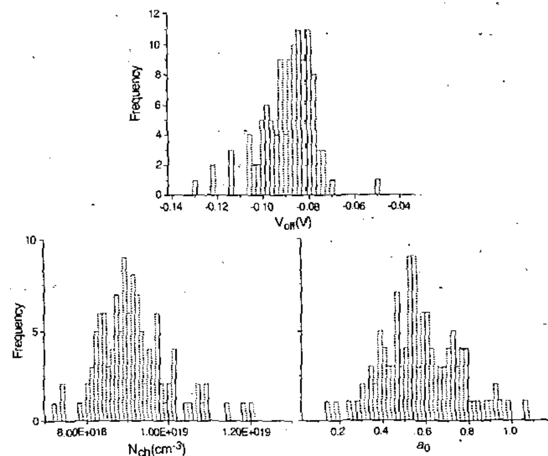

Fig. 5 Distributions of critical BSIM3.3 parameters over an ensemble of 100 compact models calibrated to gate and drain characteristics of the devices in figure 4.

In this second phase of extraction, parameters are tuned by first considering gate characteristics at low drain bias to match device threshold voltage and sub-threshold slope. Then the saturation regime is matched at high drain bias. The quality of the extracted compact models are equivalent to those of figure 3.

Compared to other statistical compact modelling methodologies, the advantage of this two phase extraction strategy is that it can guarantee compact models which closely match the real ensemble of device results, whilst remaining feasible for the large ensemble sets necessary to obtain statistical circuit information.

As an initial application of this methodology, we consider the distribution of propagation delays found in a simple inverter circuit subject to 'atomistic' fluctuations. One hundred circuits are simulated using HSPICE, with nMOSFETs from our ensemble, and continuously doped pMOSFETs calibrated from [8]. The pMOSFETs have width scaled ×2.5 to match the nMOSFET drive current. Because of this symmetry, it can be seen that the modelled circuits will have a standard deviation $\sqrt{2}$ less than a complete simulation with 'atomistic' p and nMOSFETs. The input signal is from an ideal source with rise and fall times of 5 ps, and a load of 5 fF. Inverter delay is measured at 50% of supply voltage. Results are shown in figure 6, and it can be seen that in this, best possible case scenario, the circuit has an average propagation delay of 10.9 ps. The graph has a standard deviation of 1.3 ps.

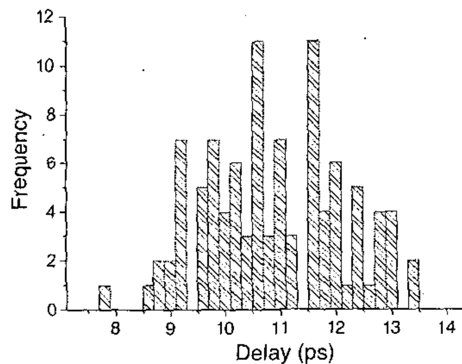

Fig. 6 Distribution of circuit delays for inverter circuits incorporating nMOSFETs from 'atomistic' ensemble.

4. Ring Oscillator

The simplest CMOS circuit for timing tests is the ring oscillator – and the circuit diagram of a five stage oscillator is shown in figure 7. This circuit will give an indication of the performance of inverters in practice, when driven and loaded realistically. The inverters themselves are modelled as above, with interconnect capacitances assumed to be negligible.

The results of circuit simulations on this system are shown in figure 8. The average period of the whole five stage circuit is 150.6 ps with $\sigma = 4.2$ ps, equivalent to a frequency of 6.6 Ghz with $\sigma = 0.1$ Ghz, and a five stage delay of 75.3 ps with $\sigma = 2.1$ ps. When accounting for more realistic inverter loads, and more importantly, the finite I_{on} available in inverters as drivers, the single stage delay increases from 10.9 ps to 15.1 ps. In addition the standard deviation of the delay, naïvely calculated from a single inverter stage (assuming independence of the variations of each inverter stage) as $\sqrt{5} \times 1.3$ ps = 2.9 ps compares well with the actual variation of 2.1 ps.

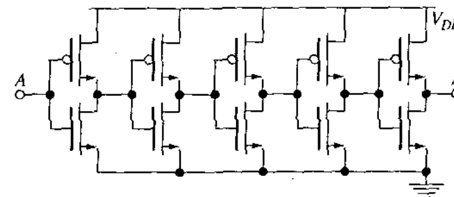

Fig. 7 Five-stage ring oscillator circuit.

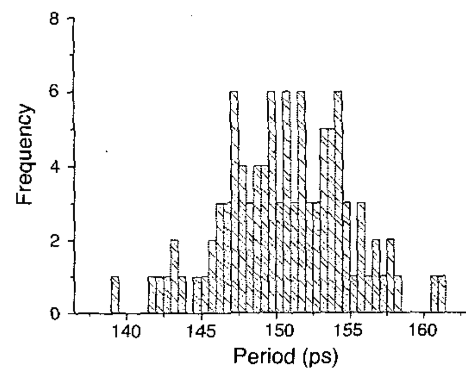

Fig. 8 Distribution of minimum period for ring oscillator incorporating nMOSFETs from 'atomistic' ensemble.

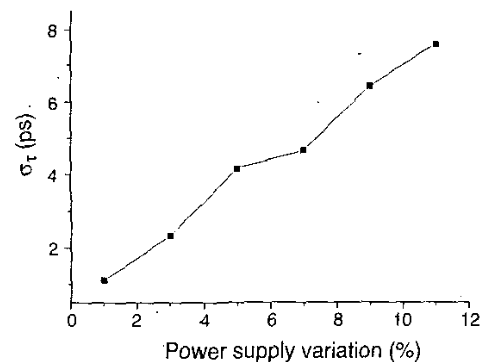

Fig. 9 Distribution of circuit delays for inverter circuits incorporating nMOSFETs from 'atomistic' ensemble.

Deviations in propagation delays due to 'atomistic' effects are modest. This is as expected, not only because the averaging effect of the ring oscillator stages, but also because the period is substantially dependant on drive current, which, due to screening in strong inversion, is relatively resistant to 'atomistic' fluctuations. It is emphasised in figure 9, which shows the standard deviation in period caused by power supply instability. 'Atomistic' ring oscillator fluctuations for 35 nm nMOSFETs are of the same order as fluctuations caused by a 5% supply instability.

5. Current Mirror

To demonstrate the effects of 'atomistic' fluctuations in a simple analogue circuit, a four nMOSFET transistor cascode current mirror, shown in figure 10, is chosen.

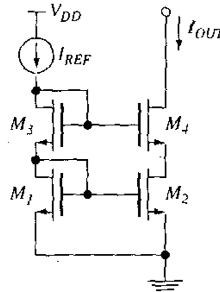

Fig. 10 Cascode NMOS current mirror circuit.

Figure 11 shows the I_{out} variation on an output voltage change (the voltage at the drain of M_1) of 0.5V. The variation is minimal, suggesting that 'atomistic' fluctuations do not significantly affect device output resistance in saturation.

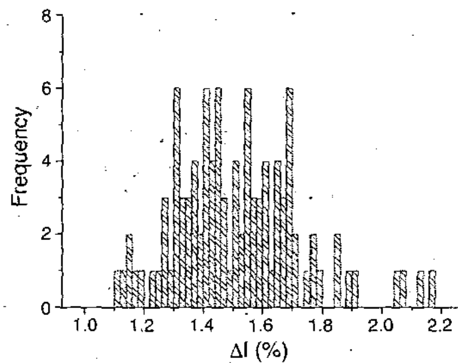

Fig. 11 I_{out} variation distribution on a V_{out} change of 0.5V, for Cascode NMOS current mirror.

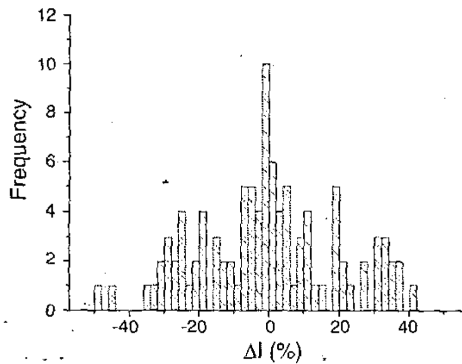

Fig. 12 Mismatch between I_{ref} and I_{out} distribution for Cascode NMOS current mirror.

However, transistor matching through V_t is critical for analogue circuit design, and fluctuations will introduce pronounced mismatch between macroscopically identical devices. Figure 12 clearly shows this effect; the mismatch distribution between I_{ref} and I_{out} is spread from -40% to +40%, reflecting a large threshold fluctuation due to random dopants.

6. Conclusions

We have presented a methodology for integrating the results of 'atomistic' parameter fluctuations into compact model ensembles, for investigation of analogue and digital circuits using devices in the nanometre regime. This methodology will allow analysis of the effects of a range of 'atomistic' phenomena – both singly and in combination – on circuits and systems. We have shown examples of this methodology applied to CMOS inverter and ring oscillator circuits, and to an analogue NMOS current mirror.

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