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Optimizations of sub-100*nm* Si/SiGe MODFETs for high linearity RF applications

L. Yang, A. Asenov, M. Boriçi, J. R. Watling, J. R. Barker, S. Roy, K. Elgaid, I. Thayne and T. Hackbarth

Abstract - Based on careful calibration in respect of 70nm n-type strained Si channel Si/SiGe modulation doped FETs (MODFETs) fabricated by Daimler Chrysler, numerical simulations have been used to study the impact of the device geometry and various doping strategies on device performance and linearity. The device geometry is sensitive to both RF performance and device linearity. Doped channel devices are found to be promising for high linearity applications. Trade-off design strategies are required for reconciling the demands of high device performance and high linearity simultaneously. The simulations also suggest that gate length scaling helps to achieve higher RF performance, but decreases the linearity.

I. INTRODUCTION

High mobility Si/SiGe MODFETs have been widely studied for high frequency and low-noise applications. Similar to their III-V counterparts, the Si/SiGe MODFETs have a strained channel which enables high mobility and high sheet carrier density. Moreover, the compatibility of Si/SiGe MODFETs with existing Si technology makes them promising candidates for system-on-chip applications. 100*nm* Si/SiGe MODFETs with cut-off frequency, f_T, of 74GHz and maximum oscillation frequencies, f_{max} of 158GHz at room temperature, have been successfully demonstrated [1], [2]. However, little work has been done to optimize such devices for communication applications, bearing in mind that power amplification for wideband communications requires high linearity to minimize the intermodulation distortion.

In this paper, we use numerical simulations to optimize the Si/SiGe MODFET device architecture for high linearity RF applications. The simulations are based on extensive calibration in respect of a 70*nm* *n*-type buried strained Si channel Si/SiGe MODFET fabricated by Daimler Chrysler. The linearity has been found to be sensitive to the doping strategy, the vertical layer structure and the lateral device design. In agreement with previously published work on III-V HEMTs [3], we have found that the doped channel devices have better linearity compared to their side-doped counterparts. However, the channel doping reduces the mobility resulting in lower drive current, along with reduced transconductance and RF performance. This requires a careful trade-off design balancing between high RF performance and high linearity. We have also carried out a scaling study based on our previous work [4]. The simulations show that the proper scaling results in improved RF performance, but has a negative impact on the linearity.

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II. SIMULATION METHODOLOGY

Simulations are carried out using the drift-diffusion device simulator MEDICI [5]. A time domain approach has been used to extract the RF performance [6], [7]. As a figure of merit for the linearity of investigated devices, we have adopted a classical approximation of PIP3, which represents the input signal power leading to excess third-order intermodulation [8]:

$$PIP3 = \frac{4g_m}{g_{m2}R_s}, \qquad (1)$$

where g_m is the transconductance, g_{m2} is the second derivative of g_m in respect of the gate voltage (V_g), and R_s=50Ω is the load resistance.

Possion-Schrödinger solutions have been used to understand properly aspects of the device operation related to quantum confinement in the channel. Comprehensive calibration in respect of 70*nm* *n*-type Si/SiGe MODFETs fabricated by Daimler Chrysler precedes the simulation study. The calibration methodology has been published elsewhere [4]. The layer stack of the calibrated 70*nm* MODFET was grown by molecular beam epitaxy (MBE) on a graded $Si_{0.55}Ge_{0.45}$ virtual substrate grown by low energy plasma enhanced chemical vapor deposition (LEPECVD). The layer sequence (from bottom to top) of the calibrated device is: a p^- substrate with ρ>1000Ω*cm*; a relaxed SiGe buffer with linearly graded Ge content up to 45%; a 5*nm* SiGe supply layer with a dopant concentration of $2.5\times10^{18} cm^{-3}$; a 3.5*nm* SiGe spacer; the 9*nm* strained Si channel; a 3*nm* SiGe spacer; a 5*nm* SiGe supply layer with

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a doping level of $1.0\times10^{19}cm^{-3}$; a $6nm$ SiGe cap layer and a $2nm$ Si cap layer. The T-shape Au/Pt gate is located with a source-gate distance of L_{gs}=0.5μm while the total drain-source distance is L_{ds}=1.0μm.

Fig. 1 which shows the I_D-V_G characteristics demonstrates good agreement between measurements and simulations. The slight discrepancies at high V_D can be attributed to self-heating effects which are not included in our simulations [9].

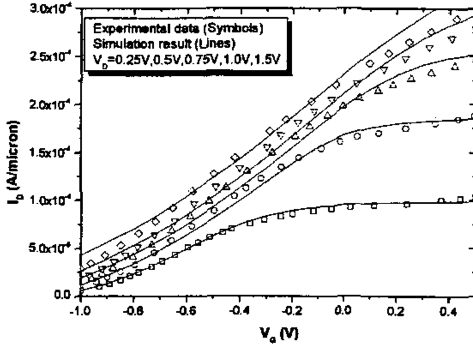

Fig. 1. I_D-V_G characteristics of simulated and experimental data.

High mobility undoped channel MODFETs aiming for the high frequency applications require high sheet carrier density and good control of the gate on the channel. However, the achievement of high linearity requires widening of the operating range of the gate control. Therefore, for high linearity applications, aspects of the design which generate high channel mobility can be sacrificed to balance between the high linearity and high speed designs.

In this work, the traditional side doping strategies aiming for high mobility in the undoped channel are combined with various channel doping scenarios to investigate the impact on linearity. Three different devices with identical layer structures have been studied in this paper. Structure A is the original MODFET used in the calibration process, with double side SiGe doping layers and an undoped channel. Structure B is the MODFET with a reduced side doping above the channel compensated by an equivalent amount of channel doping, 1×10^{18}cm^{-3}. Structure C is the doped channel FET (DCFET) without side doping and with a channel doping, 6×10^{18}cm^{-3}. The channel doping is limited in the central 5nm of the channel.

III. Impact Of The Device Geometry

In the investigation of Si/SiGe MODFETs, improving the performance necessitates the optimization of device geometry in order to achieve better quantum confinement and good modulation efficiency, resulting in high density and high mobility of the carriers in the channel. However, the existence of low-mobility parasitic conduction paths in these devices limits the device performance and range of operation. At high current levels, the carrier density in the low mobility slab doping layers above the channel increases, screening further modulation of the channel carrier concentration, which in turn limits the device linearity and also degrades device performance.

The gate-to-channel distance is the key parameter which affects the gate control on the conduction layers. The decrease of the gate-to-channel separation helps to achieve high transconductance and better RF performance [4]. However, small gate-to-channel separations degrade device linearity by compressing the transconductance. As shown in Fig. 2, the devices with small gate-to-channel separations have lower PIP3 representing worse linearity performance, while having enhanced transconductance.

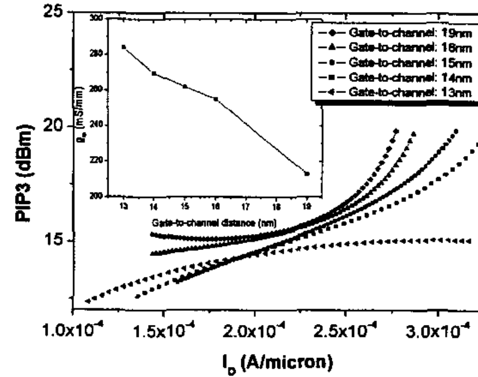

Fig. 2. The device PIP3 and transconductance (the inset) characteristics with different gate-to-channel distances.

The lateral device design also affects the linearity. The source-drain distance in the devices investigated is larger than the physical gate length in order to reduce the gate-to-contact parasitic capacitances, and increase the breakdown voltage. The transconductance is sensitive to the changes of lateral dimensions as they affect the series resistance. The source series resistance changes the shape of the I_D-V_G characteristics and therefore affects the linearity. Fig. 3 shows that although increasing the source-gate separation degrades the transconductance and drive current, it flattens the transconductance characteristics and does help to improve linearity.

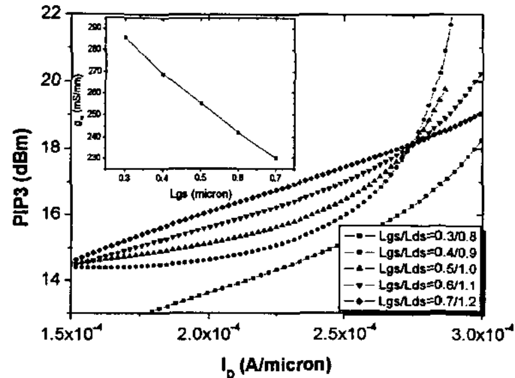

Fig. 3. The device PIP3 and transconductance (the inset) characteristics with different L_{gs}.

IV. CHANNEL DOPING STRATEGIES

Parallel parasitic channel conduction of the MODFETs is the major factor that affects linearity. The carriers supplied by the side doping layers may move from the channel to the low mobility parasitic conduction path at high gate voltages, which narrows the transconductance peak and reduces the linearity.

Existing work on III-V HEMTs has suggested that the introduction of channel doping improves linearity [3]. Transferring this idea into the Si/SiGe MODFETs, we also expect an increased linearity due to the doped channel. Compared with the side doped devices, the carriers in the doped channel devices stay in the channel for large gate voltages, which flattens the transconductance characteristics and improves the linearity, as illustrated in Fig. 4.

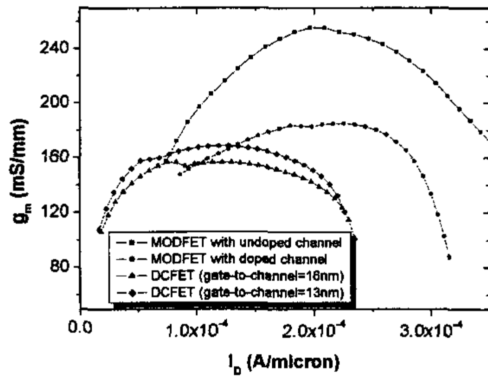

Fig. 4. The comparison of device transconductance characteristics between structure A (undoped channel MODFET), structure B (doped channel MODFET) and structure C (DCFET).

Fig. 5 shows that the linearity of doped channel devices is distinctly improved compared to that ofundoped channel devices, while the undoped channel devices have higher drive current.

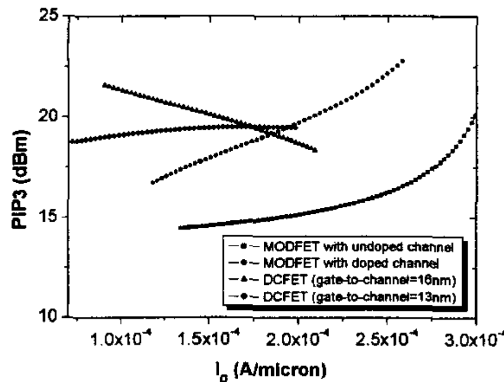

Fig. 5. The comparison of PIP3 between structure A (undoped channel MODFET), structure B (doped channel MODFET) and structure C (DCFET).

For FET-type amplifiers under small signal operation, distortion related to nonlinearities in the transconductance, g_m, is complemented by distortions associated with nonlinearities in the coupling capacitances, C_{gs}, C_{gd} and C_{ds}. From transient simulations, we have extracted and compared the voltage dependence of these intrinsic small-signal equivalent circuit parameters [4] (see Fig. 6) between structure A (MODFET, see table 1) and structure C (DCFET). It can be seen from the Fig. that in a large operation range, the capacitances of structure C are more linear than that of structure A, which contributes to the high linearity of doped channel MODFETs.

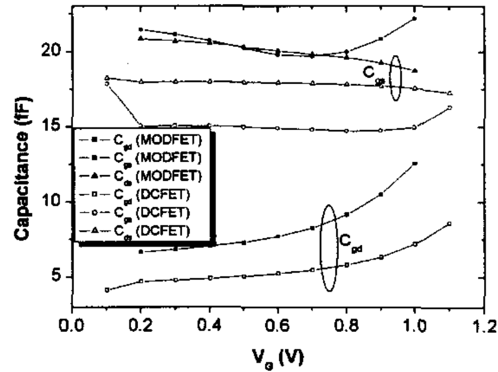

Fig. 6. The comparison of intrinsic capacitances between structure A (undoped channel MODFET) and structure C (DCFET) at V_D=1.5V.

However, figures 4 and 5 show that the drive current and the peak transconductance of doped channel MODFETs are much smaller than that of undoped channel devices due to the lower mobility within the channel. Although the doping in the channel provides a high sheet carrier density, the mobility is significantly lower than that of the undoped channel due to strong ionized impurity scattering. Using a 1-D Poisson solution, Table I compares the sheet carrier densities, n_s, in the channel, drain current, I_D, transconductance, g_m, intrinsic capacitance, $C_{gs}+C_{gd}$, and intrinsic f_T at V_G=0.4V. Even with a much lowered g_m, the doped channel MODFET achieved relatively high f_{Ti} (intrinsic f_T) because of reduced gate capacitance $C_{gs}+C_{gd}$.

TABLE I

COMPARISONS OF SHEET CARRIER DENSITY IN THE CHANNEL n_s ($\times10^{12}$ cm^{-2}), I_D ($\times10^{-4}$ $A/\mu m$), g_m (mS/mm), INTRINSIC CAPACITANCE (fF) AND INTRINSIC f_T (GHZ) BETWEEN THE DOPED AND UNDOPED CHANNEL MODFET S

Structure	n_s	I_D	g_m	$C_{gs}+C_{gd}$	f_{Ti}
A	2.18	2.8	231	27.7	83.8
C	1.91	1.4	156	18.9	69.7

V. THE IMPACT OF SCALING

When the device is laterally scaled, the RF performance is improved, as illustrated in Fig. 7. In the simulations, the drain voltage, V_D=1.5V, the mobility and

the saturation velocity are assumed to be the same during scaling. Nevertheless, 2-D effects due to lateral dimension scaling mainly associated with DIBL affect the threshold voltage and subthreshold slope and increase the off-state current. During the gate length scaling, the intrinsic gate capacitance $C_{gs}+C_{gd}$ is monotonically reduced. The transconductance starts to decrease at L_g=~90nm [10] (see Fig. 7 and the inset), which is due to poor gate control over the channel and parasitic conduction layers. Considering the expected velocity overshoot in very short channel devices, the RF performance should be improved more than our prediction in Fig. 7 which is based on drift diffusion simulations with a constant saturation velocity [5].

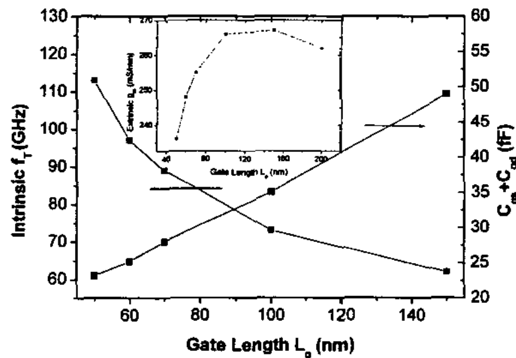

Fig. 7. The intrinsic f_T and capacitance characteristics of different gate length; the inset is the transconductance characteristics (both at V_D=1.5V).

Unfortunately, the gate length scaling doesn't help us to achieve better linearity. For conventional CMOS devices [11], PIP3 starts to decrease when the device is scaled into the deep submicron regime and eventually rises at very small gate length (<100nm). In our simulations, the modulation doped device behaves similarly to the traditional MOSFET, as illustrated in Fig. 8.

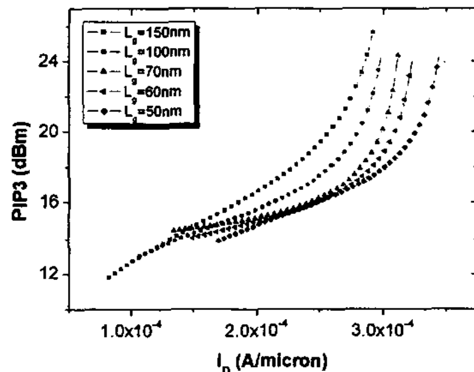

Fig. 8. The device PIP3 characteristics with different L_g.

In the simulations, we have preserved the vertical structure, the mobility, series resistance and saturation velocity during the scaling. If the vertical scaling is also considered, RF performance may be increased even more [4], while device linearity will be decreased due to smaller gate-to-channel separation.

VI. CONCLUSION

We have studied the RF performance and the linearity in various Si/SiGe MODFETs architectures. The gate-to-channel separation and gate to source/drain distances were found to have significant but opposite effects on device performance and linearity. The doped channel device exhibits the best linearity but at the expense of reduced drive current, transconductance and RF performance. The simulations also show that scaling helps to improve RF performance, but slightly reduces the device linearity. Trade-off designs are necessary for specific RF and/or high linearity applications.

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