Sub-100nm strained Si CMOS: Device performance and circuit behavior

L. Yang*, J. R. Watling, A. Asenov, J. R. Barker, and S. Roy
Device Modelling Group, Department of Electronics and Electrical Engineering,
University of Glasgow, Glasgow G12 8LT, UK
*E-mail: lfang@elec.gla.ac.uk, Tel: +44 141 330 4792, Fax: +44 141 330 4907

Abstract

Using comprehensive device simulations, performance enhancement of sub-100nm strained Si MOSFETs has been investigated. Circuit behavior of conventional Si, strained Si, conventional Si SOI and strained SOI ring oscillators has been assessed.

1. Introduction

The scaling of Si MOSFETs beyond the 90nm technology node requires performance boosters in order to satisfy the requirements of the International Technology Roadmap for Semiconductors (ITRS) [1]. Among the potential solutions outlined in the 2003 edition [1], transport enhanced FETs utilizing strained Si (SSi) channel are amongst the more mature technologies, having already demonstrated enhanced device and circuit performance [2,3,4,5,6].

This paper studies device performance and circuit behavior of sub-100nm strained Si CMOS employing a comprehensive simulation methodology. The simulations, using commercial simulator MEDICI [7] with Drift-Diffusion (DD) and Hydrodynamic (HD) models and our Ensemble Monte Carlo (EMC) simulator, are based on the calibrations in respect of sub-100nm n- and p-type Si and SSi MOSFETs fabricated by IBM [2,8].

2. Device structure and simulation methodology

The SSi device structures used in this study are based on the 67nm effective gate length IBM devices, which are illustrated in figure 1 featuring a SSi/SiGe heterostructure. The conventional Si (Si) devices, which are used for comparison, have the same device dimensions and doping profiles as their SSi counterparts. The 67nm n-type IBM strained Si MOSFET has a 2.2nm SiO_2 gate dielectric and a 10nm SSi channel grown on a relaxed $Si_{0.85}Ge_{0.15}$ buffer. The 67nm effective gate length p-type IBM SSi MOSFET features a 90nm physical gate length and a $SSi/Si_{0.72}Ge_{0.28}$ heterostructure. The band structure along a vertical slice through the middle of device is illustrated in figure 1, where the band offsets at both the conduction and valence bands are induced by the strain in the channel.

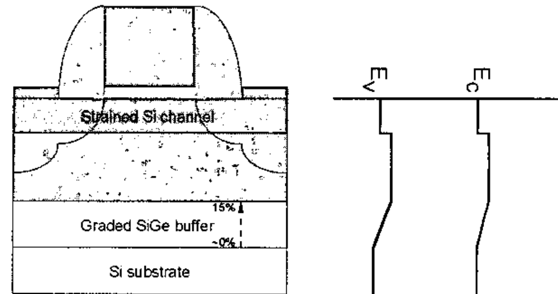

Figure 1. Schematic illustration of the SSi MOSFET structure and the corresponding band profiles

Using MEDICI, n- and p-type Si and SSi MOSFETs are calibrated against the experimental device characteristics, as shown in figure 2. Concentration-dependent, Caughy-Thomas lateral field-dependent and perpendicular field-dependent mobility models along with a simple quantum correction model [7] and correct parameters for the SSi/SiGe heterostructure [9] are used in the calibrations in order to determine the physical device structure.

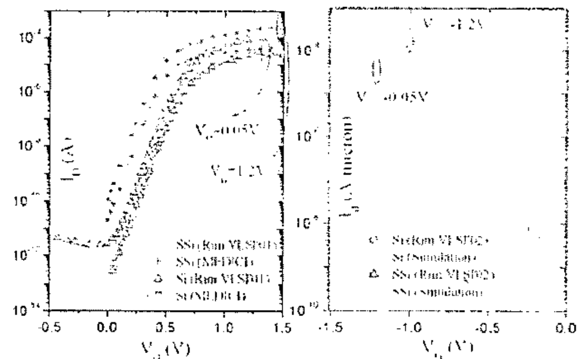

Figure 2. Calibrated I_D-V_G characteristics of the n- and p-type Si and SSi MOSFETs

As shown in figure 2, the n-type and p-type SSi MOSFETs exhibit 35% and 10% drive current enhancement over their Si counterparts, respectively. The threshold voltage difference observed between the Si and SSi devices are due mainly to the strain induced band structure change [2,8]. The calibrated device information is then used to investigate the performance

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enhancement of SSi MOSFETs for CMOS applications by employing MC and HDM device simulations in the simulations of n-type and p-type SSi MOSFETs respectively. MEDICI mixed mode simulations are also used to assess the circuit behavior of SSi CMOS, compared to the performance of Si CMOS.

Our EMC simulator incorporates all relevant scattering mechanisms including: optical phonon, inelastic acoustic phonon, ionized impurity and interface roughness (IR) [10]. The simulator has been carefully calibrated against transport behavior in bulk SSi.

3. Device performance of sub-100nm SSi MOSFETs

The calibrated 67nm n-type Si and SSi device structure is then used within our EMC simulator, which is able to reproduce the experimental device characteristics using a calibrated interface roughness model, as shown in figure 3. The interface roughness scattering model, using the RMS height and correlation length (CL) along with an exponential auto-covariance spectrum to describe the interface, has been calibrated against the universal mobility behavior of Si and SSi [11]. A slightly smoother SSi/SiO_2 interface with longer CL is used in order to achieve agreement with the reported experimental data [2]. Reduced interface roughness scattering for SSi MOSFETs contributes significantly to the observed performance enhancement for these devices.

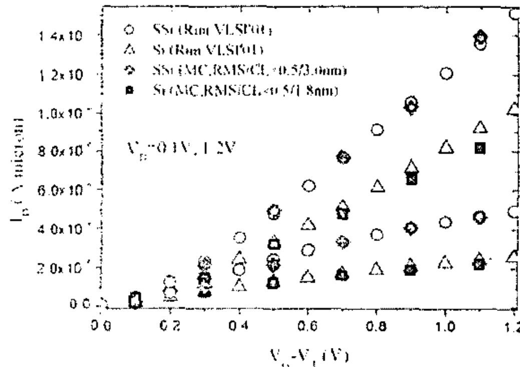

Figure 3. MC calibrated I_D-V_G characteristics of the 67nm n-type SSi MOSFETs

Figure 4 shows the average channel carrier velocities in the 67nm Si and SSi devices with and without IR scattering obtained from our MC simulations. It is clear that interface roughness significantly affects the carrier transport within the channel, limiting device performance at high field. The average channel velocity with calibrated roughness parameters in the SSi device is higher than in the Si device and is responsible for the performance enhancement observed in SSi MOSFET.

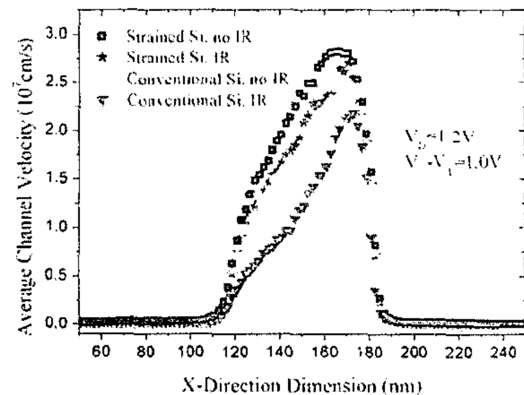

Figure 4. Average channel velocities of the 67nm n-type Si and SSi devices with and without IR scattering by MC

Monte Carlo simulations with the calibrated IR parameters for Si and SSi MOSFETs have also been used to evaluate the device performance of scaled SSi MOSFETs. An n-type Si MOSFET fabricated by Toshiba [12], with a 35nm physical gate length and 1.2nm gate oxide (relative permittivity=4.75), was used as the calibration standard. Complete device structure and doping profile were obtained from TAURUS process and device simulations [13]. Monte Carlo simulations assuming different degrees of process-induced strain within the channel are performed and the simulated I_D-V_G characteristics are plotted in figure 5.

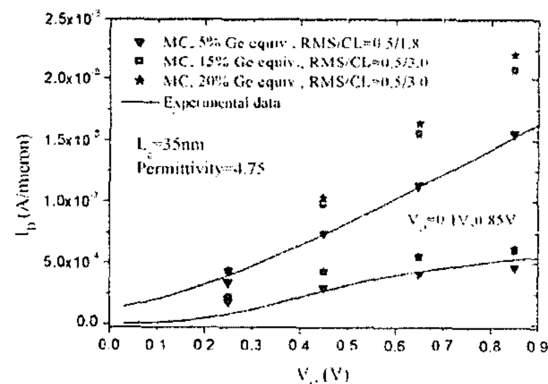

Figure 5. MC simulated I_D-V_G characteristics of 35nm n-type SSi devices with different degrees of strain

It is found that a process induced strain equivalent to the strain induced by using a relaxed $Si_{0.95}Ge_{0.05}$ substrate is appropriate to reproduce the experimental data. The 35nm SSi MOSFET with a 15% and 20% Ge content strain channel, assuming a 5% Ge intentional strain, delivers around 32% and 41% drive performance

enhancement over the 35nm Toshiba Si MOSFET. This is in agreement with the recently observed 45% drive current enhancement for a 35nm $SSi/Si_{0.8}Ge_{0.2}$ MOSFET [3]

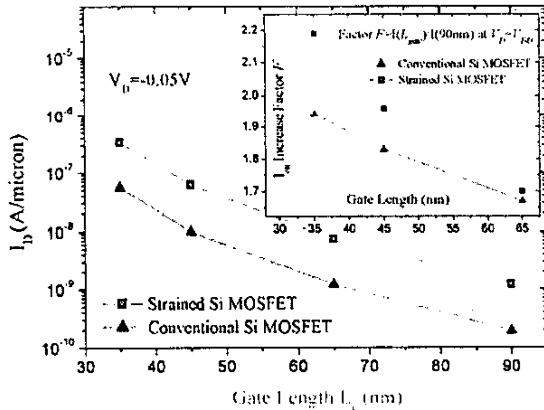

Figure 6. The low drain currents of p-type Si and SSi MOSFETs as a function of gate length (scaling from 90nm); the inset shows the high drain on current increase of scaled Si and SSi MOSFETs as a function of gate length compared to the 90nm devices

Using Hydrodynamic MEDICI simulations corrected with relaxation times obtained from our full band MC simulator, the calibrated p-type 90nm (67nm effective gate length) $SSi/Si_{0.72}Ge_{0.28}$ device structure has been scaled down to gate lengths of 65nm, 45nm and 35nm, following the technology nodes of the ITRS Roadmap [1]. The SSi and Si devices show similar behavior in the subthreshold regime during scaling. The devices behave well across all gate-lengths studied, with subthreshold slopes from 85 to 110mV/decade and a threshold voltage roll-off of around 120mV. The off-state currents of the scaled devices are shown in Figure 6. All of these important parameters meet or surpass the requirements of the ITRS roadmap. The drive current increases with scaling for both sets of devices and the current enhancement factor between the SSi and Si MOSFETs increases by 10% when the gate length is scaled from 90nm to 35nm. This is due to appreciable velocity overshoot in the SSi devices as a result of the increased hole relaxation time in strained Si. Further improvements in device performance maybe obtained by increasing the Ge content from 28% to 40%, in the substrate, *i.e.*, having higher degree of strain in the channel, which reduces inter-valley scattering and improves hole mobility in the SSi [14].

4. Circuit behavior of SSi CMOS

The calibrated 67nm effective IBM n-type and p-type Si and SSi MOSFETs are then used to construct 3-stage ring oscillators (OSCs). The device width is set to 2μm and 1μm for the p-type and n-type devices respectively in order to balance the drive currents of the p- and n-type MOSFETs. The DDM mixed mode simulations with MEDICI [7] are used to assess the circuit behavior of the investigated discrete devices. Figure 7 shows the characteristics for Si and SSi CMOS unloaded 3-stage OSCs. The delay per stage in the SSi circuit is about 6.5ps less than that in the conventional Si circuit, showing a ~20% performance enhancement for the SSi OSC without load capacitance.

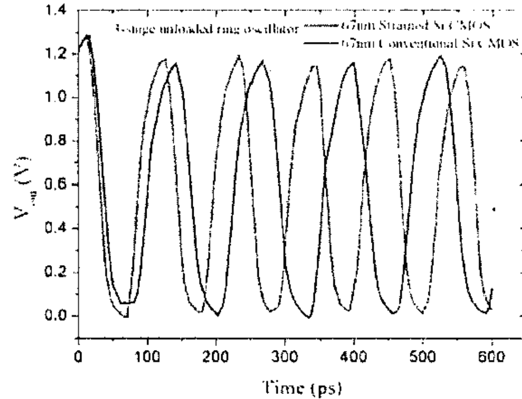

Figure 7. Output circuit characteristics for the 67nm effective gate length Si and SSi CMOS unloaded 3-stage OSCs

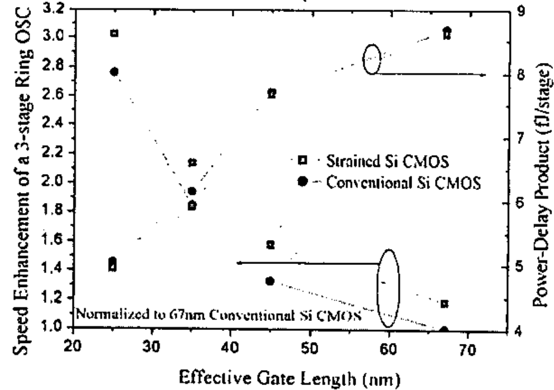

Figure 8. Speed enhancement and power-delay products against the effective gate length for Si and SSi CMOS unloaded 3-stage OSCs

The 67nm effective gate length n-type and p-type Si and SSi IBM devices have also been scaled down, ensuring that the threshold voltage for the different technology nodes is the same between the Si and SSi devices. MEDICI then simulates Si and SSi OSCs corresponding to these different gate lengths. By normalizing the circuit delays of these OSCs to that of

the 67nm Si circuit, the speed enhancement factors of these 3-stage OSCs are plotted in figure 8. It is evident that the circuit performance increases dramatically when the gate length is scaled down. The power-delay product of these circuits reduces as the gate length is scaled down.

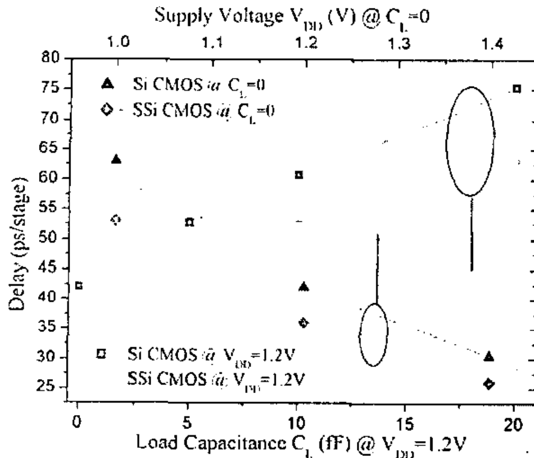

Figure 9. Circuit delays versus the load capacitance and the supply voltage for the 67nm Si and strained Si CMOS 3-stage OSCs

Figure 9 compares the simulated circuit delays of the 67nm Si and SSi OSCs when varying the power supply voltage V_{DD} and the load capacitance C_L. As V_{DD} decreases, the circuit delay of both circuits is increased. As C_L increases, the increase of the SSi circuits delay is slower than that of the Si circuit delay, indicating a performance enhancement greater than 20% for the SSi circuit with a realistic load capacitance is expected as compared to the Si circuit.

SOI devices may be used to further improve the circuit performance, in addition to the SSi technology. As a simple test case, we have used a buried SiO_2 layer within the 67nm IBM devices to form conventional Si SOI (SOI) and strained SOI (SSOI) MOSFETs. The body thicknesses of these SOI devices equal to the source/drain junction depth of the original 67nm bulk MOSFETs. Figure 10 compares the circuit delays and the power-delay products of the conventional bulk Si (Si), strained bulk Si (SSi), conventional Si SOI (SOI) and strained Si SOI (SSOI) unloaded 3-stage ring-oscillators. It is clear that the SOI circuits exhibit significant performance enhancement with lower power consumption as compared to their bulk counterparts. A combination of SSi channel and SOI device structures delivers significant performance enhancements with a lower energy/power consumption as compared to their bulk counterparts.

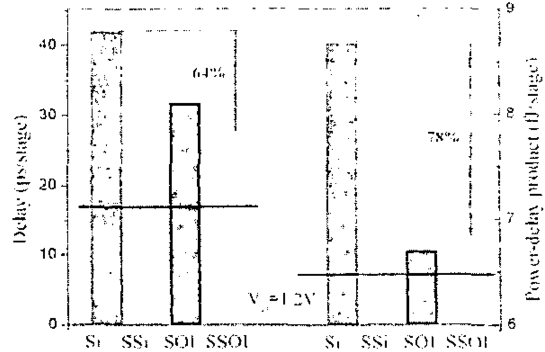

Figure 10. Comparisons of the circuit delays and power-delay products of the 67nm Si, SSi, SOI and SSOI CMOS unloaded 3-stage OSCs.

5. Conclusions

Simulations of strained Si MOSFETs with gate lengths scaled down to an effective gate length of 25nm have shown well-controlled short channel effects and enhanced performance over Si MOSFETs. The strained Si 3-stage ring oscillator exhibits ~20% performance enhancement over Si circuits. Silicon on Insulator (SOI) (Si and SSi) delivering even greater performance enhancements and consumes less power, thus leading to a promising future for Si based CMOS applications.

Acknowledgments

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