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UTB SOI SRAM Cell Stability under the Influence of Intrinsic Parameter Fluctuation

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Abstract:

Intrinsic parameter fluctuations steadily increases with CMOS technology scaling. Around the 90nm technology node, such fluctuations will eliminate much of the available noise margin in SRAM based on conventional MOSFETs. Ultra Thin Body (UTB) SOI MOSFETs are expected to replace conventional MOSFETs for integrated memory applications due to superior electrostatic integrity and better resistant to some of the sources of intrinsic parameter fluctuations. To fully realise the performance benefits of UTB SOI based SRAM cells a statistical circuit simulation methodology which can fully capture intrinsic parameter fluctuation information into the compact model is developed. The impact on 6T SRAM static noise margin characteristics of discrete random dopants in the source/drain regions and body-thickness variations has been investigated for well scaled devices with physical channel length in the range of 10nm to 5nm. A comparison with the behaviour of a 6T SRAM based on a conventional 35nm MOSFET is also presented.

1. Introduction

Ultra Thin Body (UTB) SOI MOSFETs have superior electrostatic integrity compared to conventional MOSFETs. The significant reduction in junction capacitance of SOI MOSFETs also reduces a major component of bitline capacitance, which is a critical parameter limiting SRAM performance [1]. Furthermore a steeper subthreshold slope permits trade off between power consumption and performance for SRAM cell design.

Working UTB MOSFETs with a channel length of 6nm have already been successfully demonstrated [2]. While UTB device can operate without dopant within the channel region there are necessarily discrete random dopants in the source/drain regions. At nanoscale dimensions the discreteness and randomness of the dopants in the source/drain regions will introduce fluctuations in the effective channel length and access resistance. Additionally, surface roughness at the top and bottom of the Si/SiO_2 interface will also introduce appreciable local variations in silicon body thickness and further contribute to device characteristic mismatch. Although UTB devices are the potential solution to the ultimate MOSFET scaling, an in-depth investigation of UTB MOSFET circuit behaviour in the presence of intrinsic fluctuations is important to understand the sources that have greatest contribution to device mismatch that will affect UTB SOI circuit robustness and performance. Accurate mismatch modelling is also necessary to avoid yield loss and overdesign.

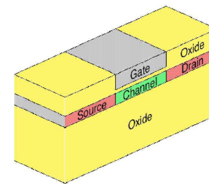


Fig. 1: Schematic view of the UTB SOI MOSFET simulated in this work.

Channel Length (nm)	10	7.5	5
Gate Oxide Thickness, T_{ox} (nm)	0.67	0.5	0.33
Body Thickness, T_{si}(nm)	2.5	2.25	2.0
Buried Oxide Thickness, T_{box}(nm)	50		
Channel Doping, N_a (cm^{-3})	1e14		
source-drain Doping, $N_{s/d}$ (cm^{-3})	2e20		

Table 1: Generic device parameters considered.

In this paper a comprehensive statistical device circuit simulation methodology is used to assess the impact of the scaling limit on fluctuation sensitive 6T SRAMs due to discrete random dopants in the source/drain regions of UTB SOI MOSFETs. The methodology also helps to identify key areas for device mismatch optimisation based on future technology trends. Frequently used in integrated systems, SRAM cells have a minimum foot print to achieve high integration density. They will be adversely affected by intrinsic parameter fluctuations between their macroscopically identical transistors, that steadily increases with the scaling [3]. A comparison with parameter fluctuation due to body thickness fluctuations [4] and random dopant induced parameter fluctuations in the channel region of conventional 35nm channel length bulk MOSFETs [5] corresponding to current 90nm node is also presented.

2. UTB SOI Structure and Simulation

The generic structure of the simulated devices is illustrated in Fig. 1 and the corresponding carefully scaled device parameters are summarised in Table 1.

In order to capture statistical variation in the device parameters associated with the discrete random dopants in the source and drain regions, an ensemble of 200 macroscopically identical, but microscopically different

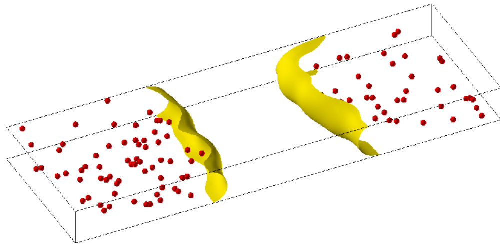


Fig. 2: Location of discrete random dopants in the source and drain regions and variation of effective channel length in the silicon body of a 10nm UTB SOI MOSFET.

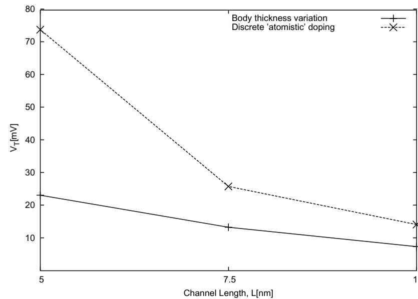


Fig. 3: Threshold voltage fluctuations (σV_T) in 10nm to 5nm UTB SOI MOSFETs from statistical simulations of an ensemble of 200 devices with different sources of intrinsic parameter fluctuation. The threshold voltage is approximately 200mV.

devices is created and simulated using the Glasgow 3D 'atomistic' drift diffusion simulator [6]. The simulator includes density gradient quantum corrections which take into account the thin-body confinement effects. The individual dopants are introduced in the simulation using a rejection technique describe in [7]. Fig. 2 illustrates the location of the discrete random dopants in the source/drain regions and corresponding variation of effective channel length in the silicon body of a 10nm channel length UTB SOI MOSFET.

As shown in Fig. 3, the random source/drain dopants introduce threshold voltage fluctuations, with a standard deviation (σV_T) increasing from 14mV to 74mV as the device is scaled from 10nm to 5nm. It is also evident that discrete 'atomistic' doping in the source/drain regions will become a dominant source of intrinsic parameter fluctuation in UTB SOI devices compared to parameter fluctuation due to body thickness variation.

3. Statistical Circuit Simulation

An improved two-stage statistical parameter extraction methodology [4] is employed to capture all device fluctuation information obtained from the 3D 'atomistic' simulator into a representative set of BSIMSOI-FD compact models using Aurora™. In principle, BSIMSOI-FD is flexible enough to describe device mismatch caused by 'atomistic' fluctuation using a number of carefully choosen empirical parameters originally introduced to model device performance variation caused by different foundry processes. Our statistical circuit strategy assure accurate description limited only by the nature of collected

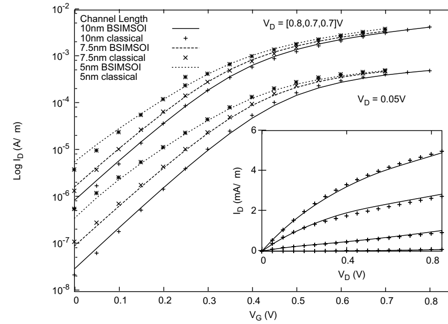


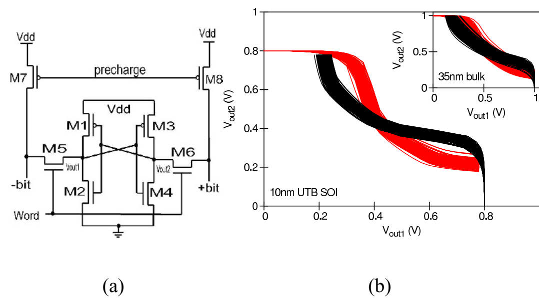
Fig. 4: Compact model calibration of gate characteristics for all channel lengths and drain characteristics for 10nm channel length. All characteristics are from nMOSFET UTB SOI.

data, whether from simulation or experiment. If used at an early stage of design cycle this methodology could minimize memory failure probability by statistical sizing of SRAM cell. Statistical circuit simulation based on principle component analysis (PCA) or backgate propagation of variance (BPV) [8] may not capture all physical fluctuation information and may produce misleading results.

Firstly, a number of key BSIMSOI model parameters are extracted from the I-V characteristics of generic devices with uniform source/drain doping using locally optimised, single device extraction strategy which is a modification to the extraction strategy used in partially-depleted devices [9]. Figure 4 illustrates the quality of BSIMSOI extraction in respect of the physically simulated I_D-V_G characteristics of 10nm, 7.5nm and 5nm channel lengths devices. Results for the I_D-V_D characteristic fit quality for the 10nm transistor are shown in the inset of the same figure.

Parameters which are insensitive to intrinsic fluctuations are fixed after this phase while seven BSIMSOI parameters are selected for extraction in the second-stage, to represent the variations in characteristics due to the random dopants in the source/drain regions. The second phase of extraction consists of two steps. The first is based on the $I_D V_G$ characteristics at low drain bias, matching threshold voltage and sub-threshold slope using R_{dsw}, Prwg, N_{factor} and V_{off} parameters. Then the saturation region is matched at high drain bias using A_1, A_2 and D_{sub} parameters.

In BSIMSOI-FD, R_{dsw} characterizes the access resistance while Prwg is the gate-bias effect coefficient of R_{dsw}. These two parameters can reflect effective channel length variation and access resistance fluctuation in the strong inversion region. In the case of body thickness fluctuation, R_{dsw} is not required and Prwg will reflect threshold voltage fluctuation in the subthreshold region. Parameter N_{factor} is an ideality factor improving the subthreshold description and accommodating different device geometries under various conditions, while parameter V_{off}, the offset voltage in subthreshold region, can be effectively used to reflect threshold voltage fluctuation caused by 'atomistic' fluctuation. Parameters A_1 and A_2 are non-saturation factors that ultimately determine saturation voltage, therefore can be used to map random dopant induced elec-



(a) (b)

Fig. 5: (a) Circuit schematic of the 6T SRAM. (b) Static transfer characteristics of 200 statistical SRAM cells utilising 10nm UTB MOSFET and 35nm bulk MOSFET.

tric field fluctuations in the pinch-off region. D_{sub} is the channel length dependence of drain-induced barrier-lowering (DIBL) effects on threshold voltage and can be used to reflect 'atomistic' fluctuation caused DIBL effects variation.

The mean RMS errors of the statistical compact model extraction from all channel lengths are less then 5% percent for each source of intrinsic parameter fluctuation and have a narrow normal distribution for the ensembles of 200 microscopically different devices. The low RMS error clearly prove that the choice of seven key parameters adequately describes the effect of discrete random dopants in the source/drain regions over the whole range of device operation for all samples of devices with channel length of 10nm, 7.5nm and 5nm. Worth noting is that the RMS error for the whole sample of transistors with a particular channel length depends on the accuracy of the uniform device parameter extraction during the first stage and could be improved by improving the extraction strategy. The statistical compact model library built during this stage are used in Spice simulations. We assume that both NMOS and PMOS devices have a similar statistical distribution due to random dopant in source-drain region, with PMOS drive half that of NMOS.

4. SNM Fluctuation due to intrinsic parameter fluctuations

A schematic of the 6T SRAM cells simulated for 10nm, 7.5nm and 5nm channel length technology with 0.8V, 0.7V and 0.7V supply voltage respectively is shown in Fig. 5(a). In SRAM cell design the stability of the cell is a critical factor to obtain the desired yield. The Static Noise Margin (SNM) [10] which is the minimum DC noise voltage needed to flip the cell state is often used to measure the cell's stability . The stability is typically assessed during the read operation when SRAM is vulnerable to noise. SRAM stability could be improved by increasing the cell ratio, defined as the ratio of M2, M4 driver transistors width/length (W/L) ratio to the M5, M6 access transistors W/L ratio. This however would also increase the overall cell size. Static transfer curves for an ensemble of 200 10nm channel length UTB MOSFETs with cell ratio 1, considering only discrete random doping in the source/drain regions, is shown in Fig. 5(b). The butterfly opening of the transfer curves can be clearly seen compared to the results obtained for 35nm conventional bulk MOSFET [5]. The bulk MOSFET performance, with the same cell ratio configuration, is worst due to the larger fluctuations resulting from discrete random doping in the channel region.

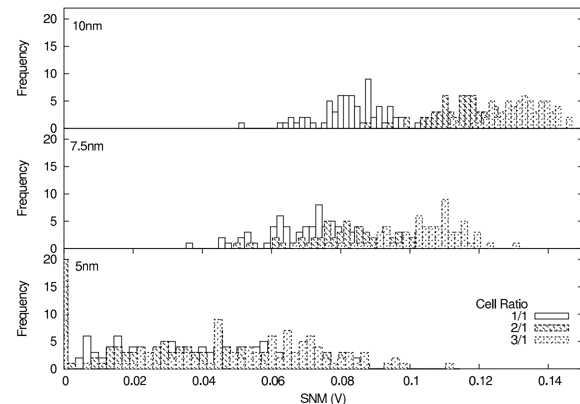


Fig. 6: SNM distributions for 10nm, 7.5nm and 5nm channel lengths UTB MOSFETs caused by random dopants in the source/drain regions.

Figure 6 illustrates the distribution of the SNM due to discrete random doping for SRAM cells based on UTB devices with different cell ratios, for each channel length being investigated here. It clearly follows the expected trend that increasing cell ratio improves cell stability for all channel lengths reflected in the reduced normalized standard deviation in Fig. 7. Larger W/L ratios also reduce the magnitude of fluctuations caused by body thickness variation, which is partly reflected in the normalised standard deviation of SNM. It is also evident that increasing the cell ratio delivers less improvement of the SNM with decreasing channel length. For example, in the case of intrinsic fluctuation caused by discrete random dopants, a cell ratio of 3 gives approximately 60% reduction of SNM normalised standard deviation for 10nm while only 30% reduction for 5nm channel length device. Although there is no extreme SNM deviation for 10nm and 7.5nm UTB SOI MOSFETs device due to random dopants in Fig. 7 and body thickness variation in the inset of the same figure, the normalised standard deviation of 5nm channel length device doubles due to fluctuations caused by random dopants in the source/drain regions. For 5nm device, resorting to a higher cell ratio would only increase the cell area, without the full benefit of SRAM scaling compared to 10nm and 7.5nm channel length

Calculated $\mu - 6\sigma$ from 200 statistical SRAM cell simulations for 10nm and 7.5nm UTB SOI MOSFETs and 35nm bulk MOSFET [5] as a function of cell ratio is shown in Fig. 8. Note that the UTB devices are only simulated from a cell ratio of 1 to 3 while bulk MOSFET are simulated from a cell ratio of 2 to 4. Fig. 8 depicts the influence of intrinsic fluctuations caused by random dopants in the source/drain regions and body thickness variation in UTB SOI devices, while the conventional MOSFET only consider discrete random doping in channel region. As apparent from Fig. 8, increasing cell ratio leads to

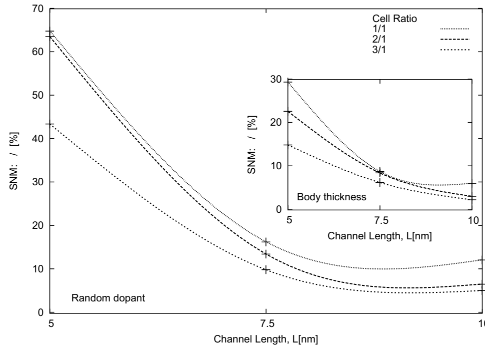


Fig. 7: Normalised standard deviation of SNM for different channel lengths and cell ratios due to different sources of intrinsic parameter fluctuations.

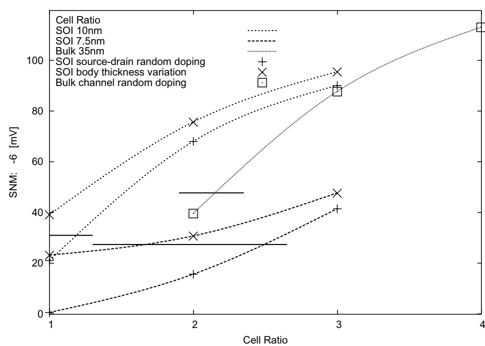


Fig. 8: μ−6σ of Static Noise Margin (SNM) as a function of cell ratio for 10nm and 7.5nm UTB SOI MOSFET and 35nm bulk MOSFET. Lines: μ−6σ>32mV for 10nm, >28mV for 7.5nm and >48mV for 35nm.

improvement in μ−6σ which implies that a larger fraction of SRAM cells for each geometry become more stable. As a guideline, μ−6σ is required to exceed 4% of the supply voltage to achieve 90% yield on 1Mbit SRAM's [11]. This translates to at least a cell ratio of 1 and 2 for 10nm and 7.5nm respectively considering only body thickness variation. If mismatch caused by random doping is taken into account, a cell ratio of 2 for 10nm and cell ratio of 3 for 7.5nm is required. From the SNM point of view this implies that 6T SRAMs may not gain the full benefits from further UTB MOSFET scaling to channel lengths smaller than 10nm.

Compared to UTB MOSFET based SRAMs, bulk 35nm MOSFETs could not operate at a cell ratio of 1 and require ratio of at least 3, considering only intrinsic fluctuations caused by discrete random doping effects in the channel region. In terms of SNM stability, 10nm UTB SOI MOSFETs is suited to replace bulk MOSFETs in SRAM cells as shown in Fig. 8. 10nm UTB device SRAM cells are more stable even though operated at 80% of the supply voltage of 35nm bulk MOSFETs.

5. Conclusions

Using statistical circuit simulation methodology, we have compared the impact of effective channel length variation and access resistance fluctuation introduced by discrete random dopants in the source/drain regions with body-thickness fluctuation introduce by interface roughness on the operation of 6T SRAMs. Simulation results show random dopants in source/drain region will become a major source of device mismatch in UTB SOI MOSFETs below the 10nm channel length margin. We have shown that the operation of 6T SRAM cells based on 10nm UTB SOI MOSFETs is more stable than cells based on 35nm bulk MOSFETs from static noise margin point of view. This could extend the benefits of SRAM scaling beyond the 25nm technology node [12]. However, novel device architectures such as Double Gate MOSFETs are required after the 10nm channel length mark. It is important that each potential source of intrinsic parameter fluctuation is carefully studied in new devices to fully map their impact on the corresponding SRAM cell generations.

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