Hot-Carrier-Induced Deep-Level Defects from Gated-Diode Measurements on MOSFET's

P. SPECKBACHER, A. ASENOV, M. BOLLU, F. KOCH, AND W. WEBER

Abstract—**We measure reverse-bias current in the gated-diode configuration of hot-carrier degraded MOS devices. It is shown that interface defects created by the degradation contribute predominantly to the generation current. Using device simulation we obtain the spatial distribution of the deep-level defects.**

I. Introduction

IN [1] gated-diode measurements were introduced as a means of detecting interfacial deep-level defects in MOS structures. Experiments record the reverse-bias generation current I_{gen} between the n^+-drain and p-type substrate of the n-channel FET as a function of the gate voltage V_G. In a recent letter [2] Giebel and Goser have employed this technique to monitor the changes of I_{gen} after hot-carrier degradation. They conclude that the degradation procedure results in bulk-type defects in the substrate below the Si–SiO_2 interface, and in bulk or interface defects in the drain–gate overlap region. Commonly the damage is described in terms of interface defects positioned in a narrow zone (typically ≈ 0.1 μm) near the drain. Sharply peaked distributions of interface states have been confirmed in charge-pumping experiments [3] and by modeling of the I_D–V_D characteristic in degraded MOSFET's [4], [5].

It is the purpose of this letter to point out that gated-diode experiments on degraded MOSFET's do show evidence for interface defects. In conjunction with two-dimensional device simulation the experiments give a detailed measure of the spatial distribution of the interface states.

II. Principle of the Measurement

Under reverse-bias nonequilibrium conditions in the depletion layer surrounding the drain in Fig. 1, Shockley–Read–Hall statisics point to midgap levels as the exponentially most effective centers for generating carriers. The generation component I_{gen} of the diode current for small positive drain bias V_D ($eV_D <$ bandgap) comes from midgap states that are located between the two contours marked φ_e^i and φ_h^i in the figure. The lines define, respectively, the position where the quasi-Fermi levels for electrons φ_e and holes φ_h coincide with

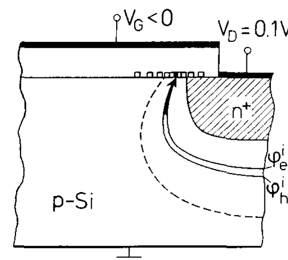

Fig. 1. Depletion zone (dashed line) at a reverse-biased drain–substrate junction in the case of accumulation at the interface. Centers at midgap between the contours φ_e^i and φ_h^i where midgap coincides with the quasi-Fermi levels for electrons and holes, respectively, are effective for generating carriers.

the intrinsic level E_i. Assuming a broad, uniform energy distribution of the defect states near E_i, the active interface centers are physically located in the narrow band between φ_e^i and φ_h^i (pointer in Fig. 1). When V_G is swept from inversion threshold through depletion into increasingly strong accumulation, the effective zone moves like a pointer of decreasing width along the interface toward the drain. The current I_{gen} rises and falls with the number of midgap interface states included in the width of the pointer. Thus I_{gen} versus V_g samples the spatial distribution of the hot-carrier-produced interface defects. It is clear that a simulation of the potential distribution is necessary to extract the desired position information. Good resolution requires small V_D.

Bulk-type midgap states in the silicon substrate can also be a source of I_{gen}. For V_G above inversion threshold they are the only active centers, because contours φ_e^i and φ_h^i do not intersect the interface. The volume contribution to I_{gen} above threshold is expected to be constant. For accumulation conditions the bulk contribution depends critically on the location of the defects. If they lie at a depth comparable to the depletion depth below the interface their contribution will be constant with V_G.

Because defects generated by hot-carrier degradation are expected to lie at the interface and close to the drain, an enhancement of I_{gen} in the accumulation regime should be observed.

III. Experiments and Device Simulation

We make use of a test structure device with effective channel length $L = 1.7$ μm (gate length $= 2.25$ μm) and width $W = 10$ μm. The oxide thickness is 40 nm. The drain has a conventional arsenic implantation profile. The reverse-bias

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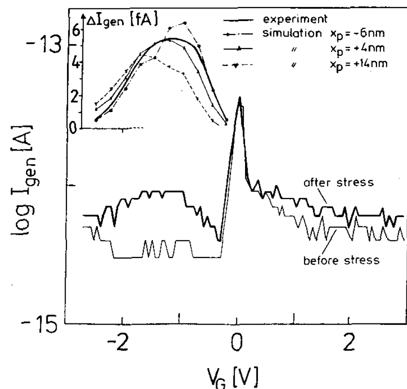

Fig. 2. Reverse-bias ($V_D = +0.1$ V) drain–substrate current as a function of gate voltage for a MOSFET before and after stress. The stress was done at $V_{DS} = 8$ V and $V_G = 3$ V for 30 min. The insert shows the smoothed (last digit = $1 \cdot 10^{-15}$ A) difference of the two curves (thick solid line) and results of the simulation for three different distributions of the interface generation velocity S. The shape is as in Fig. 3 and the position of the maximum is given by x_p, which represents the distance to the metallurgical drain–substrate junction.

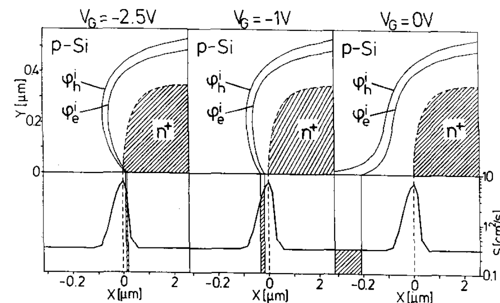

Fig. 3. Simulated contours of φ_e^i and φ_h^i ($V_D = 0.1$ V) and the distribution of the interface generation velocity S for which best fit with the experimental I_{gen} (Fig. 2, $x_p = 4$ nm) has been achieved. The reverse-bias current I_{gen} is directly proportional to the hatched area under the S distribution.

diode current in Fig. 2 is obtained at $V_D = 0.1$ V at 300 K (floating source). It is primarily a defect-generated current so that we choose to refer to it as I_{gen}. Tunneling contributions [6], [7] occur at higher V_G. We note the log scale and that currents in the femtoampere range are recorded. The insert gives the differential current ΔI_{gen} after stressing for 30 min at $V_{DS} = 8$ V, and $V_G = 3$ V. ΔI_{gen} is smoothed over the "last digit" fluctuations in the experimental curve I_{gen}.

We note that the increase of I_{gen} is substantially larger for negative V_G than for positive V_G. This has been found for many samples, including some with 1-μm lightly doped drain (LDD) technology. There is also a distinctly peaked structure for I_{gen} on the accumulation side. Both facts point to a significant interface contribution. There is a finite ΔI_{gen} above threshold (+0.5 V). The effect is small and, in Fig. 2, at the limit of detectability. Nevertheless, it is seen consistently in this and other samples. It is seen clearly when V_D is increased. Thus our data confirm the observations in [2]: hot-carrier stress can generate defects in the silicon substrate below the interface. The actual density of these defects can be estimated only roughly because their spatial distibution is not known. Assuming midgap generation centers in a volume of $1 \cdot 10^{-12}$ cm^3 (0.1 μm $\cdot$ 1 μm $\cdot$ 10 μm) close to the drain, and a capture cross section of $3 \cdot 10^{-15}$ cm^2, the current increase of $1 \cdot 10^{-15}$ A in Fig. 2 for $V_G > 0.5$ V results in a defect density of $1 \cdot 10^{13}$/cm^3. The essential point, however, is that interface damage dominates in our degraded samples. The device simulation proceeds accordingly, assuming that the I_{gen} variation below threshold is caused by interface defects only.

Simulating the potential distribution in the gated-diode configuration of the MOS device we obtain the potential contours in the upper half of Fig. 3. The generation zone ($V_D = 0.1$ V) is seen to move about in position and shape with V_G. The area of contact with the interface changes as V_G rises from -2.5 to -1.0 and 0 V. Finally (above 0.5 V) it breaks away completely from the interface.

The influence of the interface defects is represented in terms of an interface generation velocity S [8], which is proportional to an areal defect density times a generation rate. I_{gen} is then calculated (according to Shockley–Read–Hall statistics) and compared with the experimental traces. Satisfactory agreement of simulation and experiment is obtained for the spatial distribution of S given in the lower half of Fig. 3. The maximum of this distribution is located inside the drain, 4 nm away from the metallurgical drain–substrate junction ($x_p = +4$ nm). The incremental ΔI_{gen} in the insert of Fig. 2 can be perfectly well described by this peaked, skewed distribution of S. The constant background stems from fitting the original device. The insert of Fig. 2 also shows the effect of rigidly displacing the distribution by ± 10 nm in the calculation. Fig. 3 illustrates how the effective zone scans the distribution of interface states. It is obvious that device simulation is essential to locate the position, width, and shape of the effective zone and thus to relate the measured I_{gen} to the S distribution.

The magnitude of S obtained in Fig. 3 is reasonable. With the usual values of cross section and statistical emission probability for the defects, a value of $S = 1$ cm^2/s corresponds to a density of 10^{10} deep levels/cm^2. The distribution in position of the defects closely relates to the field-spike profile during the degradation [9]. The electric field also reaches inside the metallurgical drain and decreases more abruptly on the drain side.

IV. Conclusions

Using small V_D and I_{gen} in the femtoampere range, our gated-diode measurements on n-channel conventional (and preliminary on 1-μm LDD) MOSFET's show that predominantly interface defects have been created by hot-carrier degradation. Two-dimensional simulation appears very sensitive to the position (within 10 nm) and shape of the spatial distribution of the generation centers. For our stress condition ($V_{DS} = 8$ V, $V_G = 3$ V), the defect distribution is within 100 nm around the drain–substrate junction and drops more steeply on the drain side. To a lesser extent bulk defects, more than the depletion depth away from the interface, have also been found. This observation suggests that, although the interface appears to be more susceptible to degradation, defects that have been related to the interface may partly be located in the

substrate. Indeed, a very special highly peaked distribution of volume defects, near the drain and at a shallow depth (much less than the depletion depth), can, in principle, also serve to

[4] A. Schwerin, W. Hänsch, and W. Weber, "The relationship between oxide charge and device degradation: A comparative study of n- and p-channel MOSFET's," *IEEE Trans. Electron Devices,* vol. ED-34, pp. 2493–2500, 1987.