The "Gated-Diode" Configuration in MOSFET's, A Sensitive Tool for Characterizing Hot-Carrier Degradation

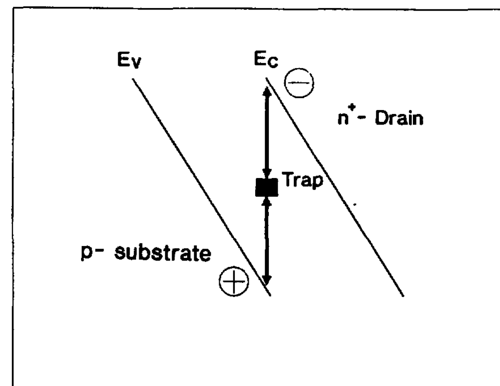
Peter Speckbacher, Josef Berger, A. Asenov, Frederick Koch, and Werner Weber

Abstract— **This paper describes a new measurement technique, the forward gated-diode current characterized at low drain voltages to be applied in MOSFET's for investigating hot-carrier stress-induced defects at high spatial resolution. The generation/recombination current in the drain-to-substrate diode as a function of gate voltage, combined with two-dimensional numerical simulation, provides a sensitive tool for detecting the spatial distribution and density of interface defects. In the case of strong accumulation, additional information is obtained from interband tunneling processes occurring via interface defects. The various mechanisms for generating interface defects and fixed charges at variable stress conditions will be discussed, showing that information complementary to that available from other methods is obtained.**

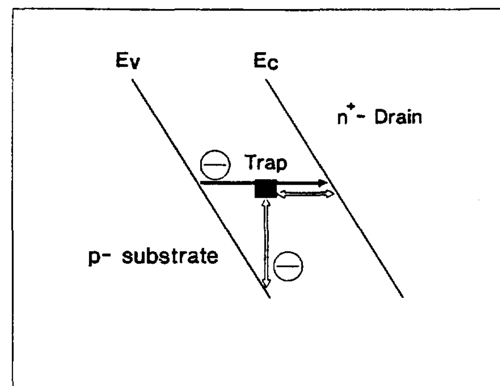
I. Introduction

It has long been acknowledged that hot-carrier degradation of MOS transistors results in long-term instabilities which impose serious limitations on the reduction of feature size [1]. The classical concept of hot-carrier degradation is that in short-channel MOSFET's electrons are strongly heated in the electrical field near the drain and emitted into the gate oxide. This leads to electron trapping and/or formation of interface states near the drain, which results in experimentally observed changes in threshold voltage and transconductance [2], [3].

Not only the number but also the spatial distribution of hot-carrier induced interface defects in MOSFET's determines the degradation of device performance. Defects above the drain region can set limits for the minimum gate-to-drain overlap and the permitted dose of the n^- implantation. Initially charge pumping measurements [4] and [5] were used to evaluate the spatial profile of interface traps in MOSFET's. This method and the more conventional electrical current measurement methods are more or less insensitive to defects created in the region of drain-to-gate overlap. In [6] the gated diode measurements were introduced as a means of detecting interfacial deep-level defects in MOS structures. Data are presented on the reverse-bias generation current I_G between the n^+-drain and p-type substrate of the n-channel FET as a function of the gate voltage V_G. In [7] Giebel and Goser employ this technique to monitor the changes of I_G after hot-carrier degradation. They conclude that the degradation procedure results in bulk-type defects in the substrate below the Si-SiO$_2$ interface, and in bulk or interface defects in the drain-gate overlap region. The forward bias measurement of



(a)



(b)

Fig. 1. A view of possible transport mechanism in the "gated-diode" in accumulation. The "hot-carrier" induced defect is located in the drain-substrate diode at the Si/SiO$_2$ interface. (a) weak accumulation: generation/recombination process; (b) strong accumulation: defect-assisted tunneling process.

Manuscript received September 15, 1994; revised December 28, 1994. The review of this paper was arranged by Associate Editor B. Ricco.

P. Speckbacher is with Dr. Johannes Heidenhain GmbH, Research and Development, D-83301 Traunreut, Germany.

J. Berger and A. Asenov are with the Department of Electrical and Electronic Engineering, University of Glasgow, Glasgow G12 8QQ, Scotland.

F. Koch is with Physik-Department E16, Technical University München, D-85747 Garching, Germany.

W. Weber is with Siemens AG, Corporate Research and Development, D-81730, München, Germany.

IEEE Log Number 9411409.

0018-9383/95$04.00 © 1995 IEEE

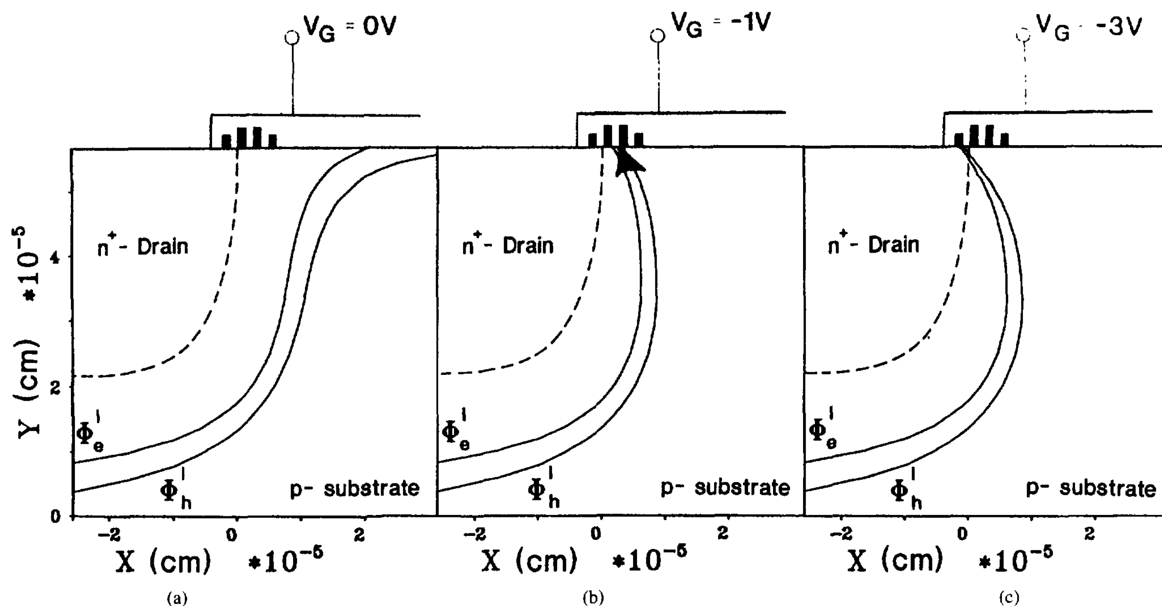


Fig. 2. Simulated contours of Φ_e^i and Φ_h^i at a drain voltage $V_D = 0.2$ V for a reverse biased drain-to-substrate junction in the case of (a) threshold voltage, (b) weak accumulation, and (c) strong accumulation. In-between the contours Φ_e^i and Φ_h^i where mid-gap coincides with the quasi-Fermi levels for electrons and holes, respectively, midgap centers are effective for generating carriers.

the current of the drain gated diode [8] as a function of gate voltage V_G has been used for monitoring the hot-carrier induced defects. Recently it has been shown [9] and [10] that measurement of reverse/forward bias current in the gated-diode configuration of hot-carrier degraded MOS-devices in combination with 2D-numerical simulation, can provide a detailed measure of the spatial distribution of the interface states, including the gate-to-drain overlap region.

It is the purpose of this work to obtain a precise knowledge of the gated-diode configuration in MOSFET's in order to use it as a sensitive tool for characterizing hot-carrier stress. In particular the zone most affected by electrical stress, close to and within the drain region, will be detected very sensitively using the gated-diode technique in comparison with other measurement methods, such as charge-pumping and subthreshold measurement. In Section IV.A generation/recombination currents in the reverse and forward mode of the gated-diode are used to obtain the spatial distribution and density of the deep level defects. In Section IV.B we report on band-to-band tunneling processes which are strongly affected by interface trap generation. The creation of interface defects and/or fixed charges at different stress conditions will be discussed in Section V, whereby information will be obtained from the gated-diode technique.

This new insight into the underlying mechanisms of generation/recombination and tunneling in the gated-diode configuration makes this technique a powerful and reliable quantitative method for determining interface state density and its spatial distribution—even for small area MOS transistors.

II. Principle of Measurement

As far as the gated-diode at moderate accumulation gate voltages is concerned, we observe generation/recombination processes (Fig. 1(a)). In strong accumulation, interband tunneling processes occur (Fig. 1(b)), which in particular take place in the gated-diode configuration after hot-carrier stress.

Assuming a broad uniform energy distribution of the defect states around the intrinsic level E_i, the active interface centers are physically located in the narrow band between Φ_e^i and Φ_h^i (pointer in Fig. 2). The lines define respectively the position where the quasi-Fermi levels for electrons Φ_e and holes Φ_h coincide with the intrinsic level E_i. When gate voltage V_G is swept from inversion threshold, through depletion into increasingly strong accumulation in Fig. 2(a)–(c), the effective zone moves like a pointer of decreasing width along the interface toward the drain. The area of contact with the interface changes as V_G rises from 0 V to -1 V and -3 V. Finally (above 0.3 V) it separates completely from the interface.

Moderate Accumulation: Under small reverse or forward bias nonequilibrium conditions in the depletion layer surrounding the drain in Fig. 2, Shockley-Read-Hall statistics [11] point to mid-gap levels as the exponentially most effective centers for generation/recombination processes of carriers. The generation/recombination component $I_{\text{G-R}}$ of the drain-to-substrate diode current for small drain bias V_D ($|V_D| < 0.3$ V) comes from mid-gap states that are located between the two contours marked Φ_e^i, Φ_h^i in Fig. 2. Since defects generated by hot-carrier degradation are expected to lie at the interface and close to the drain [12], an enhancement of $I_{\text{G-R}}$ in the accumulation regime should be observed. The current $I_{\text{G-R}}$ rises and falls with the number of mid-gap interface states included in the width of the pointer. Thus $I_{\text{G-R}}$ vs V_G samples the spatial distribution of the hot-carrier produced interface defects.

Strong Accumulation: At strong accumulation in Fig. 2(c), an additional contribution to the generation/recombination

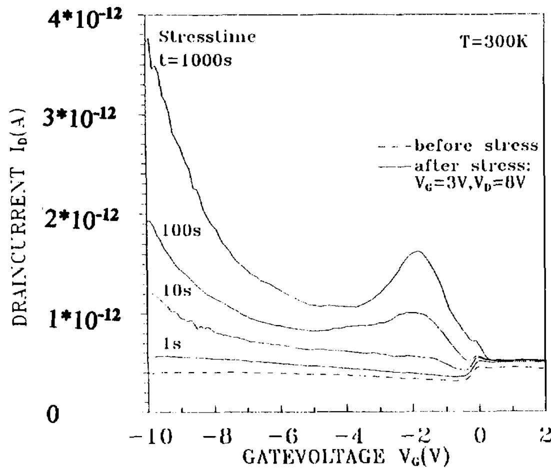


Fig. 3. Forward biased ($V_D = -0.2$ V) drain-to-substrate current as a function of gate voltage V_G for a conventional n-channel MOSFET before and after hot-carrier stress. The stress was performed at $V_G = 3$ V and $V_D = 8$ V for different stress times t.

current arises from tunneling leakage current I_T. The higher the gate voltage $|V_G|$, the smaller the active zone in Fig. 2(c) (typically <100 Å at $V_G < -5$ V), resulting in increased tunneling probability. The tunneling current I_T is described as an interband process between valence band E_v and conductance band E_c which is strongly influenced by interface defects. These tunneling processes predominantly take place at the Si/SiO_2 interface since the tunneling barrier is smallest there.

III. Experimental

A. Device Preparation

We make use of n-channel LDD MOSFET test structure devices with effective channel length $l = 0.7$–$1.5\,\mu$m, width $w = 10\,\mu$m and a gate oxide thickness $d_{\text{ox}} = 20$ nm. The channel acceptor concentration is $5 \cdot 10^{16}$ cm^{-3}. The n^--implantation of the LDD is phosphorous with a dose of $3 \cdot 10^{13}$ cm^{-2}.

B. Measurement

All measurements are carried out with a computer controlled HP4145-A digital analyzer. The channel hot-carrier stress is performed at various gate voltages V_G and stress times t with the drain voltage V_D fixed at 8 V.

In Fig. 3 the drain-to-substrate current after three different stress times with $V_G = 3$ V, $V_D = 8$ V is compared with the current before stress. The forward bias drain-to-substrate diode current before and after stress in Fig. 3 is obtained at drain voltage $V_D = -0.2$ V at 300°K (floating source). The gate voltage V_G is swept from accumulation ($V_G = -10$ V) via flatband ($V_G = -0.5$ V) to inversion ($V_G = 0$ V).

At moderate gate voltages (-4 V $< V_G < -0.5$ V), discussed in part IV.A, we predominantly obtain defect generated currents, so that we choose to refer to it as $I_{\text{G-R}}$. In a recent publication [10], the spatial distribution of the interface defect density $N_T(x)$ was extracted from the curves with the help of 2D-numerical simulation. At more negative gate voltages in strong accumulation, there is additional contribution to the current due to defect assisted interband tunneling processes. We note that the increase of $I_{\text{G-R}}$ is substantially larger for negative V_G than for positive values. This has been found for many samples with and without LDD ("lightly-doped-drain") technology. A distinctly peaked structure for $I_{\text{G-R}}$ occurs on the accumulation side. At highly negative gate voltages ($V_G < -4$ V), discussed in Section IV.B, we observe additional contribution to the generation/recombination current due to tunneling processes, which are strongly affected by hot-carrier stress. Both facts point to the domination of the significant interface contribution after hot-carrier damage for the parameters investigated here.

IV. Results and Discussion

A. Generation/Recombination Processes

In the following section we describe the drain-to-substrate diode current at moderate gate voltages V_G in accumulation by means of generation/recombination processes via midgap states. The difference between reverse and forward biasing the drain-to-substrate diode will be discussed.

According to "Shockley-Read-Hall" statistics, midgap levels are exponentially most effective centers for generation/recombination of carriers [10]. From the experimental data in Fig. 3 we extract the temperature dependence of the activation energy E_a at fixed gate voltages V_G. By taking the maximum current of the hump at moderate gate voltage $V_G \approx -2$ V, an activation energy of 0.6 eV is estimated before and after stress, indicating that generation/recombination processes dominate compared to tunneling processes. In strong accumulation ($V_G = -6$ V) the temperature dependence becomes weaker ($E_a \approx 0.25$ eV), suggesting the occurrence of tunneling processes, which will be discussed in Section IV.B.

Let us consider the difference between reverse and forward biasing the drain-to-substrate diode at small drain voltages ($|V_D| < 0.3$ V). As discussed in a recent publication [9], only generation processes via midgap states will occur in reverse bias. This generation current as a function of gate voltage, together with 2D-numerical simulation, provides the spatial distribution of hot-carrier generated interface defects.

In contrast, biasing the drain-to-substrate diode in the forward mode the current I_F consists of two components, an ideal diode diffusion current I_{diff} and a bulk or surface recombination current I_{rec} in the depletion region [11]. For small forward biases ($|V_D| < 0.3$ V) the recombination current dominates and is also a monitor for the concentration of stress created recombination centers [10].

In Fig. 4 the shape of the surface generation rate $G(x)$ along the interface for a gate voltage $V_G = -2.6$ V and a reverse drain voltage $V_D = 0.2$ V is compared with the recombination rate $R(x)$ in forward bias condition with $V_D = -0.2$ V. We should point out that a logarithmic scale is used for the ordinate

of the diagram. The generation rate $G(x)$ shows a relatively weak dependence on position, where midgap lies in-between the electron and hole quasi-Fermi level. A spatial resolution of about 20 nm is obtained in this case. The recombination rate $R(x)$ through midgap levels, however, exhibits a sharp peak at the position where the injected electron and hole concentrations coincide and drops exponentially away from this point yielding an improved resolution of less than 5 nm. With decreasing temperature T the sharpness of $R(x)$ increases. Furthermore, the magnitude of the recombination amplitude depends on the level of injection.

To demonstrate the higher resolution from forward biasing the drain-to-substrate diode, we present results in a recent publication [10] for forward and reverse gated-diode measurements on the same sample before and after stress. As expected, because of the sharpening of the "pointer" in the forward mode measurement (Fig. 4) the spatial resolution is increased. In addition, the current measured is by a factor of approximately one order of magnitude higher than the reverse one without any loss of information. In the forward bias condition, the relative change of the current corresponding to the same amount of stress-induced defects is higher than in reverse bias conditions.

When gate voltage V_G is swept from threshold voltage V_T into accumulation, the generation/recombination maximum (pointer in Fig. 2) scans like a pointer along the interface toward the drain. The difference $\Delta I_{\text{G-R}}(V_G)$ between the measured current before and after stress provides information for the spatial distribution of the stress generated defects. Under the assumption that

a) the stress-induced defects are mainly interface defects
b) the electron and hole surface recombination rates are equal $\Delta S_n = \Delta S_p = \Delta S$
c) the energy distribution of the states near midgap is smooth

the excess generation/recombination current ΔI_F after stress can be expressed as [8]

$$\Delta I_F(V_G) = ew \int_{x_1}^{x_2} \Delta S(x) F(V_G, x)\, dx \tag{1}$$

with

$$F(V_G, x) = \frac{n(V_G, x)p(V_G, x) - n_i^2}{n(V_G, x) + p(V_G, x) + 2n_i} \tag{2}$$

where x_1 and x_2 are the boundaries of the depletion region along the surface, e the unit charge, W the transistor width, and n, p, and n_i, the carrier concentrations of electrons, holes and intrinsic carriers, respectively.

The function $F(V_G, x)$ is more sharply peaked in forward mode than in reverse mode, whereby both are compared at a position $x_m(V_G)$ where $n(V_G, x_m) = p(V_G, x_m)$. When $\Delta S(x)$ varies slowly in the vicinity of x_m we obtain a simple relation for $\Delta S(x_m)$ from (1)

$$\Delta S(x_m) = \frac{\Delta I_F(V_G)}{ew \int_{x_1}^{x_2} F(V_G, x)\, dx}. \tag{3}$$

A 2D-numerical simulation provides the shape of the peak position of $F(V_G, x)$ for the set of gate voltages corresponding to the measurement conditions. Thus the position of the peak in combination with Eq. 3 determines the spatial distribution of the excess surface recombination velocity $\Delta S(x)$. We note that $\Delta S(x)$ is proportional to the stress-generated interface defect density $\Delta N_T(x)$ near midgap which acts as recombination centers $\Delta S(x) = v_T \sigma N_T(x)$. v_T is the thermal velocity and σ is the defect capture cross section.

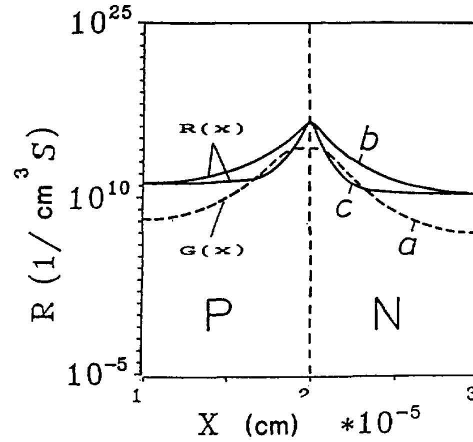


Fig. 4. Surface recombination rate $R(x)$ and generation rate $G(x)$ for the forward ($V_D = -0.2$ V) and reverse ($V_D = 0.2$ V) biased drain-to-substrate junction in accumulation ($V_G = -2.6$ V) at a constant surface recombination velocity $S = 100$ cm/s. (a) reverse bias: $V_D = 0.2$ V, $T = 300°$K; (b) forward bias: $V_D = -0.2$ V, $T = 300°$K; (c) forward bias: $V_D = -0.8$ V, $T = 77°$K.

For an n-channel LDD-MOSFET device, the difference of the forward bias drain-to-substrate current before and after stress, ΔI_F, with stress condition $V_G = 3$ V, $V_D = 8$ V, is plotted in Fig. 5 (solid line) and the extracted spatial distribution of the excess surface recombination velocity is given in Fig. 6. In this figure, the spatial distribution of the stress generated defect is obtained under the assumption that their capture cross section is $\sigma = 1 \cdot 10^{-15}$ cm^2. The maximum value of the defect density $N_T = 6 \cdot 10^{11}$ cm^{-2} corresponds to results published by Haddara [13]. To verify the assumption that the spatial variation of $\Delta S(x)$ is smoother in comparison with $F(V_G, x)$, we recalculate the excess recombination current ΔI_F according to (1), using predetermined $\Delta S(x)$ (+ in Fig. 5).

We would like to point out that the deep levels generating the diode current are not necessarily the same observed in "charge-pumping" and in "subthreshold-shift". Besides interface defects the diode current is in fact sensitive to bulk defects located in the bulk Silicon whereas the alternative methods are not. A small effect of such defects has in fact been proven. This observation suggests that, although the interface appears to be more susceptible to degradation, defects that have been related to the interface may partly be located in the substrate.

B. Defect Assisted Tunneling Processes

It has long been recognized that tunneling processes occur in MOS devices before and after stress. By measuring the "subthreshold" characteristics of hot-carrier stressed MOSFET's

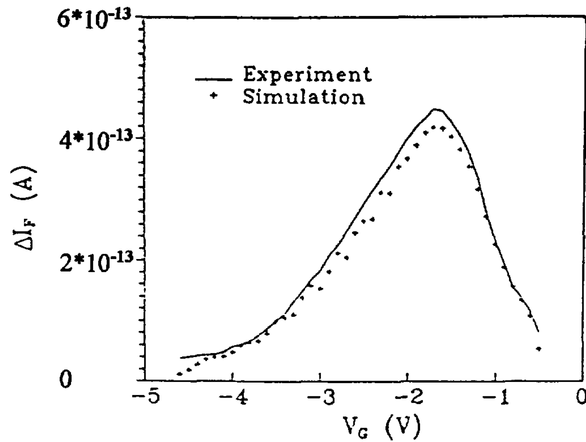


Fig. 5. Difference between the excess recombination current before and after stress, ΔI_F, as a function of gate voltage V_G (solid line), extracted from the experimental data in Fig. 6. The crosses are the result of a recalculated recombination current ΔI_F using Eq. 1, and a pre-determined $\Delta S(x)$ from Fig. 9.

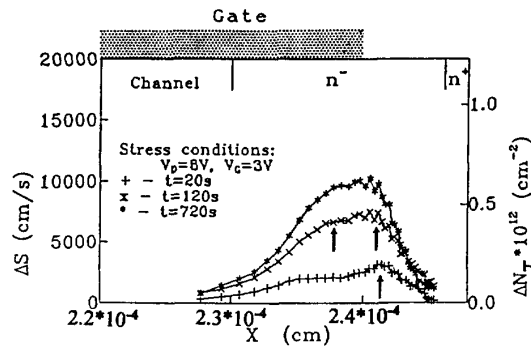


Fig. 6. Spatial distribution of the surface recombination velocity $\Delta S(x)$ and defect density $\Delta N_T(x)$, extracted from the data in Fig. 9.

resonant *intraband* tunneling processes, strongly affected by interface defect creation are observed [2]. On the other hand, *interband* tunneling currents in the gated-diode configuration in strong accumulation have been reported. When the field-induced p^+-n^+ junction is biased through the application of a drain-to-substrate voltage, a tunneling conduction mechanism can exist in a field-induced junction with a narrow transition width (~ 100 Å) and a high electric field ($\sim 10^6$ V/cm). In [16] the leakage current is shown to occur by tunneling of carriers from the valence to the conductance band. Band-to-band tunneling processes are described in [17] as a significant current leakage mechanism in VLSI devices under high bias conditions. In [18] the possibility of defect-assisted tunneling processes in germanium pre-amorphized MOSFET's is pointed out.

In earlier publications, the tunneling currents in the gated-diode in accumulation were observed on fresh devices without hot-carrier stress at high drain voltages V_D [19]. Our measurements were taken at small V_D values ($|V_D| < 0.3$ V) and high gate voltages ($|V_G| > 5$ V) leading to dimensions of the "active zone" of less than 100Å, by which we obtain a high

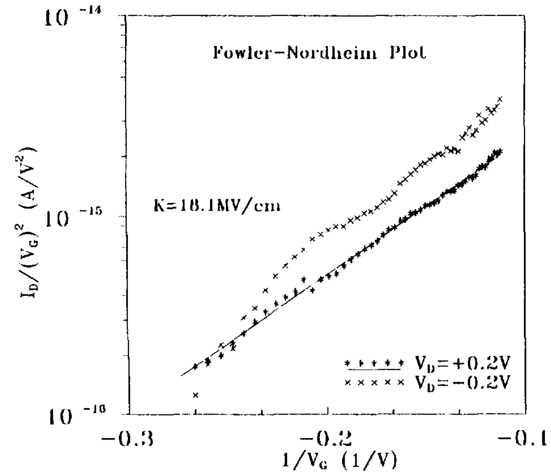


Fig. 7. "Fowler-Nordheim" plot of the reverse biased (solid line) and forward biased (dotted line) drain-to-substrate diode current I_D for gate voltage $V_G < -4$ V. From the slopes in the diagram, we calculate the effective tunneling barrier height E_B around mid-gap.

spatial resolution. This section of the paper aims to focus on defect-assisted tunneling processes in the forward *and* reverse mode of the gated-diode in contrast to the explanation given in [19]. In comparison with the distinctly peaked structure of the generation/recombination current before and after stress discussed in Section IV.A, we gain more insight into the transport mechanism of the gated-diode in strong accumulation before and after stress.

Regarding the fact, that the temperature dependence of the gated-diode current is weak in strong accumulation ($V_G < -5$ V), and that the "active zone" in the simulated potential distribution in Fig. 2(c) is very narrow (<100Å), we infer that tunneling currents become dominant over generation/recombination processes. Indeed, whereas the activation energy in depletion and inversion is about 0.65 eV—a reasonable value for the generation/recombination process in silicon, it is found to be 0.25 eV in strong accumulation.

We describe the leakage current in strong accumulation by "Fowler-Nordheim" interband tunneling [11] from the valence band to the conduction band through a triangular barrier by

$$I_T = \text{const} * E_S^2 \exp(-K/E_S). \tag{4}$$

Furthermore, we prove by simulations that the electric field E_S across the drain-to-substrate diode at the Si/SiO$_2$ interface is proportional to the gate voltage V_G, which is correct for V_G below than approximately -4 V as shown by simulation of the potential distribution. Thus we plot the experimental data, extracted from the gated-diode measurement in a "Fowler-Nordheim" plot as shown in Fig. 7 for the reverse and for the forward modes. It is observed that the leakage current follows a (I/E^2) versus $(1/E)$ relationship, characteristic of "Fowler-Nordheim" tunneling.

The effective barrier height E_B for indirect tunneling processes in silicon [20] can be calculated according to

$$K = \frac{8\pi^2\sqrt{2}(m^*)^{1/2}(E_{\text{gap}} - E_p)^{3/2}}{3eh} \tag{5}$$

where K describes the slope of the curve in MV/cm in the "Fowler-Nordheim" plot, m^* the effective mass of the carrier, E_{gap} the bandgap energy in silicon, and E_p the energy of the phonon necessary to conserve momentum with an indirect transition. As the value of m^* is not known exactly, an uncertainty in the values of E_B results. The values of m^* used are 0.33 m_o [21] from experiments and 0.198 m_o [22] from theory.

Reverse Bias Mode: In order to verify the assumption that tunneling processes occur, we plot the current I_D/V_G^2 vs. $1/V_G$ from the experimental data at the reverse gated-diode ($V_D = +0.2$ V) in a "Fowler-Nordheim" plot in Fig. 7. For gate voltages $V_G < -4$ V the straight lines show "Fowler-Nordheim" tunneling behavior. From the slope in Fig. 7 we obtain $K = 18$ MV/cm. We recalculate the effective barrier height using an effective mass of 0.198 m_o obtaining an energy barrier of 0.7 eV, while an effective mass of 0.33 m_o yields an energy barrier of 0.5 eV. These two calculated values indicate that the tunneling involves a state near mid-gap.

In view of the strong increase in tunneling current I_T after hot-carrier stress and the distinctly peaked structure for moderate gate voltage, we expect defect-assisted interband tunneling processes with effective barrier height around mid-gap to occur. The possible transport mechanisms are described in Fig. 8(a). Due to the observed decrease in I_T for lower temperature T (zero at $T = 4$°K) we refer to transport mechanism 2 in Fig. 8(a). An electron becomes thermally activated into the hot-carrier induced interface defect, from which tunneling by a decreased barrier height E_B into the conductance band occurs.

In the case of small drain voltage $V_D = V + 0.2$ V and high gate voltage V_G our measurements at the gated-diode indicate defect assisted interband tunneling processes. By increasing the drain voltage (typically $V_D > 2$ V) which was experimentally verified in [19], an additional contribution to the current was observed by band-to-band tunneling processes directly from the valence band to the conductance band (process 1 in Fig. 8(a)).

Forward Bias Mode: In contrast to the reverse mode, where direct band-to-band tunneling processes may occur at high gate or high drain voltages [19], those are forbidden in the forward mode because of the small band bending.

From the experimental data obtained for the tunneling current I_T in Fig. 3 we depict the "Fowler-Nordheim" plot for the forward gated-diode ($V_D = -0.2$ V) in strong accumulation in Fig. 7. The slope in the figure gives us $K = 18$ MV/cm for which (5) yields an effective barrier height E_B of about mid-gap. The peak structure in the diagram is described by tunneling processes via individual defects because of the narrow "active zone" in the forward mode (Fig. 4). In Fig. 8(b) we schematically describe the transport mechanism by defect-assisted interband tunneling processes in which an electron is tunneling from the degenerated conductance band into an interface defect, from which recombination with a hole in the degenerated valence band occurs. The degeneration in the valence band at the Si/SiO_2 interface is due to the strong accumulation at high negative V_G. The strength of the tunneling process is comparable to the well-known "excess-current" in the "Esaki-Diode" [11] because the degenerated p^+/n^+ region at the Si/SiO_2 interface acts like a tunneling diode with defects in the p^+/n^+ junction.

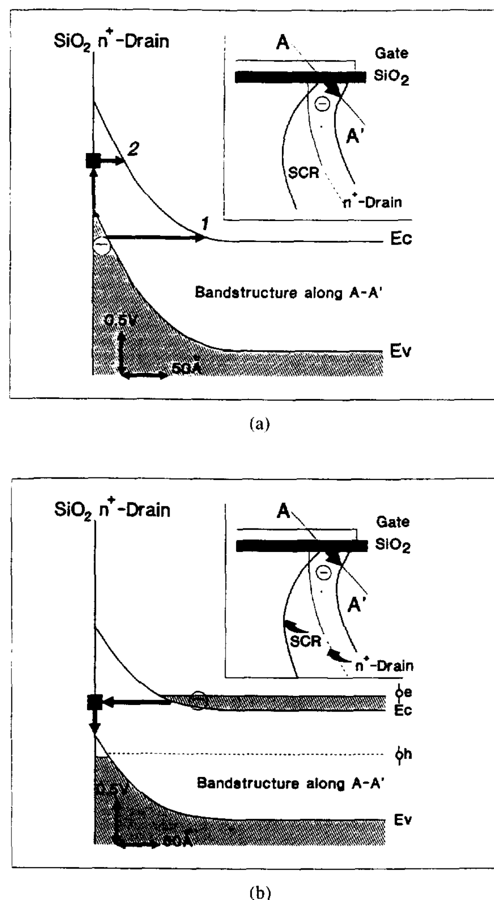


Fig. 8. Possible band-to-band tunneling processes for the (a) reverse biased and (b) forward biased gated-diode in strong accumulation. As indicated in the diagram, the transport mechanism takes place predominantly at the Si/SiO_2 interface.

The physical origin of the structure in Fig. 7 we explain by spatial scanning of individual defects due to the very narrow active zone ("pointer in Figs. 2(c) and 4). With decreasing gate voltage V_G in moderate accumulation, the active zone moves toward the drain and samples the spatial distribution of hot-carrier generated defects. The spatial scan of the active zone is approximately 100 nm when varying the gate voltage from $V_G = -0.5$ V to $V_G = -3.5$ V (generation/recombination current in Section IV.A). In strong accumulation ($V_G < -5$ V), the active zone moves into the drain slowly, for example by 10 nm when changing the gate voltage from $V_G = -5$ V to $V_G = -10$ V. Simultaneously the width of the active zone and thus the distance between valence band and conductance band is reduced to values smaller 10 nm. These tunneling processes are strongly enhanced by stress induced interface defects and thus become dominant for highly degraded devices even at moderate negative gate voltages.

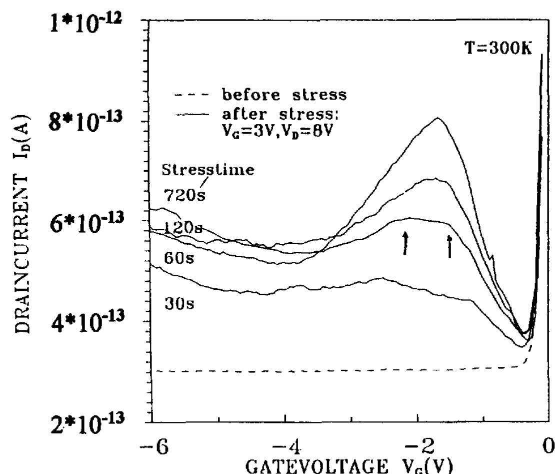


Fig. 9. Forward biased $V_D = -0.2$ V) drain-to-substrate current I_D as a function of gate voltage V_G for an n-channel LDD MOSFET before and after different times of stress at $V_G = 3$ V and $V_D = 8$ V.

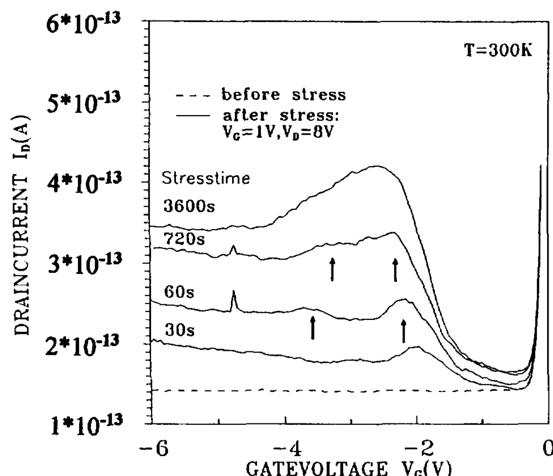


Fig. 10. Data analogous to Fig. 9, but with $V_G = 1$ V and $V_D = 8$ V applied for stress.

The degradation effect provides a peaking density of trap states (about 10^{12} cm^{-12}) in a narrow strip of width ≈100 nm located at the drain edge. For each micron of transistor width, the damaged strip has an area of 10^{-9} cm^2 and contains $10^2 10^3$ of trapped charges. In the narrow active zone with a width of approximately 5 nm in strong accumulation, just one to a few individual defects should be detectable by tunneling processes via interface defects.

At low temperatures the "active zone" decreases (typically to values less than 5 nm at 77°K) leading to a very sensitive "pointer" of nanometer dimensions for detecting individual defects. Those can be studied, before and after hot-carrier degradation, with the gated-diode in strong accumulation by tunneling and random-telegraph-noise measurements. Detailed experimental data for studying individual defects with the mesoscopic system in the gated-diode will be presented in a coming publication.

V. The Application of the Gated-Diode Current Method to Device Degradation

A. Discussion of the Results Regarding the Spatial Distribution of Hot-Carrier-Induced Deep Level Defects in LDD- MOSFETs

The gated diode measurement of an n-channel LDD- MOSFET device before and after stress is plotted in Figs. 9 and 10 under different stress conditions. The applied stresses are $V_G = 3$ V and $V_D = 8$ V in Fig. 9 and $V_G = 1$ V and $V_D = 8$ V in Fig. 10. As compared to Fig. 3, the tunneling regime is essentially avoided in Fig. 9 by choosing an LDD source/drain structure whereas the conventional profile in Fig. 3 leads to an interference of the tunneling regime with the generation/recombination regime.

It is interesting to note that owing to the fringing field effect in the n-channel LDD [14], the maximum of the stress created defects in Fig. 6 is located near the gate edge. Two maxima can be distinguished at each stress time. For the shortest stress time both are observed directly in the current (humps in Figs. 9 and 6) at $V_G = -1.2$ V and $V_G = -2.6$ V ($t = 30$ s). Two peaks at locations according to those detected experimentally were also found by simulation of LDD- MOSFET's [14] in the electric field distribution. One of the peaks ($V_G = -1.2$ V) corresponds to the maximum channel field, whereas the other peak refers to the fringing field of the gate edge. With increasing stress time, the channel maximum moves toward the n^+-part of the drain until it merges into the second maximum. The shift of the location of the channel maximum may be responsible by injected carriers but a definite proof for this hypothesis is missing. At this point we like to mention that besides the data shown in Figs. 6 and 9 a number of devices have been measured, all showing a weak but clear double peak structure.

The channel maximum dominates the degradation of the electric device characteristics. Its shift into the drain for increasing stress times supports an explanation given for the saturation in n-channel LDD device degradation vs time in terms of a series resistance increase [15]. While the electrical current parameters are highly influenced by the series resistance increase, the diode current remains virtually unaffected. In particular, the linear mode drain current degradation, dominated by the interface state generation above the channel region, saturates while the continuing degradation within the drain region is clearly observed in the diode current.

Lowering the gate voltage during stress leads to an increase of the electric field E_{LDD} at the gate edge, as simulations of the electric field distribution show [14]. This was experimentally verified in Fig. 10 with a stress condition $V_G = 1$ V and $V_D = 8$ V. Owing to the increase of the fringing field under these stress conditions in Fig. 10, we observe an increase in the related current hump at $V_G = -3.7$ V ($t = 60$ s) in comparison with Fig. 9 where a stress condition of $V_G = 3$ V and $V_D = 8$ V is used. In this way our data confirm the simulation in [14]. A decrease of the gate voltage V_G during

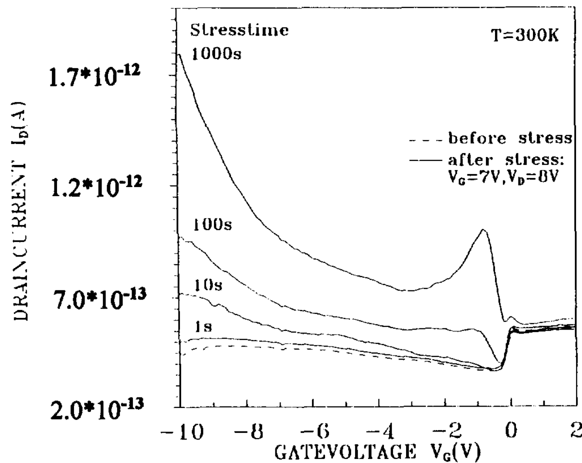


Fig. 11. Forward biased ($V_D = -0.2$ V) drain-to-substrate current I_D as a function of gate voltage V_G for an n-channel MOSFET before and after different times of stress at $V_G = 7$ V and $V_D = 8$ V.

stress tends to increase the interface state density due to the higher magnitude of the electric field E_{LDD}.

B. Different Stress Conditions Characterized by the Gated-Diode Measurement Technique

In this section we discuss alternating stress conditions in MOS devices. The formation of interface defects and/or fixed charges after hot carrier degradation as a function of stress conditions is currently discussed extensively in the literature (cf. [23]). Stress conditions varied for $V_G = 1$ V to 7 V with fixed drain voltages lead to varying injections of hot electrons and/or holes and thus to varying ratios for the creation of interface defects and fixed charges.

It is not the purpose of this section to present a complete model for hot-carrier degradation, which has been published elsewhere [24], but to emphasize and illustrate how the gated-diode technique yields additional valuable information for understanding the degradation behavior.

It is well-established, that a stress condition $V_G = 3$ V, $V_D = 8$ V usually leads to the creation of interface traps rather than fixed negative charges. This behavior was recently described quantitatively in [25], showing that the contribution of negative oxide charges is less than 3% of the total interface defect density. Our measurements with the gated-diode configuration in Fig. 3 confirm the data in [25]. Interface defect creation is the dominant effect, apparent from the distinct peak structure of the generation/recombination current at moderate gate voltages and the strong increase in tunneling current I_T in strong accumulation with an increasing stress time t.

In Fig. 11 we characterize the stress condition $V_G = 7$ V, $V_D = 8$ V for different stress times t on the same test structure used previously. We compare the experimental data in Fig. 11 with the one in Fig. 3 at a stress condition $V_G = 3$ V, $V_D = 8$ V. The distinct generation/recombination peak which samples the spatial distribution of hot-carrier-induced interface defects is shifted to more positive gate voltages. This shows that a significant trapping of negative charges occurs. The increase in the tunneling current I_T and the peak occurrence of increasing stress times is explained by additional interface defect formation at the Si/SiO_2 interface. Thus our experimental data confirm the results in [18] obtained with the "charge-pumping" method. In addition to interface defects, fixed negative charges build up as a consequence of hot-electron injection at high gate voltages.

For a stress condition of $V_G = 1$ V, $V_D = 8$ V (Fig. 10) we observe the generation/recombination peak at lower negative gate voltages, which we explain by the build-up of positive fixed charges due to hole injection. The weak increase of the tunneling current I_T and the generation/recombination peak, even at long stress time, is explained by a smaller interface defect density than that for the stress conditions mentioned before.

It is important to note that under the lowest gate voltage stress condition, interface traps are still being generated, but they do not influence the electrical characteristics very much because they are masked by the positive charge at the drain [3], [24].

The fact that fixed positive charges can be neutralized by hot-electron injection, is verified experimentally in Fig. 12. In a first step we stressed the devices with a condition $V_G = 1$ V, $V_D = 8$ V which leads to the formation of interface defects and fixed positive charges. After a short injection of hot-electrons ($V_G = 7$V, $V_D = 8$V), the previously positive fixed charges are compensated by the injected electrons, which causes a shift of the generation/recombination current peak to more positive gate voltages. Additional injection of hot electrons with longer stress times t leads to the build-up of negative fixed charges (due to hot-electron injection) and to the creation of additional interface defects, to which we attribute the formation of a second generation/recombination hump in Fig. 12 (stress time $t = 60$ s). This finding is somewhat analogous to the results discussed in Section V-B, where two spatially separate interface defect distributions were discussed that originated from two electric field peaks occurred separated by a certain distance.

VI. Conclusion

In this paper the unique features of the gated-diode technique have been reviewed and its important role in the understanding of the hot-carrier behavior of MOSFET's has been highlighted. Although the cases presented only deal with degradation under DC and alternating injection stress conditions, the gated-diode measurement can also be expected to play a key role in the study of AC stress hot-carrier degradation.

The key issue of this paper is to have shown that the spatial distribution of hot-carrier induced interface traps can be determined precisely. In particular in the region of gate-to-drain overlap this information has been obtained for the first time. In this way, the gated-diode technique becomes a very powerful tool and a reliable quantitative method for determining the interface density and its spatial distribution in

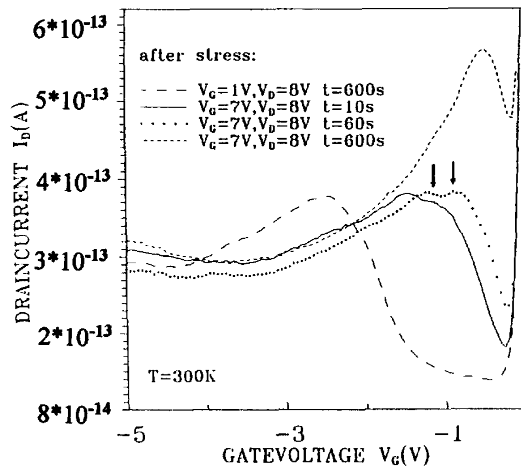


Fig. 12. Data analogous to Fig. 11, but with $V_G = 1$ V and $V_D = 8$ V applied for stress, followed by $V_G = 7$ V, $V_D = 8$ V.

MOS transistors especially when 2D-numerical simulation is applied. The influence of hot-carrier induced interface defects and/or fixed charges under different stress conditions is understood more deeply by detecting generation/recombination and tunneling currents with the gated-diode technique.

References

[1] S. A. Abbas and R. C. Dockerty, "N-channel IGFET design limitations due to hot-electron trapping," *IEDM Tech. Dig.*, p. 35, 1975.

[2] A. Asenov, M. Bollu, F. Koch and J. Scholz, "On the nature and energy distribution of defect states caused by hot electrons in Si," *Appl. Surf. Sci.*, vol. 30, p. 319, 1987.

[3] A. V. Schwerin, W. Hänsch and W. Weber, "The relationship between oxide charge and device degradation: A comparative study of n- and p-channel MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-34, p. 2493, 1987.

[4] G. Groesenecken, H. E. Maes, N. Beltran and R. F. De Keersmaecker, "A reliable approach to charge-pumping measurements in MOS-transistors," *IEEE Trans. Electron Devices*, vol. ED-31, p. 42, 1984.

[5] M. G. Ancona, N. S. Saks and D. Mc. Carthy, "Lateral distribution of hot-carrier induced interface traps in MOSFET's," *IEEE Trans. Electron Devices*, vol. 35, p. 2221, 1988.

[6] A. S. Grove and D. J. Fitzgerald, "Surface effects on p-n junctions: Characteristics of surface space-charge regions under nonequilibrium conditions," *Solid-State Electr.*, vol. 9, p. 783, 1966.

[7] T. Giebel and K. Goser, "Hot-carrier degradation of n-channel MOSFET's characterized by a gated-diode measurement technique," *IEEE Electron Device Lett.*, vol. 10, p. 76, 1989.

[8] A. Acovic, M. Dutoit and M. Ilegems, "Characterization of hot-electron-stressed MOSFET's by low-temperature measurements of the drain tunnel current," *IEEE Trans. Electron Devices*, vol. ED-37, p. 1467, 1990.

[9] P. Speckbacher, A. Asenov, M. Bollu, F. Koch and W. Weber, "Hot-carrier-induced deep-level defects from gated-diode measurements on MOSFET's," *IEEE Electron Device Lett.*, vol. 11, p. 95, 1990.

[10] A. Asenov, J. Berger, P. Speckbacher, F. Koch and W. Weber, "Spatially-resolved measurements of hot-carrier generated defects at the Si-SiO_2 interface," in *Proc. INFOS '91*, W. Eccleston, M. Uren, Eds. New York: Adam Hilger, 1991, p. 247.

[11] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed., 1981.

[12] T. Poorter and P. Zoestbergen, "Hot carrier effects in MOS transistors," *IEDM Tech. Dig.*, p. 100, 1984.

[13] H. Haddara and S. Cristoloveanu, *Solid-State Electron.*, vol. 29, p. 767, 1986.

[14] M. K. Orlowski and C. Werner, "Model for the electric fields in LDD MOSFET's—Part II: Field distribution on the drain side," *IEEE Trans. Electron Devices*, vol. 36, p. 382, 1989.

[15] Q. Wang, W. H. Krautschneider, M. Brox and W. Weber, "Time dependence of hot-carrier degradation in LDD nMOSFET's," in *Proc. ESSDERC '91*.

[16] S. Banerjee, D. Coleman, W. Richardson and A. Shah, "Leakage mechanisms in the trench transistor DRAM cell," *IEEE Trans. Electron Devices*, vol. 35, p. 108, 1988.

[17] G. Q. Lo, A. B. Joshi and Dim-Lee Kwong, "Hot-carrier-stress effects on gate-induced drain leakage current in n-channel MOSFET's," *IEEE Trans. Electron Device Lett.*, vol. 12, p. 5, 1991.

[18] J. Y. Choi, P. K. Ko, C. Hu and W. F. Scott, "Hot-carrier-induced degradation of metal-oxide-semiconductor field-effect transistors oxide charge versus interface traps," *J. Appl. Phys.*, vol. 65, no. 1, p. 354, 1989.

[19] A. Acovic, M. Dutoit and M. Ilegams, "Characterization of hot-electron-stressed MOSFET's by low temperature measurements of the drain tunnel current," *IEEE Trans. Electron Devices*, vol. 37, p. 1467, 1990.

[20] E. O. Kane, "Theory of tunneling," *J. Appl. Phys.*, vol. 32, p. 83, 1961.

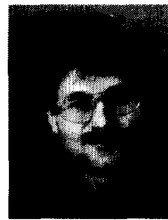
[21] A. G. Chynoweth, W. L. Feldman and R. A. Logan, "Ionization rates for electrons and holes in Silicon," *Phys. Rev.*, vol. 121, p. 684, 1961.

[22] P. N. Butcher, K. F. Hulme and J. R. Morgan, *Solid-State Electron.*, vol. 3, p. 358, 1962.

[23] S. A. Lyon, *Appl. Surf. Sci.*, vol. 39, p. 552, 1989.

[24] P. Heremans, R. Bellens, G. Groesenecken and H. E. Maes, "Consistent model for the hot-carrier degradation in n-channel and p-channel MOSFET's," *IEEE Trans. Electron Devices*, vol. 35, p. 2194, 1988.

[25] W. Hänsch, A. V. Schwerin and F. Hofmann, "A new self-consistent approach to investigating MOSFET degradation," *IEEE Electron Device Lett.*, vol. 11, p. 362, 1990.



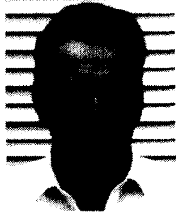
Peter Speckbacher was born in Traunstein, Germany, in 1960. He received the Dipl. Phys. degree in 1989 and the Dr. rer. nat. degree in 1992, both from the Technische Universität München.

From 1989 to 1992, he was working toward the Dr. rer. nat. degree under a cooperative program with the Research Laboratories of Siemens AG, Munich and Daimler Benz AG, Ulm. His dissertation investigated the research of hot-carrier effects in MOS devices. Since 1990, he has been with the Research Laboratories of Dr. Johannes Heidenhain GmbH, Traunreut, Germany, were he is engaged in electron-beam-lithography and optical-lithography. His research interests and activities are focussed on the development of solid-state integrated sensors, integrated optical devices, fabrication and application of micro- and nanostructures.

Josef Berger was born in Watzendorf, Germany, in 1963. He received the Dipl. Phys. degree from the Technische Universität München in 1991. His Master's thesis research involved the study of hot-carrier effects in MOS devices.

He joined the Bayerische Versicherungskammer, Germany, in 1993 were he has been engaged in the development of ecological planning and environmental protection.

A. Asenov, photograph and biography not available at the time of publication.



Frederick Koch was born in Berlin, Germany on January 6, 1937. He received the B.A. from New York University in 1958, and the Ph.D. in physics from the University of California, Berkeley in 1962.

He was an Assistant Professor at Berkeley from 1962 to 1963, and an Assistant Full Professor, University of Maryland, College Park, from 1963 to 1972. Since 1972, he has been a Professor of Physics, Technical University München, Munich, Germany. His research interests are in semiconductor physics and devices with emphasis on surface and interfacial phenomena.

Werner Weber was born in Ruhstorf, Germany, in 1952. He received the Dipl. Phys. degree from the Technische Universität München in 1976 and the Dr. rer. nat. degree from the Ludwig-Maximilians-Universität München in 1981.

In 1981, he was on a one-year assignment at the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, where he worked in the field of semiconductor thin films. Since 1983, he has been with the Research Laboratories of Siemens AG, Munich, Germany. He is engaged in MOS physics and basic circuit design and has authored or co-authored over 60 papers. In 1992, he received the award of the German Information Technology Society for a publication on physical effects of hot-carrier degradation. Since 1995, he has been managing a project on basic circuits in nonvolatile memories.

Dr. Weber is a member of the German Physical Society (DPG) and the German Information Technology Society (ITG).