examined devices submitted to HBM pulses, with a 10 ns rise time and a 150ns time constant. These pulses are applied on the collector of the simulated devices, while their emitter and substrate are grounded. The thermal boundary condition is considered to be a constant temperature of 300K at the bottom of the simulation domain which corresponds to the substrate electrode.

Fig. 2 shows the calculated transient voltage responses of the two transistors submitted to a low stress level (peak current I_p = 8mA/μm) and to a high stress level (I_p = 15mA/μm). This figure shows that initially the voltage across the device increases up to the triggering level (points A and A′, Fig. 2). The simulated values of the triggering voltage of the two devices are in good agreement with the experimentally measured values (Table 1). In fact, the triggering voltages under transient conditions are lower than under static conditions owing to capacitive effects and the existence of displacements currents. Accordingly, the devices enter in snap-back and the voltage decreases up to the sustaining level (points B and B′, Fig. 2). When this occurs, the greatest part of the discharge current flows laterally from the collector to the emitter under the field oxide (PBL, see Fig. 1*a*), while the conductivity of the base region is significantly modulated [6], which leads to a decrease in the resistance of the discharge path. However, the applied current still increases, since its maximum value is attained at 10ns (points C and C′, Fig. 2), also causing the terminal voltage to increase. Subsequently, the current decays exponentially and when it reaches the value for which the snap-back condition is not satisfied anymore, the terminal voltage goes back to the triggering voltage of the device (points E and E′, Fig. 2).

Fig. 2 also shows that at high stress level the terminal voltage of the CPW device increases after the current has reached each peak value, and that it decreases in the case of the ODPW device (points D and D′, Fig. 2). This is a thermal effect and can be attributed to the decrease of the mobility as well as to the increase of the avalanche voltage at high temperatures. The calculated maximum temperature transients for the different stress levels of the examined devices (Fig. 3) show that at high stress level the maximum temperature in the CPW device is considerably higher than in the ODPW device. This fact is probably the cause of the observed different failure levels of the tested transistors.

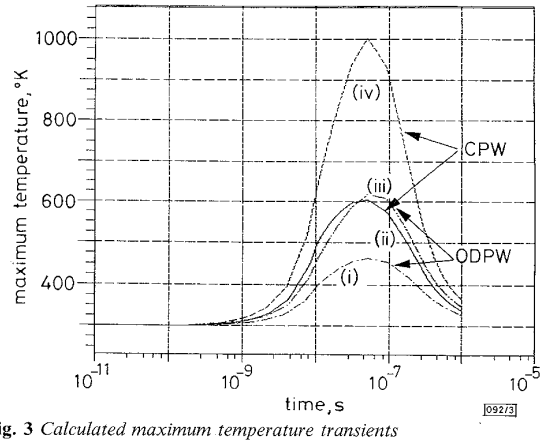

Fig. 3 *Calculated maximum temperature transients*

Low stress level: (i) and (ii)
High stress level: (iii) and (iv)

The increase in the lattice temperature is proportional to the product of the electric field by the current density. The electric field is lower in the ODPW device owing to the lower sustaining voltage in comparison with the CPW device. Conversely, Fig. 4 shows that, in the case of the ODPW device, the current density under the field oxide, when the discharge current reaches its peak value (i.e. 15mA/μm), is lower and spreads deeper in the base region, than in the case of the CPW device. This effect can be attributed to the additional implantation existing in the ODPW devices.

Conclusion: A simple process modification (over-doped *P*-well) can lead to a faster activation of a classical field oxide transistor and to a significant increase of the failure level. The higher performance of these devices is caused by the lower heat dissipation provoked by the lower electric field and by the spreading of the discharge current deeper in the device.

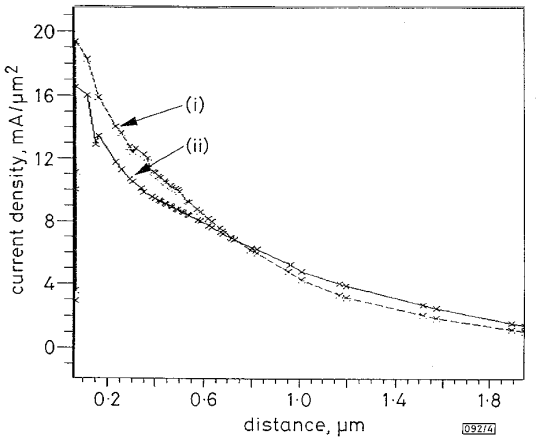

Fig. 4 *Calculated current density under PBL for high stress conditions*

(i) CPW, (ii) ODPW

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Gate recess engineering of pseudomorphic $In_{0.30}GaAs/GaAs$ HEMTs

N.I. Cameron, S. Murad, H. McLelland, A. Asenov, M.R.S. Taylor, M.C. Holland and S.P. Beaumont

Indexing terms: High electron mobility transistors, Semiconductor devices

The authors report how the performance of 0.12μm GaAs *p*HEMTs is improved by controlling both the gate recess width, using selective dry etching; and the gate position in the source drain gap, using electron beam lithography. *p*HEMTs with a transconductance of 600mS/mm, off state breakdown voltages >2 V, f_T of 120GHz, f_{max} of 180GHz and MAG of 13.5dB at 60GHz are reported.

Introduction: The Schottky gate contact of a GaAs *p* HEMT is usually formed in a shallow etched recess. The depth of the recess sets the gate to channel spacing and controls the gate source capacitance, transconductance, pinch off voltage and high frequency current gain; and the extent of the recess towards the drain affects the drain extension of the gate depletion region and controls the feedback elements: gate drain capacitance, output conductance and hence high frequency power gain. The width of the recess also dramatically affects the access resistance of the device [1]. It is desirable to engineer the size and shape of the recess to control device performance. The recess is typically formed either by wet or dry etching, both of which may be either selective or non-selective [2 – 5]. When a non-selective etch is used the gate recess depth is usually controlled by etching until a desired saturated drain current is achieved [2, 4]. No independent control over the width of the recess is afforded. Where a selective etch is used, tighter control over the etch depth is generally achieved as the depth is accurately set by the epitaxial layer structure [3, 5]. In addition, lateral over etching of the recess can be used to increase the gate recess width provided the selectivity is high enough to prevent further vertical etching. Wet etches do not generally have sufficient selectivity to allow extended overetching, and wetting effects can also degrade lateral etch control. With selective dry etching issues such as ion induced damage, material deposition and etch anisotropy must be addressed. Here we report on the use of a highly selective low damage process employing $SiCl_4/SiF_4/O_2$ to engineer the gate recess of 0.12μm GaAs *p* HEMTs.

Fabrication: The GaAs *p*HEMT layer structure was grown as follows: 600nm GaAs buffer, 10nm $In_{0.3}Ga_{0.7}As$ channel, 2.5nm $Al_{0.2}Ga_{0.8}As$ spacer, $7 \times 10^{12}cm^{-2}$ Si delta doping layer, 10nm $Al_{0.2}Ga_{0.8}As$ barrier, 2.5nm GaAs surface buffer, 5nm $Al_{0.2}Ga_{0.8}As$ etch stop layer and 30nm $4 \times 10^{18}cm^{-3}$ GaAs cap. This layer structure is fairly conventional except that a thin GaAs surface buffer layer is used to prevent deep oxidation of the AlGaAs exposed in the gate recess. In addition the structure is quite aggressively scaled for optimum short gate device performance in terms of In content, doping density and channel depth. After removal of the GaAs cap the layer was found to have N_{sh} of $2.4 \times 10^{12}cm^{-2}$ and μ_H of $4000cm^2/Vs$. The *p*HEMT fabrication process has been described in detail by Asenov *et al.* [6]. and further evidence for low damage etching and details of the $SiCl_4/SiF_4/O_2$ process was reported by Murad *et al.* [7]. We used $SiCl_4/SiF_4$, which forms a very tight recess and does not etch laterally, to produce *p*HEMTs in which the gate fills the recess (0nm gate offset). The addition of oxygen enhances the lateral etch rate, and allowed devices with 25 and 50nm gate offsets to be produced. Electron beam lithography allowed the position of the gate to be varied with respect to the source contact. A number of devices with 0, 25 and 50nm gate offsets and 0.5 and 0.75μm spacing between the edge of the source and centre of the gate were fabricated and characterised at DC. The RF performance was evaluated by on wafer measurement from 0–60GHz for the following four devices: 0nm gate offset devices with 0.5 and 0.75μm source to gate spacing, a 25nm gate offset device with 0.75μm spacing and a 50nm offset device with 0.5μm spacing.

Device performance: DC measurements of the off state breakdown voltage were made with a constant drain current of 1mA/mm, following the procedure of Bahl and del Alamo [8]. Devices with 25 and 50nm gate offsets showed an off state breakdown of BV_{ds} = 2.14V (1σ = 0.23V) while 0nm offset devices exhibited variable and lower breakdown in the range BV_{ds} = 0.5 to 1.3V. The variation was probably caused by variations in the contact area between the edge of the gate and the highly doped GaAs cap. Similarly the 25 and 50nm offset devices had BV_{dg} = 4.77V (1σ = 0.70V) and the 0nm devices had BV_{dg} = 3.4 to 4.4V. All the devices exhibited an on state (V_{gs} = 0V) breakdown voltage of 5V, characterised by a rapid and destructive increase in drain current probably caused by breakdown in the channel. These results agree with those of Geiger *et al.* [9], who reported an on state breakdown voltage of 5V, independent of the recess size, and recess dependent off state breakdown behaviour. Otherwise we found no variation in the DC parameters against gate source spacing and recess width. Average values from four separate fabrication lots and best standard deviation values were: I_{dss} = 630mA/mm (1σ = 41mA/mm), g_m = 600mS/mm (1σ = 41mS/mm) and V_{th} = –0.97V (1σ = 16mV).

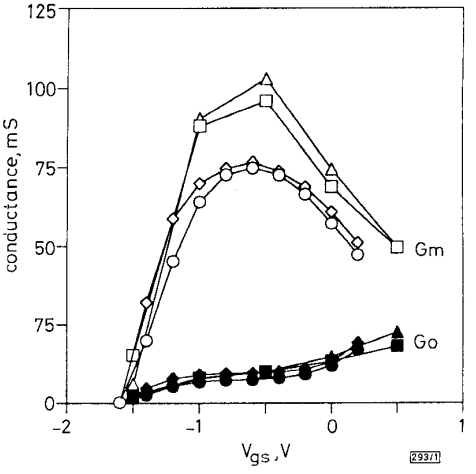

Fig. 1 *pHEMTs with filled gate recess, 0nm, have the highest transconductance, the gate source spacing has less influence, at V_{ds} = 1.5V shown, output conductance is similar for all devices*

○ 50nm, 0.75μm; ◇ 25nm, 1μm; □ 0nm, 1μm; △ 0nm, 0.75μm

Fig. 1 shows the transconductance G_m and output conductance G_o, at V_{ds} = 1.5V, extracted by a small signal equivalent circuit fit to the measured s-parameters. Higher G_m was observed for devices in which the gate was positioned close to the source, but much larger G_m was obtained for the *p*HEMTs in which the gate filled the recess compared with devices with significant gate offset. Similar behaviour was observed for C_{gs} and so an extrinsic f_T of 120GHz was obtained for all devices. All of the *p*HEMTs have

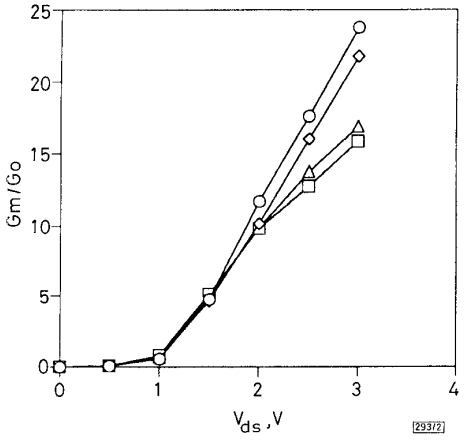

Fig. 2 *pHEMTs with largest gate offset have highest G_m/G_o ratio, the gate source spacing has a smaller influence*

V_{gs} = 0V
symbols as for Fig. 1

similar threshold voltage and peak G_m occurred at similar gate bias, suggesting that the gate to channel separation did not vary. Little variation in the output conductance (G_o) can be observed in Fig. 1. However, G_o is strongly dependent on the drain bias and, as Fig. 2 shows, variations in the ratio of G_m/G_o are observed at large V_{ds}. Similar trends were observed with C_{gs}/C_{gd}. In all the devices, as the drain field increases the gate depletion region extends toward the drain and G_o is reduced. The effect is particularly strong for the 25 and 50nm gate offset devices, although there is also a small reduction in G_o brought about by moving the gate closer to the source. The ratio of G_m/G_o and C_{gs}/C_{gd} determine the high frequency power gain, and thus the best gain is found at V_{ds} = 3V as shown in Fig. 3. The 50nm gate offset device has the highest MAG of 13.5dB at 60GHz which gives a cutoff frequency (f_{max}) of 180GHz.

The size of the gate recess and the position of the gate affects the access resistances R_s and R_d. To examine the effect of the recess size only, the extracted values of R_s and R_d were added: values of 1 to 1.5, 3.5 and 4.3Ω were found for the 0, 25 and 50nm

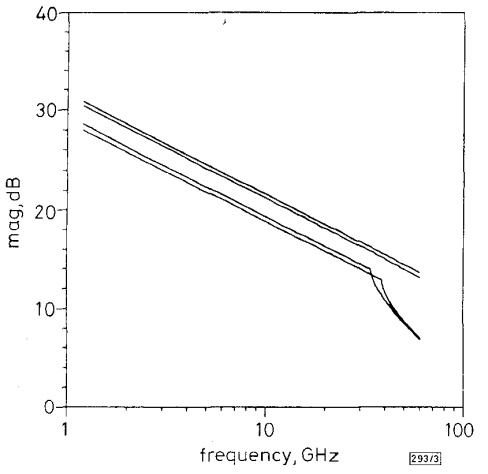

Fig. 3 *pHEMTs with gate offset of 50nm have the best magnitude of 13.5dB at 60GHz and f_{max} of 180GHz (at V_{ds} = 3V and V_{gs} = 0V), gate source spacing has negligible influence*

Lower two lines: 0nm
Above these: 25nm
Top line: 5nm

gate offset devices, respectively. Very little dependence on recess width and gate position was found for the other equivalent circuit elements, except for gate inductance (L_g) which was strongly dependent on the recess size with values of 1.1 to 1.3, 4.2 and 13.6pH obtained for the 0, 25 and 50nm gate offset *p*HEMTs. This indicates that the recess alters the shape of the magnetic field surrounding the gate.

Conclusions: We have used selective reactive ion etching in $SiCl_4/SiF_4/O_2$ to engineer the gate recess of a 0.12μm pseudomorphic $In_{0.30}GaAs/GaAs$ HEMT. Improved off state breakdown voltage, BV_{ds} > 2V, *MAG* = 13.5dB at 60GHz and f_{max} = 180GHz were achieved. Other parameters such as DC transconductance, saturated drain current density, threshold voltage and f_T were not dependent on the gate offset. The gate position was also varied and was found to have a much smaller influence than the recess.

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Ion-implanted 0.4μm wide 2-D MESFET for low power electronics

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Indexing terms: MESFETs, Ion implantation

Two-dimensional (2-D) MESFETs with 0.4μm channel widths have been fabricated on ion-implanted *n*-GaAs material. The 2-D MESFET uses sidewall Schottky contacts on either side of an Si-doped channel to laterally modulate the current. The peak drain current is 370mA/mm and the peak transconductance is 295mS/mm at room temperature. The narrow channel effect and channel length modulation have been reduced in this device.

Introduction: Recently, we proposed and fabricated a new transistor called the 2-D metal-semiconductor field effect transistor (2-D MESFET) in which sidewall Schottky contacts on either side of an AlGaAs/InGaAs/GaAs heterostructure laterally deplete the narrow 2-D electron gas (2-DEG) channel [1 – 3]. One of the principal advantages of this device is that the narrow channel effect (NCE) [4], which leads to parasitic currents at the gate edges in a top-gated structure, is eliminated by the unique sidewall gate geometry. Thus, 2-D MESFET device widths may be scaled to deep submicrometre dimensions without degradation of the electrical characteristics [5]. In this Letter, we investigate a new 2-D MESFET fabricated on ion-implanted, bulk *n*-GaAs material. The ion-implanted 2-D MESFET uses the same geometry as the PHEMT 2-D MESFET and therefore experiences no deterioration from the NCE at submicrometre widths. In addition, the ion-implanted GaAs material is cheaper to fabricate and more compatible with commercial GaAs IC fabrication processes than the MBE-grown AlGaAs/InGaAs/GaAs heterostructure devices. Also, despite a lower mobility in the bulk *n*-GaAs than in the InGaAs structure, preliminary comparisons indicate that the DC electrical characteristics of submicrometre ion-implanted 2-D MESFETs are comparable to those of submicrometre PHEMT 2-D MESFETs [6].

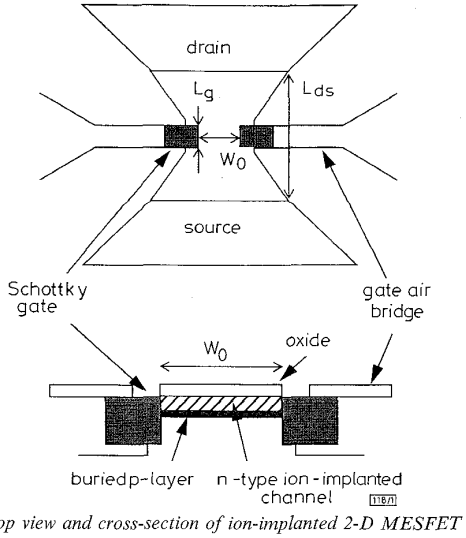

Fig. 1 *Top view and cross-section of ion-implanted 2-D MESFET*