RTS Amplitudes in Decananometer MOSFETs: 3-D Simulation Study

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***Abstract*—In this paper we study the amplitudes of random telegraph signals (RTS) associated with the trapping of a single electron in defect states at the Si/SiO_2 interface of sub-100-nm (decananometer) MOSFETs employing three-dimensional (3-D) "atomistic" simulations. Both continuous doping charge and random discrete dopants in the active region of the MOSFETs are considered in the simulations. The dependence of the RTS amplitudes on the position of the trapped charge in the channel and on device design parameters such as dimensions, oxide thickness and channel doping concentration is studied in detail. The 3-D simulations offer a natural explanation for the large variation in the RTS amplitudes measured experimentally in otherwise identical MOSFETs. The random discrete dopant simulations result in RTS amplitudes several times higher compared to continuous charge simulations. They also produce closer to the experimentally observed distributions of the RTS amplitudes. The results highlight the significant impact of single charge trapping in the next generation decananometer MOSFETs.**

***Index Terms*—Degradation, MOSFET, numerical simulation, random dopants, RTS, trapping.**

I. INTRODUCTION

MASS production MOSFETs have reached decananometer (sub-100-nm) dimensions with Intel shipping, in 2001, 60-nm transistors in the 130-nm technology node Pentium IV [1]. Prototype 30-nm MOSFETs have already been developed [2], [3] for the 65-nm technology node expected in 2005 [4]. Trapping of a single carrier charge in defect states near the Si/SiO_2 interface and the related local modulation in carrier density and/or mobility [5]–[7] in an area comparable with the characteristic device dimensions, will have a profound effect on the drain and gate current [8] in such MOSFETs. Corresponding random telegraph signals (RTS) with amplitudes larger than 60% have already been reported at room temperature in decananometer channel width devices [9]. Current fluctuations on such a scale will become a serious issue, not only as a source of excessive low-frequency (LF) noise in analog and mixed-mode circuits [10], [11], but also in dynamic memories [12] and potentially in digital applications. Depending on the device geometry a single [13], or few discrete charges [14] trapped in hot carrier or radiation created defect states will be sufficient to cause a pronounced degradation in decananometer MOSFETs.

With few exceptions [9] the recent experimental studies of RTS in MOSFETs, focusing on devices with dimensions larger than 100 nm [8], [15]–[17], lag the current scaling trends. Modeling and simulation can help to forecast the RTS amplitudes that should be expected in decananometer devices. However, the modeling and simulation efforts are mainly restricted to simple analytical models [5], [18] and 2-D numerical simulation studies [19] and, for example, fall short of explaining the wide range of RTS amplitudes observed in otherwise identical devices [20] and particularly their statistical distribution. There are suggestions that due to surface potential fluctuations and channel nonuniformity strategically located traps influence the magnitude and the spreading of RTS amplitudes [10], [11], [20]. However such potential fluctuations have been associated mainly with oxide nonuniformity [18] and fixed and trapped interface charges [21]. Only recently has the impact of the random discrete dopants, which are one of the major sources of fluctuations in decananometer devices [22], been considered [23].

In this paper we present a systematic and comprehensive 3-D simulation study of the impact of single charge trapping on the current in decananometer MOSFETs with characteristic dimensions in the range from 100 to 30 nm. The study is carried out using an "atomistic" device simulator which take into account not only localized individual trapped carrier charges but also the random discrete dopant distribution in the simulated devices [24]. We investigate the effect of the trapped charge position and the MOSFET design parameters on the RTS amplitudes comparing both continuous doping and random discrete dopants in the simulations.

II. SIMULATION APPROACH

The 3-D drift-diffusion simulator employed in this study is described in detail elsewhere [24]. A fine grid with typical spacing of 1 nm is used to resolve the "atomistic" effects associated with individual trapped charges and random discrete dopants. Density gradient (DG) corrections can be included in the simulations to account for quantum confinement effects [25]. It is well known that the drift-diffusion approach, which does not include nonequilibrium and ballistic transport, cannot predict accurately the current in decananometer devices. It, however, handles properly the electrostatics of the trapped charge through the 3-D solution of the Poisson equation and the corresponding local change in the channel carrier concentration, and therefore the associated change in the current, which determines the relative RTS amplitudes.

Our investigations focus on the change in the drain current induced by the trapping of an individual electron in an acceptor type interface state at the Si/SiO_2 interface in n-channel MOSFETs assuming continuous or discrete random doping. The simulations do not take into account the local modulation in the

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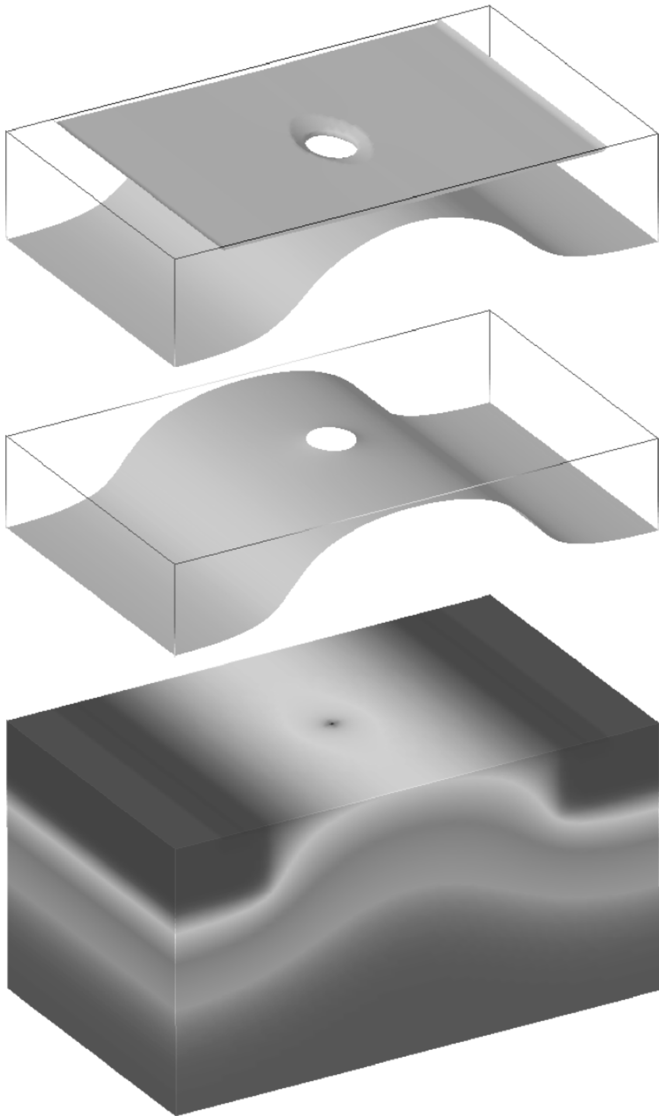

Fig. 1. (Bottom) Potential distribution in a 30×30 nm MOSFET with a single trapped electron in the middle of the channel. Equiconcentration contours corresponding to (middle) classical and (top) quantum mechanical simulations are also shown.

mobility associated with the trapped charge. It is believed that carrier number fluctuations dominate the RTS amplitudes and the LF noise in n-channel MOSFETs [9]. The simulated devices have a simplified structure with uniform channel doping $N_A = 5 \times 10^{18}$ cm^{-3}, oxide thickness $t_{\rm ox} = 3$ nm and junction depth $x_j = 7$ nm. The effective channel length $L_{\rm eff}$ and width $W_{\rm eff}$ are quoted as device dimensions in the paper. In the simulation experiments one design parameter is typically varied while the rest remain as specified above.

The potential distribution in a 30×30 nm n-channel MOSFET with continuous doping and one electron trapped exactly in the middle of the channel is presented at the bottom of Fig. 1 for gate voltage equal to the threshold voltage and low drain voltage $V_D = 10$ mV. The equiconcentration contour in the middle represents results from classical simulation with maximum electron concentration at the Si/SiO_2 interface. Quantum corrections using the density gradient formalism are incorporated in the solution corresponding to the equiconcentration contour plotted at the top and result in maximum electron concentration approximately 1.5 nm below the interface. A circular region with reduced electron concentration surrounds the trapped electron.

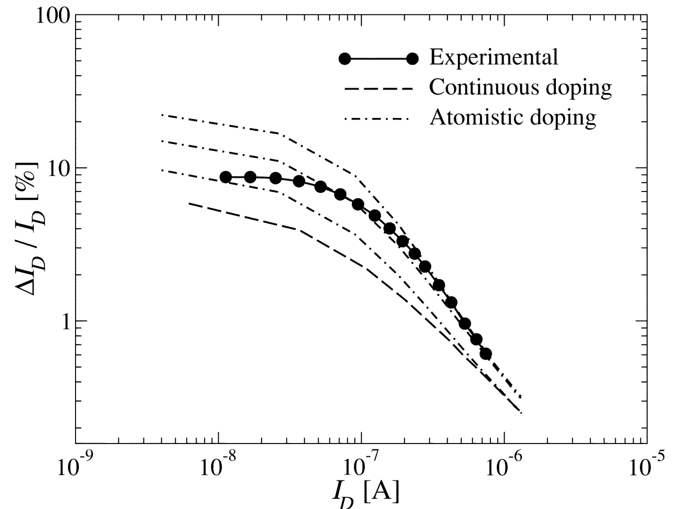

Fig. 2. Dependence of the RTS amplitude on the drain current in a relatively large MOSFET with channel width 0.1 μm, channel length 1 μm, oxide thickness 20 nm and channel doping 10^{17} cm^{-3} measured and simulated at $V_D = 50$ mV.

In order to validate our simulation approach in Fig. 2, we compare results of our simulations with experimentally measured dependence of the RTS amplitude on the drain current in a relatively large MOSFET [26] with channel width 0.1 μm, channel length 1 μm, oxide thickness 20 nm and channel doping 10^{17} cm^{-3}. Both the simulations using continuous doping distribution and random discrete dopants follow the general feature of the experimental dependence, which saturates in weak inversion and decreases with the drain current in strong inversion. However the maximum saturated value of the RTS amplitude obtained for a single electron trapped in the middle of the channel in the continuously doped case, and plotted in Fig. 2, is lower than the measured one. The introduction of random discrete dopants results in an increase and large variation of the RTS amplitudes. In Fig. 2, we have depicted only three curves from three different random dopant configurations and positions of the trapped electron, which reproduce closely the experimental results.

III. Continuous Doping

In order to understand the generic dependence of the RTS amplitudes on the position of the trapped charge and the MOSFET design parameters we first consider continuous doping charge in our simulations. It is clear that at low drain voltage an electron trapped in the middle of the channel, where the potential barrier between the source and the drain has a maximum (see Fig. 1), will have the largest impact on the current, resulting in a maximum RTS amplitude. The corresponding low drain voltage ($V_D = 10$ mV) dependence of the relative RTS amplitudes on the drain current for a set of square MOSFETs ($L_{\rm eff} = W_{\rm eff}$) covering the range of device dimensions from 100 to 30 nm is presented in Fig. 3. The effect of the trapped charge is large at low drain current

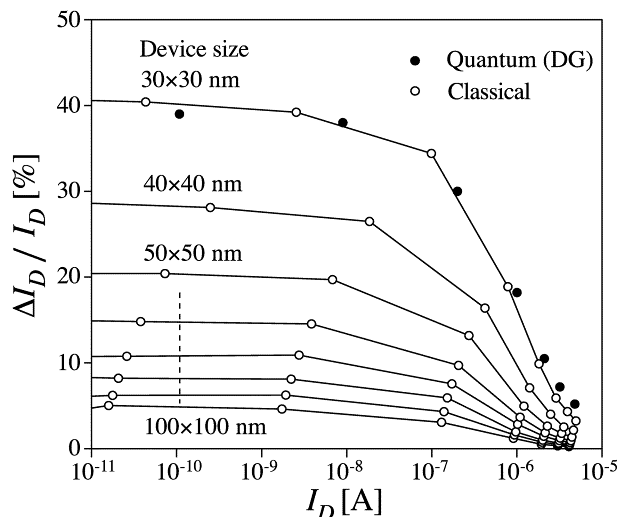

Fig. 3. Dependence of the relative RTS amplitude on the drain current for a set of square MOSFETs of different sizes and a single electron trapped in the middle of the channel at $V_D = 10$ mV.

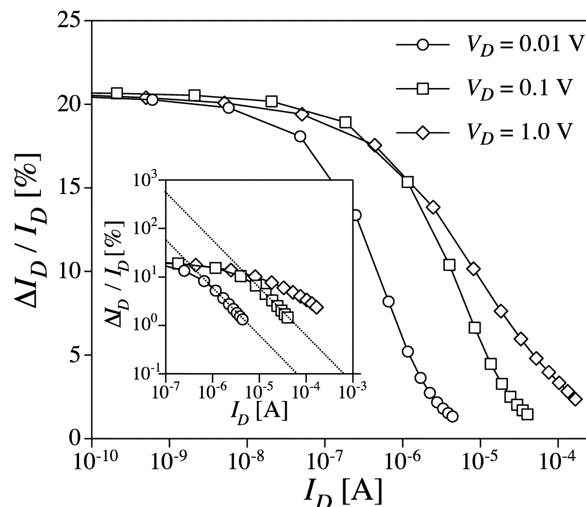

Fig. 4. Dependence of the relative RTS amplitude on the drain current for a 50 × 50-nm MOSFET with a single electron trapped in the middle of the channel at different drain voltages.

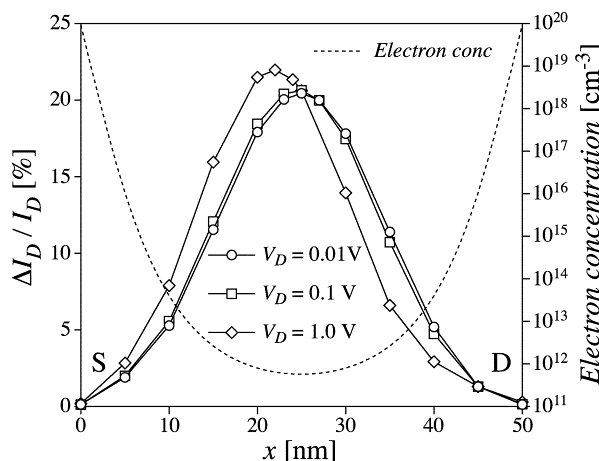

Fig. 5. Dependence of the relative RTS amplitude on the position of the trapped charge along a line running from the source to the drain through the center of the channel of a 50 × 50-nm MOSFET at different drain voltages. The electron concentration at the interface along the channel is also presented.

(weak inversion) and decreases near and above threshold due to screening of the Coulomb potential of the trapped charge by the inversion layer charge. It should be noticed that the maximum RTS amplitude in the 30 × 30 nm MOSFET is more than 40% in the subthreshold region and remains larger than 5% in strong inversion. The inclusion of quantum corrections in the simulations for the 30 × 30 nm MOSFET (black dots in Fig. 3) shows less impact of the trapped charge in the subthreshold region due to the fact that the charge is separated by approx. 1nm from the maximum in the quantum carrier distribution. In strong inversion the impact in the QM simulations is stronger because of less screening coming from the distant and somewhat spread inversion layer charge. In the transitional region between weak and strong inversion the two effects practically cancel. However, quantum effects produce little difference overall in the RTS amplitudes therefore the further results presented in this paper are based on classical simulations.

The impact of the drain voltage on the relative RTS amplitudes for the 50 × 50 nm MOSFET from Fig. 3 is illustrated in Fig. 4. For the midchannel position of the trapped electron the increase in the drain voltage does not produce appreciable change in weak inversion but increases the RTS amplitude above threshold. The behavior at low drain voltage (10 and 100 mV) is in good agreement with the experimental observations [18] showing a plateau in the relative RTS amplitudes in weak inversion and a roll-off proportional to I_D^{-1} in strong inversion at room temperature resulting in a slope of one on a double-logarithmic plot (see the inset in Fig. 4). Such roll-off slope is expected from an elementary number fluctuation estimate yielding a $1/(W_{\text{eff}} L_{\text{eff}} N_s)$ amplitude [5] when the mobility variation is neglected (N_s is the inversion layer carrier concentration per unit area). At high drain voltage, however, there is a departure from the above simple theory, which is applicable to the linear mode of operation, and the roll-off slope is reduced.

The dependence of the relative RTS amplitude on the position of the trapped charge along a line running from the source to the drain of the 50 × 50 nm MOSFET through the center of the channel is illustrated in Fig. 5. The dependence at low drain voltage has a bell-shape with a maximum in the middle of the channel and is close to zero value near the source and drain metallurgical p–n junctions. More than two orders of magnitude variation offers a first order explanation for the experimentally observed scatter in the RTS amplitudes in identical MOSFETs [18],[20],[21] without any speculative assumption about the trap nature, cross section, etc. The large variation can be understood in terms of the simple number fluctuation model bearing in mind the variation of potential and the corresponding inversion layer carrier concentration N_s along the channel. N_s increases from the center of the channel toward the source and the drain, which should result in $1/N_s$ reduction in the RTS amplitude. In the source and the drain region where the carrier concentration, determined by the junctions doping profile, is high the trapping of an electron produces minute RTS amplitudes. With the increase in the drain voltage the maximum of the potential barrier in the channel shifts from the middle toward the source and so does the maximum in the RTS amplitude distribution. The slight increase in the maximum RTS amplitude in this case

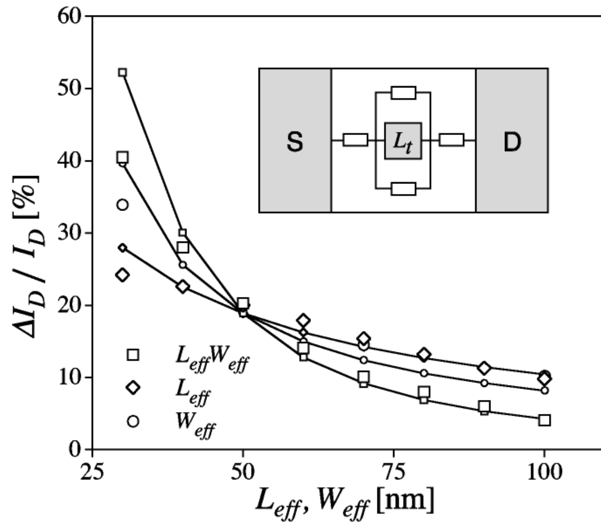

Fig. 6. Dependence the relative RTS amplitude on the characteristic device dimensions for a set of square MOSFETs with fixed effective channel width, fixed effective channel length, and with square geometry, at $V_D = 10$ mV. Stand alone symbols—numerical simulation; continuous lines—analytical model (1).

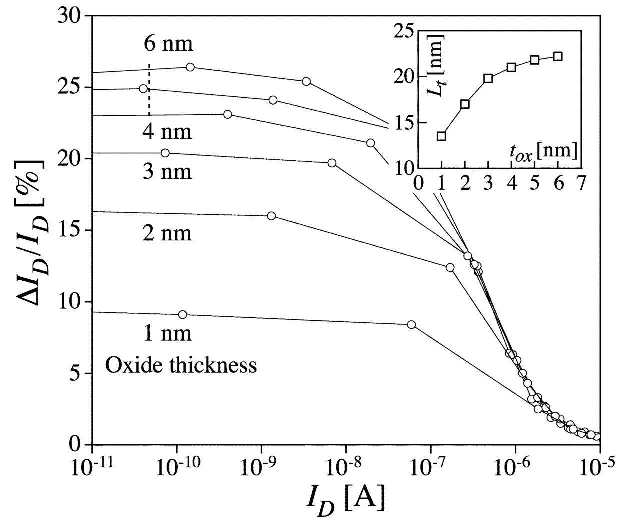

Fig. 7. Dependence of the relative RTS amplitude on the drain current for a set of 50 × 50-nm MOSFETs with different oxide thickness and a single electron trapped in the middle of the channel at $V_D = 10$ mV.

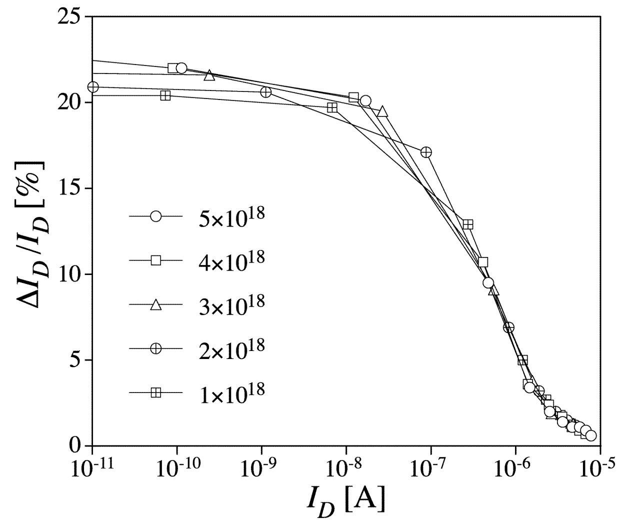

Fig. 8. Dependence of the relative RTS amplitude on the drain current for a set of 50 × 50-nm MOSFETs with different channel doping concentration and a single electron trapped in the middle of the channel at $V_D = 10$ mV.

is associated with the drain voltage induced modulation (shortening) of the conducting channel. The shift in the bell-shaped distribution with the increase in the drain voltage offers an explanation for the controversy in the drain voltage dependence of the RTS amplitude observed experimentally [6], [27]. The RTS amplitudes associated with electrons trapped in the source half of the channel will increase with the increase in the drain voltage while those resulting from trapping in the drain end of the channel will decrease.

The dependence of the RTS amplitude in weak inversion $(I_D = 10^{-10}$ A) on the effective channel length and width are plotted in Fig. 6. There is a departure from the straight $1/(W_{\mathrm{eff}}L_{\mathrm{eff}})$ dependence predicted by the number fluctuation theory [5], particularly at channel lengths/widths below 50 nm, when the simulated channel length and width dependences are distinctly different. The observed nonsymmetrical behavior can be reproduced by a simple geometrical model which introduces, similarly to [18], a square channel exclusion region with length L_t. Assuming zero conductivity in the exclusion region and solving the equivalent resistor network, illustrated as an inset in Fig. 6, yields the following expression for the relative RTS amplitude:

$$\frac{\Delta I_D}{I_D} = \frac{L_t^2}{(L_{\mathrm{eff}} - L_t)(W_{\mathrm{eff}} - L_t) + W_{\mathrm{eff}}L_t}. \quad (1)$$

The analytical estimate of L_t for an electron trapped at the interface between two media (Si and SiO_2) with different dielectric constants is a difficult task particularly in the presence of a gate electrode screening. Therefore we use L_t as a fitting parameter in (1) which we adjust to the relative RTS amplitude of the 50 × 50 nm MOSFET (the crossover point of the three dependences in Fig. 6). A good match between the numerical results (stand alone symbols) and the simple model (continuous lines) is obtained for $L_t = 19$ nm. As expected this value of L_t is larger than the estimated 8 nm in [18] which is based on the shape of the Coulomb potential in bulk Si and does not take into account the presence of SiO_2 at the interface. The RTS amplitude roll-off in strong inversion can be included in (1) through the reduction of L_t due to inversion charge screening, but again doing this analytically is a cumbersome task for the interface between two media with different dielectric constants.

Fig. 7 illustrates the influence of the oxide thickness on the maximum RTS amplitudes (midchannel trapped electron) in a set of 50 × 50 nm MOSFETs with different oxide thickness. In the subthreshold region the screening of the Coulomb potential of the trapped electron by the carriers in the gate increases with the reduction in the oxide thickness resulting in a reduction of the maximum RTS amplitudes. The corresponding reduction of the exclusion region length L_t in (1), obtained by fitting the numerically simulated relative RTS amplitudes in weak inversion $(I_D = 10^{-10}$ A), is presented as an inset in the same figure. In strong inversion the screening from the inversion layer completely masks the effect of the gate screening and, for all devices,

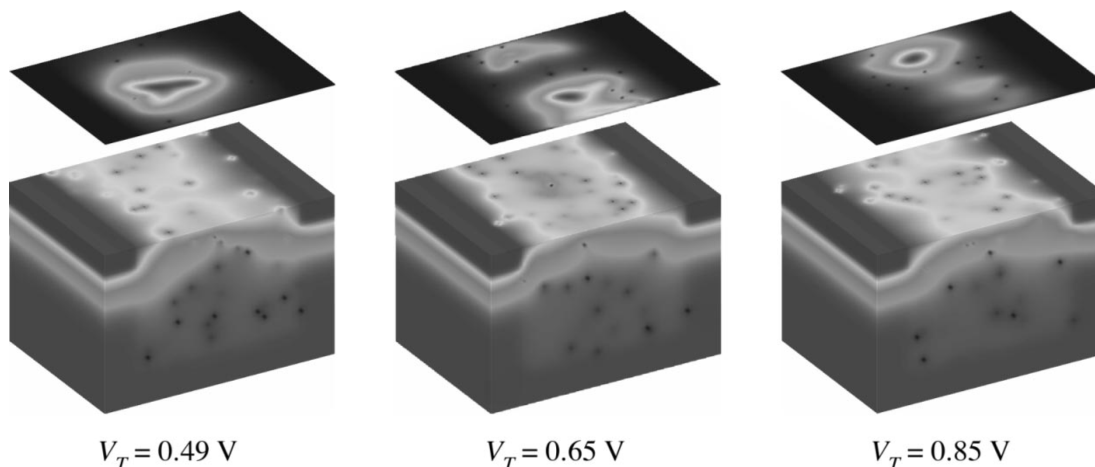

Fig. 9. Potential distribution in three 50 $\times$ 50-nm MOSFETs with discrete random dopants in the channel region. The positional dependence of the magnitude of the RTS amplitudes associated with the trapping of a single electron is mapped in the plane above each transistor.

an exclusion region length of 4 nm describes well the RTS amplitudes at $I_D = 10^{-5}$ A.

The impact of the channel doping concentration on the maximum RTS amplitude in a set of 50×50 nm MOSFETs is illustrated in Fig. 8. The relatively weak influence of the doping concentration on the amplitudes in weak inversion is associated with screening of the trapped charge by the holes at the depletion layer edge. With an increase in the doping concentration the width of the channel depletion layer decreases slowly in proportion to $1/\sqrt{N_A}$ and the screening becomes stronger.

IV. Random Discrete Dopants

In this section, we study the impact of the random discrete dopants in decananometer MOSFETs on the magnitude and the distribution of RTS amplitudes. Random discrete dopants are a major source of surface potential fluctuations in decananometer transistors [23], [25]. For example, in the 50×50-nm transistor simulated in Section III there are, on average, 170 acceptors in the channel depletion region. Their actual number follows a Poisson distribution and their positions are random. At the same time, in well controlled technology the surface density of the fixed charge is of the order of 10^{10} cm^{-2} which is equivalent to less than one additional discrete charge in every fourth 50×50-nm MOSFET. It is clear that the fixed oxide charge and the interface states have a negligible effect on the precursor potential fluctuations compared to the random dopants in such devices. The surface potential fluctuations result in current percolation through the valleys in the potential landscape which dominate the current flow, particularly in weak inversion where the ionised acceptor charges are not screened by the electrons in the inversion layer. Trapping of electrons in defect states positioned along the dominant current percolation paths will produce RTS with large amplitudes.

The potential distribution in three 50×50-nm MOSFETs with discrete random dopants in the channel region is presented in Fig. 9. The devices are selected from a sample of 200 transistors with randomly generated dopant distributions to have the smallest, the largest and a middle range threshold voltage in the distribution. The plane above the channel of each transistor maps the RTS amplitudes associated with the trapping of a

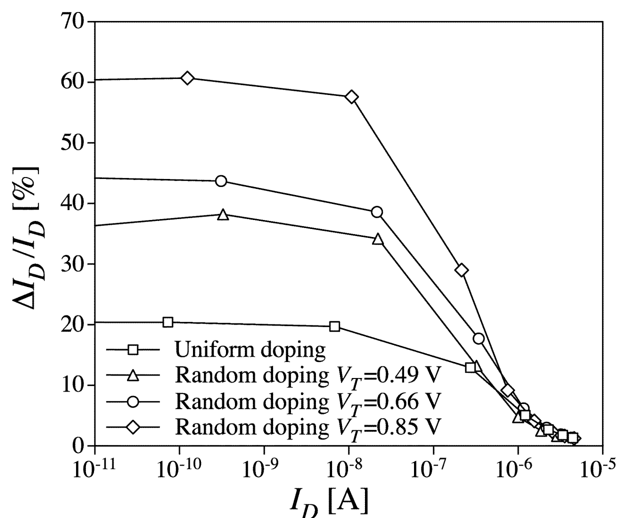

Fig. 10. Dependence of the maximum RTS amplitudes on the drain current for three 50×50-nm devices with different atomistic doping. The corresponding dependence obtained from continuous doping simulations is also presented.

single electron at the interface. Unlike the continuous doping simulations, the largest RTS amplitudes in this case are not in the middle of the channel but in the regions with the deepest valley in the potential landscape corresponding to the highest density of percolating current.

The drain current dependence of the maximum RTS amplitudes in the three transistors from Fig. 9 is compared in Fig. 10 with the corresponding continuous doping dependence from Fig. 3. In weak inversion the maximum RTS amplitudes in the discrete dopant simulations are always higher compared to the continuous doping simulations. The difference is more than three times for the discrete dopant MOSFET with the largest threshold voltage. Inspection shows that in the device with the lowest threshold voltage $(V_T = 0.49 \text{ V})$ a lucky arrangement of dopants leaves almost half of the channel relatively low doped and highly conductive. The trapping of a single electron there has a less dramatic effect compared to the other simulated devices with discrete random dopants. The MOSFET with the largest threshold voltage $(V_T = 0.85 \text{ V})$ has a large concentration of dopants in the middle of the channel leaving

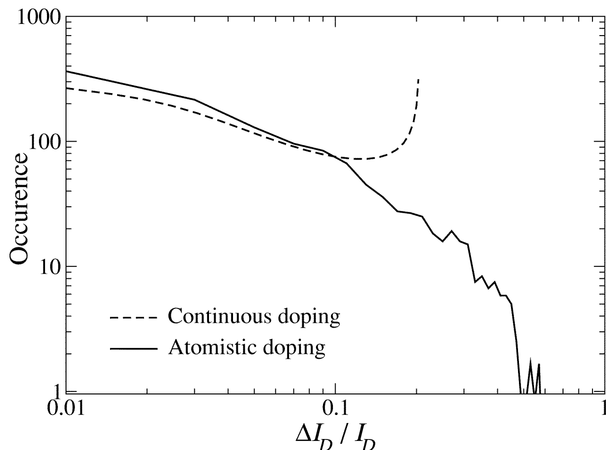

Fig. 11. Simulated distribution of RTS amplitudes in 50 × 50-nm MOSFETs with continuous doping and random discrete dopants.

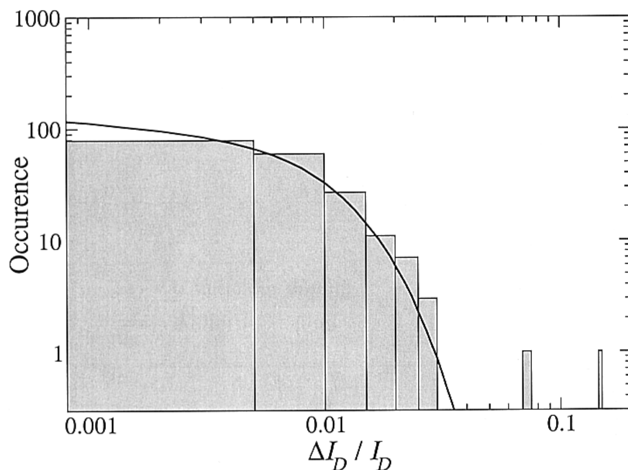

Fig. 12. Experimentally observed distribution of RTS amplitudes in 187 500 × 500-nm MOSFETs.

very narrow paths for the percolating current. The trapping of a single electron in the vicinity of a dominant but narrow current channel has a strong effect on the overall current in this device.

The simulations using continuous and the discrete doping produce distinctly different distributions of the relative RTS amplitudes illustrated in Fig. 11. The continuous doping simulations result in a two headed distribution with high density at both the smallest and the highest amplitudes. Such a distribution follows from the bell-shaped positional dependence of the RTS amplitudes illustrated in Fig. 5 where traps near the source/drain are responsible for the peak in the distribution at low RTS amplitudes, while traps along the middle of the channel result in the peak in the distribution at high amplitudes. In the discrete dopant simulation the distribution has high density at the small amplitude end, as in the continuous doping case, and a low-density tail at the high amplitude end, due to trapping along narrow current percolation paths, which is in good qualitative agreement with the experimentally observed distribution obtained from 187 different 500 × 500-nm MOSFETs illustrated in Fig. 12 [21].

V. Conclusions

Trapping and detrapping of a single charge will have a dramatic effect on the operation of the next generation decananometer MOSFETs. Relative RTS amplitudes of the order of 50% percent in weak inversion and more than 5% in strong inversion could be expected in square devices corresponding to the 65-nm technology node. This estimate is based only on the local modulation of the conducting charge in the channel and does not include the effect of the trapped charge on the channel mobility. The shape of the potential barrier in the channel and the corresponding inversion layer charge distribution result naturally in a several order of magnitude variation in the RTS amplitudes in otherwise identical devices. When the size of the region affected by the trapped charge ($\sim$ 10–20 nm in weak inversion) becomes comparable to the characteristic device dimensions we observe a departure from the $1/(W_{\rm eff} L_{\rm eff})$ dependence of the RTS amplitudes.

The random dopant induced surface potential fluctuations and the associated current filamentation are responsible for a significant increase in the RTS amplitudes in weak inversion compared to simulation results assuming a continuous doping distribution. The use of realistic random dopant distributions in the simulations also modifies the distribution of the RTS amplitudes in an ensemble of macroscopically identical but microscopically different devices reproducing the experimentally observed high magnitude tail of the distribution.

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