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Modeling the Impact of the Trench Depth on the Gate-Drain Capacitance in Power MOSFETs

Olayiwola Alatise, Nii-Adotei Parker-Allotey, Michael Jennings, Phil Mawby, Ian Kennedy and George Petkos

***Abstract*— The trench depth is important in low-voltage trench MOSFETs because it affects the switching losses through the gate-drain capacitance (C_{GD}). The dependence of C_{GD} on the trench depth is investigated by analytical modeling and experimental characterization. An analytical model that relates the trench depth, trench bottom oxide thickness, n$^-$ layer doping and the drain voltage (V_D) to C_{GD} is developed and validated by experimental measurements. Trench-MOSFETs with thick-bottom-oxides have been fabricated with 1.3, 1.5, 1.7 and 2-µm deep trenches. CV measurements show that C_{GD} is proportional to the trench depth at low V_D and becomes increasingly independent of trench depth as V_D is increased. The model is used to show that this is due to C_{GD} being dominated by the oxide capacitance at low V_D and the depletion capacitance at high V_D. The fact that the average thickness of the trench bottom oxide decreases as the trench depth increases (because of additional sidewall oxide overlapping the drain) means that the impact of the trench depth is highest at low V_D where the depletion capacitance is ineffective.**

***Index Terms*— Gate-drain capacitance, Switching losses, Trench MOSFET**

I. INTRODUCTION

Trench MOSFETs are known to outperform vertical DMOS and lateral MOSFETs as far as conduction losses are concerned. This is due to the fact that the channel current is vertical; hence, the channel density can be more readily increased by shrinking the cell pitch. However, the penalty for increased channel density is higher gate charge which translates to higher switching losses especially for power devices in fast switching applications [1]. The overlap between the gate and the drain makes the gate-drain capacitance (C_{GD}) higher for trench MOSFETs compared with other power devices. Fig. 1 shows the cross-sectional image of a trench MOSFET and a schematic illustrating the terminal capacitances inherent in the design. Since increasing the trench depth increases the gate-drain overlap, it is expected to cause higher C_{GD} and has been demonstrated to do so by previous studies [2]. To mitigate this, concepts like the thick bottom oxide (TBO), the W-gated trench [3] and the split gate have been developed to reduce C_{GD} without compromising on the conduction loss benefit of the trench structure. However, deeper trenches are known to reduce conduction losses because of increased modulation of the accumulation charge at the drain. Optimizing the trench depth is therefore very important. The objective of this study is to develop a deeper understanding of the relationship between the trench depth and the C_{GD} by correlating analytical equations to experimental measurements.

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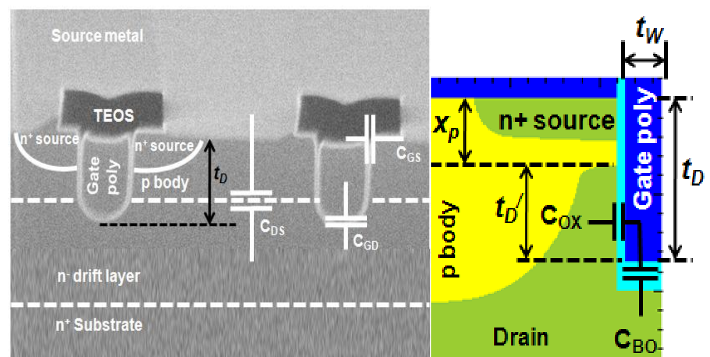

Fig. 1. A cross-sectional image and schematic of a Trench MOSFET showing the internal capacitances.

II. GATE-DRAIN CAPACITANCE MODELLING

C_{GD} is the series combination of the trench bottom oxide capacitance and the depletion capacitance. The potential difference between the drain and the gate will be shared between the gate oxide and the depletion in the semiconductor. Equation (1) below shows a simplified version of how the oxide and depletion capacitance relate with C_{GD} whereas equation (2) shows the depletion width [4]

$$C_{GD} = \left(\frac{t_W + 2t_D^{/}}{t_{cell}}\right)\left[\frac{C_{GOX}C_D}{C_{GOX} + C_D}\right] \quad (1)$$

$$W_D = \frac{\varepsilon_{Si}}{C_{GOX}}\left(\sqrt{1 + \frac{2V_D C_{GOX}^2}{q\varepsilon_{Si}N_D}} - 1\right) \quad (2)$$

where $t_D^{/}$ is the trench extension into the drain, t_W is the trench width (see Fig. 1), t_{cell} is the cell pitch, C_{GOX} is the gate oxide capacitance density, C_D is the depletion capacitance density, ε_{Si} is the dielectric constant of silicon, V_D is the drain voltage, q is the electric charge and N_D is the doping concentration of

the drift layer. Because the trench bottom is usually deeper than the p-body extension, ($t_D^{/}$ in Fig. 1 is greater than zero) C_{GOX} in (1) is a parallel combination of the sidewall oxide capacitance (C_{OX}) and the bottom oxide capacitance (C_{BO}). For conventional MOSFETs, $C_{OX} = C_{BO}$ and for TBO MOSFETs, $C_{OX} > C_{BO}$ (thinner sidewall oxides). Since the MOS capacitor at the trench bottom is a parallel combination of the bottom oxide capacitance (which is independent of t_D) and the trench sidewall capacitance (which is dependent on t_D), then C_{GOX} can be expressed mathematically as

$$C_{GOX} = \frac{t_D^{/} C_{OX} + t_W C_{BO}}{t_D^{/} + t_W} = \frac{(t_D - x_P) C_{OX} + t_W C_{BO}}{(t_D - x_P) + t_W} \quad (3)$$

where x_P is the p-body extension (see Fig. 1). Hence, as the trench depth is increased, $t_D^{/}$ increases and it can be seen from (3) that C_{GOX} tends towards C_{OX}. Likewise, as the trench depth is decreased, $t_D^{/}$ decreases and C_{GOX} tends towards C_{BO}. Equation (3) applies to both conventional and TBO MOSFETs. For conventional MOSFETs, it can be seen in (3) that $C_{GOX} = C_{OX}$. It can also be seen from (3), that in the case of zero trench extension into the drain ($t_D^{/}=0$), then $C_{GOX}=C_{BO}$. The depletion capacitance C_D can be derived as the ratio of the dielectric constant of silicon to the depletion width.

$$C_D = C_{GOX}\left(\sqrt{1+\frac{2V_D C_{GOX}^2}{q\varepsilon_{Si} N_D}} - 1\right)^{-1} \quad (4)$$

By substituting (4) into (1), an equation for the C_{GD} is derived showing its dependence on the trench depth and the drain voltage.

$$C_{GD} = C_{GOX}\left(\frac{t_W + 2t_D^{/}}{t_{cell}}\right)\left(1+\frac{2V_D C_{GOX}^2}{q\varepsilon_{Si} N_D}\right)^{-\frac{1}{2}} \quad (5)$$

Equation (5) shows that the as C_{GOX} and/or V_D increases, the dependence of C_{GD} on V_D tends increasingly towards $C_{GD}\, \alpha\, V_D^{-0.5}$. Equation (5) is useful in the sense that it can help device designers make a quick calculation of the C_{GD} given the drift layer doping concentration (which will be fixed for a certain device voltage rating) and the thickness of the bottom oxide. This equation refers specifically to trench MOSFETs (both conventional and TBO); hence modifications will have to be made to optimize it for split-gate and other variants. Fig. 2 shows a series of normalized C_{GD} curves generated using the model in (5) with $N_D = 1 \times 10^{16}$ cm^{-3}. The capacitances have been normalized by using capacitance at 1.3 µm trench depth as the reference. These characteristics have been generated without taking the dependence of C_{GOX} on the trench depth into account i.e. a constant value of C_{GOX} is used in (5). Next, the dependence of C_{GOX} on the trench depth is taken into account by using (3) and (5) to generate C_{GD} *vs.* V_D characteristics for different trench depths. It can be seen in Fig. 3 that the C_{GD} for the different trench depths converge at higher V_D which is not the case in Fig. 2. To understand this, we need to refer back to (1), where the C_{GD} is expressed as a series combination of C_{GOX} and the C_D and to (3) where C_{GOX} is expressed as a parallel combination of C_{OX} and C_{BO} (and the dependence of C_{GOX} on the trench depth is taken into account). At low V_D, the depletion width is small; hence C_D is large meaning that C_{GD} is dominated by C_{GOX}. However, as V_D increases, C_D decreases due to the widening depletion width and C_{GD} becomes dominated by C_D; hence the differences in the C_{GOX} become irrelevant. In other words, as V_D increases, (5) tends towards $C_{GD}\, \alpha\, V_D^{-0.5}$ and C_{GOX} becomes irrelevant.

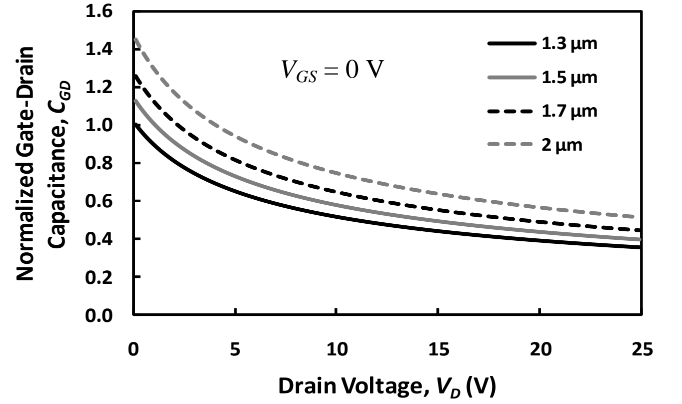

Fig. 2. Normalized C_{GD} *vs.* V_D for different trench depths predicted using the model in (5) with constant C_{GOX}.

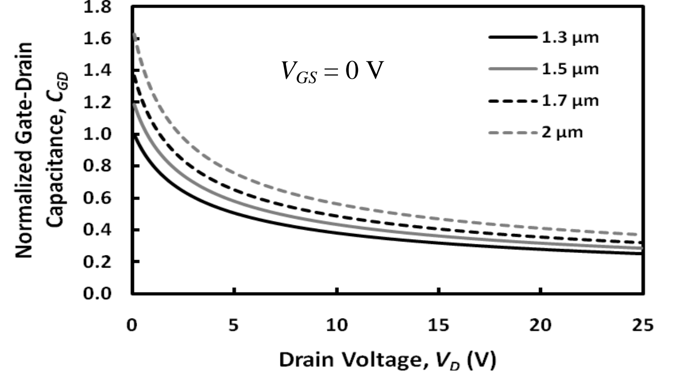

Fig. 3. Normalized C_{GD} *vs.* V_D for different trench depths predicted using the model in (5) with C_{GOX} determined by (3).

III. MEASUREMENTS AND DISCUSSION

Trench MOSFETs with TBOs have been manufactured with different trench depths so as to investigate the dependence of the C_{GD} on the trench depth and validate the C_{GD} model in (5). The fabrication process of the MOSFETs is detailed elsewhere [5]. The gate voltage vs. charge characteristic is measured and is shown in Fig. 4 where it can seen that there is a clear correlation with trench depth. The plateau in the characteristics of Fig. 4 indicates the period during the switching of the devices when C_{GD} is being charged/discharged, hence the length of the plateau is proportional to C_{GD}. The C_{GD} of the devices were measured on a parameter analyzer, the results of which as shown in Fig. 5 as a function of V_D. It can be seen in

Fig. 5 that C_{GD} increases with the trench depth and with a stronger degree at lower V_D. The characteristics exhibited in Fig. 5 resemble those in Fig. 3 more than Fig. 2 in the sense that the C_{GD} for the different trench depths converge at higher V_D.

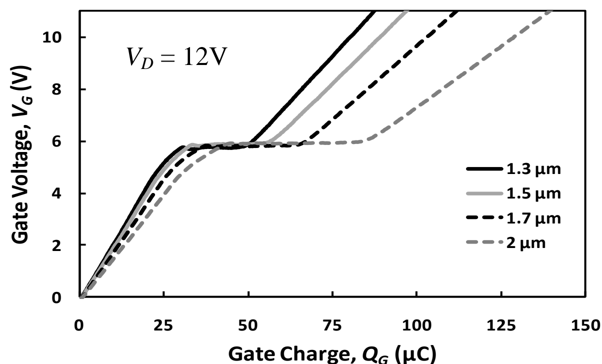

Fig. 4. The gate voltage as a function of gate charge for different trench depths showing gate charge increases with trench depth.

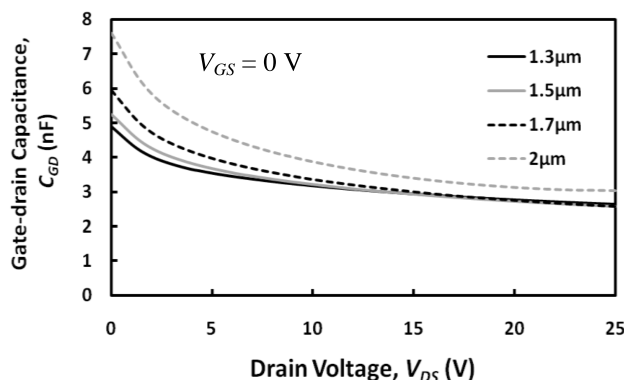

Fig. 5. The measured gate-drain capacitances as functions of trench depths for the trench MOSFETs.

Fig. 5 shows the importance of (3) since an increase in the trench depth (which is an increase in $t_D^{/}$ for the same p-body) results in a decrease in the average oxide thickness overlapping the drain for TBO MOSFETs. The model in (5) was only able to predict the behavior of the experimental measurements when the effect of the sidewall capacitance was taken into account. Hence, the C_{GD} characteristics in Fig. 5 converge for the different trench depths as is predicted by (3) and (5).

Both the analytical model in (5) and the experimental measurements in Fig. 5 show that C_{GD} increases with the trench depth (t_D) particularly at low V_D where the oxide capacitance dominates. Fig. 6 shows the percentage increase in C_{GD} as a function of trench depth for the measurements, the model with (3) and the model with constant C_{GOX} at $V_D = 1$ V. Fig. 6 shows that incorporating (3) into the model causes it to predict a higher rate of change in C_{GD} with respect to t_D. Some discrepancy between the models and measurements is expected since (5) is limited because it does not account for MOSFET edge termination effects. At the edge termination, a gate polysilicon extension (designed to connect the gate poly to the gate metal) overlaps the drain field plate (designed for terminating fringing fields at the device edge) with a thick layer of TEOS (typically over 500 nm) as a buffer. Equation (5) describes the operation in the active area and is useful as a first approximation with more detailed knowledge of the mask design at the edge termination required to improve the accuracy of the model.

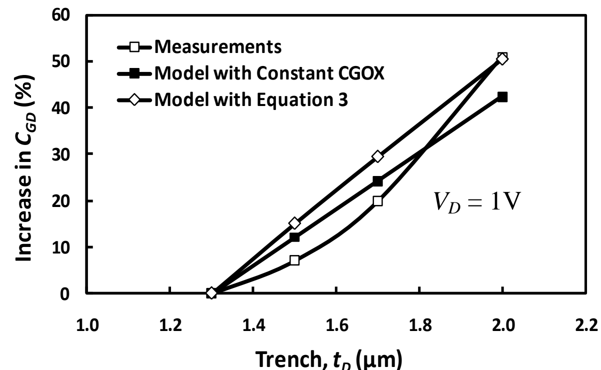

Fig. 6. Percentage increase in C_{GD} as a function of trench depth

IV. CONCLUSION

An analytical model has been developed for the C_{GD} of discrete power trench MOSFETs relating the C_{GD} to the trench depth, the trench bottom oxide thickness and drain voltage. Experimental measurements of C_{GD} on fabricated devices with different trench depths have been used to validate the model which shows that C_{GD} is proportional to the trench depth. The model also shows that the relationship between C_{GD} and the drain voltage is best predicted when the dependence of the gate oxide capacitance on the trench depth is taken into account. Because increasing the trench depth has the effect of decreasing the average oxide thickness overlapping the drain, the measured characteristics for the different trench depths showed a convergence of the characteristics at high drain voltages.

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