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Design of a Field-Portable Low Power Personal Data Logger - A Hardware Perspective

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ABSTRACT

There are a vast number of field–portable data loggers currently on the market. They differ greatly in terms of capability and complexity, in many cases being application or function specific. A survey was undertaken to identify market trends and future developments, system hardware specifications and the technologies employed. After comparing system specifications, it was apparent that there was a strong correlation between system performance and power consumption - high performance systems tend to be power hungry, and are typically larger and heavier than their lower performance counterparts.

The aim of this project was to design the core of an advanced, flexible, low-power portable data acquisition system, a 'personal' data logger (PDL), suitable for medical or athletic performance monitoring. The pocket-sized target system should be capable of high performance - sampling daily or up to 20,000 samples per second – with low power operation, and should be able to measure both analogue and digital signals. The data must be stored in a high-capacity non-volatile memory card, with USB and RS-232 ports provided for data upload and system configuration.

With the design specification defined, low power design techniques and the various battery and power supply options were investigated. A survey of system components was carried out and suitable low-power parts identified and selected for the design. After checking the project schematics, the circuit board was designed, manufactured and carefully assembled, ready for function and performance testing.

The test results indicated that the project met the design specification, demonstrating its potential for use in a small portable personal data logger. Further work would be

required to refine the power supply and power management systems, add an interface board housing a real-time clock, analogue signal conditioning, and input and output connectors, and to develop embedded system software.

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Chapter 1 - Systems Review

1.1 Overview

Portable or field instrumentation can encompasses everything from simple low-cost meters and data loggers, to expensive precision measurement, and high-performance data acquisition systems. The first 'portable' data loggers in the 1930s were quite large and heavy analogue systems such as chart recorders, which plotted data graphically on a roll of paper, tape recorders, or wire recorders that stored data on a spool of stainless steel wire.

The rise of digital systems and the development of the first microprocessors in the early 1970s, and solid-state memory saw the appearance and growth of digital logging systems. The increasing popularity of lower power CMOS circuitry and higher storage capacities over the following years saw the emergence of an increasing number of battery-powered systems.

Field instruments or portable data loggers are designed for use in mobile or remote applications, and are capable of reliable operation outdoors or outside of a controlled laboratory environment. In addition to application specific issues, systems should generally be:

- As small and lightweight as possible for portability
- Capable of operating from internal or external batteries, or a local power supply such as a car's auxiliary power supply
- Rugged enough to withstand both environmental conditions and user abuse

1.2 System Manufacturers

The systems featured in this study were chosen as they are representative of the many varied units available in the marketplace, and reflect a range application areas, interface options and technologies. The selection includes both simple and sophisticated systems and demonstrates both typical market trends and emerging developments.

Campbell Scientific

Campbell specialise in instruments for weather stations and environmental monitoring. They also provide a wide range of versatile systems for use in engineering research applications.

Comark

From developing the first digital thermometers in the 1960s, Comark specialise in temperature and humidity sensing and monitoring equipment.

Cranfield Impact Centre

The current generation of CIC's CardCorder rugged product family are of modular design and may be configured according to test requirements. Units have found use in motor racing, automotive testing, engineering research and aerospace.

Datataker

A provider of flexible data acquisition systems for environmental and industrial applications, Australia-based Datataker are part of the Grant Instruments group of companies.

Grant Instruments / Eltek

Grant supplies a range of scientific equipment for the laboratory and portable data acquisition systems for field use. The Grant group of companies include Datataker, and are active in bioscience, environmental monitoring and engineering research.

Eltek are associated with Grant, and provide customised versions of their Squirrel data logger.

Gemini Data Loggers

Gemini produce the Tinytag range of compact battery-powered data loggers and accessories for environmental, and shock and vibration monitoring.

IMC Dataworks

A provider of high specification data acquisition systems and data analysis software, IMC specialise in rugged modular and CAN-based instruments for automotive and engineering research.

Pace Scientific

Pace manufacture a range of compact and low power monitoring systems and sensors for a wide range of applications.

Racelogic

With a focus on CAN and differential GPS measurement, Racelogic offer a range of data acquisition and monitoring products. CAN expansion enables thermocouple, analogue and digital inputs to be added to a basic system for automotive and engineering testing.

SoMat (Ncode)

The modular Edaq family offer a wide range of input interface options for direct sensor connection, having a particular strength in strain measurement and fatigue. Designed to operate in challenging environments, application areas include aerospace and automotive testing, and engineering research.

Valitec

Valitec manufacture a series of low power, battery equipped, portable data loggers for field-based applications.

Zeta-Tec

A supplier of low cost, compact, battery operated data loggers, low power Zeta-Tec systems focus on temperature and humidity monitoring applications.

1.3 Overview of System Parameters

The majority of field-based data loggers, data acquisition systems and instruments have a similar architecture. This may differ in detail as some systems may use highly integrated chips that combine several functions, and others may have multiple input blocks to cater for high input channel counts, but the general layout is essentially that shown in *Figure 1*.

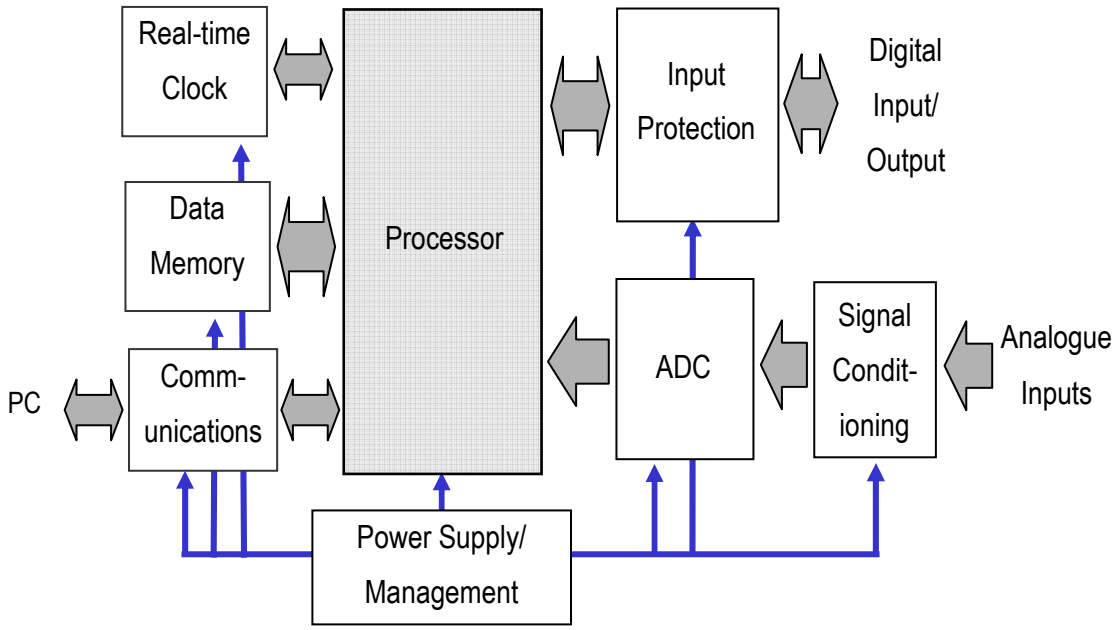

Figure 1: A Basic Data Logger System Architecture

When considering different systems, it is important that the various parameters are well defined; these are discussed next:

1.3.1 Analogue Inputs

These are able to measure a continuously varying analogue waveform, i.e. a voltage or current, from a signal source or transducer. The majority of transducers produce signals in an analogue form (at least at origin), and therefore sensors with analogue output signals tend to be more numerous (*Texas, 1996*) than the various digital options (which are described in section 1.3.4).

There are many different types of sensors with analogue outputs, e.g. for measuring temperature, strain, force, displacement, rotation, pH and gas concentration. These signals may have markedly different properties, which could be incompatible with a data logger's input requirements. To overcome this problem additional signal-conditioning circuitry may be necessary to optimise sensor outputs to suit system input

requirements. Some systems feature dedicated inputs to accept specific sensor types, such as thermocouples.

The various analogue input types are shown below:

1.3.1a Single Ended Input

This is the simplest and most common signal type, and consists of single input channel to accommodate a signal carried on a single wire (usually) referenced to signal ground. A number of single-ended (SE) inputs referenced to a common signal ground reduces the number of connector terminals required, which may be advantageous in smaller systems.

1.3.1b Differential Input

Here, two inputs are required, often referred to as *signal+* and *signal-* as one is the inverse of the other, to accommodate signals carried on a pair of wires, usually referenced to signal ground. As it is the difference between the two signals that is ultimately measured, any signal noise present on the pair of wires is removed by cancellation. Differential inputs exhibit superior signal to noise ratio to single-ended inputs, and have better performance for small signals and long cable runs.

1.3.1c Bridge Input

Bridge based transducers, such as strain gauges, have differential outputs, but require special signal conditioning. In essence, a strain gauge bridge features four resistive elements, one or more of which may be a strain gauge. The gauge itself consists of a length of resistive material of constant width and thickness on an insulated substrate. When strain is applied, there is a minute change in length (and therefore resistance), of the material which is proportional to the applied strain.

Strain gauges may be used in quarter, half, or full bridge configuration, therefore bridge completion resistors (mounted on-board or externally) may be required to provide a functioning Wheatstone bridge circuit.

As the changes in resistance can be very small, the resistance of the wires connecting the sensor to the signal conditioning may become significant. Some systems provide methods of compensating for these effects using sense inputs to determine the cable resistance.

As the sensor bridge is ratiometric, having the ability to increase a programmable excitation voltage will result in a larger output response. This can be desirable as it effectively reduces the signal to noise ratio, although the effect of self-heating ($P = V^2/R$) can cause problems under some circumstances unless compensated for.

1.3.1d Piezo Sensor Inputs

This is a special type of single-ended input for use with piezo-resistive and piezo-capacitive sensors. These sensors feature a small piezo transducer and normally require an external charge amplifier to condition the output signal to appropriate levels; some forms have integral amplification providing a low impedance AC-coupled output signal. PCB Piezotronic's ICP-type sensors utilise the signal output pin to provide a 2-20mA constant current input at 18-30V, which powers the sensor (*PCB Piezotronics, 2007*).

These sensors only provide a dynamic output as the piezo-element has no charge under static conditions. Common examples include force sensors, such as accelerometers.

1.3.1e 4-20mA Input

This is a widely used industrial standard for instrumentation and control systems with a wide range of available sensors. The signal is scaled from zero to 100% for the 4 to 20mA range.

1.3.1f Thermocouple Input

A thermocouple consists of a welded junction of two dissimilar metals. The thermoelectric voltage produced across the junction, which ranges from μV to mV, is proportional to temperature and differs according to the metals used. Temperature is measured relative that of the measurement circuit's Cold Junction Compensation (CJC) sensor, which should ideally be positioned next to the input connector as this can form another junction. The calibration for each type of thermocouple, i.e. E, J, K, N, T, is different, and non-linear, requiring the appropriate compensation and linearization to convert Volts to Celsius, or the preferred temperature scale.

1.3.1g Smart Sensor Input

By combining an analogue sensor with a small programmable memory circuit, sensor details and calibration may be stored. Known as TEDS (Transducer Electronic Data Sheets), these smart sensors require special inputs with digital capability, namely a serial bus. Designed as 'plug and play' devices, a suitably equipped data logger can configure system parameters autonomously from TEDS settings.

1.3.2 Analogue Input Range

It is vital that the measured signal range falls within the input range of a data logging system; this means that the signal may need to be attenuated if too large, or amplified if

the sensor output is of a low level. The most popular input range is 0–5Vdc, although ranges such as 0-10V and ±5V are not uncommon.

Systems with a programmable input range have the greatest flexibility as this can be adjusted to match a specific sensor. At higher voltage gains, the effect of voltage offset can become significant as the DC gain can take the signal outside the measurement range; in this instance, the addition of programmable offset adjustment is a desirable feature.

1.3.3 ADC Resolution

Resolution is normally described by the number of bits. Two raised to the power of this value gives the number of discrete steps that the ADC chip's input range may be divided by, hence:

12 bits gives a resolution of $V_{in}/2^{12} = V_{in}/4096$

16 bits gives a resolution of $V_{in}/2^{16} = V_{in}/65536$

For a 0-5V input range, this gives a minimum resolution of 1.2 mV and 76.3 µV respectively.

1.3.4 Digital Inputs

These are compatible with discrete voltages representing binary values or digital waveforms. Signals are often at TTL-level (0 – 5 Volts) but may be much higher. Digital inputs can take many forms; these are described below:

1.3.4a Pulse Counter Input

This is used to measure pulse frequency. The number of pulses are counted over a period, (typically one second), to produce pulse frequency. Some systems provide the alternative of accumulating the number of pulses to give a total figure.

1.3.4b Period Measurement Input

As an alternative to pulse counting, the period of a pulse may be measured to give instantaneous frequency measurement or timing information.

1.3.4c Event Input

This is used to monitor 'binary states', such as a switch or relay status, or signal logic. Event inputs are sometimes used to trigger recording.

1.3.4d CAN Bus Input

The Controller Area Network, or CAN bus, is a serial differential data bus standard for linking sensors and control and instrumentation systems. Originally developed by Bosch for automotive use, CAN and its derivatives have found acceptance in many other application areas.

With a data rate of up to 1Mb/second relatively high performance is possible across a few channels, although it is more commonly used to transfer data from a number of sensors (up to 128) sampled at lower rates. Data from many sensors or other systems, sampled at different rates, may be processed and recorded. As it is bidirectional the CAN bus can also be used to output data; and thus, it may be used for device networking.

1.3.4e Serial Data Input

RS-232 or RS422/485 serial ports may also be used to receive data from intelligent sensors or external devices. The serial output from a GPS receiver can provide geographical position and timing information for mobile applications once the data has been decoded.

1.3.5 Sample Rate

This dictates the number of discrete measurements that may be taken within a given period, usually one second. This is usually quoted in samples per second or Hertz (Hz). Some systems allow the user to set different sample rates for individual input channels whilst others use global settings.

Some manufacturers quote aggregate sample rates; this is the combined rate of all active input channels.

1.3.6 Triggering

Multiple triggering options are usually available to initialize recording. A manual trigger, such as a switch on an instrument's enclosure, is perhaps the simplest triggering method. Alternatively, an event or control input may be connected to a remote switch or external control circuit.

For long-term unattended operation, there are two main triggering methods. The first method utilises the system's real-time clock, which may be used to initiate recording at a predetermined and pre-programmed time and date. The second monitors sensor inputs, and starts recording upon preset conditions on one or more of these being met.

1.3.7 Data Storage

Data memory may take several forms: volatile SRAM or DRAM, non-volatile battery-backed SRAM, Flash ROM, or compact flash (CF), Secure Digital (SD), PCMCIA (PC) or Multimedia (MMC) flash memory card. Some manufacturers quote the physical storage capacity, e.g. 512 kb, whilst others specify the number of samples that may be stored. As data memory typically has a byte-width of 8-bits, a 12 or 16-bit data sample must be stored as two bytes; therefore specifying the maximum data samples capacity provides a more realistic storage figure, and makes it easier to calculate recording duration.

1.3.8 Communication

A communications link to a PC or PDA is used to upload settings, download logged data or interrogate a system in real-time. Most systems have one or more serial data ports. Currently RS-232 is the most common method of data transfer; although this is starting to become obsolete as most new notebook PCs do not have a compatible serial port. This does however permit connection to a GSM cellular or radio modem for remote access, which opens up the possibilities of sending reports and alarms via text message, or broadcasting data (at low sample rates) in real-time.

USB, Ethernet, Bluetooth and GSM cellular modems are becoming more popular; USB and Ethernet in particular offer high data transfer rates, facilitating the downloading of large data files. Ethernet also provides a portal for internet connectivity allowing systems to be connected to a central server, or, if data is stored in the correct format, interrogated using standard SQL (Structured Query Language) commands.

1.3.9 Outputs

Some systems provide analogue or digital outputs, which may be user programmable. These can be used as indicators or alarms, or for control applications when used in conjunction with other devices.

1.3.10 Sensor Excitation Voltage

Many systems provide sensor excitation outputs to power sensors. These may be fixed or variable, common rail or separate supplies for each sensor, and are normally current limited or fuse protected.

1.3.11 Power Source

Manufacturers use a variety of different power supply options. Some systems require an external power source, typically in the range of 6-24 Volts dc; others operate from removable batteries or integral rechargeable battery packs.

The power source is an important consideration for field-based instrumentation as it can determine how a system is used, and its size and weight. The number and type of batteries (primary cells or rechargeable), internal or external fitment, and whether they are fixed or removable, will largely depend on power demand, typical usage cycles, the application and environmental factors – this is discussed in detail in chapter 4.

1.4 A Comparison of System Features

The systems featured in the following comparison shown in *Tables 1a*, *1b*, *2a* and *2b*, are representative of those currently on the market. The contrasts between various system parameters illustrate the differences between the systems; these are discussed in section 1.4.

System	Maker	Inputs		Max	Resolution/ bits	Sampling Rate/ Hz
		Analogue	Digital			
CR1000	Campbell Scientific	8 Diff/ 16 Single-Ended (programmable)	2 x pulse/ 8 x event (programmable)	26	13	100
CR200	Campbell Scientific	5 Single-Ended analogue/ digital	2 pulse + 2 control	9	12	1
CR5000	Campbell Scientific	20 Diff/ 40 Single-Ended (programmable)	2 x pulse/ 8 x event (programmable)	50	16	100
CR800	Campbell Scientific	3 Diff/ 6 Single-Ended (programmable)	2 x pulse/ 4 x I/O (programmable)	12	13	100
CR9000X	Campbell Scientific	14 Diff/ 28 Single-Ended (programmable)	2 x pulse/ 8 x event (programmable)	38	16	100,000
Diligence EVG	Comark	8 thermocouples	none	8	8	0.1
CardCorder	Cranfield	16-48 Diff/ 48 SE/ICP/ 96 Single-Ended (programmable)	8 x pulse/ 8 x period/ 32 event/ serial/ CAN (programmable)	101	12	100,000
CardCorder Pro	Cranfield	32 Diff/ 64 Single-Ended /ICP (programmable)	8 x pulse/ 8 x period/ 32 event/ serial (programmable)	113	12	300,000
DT50	Datataker	5 Diff/ 10 Single-Ended (programmable)	3 pulse + 5 x I/O	18	15	25
DT500	Datataker	10 bridge/ 30 Single-Ended (programmable)	3 pulse + 4 x I/O	37	15	70
DT800	Datataker	12 bridge/ 24 Diff/ 42 Single-Ended (programmable)	16 x I/O + 1 x serial (programmable)	59	16	100,000

Table 1a: System Input Properties and Maximum Sampling Rates – part 1

System	Maker	Inputs		Max	Resolution (bits)	Sampling Rate/ Hz
		Analogue	Digital			
Squirrel 851	Eltek Ltd	8 Single-Ended (programmable)	1 x pulse/ 8 x event	17	12	1
Squirrel 2040	Eltek Ltd	16 bridge/ 32 Single-Ended (programmable)/ 2 high voltage	4 x pulse/ 8 x event	44	24	100
Tinytag IS-0020	Gemini	Thermistor probe	none	1	10	1
DAX-2408	IMC Dataworks	8 Differential / TEDS (programmable)	4 pulse/ 16 event/ 2 CAN	30	16	400,000
XR440	Pace Scientific	4 (programmable)	1 x pulse	5	12	200
VBOX III	Racelogic	4 (programmable)	2 x pulse/ 2 CAN (programmable)	8	24	100
E-DAQ Lite	SoMat	32 bridge/ Differential/ (programmable)	96 (programmable)/ GPS	96	16	100,000
E-DAQ Plus	SoMat	128 Single-Ended / 64 bridge/ Differential / thermocouple (programmable)	256 pulse/ event/ I/O + GPS/ CAN	192	16	400,000
AD128	Valitec	8	16	24	8	500
AD2012	Valitec	12	4	16	12	500
uLogger-4V	Zeta-Tec	4 x 0-2V	none	4	12	1

Table 1b: System Input Properties and Maximum Sampling Rates – part 2

System	Maker	Comm Ports	Data Storage	Min Size (mm)/ Weight	- - - - Power - - - -		Misc
					Source	Current	
CR1000	Campbell	RS232	2Mb + Compact Flash	216 x 99 x 22/ 1 kg	External 9.6 - 16 Vdc	4 - 28 mA	
CR200	Campbell	RS232	128kb	140 x 76 x 51/ -	External 7 - 16 Vdc	4 mA+	Telemetry
CR5000	Campbell	RS232	900 k samples + PC card	247 x 210 x 114/ 5.5 kg	7 Ah Battery/ External 11 - 16 Vdc	-	LCD
CR800	Campbell	RS232	2 Mb	241 x 104 x 51/ 0.7 kg	External 7 - 16 Vdc	4 mA+	PAKbus
CR9000X	Campbell	RS232/ Ethernet	128Mb + PC card	457 x 343 x 229/ 19.1 kg	14 Ah Battery / External 9.6-18 Vdc	525 mA +	Modular
Diligence EVG	Comark	RS232	64 k samples	190 x 138 x 45/ -	4 x AA Batteries / External DC	-	LCD
CardCorder	Cranfield	RS232	1 Gb Compact Flash card	105 x 95 x 74/ 1-2 kg	External 9 - 36 Vdc	0.4 - 1.5 A	Modular
CardCorder Pro	Cranfield	RS232	4 Gb PC card	189 x 149 x 88/ 2-4 kg	External 9 - 36 Vdc	0.7 - 2.5 A	Modular
DT50	Datataker	RS232	166 k samples	260 x 110 x 55/ 1.5 kg	External 9 - 18 Vdc	80 mA	+ PC card
DT500	Datataker	RS232	166 k samples	260 x 110 x 85/ 2.2 kg	External 9-18 Vdc/ 1.2 Ah Battery	80 mA	+ PC card
DT800	Datataker	RS232/ Ethernet	130 k samples	260 x 110 x 90/ 3.1 kg	External 11-28 Vdc/ 2.2Ah Battery	420 mA	+ PC card

Table 2a: Data Storage, Power and General System Properties – part 1

System	Maker	Comm Ports	Data Storage	Min Size (mm)/ Weight	Power		Misc
					Source	Current	
Squirrel 851	Eltek Ltd	RS232	250 k samples	180 x 120 x 85/ -	6 AA cells/ External 9-14 Vdc	155 mA	LCD
Squirrel 2040	Eltek Ltd	RS232/USB	1.8 M samples	235 x 175 x 92/ 1.5 kg	6 x AA cells/ External 9-18 Vdc	80 mA	LCD
Tinytag IS-0020	Gemini	RS232	16 k samples	80 x 59 x 34/ 100 g	3.6V 1/2 AA Li Battery		
DAX-2408	IMC Dataworks	RS232/ Ethernet	PC card	195 x 120 x 110/ 1.8 kg	External 9 - 36 Vdc/ 'UPS' Battery	830 mA	Modular
XR440	Pace	RS232	32 k samples	120 x 61 x 24/ 156 g	9V Li PP3 Battery		
VBOX III	Racelogic	RS232	Compact Flash	170 x 121 x 41/ 900 g	External 5.3 - 30 Vdc	900 mA	GPS
E-DAQ Lite	SoMat	Ethernet/ RS232	64Mb/ 256 Mb Compact Flash	180 x 140 x 45/ 1-2 kg	External 10-18 Vdc/ 0.6Ah UPS Battery	0.9 - 4.2 A	Modular
E-DAQ Plus	SoMat	Ethernet/ RS232	64Mb/ 256 Mb Compact Flash	274 x 231 x 154/ 3.4 kg	External 10-60 Vdc/ 0.6Ah UPS Battery	0.9 - 4.2 A	Modular
AD128	Valitec	RS232	130 k samples	147 x 91 x 33/ 225 g	External 7 - 12 Vdc/ PP3 Battery	4-10 mA	
AD2012	Valitec	RS232	540 k samples	147 x 91 x 33/ 225 g	External 7 - 15 Vdc/ PP3 Battery	20-32 mA	
uLogger-4V	Zeta-Tec	RS232	32 k samples	50 x 24 x 90/ -	AA cell		

Table 2b: Data Storage, Power and General System Properties – part 2

1.4.1 ADC Resolution

Figure 2 depicts the ADC resolution of the systems in this survey. Those systems with 24-bit resolution employ delta sigma ADCs. These chips can provide a very high effective resolution at low sampling frequencies due to high oversampling ratios, noise shaping, averaging and digital filtering; however, this also limits the maximum sampling rate. As sampling rates rise, the oversampling ratio is reduced and the noise reduction techniques less efficient, resulting in a much lower effective resolution.

The remaining systems use the more common Successive Approximation ADCs with a resolution of 12 to 16 bits. Here the basic resolution is unaffected by the sample rate, which may be as high as hundreds of thousand samples per second.

1.4.2 Data Storage

To compare system's data memory, the storage capacities have been converted to data samples where appropriate. For comparative purposes, it is assumed that a data sample takes up two bytes of memory unless stated otherwise in the manufacturer's literature.

The differences are shown in *Figure 3*. There are several orders of magnitude between the top and bottom ranked systems. The data storage capacity shows correlation to the sampling rate (*Figure 5*), and the number of signal inputs (*Figure 4*), but also to the application. The Tinytag, a digital thermometer with a 16,000-sample capacity, does not need much memory; if used to log the temperature every hour it would take 666 days to fill the memory. The DAX-2408, E-DAQ or CardCorder Pro sampling eight inputs at 10 kHz per channel, would require 80,000 samples per second of recording time. More signals, sampled quickly, require more storage.

As memory is now relatively cheap, especially in the form of flash memory cards, and accounts for a relatively small percentage of component costs, large storage capacities are not necessarily restricted to premium products.

Many systems provide the option of additional flash memory cards storage; however, only the primary storage capacity is considered here. Systems with secondary storage options are shown in highlights.

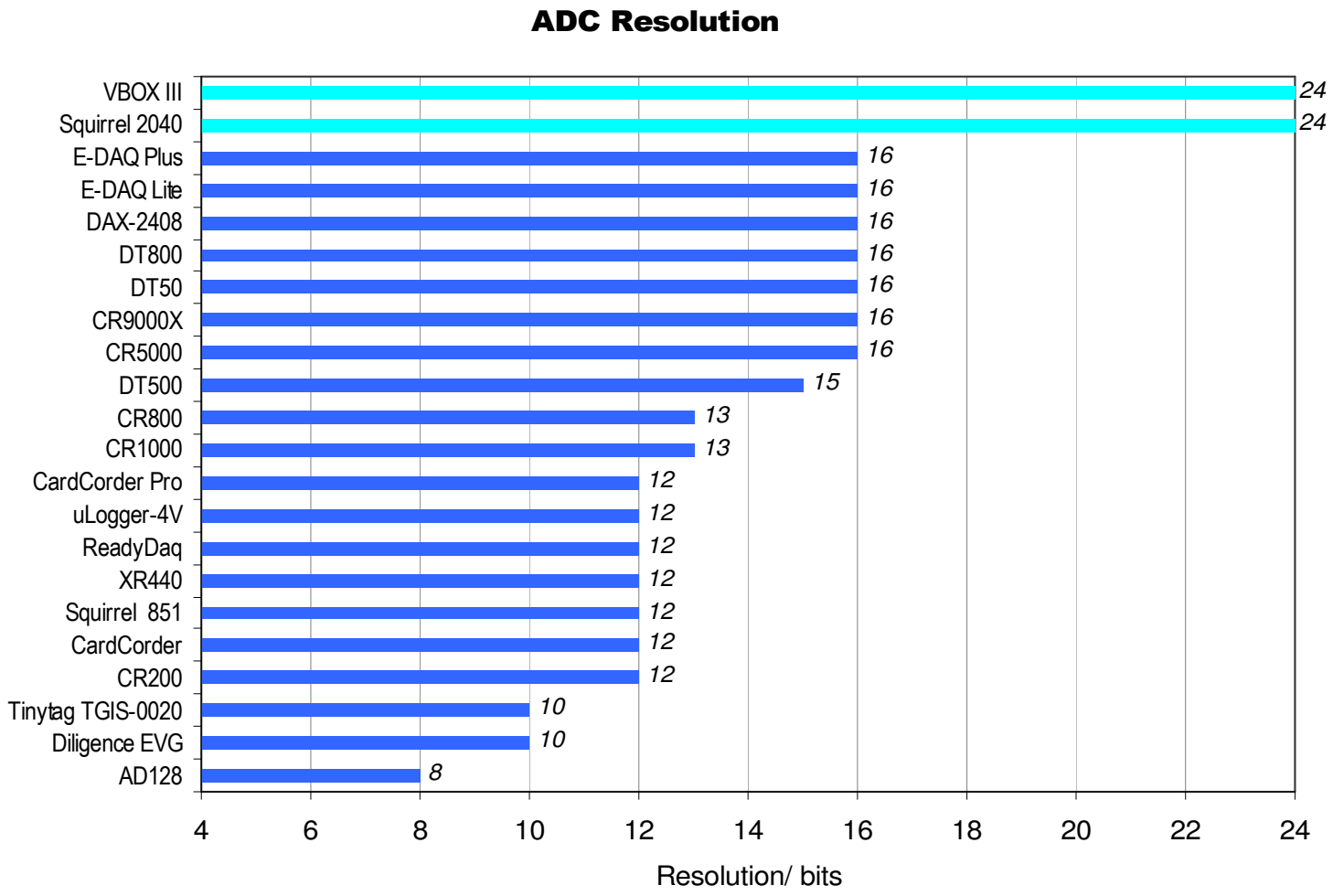

Figure 2: ADC Resolution

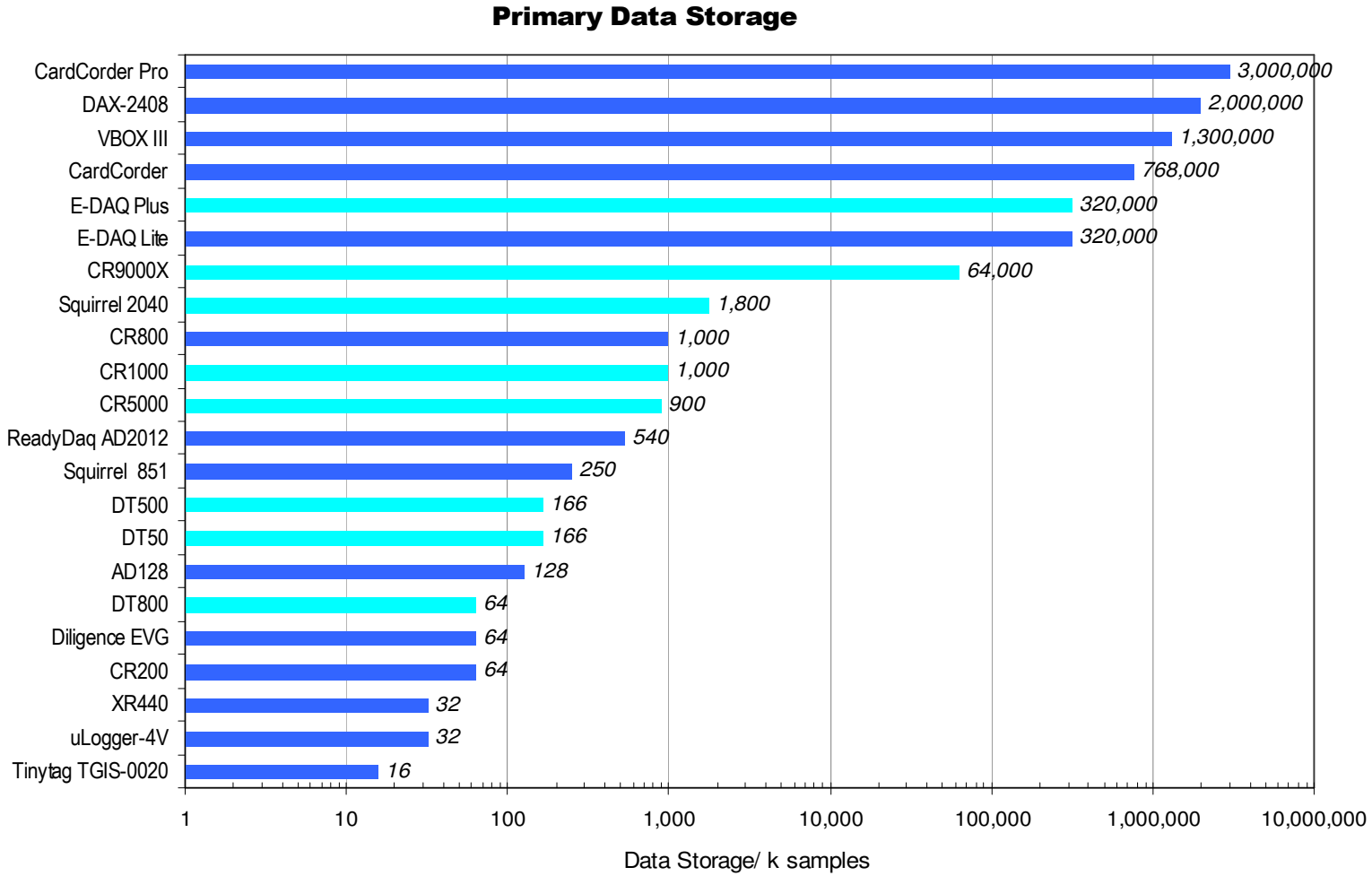

Figure 3: Primary Data Storage Capacities

1.4.3 Input Channels

All the input types previously discussed may be found amongst the featured systems. Analogue inputs dominate, although most units also accommodate a range of digital inputs.

Regarding the analogue channels, single-ended inputs are the most prevalent with some systems being configurable for single-ended, differential, or range of other input types. For field-based systems, integral signal conditioning is an important feature; external boxes add to the overall size and weight, and may prove cumbersome. A number of systems include this feature; some offer dedicated inputs while others have various levels of programmability. For instance, systems designed with engineering applications in mind may feature inputs specifically for use with strain gauge based sensors.

The most common forms of digital input are the pulse and event inputs. Some systems provide programmable digital channels that may be used as pulse inputs or for input or output tasks. The CAN bus appears to be a growth area, having expanded beyond the confines of the automotive world into other sectors (*Marsh, 2002*). Many suitably equipped units are currently available. Some manufacturers use CAN to add remote modules, providing additional analogue and digital sensor inputs.

To illustrate the difference between systems, the total input channel count is shown in *Figure 4*. The top five units are of modular construction and may be configured with the number and type of interface modules to suit individual monitoring applications.

The maximum number of inputs quoted is the maximum that may be directly connected, ignoring additional inputs from network expansion devices. In the case of modular systems, it assumes that the maximum number of modules are fitted.

1.4.4 Sample Rates

It is perhaps the range of aggregate sample rates, as shown in *Figure 5*, that best exemplify the differences between the various systems. In fact, when divided into three bands, these closely match the systems' typical application areas: environmental applications tend to require sample rates from daily to a maximum of 50 Hz per channel, whereas engineering research may require rates from 1 Hz to 50 kHz. General purpose applications (0.1 to 200 Hz per channel) span the middle ground.

The higher speed systems can sometimes only maintain these rates for a few seconds at a time; nevertheless, with the right triggering, they would prove to be very useful for anomaly or 'glitch' detection.

1.4.5 Power Consumption

The respective systems' typical current consumption, less sensors, is displayed in *Figure 6*. It can be quite difficult to extract typical power figures from manufacturers' data sheets; the information some provide could best be described as sparse. This is perhaps understandable as there are a number of variables that affect power consumption:

It is the operating current of a unit running in a typical configuration that is of most interest. Thus, if powered by batteries, the likely continuous operating duration can easily be calculated. In the case of long-term monitoring, sampling perhaps hourly, a

system can enter a low power standby mode between sample intervals to prolong battery life; consequently, battery duration is dependent upon the sampling interval. Manufacturers commonly quote typical battery life, without specifying the duty cycle, rather than operating current.

It may prove difficult to assess the power demand of a modular system, as this is dependent of the number and type of modules fitted. The figures quoted are most often for a specific basic configuration. Even where the demand of individual modules is specified, the total power consumption may differ from the sum of the parts

A consideration often overlooked is sensor power budget. Most systems provide regulated, low-noise supplies to power sensors. The current demand of potentiometric devices, such as displacement transducers, or semiconductor temperature sensors is typically no more than a few milliamps (*Active Sensors, 2006*). In the case of standard 120Ω or 350Ω strain gauges, power demand can quickly escalate: in the case of sixteen 350Ω gauge inputs supplied with 5V excitation, the current demand would be 229 mA.

There is an immediate correlation between current consumption and sampling rate. The units with the highest sampling rates, shown highlighted, head the ordered table; the VBOX III's ranking is due in part to its onboard differential GPS receiver.

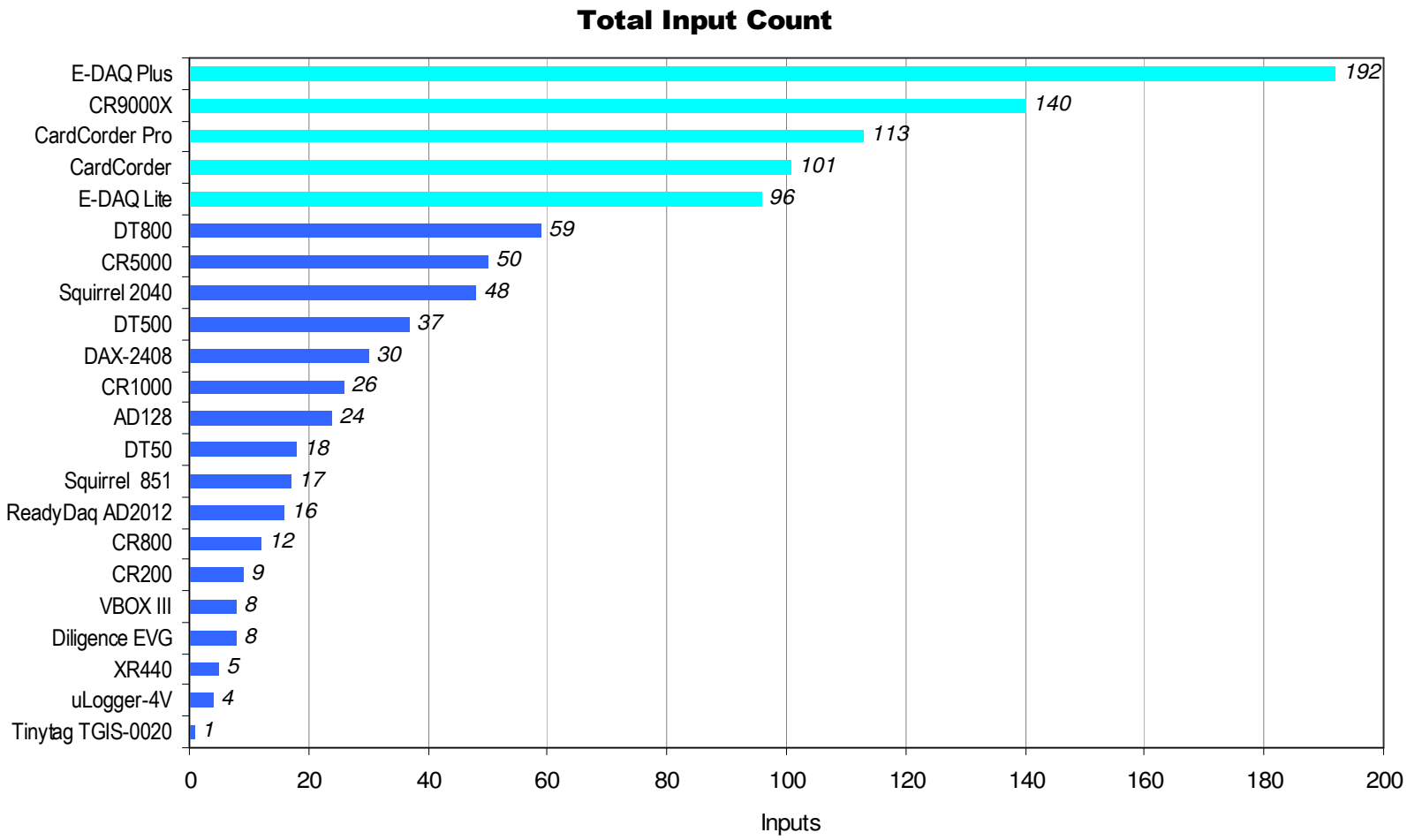

Figure 4: Total Input Channel Count

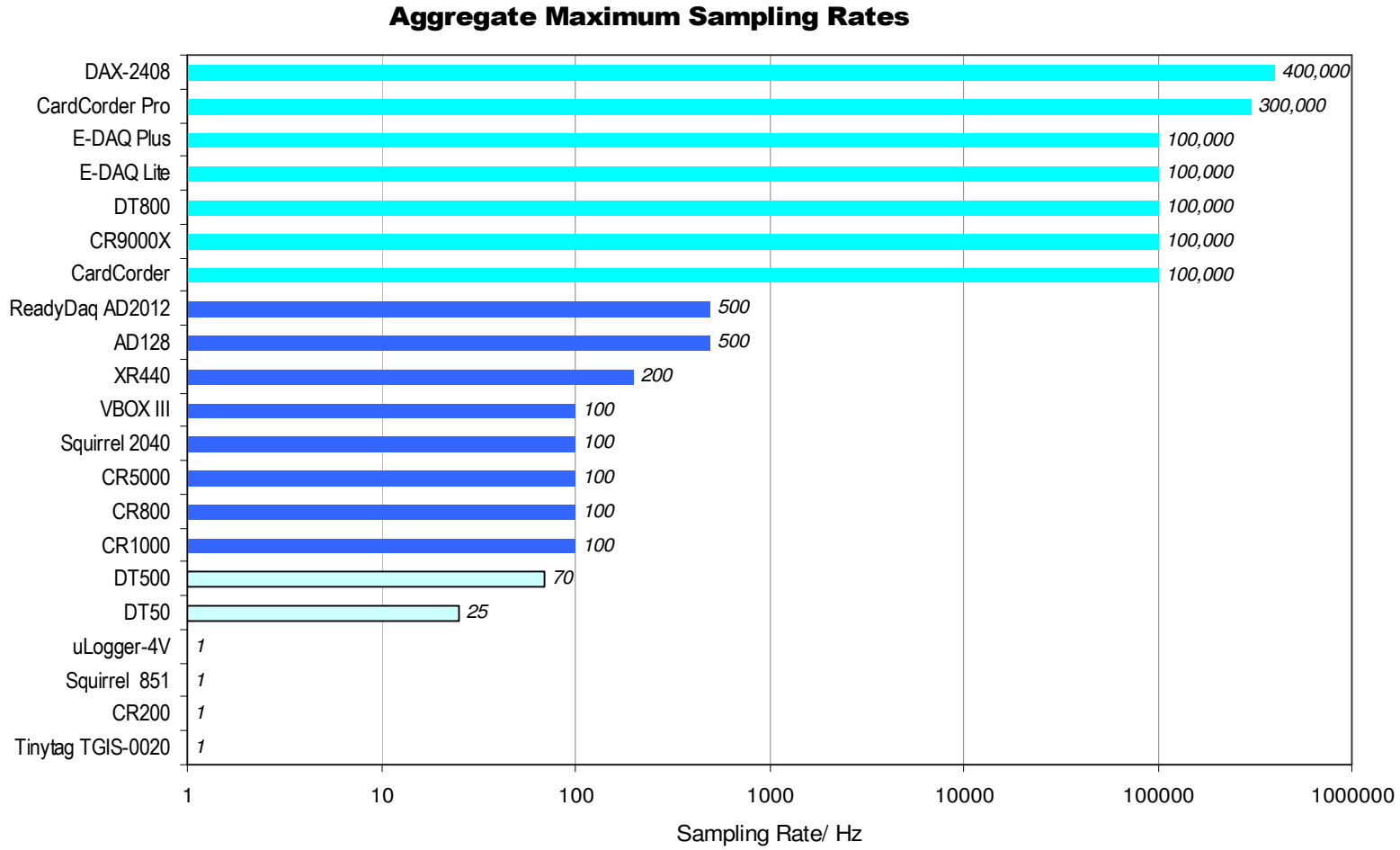

Figure 5: Aggregate Maximum Sampling Rates

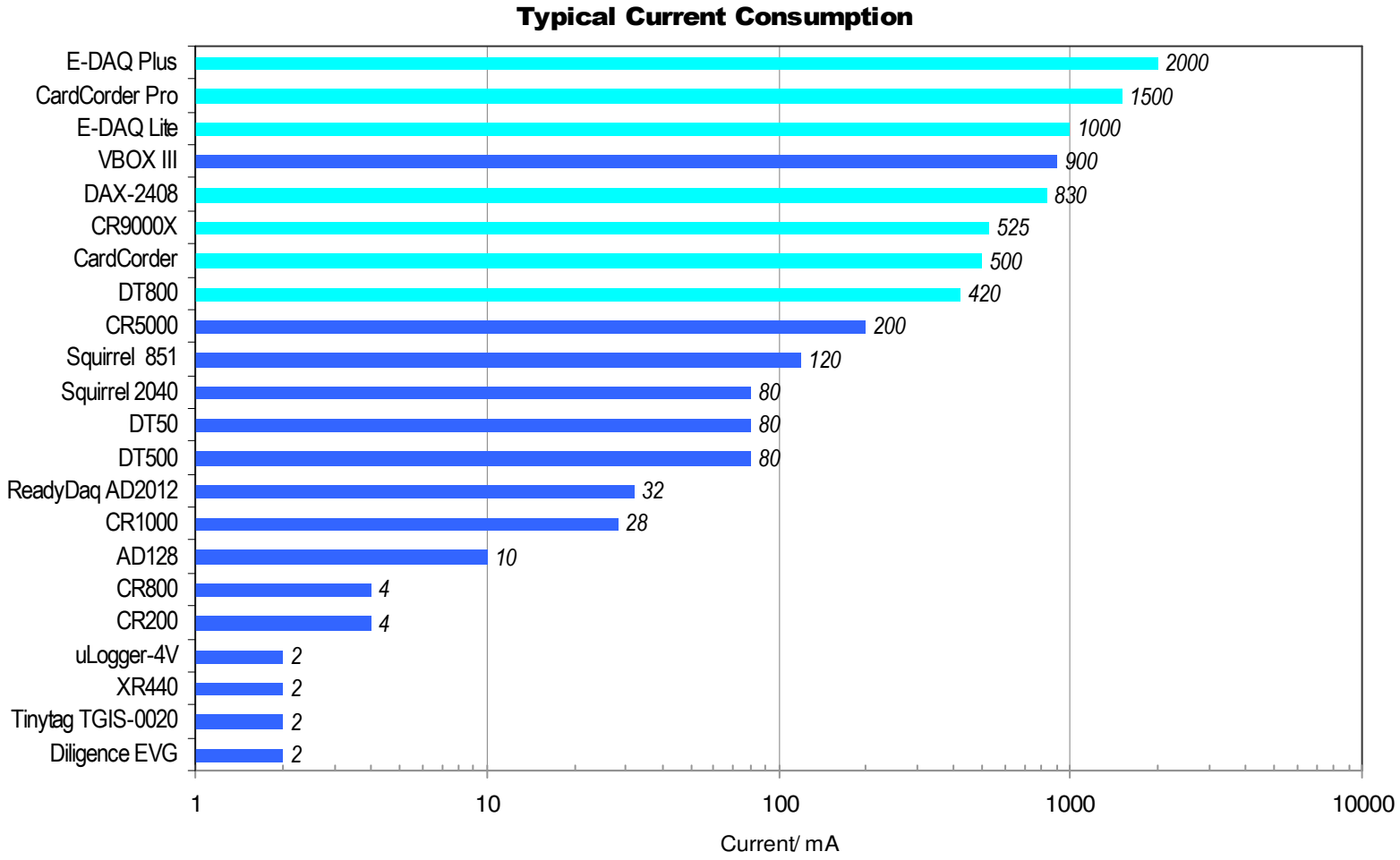

Figure 6: Typical System Current Consumption

1.5 Aim and Objectives

After investigating the features of a broad spectrum of currently available field instrumentation systems, one thing that stands out is the relationship between power demand and sampling rate. This is best illustrated by the graph shown in *Figure 7*; units with higher sampling rates tend to consume more power. In practice, this often leads to a requirement for larger batteries, increasing system size and weight, or external power sources. This has serious repercussions for system portability and places serious restrictions on usage.

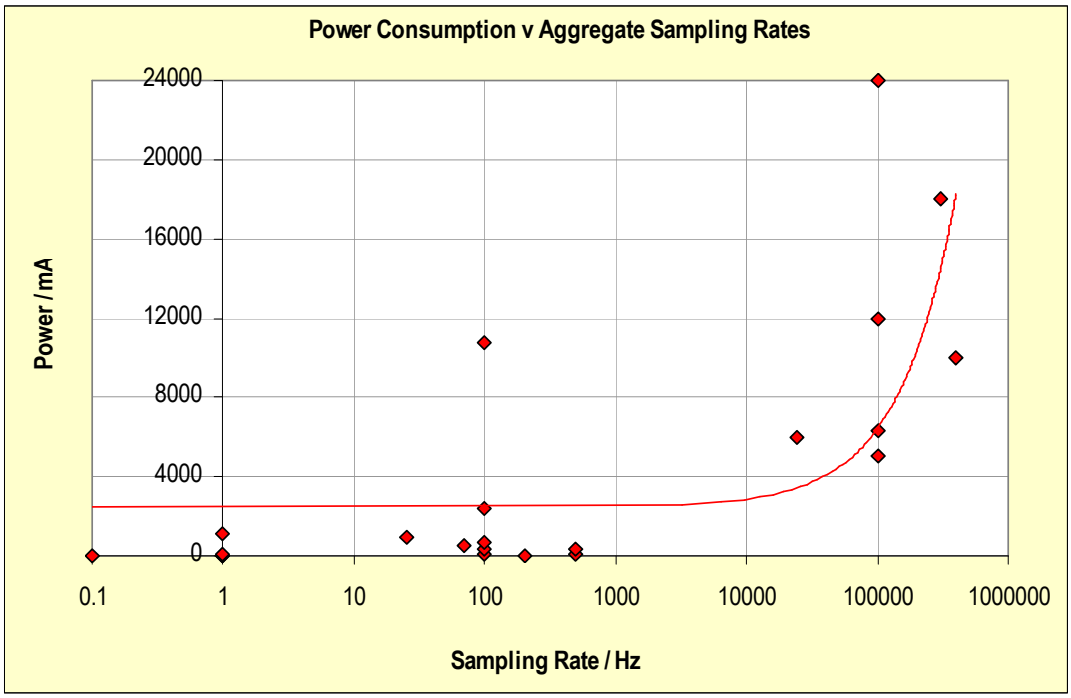

Figure 7: A Comparison of System Power Consumption v. Sampling Rate

The aim of this project is to design the core of an advanced small, flexible, low-power data acquisition system. The application focus is a 'personal' data logger (PDL), a pocket-sized portable system that may be used to measure a range of parameters for medical or athletic performance monitoring. Parameters of interest could include

temperature, humidity, heart monitoring (ECG), breath flow, acceleration and stress/strain, for monitoring both human performance and that of prosthetics or sports equipment. These could be measured with out the encumbrance of umbilical cables.

The circuit board must be compact, rugged, and lightweight, with sophisticated power management features, and capable of autonomous operation. As the system is to ultimately operate from a small battery pack, current consumption should be minimised to preserve battery life. For maximum flexibility, it is desirable that the system should be capable of aggregate sample rates from below 1Hz, up to around 20 kHz across multiple input channels.

Project objectives are split into five main areas:

- To define the system product design specification
- To investigate suitable low power design techniques
- To determine the optimum power supply system
- To produce a detailed circuit design
- To quantify the design's performance

The design would also provide an ideal hardware platform for use in a diverse range of field applications, including both long-term monitoring and transient capture. This however, is outside the scope of this project.

Chapter 2 - Defining the Design Specification

2.1 Introduction

The project brief is to produce a flexible design for a personal data logger (PDL). It should be able to sample data at high or low recording rates whilst minimising power consumption. There are many factors which must be considered in designing a viable system, some of which have an influence on power demand. These factors are discussed below:

2.2 System Parameters

2.2.1 Analogue Inputs

From the system survey, it is apparent that although many units may cater for both differential and single-ended inputs, it is the latter that are the most numerous (*see tables 1a and 1b*) of the general purpose analogue input forms. By using a common signal ground, single-ended inputs offer a high connector pin density and require minimal interface circuitry.

Ideally, at least eight inputs should be provided, each with some form of protection from voltage transients and high frequency signal noise. A nominal input range of zero to 5 Volts dc will accommodate most common sensors, although programmable gain would offer greater flexibility.

2.2.2 ADC Resolution

After surveying currently available systems, it is clear that resolutions of 12 and 16-bits dominate; with more recent devices showing a tendency towards 16 bits.

It should be noted that more bits do not necessarily mean greater precision; this has as much to do with the sensor. If a sensor is only able to measure to a precision of 0.1% for example, this is a good match for a 10-bit ADC (100% x $1/2^{10}$ = 0.098%). Thus, a 12-bit device able to measure to 0.02% of full scale (100% x $1/2^{12}$), or 16- bits, down to 0.0015%, do not offer any real benefit. In addition, higher resolution devices, capable of measuring down to microvolt levels, make extremely effective noise measurement systems unless due care is taken with noise reduction techniques. It could be argued, perhaps, that the drive for higher resolution sometimes has more to do with product marketing than operational requirements.

2.2.2a Noise Issues

As small portable instruments do not have the benefit of racks of signal processing boards, or a closely controlled laboratory environment, it can be much more difficult to achieve low noise figures. Noise sources such as transmitted electromagnetic interference (EMI) from radio signals or 50Hz mains noise, and the environmental effects of temperature, humidity and vibration upon sensors can all lead to signal degradation.

Most of the higher performance systems use onboard digital signal processing (DSP) techniques (e.g. Somat's EDAQ series) or sophisticated filtering techniques to achieve low noise figures. Filters in particular require very careful design and application. If the wrong type or class of filter is used, or the cut-off frequency is incorrectly applied, it may be ineffective, or perhaps worse, attenuate the signal of interest.

Without careful attention to signal and system screening, careful circuit layout and passive noise reduction, it is possible that a 16-bit field-based system will measure as

many as six bits of noise. With the PDL's constraints on size and power demand, DSP is out of the question. The selective use of low power programmable filter chips, such as Maxim's MAX7409/7410 (*Maxim, 1998*), could be of benefit for particularly noisy signals.

2.2.2b ADC Selection

In choosing to base the design around a 16-bit ADC, it is possible to provide both high resolution, where appropriate, and additional flexibility. By using a software bit-masking technique to create a 'data window', as depicted in *Figure 8*, it is possible to reduce the full 16-bit sample to 12 or 14 bits. This may be performed dynamically at slower sample rates or on a PC prior to data analysis. If the data memory is of a limited size, this dynamic scaling can effectively increase the number of samples that may be stored. With the PDL, storage capacity is not an issue, but this method still provides benefits as shown.

If 12-bits are to be recorded, moving the window left or right provides effective signal gain or attenuation. If the incoming signal is large, the window may be shifted fully left masking the bottom four bits. Assuming an input range of 0 to 5 Volts, this reduces the resolution to 1.2mV per bit, and potentially removes a milliVolt of signal noise.

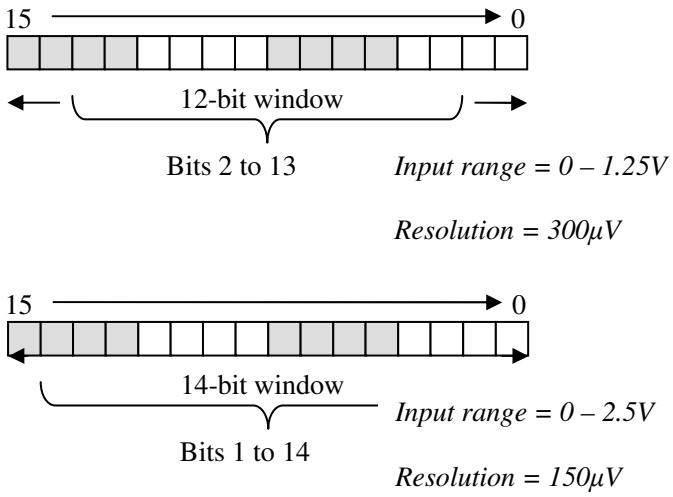

Figure 8: ADC bit-masking to create a data window

Moving the window fully to the right and masking the top four bits gives an equivalent input range of 0 to 0.3125 V. Whilst reducing the dynamic range, this scaling method provides an effective voltage gain of 16. This is useful for small signal levels, although with a resolution of 76µV per bit, any signal noise could be significant.

This technique was successfully employed in early versions of the Cranfield-developed CardCorder data acquisition systems in 1990. By effectively providing the design with a virtual multi-channel programmable gain amplifier (PGA), this gives the PDL considerable flexibility, with no power budget penalties or an increased chip count.

2.2.3 Sample Rate

From the analysis of current systems, it is clear that the sampling rate often defines the application area. As previously stated, this design project aims to provide a flexible platform with a wide range of sampling rates. The benefits of sampling at higher frequencies must also be considered; more data points over the sampling period can

provide more signal information for data analysis. When considering the sampling rate, the following points should be taken into account:

2.2.3a The Nyquist Rate

According to The Sampling Theorem (*National Semiconductor, 1980*), signals should always be sampled at frequencies at or above the Nyquist Rate (*Nyquist, 1928*), i.e. at least twice a bandwidth-limited signal's maximum frequency, in order to be able to reconstruct the original waveform. Thus, the Nyquist frequency of a 10 Hz signal is 20 Hz. Sampling at a higher rate will naturally give more data points and therefore clearer signal reproduction.

2.2.3b Oversampling

Sampling above the Nyquist frequency is known as oversampling. The greater the oversampling ratio, the better its' reproduction as more data points are produced for a given period. In addition, by oversampling a waveform, the extra data samples can be digitally manipulated to help reduce noise and improve resolution. Although digital signal processing is it is beyond the scope of this project, it is however worth mentioning one commonly applied technique.

Sampled data can sometimes have several bits of signal noise; this can be reduced, and ADC resolution improved, by a combination of oversampling and averaging. First, the waveform must be oversampled at four times the Nyquist frequency for every additional bit of resolution *(Atmel, 2005)*, i.e.:

$$f_{oversampling} = 4^n \times f_{nyquist}$$

where n is the number of bits

A moving average applied to these extra samples, i.e. sequentially taking the sum of a block of 4^n samples and dividing by 4^n. This results in the attenuation of signal noise and the flattening of any sharp peaks. If the system processor has sufficient performance, this process may be performed dynamically, 'online'. For data acquisition systems however, it is arguably better to perform signal processing tasks offline during post-processing unless there adequate memory for the 'raw' data to be retained.

2.2.3c Summary

Having a wide sampling range greatly enhances the PDL's flexibility. Hence the design should be capable of achieving an aggregate sample rate from once daily to around 20 kHz, with a maximum of around 10 kHz on an individual channel. In considering Nyquist, a 10 kHz anti-aliasing filter is required to band-limit each input.

2.2.4 Digital Inputs

It is desirable to provide at least one TTL-level 16-bit pulse counter (giving a count of up to 65535 before resetting), and one or more event inputs; these functions may be combined to save input connector pins. In addition, there should be a dedicated trigger input to initialize remote recording.

Each input would need to be provided with some form of protection from voltage transients and high frequency signal noise. Galvanic isolation, using opto-isolator circuits, would provide the necessary protection. However, the turn-on current may be several milliamps per input, and then there is of course the detector current to consider. Simple resistor-capacitor circuits, clamping diodes and Schmitt-input logic may offer a reasonable lower power solution.

2.2.5 Triggering

The design should have a trigger input capable of waking the system from shutdown, and initialise data logging. The trigger source could be from an off-board manual switch or an active signal from a programmable device.

2.2.6 Data Storage

From the study in the previous section, it can be seen that a range of storage sizes and technologies are in common usage. For maximum flexibility, the PDL should include mass storage capability. This offers the benefit of high sampling rates, a long recording duration, or a combination of the two. If sufficient processor performance is available for on-board data processing, a large data memory also allows both raw and processed data to be retained.

For autonomous operation, and the use of power management techniques to maximize battery life, the data memory must be non-volatile. Available technologies include battery-backed SRAM, Ferroelectric RAM (FRAM), flash ROM and flash memory cards. Of these, Flash memory and SRAM are the most popular.

SRAM offers fast access times, but has relatively low memory density and is volatile, requiring that power, often from a backup battery, is supplied to the chip's voltage terminals to prevent data being lost.

Flash has slower access times, but offers very high memory density and is non-volatile. Hence, Flash is the preferred option.

2.2.6a Flash Memory Cards

In choosing to use Flash memory, either an array of chips, together with the associated address decoding logic, or memory cards may be used. Memory cards offer the advantages of integral memory controller chips, very high memory density and compact packaging, in addition they are readily available in a range of form factors and storage capacities, at low cost.

System storage capacity is often a major factor in determining pricing in a product range, the top of the range models having the largest memories. If this design project was a commercial system, the cost difference between 128MB and 2GB Flash cards would likely be less than £10 to the manufacturer, but could command a premium several times higher in the marketplace.

2.2.7 Communication

The design should have an RS-232 port for serial communication with suitably equipped PCs, modems and a range of other devices. As autonomous operation (whether long-term or otherwise) is a key feature for the PDL, serial connection to a GSM cell phone or a low-power radio modem could provide remote wireless access.

The serial port may also be used as a digital input. If connected to a GPS (Global Positioning System) receiver for example, longitude and latitude position may be logged, or a number of systems synchronised to the GPS clock signal. The port's Baud rate should be software programmable, and capable of operating at all common data rates up to a maximum of 115 kBaud.

With a large data memory, a USB (Universal Serial Bus) port will greatly improve data upload performance compared to the RS232 port. Performance should be roughly

comparable to that typically experienced with MP3 players and digital cameras. As USB offers high data rates, it may also be possible to stream data direct to a host PC in real time, albeit at reduced sample rates. USB could also provide system power to preserve battery life during data uploads.

2.2.8 Power Management

To save power, power management techniques should be employed. The PDL core should have the facilities to control a number of off-board power supplies serving both the system itself, and providing excitation for sensors.

2.2.9 Power Sources

The PDL should be capable of running either on internal removable batteries, or from an external power source, such as that available from a host PC's USB port. The various power supply options are discussed in detail in *Chapter 4*.

2.2.10 Other Considerations

Like all field-portable systems, the PDL should be of rugged construction. Components should be capable of withstanding the effects of vibration and mechanical shock. Compact size is a desirable feature; therefore, circuit boards should have as small a footprint as practical component spacing constraints permit. The battery pack and input/output connectors ultimately determine overall system dimensions, but the ubiquitous Sony Walkman would be close to the ideal system size.

2.3 Summary

Based on the preceding discussion, the design specification for the Personal Data Logger core is summarized below:

- Eight single-ended analogue inputs, with a nominal 0 – 5 Volt input range.
- 16-bit ADC resolution.
- Sample rate ranging from daily to around 20 kHz aggregate.
- One 16-bit pulse counting input.
- One event input.
- External input for system wakeup and/or triggering.
- Large Flash Card (i.e. at least 512MB) for mass data storage.
- Serial RS-232 and USB communication ports.
- Control of off-board voltage regulators or power supplies for system and sensor supplies.
- Maximum transient system operating current of around 300mA.
- Capable of operation from two to six batteries, or an external supply.
- Rugged, compact board design – ideally less than 75 x 50mm

Chapter 3 - Low Power Design Techniques

3.1 Overview

Lowering a battery-powered circuit's power consumption means that operating duration may be usefully extended, or smaller or fewer batteries may be used, offering packaging advantages. In addition, less heat is dissipated, reducing the size of, or even eliminating the need for cooling fans and heat sinks. This has the advantage of reducing the effects of thermal drift in measurement circuits, which in turn may remove the need for temperature compensating components.

Low-power circuit design may only be achieved by the combination of a number of design techniques. As the circuit board track lengths are relatively short, the power hungry buffers and bus driver chips associated with large systems will not be required. Selecting low-power components and minimising the component count is a good starting point. This, together with effective power management, will have a significant effect, but there are many additional factors to consider.

3.2 Component Selection

When selecting a component, its typical operational power consumption must be considered in addition to the usual primary performance criteria. Many modern chips are based on CMOS (Complementary Metal Oxide Semiconductor) technology or its various derivatives. Under static conditions, CMOS power demand is minimal. Dynamic power requirements however can be considerable.

3.2.1 Power in CMOS Circuits

Field effect transistors (FETs) are the building blocks of all CMOS integrated circuits (ICs), microprocessors are constructed from many thousands of these devices. FETs in CMOS microprocessors, memory and digital systems operate as switches to provide binary logic functions. The FET's input, or *gate terminal*, has a resistance of many MegOhms and thus draws negligible static current. Dynamic power demand is due to the capacitance of gate terminal. As each logic transition causes the capacitor to charge or discharge, causing power to be dissipated. The more transitions, the greater the current consumed; thus, power demand is directly proportional to switching speed.

All microprocessor-controlled systems are synchronised to the system clock. The clock frequency, normally derived from a crystal–controlled oscillator, largely determines processor performance. As the clock frequency controls logic switching speed, it follows that higher clock speeds consume more power. This may be expressed in the form:

$$Power = V_{dd}^{2} f (C_L + C_d)$$

where V_{dd} = IC supply voltage, f = clock frequency,

C_L = load capacitance and C_d = device capacitance.

Like power consumption, processor performance, usually quoted in millions of instructions per second (MIPS) is also proportional to clock frequency. The ubiquitous desktop PC best illustrates this relationship; as performance has increased in line with processor clock speed, it can be seen that both the power supply and heat sink have significantly increased in size.

Whilst reducing the clock frequency to a minimum is desirable, this adversely affects processor performance capability. Some newer microprocessors use internal programmable phase-locked loops (PLLs), often indexed to an external crystal oscillator, to generate the system clock. This allows dynamic adjustment of the clock frequency to suit system performance requirements. Such devices, benefiting from a 4:1 clock ratio or better, provide a good balance of power versus performance.

The supply voltage, which is a squared term in the equation, may be reduced from the once common 5 Volt (TTL-level) to 3.3 Volts, or lower, on many devices. This would reduce power consumption by almost one-third. The latest generation of PC processors have a core voltage of 0.8 to 1.0 Volts to minimise power dissipation.

3.2.2 Microprocessor Busses

Microprocessors use pipelines known as busses to communicate with memory and peripheral devices. For optimum performance, these normally consist of parallel signal paths. The data bus, as the name suggests, carries system data, and in most instrumentation systems is either eight or sixteen bits wide. The address bus is used to map the memory and input / output peripherals, allowing individual locations to be addressed for read or write operations. Address bus width is dependent on the size of the memory to be addressed, thus a one-megabyte memory requires twenty (2^{20} = 1024kb) address bits.

When memory is accessed a considerable number of address and data bits are active, all at high switching frequencies. The more lines that are active, the greater the devices' load capacitance, and hence, the higher the power demand. As the width of the address bus increases with memory size, larger memories tend to consume more power. By

minimising the number of active bus lines, through multiplexing the address and data busses, or better still, by using a serial bus, power may be saved.

Serial busses typically require between one and four data lines to communicate with peripheral circuitry. Although usually lacking the throughput of parallel busses, serial busses offer a number of advantages:

- Fewer active lines result in lower load capacitance, reducing power demand
- Simplified circuit board layout and improved packing density
- Easier system expansion as fewer lines are required
- Fewer high speed signal lines may result less induced circuit noise

3.2.2a The I^2C Bus

Philips Semiconductor originally developed the Inter Integrated Circuit, or I2C bus, in the early 1980s (*Philips Semiconductor, 2000*). Many semiconductor manufacturers have since licensed the bus technology and it is in common usage. I2C also forms the basis of other bus systems, such as SMbus, which can be found in intelligent power supplies.

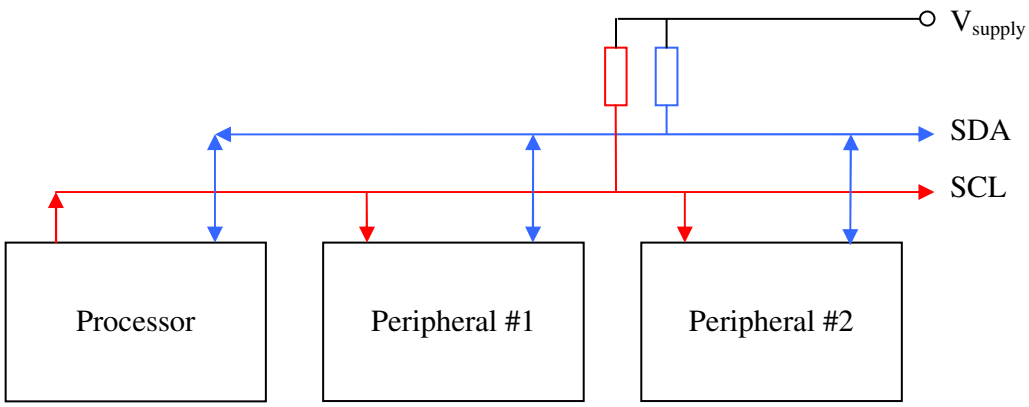

Figure 9: I^2C Connectivity

A master-slave system, I^2C uses two lines for synchronous half-duplex communication (see *Figure 9*): SCL, a master clock signal, and SDA, a bidirectional data line. Both lines are of open-drain configuration and thus require the addition of pull-up resistors to produce the higher logic state.

Compatible devices have encoded addresses assigned to them; Philips provides these to the manufacturer. In its original form, the seven-bit addressing could manage up to 128 nodes, with a typical bus speed of 100 kbits per second (kb/s). Later incarnations with ten-bit addressing, offer up to 1024 nodes at 400 kb/s (Fast Mode) and even 3.4 Mb/s (High-Speed Mode).

The I^2C bus tends to be used for less demanding, lower speed or infrequent communication between a processor and its peripherals. Typical examples include Electrically Erasable Memory (EEPROM or E^2ROM), real-time clock, lower speed analogue-to-digital and digital-to-analogue converters (ADCs and DACs), digital environmental sensors and power management chips.

3.2.2b The SPI Bus

Motorola's Serial Peripheral Interface (SPI) bus (*Freescale Semiconductor, 2003*), and the similar Microwire (National Semiconductor) and Three-Wire busses, are proving an increasingly popular means of IC data transfer. Like I^2C, SPI is a master-slave system. It uses three data lines for synchronous full-duplex communication, plus a separate chip select line for each peripheral device. Whilst this places a greater demand on the number of processor input/output (I/O) pins, it is outweighed by the performance benefits of the high bus speed (typically several Mbits per second).

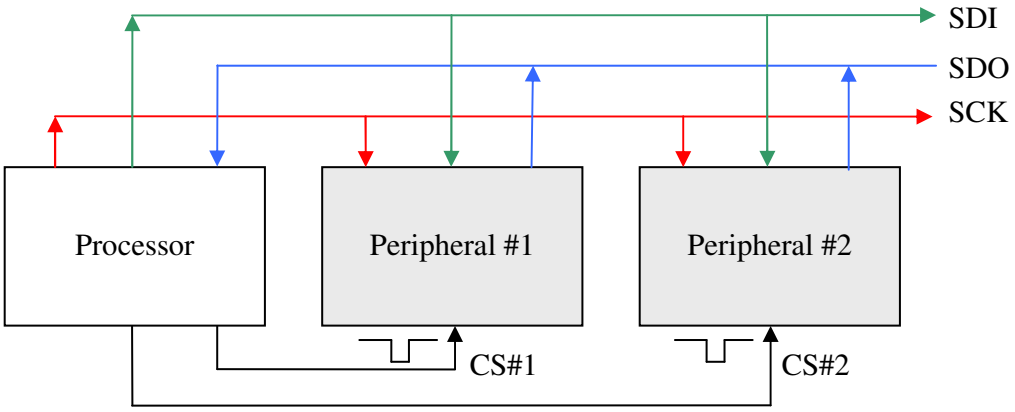

Figure 10: SPI Connectivity

The master clock signal, SCK, synchronises bus operation. In a conventional arrangement, the SDI (Slave Data In)/MOSI (Master Out Slave In) line outputs processor data, and the SDO (Slave Data Out)/MISO (Master In Slave Out) line receives data from peripherals. Peripherals are selected by driving the appropriate chip select (CS or SS, Slave Select) low.

In addition to its high bus operating frequency, SPI also has less software overheads than most other serial busses. The SPI bus offers the high-speed communication essential for acquiring, and storing, data logged at the throughputs called for in this project. Typical example devices include EEPROMs, flash memory cards, real-time clocks, ADCs, DACs (Digital to Analogue Converters) and programmable signal conditioning.

3.3 Power Management

The essence of power management is to minimise power usage. There are a number of active and passive techniques that may be used to reduce circuit power consumption.

3.3.1 Passive Methods

Most digital circuits use a few resistors tied to the supply Voltage (pull-up) or ground (pull-down) to maintain a signal line in a known state, high or low respectively. As current flows when the signal level opposes that of the resistor, it follows that a pull-up or pull-down resistor should be chosen to match the default logic of the signal line. Thus, power is only consumed only while the signal is active, and not in it's low-power state. The same principle holds when considering driving LEDs and output loads.

The value of a circuit's pull-up and pull-down resistors must also be considered. Values of 10k Ohms are very common. With a 5 Volt supply, each resistor will see a current of 0.5 mA; this can easily add up to a few milliamps across a circuit. As the input impedance of digital CMOS circuitry is very high, these resistor values may be increased to as much as 1M Ohm. Notable exceptions to this are when rise times or switching speed is critical. The gate capacitance of the FET CMOS input must be considered; lower resistances allow this to charge quicker, improving performance.

3.3.2 Active Control Methods

In most electronic circuits, there are usually some parts of the design that are only used periodically. Analogue signal conditioning for example has little part to play unless signals are to be monitored. To save power, the voltage supply to redundant circuitry may be turned off until needed. If power is to be selectively turned off, there are three main ways of achieving this. In the first two instances, care must be taken to ensure digital devices respond in a controlled manner once power is applied. If spurious signals appear on lines connected to the processor, they may cause a variety of intermittent problems or even cause the embedded software to crash.

3.3.2a Regulator Control

Many commonly available voltage regulators are provided with a shutdown terminal, this normally being pulled down to ground to disable the voltage output. If different functional blocks are powered from separate regulators, inactive circuits may be shutdown under processor control.

3.3.2b FET Power Control

An alternative to using several voltage regulators to control power is to use a number of FETs; these may also be switched under processor control. With an On Resistance (R_{DS}, or drain-source resistance) as low as a fraction of an Ohm, FETs are very efficient as there is negligible voltage drop and little power is consumed by the device.

3.3.2c IC Shutdown

Many devices now feature shutdown terminals allowing them to be individually disabled. Although valuable for minimalist designs, those with moderate chip counts would necessitate a significant number of dedicated control lines, tying up precious microprocessor outputs or requiring additional multiplexer chips.

Some advanced devices, such as RS-232 driver chips, automatically enter a low-power or sleep mode after a period of inactivity, awakening if a signal is detected on an input terminal. The number and type of chips with auto-shutdown is relatively small, although increasing, and is a likely growth area.

3.3.3 Phantom Power Problems

When devices are in their shutdown mode, or the voltage supply to their power terminals disabled, it is possible that they may still be drawing power from signal lines. A typical CMOS input, as depicted in *Figure 11*, features protection diodes that connect

the input to the power rails. If power is absent and the input is driven to a high logic level, current *i* can flow through the protection diode to power the chip.

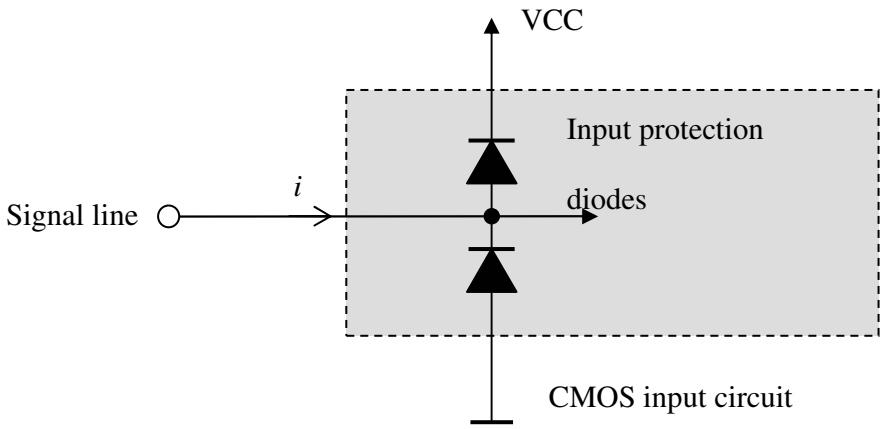

Figure 11: Phantom Power in a CMOS Input Circuit

After observing this phenomenon, whilst prototyping programmable gain signal conditioning based upon Maxim's MAX1452, a number of methods were employed to control the effects. Firstly, signal lines should ideally be held in a low logic state whenever components are in shutdown. This is not always possible as some lines, such as bus signals for example, may also be connected to active parts of the circuit. In this instance, the addition of a series resistor can limit the current flow to more acceptable levels.

Chapter 4 - An Investigation of Power Supply Options

Field instruments are often powered by internal batteries, although some depend on external supplies. There are a variety of battery technologies available, in a range of shapes and sizes, and with different terminal voltages and capacities. The power source feeds the system's power supply circuitry which may provide several different voltage outputs to satisfy the demands of the system circuitry.

4.1 Types of Battery

Batteries, which, strictly speaking are a collection of cells, are classified as either primary (single-use or non-rechargeable) or secondary (rechargeable). Battery capacity is quoted in milliamp hours (mAh), which is a measure of duration when delivering current into a load impedance. This section discusses the benefits of the various battery types.

4.1.1 Primary Cells

Primary cells include Zinc-Carbon, Zinc-Chloride, Alkaline, Lithium Thionyl Chloride (Li-$SOCl^2$), Lithium-Iron Disulphide (Li-FeS^2) Mercury and Silver Oxide. Of these, Mercury cells are too specialised, not to mention difficulties with the Restriction of Hazardous Substances (RoHS) regulations (*HMSO, 2006*), and Silver Oxide cells, as found in watch batteries, are expensive and of limited capacity. Examples of the various formats and their form factors are described in *Table 3*.

4.1.1a Zinc Carbon/Zinc Chloride

These are the standard consumer batteries, having a cell voltage of 1.5V. They are now largely being supplanted by Alkaline batteries on supermarket shelves. They suffer

minimal self-discharge, but have a relatively high internal resistance which precludes their use in applications requiring higher currents.

4.1.1b Alkaline

Alkaline Manganese Dioxide cells (normally shortened to Alkaline) have the same terminal voltage and shelf life as Zinc Chloride, with a reduced internal resistance and higher capacity. Thus, they are better suited to higher current applications.

4.1.1c Lithium-Iron Disulphide

Li-FeS^2 cells are compatible with both alkaline and Zinc Chloride cells, but offer extended shelf life and operating temperatures and provide a high current output.

4.1.1d Lithium Thionyl Chloride

These have a terminal voltage of 3.6V (twice that of the other types), a relatively high capacity and a wide operating temperature range. They are designed for long-term use rather than high current drain, but are quite expensive and not readily available.

Type	Manufacturer	Format	Voltage (V)	Capacity (mAh)	Size (mm)
Zinc Chloride	Eveready Silver	AAA	1.5	560*	44.5 x Ø10.5
Alkaline	Duracell Plus	AAA	1.5	1,150*	44.5 x Ø10.5
Li-FeS^2	Energizer L92	AAA	1.5	1,250***	44.5 x Ø10.5
Alkaline	Duracell Plus	AA	1.5	2,850*	50.5 x Ø14. 5
Li-FeS^2	Energizer L92	AA	1.5	3,000**	50.5 x Ø14. 5
Li-$SOCl^2$	Saft LS14500	AA	3.6	2,250	50.3 x Ø14.65
Alkaline	Energizer E93	C	1.5	8,350*	50.5 x Ø26.2
Alkaline	Energizer	PP3	9.0	625	48.5 x 26.5 x 17.5

The quoted capacities assume an endpoint voltage of 0.8V, 0.9V** and 1.0V *** respectively.*

Table 3: A Comparison of Primary Cells

(Source: RS Components and Manufacturer's Data Sheets)

4.1.1e Primary Cell Comparison

In considering AAA cells, Zinc Chloride has half the capacity of Alkaline or Li-FeS2. In turn, AA cells are just over twice the volume of AAAs but have a superior energy density. The PP3 battery has the lowest energy density of all; the combined internal resistance of its six series-connected cells also seriously restricts is use in anything except low power applications.

4.1.2 Secondary Cells

Common secondary cells include Lead-Acid, NiCad, NiMH, Lithium-ion and Lithium Polymer. Lead-Acid batteries must be discounted due to their size and weight; they are better suited to high-power applications in larger systems. Over the last few years, NiCad batteries have gradually fallen out of favour and are generally being replaced by the more environmentally friendly NiMH cells; thus, they too are not included in the comparisons in *Table 4*.

4.1.2a Nickel Metal Hydride

Rechargeable NiMH cells (which a have a low internal resistance) are replacing Alkaline cells in many applications where a high current demand is required. They are available in both OEM packages and a range of popular sizes, and in many cases, the nominal 1.2 – 1.3V terminal voltage is close enough to that of Alkaline batteries to ensure compatible operation. They may be recharged at rates ranging from a trickle (a few mA) to a fast charge at 1C (equal to the mA capacity rating) or more.

Drawbacks of this technology are self-discharge, which can exceed 20% of the total capacity in a month (depending on the ambient temperature), and a limited charge/discharge cycle life. Most manufacturers quote a typical life expectancy of 500

cycles, although this is dependent on the typical duty cycle, charge and discharge rates and temperature. The maximum storage capacity also deteriorates as the battery ages; this is a good indication that replacement is due.

4.1.2b Lithium-Ion and Lithium Polymer

The major difference between the two forms of rechargeable Lithium cells is the electrolyte. With Li-ion, it has a liquid or gel form, whilst in Li-Poly cells it is a solid polymer, and thus leak-free. This subtlety does affect performance; both types offer high capacity but Li-Ion has a superior current output capability. The cells are generally designed for OEM (Original Equipment Manufacturer) use and non-removable. The packaging, which can be of a thin flat housing or of a soft and flexible construction, facilitates accommodation in a small enclosure. These cells offer most of the benefits of NiMH, but with higher energy densities, and significantly lower self-discharge. They offer the best volumetric and gravimetric energy efficiency of all of the cell types studied.

There are a number of issues with to consider with Lithium secondary cells. They require a special charging regime (constant current - constant voltage), and may be irreversibly damaged if overcharged or discharged excessively. To prevent damage they are normally fitted with onboard protection circuits, but careful battery management is required for optimal performance. Although they typically have a reasonable life cycle, cell capacity shows irrecoverable degradation over time. This is charge and temperature dependent and can exceed 30% per annum.

In its metallic form, Lithium is highly reactive. At higher temperatures batteries may even ignite or explode. Lithium cells gained a certain amount of notoriety during 2006

after the widely reported problems with laptop PC batteries catching fire. This prompted system manufacturers to recall several million Sony-produced batteries.

Type	Manufacturer	Format	Voltage (V)	Capacity (mAh)	Size (mm)
NiMH	Sanyo HR-4U	AAA	1.2	1,150	44.5 x Ø10.5
NiMH	Duracell	AA	1.2	2,500	50.5 x Ø14. 5
NiMH	Ansmann	C	1.2	3,500*	50.5 x Ø26.2
Li-Ion	Enix 800040	Soft Pack	3.75	6,800	70 x 60 x 20
Li-Ion	Enix 800052	Soft Pack	7.5	2,200	70 x 37.5 x 19
Li-Poly	Varta PoLiFlex	Pack	3.7	1,560	66 x 35 x 4.2

Table 4: A Comparison of Secondary Cells

(Source: RS Components and Manufacturer's Data Sheets)

4.1.2c Secondary Cell Comparison

Compared to Lithium cells, NiMH are cheap and well established. Both degrade over time, with Lithium being the worst offender. Whilst both battery types suffer from self-discharge, Lithium is markedly better than NiMH. With respect to charging, both may be fast charged (in an hour or less) although the charger requirements are quite different. Lithium cell packaging requires that they are built-in to equipment, requiring the development of battery management and charging circuitry. NiMH cells are, for the most part, compatible with popular non-rechargeable cells; this facilitates their in-field replacement with whichever type is appropriate or freely available. For this reason, the comparison in *Section 4.3.2* will focus on NiMH cells.

4.2 Voltage Regulation

The problem with battery power is that the voltage level changes over time as the battery discharges. For reliable operation, both analogue and digital circuits need to run

from a constant voltage source. A voltage regulator maintains a constant output voltage from a variable voltage input. There are two types of voltage regulator, linear and switch mode. These are described and compared in the next sections:

4.2.1 Linear Regulators

These are the simplest and cheapest type of voltage regulator. Linear regulators are offered by many semiconductor manufacturers, and come in a variety of packages, voltage and power ratings, with fixed or adjustable outputs, and with or without shutdown options. Few additional components are required (see *Figure 12*) to construct a basic circuit.

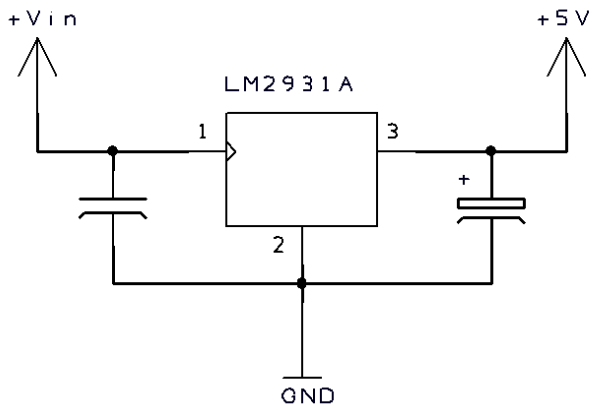

Figure 12: A Typical Linear Regulator Circuit

A characteristic of all linear regulators is that the input voltage must be higher than the output (*Maxim, 2001*). For maximum efficiency, the difference between the input and output, known as the Drop-out voltage, should be as small as possible; the greater the difference, the more power is wasted as heat. Power dissipation is given as:

Power Dissipation = (Voltage in – Voltage out) / Current out

Low drop out (LDO) devices with a dropout voltage of around 100 mV are available for lower current ratings.

4.2.2 Switch Mode Regulators

Unlike linear regulators, switching, or switch-mode voltage regulators are able to produce higher, lower or negative outputs with respect to the input. There are various circuit configurations to satisfy the output requirements, but they are all loosely based around a PWM (pulse width modulation)-controlled transistor controlling the charge/discharge cycle of a inductor and capacitor circuit. The switching frequency is normally quite high (up to a megahertz) as this allows lower value, and therefore smaller inductors and capacitors to be used.

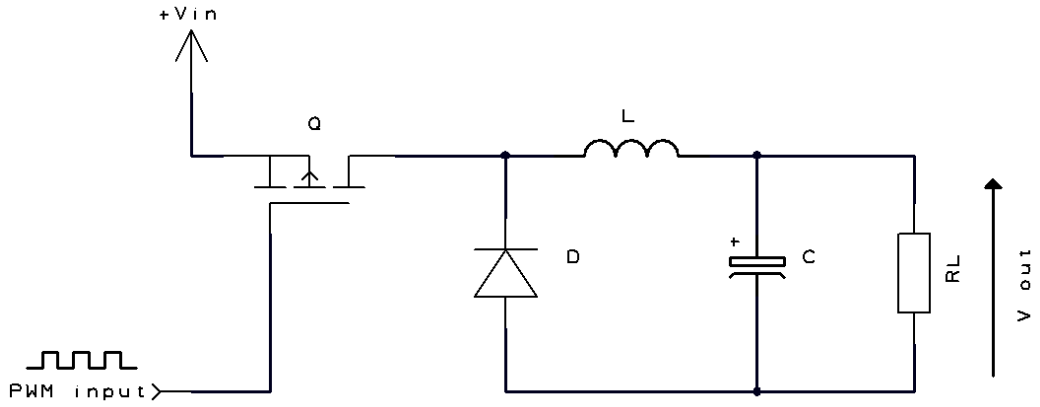

Figure 13: A Basic Step-Down or Buck Converter Circuit

The layout of a basic step-down switching regulator (*National Semiconductor, 2002*), also known as a buck converter, is shown in *Figure 13*. Turning on the FET, *Q*, causes the inductor, *L*, to charge and initiates the charging of capacitor *C*. When *Q* is turned off, the inductor discharges through capacitor *C*, which smoothes the output to drive a load, R_L. The output voltage is dependent on the duty cycle of the PWM control

signal; the feedback circuit that controls this is not shown in the schematic. As the transistor is either turned off, or saturated, it consumes little power; efficiency ratings approaching 95% are not uncommon.

A SEPIC (Single Ended Primary Inductance Converter) can provide a good solution for battery powered systems. It is able to both step-down and boost the input voltage, as appropriate, to maintain a constant voltage output. This can help extract more energy from a partly discharged battery's reduced terminal voltage. SEPICs tend to add to circuit complexity and component count although single chip solutions, requiring only external passive components, are readily available.

A drawback of all switching regulators is that they generate circuit noise. This is due to switching noise caused by surges as the inductor charges and discharges. The noise produced is predominantly at the switching frequency (and its harmonics) and can be as high as 200mV peak to peak.

4.3 Power Supply Selection

For optimum performance, the battery characteristics should be a good match for both the instrument's power requirements and usage patterns. Therefore, the PDL's typical usage pattern and duty cycle must be considered. Ideally, the power supply should have the following properties:

- Output for 3.3V (200mA*) digital supply,
- Outputs for separate 5V analogue (50mA) and 5V sensor excitation (50mA) supplies, with shutdown facilities,
- Low noise
- Battery powered
- USB power option

- Capable of running for extended periods on one charge or set of batteries

* The specified output current for the 3.3V supply is based upon a worst case estimate, and allows around 10% headroom.

4.3.1 Regulator Selection

In selecting the type of regulator for the design, their respective properties must be carefully considered:

Switching regulators are more efficient than their linear counterparts, and, as they may operate from voltage levels below that of their outputs, are able to extract more power from a battery. The inherent switching noise however is a concern for precision analogue circuits.

Linear regulators cannot offer the same levels of efficiency as switching circuits, extract less power from a battery and may require heat sinking. Their benefits lie in low-noise operation and a minimal component count.

Ultimately regulator choice boils down to efficiency versus noise, and which is of greater importance for the design – battery life or measurement accuracy. Consensus in manufacturer's design guides, application notes, and textbooks (e.g. *Hill and Horowitz, 1989*), is that switching regulators should be avoided for precision analogue measurement circuits. Switching noise may be reduced, by adding a LDO linear regulator to the switching regulator's output (reducing efficiency) and/or adding RC low-pass filters around the circuit for example, but only at the expense of increased complexity, component count and therefore, cost.

As the PDL has the potential to sample analogue signals to a 16-bit resolution, circuit noise would seriously compromise measurement accuracy. Thus, in keeping with best

practice, linear regulators would provide the best option. Even with a dynamic load, as the power management control demands more or less current, noise should be kept in check. Although efficiency is sacrificed, power losses may be reduced if a device with a very low dropout voltage is specified.

4.3.2 Battery Selection

If linear regulators are to be used, the battery output must be greater than that of the highest voltage regulator. As a 5v supply is required, this necessitates a battery output of at least 5V plus the regulator's drop-out voltage. When considering the different cell types, in practical terms this provides the options shown in *Table 5*.

Cell Type	Terminal Voltage	No. of Cells	Output Voltage
Alkaline	1.5V	4	6V
Alkaline	1.5V	5	7.5V
NiMH	1.2V	5	6V

Table 5: A Comparison of Battery Output Levels

As the battery output voltage is close to that of the regulator's minimum input, the battery characteristics are of particular interest. The simple test circuit in *Figure 14* was constructed, with load resistor (R_L1 and R_L2) values of 10Ω and 3.3Ω being selected for two tests.

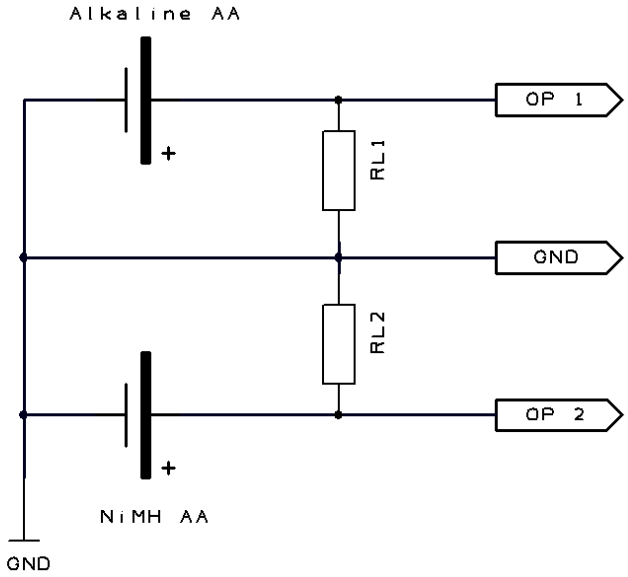

Figure 14: Battery Discharge Test Circuit

These loads were chosen as they represent estimates of the typical operational and worst case maximum transient system loads respectively. Outputs *OP 1* and *OP 2* were connected to the analogue inputs of a CIC CardCorder data acquisition system to log the test results.

Figures 15 and 16 depict the comparative discharge characteristics of Alkaline (Duracell Procell) and freshly charged NiMH (Uniross 2500 mAh) AA cells. The shape of the discharge curves in both graphs is very distinctive. The Alkaline cell voltage shows a gradual voltage drop off as it discharges while the NiMH cell voltage plateaus before falling away rapidly.

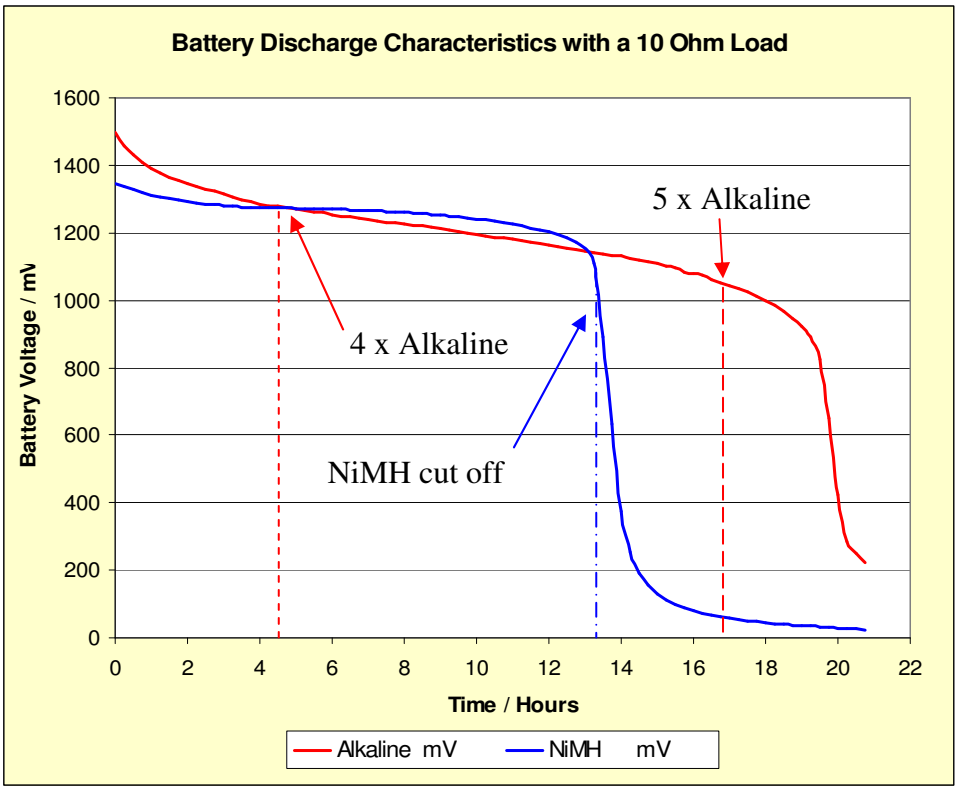

Figure 15: A Comparison of Battery Discharge Characteristics with a 10Ω Load

It should be noted that as the initial terminal voltages are different for the two battery types, Ohm's law comes into to play. As the current drawn is dependent on the initial terminal voltage, the initial currents would be:

Alkaline cell - 1.5V / 10Ω = 150 mA & 1.5V / 3.3Ω = 454 mA

NiMH cell - 1.3V / 10Ω = 130 mA & 1.3V / 3.3Ω = 393 mA

As this demonstrates, the initial current consumption at 10Ω and 3.3Ω loads is around 15% higher.

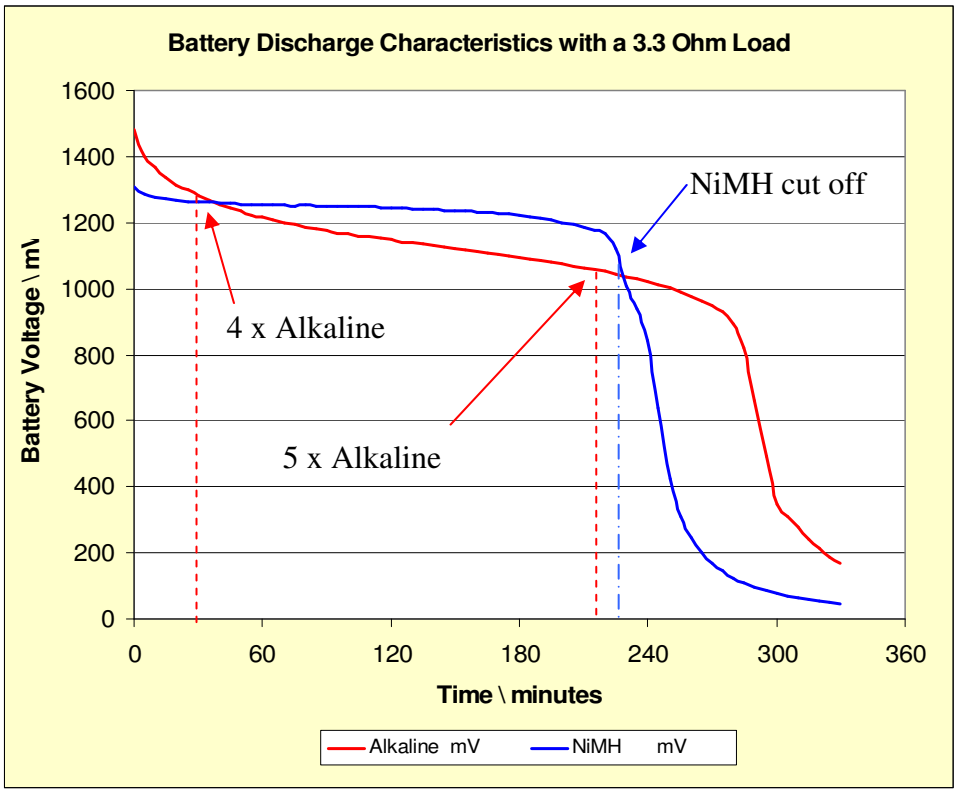

Figure 16: A Comparison of Battery Discharge Characteristics with a 3.33Ω Load

Of particular interest is the minimum voltage required to operate a 5V voltage regulator. The input threshold for a 5V LDO regulator is a nominal 5.2V; dividing this figure by the number of cells gives the cell cut-off voltage. The cell cut-off voltages for the battery packs quoted in *Table 5* are shown in *Figures 15 and 16*. The quoted endpoint discharge voltage for a NiMH cell is 1.1V and therefore this figure is used for the cell cut off voltage.

Cells	Cut Off	10Ω Continuous	3.3Ω Continuous
4 x Alkaline	1.3V	4.5 hours	0.5 hours
5 x Alkaline	1.05V	17 hours	3.5 hours
5 x NiMH	1.1V	13 hours	3.75 hours

Table 6: Approximations of Battery Life for Continuous Operation with a 5V LDO Regulator

The approximations of continuous battery life shown in *Table 6* must be treated as such as there are other issues to consider when dealing with multiple cells. Alkaline cells have a relatively high internal resistance, which increases as the cell discharges. As the internal resistance of a battery pack is the sum of that of the cells, the voltage drop off will be more pronounced.

In continuous operation, the PDL's power management can reduce power consumption to a minimum by shutting down redundant circuits. This would extend battery life well beyond the figures quoted in this section. With intermittent use of perhaps one hour per day (an average of $1/24^{th}$ of continuous use) and power management, PDL battery life expectancy would be improved dramatically.

Even though the Alkaline cell initially appears (graphically) to offer the best operating time, examination of the respective cut off voltage markers tells a different story as much of the cell's capacity is unused. NiMH cells show a superior performance with higher power demands, but for long-term operation self-discharge becomes an issue.

An important point of concern is that of operating temperature; most batteries show reduced terminal voltages and capacities at temperatures approaching 0°C. The resulting reduction in battery life can be quite dramatic as the lower terminal voltage means operating closer to the regulator's cut off voltage. Some alkaline batteries can lose up to 60% of their normal capacity *(Energizer, 2007)* at 0°C compared to that at room temperature (20°C). Nickel Metal Hydride cells demonstrate better low temperature characteristics, losing around 30% of their capacity over the same range *(Energizer,*

2001). Compared with these technologies, Lithium iron disulphide (Li/FeS_2) cells offer superior performance over a broader temperature range *(Energizer, 2005)*.

All three battery technologies discussed in the previous paragraph are available in the familiar AA and AAA form factors. In terms of gravimetric energy density, manufacturer's data sheets (Energizer) show Li/FeS_2 at 208 mAh/g, alkaline at 124 mAh/g and NiMH providing 83 mAh/g for AA cells. Here the Li/FeS_2 cells come out on top. With discharge characteristics similar to alkaline cells, they are more expensive, but with increased capacity and extended operating temperature range, they provide a useful alternative.

For field applications, the ability to easily replace old or tired batteries rather than charge equipment before use can be advantageous - the user should never be left high and dry. Popular battery sizes such as AA and AAA are readily available, and the appropriate technology may be selected to suit the application and environmental conditions.

Chapter 5 - Circuit Design

5.1 System Architecture

The architecture of the basic system in *Figure 17* shows how the various component blocks are arranged. At the heart of the system is a microcontroller, this is typically based on the common 8051 processor core, or one of Atmel's AVR or Microchip's PIC family of devices. There are many variants of these devices with on-chip 10- or 12-bit ADCs and real time clocks; this level of integration can simplify the design, minimising external components and saving valuable circuit board space

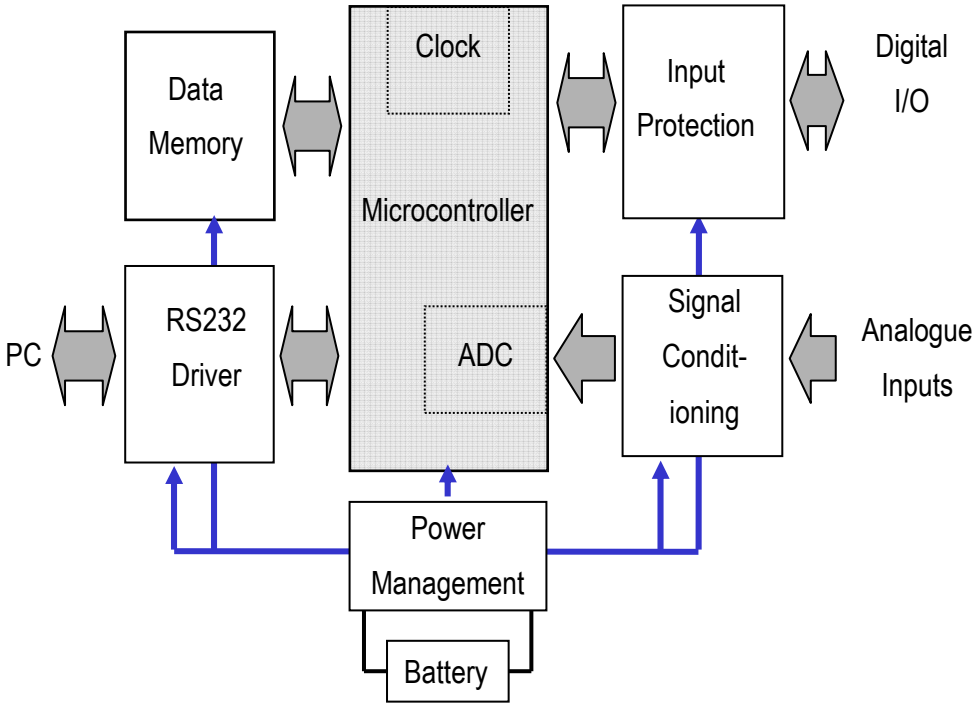

Figure 17: Basic System Architecture

To reduce the circuit's power demand the microcontroller operates from a minimal crystal frequency. This frequency will be determined by the level of performance required, and the microcontroller's UART's (Universal Asynchronous Receiver/ Transmitter) demands in interfacing to an RS-232 port at standard baud rates.

5.1.1 Design Outline

Whilst similar in concept, the Personal Data Logger (PDL) design is split into functional areas, on separate circuit boards. This project is concerned with the design of the PDL system core, as depicted in *Figure 18*, which controls all aspects of system operation.

An integrated ADC typically has inferior resolution, performance and signal-to-noise ratio than a dedicated chip, which provides the best all-round option. In addition, the design includes a USB and serial interfaces, and a flash card for mass data storage. Other components, such as the real time clock, would feature on a second circuit board together with the system power supply and connectors; further details may be found in *Section 5.6*.

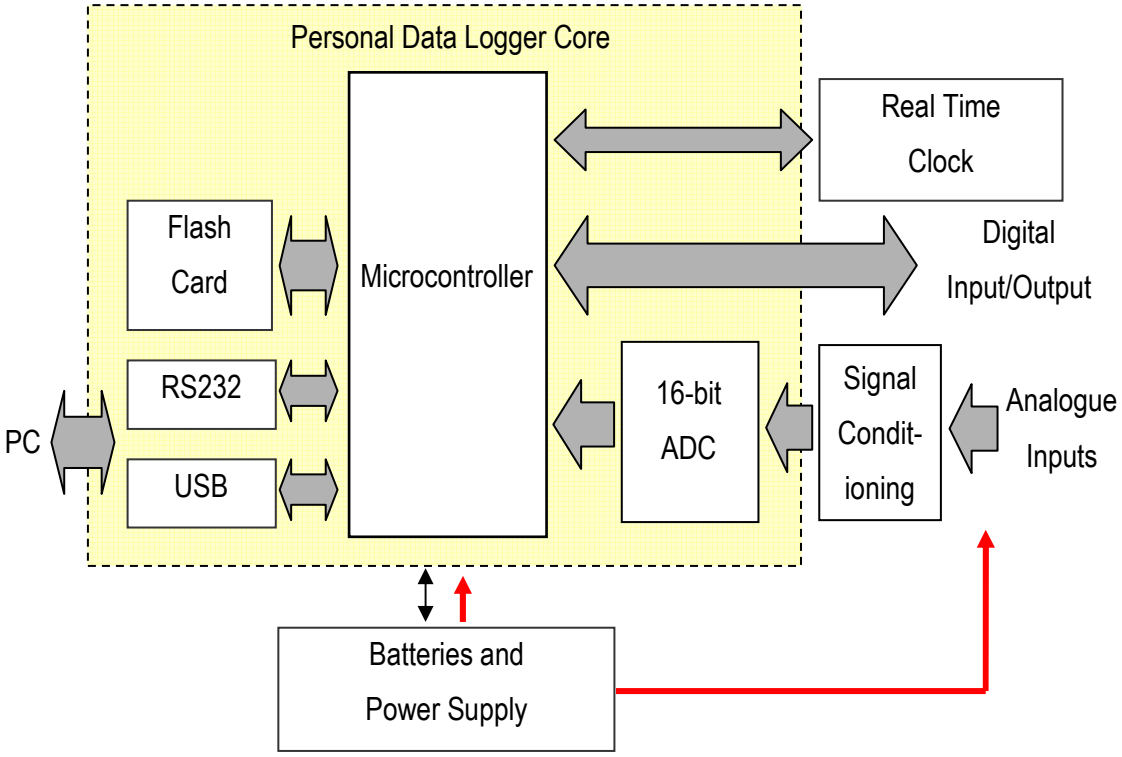

Figure 18: Design Project System Architecture

5.2 Device Selection

When selecting components for the design, there are some common criteria to consider in addition to type-specific issues :

Power demand: Low power devices are preferred.

Availability: Parts should be of current manufacture, and not subject to extended lead times or large minimum order quantities.

Packaging: Devices should be available in packages suitable for low-volume manual assembly.

Component availability proved to be a bigger issue than originally anticipated. Some supplier's offerings are seemingly only available to the volume market. Thankfully, there are a few manufacturers, such as Maxim, Microchip and Ramtron, who are pleased to provide sample quantities; these are ideal for prototyping.

Another important issue is that of chip packaging. The push for ever smaller components is driven by the mass market demand for hand-held, high-tech consumer electronics. Some otherwise ideal components could not be considered due to their small size and terminal arrangement, with Ball-Grid Array (BGA) and the increasingly popular Quad Flat No-lead (QFN) being the main culprits. Miniaturisation is perfectly suited for mass production, but without specialist equipment is a step too far for low volume production. Hand assembly is not an option.

5.2.1 Choosing a Microcontroller

There are many devices that may be considered, including high performance chips from Atmel's AVR and Microchip's PIC families and the MSP430 series from Texas

Instruments. Whilst systems based upon both PICs and AVRs have been successfully developed within the school, the highly-integrated ARM-based microcontrollers are of greater interest. They have many of the features found on AVRs and PICs, but their RISC (Reduced Instruction Set Computer) architecture offers distinct advantages. RISC machine code, which is executed at one instruction per clock cycle, is both code-efficient and offers performance benefits. Many manufacturers offer chips based around the ARM-7 processor core. These may differ in terms of the range of features provided, but typically share the same software development environment and tools.

The ideal microcontroller for this design project should have the following features:

- Low power operation, with power saving and power-down modes
- Programmable clock frequency to optimize system performance
- On-chip SRAM for temporary storage
- On-chip Flash memory for embedded code storage
- In System Programming (ISP) and good software development tools
- SPI and I^2C serial bus interfaces
- On-chip USB controller
- On-chip UART for serial RS-232 interfacing
- 16 or 32-bit timer/counter inputs
- Multiple general purpose I/O (input/output) terminals

The properties of a range of ARM processors from a range of manufacturers are shown in *Table 7*:

	STR711FR2T6	AT91SAM7S64	LPC2148
Clock	66 MHz max	55 MHz max	60 MHz max
Number of Pins	64	64	64
Flash (kB)	272	64	512
SRAM (kB)	64	16	40
USB	Yes	Yes	Yes
Clock Scaling	Yes	Yes	Yes
Max Current (mA)	150	50	90
SPI	2x	1x	2x
I^2C	1x	1x	2x
JTAG	Yes	Yes	Yes

Table 7: A Comparison of ARM Processor Properties

After careful consideration of the various ARM devices, taking into account the aforementioned features and component availability, the Philips LPC2148 microcontroller (*NXP, 2005*) was selected for the project.

5.2.1a LPC2148 Key Features

Low Power Consumption

The ARM7 processor core runs at 1.8V, which helps reduce power consumption. This voltage is derived from the 3.3V supply via an on-chip dc to dc. Operating from an external 60MHz crystal, the LPC2148's programmable phase-locked loop (PLL) provides system clock frequencies of 10 - 60 MHz. This gives a net current consumption ranging from 15 – 90mA at 3.3V (*NXP, 2006*), depending on the PLL setting and the number of active on-chip peripherals; inactive parts of the device may be shutdown under software control to minimise power demand. Power-down modes can reduce consumption to round 100μA.

Memory

The chip has a generous 512kB of flash memory for embedded software code or long-term data storage. With this amount of non-volatile memory, there is plenty of code space available for software development. In addition, 32kB of on-chip SRAM may be used to temporarily store code or data.

In-System Programming

An industry standard JTAG (Joint Test Action Group) port is provided for in-system programming, software development and debugging. A range of software tools, JTAG adapters and emulators are available from leading vendors such as IAR Systems and Keil; these are available within the School.

Serial Busses

The device features two I^2C bus interface ports. These are capable of operating at up to 400 kB/second, and in master or slave configuration. For higher speed operation (up to an eighth of the system clock frequency), SPI is available. Additionally an SSP (Synchronous Serial Port) bus may be configured for SPI, Microwire or Three-Wire bus operation.

Communications

Two UARTs (Universal Asynchronous Receiver Transmitters) are available for serial communication. UART0 offers a basic transmitter-receiver pair whilst UART1 has a full eight-line modem interface. An on-chip USB controller is provided for high-speed data transfer, at up to 12 megabits per second, to a USB host.

General Purpose Input/Output Terminals

Most terminals have multiple functionality. The chip's Pin Connect Block allows individual terminals to be configured as either basic input or output pins, or for a range of other functions depending on design requirements.

Other Features

The chip also has a range of other features which include:

- an onboard real-time clock running from an external 32kHz crystal
- up to fourteen 10-bit analogue to digital converter (ADC) inputs
- a 10-bit digital to analogue converter (DAC) output
- up to six pulse width modulation (PWM) outputs
- two 32-bit timer/event counters
- external interrupt pins
- sophisticated power management

5.2.1b LPC2148 Pin Assignments

With such a versatile device as the LPC2148, there are many design decisions that must be made. The chip has 64 terminals, most of which (as previously stated) support a number of different functions. This is best illustrated in *Figure 19*:

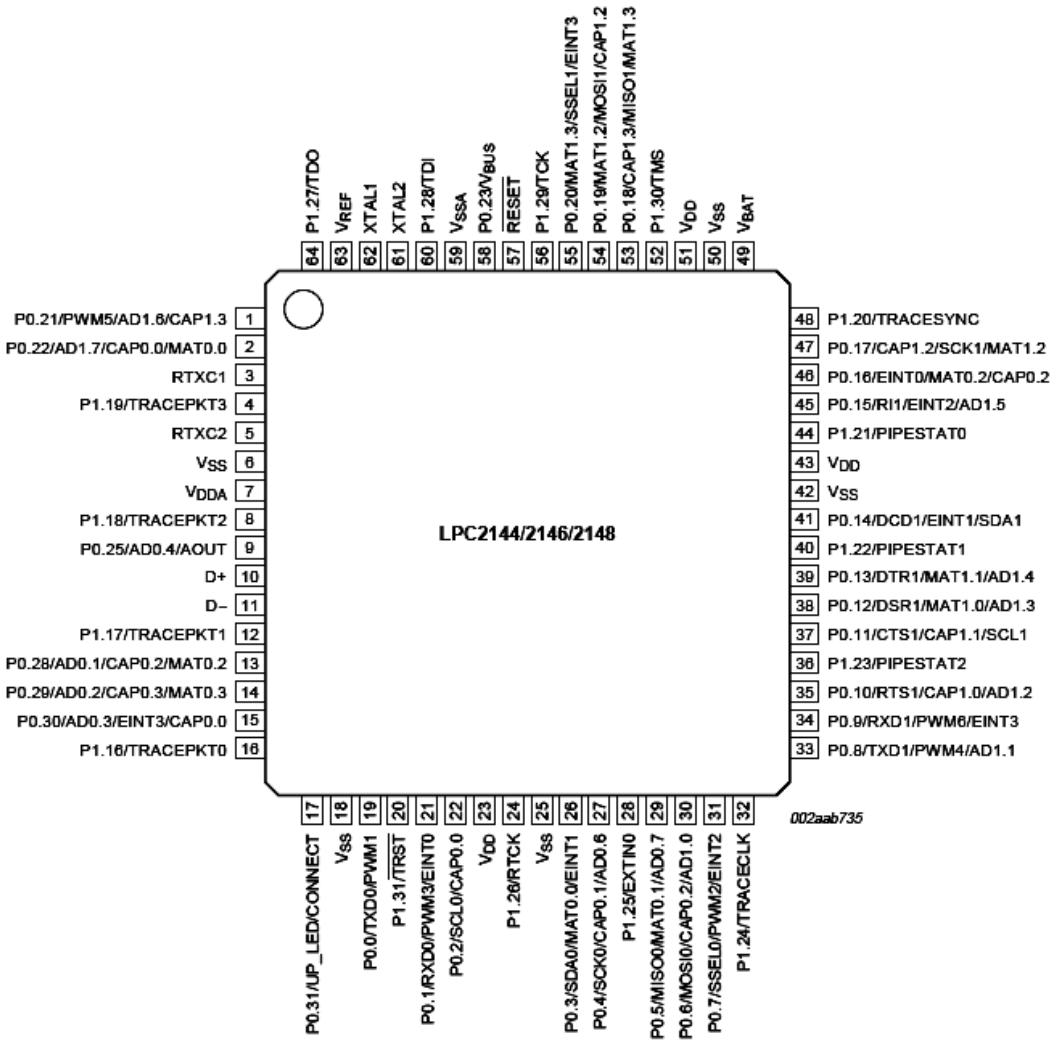

Figure 19: LPC2148 Microcontroller Pin Mapping (NXP, 2005)

Careful consideration is required before pin functions can be defined. The primary purpose of the design is to acquire and store data, with an emphasis on high performance. Therefore, as two SPI-compatible serial busses are available this allows the memory and ADC to be assigned to separate busses, improving system performance. An I^2C port provides interfacing for a real-time clock and board expansion.

As the design has the option of mass data storage via an onboard memory card, USB will be the primary means of transferring data. A basic RS-232 serial port provides a

lower-speed secondary transfer method and serial expansion, the full modem interface of UART1 is not required. In considering these issues, the device pin assignment outline can be simplified as shown in *Figure 20.*

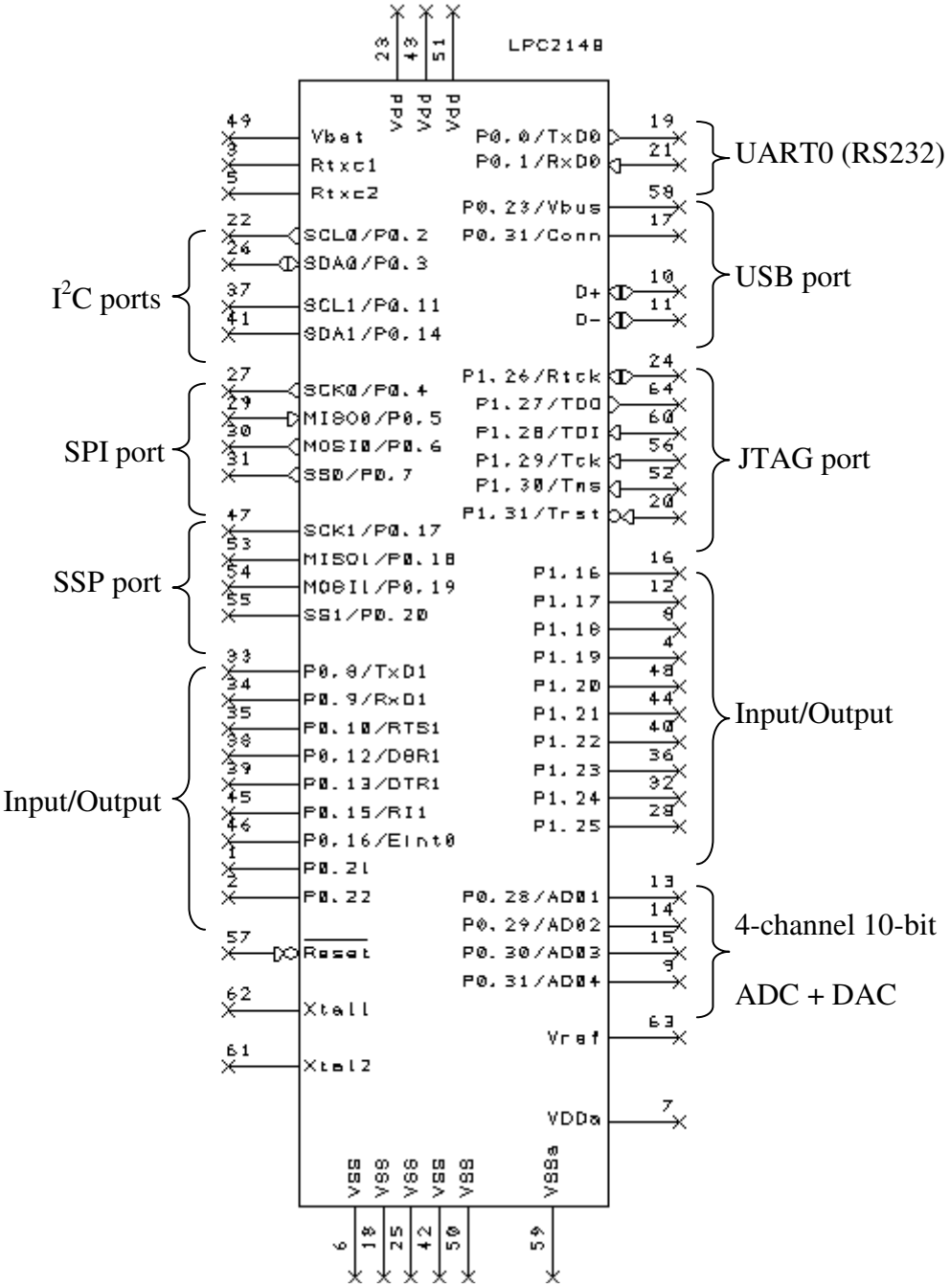

Figure 20: LPC2148 Microcontroller Pin Assignments

5.2.2 Selecting an ADC

A typical analogue data acquisition sub-circuit usually consists of a number of chips – a multiplexer, sample and hold amplifier, voltage reference and ADC at its most basic level.

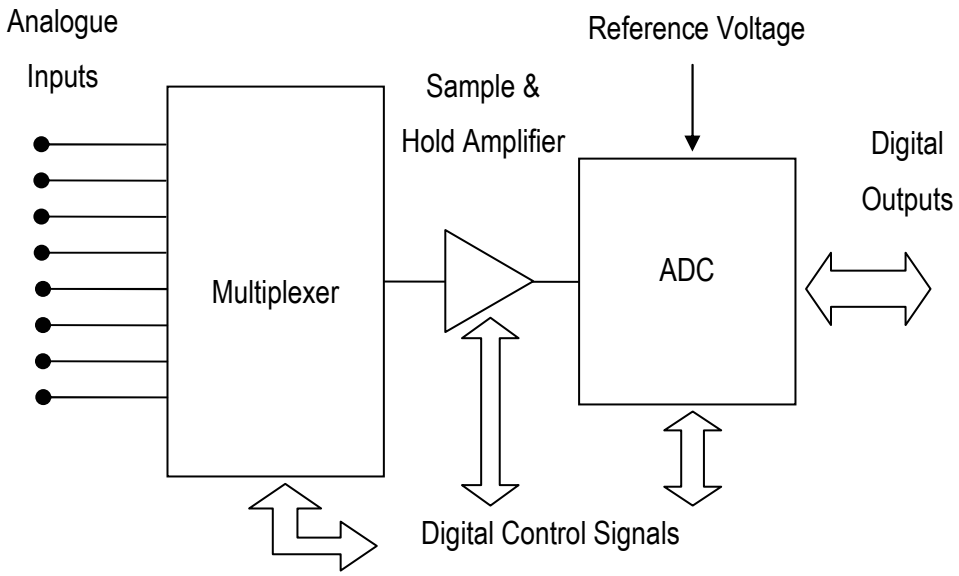

Figure 21: A Basic Analogue Data Acquisition Circuit

The multiplexer sequentially switches an analogue input to the sample and hold amplifier, here the waveform is sampled and 'frozen' while the ADC performs the analogue to digital conversion. With the conversion complete, the ADC sends a signal to a microprocessor that initiates the process once more.

The throughput of the circuit is dependent upon the sum of the multiplexer settling time, the acquisition time of the sample and hold amplifier and the conversion time of the ADC. The timing of the control signals is critical for accurate data conversion.

The analogue to digital conversion process has largely been streamlined with the advent of chips that include all the necessary circuitry in a single monolithic package.

Apart from the convenience a single-chip solution offers, the timing is simplified and there is a significant saving in both cost and board space.

The design specification calls for a multi-channel 16-bit ADC, with a serial SPI compatible interface. In addition, the device should also:

Operate from a single-rail supply voltage of no more than +5 Volts, with the possibility of running the digital interface from a lower voltage to save power.

be capable of sampling at more than 100,000 samples per second

have an integral multiplexer providing at least four, or preferably eight analogue input channels

There are a number of seemingly suitable ADCs available; their specifications are shown in the following table:

Device	**Manufacturer**	**Power (mW)***	**Sample Rate (ksps)**	**Inputs**	**Input Range**
LTC1859	Linear Tech	40	100	8	0-2.5V, 0-5V, ±5V, ±10V (programmable)
LTC1867	Linear Tech	6.5	200	8	0-4.096V, ±2.048V
MAX1168	Maxim	13.3	200	8	0-4.096V, 0-V_{ref}
ADS8345	Texas	10	100	8	Vcc/2

Table 8: A Comparison of Selected ADC Properties

** The power consumption quoted is the typical power at the given sample rate; this figure should be reduced at lower sampling rates.*

There are surprisingly few ADC chips that meet the criteria. The LTC1859 can be disregarded due to its relatively high power demands. Of the other three, the ADS8345 appears quite attractive due to its convenient input range. However, the MAX1168

requires much less processor intervention, and therefore less software overheads, as the converted data from all eight channels is read by the processor in one go. This compares favourably against the other ADCs which transfer data one channel at a time. For this reason, and the fact that the chip has been used successfully in Cranfield Health's Tandem Gas Analyser instrument, the MAX1168 was selected for the design.

5.2.3 Data Storage

After evaluating available options, it was decided the best approach was to include two memory devices, a flash card for mass data storage and a small non-volatile memory chip for local or temporary storage. The addition of the second device allows the contents of the microcontroller's registers and critical data to be backed up for continuity after system power failure. It would also provide a small amount of data memory, permitting the design to operate without the flash card for power critical applications where only minimal storage capacity is necessary.

5.2.3a Flash Card Storage

There are numerous different types of Flash memory card available: PCMCIA (also known as PC Card), Compact Flash (CF), MMC, SD, XD-Picture Card and Memory Stick Pro to name but a few. Factors that must be considered in choosing a card include-

Power Consumption

The device should ideally operate from a single supply voltage of 3 to 5 Volts, and draw minimal current. It should be noted that although the quoted power consumption can be quite high, this is often a worst case. Actual consumption is dependent on whether data is being written to the card or read from it; the quiescent current is usually very low (typically around 500 μA) and may be considered to be negligible.

Connector Availability

Printed circuit board (PCB) mounted connectors should be readily available from a number of different suppliers. The card housing should be firm and secure, and not significantly larger than the card itself. As it is intended to leave the card in-situ, an ejecting card socket is not essential.

Bus interface

The flash card should be compatible with the SPI serial bus interface

Data Read and Write Times

System performance is, in part, dependent on the time required to write logged data to the card. A fast card is therefore desirable as this maximises system performance. The read time is not so critical but this may have influence on data download times.

Size

The card should be reasonably small as card size will have an influence on circuit board size, and determine circuit board layout.

The selected media should be widely available and not disproportionately more expensive than other flash cards. XD and Memory Stick Pro cards are largely proprietary to Olympus\Fujifilm's and Sony's products respectively, and are not that well supported; thus for this reason they were not considered for this design.

The following table shows a comparison of three popular card types, each with a 2GB memory capacity:

Manufacturer	Type	Bus	Power (mW)	Write Speed (MB/sec)	Size (mm)
Lexar - Professional	CF#	ATA	165	20	42.8 x 36.4 x 3.3
Transcend	MMC	SPI	66	2	34 x 24 x 1.4
Sandisk – Extreme III	SD	SPI/ 4-bit	200	20	34 x 24 x 2.1

Table 9: A Comparison of Selected Flash Card Properties

Compact flash, MMC and SD cards are perhaps the best supported and amongst the most popular of available cards. MMC and SD cards have the same form factor and are around half the size of the older Compact Flash. Another difference is the bus type. Compact Flash has a standard parallel ATA interface, this is electrically the same as many (non-SATA) hard disk drives. SD cards are designed around a 4-bit bus, but will operate in serial mode using SPI; in this mode they are also compatible with MMC cards. For these reasons, SD/MMC memory was selected for the design.

5.2.3b Local Storage

There are three basic technologies available to satisfy local storage requirements: E^2PROM or EEPROM (Electrically Erasable Programmable Read-Only Memory), Flash and FRAM (Ferroelectric Random Access Memory), which is the most recent development. Devices based upon all of these are non-volatile and available with SPI interfaces. Current consumption is generally similar (around 35 mA) and is relative to the operating frequency of the SPI bus. The pros and cons are outlined in *Table 10*.

Technology	Pros	Cons
E^2PROM	Widely available	Slow access and erase times, capacity
Flash	High capacity	Slow access and erase times
FRAM	Read and write speeds	Limited selection, capacity

Table 10: A Comparison of Secondary Storage Technologies

To summarise - E^2PROM and Flash are broadly similar in performance terms, with the latter offering large storage capacities, whilst FRAM has far superior performance but lower capacities. As the 8-pin variants are pin compatible and offered in the same industry standard packages, differing only in software routines, this allows the end application to determine the type of memory to be fitted. For general-purpose applications, Ramtron's FM25L512 provides fast access times and 64k x 8 of storage. For power critical, low speed use, Atmel's 8Mbit AT26DF801 could replace the SD card as the prime data storage medium.

5.3 Description of Design Schematics

The schematic design and circuit board layout was produced using Easy-PC for Windows CAD software, supplied by Number One Systems Ltd. After creating schematic and circuit board layout symbols, and producing library files for all necessary components, the multi-sheet schematic design went quite smoothly. The full schematics may be found in Appendix A.

5.3.1 LPC2148 Microcontroller Connections

The chosen pin assignments are shown in the following tables, grouped by their board functions. The microcontroller's pin connect block must be programmed to enable these functions to ensure correct circuit operation from power up.

5.3.1a Defined Control Pins

These pins are defined for the control of specific on-board devices.

Pin Name	Pin Number	Defined Control Pins
P0.21	1	ADC End of Conversion (EOC) output
P1.16	16	Power control switch, FET Q2
P1.17	12	FRAM Chip Select (pin 1)
P1.18	8	FRAM Data Hold (pin 7)
P1.19	4	FRAM Write Protect (pin 3)

Table 11: LPC2148 Defined Control Pins

5.3.1b The SPI Memory Bus

This used by the SD flash card (*Philips Semiconductors, 2005 – AN10406*) and FRAM for all memory read and write operations.

Pin Name	Pin Number	SPI Memory Bus
P0.4/SCK0	27	Clock, connects to SD card pin 5 & FRAM pin 6
P0.5/MISO0	29	Data In, connects to SD card pin 7 & FRAM pin 2
P0.6/MOSI0	30	Data Out, connects to SD card pin 2 & FRAM pin 5
P0.7/SS0	31	Slave Select, connects to SD card Chip Select, pin 1

Table 12: The SPI Memory Bus

5.3.1c The SPI Input/Output Bus

The LPC2148's second SPI port is used by the MAX1168 ADC for data transfer, and also provides off-board expansion. This allows additional SPI devices, such as slave microcontrollers, ADCs, DACs, programmable instrumentation amplifiers and signal conditioning, to be connected and controlled by the host microcontroller. For optimum performance with the MAX1168 ADC, off-board access should be limited during high-speed data conversion.

Pin Name	Pin Number	SPI (SSP) Input/Output Bus
P0.17/SCK1	47	Clock, connects to ADC pin 4 & DIO header, pin 9
P0.18/MISO1	53	Data In, connects to ADC pin 3 & DIO header, pin 6
P0.19/MOSI1	54	Data Out, connects to ADC pin 5 & DIO header, pin 5
P0.20/SS1	55	Slave Select, connects to ADC Chip Select, pin 20

Table 13: The SPI Input/Output Bus

5.3.1d Serial Port

This connects to the MAX3227 to produce RS-232 level signals at the DIO header.

Pin Name	Pin Number	RS-232 Serial Port
P0.0/TxD0	19	UART0, serial data transmit MAX3227, pin 11
P0.1/RxD0	21	UART0, serial data receive MAX3227, pin 9

Table 14: LPC2148 Serial Port Connections

5.3.1e USB Port Implementation

The LPC2148's on-chip USB controller requires minimal external components (as shown in *Figure 22*) to implement USB 2.0 compliant data transfer at up to 12 Mb/second to a USB host.

The presence of USB power V_{USB} (+5 Volts), and therefore a USB connection, is detected via a pull-up resistor connected to the *P0.23/VBUS* terminal. Data lines *D+* and *D-* are protected by 33Ω series resistors (*Philips Semiconductors, 2005 - datasheet*), whilst a 1.5kΩ pull-up resistor connects *D+* to the SoftConnect circuit controlled by transistor Q1. SoftConnect, as perhaps its name suggests, allows connection to the USB bus under software control. Switching in the 1.5kΩ pull-up resistor identifies the device to the host as USB 2.0 compliant.

Pin Name	Pin Number	USB Port
D+	10	USB data i/o
D-	11	USB data i/o
P0.23/VBUS	58	USB power detect
P0.31/Connect	17	USB Soft Connect

Table 15: LPC2148 USB Port Connections

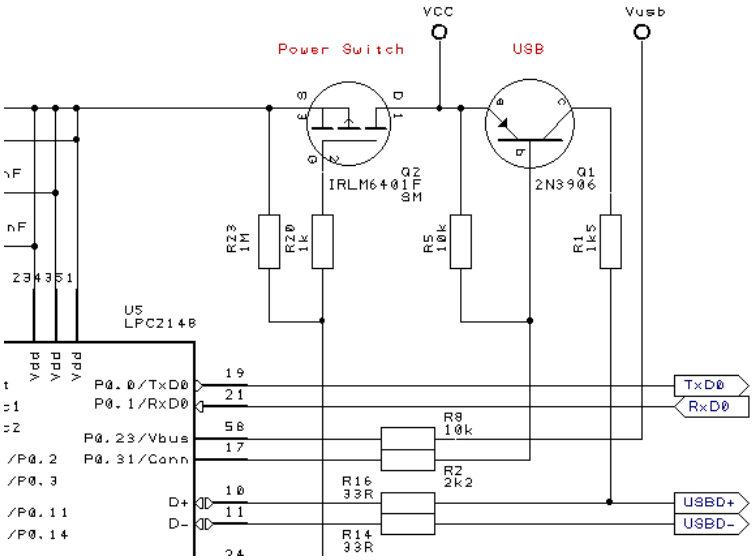

Figure 22: LPC2148 USB Port Connections

5.3.1f Digital Input/Output Expansion

The majority of the LPC2148's terminals have multiple functionality, as defined by the *Pin Connect Block*. Those pins not already assigned for system functions are available for off-board expansion. At the most basic level they can be used for general purpose input and output utilities; these range from turning on LEDs or power switches, to system event or control inputs and providing chip select outputs for SPI I/O bus expansion. Some of the pins however offer additional functions, these include:

- Two I2C serial ports - P0.2, P0.3 and P0.11, P0.14
- Two Pulse Width Modulation (PWM) outputs – P0.8, P0.9

- Two timer inputs – P0.10, P0.22
- An external interrupt input for system management – P0.16
- A second serial port with full modem interface (UART1) – P0.8 to P0.15

Pin Name	Pin Number	Digital Input/Output Header
P0.2/SCL0	22	DIO header, pin 24 I^2C port 0, SCL0 clock
P0.3/SCL0	26	DIO header, pin 25 I^2C port 0, SDA0 data
P0.11/SCL1	37	DIO header, pin 17 I^2C port 1 - SCL1 clock, UART1 CTS, GP i/o
P0.14/SDA1	41	DIO header, pin 13 I^2C port 1 - SDA1 data, UART1 DCD, GP i/o
P0.9/RxD1	34	DIO header, pin 20 general purpose i/o / UART1 receive / PWM output
P0.8/TxD1	33	DIO header, pin 21 general purpose i/o / UART1 transmit / PWM output
P0.13/DTR1	39	DIO header, pin 15 general purpose i/o / UART1 DTR
P0.12/DSR1	38	DIO header, pin 16 general purpose i/o / UART1 DSR
P0.10/RTS1	35	DIO header, pin 19 Timer input / general purpose i/o / UART1 RTS
P0.15/RI1	45	DIO header, pin 11 general purpose i/o / UART1 RI / ext interrupt input
P0.16/EINT0	46	DIO header, pin 10 external interrupt input / general purpose i/o
P0.22	2	DIO header, pin 7 general purpose i/o / timer input
P1.25	28	DIO header, pin 22 general purpose i/o / external trigger input
P1.20	48	DIO header, pin 8 general purpose i/o
P1.21	44	DIO header, pin 12 general purpose i/o
P1.22	40	DIO header, pin 14 general purpose i/o
P1.23	36	DIO header, pin 18 general purpose i/o
P1.24	32	DIO header, pin 23 general purpose i/o

Table 16: LPC2148 Digital Input/Output Connections

The terminals in the preceding table are connected to the digital input/output header (DIO) as shown in *Figure 23*.

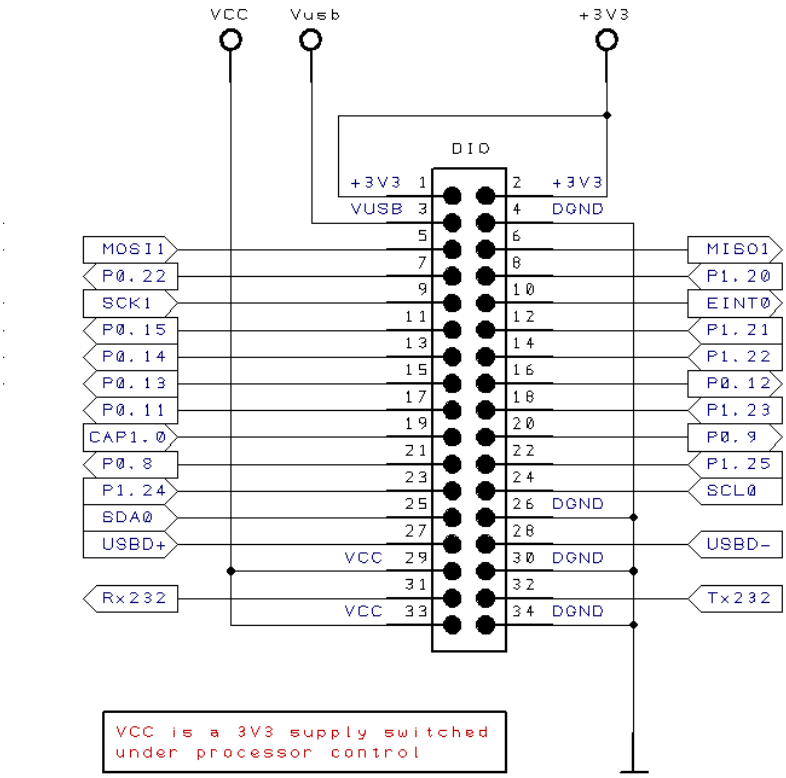

Figure 23: Digital Interface Header

5.3.1g JTAG System Debugging

JTAG (*Texas Instruments, 1997*) provides an in-circuit debugging capability. The microcontroller's JTAG pins connect to an industry-standard test header as shown in *Figure 24*. The header is compatible with a number of popular interface adapters, such as *CrossConnect for ARM* from Rowley Associates and the *Wiggler*, originally developed by Macraigor Systems, but widely available from other manufacturers. Both adapters allow JTAG interfacing to either a PC's parallel or USB port for software development and debugging. These devices, together with ARM software development tools, are available within the School.

Like most other LPC2148 pins, the JTAG connections also have alternative functions. Thus the JTAG header may also be used for digital expansion if not required for system debugging.

Pin Name	Pin Number	JTAG System Debugging Header
P1.31/TRST	20	JTAG header, pin 3 JTAG Test Reset input
P1.28/TDI	60	JTAG header, pin 5 JTAG Test Data input
P1.30/TMS	52	JTAG header, pin 7 JTAG Test Mode Select input
P1.29/TCK	56	JTAG header, pin 9 JTAG Test Clock input
P1.26/RTCK	24	JTAG header, pin 11 JTAG Returned Clock Test output
P1.27/TDO	64	JTAG header, pin 13 JTAG Test Data output

Table 17: The LPC2148 JTAG Port

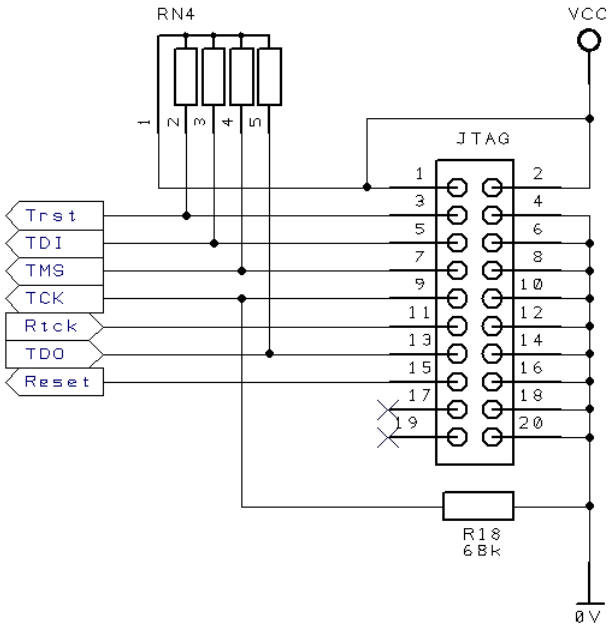

Figure 24: JTAG Header Connections

5.3.1h On-Chip Analogue Input/Output

The microcontroller has a number of 10-bit ADC input terminals; four of these connect to the Analogue Input/Output header (*ANA1*) as shown in *Figure 26* and described in section 5.3.3. The LPC2148 has a separate analogue supply input (VDD_A) and analogue ground (VSS_A); these power the on-chip ADC and DAC. In an effort to provide noise immunity, the analogue supply connects to the circuit's 3.3 Volt supply via a series inductor (*L1*), whilst bypass (*C18*) and decoupling (*C20*) capacitors connect to analogue ground. The ADC voltage input range set by a 2.5 Volt bandgap voltage reference *(ZD1*) which connects to the *VREF* terminal.

Pin Name	Pin Number	Analogue Input/Output
P0.28/AD01	13	ANA1 header, pin 3 ADC input 1 / timer input / general purpose i/o
P0.29/AD02	14	ANA1 header, pin 4 ADC input 2 / timer input / general purpose i/o
P0.30/AD03	15	ANA1 header, pin 5 ADC input 3 / timer input / general purpose i/o
P0.25/AD04	9	ANA1 header, pin 6 ADC input 4 / DAC output / general purpose i/o
VREF	63	ADC voltage reference
VDD_A	7	+3.3 Volt analogue supply
VSS_A	59	Analogue Ground

Table 18: LPC2148 Analogue Input/Output Connections

5.3.1i Miscellaneous Functions

The LPC2148 has a number of fixed function terminals; these are shown in the *Tables 18 and 19*. The *Reset* pin, as its name suggests, is used to reset the processor, and connects to both the JTAG header, for in-system debugging and programming, and a MAX821 watchdog chip, which invokes a system reset if the voltage level falls below preset thresholds. A 12 MHz crystal oscillator connected to *XTAL1* and *XTAL2* provides

the input for the system clock. The onboard real-time clock, which is not used on this design, accounts for the remaining terminals *RTXC1*, *RTXC2* (32 kHz oscillator inputs) and *VBAT* (the clock battery back up voltage input).

Pin Name	Pin Number	Miscellaneous Functions
Reset	57	MAX871 watchdog + JTAG header, pin 9
XTAL1	62	Oscillator in
XTAL2	61	Oscillator out
VCC	23, 43, 51	+3.3 Volt supply
VSS	6, 18, 25, 42, 50	Digital Ground
RTXC1	3	Not used
RTXC2	5	Not used
VBAT	49	Not used

Table 19: Miscellaneous LPC2148 Terminals

5.3.2 MAX1168 ADC Connections

The ADC connections are shown in *Figure 25*. The digital interface is powered by the system 3.3V supply; a decoupling or bypass capacitor (C12) between *DVdd* and digital ground should help reduce circuit noise. *DSPR* is pulled-up to the digital supply (R15) to enable SPI operation. *DSEL*, the data bit transfer input, is connected to digital ground to select 8-bit wide data transfer. The four-wire serial bus connects to SPI1, the SSP bus, while the end of conversion output *EOC* connects to processor terminal *P0.21*, providing the necessary ADC timing information.

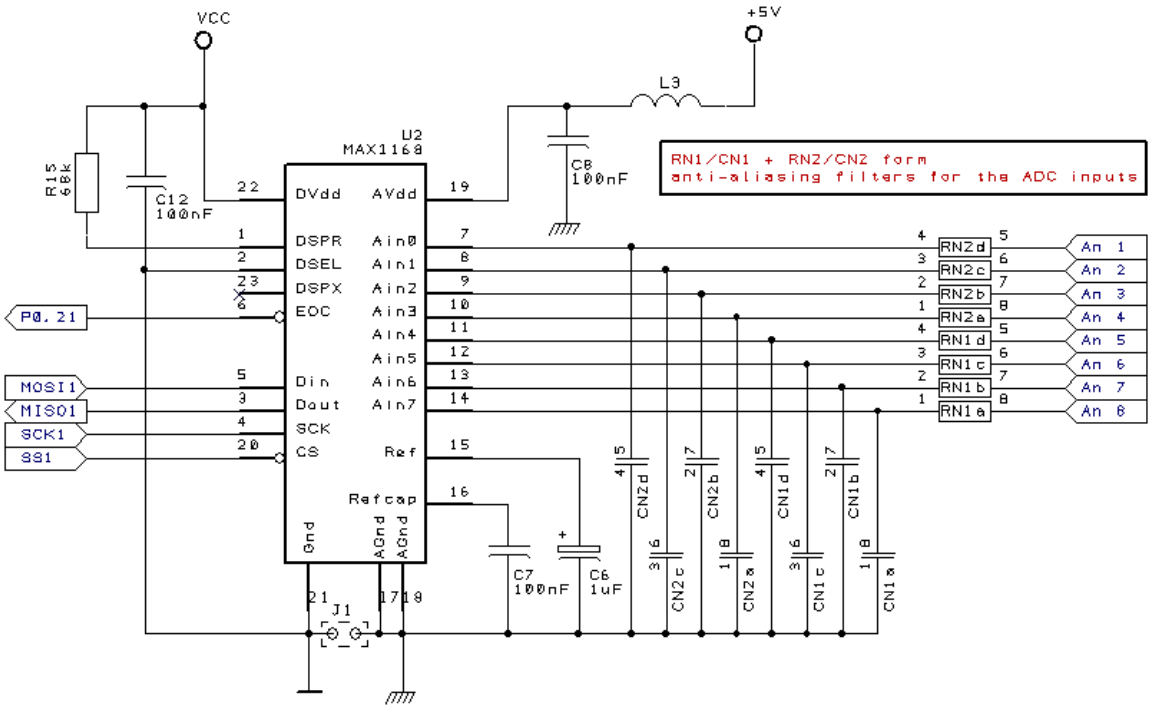

Figure 25: MAX1168 ADC Connections

On the analogue side of the device, the analogue supply terminal *AVdd* connects to +5V via a small series inductor (L3) which should help remove any high-frequency noise. A power supply decoupling capacitor (C8) connects to analogue ground, and should be placed close to the power terminal. As the chip's internal reference is used, the *Ref* and *Refcap* terminals are bypassed to analogue ground (via capacitors C6 and C7 respectively) as suggested on the device datasheet.

Each ADC input, *Ain0* to *Ain7*, is provided with a simple low-pass RC (resistor-capacitor) anti-aliasing filter (RN1/CN1 and RN2/CN2). These filters limit the bandwidth of the input signals to satisfy the demands of the Sampling Theorem (*National Semiconductor, 1980*). The filter roll-off is very gentle; the frequency of the 3db point may be calculated using the following formula:

$$f = 1 / 2\Pi RC$$

With a capacitor value of 33nF and resistance of 1kΩ, the 3db point of the anti-aliasing filter is:

$$f = 1 / 2\Pi \times 1000 \times (33 \times 10^{-9)}$$

$$f = 4.83 \text{ kHz}$$

As the MAX1168 has an input range of 0 – 4.096V, the analogue inputs would require scaling to accept a 0 – 5V signal. This would require the addition of appropriate scaling resistors to form potential divider circuits on each input; these attenuators would then feed simple non-inverting unity gain op-amp buffers. The op-amps also offer extra input protection and provide low impedance outputs (set by output resistors) to the ADC. This circuitry would be added to a second board (see the signal conditioning block shown in *Figure 18*).

5.3.3 Analogue Interface Connections

All analogue input signals connect to the board via a 20-pin header (*ANA1*), shown in *Figure 26*. This accommodates the eight inputs to the MAX1168 ADC (*An1 to An8*), the +5 Volt supply and analogue ground, plus four inputs (*AD01 to AD04*) to the microcontroller's own onboard ADC. The latter features the same low-pass RC anti-aliasing filters (RN3/CN3) as the MAX1168 ADC inputs. Terminal *AD04* may be configured as a DAC output for control applications. The addition of the LPC2148's on-chip ADC inputs provides the board with a total of twelve analogue input channels, eight 16-bit and four 10-bit; if *AD04* is used in DAC mode, 11 analogue inputs and one output are available.

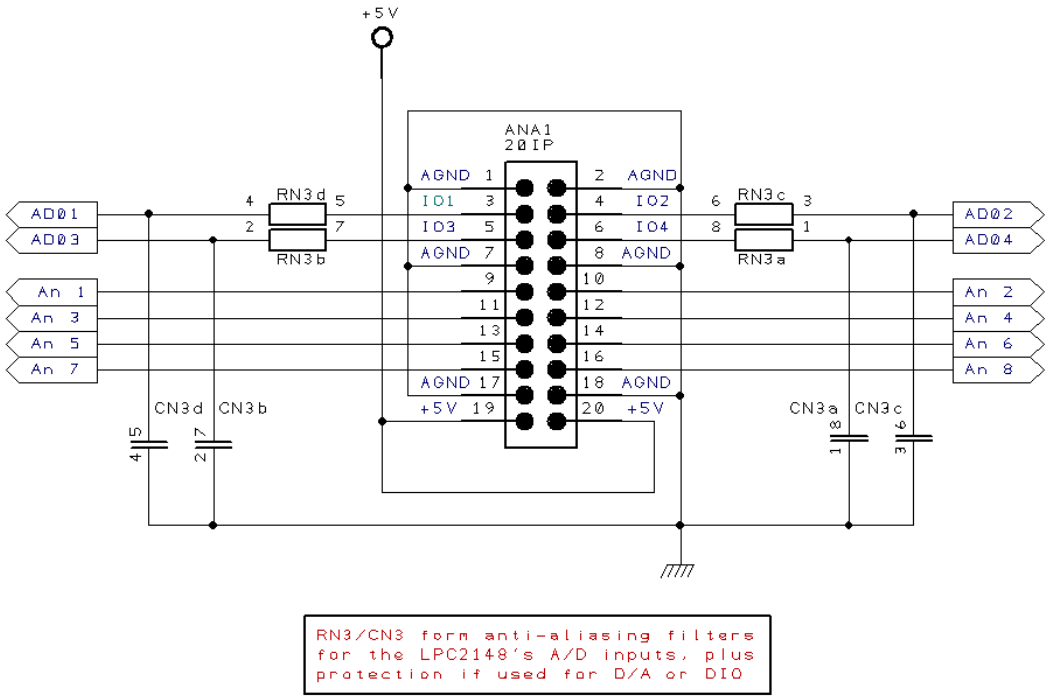

Figure 26: Analogue Interface Header

5.3.4 Memory Connections

Both the SD flash card and the FM25L512 FRAM chip, shown in *Figure 27*, connect to the processor via the SPI serial bus, and are powered from the same 3.3 Volt system supply (VCC). The flash card has a decoupling capacitor (*C4*) and a bypass capacitor (*C2*) across the power rails. The bypass capacitor is a 10µF tantalum device, which, like the 100nF decoupler, will help reduce power supply noise, but also acts as a reservoir to smooth out momentary power surges as the flash card becomes active. The two RSV terminals, which are used in the SD card's four-bit operating mode, are pulled high through the 1MΩ resistors *R3* and *R11*. Two further pull-ups (*R4* and *R9*) hold the *DO - MISO* and *CS/SS0* (Chip Select) lines high to enable the SD card to start correctly on boot-up.

The FM25L512 has its own decoupling capacitor (C15) connected across the power rails. The chip's write protect terminal, *WP,* is connected to processor pin *P1.19*, and is normally held high, in its protected state, by pull-up resistor R17. The *Hold* and *CS* (Chip Select) pins connect to *P1.18* and *P1.17* respectively on the processor. With CS/P1.17 held high by the processor, the FM25L512 automatically enters a standby mode which reduces the current demand to around 20 µA.

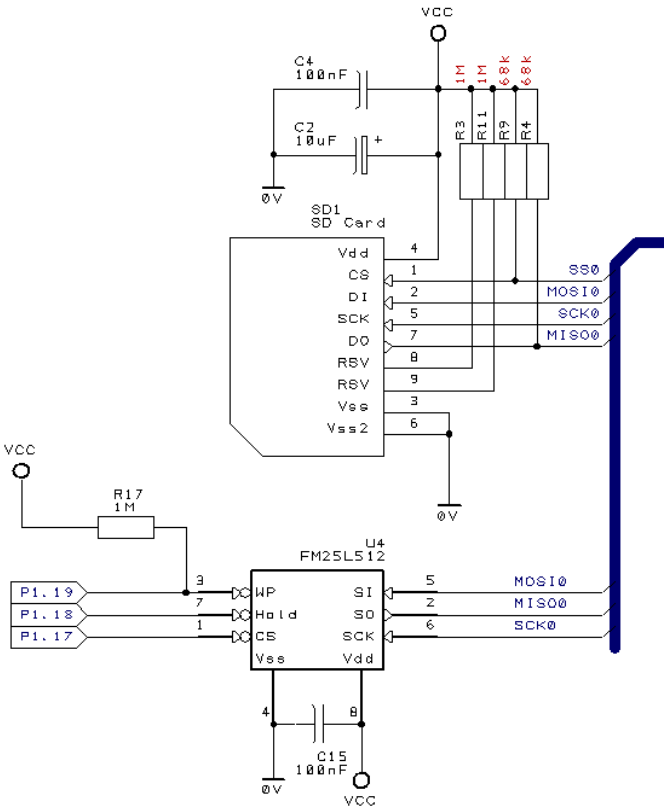

Figure 27: SD Card and FM25L512 FRAM Connections

5.3.5 RS-232 Driver

The MAX3227 line driver (*Maxim, 2005*) derives the voltages required for RS-232 compliant communication from the system 3.3V supply (*VCC*). The device's on-chip voltage converter produces a ±5.5 Volt regulated output from a dual charge pump

circuit, one acting as a voltage doubler, the other as a voltage inverter. *Figure 28* shows the four 100nF capacitors, (*C5*, *C9, C10* and *C14*) form the charge pump whilst a fifth (*C11*) is used for power supply decoupling.

The LPC2148's UART0 terminals, the transmit output *TxD0* and receive input *RxD0*, connect to pins 11 and 9 respectively on the 'digital voltage' side of the MAX3227's RS232 transceiver. The *Rx232* input and *Tx232* output connect to the chip's RS-232 side, providing RS-232 level signals to the digital input/output header, *DIO*. The MAX3227 is specified for use over the full range of common serial data rates and is capable of high-speed operation up to 1Megabaud.

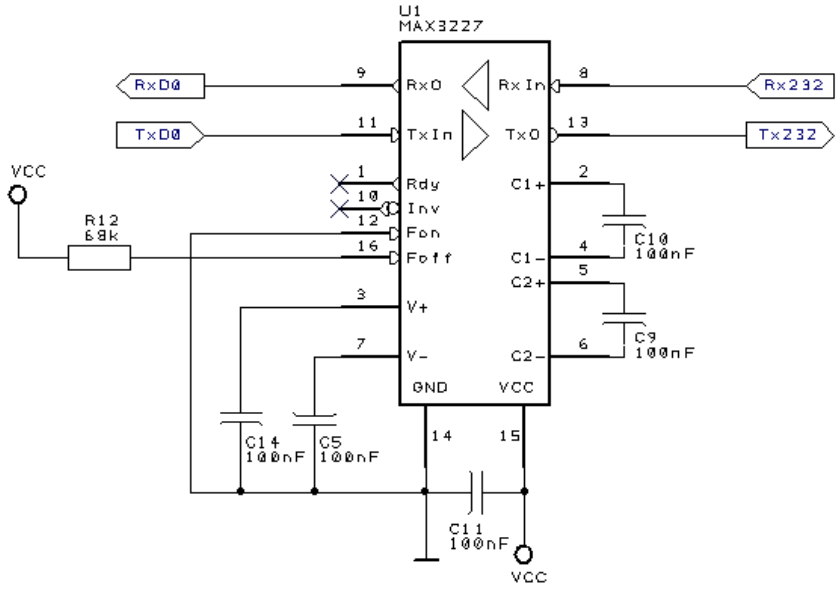

Figure 28: MAX3227 RS-232 Driver Connections

A useful feature of the chip is its Auto-Shutdown Plus Mode which can reduce current consumption to around 1µA. This enabled by the pull-up resistor (R12) holding *ForceOff* (pin 16) high and connecting *ForceOn* (pin 12) to digital ground. Auto-shutdown becomes active if the serial port is dormant for more than thirty seconds. This

disables the MAX3227's charge pumps and sets the transmit output to a high-impedance state

5.3.6 Power Management

All circuits, with the exception of the analogue side of the MAX1168 ADC, operate solely from a 3.3 Volt supply. The LPC2148 processor connects directly to this supply, while the other devices connect to *VCC,* a switched 3.3 Volt supply controlled by the PMOS FET, *Q2* (see *Figure 22*). Resistor R23 pulls the FET's gate high, holding *VCC* off until LPC2148 terminal *P1.16,* which controls the FET's gate, is held at a low logic level, turning *VCC* on. With this arrangement, the microcontroller is able to control system power - switching on *VCC* at power up, or upon waking up from shutdown.

The general-purpose I/O pins described in *section 5.3.1f* may be used to control off-board voltage regulators. This would allow the analogue 5V supply and sensor excitation voltages to be shutdown when not required.

5.3.6a System Clock Control

Power consumption of the LPC2148 is a function of the Phase locked Loop (PLL) derived system clock frequency. This is software selectable (*NXP, 2005*), and may be set using the following formulas:

$$C_{CLK} = M \times F_{OSC} = F_{CCO}/2P$$

$$F_{CCO} = F_{OSC} \times 2 \times M \times P$$

Where C_{CLK} is the system clock frequency, F_{OSC} is the crystal oscillator frequency and F_{CCO} is the frequency of the PLL current controlled oscillator. Two registers control the values of M (1 to 32) and P (1, 2, 4 or 8), the PLL multiplier and divider

respectively. The register values must be set to keep F_{CCO} in the range 156 – 320 MHz and C_{CLK} between 10 and 60 MHz. With a 12 MHz oscillator, this gives system clock frequencies (C_{CLK}) of 12, 24, 36, 48 and 60 MHz. Operating at lower clock frequencies reduces power demand, but reduces system performance; thus, a balance between these factors must be found to suit the PDL's operational requirements.

5.3.6b Microcontroller Power Saving Modes

The LPC2148 has a number of power saving modes allowing redundant on-chip peripherals to either be disabled or operate in lower power modes. For example, the 48 MHz PLL-derived USB clock may be disabled unless a USB connection is present, and the SPI bus frequencies reduced if the PDL is required to record at slow sample rates (e.g. an aggregate of less than 200 samples per second).

Ultimately, the chip can enter a power-down or sleep mode, reducing current consumption to around 50 μA. On entering power down, which is controlled (in software) by the Power Control Register, the system clock and peripherals are shut down. The contents of the local RAM and registers are preserved ready for use on wake up.

The presence of a USB connection or a signal on *P0.16/EINT0*, an external interrupt pin, can reawaken the microcontroller from power-down. The source of the interrupt signal could be a simple push-button switch, the alarm output from a real time clock chip or a combination of these and other inputs.

5.4 Circuit Board Layout and Assembly

Having produced the schematic design, the Easy-PC for Windows CAD software was used to layout and manually route the circuit board. An important feature of the

software was that design integrity between the schematic and circuit board layout was maintained by a common netlist (or database). Design rule checking (DRC) against specified tolerances identified clearance issues and tracking errors.

The majority of the components used are surface mount devices (SMD). This is partly due to limited choice as many semiconductor manufacturers only offer chips in these packages. However, the majority of components used are SMDs, even when conventional alternatives are readily available. As SMDs are relatively small, and have minimal mass, they are less prone to damage due to high shock or vibration levels than most conventional components. The use of surface mount technologies greatly improves the ruggedness of the design.

5.4.1 Component Placement

Size was an important consideration in this design, which thus necessitated the use of surface mount components. These offer a small footprint and may be mounted on either or both sides of the board, effectively doubling the potential board density.

Components were arranged and placed on both sides of the board. Two major factors determined placement: (1) the separation of analogue and digital components to reduce signal noise, and (2) the minimisation of track lengths. The final layout is shown in *Figures 29 and 30*. The disproportionate size of the passive components (i.e. the resistors and capacitors), and connectors, compared to that of the semiconductor devices, is quite apparent. In the case of the passive components, which are mostly of a 0805 case size (2.0 x 1.25mm), this is due to the restrictions placed upon component size by manual assembly; in volume production, these could be significantly smaller.

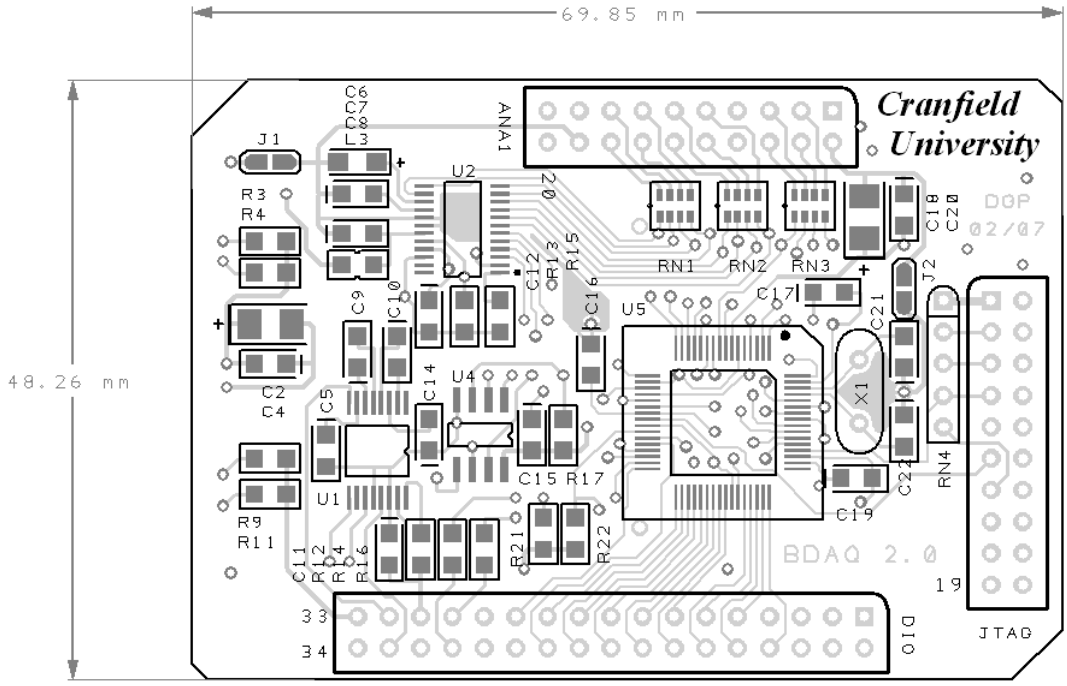

Figure 29: Circuit Board Artwork Top View

In keeping with best practice, the decoupling capacitors for each chip were placed close to voltage terminals to provide localised power filtering. The LPC2148 microcontroller (*U5*) was positioned centrally to facilitate connection fan out to the rest of the circuit. The 12 MHz crystal oscillator, *X1*, was placed close to the microcontroller's oscillator input terminals together with the oscillator's capacitors (*C21* and *C 22*).

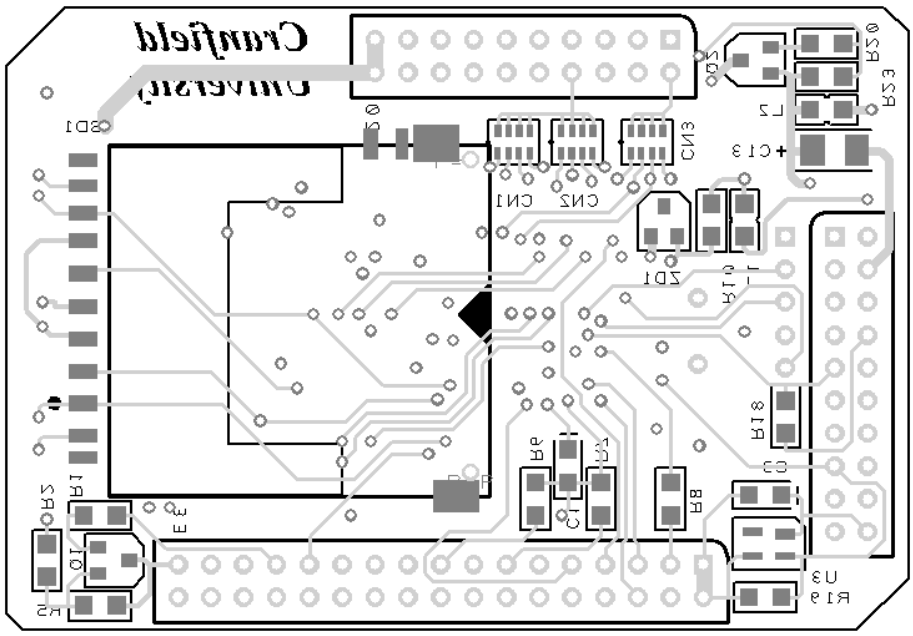

Figure 30: Circuit Board Artwork Bottom View (shown mirrored)

5.4.2 Circuit Board Layout

After starting to route the interconnections, it soon became clear that the top and bottom copper layers would not be sufficient to complete the design without increasing board size. To address this problem it was decided to opt for a four-layer circuit design. The two new internal layers were used for analogue and digital ground and power planes (plus a few signal lines). As the planes offer a very low resistance path for the power rails, reducing ground loops, and provide screening for the two outer signal layers, this should result in lower circuit noise.

Noise sensitive tracks, such as analogue signal inputs and ADC voltage references, were kept away from high-speed digital signals (e.g. busses and clocks) to further reduce induced circuit noise; and where possible, routed on a different electrical layer.

In an effort to minimise board problems due to manufacturing processes, the software's design rules were set to maintain relatively generous clearances. The design's minimum track thickness and clearance of 0.2 mm may be compared favourably to the 0.15 mm quoted by many circuit board manufacturers (*Beta Layout, 2004*). Via holes, used to connect between electrical layers, were also optimised with this in mind and were kept to a minimum wherever possible. To ensure good connectivity, surface mount component pads were made slightly larger than industry standards as an aid to hand soldering.

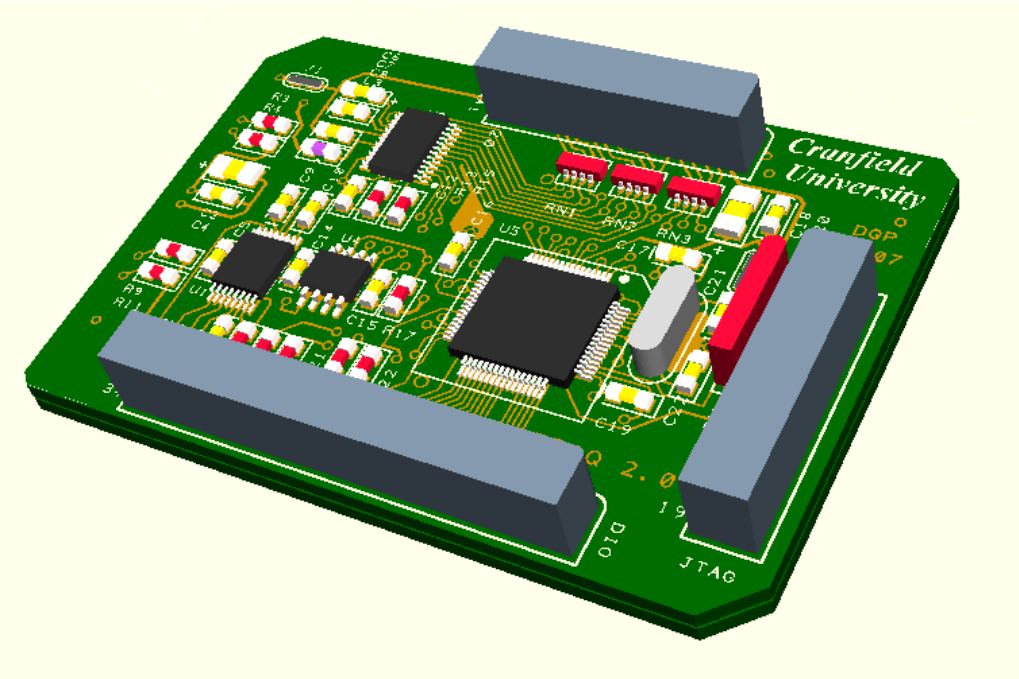

Figure 31: 3D CAD Circuit Board Image

5.4.3 Circuit Board Assembly

The circuit was carefully hand-assembled using tweezers, side cutters, long-nosed pliers, solder braid, low melting point solder (Smartwire), a head-mounted magnifier (Optivisor) and a conventional soldering iron.

First a corner pad of the LPC2148 layout shape was tinned. With the chip carefully positioned, the pad reflowed to secure one corner. After reflowing the joint a second time to ensure correct alignment between the chip's other terminals and the solder pads, the pin diagonally opposite was soldered down to anchor the device flat to the board. With a pin pitch of 0.5 mm, it would prove almost impossible to individually solder all the LPC2148's 64 pin without bridging (and therefore short-circuiting) a few pins. Instead, the well-tinned soldering iron was dragged along each side of the chip to produce continuous solder fillets. Excess solder was then removed with solder wick to leave perfect solder joints. A similar process was used to mount the MAX1168, MAX3227, and the surface mount resistor and capacitor networks, which also have small pin pitches.

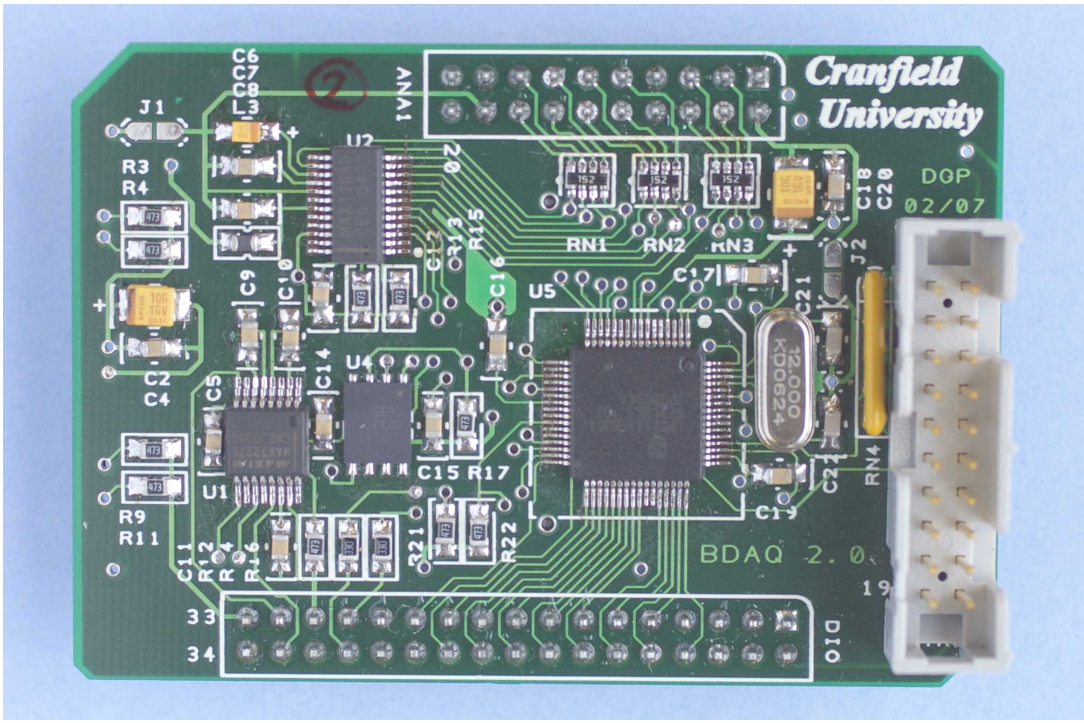

Figure 32: Assembled Circuit Board – Top Side

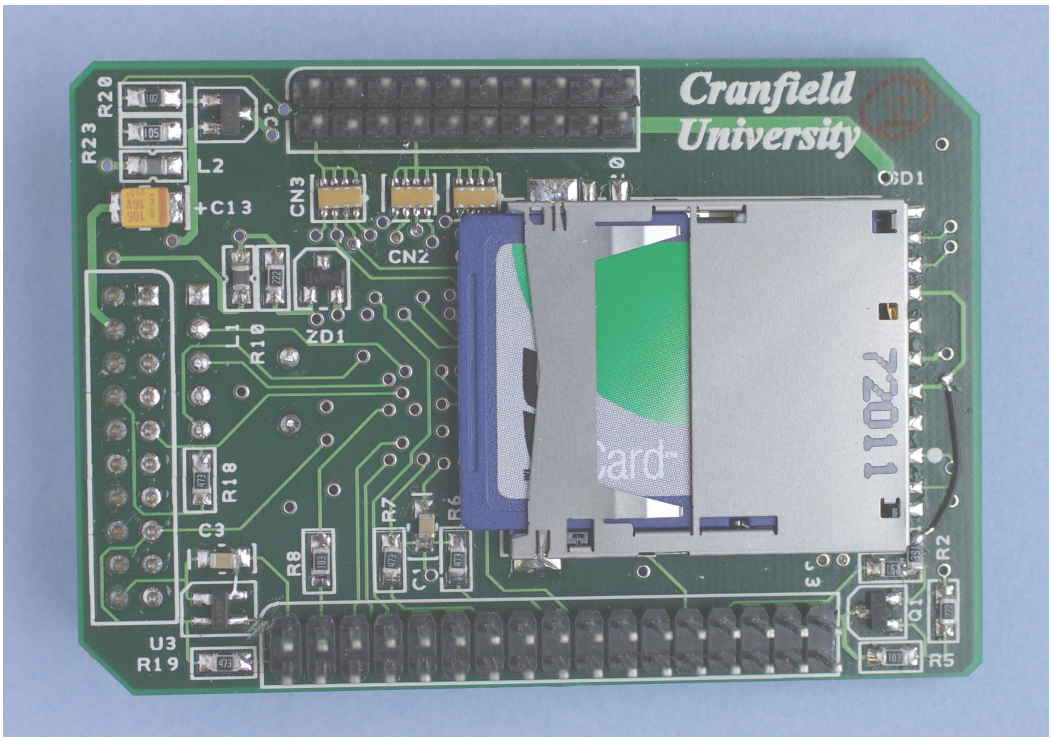

Figure 33: Assembled Circuit Board – Bottom Side with SD Card Inserted

The pin spacing of the remaining surface mount components was large enough to permit the terminals to be soldered individually. Again, one pad on each component was tinned, and, with the component in position, reflowed. Where necessary, the joint was again reflowed to ensure optimal pin alignment and component flatness. The remaining terminals were then soldered. To simplify initial testing, the power control FET, *Q2*, was omitted at this stage, and the drain and source connections shorted together.

The plated through hole components were the last to be fitted, in order of height. Each component was held flat to the board while (with the exception of the two-pin crystal) the corner pins were soldered. The rest of the pins were soldered and the leads clipped short.

Chapter 6 - System Testing

In order to test the PDL board, the test rig shown in *Figure 34* was designed and assembled. This provided circuit power, connections to a PC's USB and serial ports, and analogue inputs. After visual inspection using an Optivisor and carefully checking for continuity and short circuits on the board's power supply rails, the PDL was plugged into the test rig to commence testing.

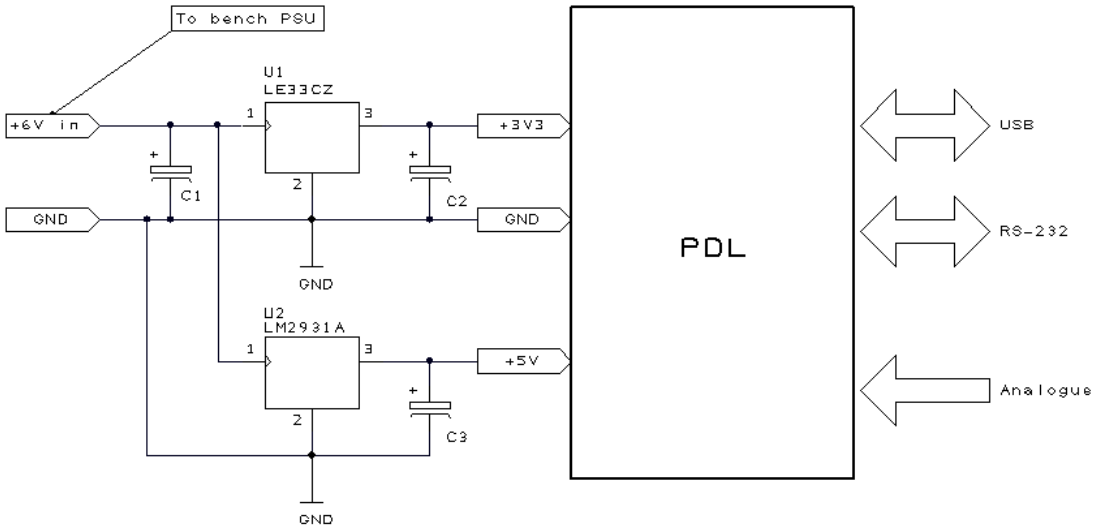

Figure 34: PDL Circuit Board Test Rig

6.1 Board Tests

With the bench power supply (PSU) set to 6V and a current limit of 200mA, power was applied to the circuit. Initially no apparent problems were observed, so a JTAG debugger was connected to the JTAG header and the power cycled. The board failed to communicate with the test PC and after monitoring the state of the JTAG bus with an oscilloscope; it was found that the Reset terminal could not be pulled low to assert a system reset. The fault was traced to a design error caused by transposed pin assignments when the MAX821 watchdog chip was added to the CAD library. The

offending tracks on the PCB were cut and corrections made using a short length of wire. This proved to be successful.

With the modification to the Reset line, the JTAG was able to connect to the PDL but communication proved to be unreliable. Closer examination of the PDL's JTAG connections, and reference to *Section 22.5* of NXP's LPC214x User Manual (*NXP, 2005*), established that the *P1.26/RTCK* pin required a pull-down resistor. A 10kΩ 0805 resistor was added between pins 11 (*RTCK*) and 12 (*VSS/GND*) on the back of the JTAG port. Following this change, the JTAG port operated correctly.

A number of test programs produced and provided by Paul Knight were used to assess system performance. These results of these tests are discussed in the following sections.

6.1.1 Processor Power Consumption and Performance

A basic monitor program was downloaded to the PDL board via the JTAG link. This allowed the system clock frequency to be changed, as discussed in *Section 5.3.6a,* to determine the board's current consumption. In addition, code was included to run the *Sieve of Eratosthenes* benchmark; an algorithm for finding prime numbers used to check processor or code performance (*Keil, 2007*).

The results in *Table 20* show the trade-off between power and performance. The tests were performed without an SD Card and with the SPI clocks disabled in software. As the power control FET was effectively always on (see the end of *Section 5.4.3*), all other devices were powered. As the PDL board's RS-232 port was fully functional, this was used to control the tests via a serial terminal program running on a PC, and the JTAG adapter was disconnected. The supply current quoted is that measured at the bench PSU.

Regarding the supply current, this reduced by 5mA when the MAX3227 entered auto-shutdown after 30 seconds of inactivity. It was determined that the regulators on the test rig were responsible for another 2mA. The actual current drawn by the PDL board at 60MHz operation, with the MAX3227 shutdown, was therefore approximately 58mA. Enabling the SPI clocks increased demand to around 85mA at 60MHz.

System Clock (MHz)	Supply Current	Sieve Test (seconds)
12	25	0.0728
24	35	0.0364
36	45	0.0242
48	55	0.0182
60	65	0.0145

Table 20: PDL Board - Power v. Performance Tests

An interesting comparison may be made with the *Sieve* benchmarks of other board/processor combinations. This standard performance data was collected by Paul Knight over a period of time from various devices used in Cranfield University projects. Some examples are shown in *Table 21*.

Board/Processor	System Clock (MHz)	Complier	Time per Loop (seconds)
Phycore/ Philips 80591	12	Keil v4.0	0.306
Atmel AVR Mega103	4	GCC 2.95	0.1
Taskit 386	25	Borland 16 bit	0.0479
DSP Design/ Elan 486	66	Borland 16bit	0.0435
EB01/ ARM7 TDMI	32	GCC3.0 Thumb Mode	0.0206
PDL/ LPC2148	60	GCC 4.1 Thumb Mode	0.0145
Home Celeron PC	800	Borland 16bit	0.0018

Table 21: PDL Board - Performance Comparison

The PDL board's performance on this benchmark compares favourably with the other combinations, particularly considering it has much lower current consumption than some of its closest competitors. The Elan 486 board for example, which is based around the AMD SC400 486-class processor, has a third of the performance yet takes more than five times the power.

6.1.2 Flash Card Performance

The PDL board's ability to log data at high speed is largely determined by the time taken to write data to the SD card. Memory test software developed for another ARM processor (Atmel's SAM7x), was modified to run on the PDL board. After confirming that the SPI memory bus was working, performance tests were conducted on some example SD cards with the bus running at 7.5 MHz.

Card Type	Test Figures (kb/sec)		Claimed (kb/sec)	
	Write	Read	Write	Read
Kingston 256MB (*33x*)	105	415	1,500	5,000
Kingston 2GB (Mini SD)	200	716	-	7,500
Sandisk 256MB (*66x*)	273	573	-	10,000
Lexar 64MB (Mini SD) (*66x*)	501	603	-	10,000

Table 22: PDL Board – SD Card Performance Tests

The test results show a wide spread in performance, demonstrating the difference between read and write speeds. The published performance figures appear to be based upon four-bit bus operation. Data published by Sandisk (*Sandisk, 2003*) shows times of 163.8µs and 41.0µs for SPI and four-bit mode respectively, to transfer 512 bytes of data with a 25MHz bus for their standard (66x) card. Thus, four-bit mode is four times faster than SPI. Taking this into account together with the difference in bus speed – 7.5 MHz in the performance tests compared with 25 MHz for published figures – the system's

SPI bus performance is 13.33 times *([12.5/3.125] x [25/7.5])* slower than the optimum. Multiplying the measured speeds by this factor gives figures much closer to those published by the manufacturers.

Card performance is normally specified as multiples of 150 kbps, e.g. 66x cards have a notional performance of 66 x 150kbps or 9.90 Mbps. It should be noted that these figures are typical rates and do not indicate whether read or write speeds (which are typically lower) are being quoted. Faster cards, such as 133x (19.95 Mbps) and 150x (22.5 Mbps), offer improved system performance potential (> 1Mbps using SPI running at 7.5 MHz); this is ultimately limited by a combination of card and SPI bus speed.

6.1.3 USB Port Performance

The JTAG port was used to download software to test the USB port (*Sourceforge, 2006*), courtesy of Paul Knight. After successfully testing USB operation, some benchmark tests were performed to study the effect of data block size on USB throughput. Data blocks read from the LPC2148's buffer were stored to disc on the host PC, and the transfer rate measured.

Block Size (bytes)	**Transfer Speed (KBytes/sec)**
512	255
1024	340
2048	511
3072	613
4096	680

Table 23: PDL Board – USB Port Performance Tests

The test results (see *Table 23*) show that transfer speed increases with data block size. Each time a data block is read, the host device must request the next block to sent

and receive an acknowledgement in return. This 'handshaking', together with cyclic redundancy check (CRC) error correction, adds a quite an overhead to data block transfer. Increasing the block size improves the data block-to-overhead ratio, improving transfer times.

6.1.4 ADC Performance

Some basic performance tests were carried out using modified code originally developed for the LPC2294 ARM processor used in Cranfield Health's Vapour Guard system. With the SPI I/O bus running at 4MHz, and a single conversion requiring a single-byte write and two-byte read (24-bits in total), the maximum performance of the MAX1168 was measured at 166ksps (k samples per second), compared to the stated maximum of 200ksps.

This only tells half the story, as the sampled data must stored on a SD card if it is operate as a data logger. Here, the write time for the SD card is the controlling influence on logging performance. Tests with a Sandisk 256MB card (with a write speed of 273 kb/second) gave a reliable logging performance of 30ksps.

Test signals, from both a DC source and a function generator, appeared quiet, with only two to three bits of noise, despite a lack of screening.

6.2 Conclusions and Further Work

The aim of the project, though challenging was achieved. A system capable of operating as the core of a Personal Data Logger, was designed, built and tested in the laboratory. The small board size combined with a low-power high performance ARM

processor, SD card for mass data storage, high-speed 16-bit analogue data converter, USB and RS-232 ports, and provision for further expansion, provides a potent package.

The test results demonstrate that the design certainly has the potential to fulfil its intended role as the heart of a portable pocket-sized personal data logger. The wide range of sampling rates and virtual programmable analogue gain, encompassing many types of sensors, offers a flexible platform for the measurement of various parameters for dynamic health or athletic performance monitoring.

There are two design errors to correct (the pin connections to the MAX821 and the addition of a pull-down resistor on the JTAG port), and further checks to fully test the analogue performance criteria. With such a large number of system variables to consider, comprehensive testing or modelling would be required to establish power consumption for all operating modes.

In addition, the design of the second PDL board to must be considered; this would feature analogue signal conditioning, a real-time clock circuit, power supplies and all external system I/O connections. Once completed, there is the not insignificant task of developing the embedded software that turns an otherwise inert circuit board into a functioning data logging system.

A proposed design combining a real-time clock and trigger circuitry is shown in *Figure 35*. Both the clock chip and the three-input AND gate are powered from the same voltage source; this may be either +5V, if available, or a backup battery to maintain supply. The clock chip provides timing data via an I2C interface to the PDL core.

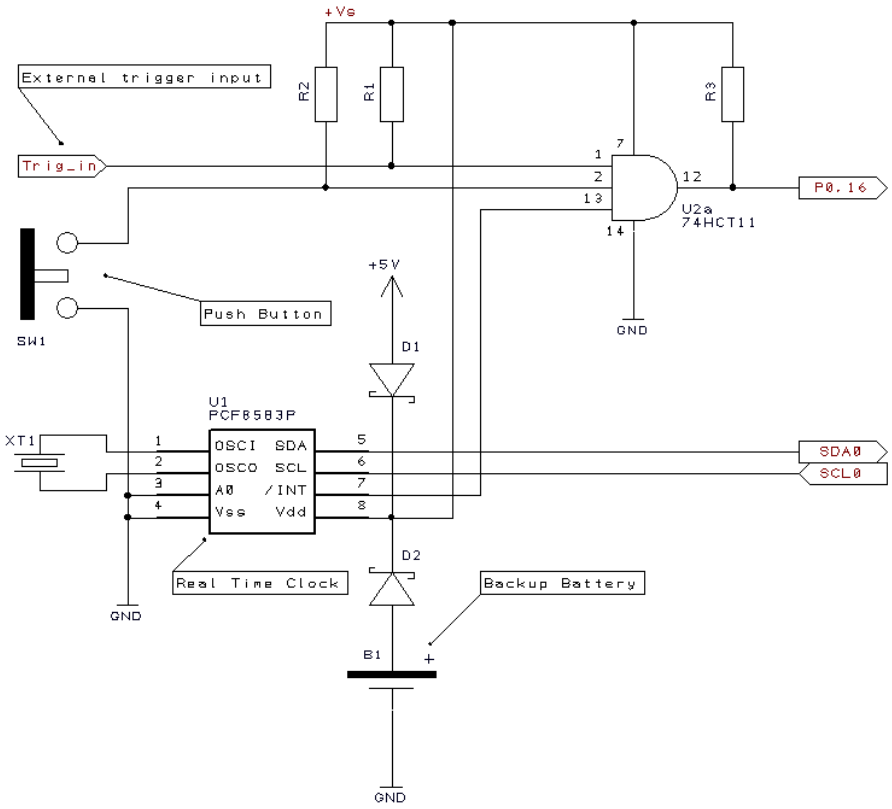

Figure 35: Proposed Real-Time Clock and Trigger Circuit

The three-input AND gate connects to the PDL core's External Interrupt pin (*P0.16/Eint0*), and is held high by resistor *R3*. If any of the gate's normally high inputs, push button *SW1*, external trigger input or the clock's alarm output, go low, this flips the output, waking up the LPC2148.

Following the discussion in *Section 4.3.1*, although linear regulators are the best low-noise option, SEPIC regulators are worthy of further study. Their ability to operate at voltages below their output level allows increased efficiency as more energy may be extracted from a battery pack; it also gives the option of using fewer batteries. With a high switching frequency (e.g. >1MHz), the noise generated may prove easier to filter, or, being several orders of magnitude above the maximum sampling frequency, may

have little effect on analogue signals. Comparative performance tests with a linear regulator would be necessary to establish the amount of noise present.

For all their added complication, lithium secondary cells, with their small size and high energy density have a lot to offer. Lithium polymer (Li-poly) cells are preferred to lithium-ion as they are more robust, but still capable of delivering ample supply current (*see section 4.1.2b*). The high volumetric and gravimetric efficiency and range of packaging options would allow either single (with a SEPIC regulator) or dual cell operation, whilst keeping overall system size to a minimum.

Choosing Li-poly cells would necessitate the development of battery charger and battery management circuits for optimum performance. For field use, it would be desirable to combine the Li-poly cells, charger and management circuitry into a removable pack – these could then be charged remotely if necessary and exchanged as required. The charger should have a wide voltage input range to facilitate recharging.

A combination of low-noise SEPIC regulators and Li-poly battery packs (including battery management and charger circuitry as discussed), could provide the best all-round solution. Although the mechanical aspects of the design would need careful attention, building the cells and circuitry into a removable pack eliminates the main drawbacks of running from fixed integral batteries.

Ideally some of these points would have been addressed and investigated as part of this project. Unfortunately, time constraints prevented this work from being undertaken in time for the completion of this thesis. However, development of the technologies described in this project, including research on SEPIC regulators and lithium batteries, continues as part of various Cranfield Health research projects.

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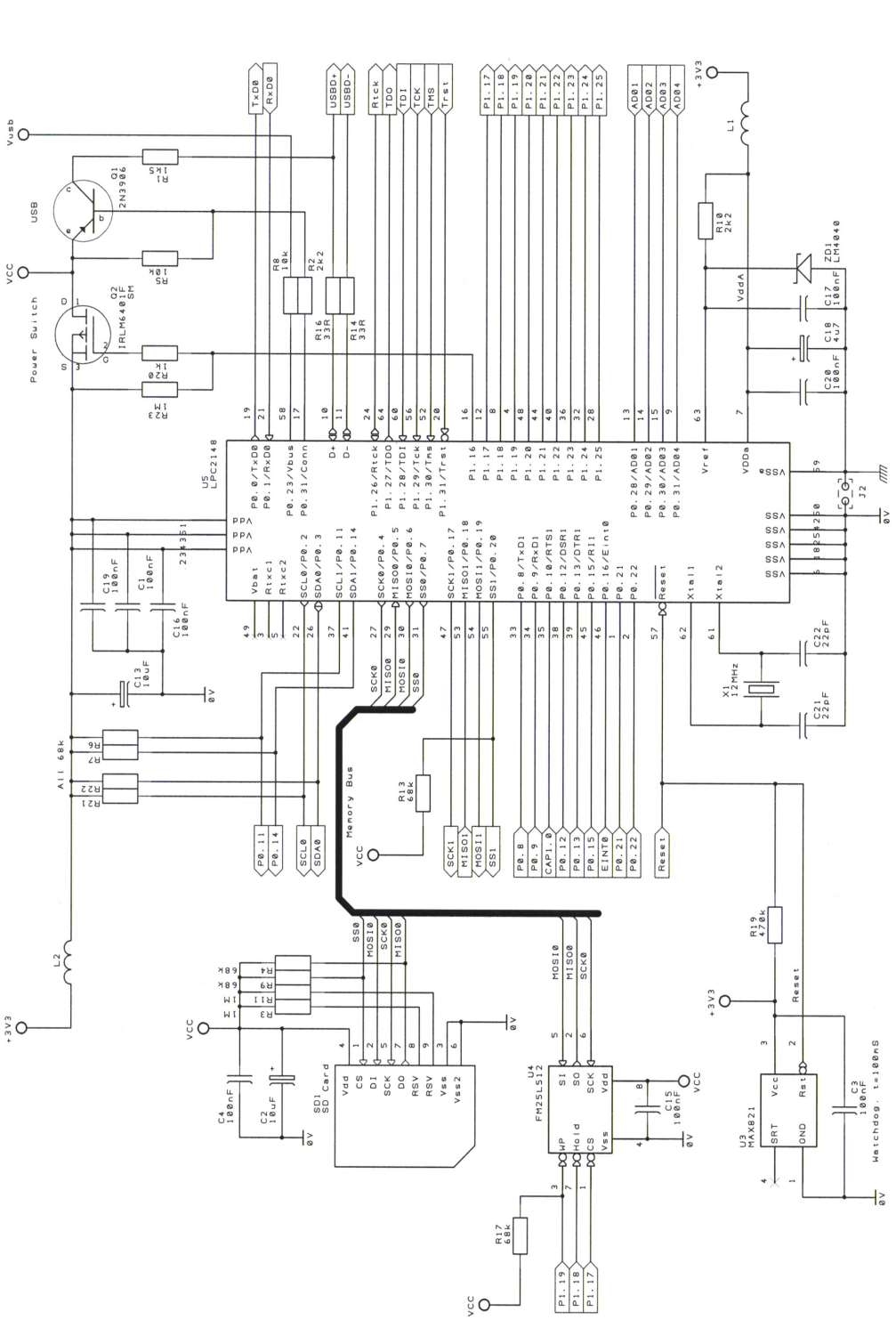
APPENDICES

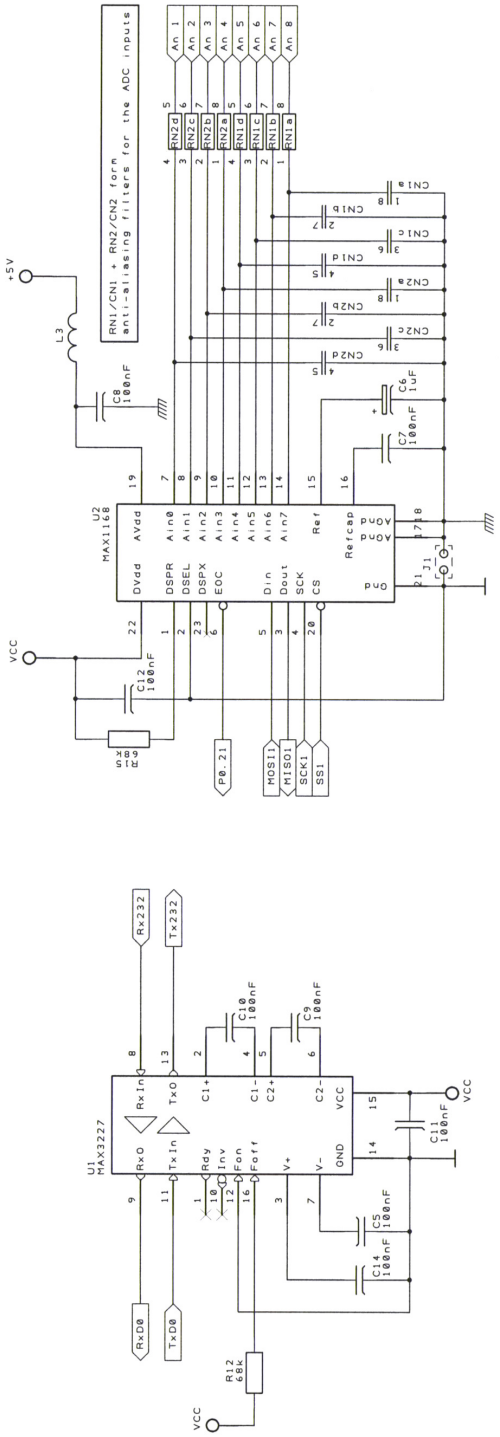
Appendix A

Personal Data Logger

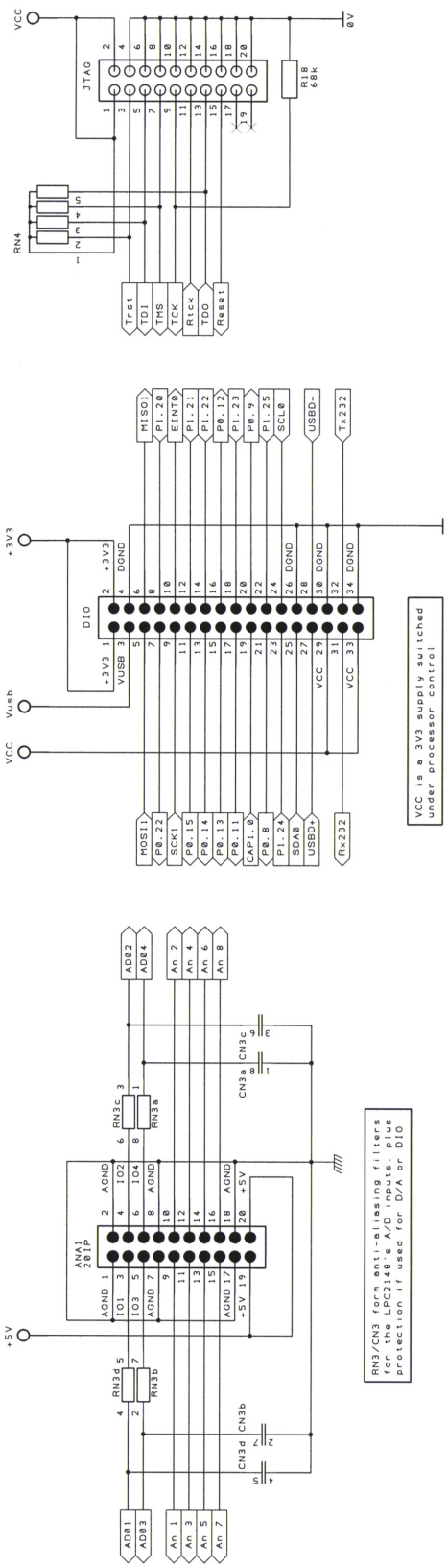
Circuit Schematics



Processor and Memory Arrangement



Serial Interface and Analogue to Digital Converter



System Input and Output Port Connections

Appendix B

Personal Data Logger

Parts List

Ref	Name	Function	Side	Package
C1	100nF capacitor	LPC2148 Decoupler	Bottom	0805 sm
C2	10uF 10V tantulum capacitor	SD Decoupler	Top	TAJB sm
C3	100nF capacitor	Watchdog Decoupler	Bottom	0805 sm
C4	100nF capacitor	SD Decoupler	Top	0805 sm
C5	100nF capacitor	MAX3227 V- Decoupler	Top	0805 sm
C6	1uF 10V tantulum capacitor	ADC Ref	Top	TAJA sm
C7	100nF capacitor	ADC RefCap	Top	0805 sm
C8	100nF capacitor	ADC Avdd Decoupler	Top	0805 sm
C9	100nF capacitor	MAX3227 Boost Cap	Top	0805 sm
C10	100nF capacitor	MAX3227 Boost Cap	Top	0805 sm
C11	100nF capacitor	MAX3227 Decoupler	Top	0805 sm
C12	100nF capacitor	ADC Decoupler	Top	0805 sm
C13	10uF 10V tantulum capacitor	Power Decoupler	Bottom	TAJB sm
C14	100nF capacitor	MAX3227 V+ Decoupler	Top	0805 sm
C15	100nF capacitor	FRAM Decoupler	Top	0805 sm
C16	100nF capacitor	LPC2148 Decoupler	Top	0805 sm
C17	100nF capacitor	LPC2148 Vref Decoupler	Top	0805 sm
C18	10uF 10V tantulum capacitor	LPC2148 VddA Decoupler	Top	TAJB sm
C19	100nF capacitor	LPC2148 Decoupler	Top	0805 sm
C20	100nF capacitor	LPC2148 VddA Decoupler	Top	0805 sm
C21	22pF capacitor	Crystal Capacitor	Top	0805 sm
C22	22pF capacitor	Crystal Capacitor	Top	0805 sm
CN1	33nF capacitor array	ADC Anti-Aliasing Cap	Bottom	C0612 sm
CN2	33nF capacitor array	ADC Anti-Aliasing Cap	Bottom	C0612 sm
CN3	33nF capacitor array	LPC2148 Anti-Aliasing Cap	Bottom	C0612 sm
L1	Ferrite Chip Bead	LPC2148 Avdd Filter	Bottom	0805 sm
L2	Ferrite Chip Bead	LPC2148 Power Filter	Bottom	0805 sm
L3	Ferrite Chip Bead	ADC Power Filter	Top	0805 sm
R1	1k5 resistor	USB Soft Connect	Bottom	0805 sm
R2	2k2 resistor	USB Connect	Bottom	0805 sm
R3	47k resistor	SD RSV pull-up	Top	0805 sm
R4	47k resistor	MISO0 SD pull-up	Top	0805 sm
R5	10k resistor	USB Connect pull-up	Bottom	0805 sm
R6	47k resistor	SCL1 I2C pull-up	Bottom	0805 sm
R7	47k resistor	SDA1 I2C pull-up	Bottom	0805 sm
R8	10k resistor	USB V+ Detect	Bottom	0805 sm

R9	47k resistor	SS0 SD CS pull-up	Top	0805 sm
R10	2k2 resistor	LPC2148 Vref	Bottom	0805 sm
R11	47k resistor	SD RSV pull-up	Top	0805 sm
R12	47k resistor	MAX3227 Foff pull-up	Top	0805 sm
R13	47k resistor	SS1 SPI pull-up	Top	0805 sm
R14	33R resistor	USB Input	Top	0805 sm
R15	47k resistor	ADC DSPR pull-up	Top	0805 sm
R16	33R resistor	USB Input	Top	0805 sm
R17	47k resistor	FRAM WP pull-up	Top	0805 sm
R18	47k resistor	JTAG TCK pull-down	Bottom	0805 sm
R19	470k resistor	Reset pull-up	Bottom	0805 sm
R20	1k resistor	PFET Switch - Gate	Bottom	0805 sm
R21	47k resistor	SCL0 I2C pull-up	Top	0805 sm
R22	47k resistor	SDA0 I2C pull-up	Top	0805 sm
R23	1M resistor	PFET Switch - Gate pull-up	Bottom	0805 sm
RN1	1k resistor array	ADC Anti-Aliasing Res	Top	1206sm array
RN2	1k resistor array	ADC Anti-Aliasing Res	Top	1206sm array
RN3	1k resistor array	LPC2148 Anti-Aliasing Res	Top	1206sm array
RN4	47k resistor network (common)	JTAG pull-ups	Top	SIL-5 pth
Q1	2N3906 PNP transistor	USB Soft Detect	Bottom	SOT-23 sm
Q2	IRLM6401F PMOS FET	P-channel MOSFET	Bottom	SOT-23 sm
U1	MAX3227	RS232 Driver	Top	SSOP-16 sm
U2	MAX1168	ADC	Top	QSOP-24 sm
U3	MAX821	Watchdog	Bottom	SOT-143 sm
U4	FM25L512	FRAM	Top	SO-8 sm
U5	LPC2148	Microcontroller	Top	LQFP64 sm
X1	12.000 MHz Crystal	System Clock	Top	HC49/4H pth
ZD1	LM4040	LPC2148 Vref	Bottom	SOT-23 sm
ANA1	10x2 0.1" Header	Analogue I/O	Bottom	pth
DIO	17x2 0.1" Header	Digital I/O	Bottom	pth
JTAG	10x2 0.1" Header	JTAG Header	Top	pth
SD1	Mini SD Skt	Data memory	Bottom	sm
J1	Solder Link	ADC Ground Link	Top	n/a
J2	Solder Link	LPC2148 Ground Link	Top	n/a