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Readout of the UFFO Slewing Mirror Telescope to detect UV/optical photons from Gamma-Ray Bursts

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ABSTRACT: The Slewing Mirror Telescope (SMT) was proposed for rapid response to prompt UV/optical photons from Gamma-Ray Bursts (GRBs). The SMT is a key component of the Ultra-Fast Flash Observatory (UFFO)-pathfinder, which will be launched aboard the *Lomonosov* spacecraft at the end of 2013. The SMT utilizes a motorized mirror that slews rapidly forward to its target within a second after triggering by an X-ray coded mask camera, which makes unnecessary a reorientation of the entire spacecraft. Subsequent measurement of the UV/optical is accomplished by a 10 cm aperture Ritchey-Chrétien telescope and the focal plane detector of Intensified Charge-Coupled Device (ICCD). The ICCD is sensitive to UV/optical photons of 200–650 nm in wavelength by using a UV-enhanced S20 photocathode and amplifies photoelectrons at a gain of 10^4 – 10^6 in double Micro-Channel Plates. These photons are read out by a Kodak KAI-0340 interline CCD sensor and a CCD Signal Processor with 10-bit Analog-to-Digital Converter. Various control clocks for CCD readout are implemented using a Field Programmable Gate Array (FPGA). The SMT readout is in charge of not only data acquisition, storage and transfer, but also control of the slewing mirror, the ICCD high voltage adjustments, power distribution, and system monitoring by interfacing to the UFFO-pathfinder. These functions are realized in the FPGA to minimize power consumption and to enhance processing time. The SMT readout electronics are designed and built to meet the spacecraft's constraints of power consumption, mass, and volume. The entire system is integrated with the SMT optics, as is the UFFO-pathfinder. The system has been tested and satisfies the conditions of launch and those of operation in space: those associated with shock and vibration and those associated with thermal and vacuum, respectively. In this paper, we present the SMT readout electronics: the design, construction, and performance, as well as the results of space environment test.

KEYWORDS: Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases); Digital electronic circuits; Space instrumentation; Detectors for UV, visible and IR photons

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1 Introduction

Launched in 2004, *Swift* space observatory has provided first and a variety of multi-wavelength information on gamma-ray bursts (GRBs; [1]) including UV/optical light curves in the sub-minute time scale in spite of a limitation in the response time [2]. After the *Swift* has localized a GRB through X-ray detection by its Burst Alert Telescope, it takes about a minute to reorient the entire spacecraft to the GRB location coordinates [3]. However, in the intervening time valuable information may be lost. In order to capture UV/optical photons from GRBs nearly at the same time as X-ray detection, the Ultra-Fast Flash Observatory (UFFO) has been proposed as a space mission. To achieve these extremely fast response times, the UFFO is based upon the concept of a Slewing Mirror Telescope (SMT) [4]. A pilot experiment, the UFFO-pathfinder, employs a novel approach of the beam steering: the utilization of a motorized mirror to redirect photons from the GRB to a UV/optical telescope on axis [5]. The UFFO-pathfinder consists of two telescopes; the wide field-of-view (FOV) X-ray UFFO Burst Alert & Trigger Telescope (UBAT) for localization of GRB event [6], and the SMT for the rapid measurement of a UV/optical within a narrow FOV [7, 8]. Additionally, the UFFO Data Acquisition system (UDAQ) controls each telescope of the UFFO-pathfinder and interfaces with the satellite [9].

From a functional perspective, the SMT has two subsystems. One is an opto-mechanical system detailed in [7], and the other consists of readout electronics including a focal plane detector and a slewing mirror. The FOV of the focal plane detector is 17×17 arcmin² determined by SMT optics, and it is wide enough to contain a potential source of GRB detected by the UBAT with a

localization accuracy of 10 arcmin in 7σ . The mirror rotation angle is ± 35 degree, and thus the effective coverage of SMT extends to 70×70 degree² that corresponds to the half-coded FOV of UBAT. An Intensified Charge-Coupled Device (ICCD) with double multi-channel plates (MCPs) was adopted as the focal plane detector, like the *Swift*'s UV/optical telescope, to observe light from the distant GRBs. To meet the UFFO's requirements for achieving the fastest yet response to prompt photons from GRBs, we chose commercial rotary encoders and stepping motors with sealed bearing systems. The slewing mirror is driven by two gimbal motors that provide a 1 sec response over the entire FOV with sub-arcsec positioning accuracy and a settling time of less than 350 msec. These electric motors which drive the gimbal-mounted mirror are simple, robust, and space qualified.

The readout electronics controls the slewing mirror, reads out the ICCD as well as the entire SMT system, monitors housekeeping sensors, and communicates with the UDAQ. As with other space experiments, the UFFO pathfinder has substantial limitations both in power consumption and real-time processor speed. Even more so, the electronics must be compact due to volume constraints, especially because, unlike previous GRB missions, the proposed device contains several electronics modules onboard [3, 10, 11]. Additionally, the SMT requires fast algorithms to slew the mirror in response to the UBAT trigger. These requirements are satisfied by employing a Field-Programmable Gate Array (FPGA) in place of CPU. The FPGA includes a variety of functions required for the SMT readout and control as well as the interface to the payload system. Moreover, in order to ensure the best performance of the ICCD for our application, the control of clock signals and high voltages is customized in the FPGA. We also tested the readout electronics in the extreme environments simulating those that will be encountered during a space mission, and they passed all requirements for operation in space.

This paper focuses on the design and construction of the SMT readout, and is organized as follows: section 2 explains: the overall architecture of the SMT's readout and control system; the CCD and its readout, data taking and storage; and the monitoring and control of the slewing mirror essential to the SMT. In sections 3 and 4, we report on the results of the performance and space environment tests, respectively. Finally, we summarize the results in section 5.

2 Readout and control electronics of SMT

The main goal of the SMT readout is to achieve rapid mirror slewing, control of the focal plane detector, and fast readout, and thus, ultimately, to take the data with fine time resolution immediately after the trigger. The readout electronics include the following functions:

- Motor control and encoder calibration
- Generation of the CCD control clocks
- Adjustment of high voltage to control the ICCD gain
- Data acquisition and storage
- Communication with the UDAQ to send data and to receive commands
- Monitoring the housekeeping data including temperature and current.

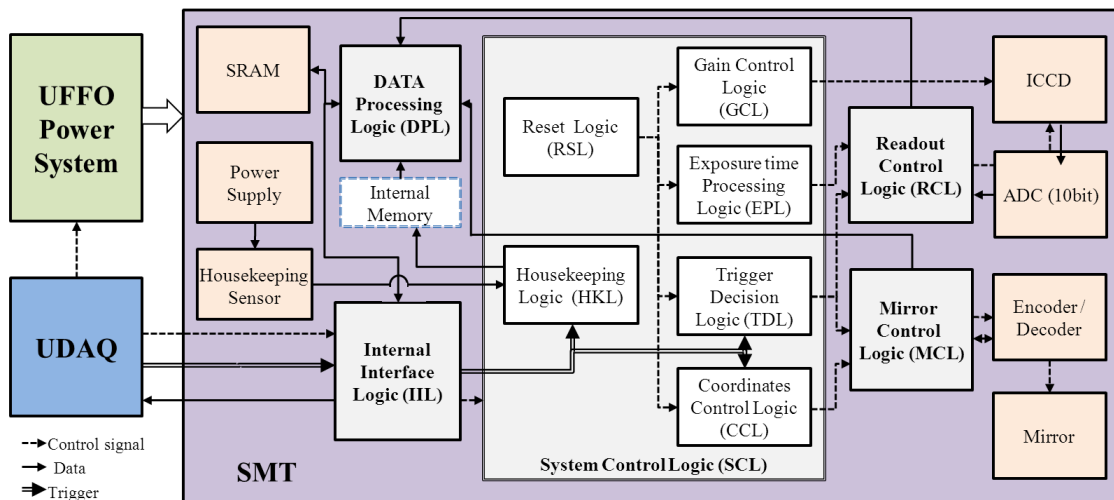


Figure 1. Architecture of the SMT readout and control, which shows the trigger flow (double line) from the UDAQ, the data flow (single line) from the ICCD to the UDAQ, and the control signals (dashed lines).

The SMT readout is controlled by an ACTEL A3P100 0-PQ208 FPGA chip. The most critical requirements of the SMT are the fast processing time, as stipulated for the UFFO, and as is typical in space applications, the minimization of the power consumption. Both requirements are accomplished by using, in place of a traditional microprocessor, an FPGA, which consumes less than 1W to program all functions.

Figure 1 shows the readout and control architecture of the SMT. The architecture has 5 logic blocks, each in charge of its own hardware: the Motor control logic (MCL) regulates the motor and reads the encoder; the Readout Control Logic (RCL) governs the ICCD control and data acquisition, which includes the CCD readout. The System Control Logic (SCL) is the main block of the SMT readout as well as the control that manages and the interactions among all logic blocks, itself included, and serves additionally to control the SMT memory and processors. The SCL includes the Reset Logic for the internal system reset, the Trigger Decision Logic (TDL) for the action of the slewing mirror and ICCD by trigger decision, the Coordinates Control Logic (CCL) for decoding the coordinates value, the Gain Control Logic (GCL) for the ICCD gain adjustment, the Exposure time Processing Logic (EPL) for the exposure time setting to optimize the measurement of GRB light, and the Housekeeping Logic (HKL) for monitoring of current, voltage, and temperature of the electronics boards. All the logic blocks in the FPGA include the reset signal as an input source, and to achieve system stabilization, they are controlled by the Reset Logic. After the system turns on, the Reset Logic counts the time and waits until the FPGA power is stable, and then it pulls down the reset signals of the entire logic block. To write or read the data, the Data Processing Logic (DPL) manages the external memory. The Internal Interface Logic (IIL) is responsible for communication between the UDAQ and the SMT system.

2.1 Detector and CCD readout

As with the *Swift*, the ICCD has been adopted as the SMT's focal plane detector. This device consists of an intensifier and a CCD coupled by a fiber optics taper. The intensifier is comprised of an

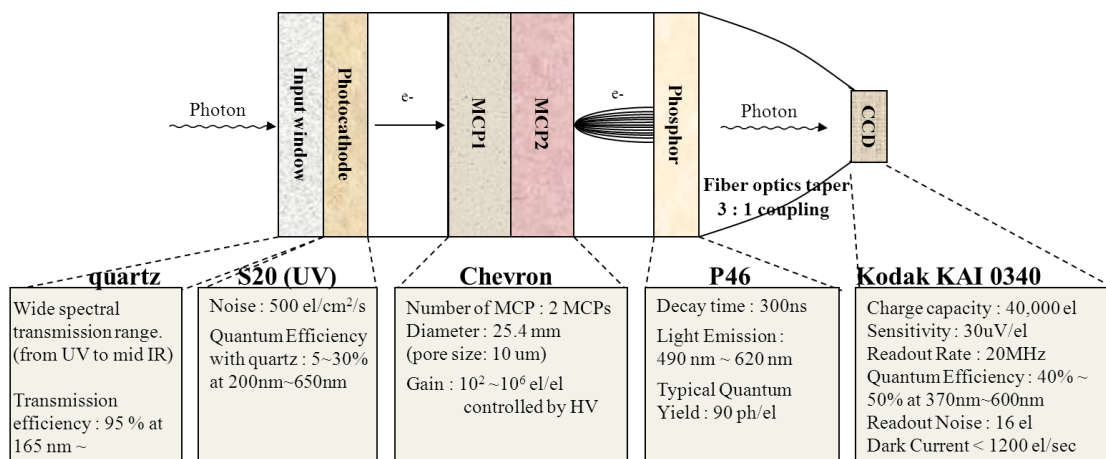


Figure 2. Structural diagram of the customized ICCD for the SMT.

input window, a photocathode, double Micro-Channel Plates (MCPs) with a two-stacked structure, and a phosphor screen, as shown in figure 2 and detailed below. The intensifier is optimized over the 200–650 nm band as determined by the photocathode and the detector input window. Photons entering the ICCD are converted into electrons at the photocathode and are subsequently multiplied by a factor of up to 10^6 within the MCPs. Clusters of these electrons strike the phosphor screen, which changes the amplified electrons into visible light, and this light reaches the CCD sensor through the fiber optic taper.

The input window is made of quartz, a material which limits the spectral response of the photocathode at short wavelengths, i.e. to 165 nm or greater at the lower limit. Nevertheless, the UV-enhanced S20 photocathode beneath the input window provides better sensitivity at UV/optical wavelengths (<350 nm) than other photocathodes; the spectral response of the photocathode is shown in figure 3. The spectral sensitivity is higher than 50 mA/W for $\lambda < 450$ nm, and the maximal sensitivity is 65.6 mA/W at 280 nm, which corresponds to a quantum efficiency of about 29.1%. The photocathode has a dark current of about 500 electron/cm²/sec at room temperature contributed chiefly by thermal noise. This dark rate can be negligible for pixels of $23.68 \times 23.68 \mu\text{m}^2$ at an exposure time of 20 msec.

An electron from the photocathode enters the MCPs and produces secondary electrons upon striking the inner walls of the MCPs. These secondary electrons are further accelerated by a voltage applied across the MCPs to produce additional multiplication; the electron multiplication factor per MCP is 1000 average. We have chosen dual MCPs in order to better discriminate the signal of the faint source from the background noise. By providing dual MCPs, our ICCD achieves gains of up to 1.2×10^6 W/W at 480 nm and can also be operated as a photon counting detector. The measurement of faint sources requires long exposure times, which in turn increase accumulated noise. Therefore, high amplification for given photons is relatively free of random noise. Each MCP has a diameter of 25 mm, and its pore size is $10 \mu\text{m}$, with a pitch size of $12 \mu\text{m}$.

Fast readout requires a phosphor with a rapid decay time. If the decay time is slower than the readout time, the image taken by CCD will be distorted by a smearing effect. We use a P46 phosphor screen with a decay time of 300 nsec and a light emission range of 490–620 nm. Because

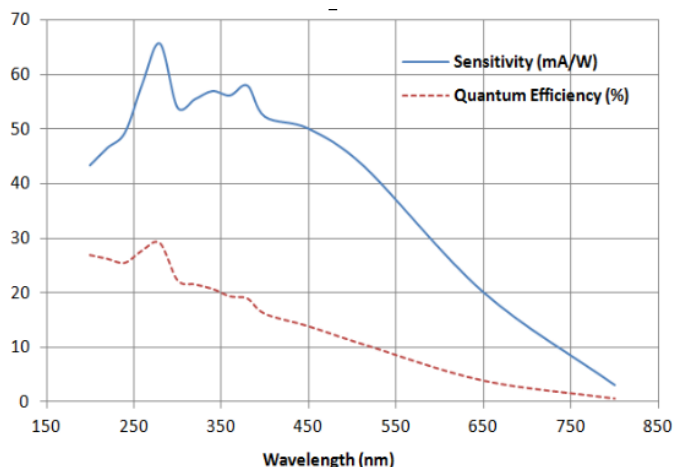


Figure 3. Spectral response and quantum efficiency of the ICCD photocathode as a function of wavelength (measured by Proxitronic Detector Systems GmbH). The solid line indicates the spectral sensitivity and the dashed line the quantum efficiency.

the diameter of the MCPs is larger than the active CCD area, the phosphor is connected with the CCD by a fiber optics taper coupling ratio of 3.2:1. The fiber coupling blocks out stray light and minimizes light loss; consequently, this method of coupling between phosphor and CCD ensures much a better signal to noise (SNR) ratio than the lens coupling method. Furthermore, fiber coupling allows a strong fixation and robust structure for the ICCD and makes it more suitable for space application where no changes are possible once the structure is set up.

Light emitted from the phosphor screen passes through the fiber optics taper and is read out by the CCD. We have chosen a commercial interline CCD, the Kodak KAI-0340, which provides a fast pixel readout rate up of to 40 MHz. The CCD dimensions are 640×480 pixels; however, for our observations we employ only 256×256 pixels of the total resolution. Likewise, as described in the following section, the CCD readout has been customized for our application. Therefore, the size of focal plane detector, i.e. size of the ICCD, is $6.062 \times 6.062 \text{ mm}^2$ when the coupling ratio is taken into account, and the dimensions of the individual pixels are $23.68 \times 23.68 \text{ }\mu\text{m}^2$. The angular resolution for each pixel is $4 \times 4 \text{ arcsec}^2$.

The CCD readout is a new design, intended chiefly to meet the requirements for application in space, i.e. power consumption and volume, and is connected to the spacecraft by a bus interface. The readout has several processors to provide various control clocks for CCD operation and to process the signal from the ICCD. We have chosen an FPGA to implement the readout and control of the CCD, which allows us to make compact system. The ICCD is divided physically into three functional boards, as shown in figure 4; a CCD-sensor board for the mount of the CCD chip, a clock-generator board for CCD control, and a SMT-DAQ board for data acquisition and system control.

The CCD-sensor board is required to bridge the ICCD and the readout boards both mechanically and electronically. This sensor is placed at the back of the ICCD and provides a mechanical decoupling for the ICCD from the readout boards, and contains a delicate structure of fiber couplings inside which offer protection against the shock and vibration expected from the launch of

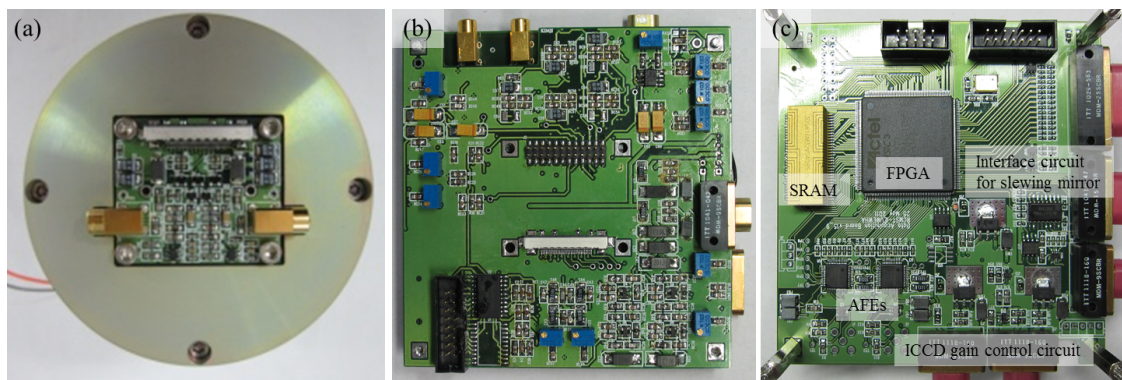


Figure 4. ICCD combined with the CCD sensor board (left) the clock-generator board (center) and the SMT-DAQ board (right).

satellite. The board's size is $35 \times 40 \text{ mm}^2$, and it contains a socket for the insertion of the CCD chip. The CCD output signal is buffered by an emitter follower before it is sent to the clock-generator board through a coax cable and eventually to the SMT-DAQ board.

The clock-generator board generates a variety of 20 MHz control signals to operate the CCD. The board drives 4 horizontal clocks, 4 vertical clocks, a reset clock, 2 fast dump signals used for the selection of an imaging area from the CCD's 640×480 pixels, a signal for electronic shuttering, and a voltage signal for protection against electrostatic discharge. These clocks and signals are transmitted to the ICCD through the CCD-sensor board.

As shown in figure 4(c), the SMT-DAQ board is made of an FPGA, an SRAM, a circuit to control the ICCD gain, an interface circuit to slew the mirror, two front-end circuits for the processing of the analog signal from CCD, and two sensors for monitoring board temperature and current.

A fast pixel readout rate, i.e. a high frame rate, is possible in the interline transfer type of CCD. However, such fast rates limit the capacity of the charge held in a pixel, illustrating the trade-off between readout rate and dynamic range. We employ a 20 MHz rate instead of the allowed maximum of 40 MHz, and as a result we are able to extend the maximum charge capacity to a value of 40,000 photoelectrons. Additionally, power consumption is reduced substantially at this relatively slow frame rate.

The CCD requires multiple clocks related to the readout of pixel, line and frame, and their control signals. These are organized in three controllers shown in figure 5. The line controller generates a line-readout clock and a line valid by counting the pixel-readout clock cycles, while the horizontal clock block generates 4 horizontal clocks and a reset clock. A vertical clock corresponds to 256 horizontal clocks. The frame controller produces a frame-readout clock and a frame valid by counting the line-readout clock cycles, while the vertical clock block produces the 4-type vertical clocks. A frame clock corresponds to 256 vertical clocks.

Analog signals from CCD sensor are processed in an AD9840A chip indicated in figure 8 as the CCD signal processor (CSP). The CSP includes a 10-bit analog to digital converter (ADC). Data and image processing in the CSP are performed by the CSP controller of the FPGA via a 3-wire serial interface. The CSP controller also adjusts the gain for the ADC on the basis of predefined parameters for CSP chip and black level adjustment.

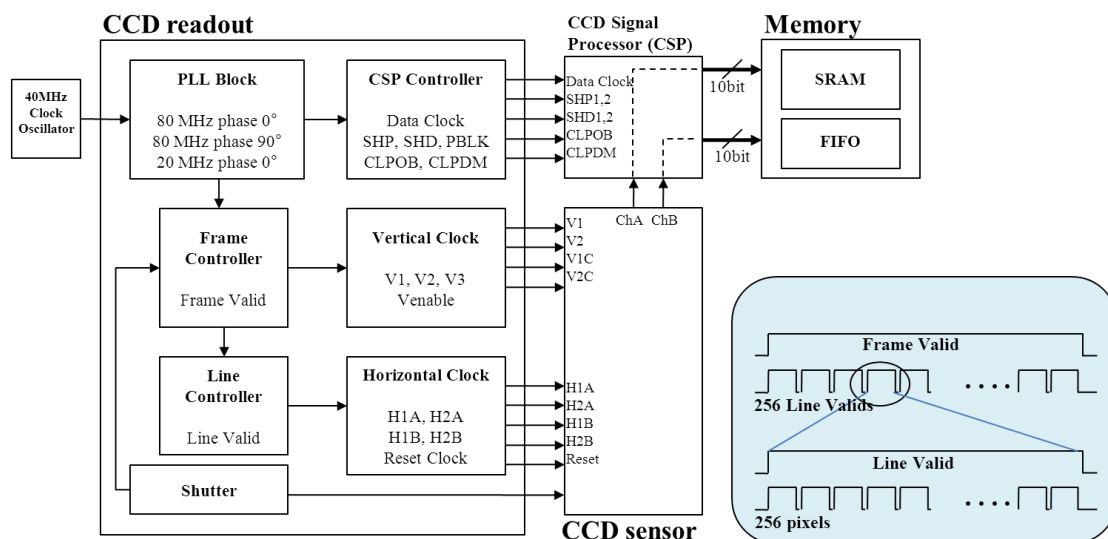


Figure 5. Block diagram depicting how the CCD readout system of the FPGA generates clocks and provides them for the CCD chip. These clocks are used to control the CCD chip and read out the charge in each pixel. The blue box shows how the pixel clock is related to the line clock and the frame clock.

2.2 Data acquisition and storage of SMT

The ICCD data is read out by a 10-bit ADC. However, it is resized as 8-bit data to optimize the bit size of SRAM and to reduce data size. When the ICCD data value is low and the data do not require large numbers, then the 2 bits from Most Significant Bits (MSB) are cut. Otherwise, 2 bits are removed from the Least Significant Bits (LSB). Likewise, The DPL determines the reasonable bit range for the ICCD data and records the resizing factor in the housekeeping data. Consequently, the ICCD data size becomes 512 kbits, and 32 frames are stored in the 16 Mbits SRAM. The housekeeping data is updated every frame, and its data size is 4 kbits. The DPL which manages the memory to read or write the data arranges the ICCD data in the SRAM and the housekeeping data in the First-In, First-Out (FIFO), and combines both into a single frame.

At the initial trigger, the exposure time is same as the integration time for a single frame. At that time, the SRAM is full in 640 msec because of limitation of storage, and the dead time which takes to clear the memory occurs before next exposure. Additionally, the readout rate is 20 Mbytes/sec at the initial trigger, but the transfer rate between the UDAQ and the SMT is 2 Mbytes/sec. Therefore, to prevent problems, the DPL controls the data transfer by sending the data to the UDAQ while receiving the data from the ICCD asynchronously.

2.3 Control of SMT and interface with UFFO Data acquisition system

The SMT receives the trigger and control signals from the UDAQ, and also transfers its physical data to the UDAQ. The communication between the SMT and the UDAQ is accomplished through a Serial Peripheral Interface bus (SPI). The IIL formats the UDAQ's serial commands as parallel, sends commands to the inner logic of the SMT, and then returns the data to UDAQ, after changing parallel-type data back to serial. The data from UDAQ includes the commands, coordinates and time information, which the IIL decodes according to their indicators and classifies before sending them to the SCL.

Table 1. Exposure time defined for one GRB event.

Session	Exposure time (sec)	Number of frames	Duration time (sec)
1	0.02	20.00	0.40
2	0.20	38.00	7.60
3	1.00	42.00	42.00
4	5.00	50.00	250.00
5	10.00	70.00	700.00
Total		220.00	1,000.00

Table 2. SMT data size.

Data size of one frame		Data size of one GRB event	Data size per day
ICCD	Housekeeping		
256 ch×256 ch×8 bits	4 kbits	516 kbits×220 frames	113,520 kbits×15 events
516 kbits		113,520 kbits	~ 208 Mbytes

After the UFFO power turns on, the UDAQ sends the SMT the state signal which initializes the SMT's electronics. Then, the SCL which manages the sequence of the SMT operation powers up the slewing mirror system so that the motor initializes and stabilizes. Next, when the SMT receives a trigger signal from UDAQ, the SMT classifies the trigger type as either UBAT or an external trigger given by the other X-ray detection payload on the *Lomonosov* spacecraft. Meanwhile, the motor state remains in stand-by mode as the x, y, and z coordinates of the target, the position of which is specified with respect to the position of UFFO-pathfinder, are delivered by the UDAQ. When the motor slews to the target, the ICCD power is on, the CCD readout system is ready, and the ICCD begins taking the data.

The integration time is adjusted through electronic shuttering by the CCD chip and by default is set to 20 msec. This value is the same as the readout time for a single frame and is also set as the default exposure time. However, as determined from UV/optical light curves, some measurements show that GRB intensity has shown violent variation occurring at the initial triggering time, followed by a gradual decline in light intensity. Thus, the SMT captures data over 5 sets or sessions at the 5 different exposure durations specified in table 1. During the first session, 20 frames with exposure times of 20 msec are taken during the 400 msec immediately following the UBAT's transmission of the GRB position information to the SMT. After that, for the second session, the exposure time is raised to 200 msec by summing every 10 default frames. During the second session, the SMT captures 38 frames over a span of 7.6 sec. Likewise, the exposure time for each subsequent session is set to the duration predefined for that session. As a result, for any single event, the data of 220 frames are taken for a total duration time of 1000 sec.

The satellite moves in a Sun-synchronous orbit at an altitude of 550 km, makes 15 orbits per day at 96 minutes per orbit. The SMT generates 113,526 kbits of data per event, and selects a good candidate event per orbit. Therefore, the total data size of SMT will be ~208 Mbytes/day, as summarized in table 2. The data of 300 Mbytes/day in total allocated for UFFO-pathfinder, including the one from UBAT, will be transferred to ground stations via the UDAQ and the spacecraft.

2.4 Housekeeping

The SMT readout monitors the currents and the temperatures from sensors once per frame, and logs trigger information, including the GMT time triggered, the coordinates, and trigger identification, the received commands, the position of the mirror, the high voltage value of the ICCD, exposure time, and frame identification. The SMT writes the housekeeping data in front of every frame; thus the HKL updates and holds the data in the internal memory which is the FIFO of the FPGA, and for each frame the housekeeping data is transferred to the UDAQ.

2.5 Slewing mirror control

The motors operate in the following 6 states, or modes: the safe, initialization, stand-by, targeting, calibration, and sleep modes. Each mode determines the mirror position or its function. The motor state sequence is shown in figure 6.

Once the power is on, the motor enters safe mode until the SMT readout determines that the spacecraft has entered the night phase of its orbit. While in safe mode, the mirror remains at the position defined by 0 degree on the A- and B-axes in order to protect the ICCD from sunlight reflected by the slewing mirror. Additionally, should the SMT encounter an emergency situation in which the ICCD may be damaged, the motor state will immediately revert to safe mode. This sequence applies for all motor states. Following operation in safe mode, the motor state changes to initialization mode, activates the motor's encoder, sets parameters, and shifts automatically into stand-by mode. On the other hand, if the emergency situation terminates without power recycling, the motor state shifts directly into stand-by mode without first changing into initialization mode.

Upon entering stand-by mode, the motor moves the mirror to 0 degree on the A-axis and 45 degree on the B-axis. The advantage of maintaining the stand-by position at the angles just defined is that the rotation angle to the target decreases and, as a result, the slewing time is also reduced. When the GRB is found within our FOV during stand-by mode, the coordinate information is delivered to the FPGA, and the motor state changes to targeting mode. The mirror control logic in the FPGA calculates how many degrees the mirror must be tilted, and transfers the equivalent value of clocks to the slewing mirror system to direct the mirror forward to the target. After the motor stops, if there is no additional trigger from the UBAT within 10 seconds, the capture of the preceding event is concluded, and the motor state reverts to stand-by mode. The FPGA's motor control system always informs its readout control system as to whether the motor is moving or has already moved, because, in the event that motor should stop during targeting mode, the CCD shutter is still operational. When the mirror is slewed onto the target, the SMT readout including ICCD is ready, and starts to capture data.

In calibration mode, the encoder values are scanned and the motor position is calibrated with respect to the difference between the encoder value and the measured position. This operation is performed along the schedule predefined in the FPGA, or on command. After all procedures have been carried out, if there is no further task, to save power the motor state shifts via safe mode into sleep mode.

The orientation of the mirror with respect to the standby position can be read by encoders which are directly mounted on a mirror rotation axis via an axis-coupling, as shown in figure 7(a). Two encoders are mounted for the A- and B-axes. Analog sine/cosine outputs from these encoders

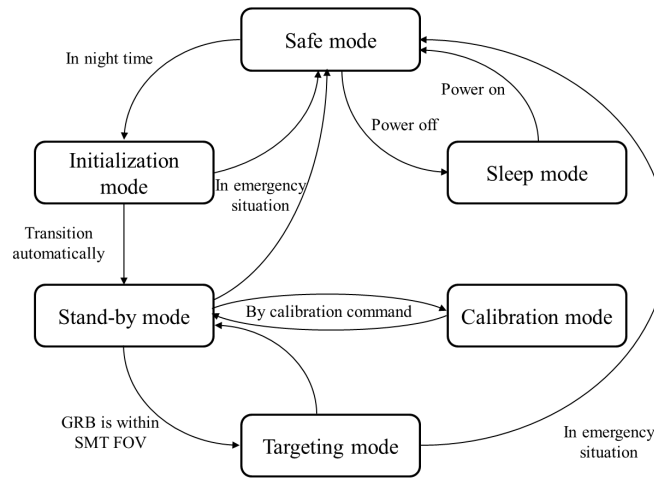


Figure 6. State and transition of slewing mirror system. Each mode determines the mirror position or its function. The ICCD is activated after the motor stops at the stand-by mode.

are converted to digital outputs on the decoders after interpolation for better precision. RS-422 differential line driver outputs from the decoder can be read using Synchronous Serial Interface (SSI) data format.

The motor rotates with respect to A and B axes that are defined relative to the platform of the UFFO-pathfinder payload as shown in figure 7(b). The motor control logic calculates the angles to be rotated using a matrix for conversion between the UFFO coordinates and the slewing mirror system coordinates. When the UBAT detects a GRB candidate, it sends a trigger signal and the location specified in celestial coordinates to the SMT via the UDAQ interface. The SMT reads the current mirror position and calculates the slewing angle to the target position within the FPGA. After tilting the slewing mirror forward to the target by that angle, the SMT begins reading the UV/optical data.

In order to calculate the motor rotation angles, the coordinate is defined with regard to a target. The target position determined relative to the UFFO coordinates is $\vec{v}_t = (x, y, z)$, and the mirror angular position defined relative to the normal vector of mirror surface is $\vec{v}_m = (x_m, y_m, z_m)$. The optical axis of the telescope specified in terms of the mirror is $\vec{v}_d = (1, 0, 0)$. Therefore, using the law of reflection, \vec{v}_m can be obtained as eq. (2.1).

$$\vec{v}_m = \frac{\vec{v}_d + \vec{v}_t}{|\vec{v}_d + \vec{v}_t|} = \frac{(x+1, y, z)}{\sqrt{(x+1)^2 + y^2 + z^2}} \quad (2.1)$$

The pointing vector, \vec{v}_m , can be considered as a combination of two motor rotations. When the mirror is parallel to the baseplate, the normal vector of the mirror is $\vec{v}_m = (0, 1, 1)$. For a rotation of the mirror by A and B, \vec{v}_m may be expressed by two consecutive rotations as

$$\vec{v}_m = \begin{pmatrix} \cos A & 0 & \sin A \\ 0 & 1 & 0 \\ -\sin A & 0 & \cos A \end{pmatrix} \begin{pmatrix} 1 & 0 & 0 \\ 0 & \cos B & -\sin B \\ 0 & \sin B & \cos B \end{pmatrix} \begin{pmatrix} 0 \\ 0 \\ 1 \end{pmatrix} = \begin{pmatrix} \cos A \sin B \\ -\sin B \\ \cos A \cos B \end{pmatrix}, \quad (2.2)$$

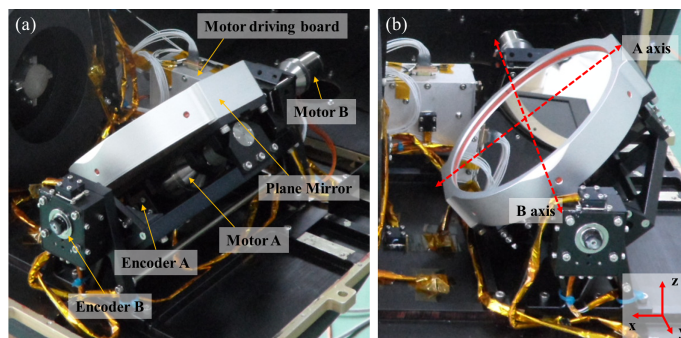


Figure 7. (a) The composition of slewing mirror system. The motor driving board is handled by readout electronics of the SMT (b) the x, y, and z coordinates are defined for the UFFO coordinate system, and A and B coordinates for the slewing mirror coordinate system.

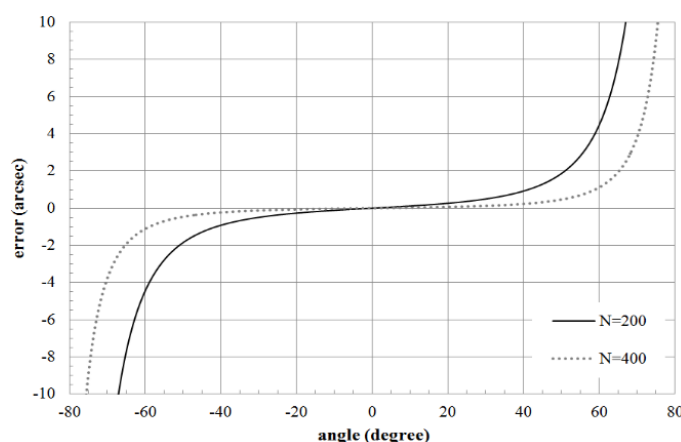


Figure 8. The angular error distributions taken by a linear interpolation with the look-up array size of N=200 and of N=400. For greater precision, a larger array size is needed. Still, N=200 is adequate for a 4 arcsec precision in mirror angle coverage during targeting mode; the value covers from -17 degree to 17 degree on the A axis, and -62 degree to -28 degree on the B axis.

where the first term is the rotation by A around the x-axis and the second term is the rotation by B around the y-axis. Combining eq. (2.1) and eq. (2.2), the motor rotation angles, A and B, may be calculated as

$$A = \arcsin\left(\frac{x+1}{\sqrt{(x+1)^2+z^2}}\right), \quad B = \arcsin\left(\frac{-y}{\sqrt{(x+1)^2+y^2+z^2}}\right). \quad (2.3)$$

To calculate the inverse sine function in the FPGA, we employ an interpolation method with a look-up table for an approximate result. Were we to use a lookup table by itself, a huge amount of memory would be necessary to achieve the precision required for the slewing the mirror, 4 arcsec per motor minimum step. However, this interpolation method offers a feasible solution using a lookup table with a small array size as in figure 8.

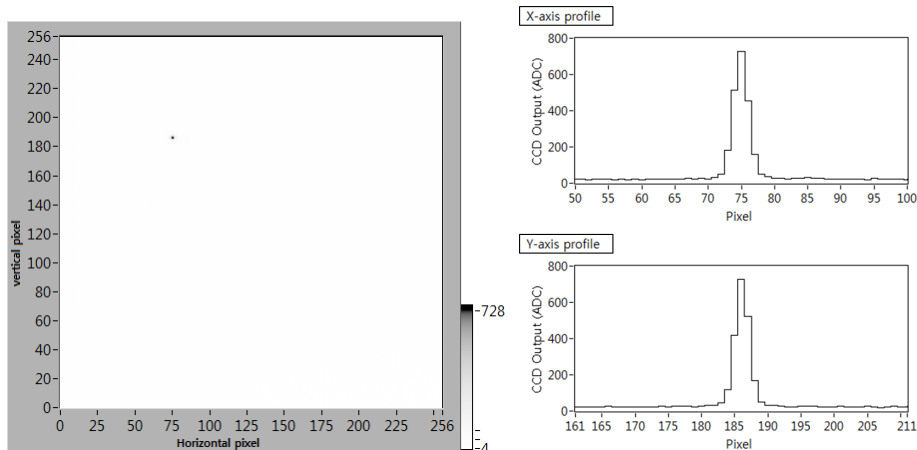


Figure 9. The ICCD image focused by the SMT RC telescope from parallel beam (left). The x- and y-profile plots of image (right) are shown.

3 Performance of SMT readout

3.1 Integration test of SMT readout

We have tested the system and logic chain in order to validate their readout operation. During operation in space, the SMT readout is centrally controlled by the UDAQ, and receives the image along with the trigger signal from the trigger telescope. However, in the standalone test, the SMT electronics were interfaced directly with the computer by the USB-8451 based on a SPI communication and handled by the interface software.

Figure 9 shows the image read out by the ICCD using a parallel beam focused by the Ritchey-Chrétien (RC) telescope and slewing mirror. The parallel beam, which was collimated as ~ 4 arcsec in beam divergence, was focused onto the ICCD through the slewing mirror, and the result image shows the spread point of 3×3 pixels as the full width half maximum (FWHM). The results demonstrate that the SMT readout works properly and prove that the angular resolution requirements to the RC telescope are satisfied [7].

3.2 ICCD response measurement

We have measured the ICCD response for a light source of known intensity by adjusting the ADC gain to determine the dynamic range. To get uniformly scattered light, we used a 12 mm diameter integrating sphere. A 470 nm light source was employed, and the light from the integrating sphere was injected uniformly over the ICCD surface. We captured the ICCD images in a dark box using a standalone SMT readout with the ICCD gain set to 10^3 . Also, the intensity of the diffused light was measured by a photodiode and a power meter.

Figure 10 shows the ICCD response for a gain of 10^3 at a given light intensity. The plot shows the linearity of the ICCD response up to a light intensity of 800 pW. However, non-linearity is observed for intensities > 800 pW, and this indicates that the CCD charge capacity is reached and saturated for the current configuration of the ADC gain. The maximum charge capacity of the ICCD is 40,000 photoelectrons. Therefore, the 700 ADC count corresponds to 40,000 photoelectrons in

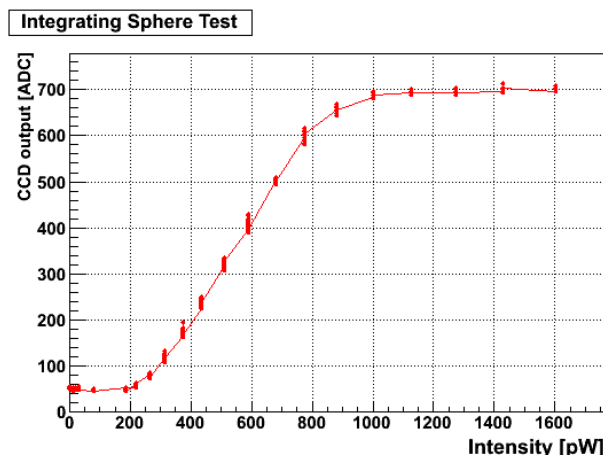


Figure 10. ICCD response to light intensity at a gain of 10^3 , with an integrating sphere used as a light source. The graph is divided into the linear range and non-linear range.

this measurement. The ICCD shows linearity up to 35,000 photoelectrons, which is about 85% of ICCD charge capacity. An ICCD with the gain of 10^3 cannot distinguish light measurements with intensities beneath 200 pW, which indicates a < 50 ADC count. The mean value of the ICCD readout noise is estimated to be 2,800 photoelectrons from the pedestal runs. The ADC range of the ICCD can be extended up to an ADC count of 1023 by re-setting the ADC gain achieve a wide dynamic range at the exact 10-bit resolution.

At gains above 10^4 , the ICCD operates in the photon counting mode. In this mode, the sensitivity is measured by counting the number of photons captured over the exposure time as indicated in table 1.

4 Space environment test

All telescope systems consist of space qualified components constructed with low-outgassing materials for greater reliability. All components must pass a shock-vibration test to be deemed capable of withstanding impact equivalent to a launch from ground and a space environment test including a thermal-vacuum test to qualify for operation in the extreme conditions above the atmosphere. The space environment test was performed at the National Space Organization (NSPO) facility in Taiwan.

The thermal-vacuum test consisted of subjecting the assembled SMT to four thermal cycles for 60 hours, at temperature ranges between -30 to 40°C under a vacuum pressure of 10^{-6} torr. The thermocouples were attached to all components subject to thermal effects, as shown in figure 11(a). The functional test was run before and after closing the vacuum chamber, and before and after each cycle. figure 11(b) shows the temperature profile for the SMT readout. The temperature profile determined for the readout in the chamber is nearly identical to that of its baseplate. The proximity of the SMT readout profile is close to the baseplate's indicates good thermal conductivity. The slow heat dissipation of the motors is also understandable because they are mounted on the gimbal structure. Furthermore, none of the electronics components were found to be burned or overheated during the testing, and the SMT readout demonstrated proper functionality throughout the tests.

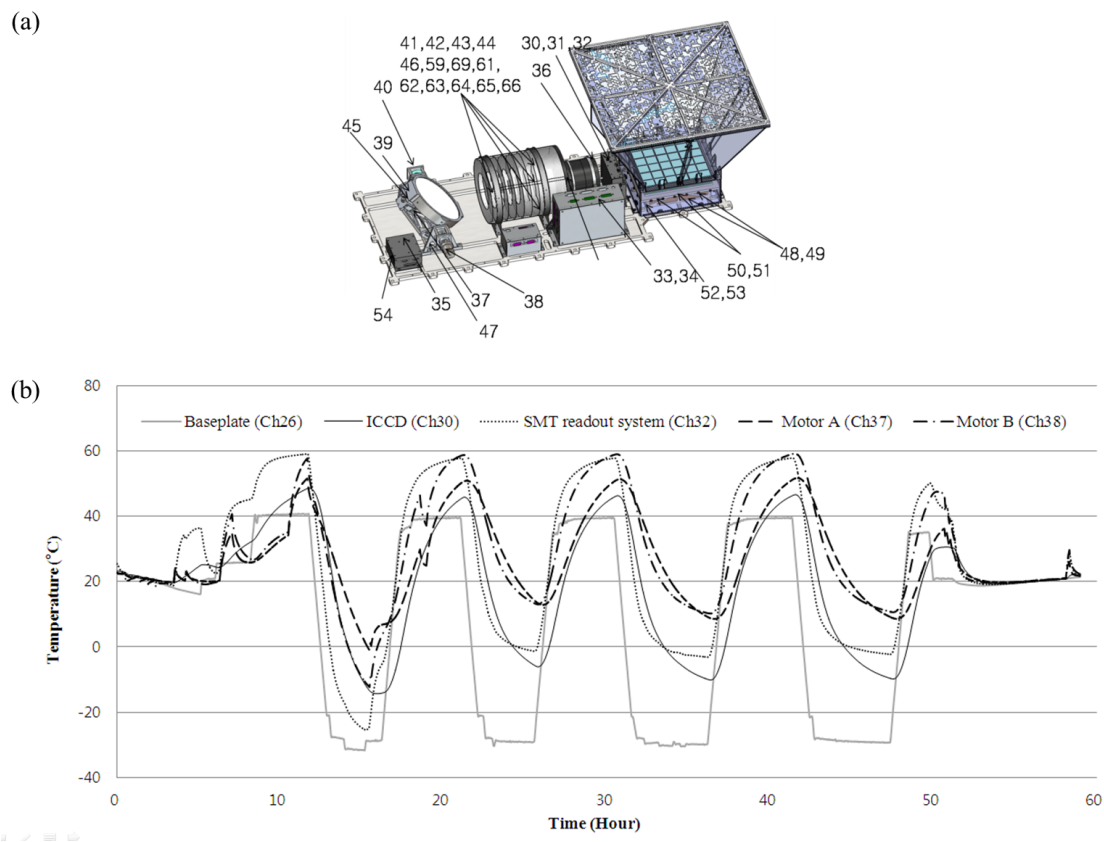


Figure 11. (a) Position of thermocouples for the thermal-vacuum test, (b) temperature profiles of baseplate, ICCD, SMT readout, and motors A and B. The fast temperature drop at 6 hours was caused by the CCD readout turning off.

Regarding the shock-vibration test results for the SMT readout, the important point is that the motors are aligned and that the ICCD's fiber coupling structure was not affected. An adaptor plate was installed for attaching the UFFO pathfinder to the shaker plate, and 31 accelerometers were installed to monitor the more vulnerable positions on the structure. As the shaking direction changed, the UFFO pathfinder's position on the shaker plate was changed as well. There were three main procedures: a sine wave vibration test, a random vibration test, and a shock test with amplitude of 45 g for 3 msec on the x-, y-, and z-axes. To check the results, and low sine wave vibration tests at 5–2000 Hz with acceleration loads of 0.3 g were undertaken before and after the shock-vibration tests. As indicated by the equivalent frequency responses recorded during before and after tests, no components were broken or damaged during the shock-vibration procedures. Additionally, the tested position where the resonance peaked for frequencies > 200 Hz during sine-wave vibration is strong enough to endure the shock and vibration during launch. As a result, the shock-vibration test was passed successfully, and we improved instrument safety without introducing any abnormalities to structural integrity [7].

5 Summary

The UFFO-pathfinder has been built to detect early photons from GRBs at the time scale of a couple of seconds for the first time. The payload is in its final stage of preparation prior to its launch aboard *Lomonosov* spacecraft later in 2013. The SMT is a key instrument of the UFFO-pathfinder for the rapid response in UV/optical observations. It is a 100 mm diameter modified RC telescope with a slewing mirror system and uses an ICCD as a photon detector. We have described the readout system of the SMT, covering data readout and system control.

The slewing mirror system, a novel feature of the SMT, is to find its first application in space. Another significant innovation is that the SMT's tracking and targeting are controlled by a FPGA without the inclusion of a CPU in the SMT readout. The slewing mirror has an accuracy of about 4 arcsec to its target, and it slews within 1.5 seconds. The ICCD, which has a gain of up to 10^6 , is designed and fabricated to observe faint UV/optical signals from the space. The ICCD is controlled and read out by the FPGA. Furthermore, the SMT readout has functions to control the SMT entire system including the slewing mirror, the adjustment of high voltage of ICCD, data acquisition and storage, data transfer and interface with UFFO Data Acquisition system (UDAQ), power distribution, and system monitoring. These functions are also developed in the FPGA to optimize the power consumption and the fast processing time.

We constructed all of the hardware and submitted the assembled device to a performance test. The SMT readout was designed and built within the constraints of the low power consumption, the limited instrument scale and the condition against the shock and vibration caused by launching and the operation under the large temperature variation and vacuum condition in the space in order to fulfil the requirements of space mission.

The SMT readout has been integrated and tested with the SMT optics system and the UFFO-pathfinder as well. We expect that the SMT will be able to detect early GRB emissions and, also, that it will be able to examine up to 15 triggered events per day to search for GRB candidates. We also expect that this new technology will provide a new data at of the early phase of GRB light curves, and thus enhanced understandings of GRB progenitors, central engines, radiation mechanisms, etc.

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