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SiC JFET Cascode Loss Dependency on the MOSFET Output Capacitance and Performance Comparison with Trench IGBTs

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Abstract— In power electronics there is a general trend to increase converters efficiencies and power densities; for this reason new power semiconductors based on materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) are becoming more popular. This is especially valid for renewable energies applications where the generated energy has a higher cost than with conventional energy sources. This paper proposes an experimental analysis of the switching performance of a high voltage SiC JFET connected in cascade connection with a low voltage MOSFET. The analysis focuses on the influence of the MOSFET output capacitance on the switching performance of the SiC Cascode connection in terms of switching energy loss, *dV/dt* and *dI/dt* stresses. The Cascode connection switching performances are compared with the switching performance latest Trench IGBTs. The analysis is based on a set of several laboratory measurements and data post-processing in order to properly characterize the devices and quantify whether the SiC JFET Cascode connection can provide good performances with a simple MOSFET gate driver.

I. INTRODUCTION

In the last years a large growth of power electronics has been experienced mainly driven by the huge interest in renewable energy sources and smarter energy use. Moreover, in many applications there is and increasing trend to improve systems efficiencies supported by state policies and by economical benefits.

Silicon Carbide (SiC) together with Gallium Nitride (GaN) have been known to be attractive wide band gap semiconductors especially suited for increasing the efficiency and power density of switch mode power supplies (SMPS) compared to silicon (Si) based SMPS [1]. They have the potential of providing power semiconductors characterized by high band-gap, higher mobility and higher thermal conductivity than Si, leading to lower conduction and switching losses, higher breakdown voltage, possibility to operate at high temperatures, increased switching frequency and power density.

The recent improvements in the crystal fabrication, fabrication yield increases and availability of new low-cost power devices based on SiC have made SiC-based power semiconductors more competitive [2][3]. However, there are still a limited number of power semiconductors available in SiC; they are limited to SiC Schottky barrier diodes, SiC Junction Effect Field Transistors (JFETs) available in both normally-on and normally-off variants, SiC Bipolar Junction Transistors (BJTs) [4] and recently SiC Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) [5][6].

SiC-diodes have become price competitive as Si-diodes; SiC-diodes are often used as replacement of Si-diodes in applications characterized by high efficiency and high voltage due to their almost zero-recovery losses at device turn-off [7]. SiC JFETs have really become price competitive and they can provide very low switching losses and low on-state resistance [8]. The main drawbacks related to the use of SiC JFETs are related to the driving circuitry: SiC JFETs are voltage driven devices with threshold and driving voltages that differ from Si-MOSFETs. Moreover, SiC JFETs require a low continuous power from the driver (high leakage current) and therefore they do not represent a direct and easy replacement for Si-MOSFETs or Silicon Insulated Gate Bipolar transistors (Si-IGBTs). The driver complexity [9] and the limited the availability of commercial drivers suited for Si-JFETs also contribute to limit the device diffusion in different applications. The driver issue in terms of continuous power from the driver is even worse for SiC-BJTs moreover, the limited availability of SiC-BJTs have also reduced their success. During 2011, SiC-based MOSFETs has been released thorough commercial channels [5]; the devices have with similar ratings as SiC JFETs promising good performance making the devices suited for significantly increase the switching frequency and the power density of power electronics converters. However, also in this case to properly take advantage of the new device a custom designed driver is required and it will probably limit the device diffusion due to the lack of commercial available drivers.
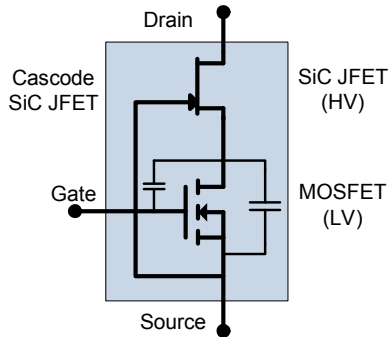
Fig. 1 High voltage (1200 V 85 mOhm, normally ON) SiC JFET in Cascode connection with a low voltage (60 V 1.5 mOhm) MOSFET showing the MOSFET's output capacitances .

Fig. 2 Inductive clamp test circuit. Highlighted in green the leakage inductance critical loop.

One common solution for easily driving SiC JFETs require using a low voltage MOSFET series connected with the SiC JFET in a Cascode connection [10]. The Cascode allows creating a high voltage valve that can be easily driven with a simple and commercially available MOSFET driver. The main drawbacks of the solution are that requires an additional low-$R_{DS,on}$ MOSFET which increases the conduction losses and has a tendency to oscillations especially at turn-off increasing the overall switching losses.

This paper focuses on performing an analysis based on experimental results of the influence of the low voltage MOSFET's output capacitance on the switching performance of the SiC JFET Cascode configuration. The analysis focuses on switching energy loss, transition times and maximum stresses in terms of *dV/dt* and *dI/dt*. Moreover, the paper also presents a comparison of the switching losses of the Cascode SiC JFET configuration with the switching performance of recent Trench IGBTs with similar ratings as the Cascode. The typical application is a 5 kW DC/DC isolated boost converter for fuel cell where the low voltage (~50 V) primary stage is designed based on MOSFETs and the high voltage (700-800 V) stage is designed based on IGBTs or SiC devices.

II. JFET CASCODE CONFIGURATION

The circuit showing the SiC normally-on JFET in Cascode connection with a low voltage MOSFET is presented in Fig. 1. The Cascode connection allows using normally-on JFETs for creating normally-off valves which are desirable in many applications where in case of failure on the gate driver a normally-on valve would create a critical and dangerous
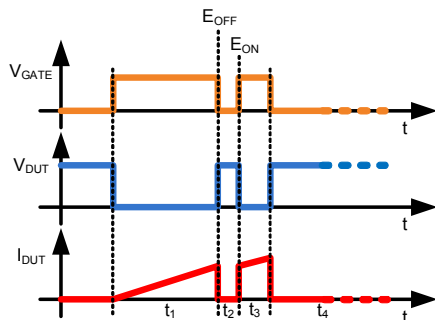
condition (e.g. short-circuit in a voltage source converter). The scalability of the Cascode connection has also been proven [11] making the Cascode connection a possible candidate for realizing high voltage SiC switches.

When the voltage applied to the MOSFET gate-source is below the MOSFET's threshold, the valve is in off-state or blocking mode. The gate of the JFET is connected to the source of the MOSFET; when a low voltage is applied across the valve drain-source the MOSFET will support most of the voltage but as soon and the voltage over the valve is increased the JFET becomes pinched off and it will support most of the voltage. The valve can be turned on by applying a voltage greater than the MOSFET's threshold across the MOSFET's gate-source. As soon as the MOSFET turns on it will subsequently, the voltage applied to the JFET's gate-source will become low turning on the JFET. In this case the JFET's turn-on/turn-off are delayed compared to the MOSFET's turn-on/turn-off.

III. SETUP CONFIGURATION AND TESTED DEVICES

The test setup is a simple pulse clamped inductive circuit shown in Fig. 2. The inductive provides an easy way to test power devices up to their nominal ratings without heating them up. To perform this, the Device Under Test (DUT), is turned on for a small time interval, during this interval the current through the load inductor (L) builds up and the desired value is reached, the DUT is turned off (Fig. 3). At this interval is possible to measure the device switching losses for the selected current value. Immediately after that the device has been turned it is possible to turn it on again. When the
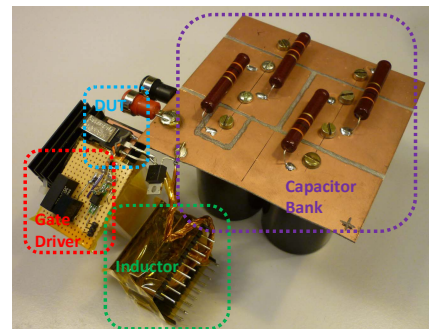

Fig. 3 Ideal double pulse testing waveforms.

Fig. 4 Hardware used for the tests. Highlighted the capacitor bank, the inductor, the gate driver and the DUT.

TABLE I
TESTED DEVICE CHARACTERISTICS

JFET SJDP120R085	MOSFET IPB017N06N3	IGBT no.1 IGW15N120H3	IGBT no.2 IRG7PH30K10
1200 V	60 V	1200 V	1200 V
85 mOhm	1.7 mOhm	2.05 Vce	2.05 Vce
27 A*	180 A*	30 A*	33 A*
17 A**	180 A**	15 A**	23 A**

*Parameter at 25 ° C
**Parameter at 100 ° C

device off-time is sufficiently low, the inductor current decay is small (the inductor discharges slightly through its resistance and through the freewheeling diode) and allows turning on the DUT for measuring a turn-on event at the same current level as the turn-off event. After this second turn-on event the device is switched off permanently and kept in off state until the inductor is completely discharged. After that it is possible to vary the first pulse width to increase or reduce the desired current and at which the measurement should be performed.

The test setup (Fig. 4) characteristics are summarized:

- DC voltage source: 700 V

- Capacitor bank: 1000 V 300 μF

- Load inductor: 285 μH

- Freewheeling diode: SiC 1200 V 20 A

A. Tested Devices

The paper focused on analyzing devices with similar characteristics in order to establish references for converters with DC voltages of 700-800 V. At this voltage levels CoolMOS provide a limited voltage margin (available up to 900 V) and their on state resistance is significantly high compared to SiC devices or Si IGBTs. Since for the candidate application efficiency is one of the most important factors, 1200 V SiC JFETs (SJDP120R085) were one of the first candidates for achieving high efficiency. Alternatively, 1200 V SiC MOSFETs could have been used however, the price performance ratio of the SiC JFET looked well application-suited. The low voltage MOSFET was selected due its very low on resistance (IPB017N06N3) that would give a minimum impact on the total on state resistance of the Cascode connection. The large availability of IGBT devices in the 1200 V range made the selection of IGBTs more complex. However, among all, trench IGBTs can provide both fast switching with limited tail current and low $V_{CE,on}$. The selected devices have similar current ratings as the selected SiC JFET and are produced by two different manufacturers identified as IGBT no.1 (IGW15N120H3) and IGBT no.2 (IRG7PH30K10) in the measurements and in the comparison plots. A summary of the main device characteristics is presented on Table I.

B. Instrumentation and Measurements

All measurements were performed with the comparable test conditions in terms of voltage, current, time intervals and temperature. The power connection from the DC-link capacitor to the power components was realized with flat copper conductor to obtain as low inductance as possible as visible on Fig. 4. The gate driver was placed close to the DUT, the wires were twisted in order to reduce the loop inductance and it was connected to a digital control card used to generate test pulses. The minimum resolution of the pulses is 1 μs with a basic accuracy of 0.25 μs. The digital control card ensured test repeatability having well defined pulses width for each current level. All measurements were performed with the same probe configuration with an exception for the IGBT measurements where there was no MOSFET's drain-source voltage measurement.

The oscilloscope features allow saving measurements directly in Matlab format for post-processing. The oscilloscope configuration was the following (examples of measured switching transients on Fig. 5):

- Ch.1: DUT source/emitter current. Current probe is a ultra miniature Rogowsky coil with a bandwidth of 20 MHz (20mV/A) measuring the Cascode source current excluding the gate driving current.

- Ch.2: Gate-source/gate-emitter voltage of the Cascode configuration/IGBTs; 100 MHz 1X voltage probe.

- Ch.3: DUT drain-source/collector-emitter voltage. High voltage probe 100X (LeCroy PPE 4 kV) measuring the Cascode drain-source voltage.

- Ch.4: drain-source voltage of the low voltage MOSFET in the Cascode configuration;100 MHz 1X voltage probe. Not used with IGBT's.
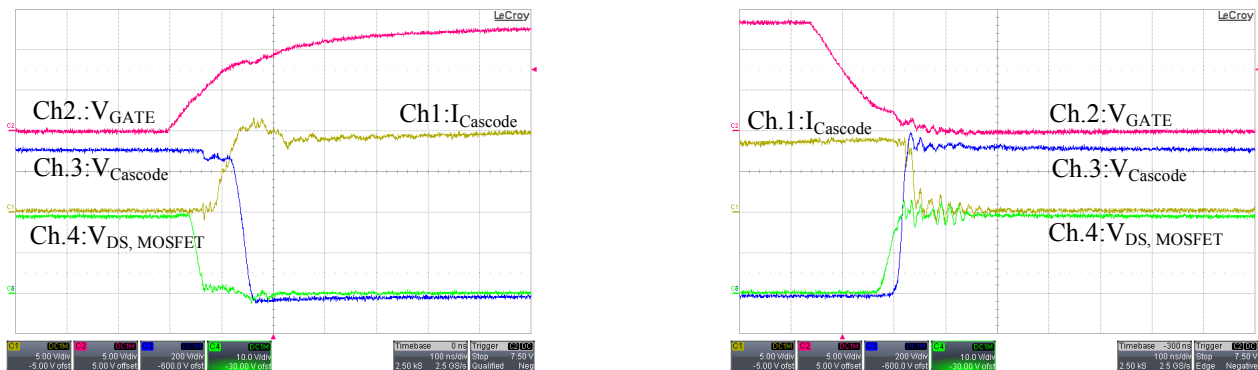

Fig. 5 Cascode JFET measured turn-on (left) and turn-off (right) detail 700 V 9 A, MOSFET gate resistance 2.5 ohm. Ch.1: 5 A/div, Ch.2: 5 V/div, Ch.3: 200 V/div and Ch.4: 10 V/div, time: 100 ns/div.
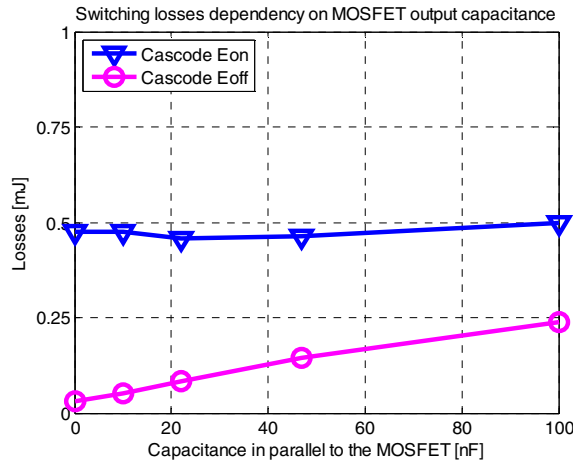
Fig. 6 Cascode switching loss dependency on MOSFET's output capacitance.

Fig. 7 Cascode *dV/dt* stress dependency on MOSFET's output

The Rogowsky coil delay was measured in a reference comparison measurement with a shunt resistor where it was quantified in 24 ns; this value is verified also in probe manual. The oscilloscope features de-skew compensation, however, this was not used but implemented digitally during data post-processing. Measurements were performed at different current levels (from 5 A to up to 20 A) for the selected DC voltage (700 V).

C. Methodology and Data Post-Processing

The first set of measurements focused on analyzing the effect of the MOSFET output capacitance on the switching performance of the Cascode configuration. The main focus was to observe if it is possible vary the switching performance with simple low voltage components instead of using components rated at high voltage [11]. To simulate a large MOSFET's output capacitance, additional capacitors of different values (0-100 nF range) were added in parallel to the low voltage MOSFET used in the Cascode connection. The capacitors were connected directly on the MOSFET's leads in order to reduce the leakage inductance to the minimum and to avoid possible unwanted oscillations. In the second step, the switching performance of the Cascode valve were measured at different current levels and as last phase the Cascode valve was replaced with the selected IGBTs for characterizing their switching performance.

All measured waveforms were stored in MATLAB format in order to allow post-processing of the measurements and create adequate plots. Light filtering was applied to the measurements for reducing the measurement noise; after filtering the waveforms were verified to ensure that the filtering process did not change the measurement information. MATLAB functions were developed for extracting the desired information from the measurement files, such as switching energy loss, the transition intervals (turn-on and turn-off times), the voltage and current stresses in terms of *dV/dt* and *dI/dt* and instantaneous peak power loss.
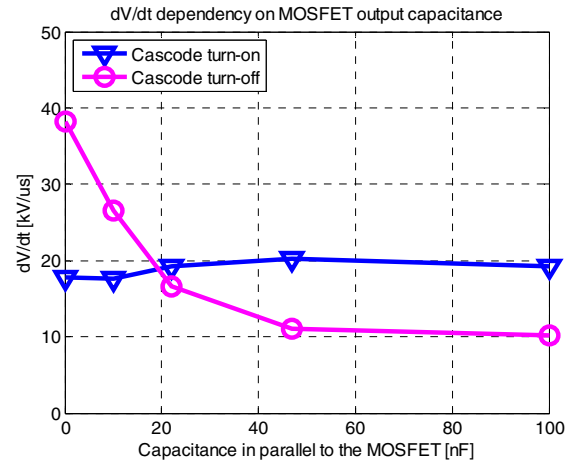
IV. CASCODE SWITCHING LOSS DEPENDENCY ON MOSFET'S OUTPUT CAPACITANCE

In the first set of measurements the switching losses of the Cascoded devices are measured by varying the MOSFET's output capacitance for a fixed current (9 A). For reasonably low additional capacitances (0-100 nF range) the turn-on losses have a minimal dependency on the MOSFET's output capacitance as observed in Fig. 6. In this case, at the Cascode turn-on the MOSFET's delay and switching speed determine the turn-on instant of the JFETs. The turn-off losses on Fig. 6 increase more than the turn-on losses, in fact as the MOSFET's output capacitance increases, the turn-off losses increase with a linear trend. This could be explained by analyzing the Cascode configuration a bit more in detail.

At device turn-on the MOSFET's output capacitance discharges through the low ohmic low voltage MOSFET and the voltage change across the JFET's gate-source (also output capacitance terminals) varies as in a capacitor discharge through a resistor with the RC-time constant defined by the MOSFET's output capacitance and the MOSFET's on-state resistance.

Vice versa, at device turn-off the MOSFET's output capacitance is slowly charged through the JFET's on-state resistance; at the start of the JFET's turn-off process the
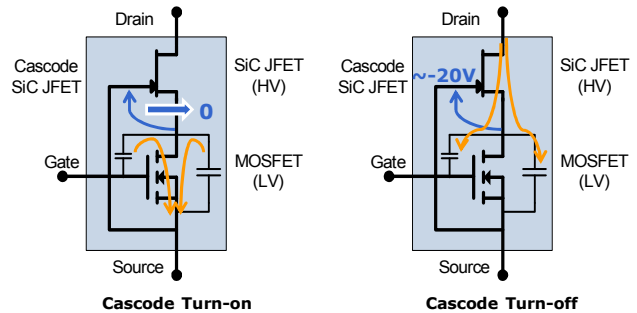

Fig. 8 Cascode turn-on (left) and turn-off (right) transients. Highlighting charge/discharge of MOSFET's output capacitance.
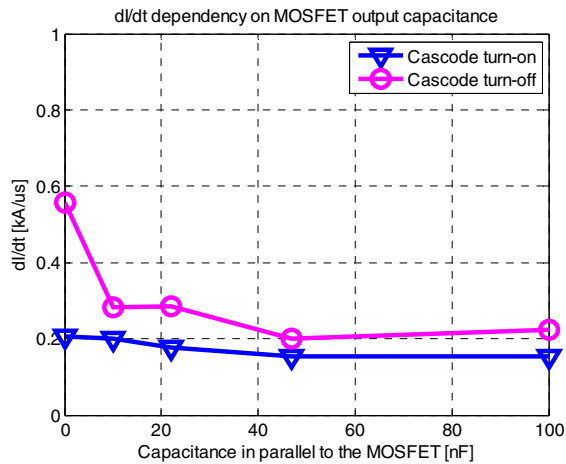
Fig. 9 Cascode *dI/dt* stress dependency on MOSFET's output capacitance.

Fig. 10 Cascode turn-on and turn-off times dependency on MOSFET's output capacitance.

voltage rises over the MOSFET with an initial RC time constant defined by the JFET's on state resistance and the total output capacitance. As soon as the voltage over the MOSFET's start to increase, the JFET's on resistance increases giving an additional contribute to the JFET's turn-off losses until the JFET becomes completely pinched off. For this reason, an increase of the MOSFET's output capacitance slightly influences the Cascode turn-on performance and will strongly influence the turn-off performance.

This effect is also observed in the *dV/dt* stress at device turn-on and turn-off on Fig. 7. The *dV/dt* stress at turn-on is slightly influenced by the MOSFET's output capacitance while the *dV/dt* stress at turn-off is significantly reduced with a large MOSFET's output capacitance. The *dV/dt* stress reduction at turn-off is large, in fact the *dV/dt* stress is reduced from 38 kV/us down to 10 kV/us with the largest tested capacitance value. According to the measurement a small capacitor can be placed on parallel to the low voltage MOSFET to reduced the turn-off *dV/dt* and balance it with the turn-on *dV/dt* reducing the immunity requirements for the
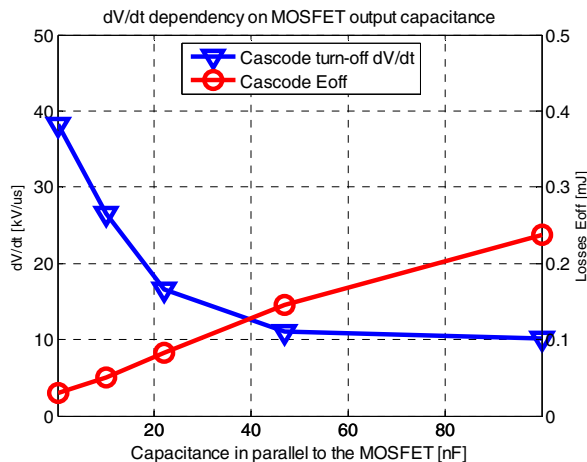
gate driver. However, it is also necessary to observe how other parameters are affected by a large MOSFET output capacitance.

It is also interesting to observe how the *dI/dt* stress varies as a function of the MOSFET's output capacitance. On Fig. 9 it can be observed that the turn-on *dI/dt* has a light variation (small reduction), however, large output capacitance mainly influences the turn-off *dI/dt*. This stress can be reduced down to about 33% or the initial value. Therefore, it can be deduced that a large MOSFET's output capacitance can reduce both *dV/dt* and *dI/dt* at turn-off. This result is also confirmed by taking a look at the transition times (turn-on and turn-off times) of the Cascode configuration on Fig. 9.

It was observed that in the Cascode configuration, the turn-on losses are dominating over the turn-off losses (Fig. 6 700 V 9 A); by increasing the MOSFET's output capacitance the Cascode turn-off time increase as seen in Fig. 11. Therefore, it is possible to find a balance between the turn-on *dV/dt* and the turn-off *dV/dt* with a slight increase of switching losses (Fig. 11). Depending on the application and on the desired performances in terms of switching losses and maximum *dV/dt* and *dI/dt* stresses, this could be advantageous for reducing the immunity requirements of the gate driver which are normally very high (recommended immunity for SiC gate drivers is about ~50 kV/us).

V. COMPARISON OF THE SWITCHING LOSSES OF SiC CASCODE WITH Si IGBTs

In multi-kW applications with DC-link voltage level of 700-800 V SiC normally-on JFET in Cascode connection with a low voltage MOSFET has to be compared with newly developed high speed trench IGBTs which, especially for the latest series (3rd generation); these devices can provide very low $V_{CE,sat}$ and low switching losses (or operation up to ~100 kHz). The IGBTs switching performance were measured with different gate resistors values; starting with a large values as used in their datasheets (e.g. 35-22 Ohm), down to a very low values (2.5 Ohm). To analyze the switching performance, the turn-on and turn-off losses are analyzed independently for IGBT no.1 and IGBT no.2. Subsequently, the total switching
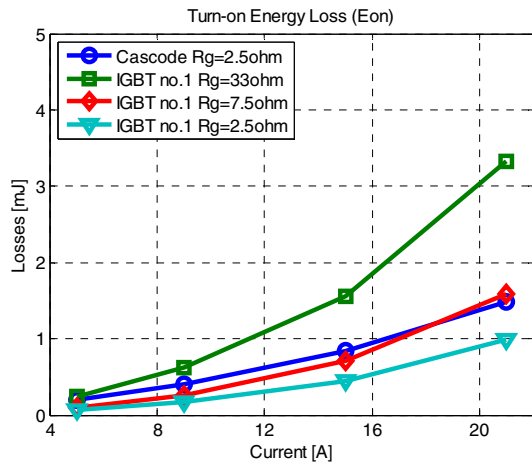

Fig. 11 Cascode turn-off switching loss and *dV/dt* dependency on MOSFET's output capacitance.

Fig. 12 IGBT no.1 and Cascode turn-on energy loss.

Fig. 13 IGBT no.1 and Cascode turn-off energy loss.

losses are analyzed in comparison with the Cascode configuration.

IGBT no.1 is a fast switching IGBT (IGW15N120H3) rated for operation up to 100 kHz; its turn-on and turn-off switching losses are presented on Fig. 12 and Fig. 13 respectively. When the IGBT is operated with large gate resistors as characterized in the datasheet, the switching losses losses are significantly higher than the SiC Cascode configuration. However, by reducing the gate resistor the turn-on losses are significantly reduced. With a minimum gate resistor the reduction can be down to 33% of the losses specified in the datasheet. The performance achieved in terms of turn-on losses are also better than the ones obtained with the SiC Cascode. Vice versa, the IGBT turn-off losses are independent form the gate resistance and vary linearly with the device current (Fig. 13). The turn-off losses are always larger than the SiC Cascode turn-off due to the IGBT tail current.

In a similar way the switching losses of IGBT no.2 are compared with the switching losses of the SiC Cascode on Fig. 14 and Fig. 15. The measured turn-on losses of IGBT no.2 are significantly lower than the ones measured for
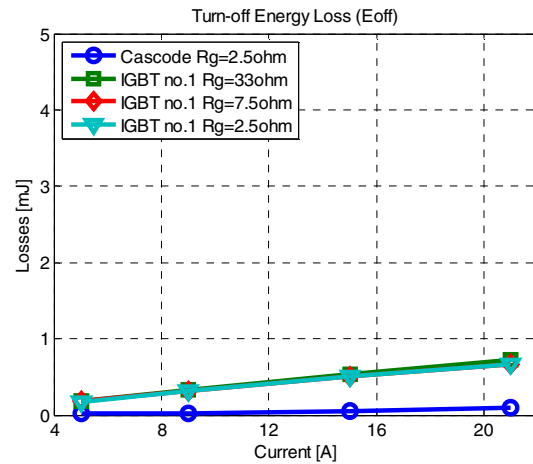
IGBT no.1 (Fig. 12 and Fig. 14) for large gate resistor values. Also in this case, with reduced gate resistors compared to the value specified in the datasheet, it is possible to reduce the IGBT turn-on losses even lower than the turn-on losses of the SiC Cascode. The turn-on losses with low gate resistors become lower than the SiC Cascode for all measured current levels. As observed in the previous case, the IGBT no.2 turn-off losses are almost not influenced by the reduction of the gate resistance and, also for this case, their value is significantly larger than the SiC Cascode turn-off losses for the entire range of tested currents. Therefore, it is observed that even though latest generation of trench IGBT have very low switching losses, the tail current is still one of the main sources of turn-off losses in IGBTs.

As observed until now is clear that when IGBTs are used up to their boundaries in terms of switching speed, they can provide good performances even in comparison to the new power semiconductors based on SiC. It is required to analyze the total switching losses (both turn-on and turn-off energy loss) to evaluate the overall performance of the devices. To achieve a complete comparison the total losses (turn-on and
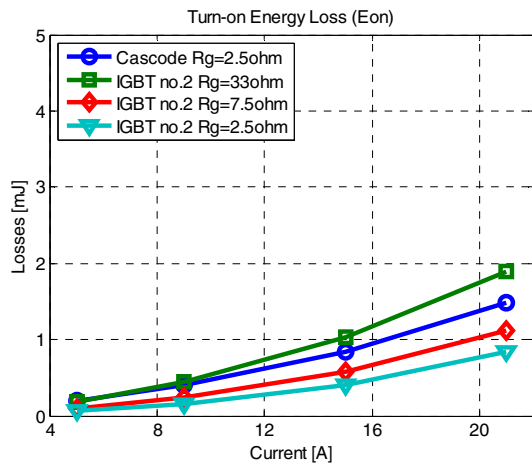

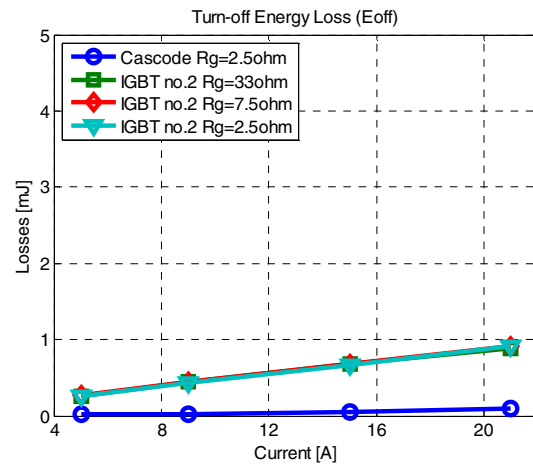Fig. 14 IGBT no.2 and Cascode turn-on energy loss.

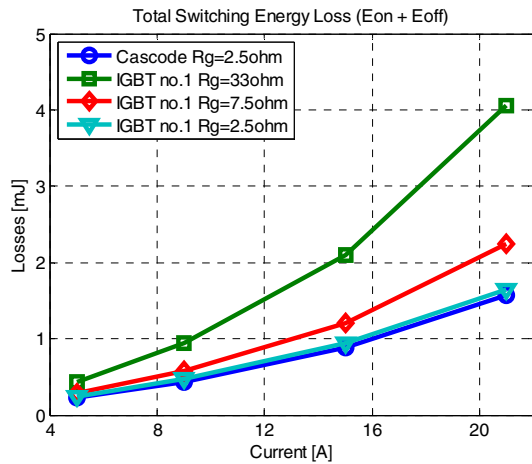Fig. 15 IGBT no.2 and Cascode turn-off energy loss.

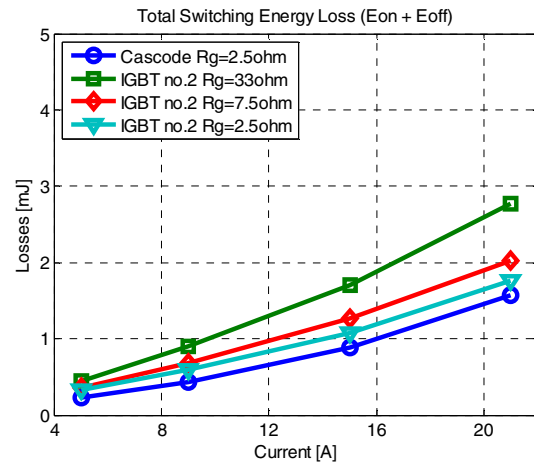Fig. 16 IGBT no.1 and Cascode total switching energy loss.

Fig. 17 IGBT no.2 and Cascode total switching energy loss.

turn-off) have to be evaluated.

A comparison of the total switching losses of IGBT no.1 with SiC Cascode and IGBT no.2 with SiC Cascode are presented on Fig. 16 and Fig. 17 respectively. Both IGBTs types are rated for high-speed (IGBT no.1 up to 100 kHz and IGBT no.2 up to 30 kHz), however, it is observed that IGBT no.1 has higher switching losses compared to IGBT no.2 when this ones are used with the gate resistors specified in the datasheet, this is observed especially at high current values (above 10 A). In both IGBTs it is possible to significantly reduce the total losses by decreasing their gate resistor to a very low value. In this case the energy loss reduction in IGBT no.1 is larger compared to IGBT no.2. The IGBTs switching performance can be increased to a level where the energy loss during the switching transient is very close to the one observed for the SiC Cascode (Fig. 16).

VI. CONCLUSIONS

The paper presented the effects of increased MOSFET's output capacitance on the switching behavior of the Cascode configuration.

It was observed that in the Cascode configuration the turn-off dV/dt stress can be significantly reduced with a limited increase of the switching losses by a larger MOSFET's output capacitance; e.g. by adding an additional capacitor in parallel to the MOSFET. The additional capacitor influences mainly the turn-off losses with little influence on the turn-on losses.

The Cascode configuration was characterized in terms of switching losses and compared with newly 3rd generation trench IGBTs. This latest IGBTs proved to be very competitive also towards SiC devices in the multi-kW power range. In fact, when IGBTs are switched very fast the measured switching losses are very close to the switching losses of a SiC Cascode configuration. Undoubtedly, pure SiC power devices provide lower losses, however, there is still a big lack of available integrated gate-driver solutions for these devices. For this reason, the Cascode configuration or latest IGBT generations are still very appealing for many applications.

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