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Preface

This thesis is submitted in partial fulfillment of the requirements for obtaining the PhD degree at the Technical University of Denmark, DTU Elektro, Electronics Group. The work was carried out during the period from May 2009 until May 2012 and was supervised by Professor Michael A. E. Andersen and Associate Professor Ole C. Thomsen at the Technical University of Denmark. The work was supported by the Danish National Advanced Technology Foundation (Højteknologifounden - HTF) under the project number HTF-008-2008-3. The work was conducted as part of a joint research cooperation between the industrial companies Danfoss PolyPower A/S and Noliac A/S.

Acknowledgment

During this PhD, I have become deeply indebted and grateful to all of those who have supported and helped me throughout this project. My special thanks, love and appreciation goes to:

- My dear family and friends for their love and never ending support, tolerance and endurance during this project.
- My supervisors, Michael A. E. Andersen and Ole C. Thomsen for giving me this opportunity and their support, encouragement, and endless confidence in me.
- All of my colleagues for their help, support, and constructive discussions.

Abstract

This work focuses on the development of a driver for a special type of actuators: "dielectric electro active polymer" (DEAP) also known as artificial muscles. The task of the driver is to transform a low voltage of 24 volts up to high voltages around 2500 volts which are needed to drive these types of actuators. The size of the driver is essential for the project as one of the major goals is to integrate the driver into a DEAP actuator. To further increase the competitive areas of DEAP actuators a nonmagnetic driver solution is required to ensure a full functionality when exposed to high magnetic fields. A driver solution based on a piezoelectric transformer is presented.

An introduction to piezoelectricity with the aspect of piezoelectric transformers is given together with a more visual understanding of the concept of electromechanical coupling in relation to the issue of zero voltage switching (ZVS). Different piezoelectric transformer designs have been simulated and optimized using a FEM tool. Prototypes of the different transformer designs have been manufactured, tested and evaluated. The end result is a tape casting compatible piezoelectric transformer with interleaved structure and interdigitated electrodes (IDE) to obtain a low profile and high efficiency thickness mode design optimised for zero voltage switching.

A compact driver solution is designed based on the developed piezoelectric transformers. The highly resonance nature of a piezoelectric transformer is also its key to high efficiency. But in combination with a temperature drifting resonance the efficiency is easily lost if the control system is not able to adapt to it. A novel self-oscillation control is invented to ensure stability and high efficiency. The developed driver was successfully integrated into a DEAP actuator. As a result the high voltage interface of the actuator was avoided and the world's first low voltage DEAP was created.

In an attempt to further increase the total systems efficiency a bidirectional driver was developed. The invention of active phase-shift control made it possible to reverse the energy flow of the piezoelectric transformer and still maintain zero voltage switching to keep the efficiency high, despite the fact that the piezoelectric transformer by itself can only zero voltage switch in one direction. As a result the total system efficiency is more than doubled with the prototyped bidirectional driver.

Dansk resumé

Dette arbejde fokuserer på udviklingen af en driver til aktuatorer af typen: "dielektrisk elektro aktiv polymer" (DEAP) også kendt som kunstige muskler. Driverens grundlæggende funktion er at transformere en lav spænding på 24 volt op til en høj spænding omkring 2500 volt, hvilket er krævet for at drive denne type aktuator. Den fysiske størrelse af driveren er af afgørende betydning eftersom et af hovedmålene for projektet er at integrere driveren ind i DEAP-aktuatoren. For yderligere at øge konkurrenceevnen for DEAP aktuatorer er det et krav at driveren er uden magnetiske komponenter, derved sikres fuld funktionalitet i omgivelser med høje magnetfelter. En løsning baseret på en piezoelektrisk transformer præsenteres.

Der gives en introduktion til piezoelektricitet med udgangspunkt i piezoelektriske transformere samtidig med en visuel forklaring af konceptet elektromekaniske kobling og dens sammenhæng med *nul-spændings-skiften* (ZVS). Forskellige piezoelektriske transformerdesigns er blevet simuleret og optimeret ved hjælp at finite element method (FEM) værktøj. Prototyper af forskellige designs er blevet fremstillet, testet og evalueret. Slutresultatet er en piezoelektrisk transformer, der bygger på en indflettet struktur samt et specielt elektrode mønster (IDE), for at opnå et lav-profil design med højeffektiv tykkelses-vibration der er optimeret for ZVS.

En kompakt driverløsning er blevet designet baseret på de udviklede piezoelektriske transformere. Den meget resonerende natur af piezoelektriske transformerer, er også nøglen til dens høje effektivitet. Men resonansen flytter sig bl.a. med temperaturen og derfor kan den høje effektivitet nemt tabes, hvis kontrolsystemet ikke er i stand til at spore denne ændring. Et nyt selv-oscillerende kontrolsystem er opfundet for at sikrer en stabil og høj effektivitet. Den udviklede driver er succesfuldt blevet integreret med DEAP-aktuatoren. Dermed er højspændingsproblematikken omkring DEAP-aktuatorer blevet fjernet og verden første lavspændings DEAP-aktuator er realiseret.

I et forsøg på yderligere at øge effektiviteten af hele systemet, er en bidirektionel driver udviklet. Med opfindelsen af aktivt-fase-skift-kontrol er det blevet muligt at vende energistrømmen gennem den piezoelektriske transformer uden at miste ZVS og derved beholde den høje effektivitet. Dette er vel og mærket selvom den piezoelektriske transformer i sig selv kun er i stand til at opnå ZVS i én retning. Systemets totale effektivitet er derved mere end fordoblet med den bidirektionelle driver.

Table of contents

Chapter 1: Introduction

1.1 Scope

The scope of this thesis is to present the research work obtained in the PhD project "*Piezoelectric transformer based power supply for dielectric electro active polymers*" carried out during the period from May 2009 through May 2012. Many of the scientific results of the research have been published in form of peer reviewed conference papers, journal paper and patent applications. The published papers form an integral part of this thesis and are included in appendix A.

The objective of this thesis is to supplement the already published information and thereby present a more coherent and complete overview of the research work and results obtained in the project.

Furthermore, the thesis is written with readers new to the field of *artificial muscles*, *piezoelectricity* and *piezoelectric transformers* in mind. However this thesis is not meant to stand alone and it is expected that references are read whenever the reader needs additional information.

1.2 Thesis structure

The structure, organization and content of the thesis are visualized in figure 1. The figure illustrates the flow through the chapters of the thesis. The amount of green color indicates the novelty of which this project has contributed to. Frame colored boxes are related to work and methods already familiar from other publications or research fields but adapted and applied in a new and different way. Full colored boxes are directly related to new and revolutionary knowledge especially for the field regarding piezoelectric transformers. Chapters and sub-chapters are linked with the associated peer reviewed conference papers, journal paper and patent applications submitted along the period of the project. These publications are indicated with blue framed boxes and are all located in appendix A.

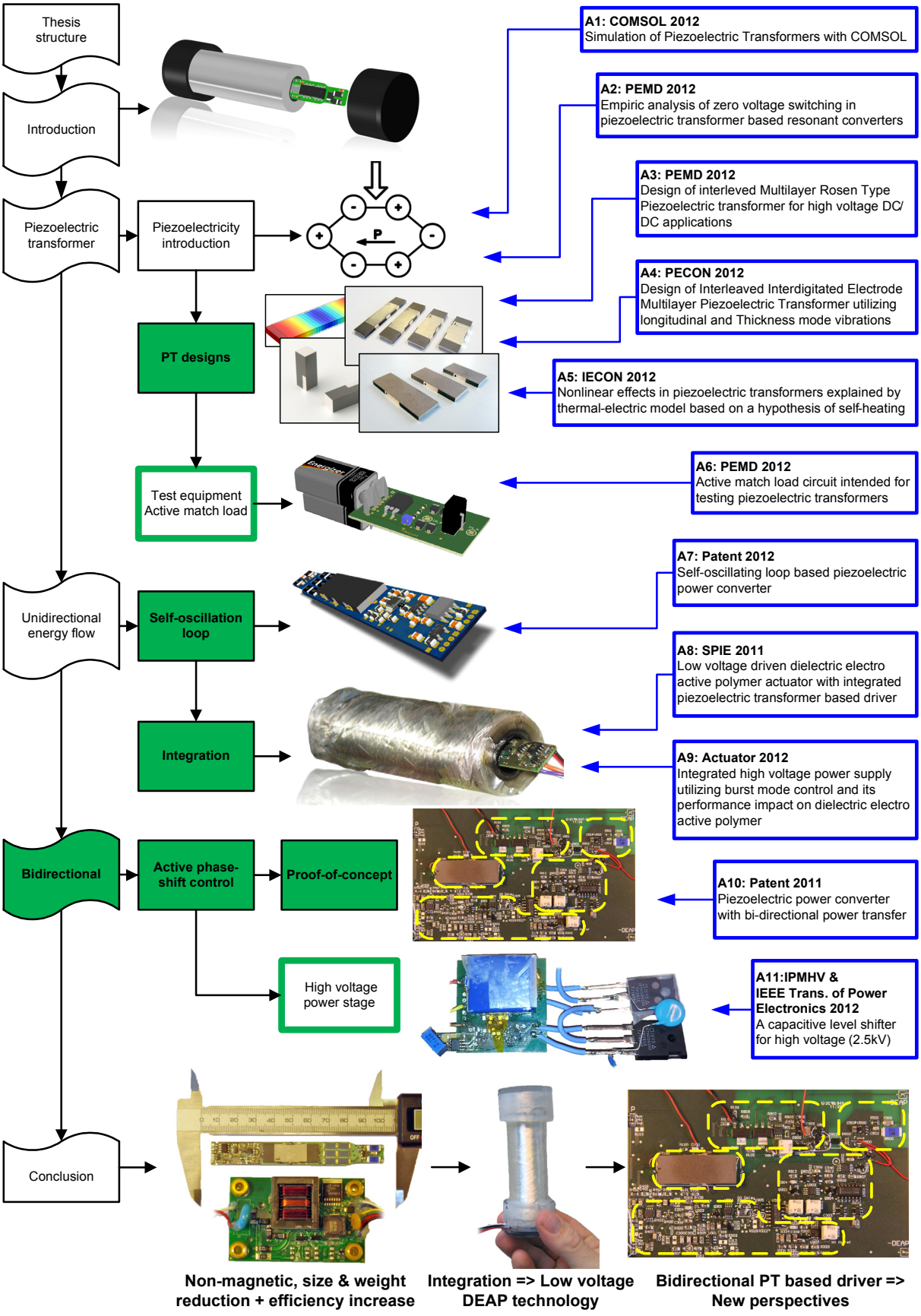


Figure 1: Thesis structure. Novelty of chapters and sub-chapters are indicated with green color. Blue boxes indicate publications and are linked to the associated chapters.

1.3 Background

1.3.1 Dielectric Electro Active Polymer

The dielectric electro active polymer (DEAP) technology, often called "artificial muscles" [1], utilizes the electrostatic force between two electrodes to compress an intermediate polymer material. For a polymer material of constant volume the induced electrical force is converted to stress perpendicular to the direction of contraction [2]. The in-plane expansion of the polymer material from the induced stress depends on the counter-forces from the polymer and the electrodes. For the PolyPower [3] film the surface of the polymer material is corrugated on a micrometer scale, this allows nanometer thin metal coated electrodes to undergo in-plane expansion without damaging the conductivity [4]. Furthermore, the surface is corrugated in only one direction to obtain anisotropic properties of the polymer material; in the direction of corrugations the compliance is increased and in the transverse direction the stiffness is increased. Figure 2 illustrates the corrugated shape of the electrodes and polymer material [2].

As a consequence the combination of corrugated and anisotropic leads to a large actuation strain of the DEAP film when compressed by an electrostatic force. This makes the PolyPower DEAP film suitable for e.g. actuator applications. Winding the DEAP film in a cylindrical shape creates a tubular actuator. The anisotropic DEAP film is winded with the compliant direction along the axial axis. The principle of the tubular DEAP actuator is illustrated in figure 3.

The tubular shape ensures a self-supported structure capable of providing a pushing

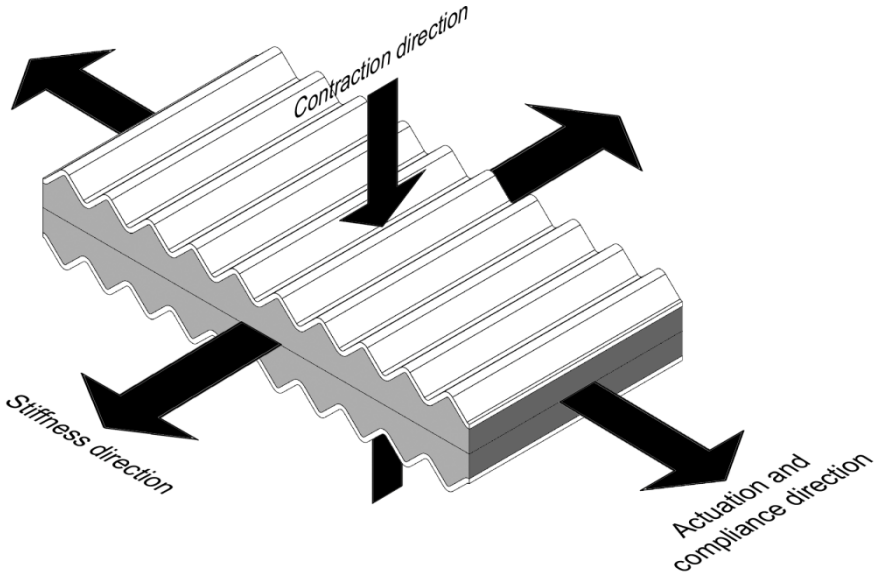


Figure 2: Corrugated shape gives the DEAP film anisotropic properties and allows metal coated electrodes to undergo in-plane expansion.

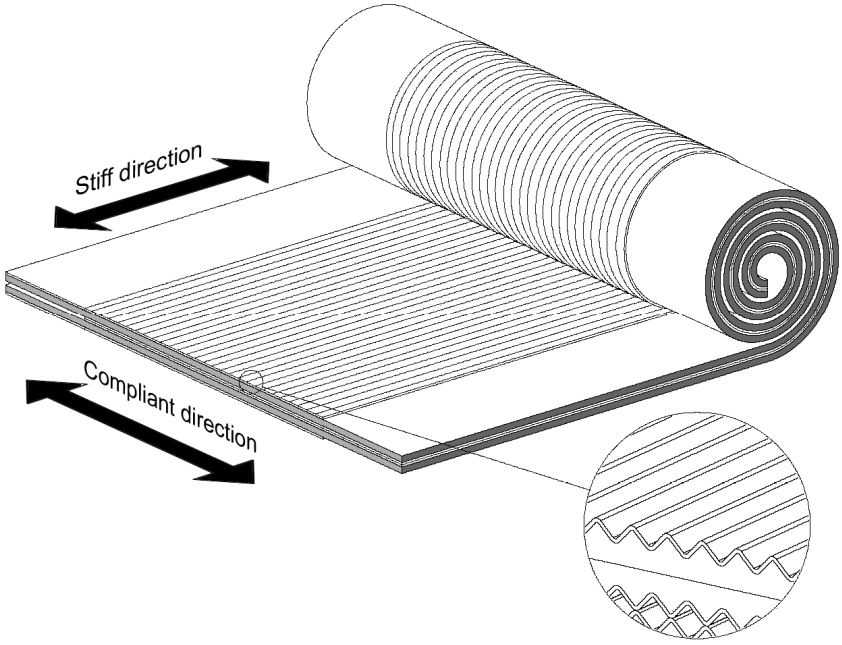


Figure 3: Concept of a tubular DEAP actuator utilizing corrugated film.

force without external mechanical mechanisms of film pre-strain [5]. Blocking force is scaled with number of winding turns. The actuator strain is related to the compressing electrostatic force from the electrodes. The electrostatic force is proportional to the square of the applied electrode potential. From an electric point of view the DEAP actuator is equivalent to a capacitor. Additional information on tubular DEAP actuators are found in: [6-9].

Danfoss PolyPower A/S offers a prototype DEAP push actuator: InLastor [10, 11]. Figure 4 illustrates the DEAP actuator. Current DEAP technology requires a high electrical field to induce substantial strain. For the InLastor the maximum operating potential is 2.5 kV which provide a stroke of 1.2 mm or a blocking force of 6 N [12]. The high operating voltage together with the capacitive nature of the DEAP actuator requires a dedicated driver suitable for both charging and discharging capacitive loads.

Figure 4: Danfoss PolyPower DEAP push actuator: InLastor. With and without enclosure. Height: 110 mm.

Danfoss PolyPower provides such a driver capable of charging a DEAP actuator to 2.5 kV [13]. Figure 5 illustrates the driver. Input voltage is 24 V and the output voltage is

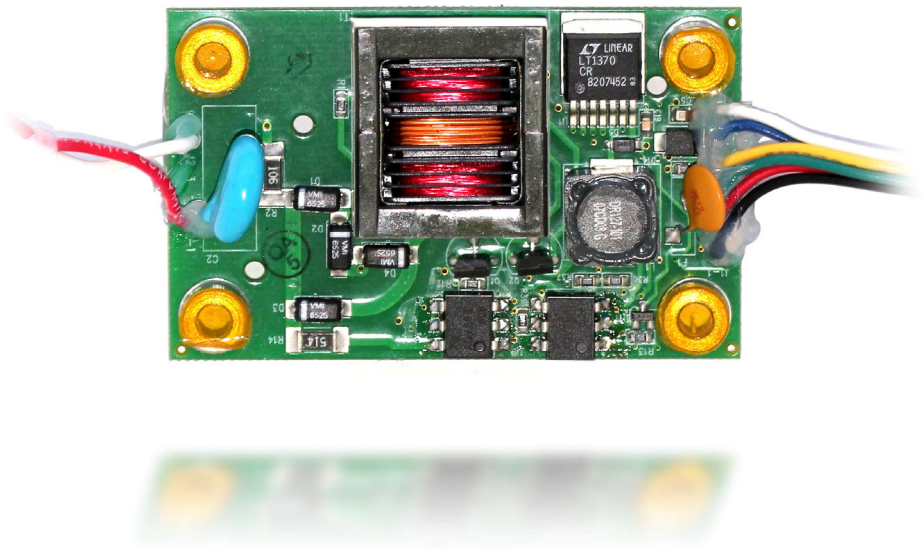


Figure 5: Electromagnetic transformer based driver: dedicated for DEAP actuators. Input voltage: 24 V, adjustable output voltage: 0.2 – 2.5 kV. Size: 74 mm x 46 mm x 19 mm, width, height and thickness respectively.

adjustable from 250 V to 2.7 kV. The charging circuit of the driver is a power supply based on a Royer oscillator [14] utilizing an electromagnetic transformer together with two transistors. Discharging of the DEAP actuator is performed by shorting the output terminals with a couple of opto-coupled MOSFETs (AQV258) through a resistive element. A control circuit controls the power supply and the discharge circuit and ensures that both are not on at the same time. The driver in figure 5 is treated as state-of-the-art for driving DEAP actuators.

The DEAP actuator not only requires a dedicated high voltage driver but the high voltage interface also demands precaution and use of high voltage graded cables and connectors to avoid any hazards. The additional safety precautions associated with a high voltage interface might be a limiting factor in some DEAP actuator applications and might therefore lead to an alternative actuator choice. One way to avoid the high voltage issues is to integrate the electronic driver into the DEAP actuator itself. The core of the tubular DEAP actuator of figure 4 is hollow and enables the possibility to incorporate the electronic driver. The principle is illustrated in figure 6. The interface of the DEAP actuator with integrated driver is solely low voltage and the end-users choice of a DEAP actuator solution is not omitted by any high voltage issues.

One of the competitive areas of DEAP actuators are applications involving high magnetic fields e.g. magnetic resonance imaging (MRI). The non-magnetic properties of the DEAP technology allows DEAP actuators to function unaffected in high magnetic fields compared to electromagnetic based actuators. However, the driver integrated into the DEAP actuator must also function correct when exposed to high

magnetic fields. Electromagnetic transformers and inductors lose their function when the magnetic field exceeds the saturation limit of the core material. This implies that the driver must be constructed without magnetic components. The principle of the electromagnetic based driver in figure 5 can therefore not be reused in the design of an integrated driver.

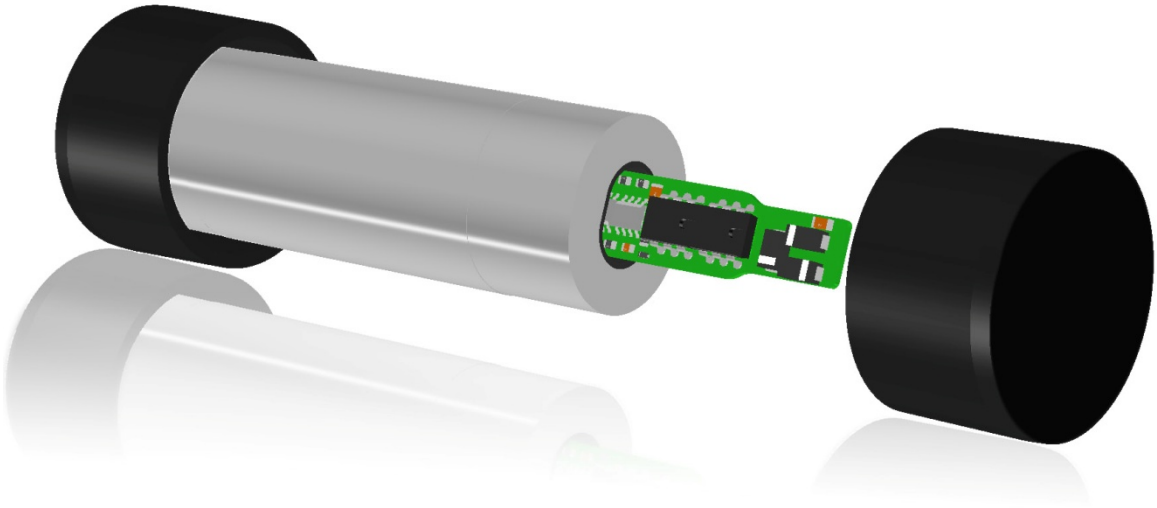


Figure 6: Principle of the electronic driver integrated into the hollow core of a tubular DEAP actuator. The result is a DEAP actuator with low voltage interface.

1.3.2 Integrated driver

To facilitate a DEAP actuator with both low voltage interface and unaffected functionality in high magnetic fields, a new DEAP driver must be constructed compact enough to fit inside the hollow volume of a tubular DEAP actuator, made completely without magnetic components and be able to transform a low voltage into at least 2.5 kV. The physical size constrains on the driver requires an efficient DC-DC switch mode power supply (SMPS) topology for charging the DEAP actuator. DC-DC SMPS without magnetic components includes two main topologies based on switched capacitor and piezoelectric transformer.

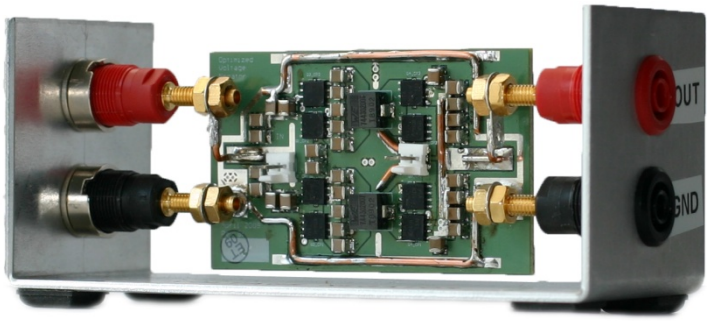


Figure 7: SMPS based on the switched capacitor topology.

The simplest switched capacitor based SMPS works in two steps: First, by charging N numbers of capacitors in a parallel configuration at low voltage. Second, stack the charged capacitors in a serial configuration to obtain an output voltage of N times the input voltage. For an input voltage of 24 V this solution requires more than 100 capacitors and more than 200 switches to reach an output voltage of 2.5 kV. Figure 7 illustrates a 400 watt SMPS based on a simple 2-stage switch capacitor topology [15]. More sophisticated switch capacitor solutions exists [16, 17] that requires less capacitors and switches: The multi phase voltage doublers [18] requires 7 capacitors and 22 switches to achieve 2.5 kV at an input voltage at 24 volts. The number of switches alone makes the switch capacitor topology less desirable for high step-up conversions.

Piezoelectric transformer (PT) based SMPS utilize an electro-mechanic coupling to obtain a voltage conversion analogues to the electromagnetic transformers utilize an electro-magnetic coupling. Figure 8 shows a picture of a PT. At one end acoustic waves are generated in the material and at the other end these acoustical waves are harvested again. The idea was developed by C.A. Rosen in the 1950s [19]. High step-up ratio is not a problem with a Rosen type PT [20-22]. The main applications of PT also involves high voltage applications [23, 24]: cold cathode fluorescent lamp (CCFL) backlighting for LCDs, negative ion generators, photomultipliers, and field emission displays (FEDs).

Figure 8: Piezoelectric transformer: Rosen type

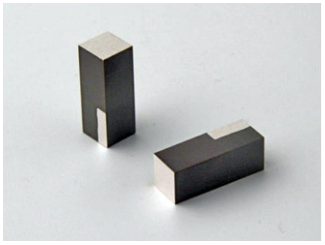
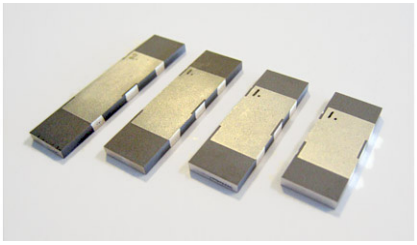
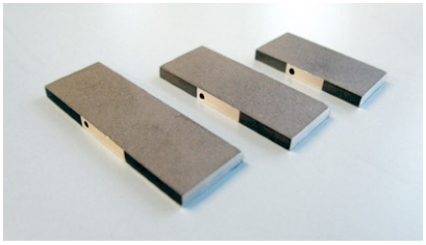
A PT based SMPS can be made completely without magnetic components [25-27] and is suitable for high voltage applications. Power density [28] of PTs is reported as high as 40 - 135 W/cm^3 [29, 30], this indicates the possibility of a compact design.

It is therefore obvious to explore the possibilities within PT based SMPS further as regard to an integrated DEAP actuator driver.

1.4 Project objectives

The success criterion for this project is to develop a PT based SMPS that can be effectively combined with the emerging DEAP technology into an integrated actuating device. The combined solution will be smaller, weigh less, be non magnetic and be significantly more efficient than the conventional solution.

Chapter 2: Piezoelectric transformers

2.1 Introduction to piezoelectricity

Piezoelectricity is a property of a material that becomes electrical charged when subjected to a mechanical stress. This effect is referred to as the direct piezoelectric effect. The piezoelectric effect is reversible, hence a mechanical deformation of the material is observed when subjected to an electrical field, this is referred to as the inverse or converse piezoelectric effect [31, 32]. The constitutive equations and standards regarding piezoelectricity can be found in [33].

The origin of the piezoelectric effect is a change in the electric dipole moment (P) [34] of the crystal structure (unit cell). Figure 9 sketches a simplified crystal structure in the absence of external strain, the charge distribution within the structure is symmetric and the net electric field is zero. Figure 10 sketches the same structure applied to an external stress, deformation of the structure alter the electric dipole moment and the charge distribution is no longer symmetric. A net polarization (P) develops and results in an internal electric field [31, 35, 36].

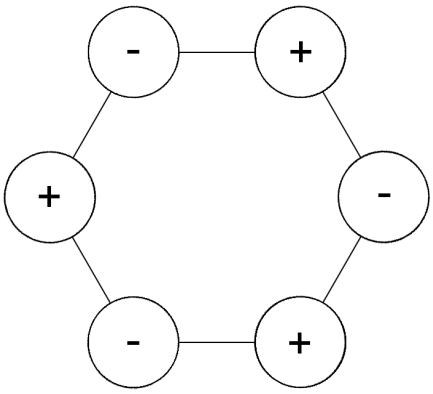


Figure 9: Undeformed

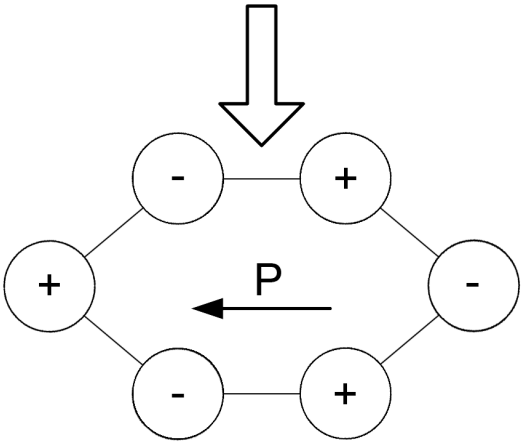


Figure 10: Deformed

2.1.1 Polarization

A piezoelectric unit cell is asymmetric and polar by nature. The orientation of a unit cell is denoted by its electric dipole moment (polarization). However, a unit cell loses asymmetry and polarization when heated above a certain temperature, which is the Curie temperature. Above the Curie temperature a unit cell does not have any polarization and is not piezoelectric. A unit cell becomes asymmetric and piezoelectric again when the temperature drops below the Curie temperature, although the orientation of polarization is changed according to the surround electrical fields. For a piezoelectric material that consists of many unit cells, the orientation of each unit cell is also affected by each other's electric dipole. Without any external influence the orientation of each unit cell is arranged so the net polarization of the material goes towards zero. Figure 11 illustrates a piezoelectric material with an orientation of unit cells resulting in zero net polarization, the material is referred to as non-polarized material. For a non-polarized material all the piezoelectric unit cells counteracts each other. The result is that non-polarized piezoelectric material does not show any piezoelectric effect on macro scale.

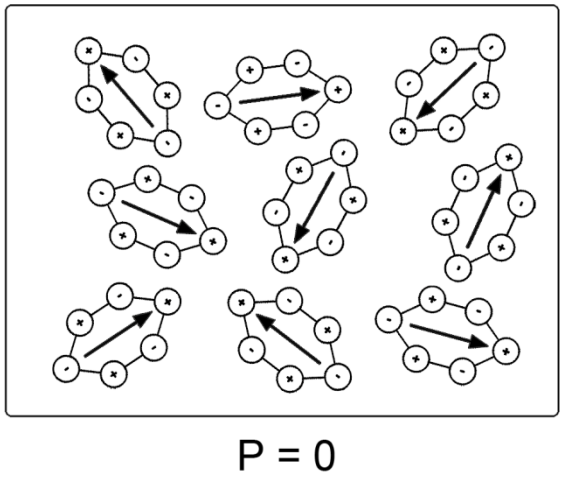


Figure 11: Piezoelectric material with a net polarization of zero, this material is referred to as non-polarized material and have no piezoelectric effect on macro scale.

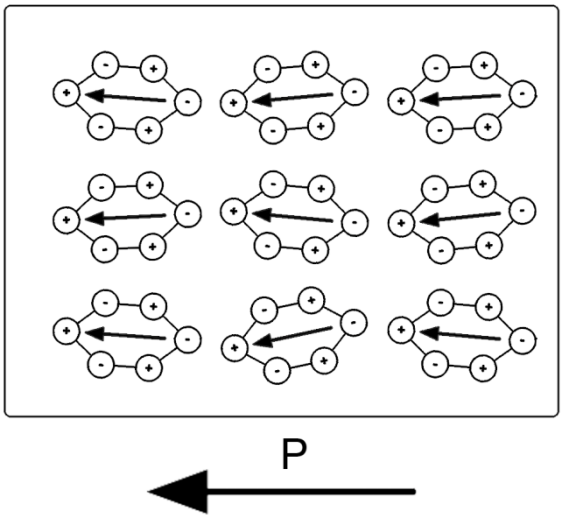


Figure 12: Piezoelectric material with aligned unit cells creates a net polarization. The net polarization gives the material piezoelectric effects on macro scale.

For a piezoelectric material to exhibit piezoelectric effect on macro scale the orientation of unit cells must be aligned towards the same direction to create the necessary net polarization. Figure 12 illustrates a polarized piezoelectric material with aligned unit cells that exhibit piezoelectric effect on macro scale. The direction of the polarization is indicated with an arrow denoted with a P. The polarization

process (aligning the unit cells orientation) is done by applying an electric field across the piezoelectric material. If the field strength is high enough the unit cells will align with the electric field. The resulting direction of polarization is equal to the direction of the applied electric field. The material will maintain this polarization even after the external electric field are removed. However, the polarization of the material will be affected if subjected to too high electric fields or mechanic stress and even depolarize if the temperature reaches the Curie temperature. Under normal use of piezoelectric material the conditions for both the electric field and mechanic stress are below the threshold of polarization impact.

The inverse piezoelectric effect is illustrated in figure 13 for material polarized in four different directions subjected to a voltage below threshold of polarization impact. The resulting deformation is exaggerated 10^8 times to clearly visualize the piezoelectric effect. As a rule of thumb the piezoelectric material elongates when the direction of polarization and electric field is equal.

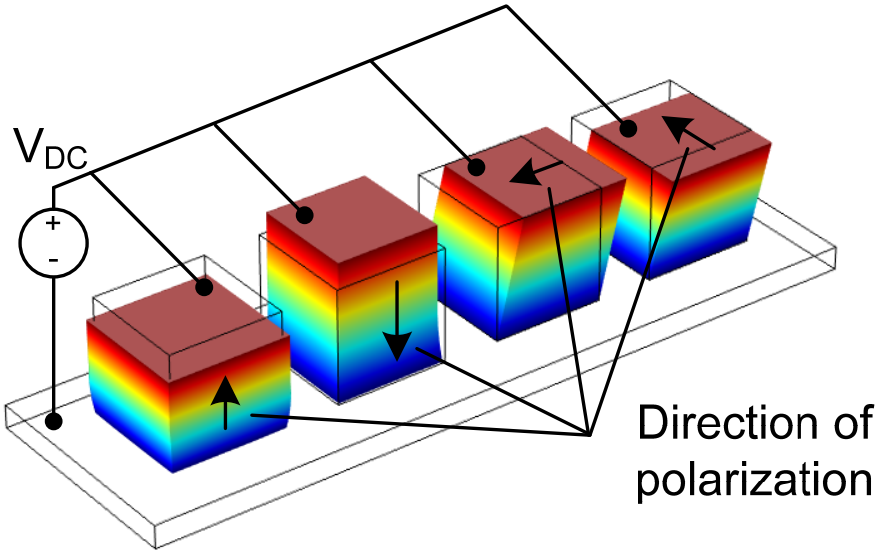


Figure 13: Simulation of four piezoelectric cubes on a conducting plate subjected to a voltage much lower than the polarization voltage. The electric potential is given by the colors. Deformation depends on the relation between direction of polarization and electric field [A1].

2.2 Piezoelectric transformers

Piezoelectric transformers (PTs) are based on piezoelectric material. This material has an electromechanical coupling and through this coupling a charge displacement is generated, which is proportional to the deformation of the material. A PT is basically

two piezoelectric elements which is joined together to form a transformer. The primary side element is then exited by an electrical AC voltage, which induces a deformation of the two joined elements. This deformation generates an AC output voltage on the secondary side element. With a proper design of the PT a desired voltage conversion can be obtained from the primary to the secondary side [A1].

In order to convert power at a high efficiency, the PT is operated in one of its resonance modes [24, 37-39]. The PT resonates each time it is possible to generate a standing wave in the element. But the design is usually optimized for one specific resonance mode, in order to obtain the highest efficiency [37, 39].

Each of the PTs resonance modes can be modelled as a distributed network, but for simplicity and mathematical representation, only the resonance mode of interest is modelled. One of the most used PT models is the lumped parameter model, which was derived by Mason in 1942 [40] and is illustrated in figure 14.

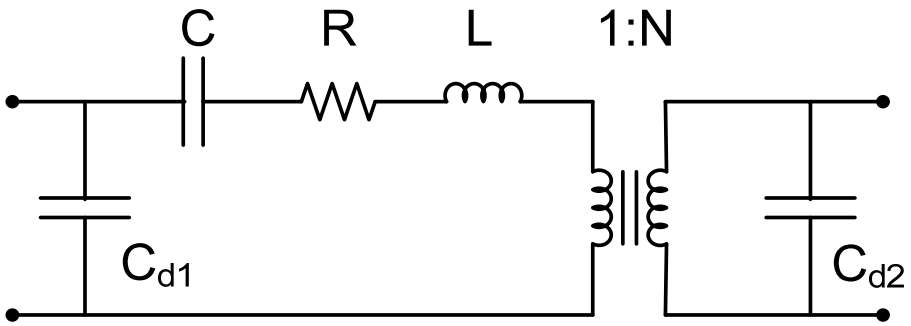


Figure 14: Electric lumped parameter equivalent of a piezoelectric transformer, valid only in the vicinity of a resonance mode.

The lumped parameters is derived from a PT design by applying the constitutive equations of piezoelectricity [33] to the geometry and electrode placement of the PT. Analytic equations can be obtained, but even for uncomplicated geometries with simple electrode placement where assumptions and symmetry can be used to reduce the problem, the solving task is complicated [22, 37, 39, 41]. However with the aid of finite element methods (FEM) the lumped parameters of the Mason model can be derived, even for complicated geometry with odd electrode arrangements. The FEM program *COMSOL Multiphysics* [42] is utilized to simulate different PT designs.

From the gained experience of simulating PTs a thorough guide has been develop to evaluate the lumped parameters by use of a FEM program [A1].

2.2.1 Zero voltage switching

Zero voltage switching (ZVS) is important in a non-magnetic PT based converter and therefore need additional attention [25-27, 43-45]. ZVS is also referred to as soft switching in contrast to hard switching. Hard switching refers to a switching event where both current and voltage are present at the same time across a switch element. Power is therefore dissipated in the switching element during the switching event. Hard switching is an inefficient switching behaviour. Soft switching on the other hand is efficient, because only current or voltage is present during the switching event.

A PT inhere the input capacitor (C_{d1}). To avoid hard switching an inductive element must be utilizes in the charging or discharging process of the capacitor (C_{d1}). For a non-magnetic PT based converter the only inductive element exists in the PT itself (L). To achieve a high efficiency the PT must be able to fully charge its own input capacitor (C_{d1}). The *ZVS factor* is the PT design parameter that describes the PT's ability to charge its own input capacitor (C_{d1}) [45]. A PT with a ZVS factor of one or more is able to charge its own input capacitor. The ZVS factor is dependent on the load conditions of the PT. However the ZVS factor is defined at matched load condition [45] (worst case). Matched load condition is given by equation (1).

$$R_{matched} = \frac{1}{\omega \cdot C_{d2}} \tag{1}$$

The ZVS factor of the PT can be calculated directly from the lumped parameter of the Mason model. A simple and transparent equation is given by [45]. The equation is shown in (2). It has the advantages of being very short and handy, as well as being transparent, providing a very good relation between the lumped parameters and the ZVS factor. The drawback is that it is too optimistic. Through employment of the expression within PT development and experimental work, it is found that a ZVS factor of at least 1.4 is needed in order to achieve soft switching.

$$V_P^{'} = N^2 \frac{C_{d2}}{C_{d1}} \cdot \frac{32\sqrt{6}}{9\pi^2} \cdot \eta \tag{2}$$

On the other hand a complete analytic expression is given by [43]. The equation is that long that it makes no sense to repeat it here. The result is a precise expression of the ZVS factor. The drawback is a complex equation, making it computational heavy and with no transparent relation between the parameters and the ZVS factor.

Therefore a new equation for the ZVS factor is derived with both good accuracy and transparent relation between the parameters and the ZVS factor [A2]. The equation is given by (3).

$$V_P^{'} = \left(0.304 \cdot N^2 \frac{C_{d2}}{C_{d1}} + 0.538 \right) \cdot \left(0.585 \cdot \eta + 0.414 \right) \tag{3}$$

For a rule of thumb the PT can ZVS if equation (4) is satisfied.

$$1.55 < N^2 \frac{C_{d2}}{C_{d1}} \tag{4}$$

Even though ZVS increases efficiency it decreases the power density of the PT [46], simply because ZVS limits the fraction of output energy. This becomes clear when electromechanical coupling is introduced. A ZVS factor much more than one is therefore undesirable.

2.2.2 Piezoelectric coupling coefficient

This chapter tries to give a brief visual understanding of the concept *electromechanical coupling* in regards to a PT design and link the concept to efficiency and the important ZVS factor.

Piezoelectric coupling coefficient (or electromechanical coupling coefficient) is an expression for the conversion of stored energy to mechanical or electric work [31, 33, 35]. In other words: the square of the electromechanical coupling coefficient is dimensionless and express the fraction of energy converted from the electrical domain into the mechanical domain or vice versa. Electromechanical coupling (5) must not be confused with energy efficiency (6). Energy efficiency involves loss of energy that cannot be recovered. That is not the case with the electromechanical coupling.

$$k^2 = \frac{W_M}{W_M + W_E} \quad OR \quad k^2 = \frac{W_E}{W_E + W_M} \tag{5}$$

$$\eta = \frac{W_{out}}{W_{out} + W_{loss}} \tag{6}$$

Piezoelectric material is anisotropic therefore the electromechanical coupling depends on the direction of: vibration, plane of electrodes and polarization. Figure 15 illustrates two important modes out of many: (left) Thickness mode (k_{33}) in which the direction of vibration and polarization is the same and the plane of electrodes is perpendicular. (Right) Transverse mode (k_{31}) the direction of vibration and plane of electrodes is the same, while the polarization is perpendicular. It is important to notice that thickness mode has higher coupling than transverse mode, according to datasheet of piezoelectric materials there is approximate a factor of two in difference (7) [47, 48].

$$k_{33} \approx 2 \cdot k_{31} \qquad (\text{typically}) \tag{7}$$

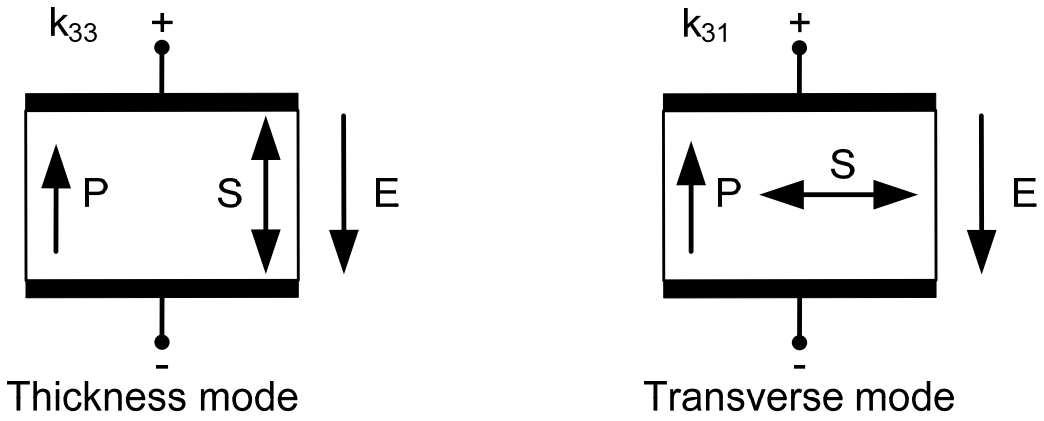


Figure 15: Two modes with different electromechanical coupling (k). Thickness mode: k_{33} (left), transverse mode: k_{31} (right).

Piezoelectric coupling coefficients are based on ideal lossless material with uniform electrical fields and polarization. In practice it is more convenient to use the effective coupling coefficient (k_{eff} or effective coupling factor) [33, 49, 50] where losses are included. The concept of electromechanical coupling is a key to understand the operation and performance of a PT design.

In figure 16 we consider the energy flow through a PT after injecting one portion of electric energy to the primary side. Units of energy is visualised by the squared boxes. Electric energy is injected to the primary section (W_{Ep}) at T_1. Due to an effective coupling coefficient of the primary section (k_p) less than one, only a fraction of the electric energy (W_{Ep}) is converted to mechanic energy (W_M). The remaining energy remains electric (W_{Ep}). At T_2 a fraction of the mechanic energy (W_M) is converted to electric energy (W_{Es}) at the secondary side. This fraction is fixed by the effective coupling coefficient of the secondary section (k_s). The remaining energy

stays mechanic (W_M) and bounces back towards the primary section. At the primary (T_3) another conversion of energy is initiated from mechanic (W_M) to electric (W_{Ep}). The fraction is fixed by k_p and the remaining part of the mechanical energy bounces back again towards the secondary section and so on and so forth.

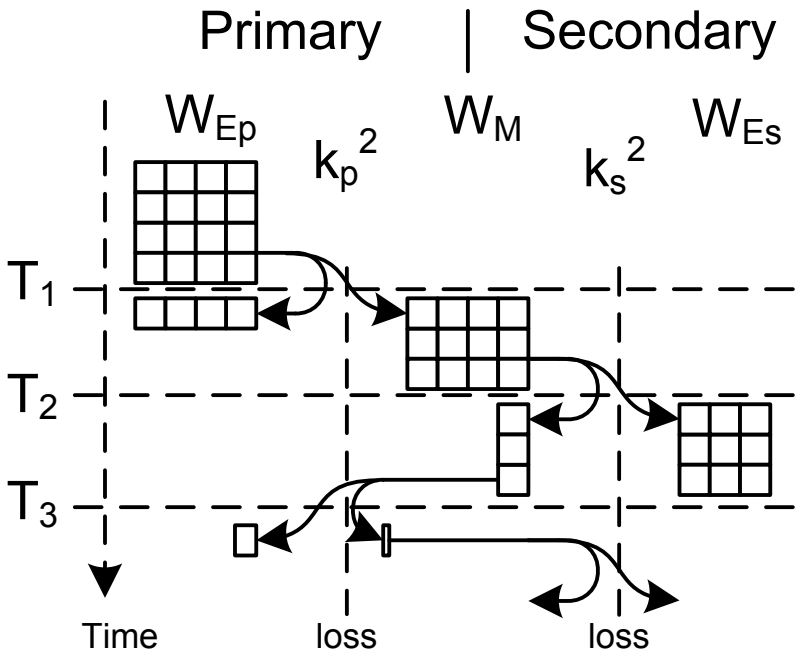


Figure 16: Simplified illustration of the energy flow in terms of squared boxes in a PT. Energy flows forth and back according to the electromechanical couplings coefficient k_P and k_S.

Figure 16 only illustrates a single energy injection at the primary side. In a steady state operation energy is injected to the primary section at every second time step.

Energy is lost in a PT, both electrically and mechanically. In figure 16 the losses are indicated at the boundaries of energy conversion. For simplicities it can be assumed that loss is directly proportional to the amount of injected input energy divided by the square of the effective coupling coefficients (k), this is illustrated by equation (8) where y is a simplified constant. The amount of output energy is proportional to the injected input energy times the square of the effective coupling coefficients (k), this is illustrated by equation (9) where x is a simplified constant. From the definition of efficiency (6) it can then be derived that a low effective coupling will lead to low efficiency (11). Thus a high effective coupling is desired.

$$W_{loss} = y \cdot \frac{1}{k^2} \cdot W_{in}\Big|_{y>0} \tag{8}$$

$$W_{out} = x \cdot k^2 \cdot W_{in}\Big|_{x>0} \tag{9}$$

$$\eta = \frac{W_{out}}{W_{out} + W_{loss}} = \frac{x \cdot k^2 \cdot W_{in}}{x \cdot k^2 \cdot W_{in} + \frac{y}{k^2} W_{in}} = \frac{1}{1 + \frac{y}{x} \cdot \frac{1}{\left(k^2\right)^2}} \tag{10}$$

$$\eta \to 0 \quad \Rightarrow \quad k \to 0 \tag{11}$$

Figure 16 also illustrates the property of the ZVS factor in terms of the effective coupling coefficients. To achieve ZVS at least a certain amount of mechanic energy (W_M) must be converted to electric energy at the primary side (W_{Ep}) at T_3. A low k_s ensures that enough of the mechanical energy is reflected back and a high k_p ensures that enough of the reflected mechanic energy (W_M) is converted over to electric energy (W_{Ep}). The ratio between the two effective coupling coefficients that satisfies the ZVS condition is given by equation (12) and can be derived from [51][A2 (a1)].

As a rule of thumb: k_p must be higher than k_s to achieve ZVS.

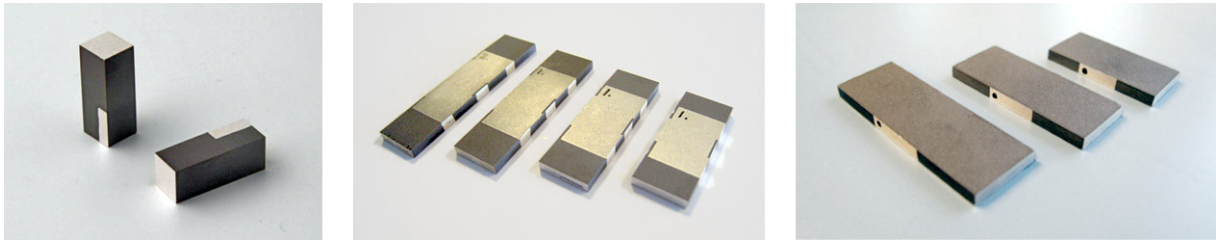
$$1.55 < \frac{\left(k_{eff\_\text{secondary}}\right)^{-2} - 1}{\left(k_{eff\_\text{primary}}\right)^{-2} - 1} \quad \Rightarrow \quad k_{eff\_\text{primary}} \gg k_{eff\_\text{secondary}} \tag{12}$$

A low k_s implies lower efficiency and power flow but increases the ZVS factor. A ZVS factor much more than one is therefore undesirable.

2.3 Piezoelectric transformer designs

Duing this project several high voltage PT designs have been derived, simulated and prototyped with focus on e.g. low profile size, efficiency, voltage gain and zero voltage switching (ZVS) factor. The different PT designs are grouped and named according to the electromechanical coupling and placement of their primary and secondary sections. The three PT designs are: Glued thickness mode, Interleaved Rosen type and Interleaved thickness mode [51], [A3, A4].

Within each group different versions are prototyped to optimise and tune specific parameters. Figure 17 shows a selection of some of the prototyped PTs.



Glued thickness mode PT | Interleaved Rosen type PT | Interleaved thickness mode PT

Figure 17: A small selection of prototyped PT designs arranged according to the electromechanical coupling and placement of their primary and secondary sections.

2.3.1 Glued thickness mode PT

Thickness mode refers to the utilisation of the piezoelectric coupling coefficient [31, 33, 35]: k_{33}, in which the direction of vibration and polarization is the same and the plane of electrodes is perpendicular.

Figure 18: Tiles of piezoelectric material are glued together to build up the glued thickness mode PT.

The PT build-up process is based on tape casting technology that allows multilayer electrode design, however the building height was limited by the manufacturer. A full build-up in one piece was therefore not possible for this PT design. To overcome the limitation in height several thinner pieces were glued together. The glued thickness mode PT design is inspired by the success of prototyping radial mode PTs from gluing pre-polarized discs of piezoelectric material together with adhesive material [52, 53]. The radial mode PT itself is not desirable due to the combination of its physical round shape and the size constrains regarding the integration of the driver DEAP. Instead tiles were produced to form a suitable size and shape. Figure 18 illustrates the tiles used to create the glued

thickness mode PT. Figure 19 sketch the concept of electrode placement with polarization and the associated stress and displacement curves. Furthermore the utilized resonance mode is illustrated to the right. The displacement curve has two zero-crosses indicate that it resonates in its second resonance mode.

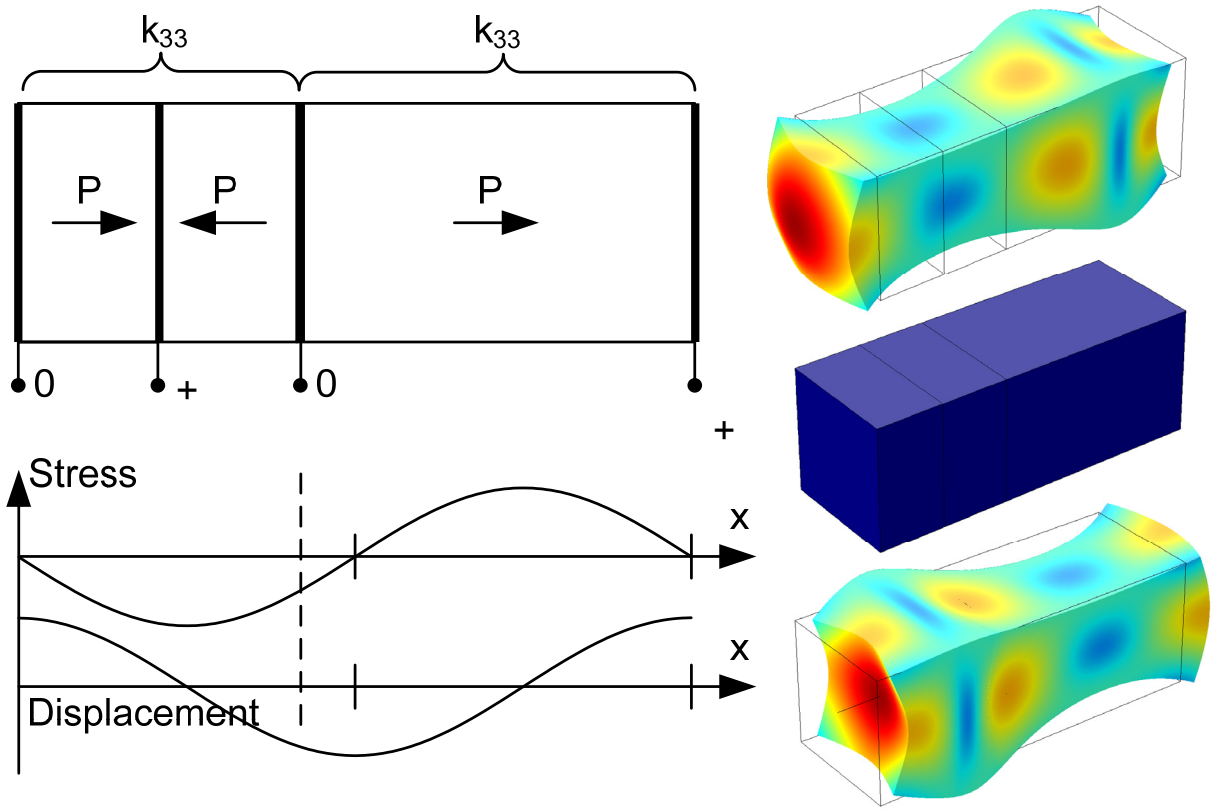


Figure 19: To the left: Concept of the glued thickness mode PT with associated stress and displacement curves. To the right: Exaggerated displacement of 2th resonance mode is visualized.

Unfortunately the glued thickness mode PT was not able to transfer much power before a fatal delamination occurred between two of the tiles. Experiments with different adhesive did not solve the problem. The exposed stress on the glue is different between radial mode design and thickness mode design. That might explain the observed delamination of the thickness mode PTs, however this have not been scientific proved.

2.3.2 Interleaved Rosen type PT

To avoid adhesive in the build-up of the PT a low profile design were required by the manufacturer. An obvious and compliant tape casting PT design is the Rosen type. The classic Rosen type design [19, 22] is shown in figure 20. A Rosen type PT design utilise a combination of thickness mode (k_{33}) and transverse mode (k_{31}) [31, 33, 35, 39]. The primary section operates in transverse mode: the direction of vibration and

plane of electrodes is the same, onto which the polarization is perpendicular. The secondary-section operates in the former mentioned thickness mode.

Figure 20: Classic Rosen type PT design.

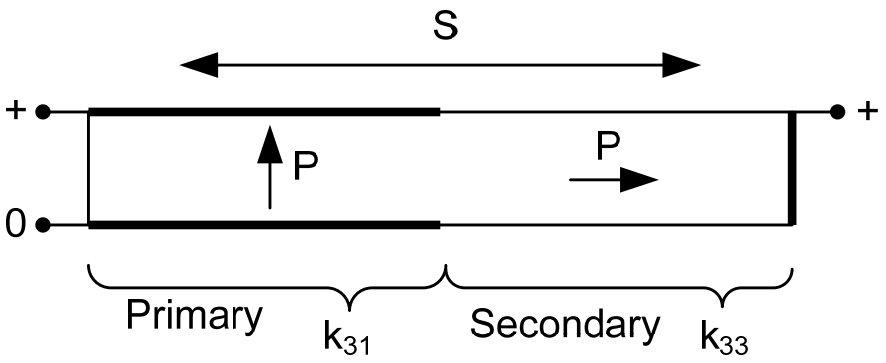


Figure 21: Concept of the classic Rosen type PT

Figure 21 sketch the concept of the Rosen type PT. The classic Rosen type has two major drawbacks: the electromechanical coupling of transverse mode is less compared to thickness mode; the overall efficiency is thus lower compared to a complete thickness mode design. Furthermore the ratio between the primary's and the secondary's effective coupling is always below one. According to equation (12) the effective coupling ratio must be above 1.55 to achieve ZVS. As a conclusion the ZVS factor for a Rosen type PT is always below one.

In order to achieve a ZVS factor above one, the effective coupling of the primary section must be increased or the effective coupling of the secondary section must be decreased. Figure 22 illustrates an interleaved Rosen type PT design with two primary layers and the associated stress and displacement curves for the first resonance mode. As a rule of thumb the effective coupling is proportional to the sum of the stress **Fejl! Henvisningskilde ikke fundet.**. By interleaving the primary section into the middle of the stress curve its effective coupling is increased, while a decrease of the secondary sections effective coupling is implied by the lower sum of stress. The ratio between effective coupling, which is related to the ZVS factor (12), can be tuned by changing the volume ratio of primary and secondary sections.

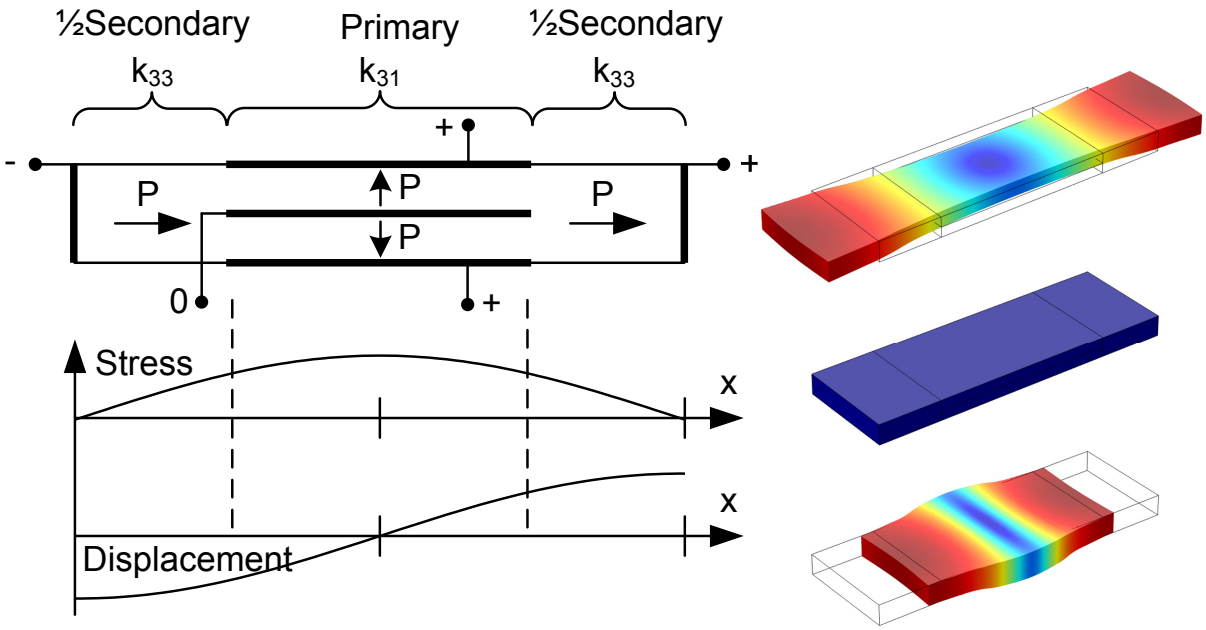


Figure 22: To the left: Concept of interleaved Rosen type PT with associated stress and displacement curves. To the right: Exaggerated displacement of 1th resonance mode is visualized for the interleaved Rosen type PT.

$$k_{eff} \propto \int_{x} Stress \tag{13}$$

The result is an interleaved Rosen type PT design optimized for a ZVS factor above one. Figure 23 is illustrates some of the produced prototypes. A detailed description of the PT design is found in [A3].

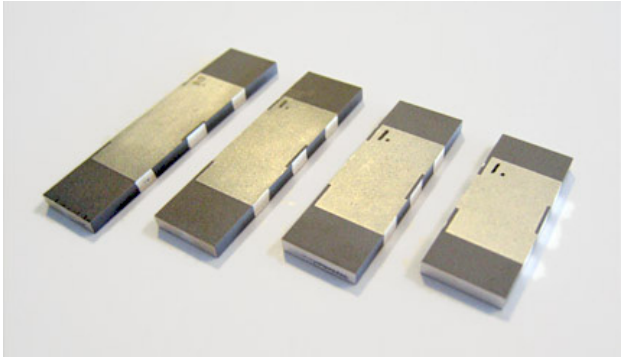


Figure 23: Interleaved multilayer Rosen type PT designs; optimized to achieve a ZVS factor above one.

2.3.3 Interleaved thickness mode PT

Introduction of interdigitated electrodes (IDE) [51][A4] by the PT manufacturer, made it possible to produce a complete thickness mode PT that is compliant with the tape casting process. Figure 24 illustrates the concept of the interleaved thickness mode PT. The PT is operated in its first resonance mode as illustrated in figure 25 together with stress and displacement curves.

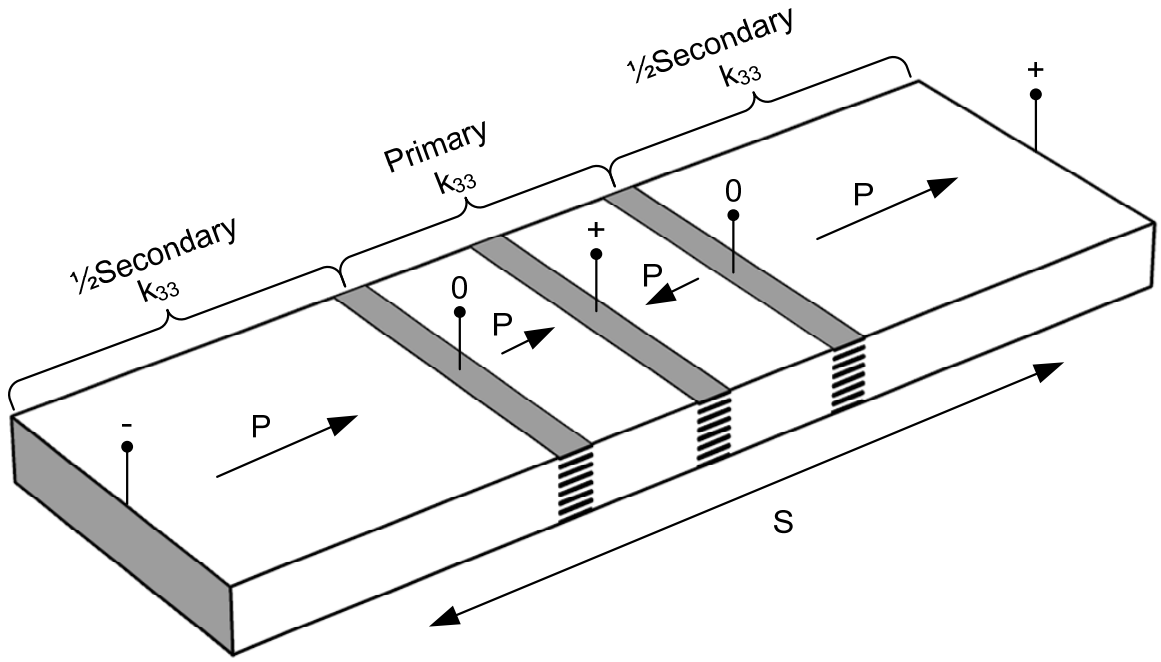


Figure 24: Concept of the interleaved thickness mode PT with interdigitated electrodes (IDE) [51][A4].

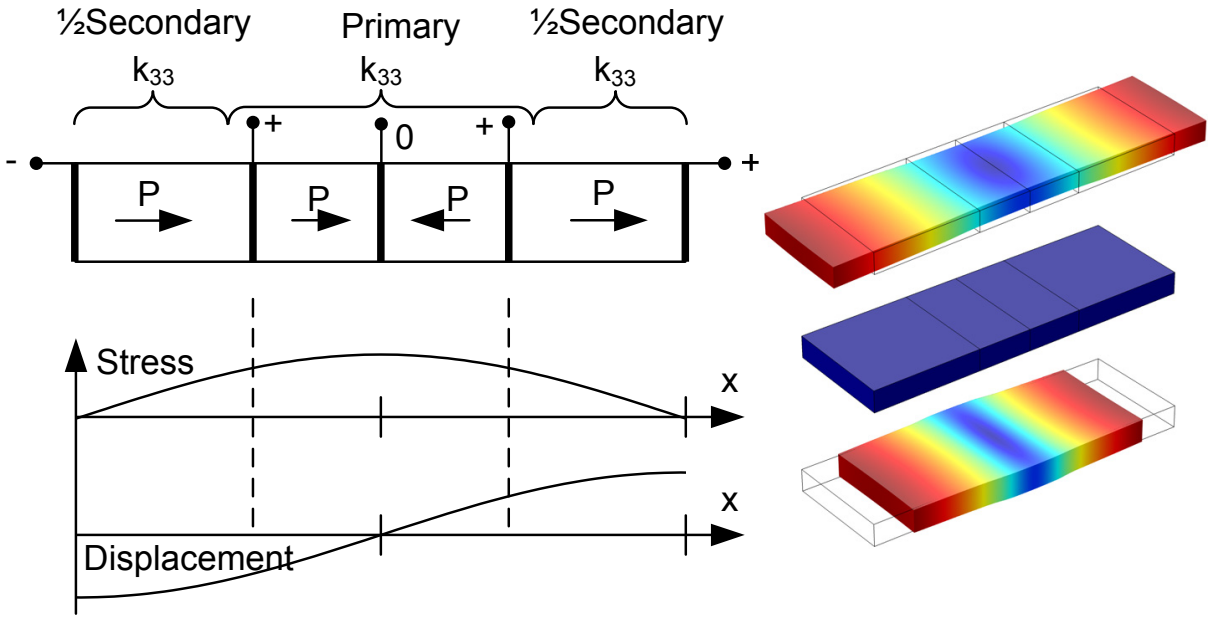


Figure 25: To the left: Concept of interleaved thickness mode PT with associated stress and displacement curves. To the right: Exaggerated displacement of 1th resonance mode is visualized for the interleaved thickness mode PT.

The ZVS factor is controlled by adjusting the volume ratio of the primary and secondary sections similar to the interleaved Rosen type PT. For an equal volume ratio of the two designs, interleaved Rosen type and interleaved thickness mode, the ZVS factor is always highest for the interleaved thickness mode because of the native higher electromechanical coupling of the primary section. As a consequence of the higher electromechanical coupling both power density and efficiency will increase according to equation (9) and (10) respectively.

Figure 26 illustrates some of the produced prototypes of the interleaved thickness mode PT design [51][A4].

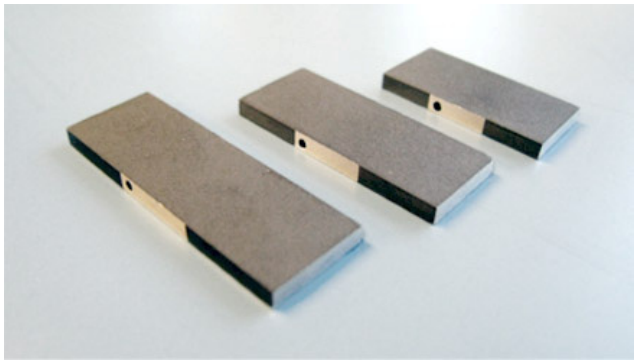


Figure 26: Produced prototypes of the interleaved thickness mode PT design.

2.3.4 Comparison of power density

Figure 27 shows a power density plot that compares the interleaved Rosen type PT with the interleaved thickness mode PT. The power density plot is obtained by controlling the excitation frequency of the PT to achieve a fixed gain equal to the optimal ZVS spot. Thereby the PT is operated similar to a non-magnetic PT based converter application. The temperature of the PT is monitored with a thermal camera. Both PTs are of identical physical shape with a volume of 0.6 cm^3 and thus the power density measurements are directly comparable for the two PTs. Defining an upper limit for the temperature rise of 40 ℃ shows an improvement in power density of approximately 5 times for the interleaved thickness design compared to the interleaved Rosen type design.

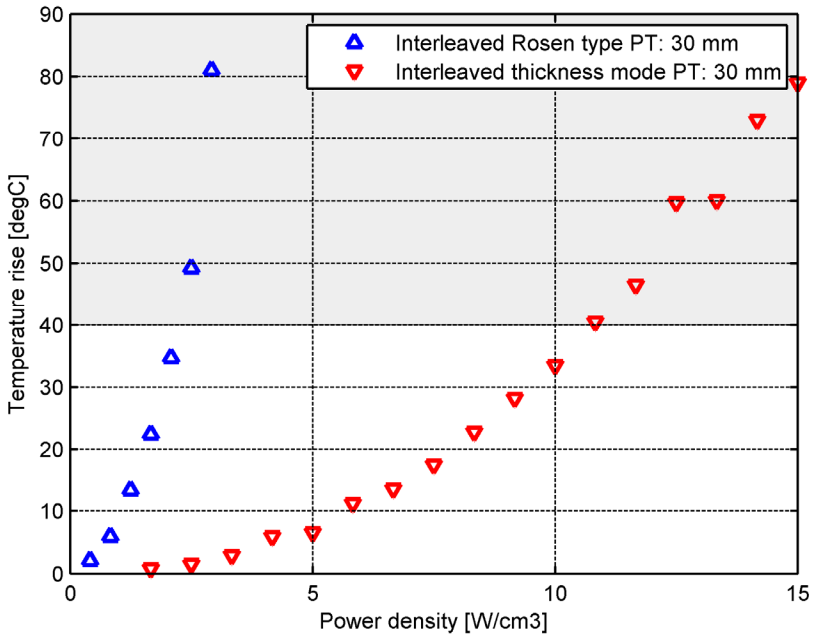


Figure 27: Power density comparison between the interleaved Rosen type PT and the high efficient interleaved thickness mode PT.

2.4 Nonlinear effects

The Mason model (figure 14) is a useful equivalent to understand the electrical behavior. However the model has its limitations. The model is only valid around the resonance frequency and it can only predict the linear behavior of a PT. The model is sufficient for power converter applications as long as the PT is kept within its linear region of operation. However the trend goes in a direction of smaller power converters and to keep up with the demand of higher power densities, PTs will be forced into the region of nonlinear operation. Therefore we need to understand the

nonlinear effects of PTs to either prevent them, by better PT designs, or deal with them in the control circuit.

Two of the nonlinear effects of PTs are gain saturation and a phenomenon called voltage jumps. In the literature these nonlinear effects are associated with the relatively large mechanical deformation that arises around resonance of a PT and are described by the nonlinear theory of electro elasticity [23, 54]. However based on empiric research in the performance of PTs exposed to high power flows a simplified thermo-electric model is derived. The thermo-electric model relates the losses in a PT to the Mason lumped parameter model by the hypothesis of self-heating and predicts the nonlinear effects of: gain saturation and voltage jumps. The model is tested against a set of measurements of nonlinear voltage jumps. Figure 28 shows a plot of measured voltage jumps and the corresponding simulation with the thermo-electric model. Figure 31 illustrates the thermo-electric model to predict gain saturation. [A5]

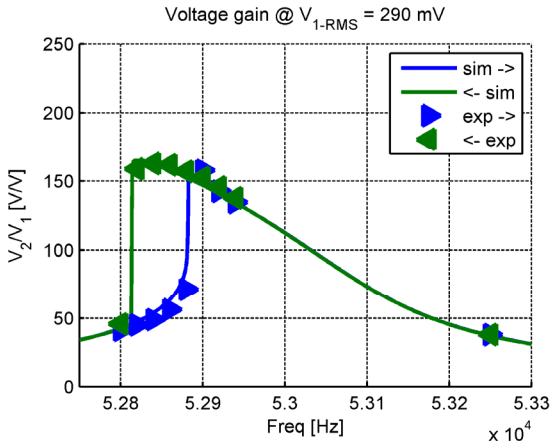


Figure 28: Voltage jumps - nonlinear effect of a PT measured and simulated with the thermo-electric model.

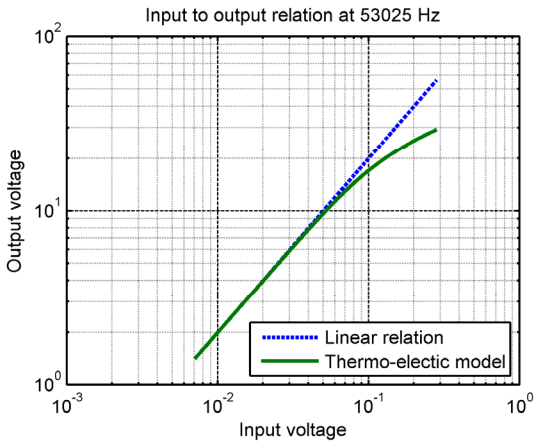


Figure 29: Gain saturation - nonlinear effect of PTs simulated with the derived thermo-electric model

The thermo-electric model has aid in a better understanding of these nonlinear phenomena which are more pronounced for PTs with high power density.

2.5 Measurement tool – matched load

From the Mason equivalent model, figure 14, the efficiency of the PT can be calculated for a given load [39, 45]. For a resistive load, the maximum efficiency is at matched load condition [39, 45] [A6]. It can also be shown that the ZVS factor, the PTs ability to soft switch, has a global minimum at match load [43, 45]. If the PT is capable of soft switching at matched load, it can soft switch for any resistive load.

Measuring the power density of PTs is done where the efficiency is highest. Therefore a matched load is connected at the output to obtain maximum efficiency.

Prior art within matched load, has been to solder off-the-shelf ¼ watt leaded resistors together in a manner to obtain the correct resistive value as well as handle the power dissipation and voltage stress. Potentiometers that can handle the power and the voltage stress suffer from high parasitic inductions and can therefore not be used. It is a time consuming process to solder a matched load, especially for high voltage and high power. Therefore an adjustable load circuit was constructed to simulate a resistive load with low parasitic capacitance and inductance. Figure 30 shows the principle: a MOSFET is controlled in its linear region to simulate a resistive load. A positive voltage across the MOSFET is needed to avoid forward biasing of the body diode. To ensure a positive voltage a high voltage full bridge rectifier with low parasitic capacitance is utilize. The voltage across the MOSFET is used as reference for the current into the circuit. To exclude the error introduced by the full bridge rectifier a current sense transformer (CST) is used to measure the current in front of the full bridge rectifier. The resulting prototype is illustrated in figure 31 [A6].

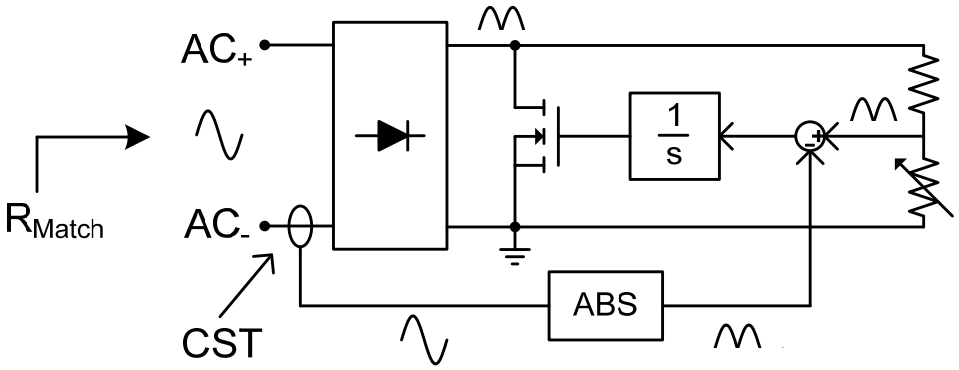


Figure 30: The principle of the active match load circuit. A current sense transformer (CST) is used together with an active rectifier (ABS) for current feedback.

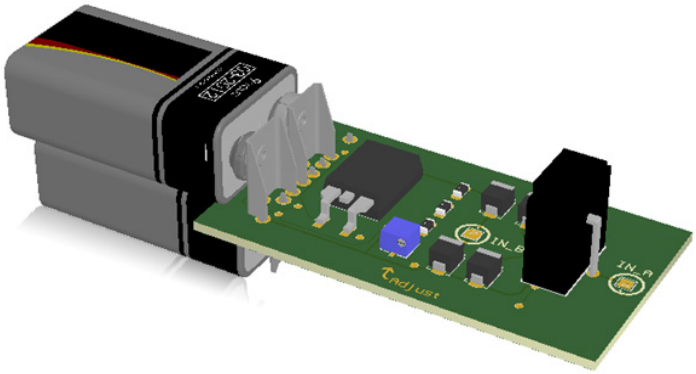
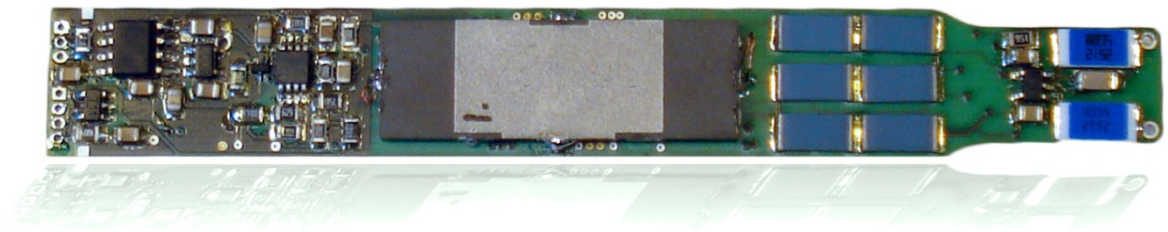


Figure 31: Adjustable load circuit for simulating a high voltage resistive load at 50kHz with low parasitic components.

Chapter 3: Driver – Unidirectional energy flow



3.1 Overview

The key specifications for the integrated driver are: non-magnetic, compact and with high efficiency. The unidirectional driver consists of three basic parts: charging, discharging and control. Figure 32 shows the block diagram of the driver and how the basic parts are interconnected.

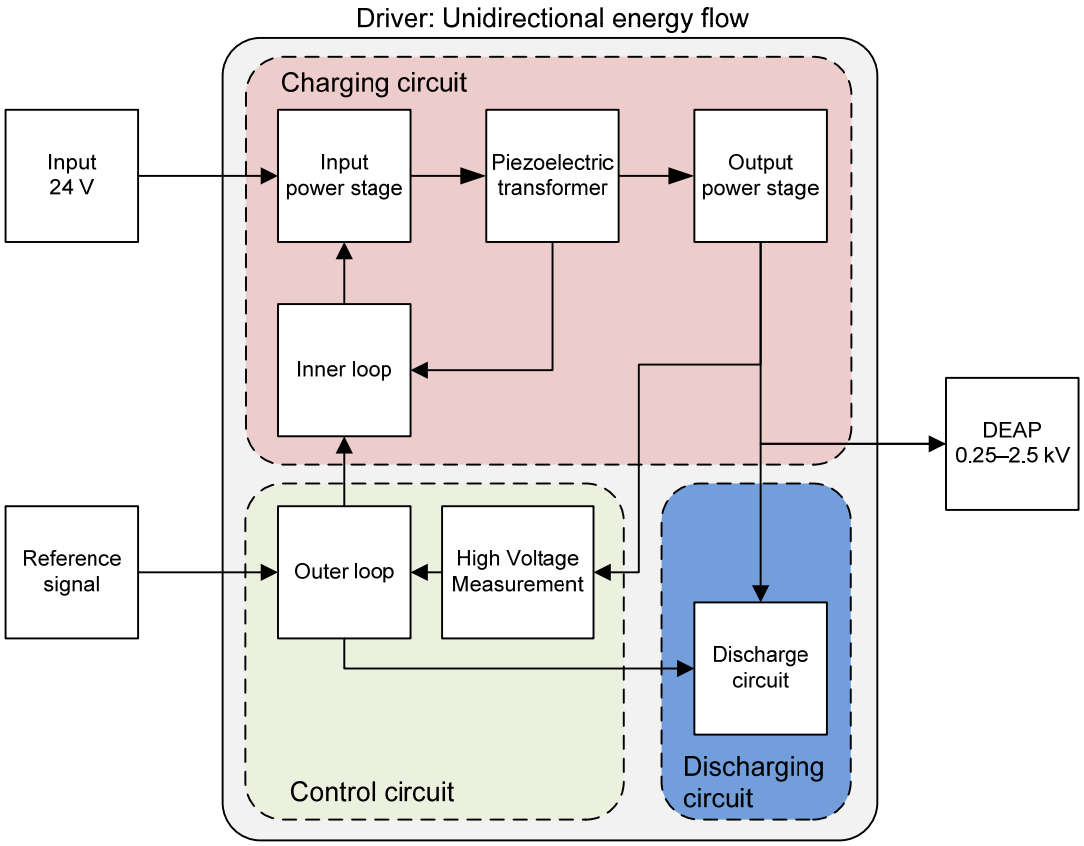


Figure 32: Block diagram of the unidirectional energy flow driver for DEAP actuators.

3.1.1 Charging circuit

The charging circuit is based on a non-magnetic PT topology [25-27, 55, 56]. A half-bridge input stage drives a ZVS optimized PT. To ensure a high efficiency the half-bridge stage must operate under ZVS. The high quality factor together with a limited ZVS factor for the PT entails a narrow frequency band of operation. Furthermore this narrow frequency band of operation changes considerable with both load and temperature [57, 58]. Therefore a closed loop is needed to maintain high efficiency. An inner loop is closed around the resonance current of the PT to facilitate self-oscillating (SO) modulation [A7]. The SO is based on a reconstruction of the resonance current [25]. The measured current is phase shifted, in order to obtain the self-oscillation. A low frequency hysteresis oscillator is implemented in the SO loop, to ensure start-up of the SO loop.

The output stage rectifies the AC output voltage of the PT in to a DC output voltage of the driver. The normal voltage doubler rectifier [59, 60] consists of two diodes however a three diode solution is utilized to decrease the parasitic load of the output to the interleaved PT design [A8].

3.1.2 Control circuit

Charging and the discharging are controlled by the control circuit. The control circuit utilize burst mode [A8][61] to control the average output power of the charging circuit. A hysteretic window set by an external reference signal is compared with a high voltage measurement (HVM) feedback signal of the output voltage. When the feedback signal is below the lower limit of the hysteretic window, the charging circuit turns on. When the upper limit is reached the charging circuit is turned off again.

The same technique is used for the discharging circuit: Another hysteretic window set by the external reference signal and compared with the feedback signal from the HVM. However, to avoid the charging and the discharging circuit to operate at the same time, the hysteretic window for the discharging circuit is slightly offset compared to the hysteretic window for the charging circuit.

Through small bursts of charging and discharging, dependent on the reference signal, the output voltage is kept within a limited range set by the reference signal. The size of the hysteresis windows and their offset can be optimized, in order to decrease the output voltage ripple. However it is a trade-off between efficiency and output ripple, because a lower voltage ripple implies a higher burst frequency and the PT takes time to build up sufficient resonance current to avoid hard switching. Therefore a higher burst frequency will lead to higher losses and lower efficiency.

3.1.3 Discharging circuit

For the driver with unidirectional energy flow the discharging of the DEAP is performed by shorting the output voltage through a resistor without retrieving any energy.

3.2 ZVS operation

The output of the PT is directly connected to a matched load, to ensure that the PT based driver is able of soft switching for any given load. Figure 33 illustrates the PT connected to a half-bridge stage with the half-bridge voltage (V_1) and the output of the PT (V_2) connected to a resistive matched load. The SO loop is not shown on the figure. Figure 34 and figure 35 illustrate a simulation of the normalized half-bridge voltage for a half-bridge stage connected to a PT that cannot soft switch and to a PT that can soft switch.

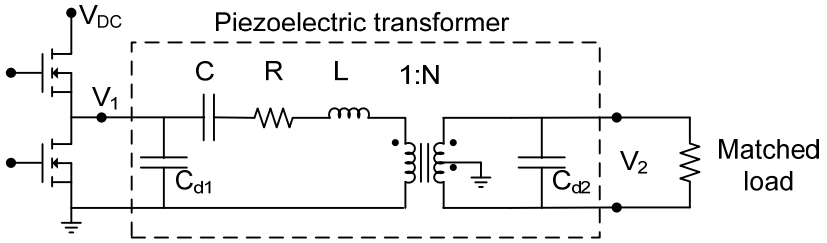


Figure 33: Setup for measuring the PT's ability of soft switching.

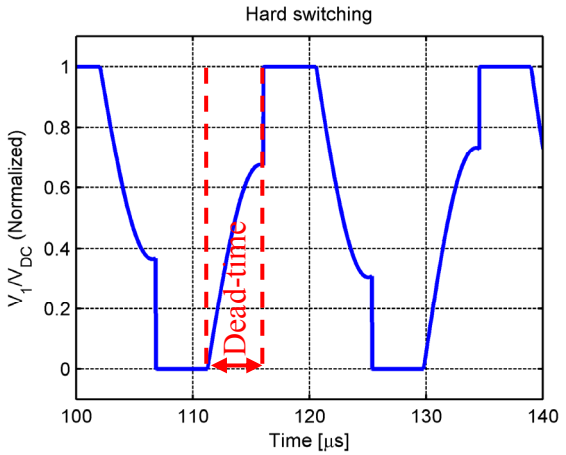


Figure 34: Hard switching occurs; PT is not able to fully charge/discharge C_{d1} in the dead-time period of the switches. ZVS factor ≈ 67 %

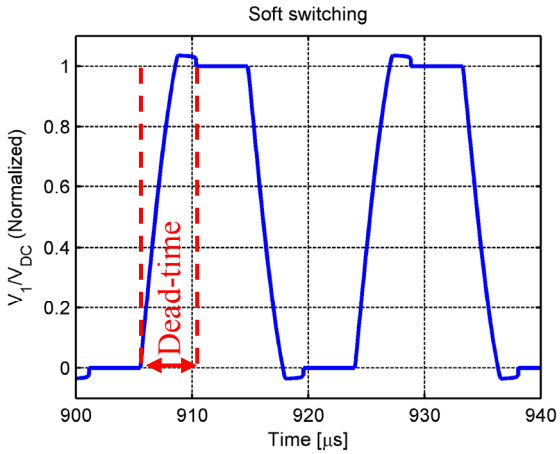


Figure 35: Soft switching occurs; PT is able to fully charge/discharge C_{d1} in the dead-time period of the switches. ZVS factor > 100 %

Figure 36 shows an oscilloscope measurement of the half-bridge voltage (yellow) and the output voltage across the matched load (green). The SO loop is tracking the right frequency and ZVS is obtained by the PT.

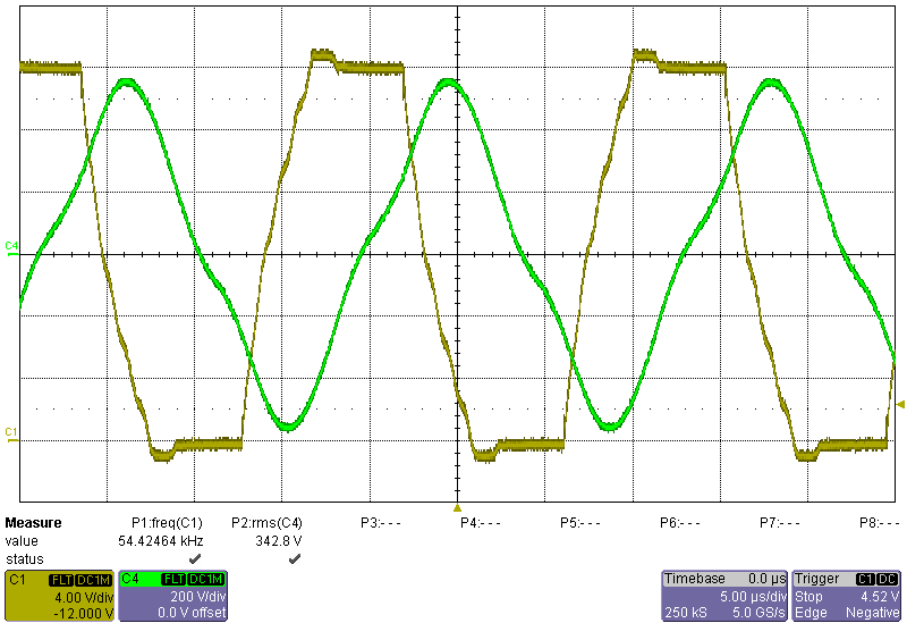


Figure 36: Demonstration of half-bridge under ZVS operation (yellow) while the output of the PT (green) is directly connected to a matched load.

3.3 Performance

A top view of one of the prototyped drivers is illustrated in figure 37. The PT used for this prototype is the interleaved Rosen type PT.

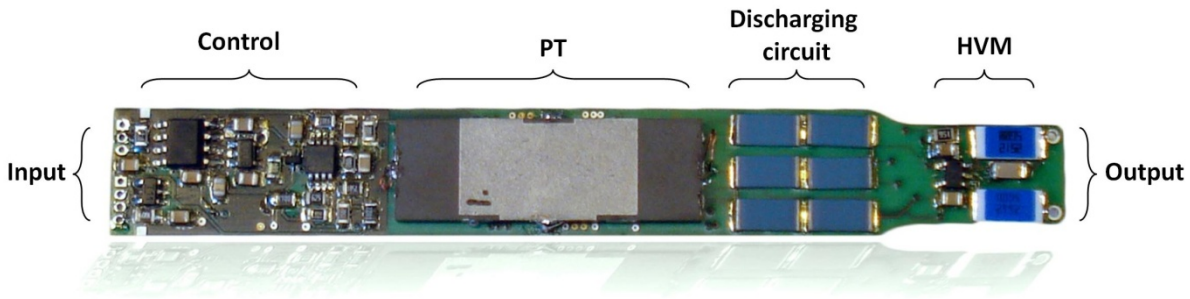


Figure 37: DEAP driver: Non-magnetic, PT based, high efficiency, compact and indented for integration

Figure 38 illustrates a simplified schematic of the prototype connected to a DEAP actuator. The following section briefly demonstrates the operation of the driver.

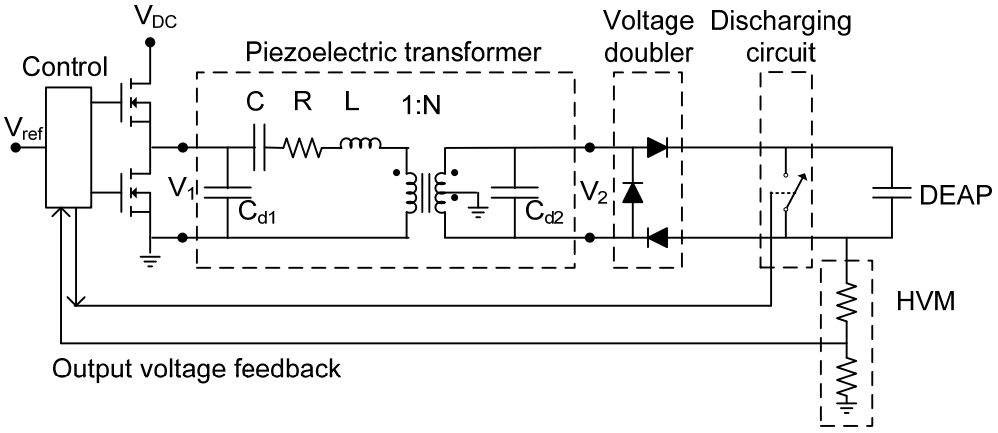


Figure 38: Simplified schematic of the unidirectional DEAP driver.

3.3.1 DEAP actuator control

Figure 39 shows the operation of the driver, with a reference square wave signal (blue) of 2 Hz applied. The output voltage across the DEAP actuator (green) increases until the desired voltage is reached set by the reference signal. Because of leakage currents in the DEAP, HVM circuit and the rectifiers are small bursts executes from the half-bridge (yellow) in order to maintain a constant output voltage.

Figure 40 shows the operation of the driver, with a sinusoidal wave reference signal (not shown) of 2 Hz. The burst periods of the half-bridge, increases and decreases in order to follow the reference signal. The voltage across the DEAP actuator (green) and feedback voltage (red) resembles a sinusoidal wave as dictated by the reference signal.

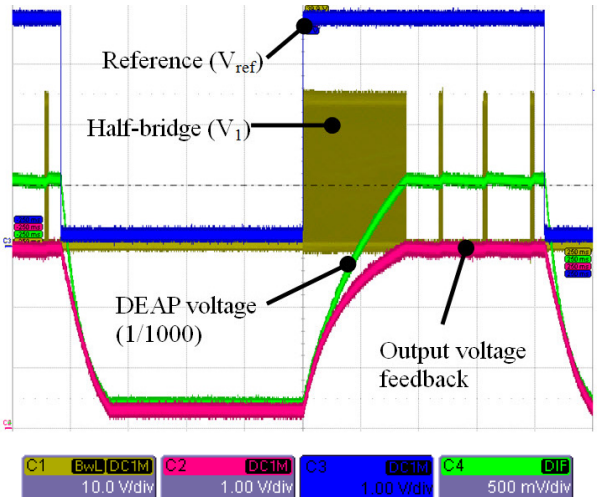


Figure 39: Operation with 2 Hz square wave reference. Yellow: Half-bridge voltage, red: Feedback voltage, blue: Reference voltage, green: DEAP voltage (0 – 2 kV).

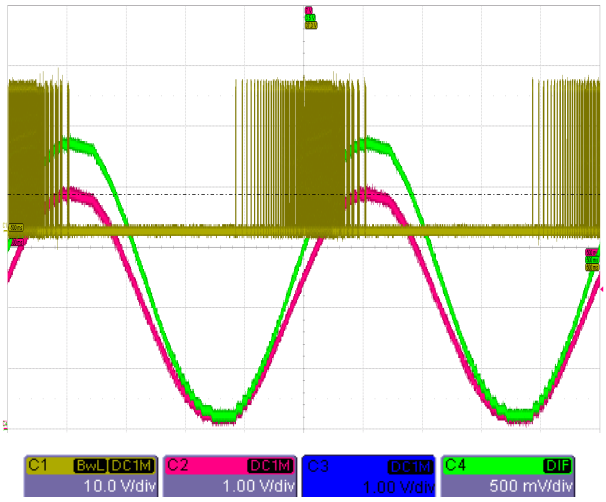


Figure 40: Operation with 2 Hz sinusoidal reference. Yellow: Half-bridge voltage, red: Feedback voltage, green: DEAP voltage (0 – 2.4 kV).

3.4 Comparison

In this section the properties of the PT based driver is compared to the state-of-the-art EMT based driver [13][A8][A9]. The PT used for the driver is the interleaved Rosen type PT.

3.4.1 Physical size

Size is an important issue as the driver has to be compact enough to be integrated into a DEAP actuator. Figure 41 shows the two DEAP actuator drivers. Dimensions are listed in table 1 together with the volume of a box of equal dimensions. A reduction of 89.2 % in the volume is achieved for the PT based driver compared to the EMT based.

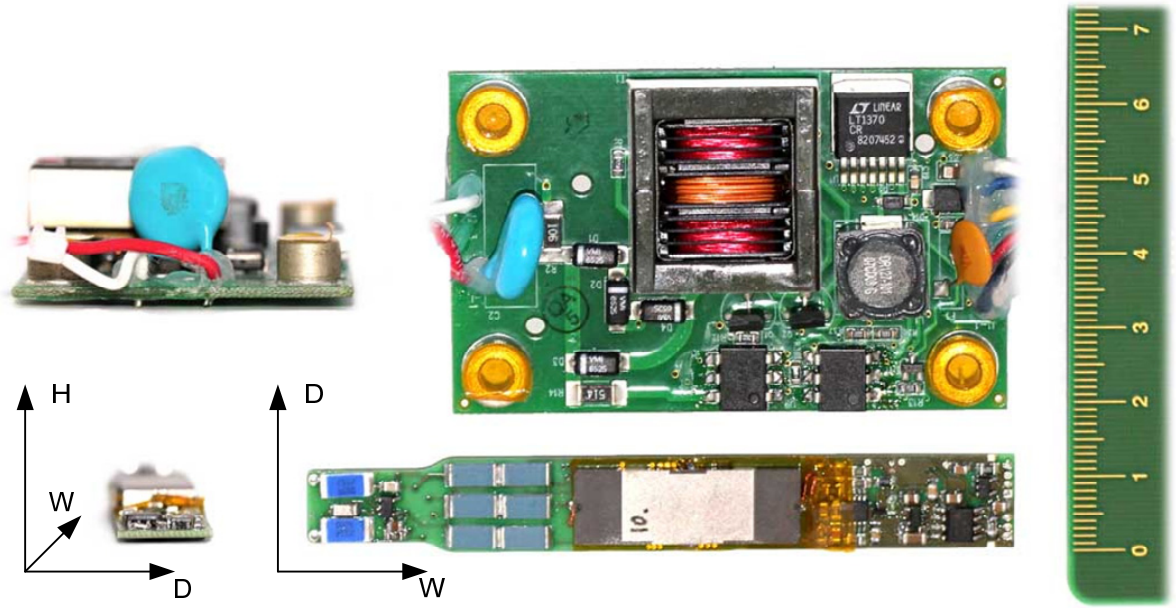


Figure 41: Side and top view of DEAP actuator drivers: EMT based (*top*) and PT based (*bottom*)

Table 1: Size comparison between the two DEAP drivers: EMT & PT

	EMT based	PT based	EMT - PT	Reduction
H	23.6 mm	7.1 mm	16.6 mm	-
W	74.0 mm	95.0 mm	-21.0 mm	-
D	46.0 mm	13.0 mm	33.0 mm	-
Box volume	80,334 mm^3	8,707 mm^3	71,628 mm^3	**89.2 %**

3.4.2 Efficiency

The efficiency of the driver is defined as the ratio between energy stored in the DEAP actuator and energy delivered to the driver (14). Figure 42 shows the setup for measuring the efficiency of the two drivers. To ensure constant capacitance during the charge period, the DEAP actuator is substituted with a film capacitor of 47 nF. Prior to the measurement the capacitor is discharged to zero volt. Input voltage is 24 volt and input current is measured as the output capacity is charged from zero to 1.9kV.

$$\eta = \frac{E_{DEAP}}{E_{input}} = \frac{0.5 \cdot C_{DEAP} \cdot V_{DEAP}^2}{\int V_{DC} \cdot I_{in} \cdot dt} \tag{14}$$

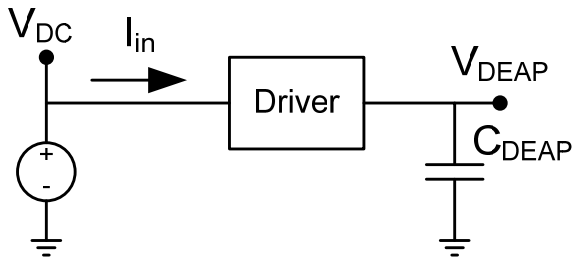


Figure 42: Setup for measuring efficiency of the driver with capacitive load

The measured input current for the PT based and EMT based driver is plotted in figure 43. When the output voltage reaches 1.9kV the control circuit turns off the half-bridge stage and the input current drops suddenly and only current consumption from control circuit is left.

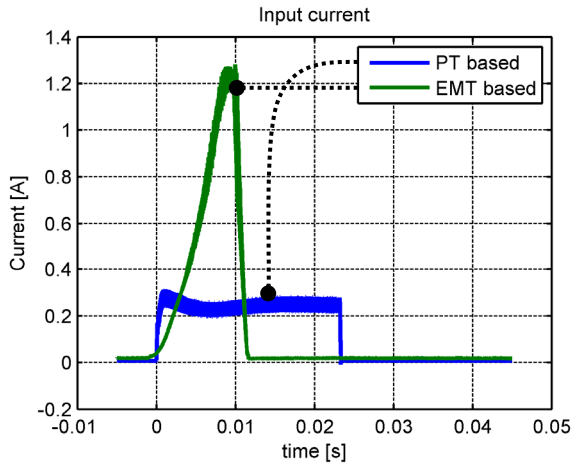


Figure 43: Measurement of input current while charging the output voltage from 0V to 1.9kV. Input voltage is constant at 24 volts.

Efficiency is calculated from the measured input current and the definition (14). Table 2 lists the values for both drivers.

Table 2: Efficiency of PT based and EMT based driver (0 – 2 kV)

Driver type	E_{input} (24V)	E_{DEAP} (47nF)	E_{loss}	Efficiency
EMT based	182 mJ	82.4 mJ	99.6 mJ	45 %
PT based	138 mJ	81.2 mJ	56.8 mJ	59 %

The energy loss is reduced by 43 % for the PT based driver compared to the EMT based driver (15).

$$PT_{loss\,reduction} = \frac{E_{loss,EMT} - E_{loss,PT}}{E_{loss,EMT}} = 43\% \tag{15}$$

3.4.2.1 Efficiency in matched load

For a PT based driver the highest efficiency for a resistive load is obtained at matched load [A6][39, 45]. Figure 44 illustrates the circuit to measure the efficiency.

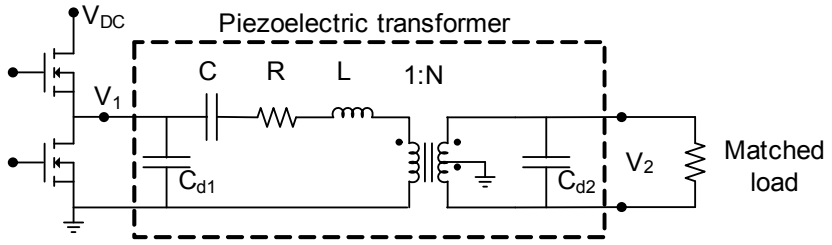


Figure 44: Circuit to measure efficiency of the PT based driver with matched load.

Figure 45 shows a plot of efficiency vs. output power for the PT based driver. The output power is controlled by the DC input voltage (V_{DC}).

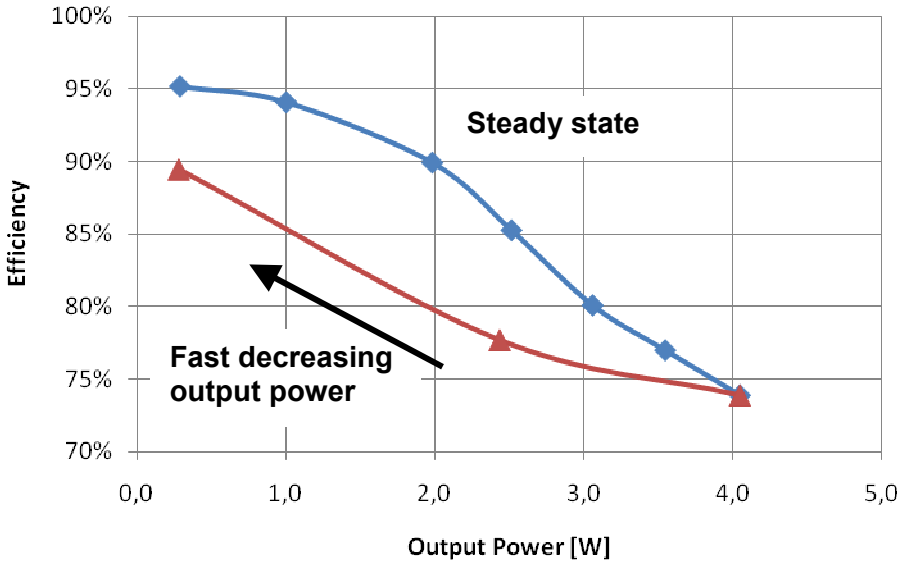


Figure 45: PT based driver: efficiency vs. output power. Blue: steady state output power, red: output power decreased from 4 watt without stabilization of temperature ("Adiabatic").

The blue line is a measurement of the efficiency at steady state output power and with stabilized temperature of the PT. At power levels below 1 watt the efficiency is above 95 %. However at an output power of 4 watts the efficiency drops to 74 %.

Loss within the PT heats up the piezoelectric material and the temperature of the piezoelectric material has impact on the efficiency [A5]. The impact of temperature on efficiency is demonstrated by measure the efficiency from 4 watts with stabilized temperature of the PT and down to 0.3 watts done faster than the PT material can stabilize in temperature, see the red line in figure 45.

Efficiency can be improved for a given PT design if the temperature rise can be reduced for instance by using heatsinks. Utilizing of heatsinks has shown that output power also can be increased [29, 62].

3.4.3 Power density

The power density of the driver is defined as the ratio between output power and volume. Volumes of the two drivers are derived in section 3.4.1. The maximum output power of the EMT based driver is 10 watts [13]. The output power of the PT based driver is measured up to 4 watt, see section 3.4.2.1. Table 3 list the power densities of the two drivers. The power density of the PT based driver is 4 times better than the EMT based.

Table 3: Comparison of drivers' power density

	EMT based	PT based
Power density of entire driver	0.12 W/cm^3	0.48 W/cm^3

3.4.4 Electromagnetic interference (EMI)

The PT based driver is without any magnetic components, so radiated EMI are expected to be low compared to the EMT based driver. Unfortunately a radiated EMI comparison was not possible. However as the PT based driver is a soft switching resonance converter, the general conducted EMI performance is expected to be good in comparison to the EMT based. Neither of the drivers have any dedicated input filter to suppress the fundamental switching frequencies.

The measurement setup for the conducted EMI measurement is illustrated in figure 46. A LISN network is connected to an EMC receiver. The utilized EMC receiver requires a steady state operation of the device under test in order to measure the EMI correct. The driver is therefore loaded with a resistive load (R_L) instead of a capacitive load.

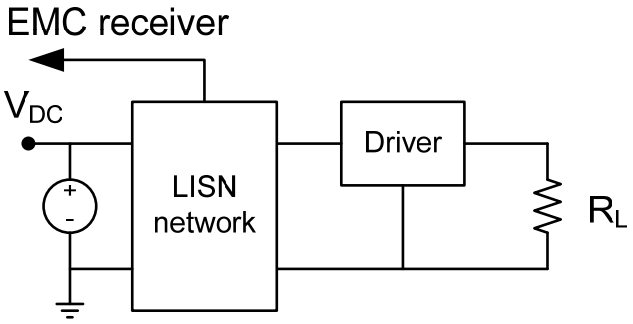


Figure 46: Setup for measure conducted EMI

The result of the EMC receiver is shown in figure 47 and figure 48 for the PT based and the EMT based driver respectively. Both measurements are performed with an output power of 4 watts. As expected both drivers lacks the ability to suppress fundamental frequencies with a peak for both drives of around 80 dBμV. However the PT based driver performs well in the high frequency region (above 1MHz) with a ≈ 25 dBμV decrease between the peak values compared with the EMT based driver.

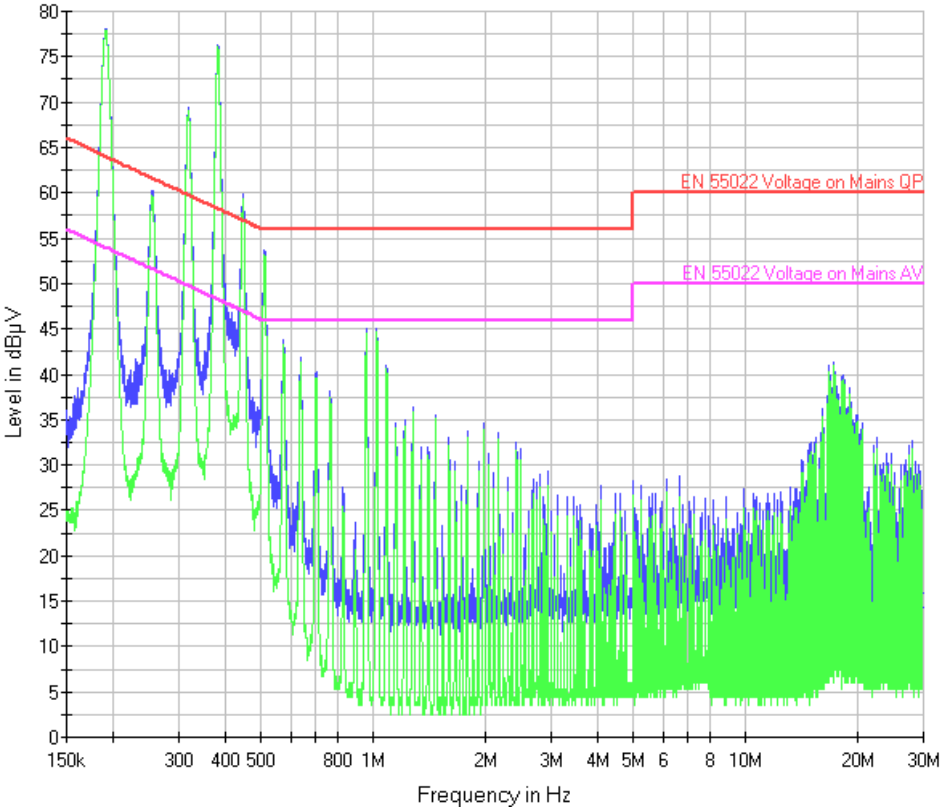


Figure 47: Conducted EMI measurement of PT based driver at 4 watts output power. Green: average measurement, blue: peak measurement.

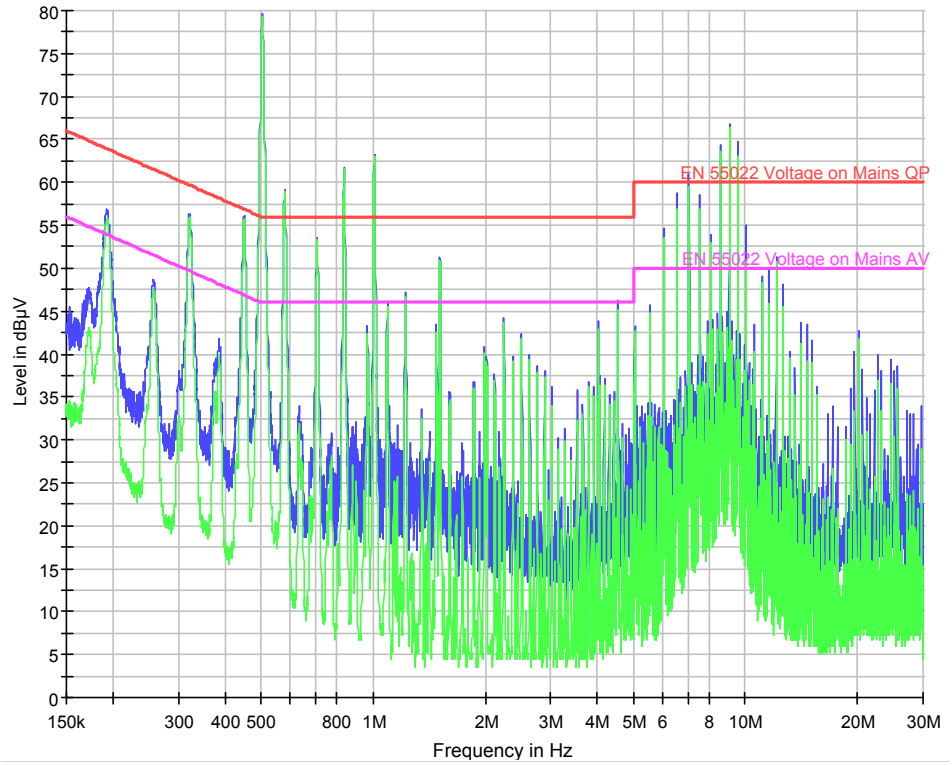


Figure 48: Conducted EMI measurement of EMT based driver at 4 watts output power. Green: average measurement, blue: peak measurement.

3.5 Integration – Low voltage DEAP

A major part of the project is to integrate the driver into the hollow section of a tubular DEAP actuator. This concept is illustrated once again in figure 49 with one of the end caps of the DEAP actuator taken off. The specific DEAP actuator is a Danfoss PolyPower InLastor [12].

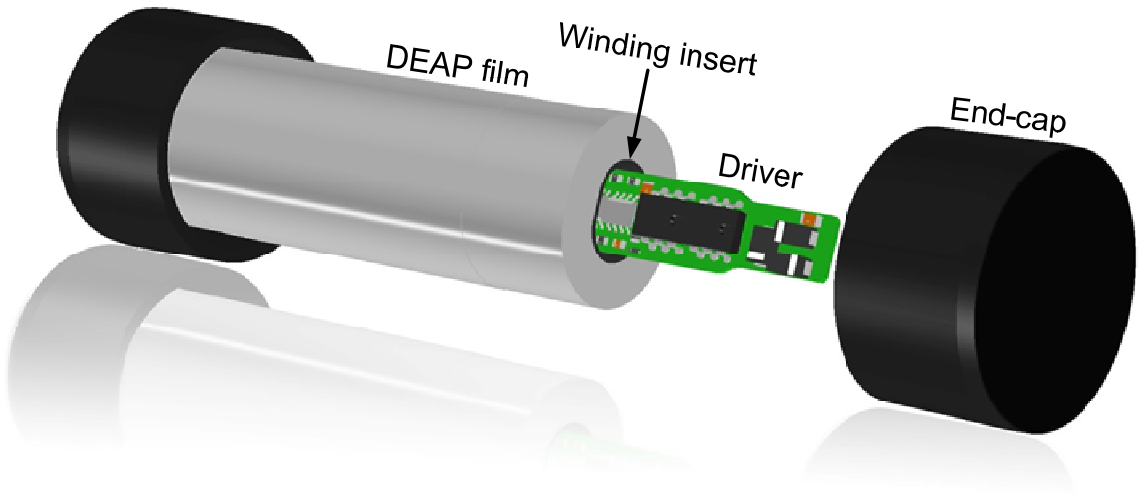


Figure 49: Principle of the electronic driver integrated into the hollow core of a tubular DEAP actuator. The result is a DEAP actuator with low voltage interface.

The actuators hollow cross section has an elliptic shape to increase the stability of the actuator. To enforce the elliptic shape the DEAP film is winded on two elliptic shaped plastic shells (winding inserts) placed in each end of the actuator. End-caps are attached in each end of the actuator to protect the DEAP film. The size constrains on the electronic driver are specified by the inner cross section of the winding inserts and the width between the end-caps.

3.5.1 Assembly

A DEAP actuator with a new set of modified winding inserts is manufactured. The winding inserts are modified with two grooves that serve as a guides and fixture. Figure 50 illustrates the cross section of the modified winding inserts. The PCB of the driver slides into the DEAP actuator in the grooves of the winding inserts. At the edges in one end of the PCB are pads with solder that acts as end stops and position the PCB. The PCB are only fixed in one end and the other end of the actuator are free to move. Wires are then

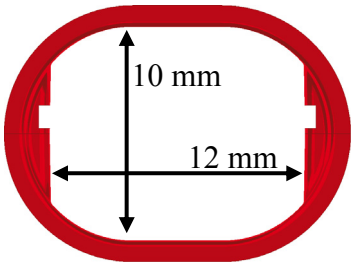


Figure 50: Cross section of a winding insert modified with grooves.

interconnected between driver and DEAP and finally end-caps are attached. Figure 51 illustrates the driver surrounded by the modified winding insert. It verifies that the PT based driver can fit into the cross section area and slide through the winding insert.

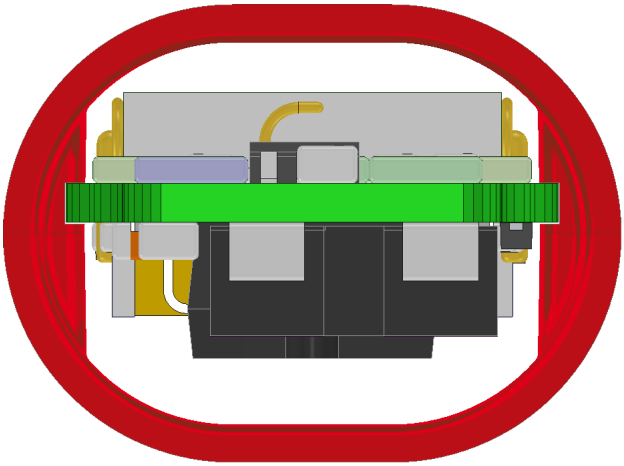


Figure 51: Cross section of winding inserts with driver in position.

Figure 52 illustrates the PT based driver integrated into the DEAP actuator. The width of the driver fits between the two end-caps. The driver PCB is fixed at the winding insert to the left and the rest of the actuator is free to move without contact to the driver.

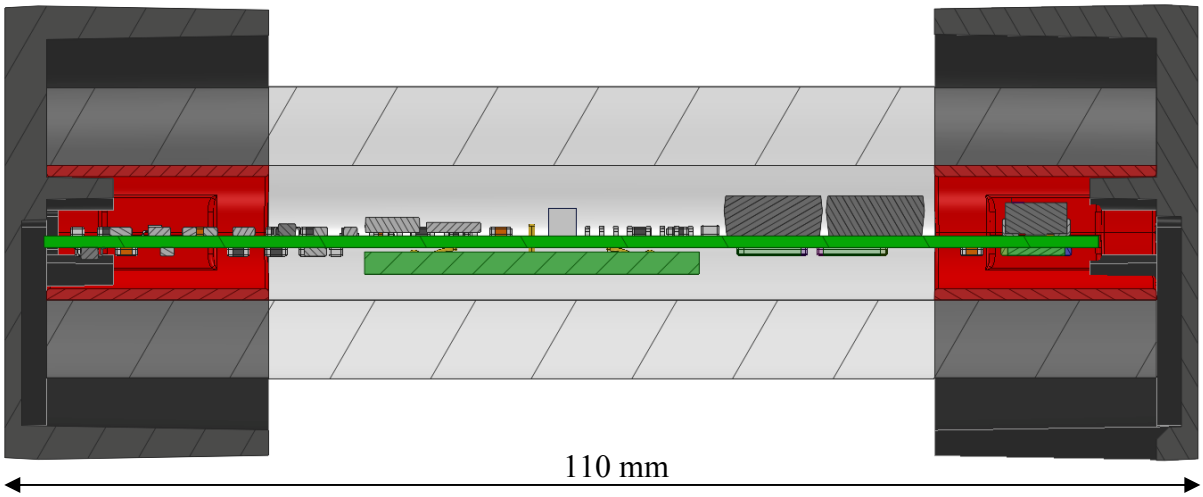


Figure 52: Cross section view of the DEAP actuator with integrated driver.

3.5.2 Prototype

The DEAP actuator with the modified winding inserts is prototyped together with the non-magnetic PT based driver. Figure 53 show a picture of the driver being integrated with the DEAP actuator. The final result is illustrated in figure 54: Proof of concept and the world's first low voltage DEAP actuator.

The mechanical performance of the integrated DEAP actuator is evaluated through a Stroke-Force measurement. The measurement is performed by preventing the

Figure 53: In process of slide the driver into the DEAP actuator.

Figure 54: World's first low voltage DEAP actuator

movement of the actuator, when applying the voltage. The actuator is then slowly released, while the force and stroke is measured. Stroke-Force measurements of the DEAP actuator, with and without driver integration, are shown in figure 55.

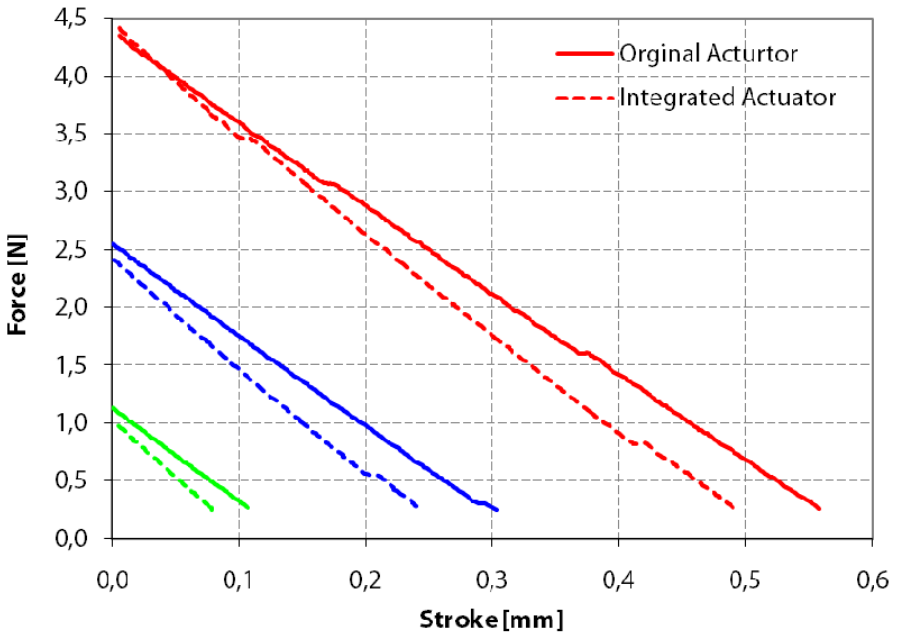


Figure 55: Stroke-Force measurement of the DEAP actuator, with and without driver integration, at different DEAP voltages. The small jumps are observed on the measurement. This is small burst from the driver, as the voltage drops due to the increase in capacitance, as the film is getting thinner. The driver will counteract this drop as it will maintain a constant output voltage.

The integration of the driver decreases the stroke performance by approximately 12%. This is due to increased tension and friction between the DEAP film and the driver. The DEAP film is not perfectly stretched inside the hollow section of the actuator and can therefore come in contact with parts of the stationary driver.

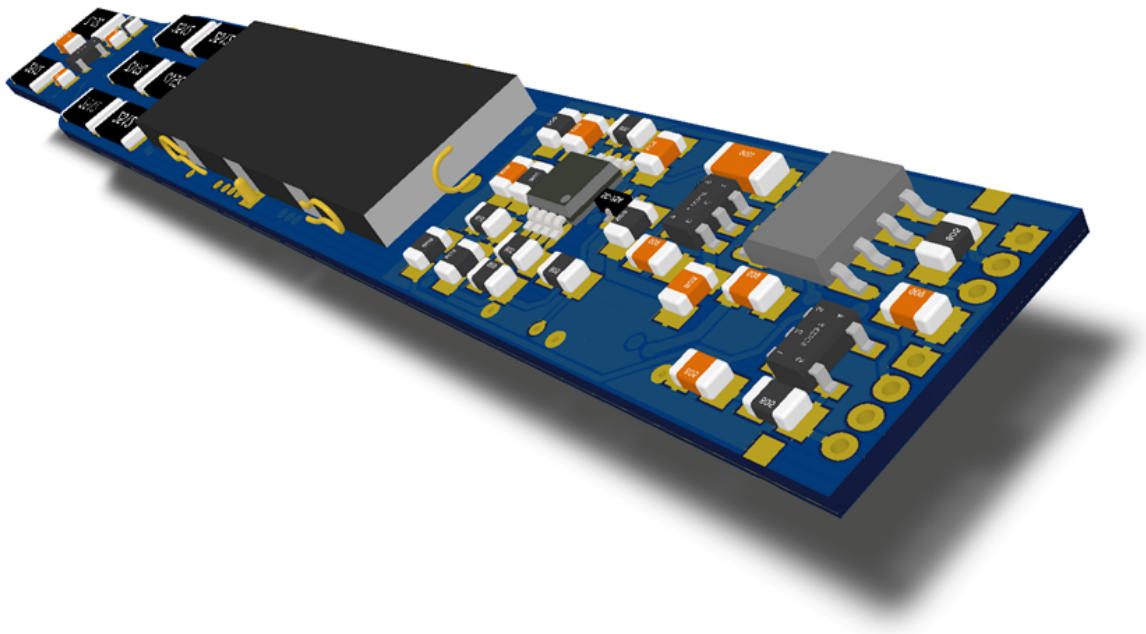
Furthermore small jumps can be observed on the measurements. This is small burst from the driver, as the voltage drops due to the increase in capacitance, as the film is getting thinner. The driver will counteract this drop as it will maintain a constant output voltage.

3.6 Summary

Table 4 summarises the performance of the EMT based driver and the PT based driver. Furthermore are the improvements of the PT based in comparison to the EMT based listed in percentage.

Table 4: Comparison of the EMT based and PT based driver and the improvements of the PT based.

	EMT based	PT based	Improvement
Box volume	80.334 mm^3	8.707 mm^3	89 % Smaller
Efficiency @ $Charge_{0\text{-}2kV}$	45 %	59 %	31 % Lower
Loss	99.6 mJ	56.8 mJ	43 % Lower
Power density	0.12 W/cm^3	0.48 W/cm^3	300 % Higher
EMI_{peak} @ f > 1 MHz	67.0 dBµV	41.3 dBµV	38 % Lower
Integrated	No	Yes	Yes
Non-magnetic	No	Yes	Yes



Chapter 4: Driver – bidirectional energy flow

Figure 56 illustrates a system combined of a driver and a DEAP actuator. It is relevant to evaluate the systems total efficiency (η_{tot}) as the ratio between mechanic energy (E_M) and the injected electric energy (E_{in}), see equation (16). For the unidirectional driver described in chapter 3 the input energy is forwarded to the DEAP actuator with a certain efficiency (η_f). The electromechanical coupling of the DEAP actuator (k) [63] determines the fraction of energy that is converted to available mechanic energy (E_M), however the conversion is not lossless and is given by a conversion efficiency (η_{Df}). The total efficiency of the unidirectional system (η_{uni}) is given by (17).

$$\eta_{tot} = \frac{E_M}{E_{in}} \tag{16}$$

$$\eta_{uni} = \frac{E_M}{E_{in}} = \eta_f \cdot \eta_{Df} \cdot k \tag{17}$$

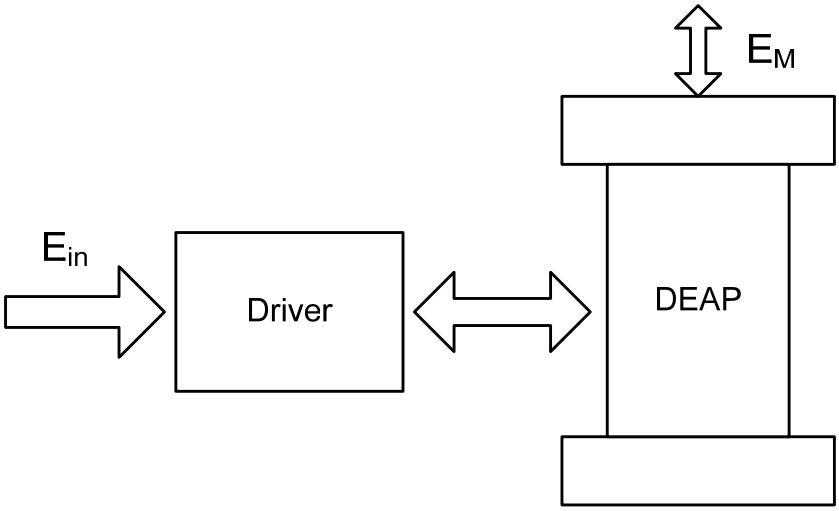


Figure 56: Total system efficiency for DEAP actuator and driver is defined by the ratio of available mechanic energy (E_M) to the injected electric energy (E_{in}).

For the unidirectional driver the energy stored in the DEAP actuator is simply discharged by dissipating the energy in a resistive load. However if the stored DEAP energy is recycled the total efficiency of the system is increased. Figure 57 illustrates the concept of the energy flow in a bidirectional driver connected to a DEAP

actuator. The energy available for recycling (E_{DEAP}) depends on the DEAP actuators reverse efficiency (η_{Dr}) and the stored energy. To recycle the energy of the DEAP actuator the driver must be able to reverse the energy flow to recover energy (E_r) that later can be used as a part of the forwarded energy (E_f). The full cycle system efficiency for the bidirectional system (η_{bi}) is derived in equations (18) to (20).

$$E_f = E_{in} + E_r \tag{18}$$

$$\eta_{bi} = \frac{E_M}{E_{in}} = \frac{E_f \cdot \eta_f \cdot \eta_{Df} \cdot k}{E_f - E_r} = \frac{E_f \cdot \eta_f \cdot \eta_{Df} \cdot k}{E_f - E_f \cdot \eta_f \cdot \eta_{Df} \cdot (1-k) \cdot \eta_{Dr} \cdot \eta_r} \tag{19}$$

$$\eta_{bi} = \frac{\eta_f \cdot \eta_{Df} \cdot k}{1 - \eta_f \cdot \eta_{Df} \cdot \eta_{Dr} \cdot \eta_r \cdot (1-k)} \tag{20}$$

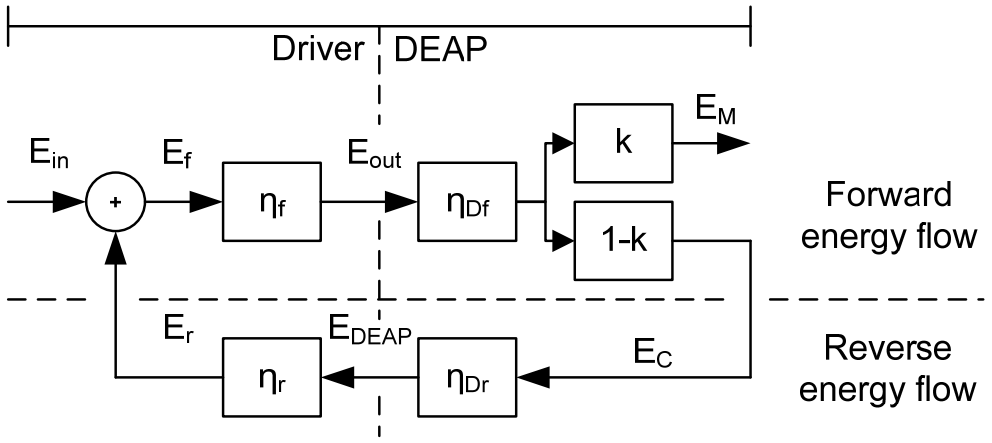


Figure 57: Energy flow in a system composed of a bidirectional driver and a DEAP actuator

4.1 Overview

A reverse energy flow through a PT requires switching on the secondary side. For the energy flow to be efficient the secondary side must be working in ZVS. However the PT design is optimized to ZVS with energy flow from low voltage to high voltage. ZVS is not directly possible if the energy flow is reversed, this becomes clear when evaluating the ratio between the electromechanical couplings coefficients of the PT working in reverse mode (12). Therefore a new PT design is required that is optimized for ZVS with energy flow from a high voltage to a low voltage and lead to a bidirectional solution with two PTs as shown in figure 58. One PT acts in a charging circuit and transfer energy from a low voltage to a high voltage, just like the

unidirectional driver. Another PT acts in a discharging circuit and transfer energy from a high voltage to a low voltage.

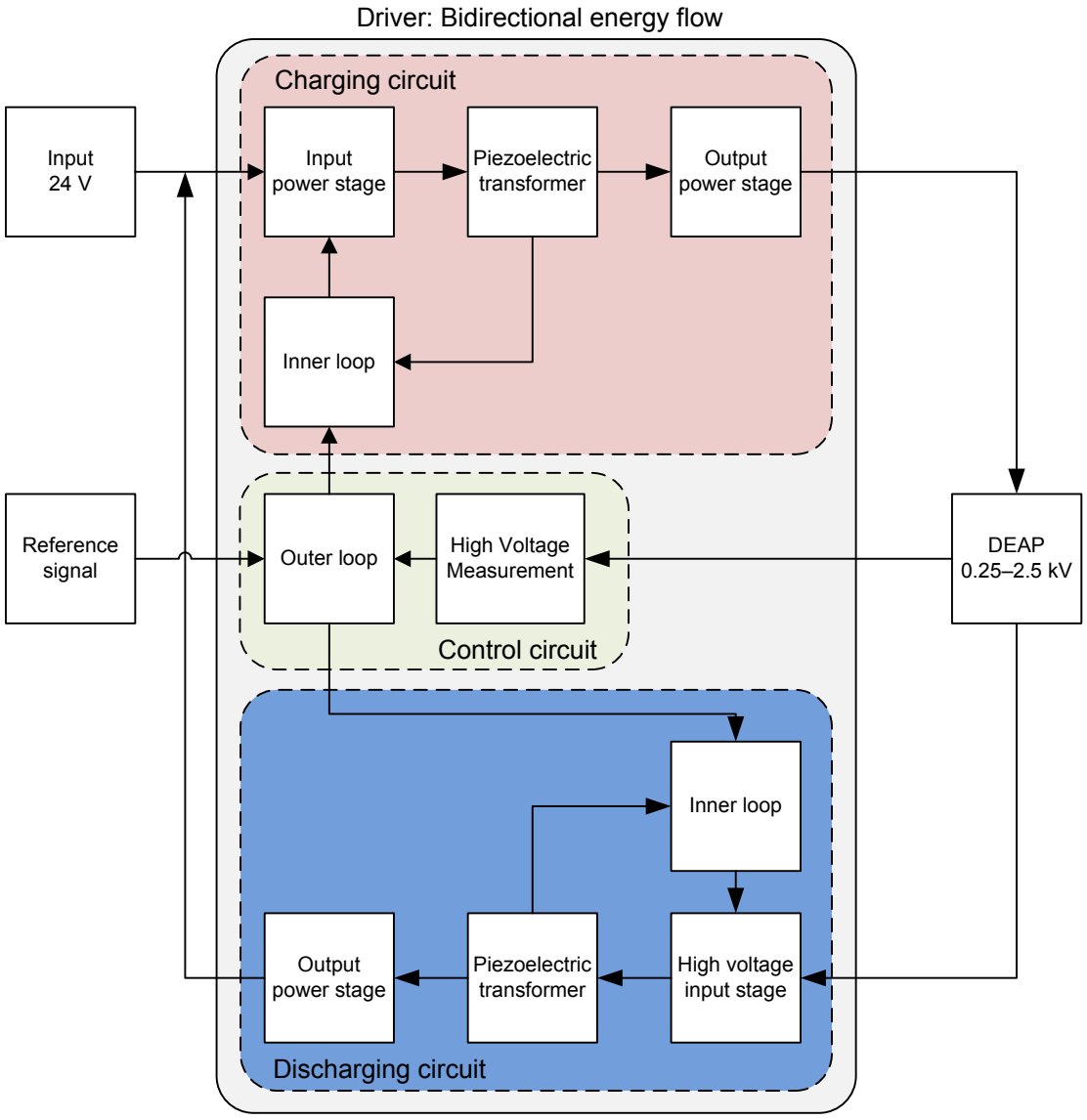


Figure 58: Block diagram of a bidirectional energy flow driver with two piezoelectric transformers.

From the PT theory of electromechanical couplings coefficients and their relations to the ZVS factor it is not possible to design a PT having a ZVS factor of 100 % or more in both directions. However, an elegant solution was invented based on phase-shift control. This solution requires only one PT to transfer energy forth and back. The phase-shift control ensures that ZVS is obtained at both primary and secondary side so high efficiency is maintain, but on the expense of a more complicated control

circuit compared to the solution with two PTs. Figure 59 illustrates the block diagram of the bidirectional driver with only one PT based on the invention [A10].

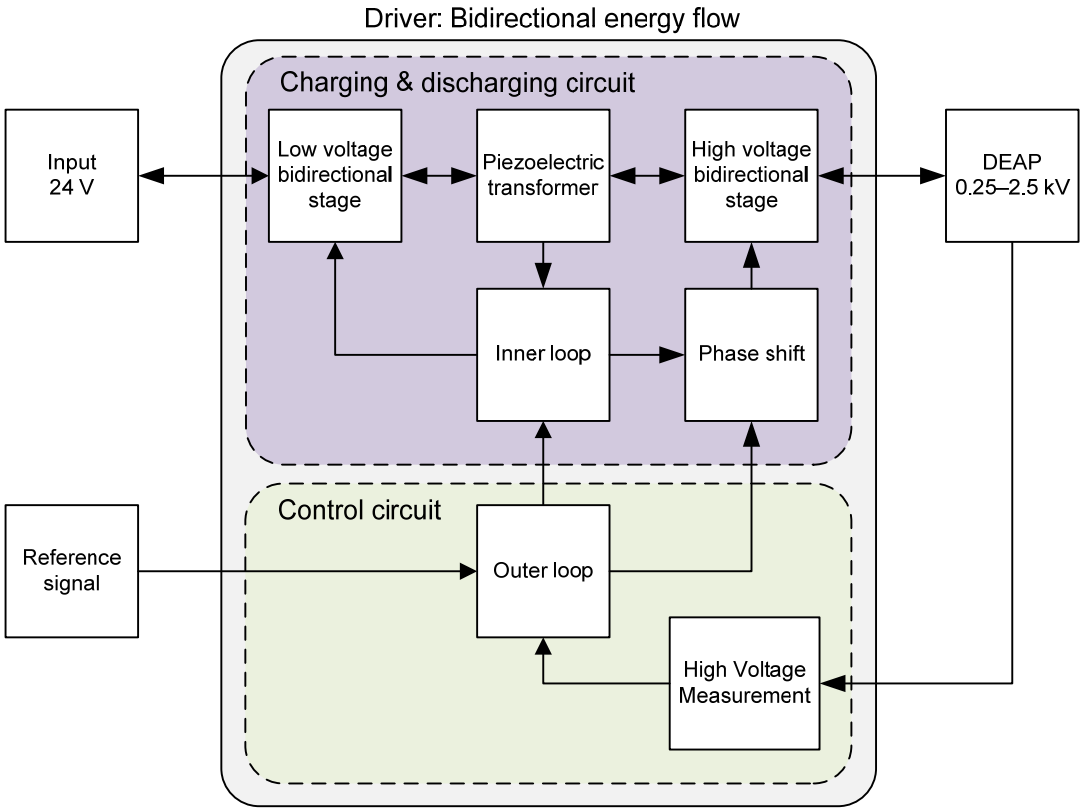


Figure 59: Block diagram of a bidirectional energy flow driver with one piezoelectric transformers and phase-shift control

4.2 Principle of the bidirectional PT topology

Figure 60 illustrates a principle schematic of the primary power stage, PT, secondary power stage and the electrical equivalent of the DEAP. Figure 61 shows the associated wave forms to describe the principle of the bidirectional PT topology.

The PT is optimized for ZVS at forward energy flow and is excitated from the primary half-bridge. This leads to ZVS operation of the primary side. Figure 61 illustrates the resulting waveforms on the secondary side and is divided into 5 sections. The energy transferred to the DEAP in one period (T) is given by the integral of the current through the high side switch (I_{D4}) and the voltage across the DEAP (21).

$$\Delta E = \int_{T} I_{D4} \cdot V_{HV} \tag{21}$$

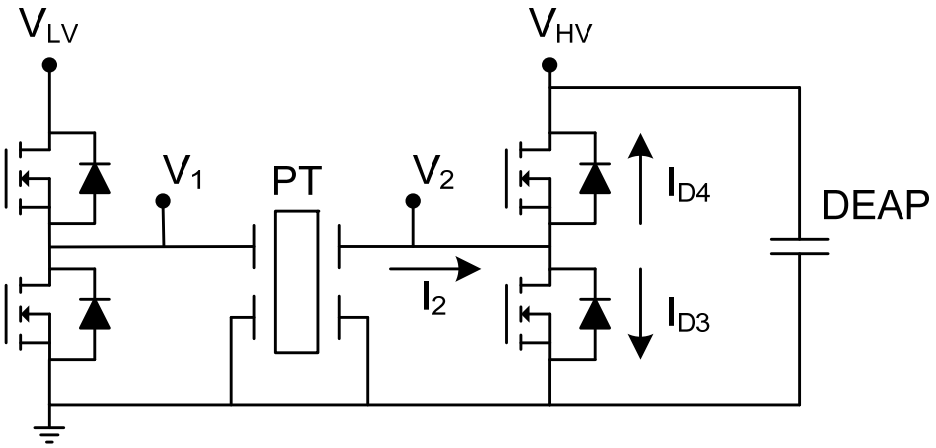


Figure 60: Simplified diagram of the bidirectional driver

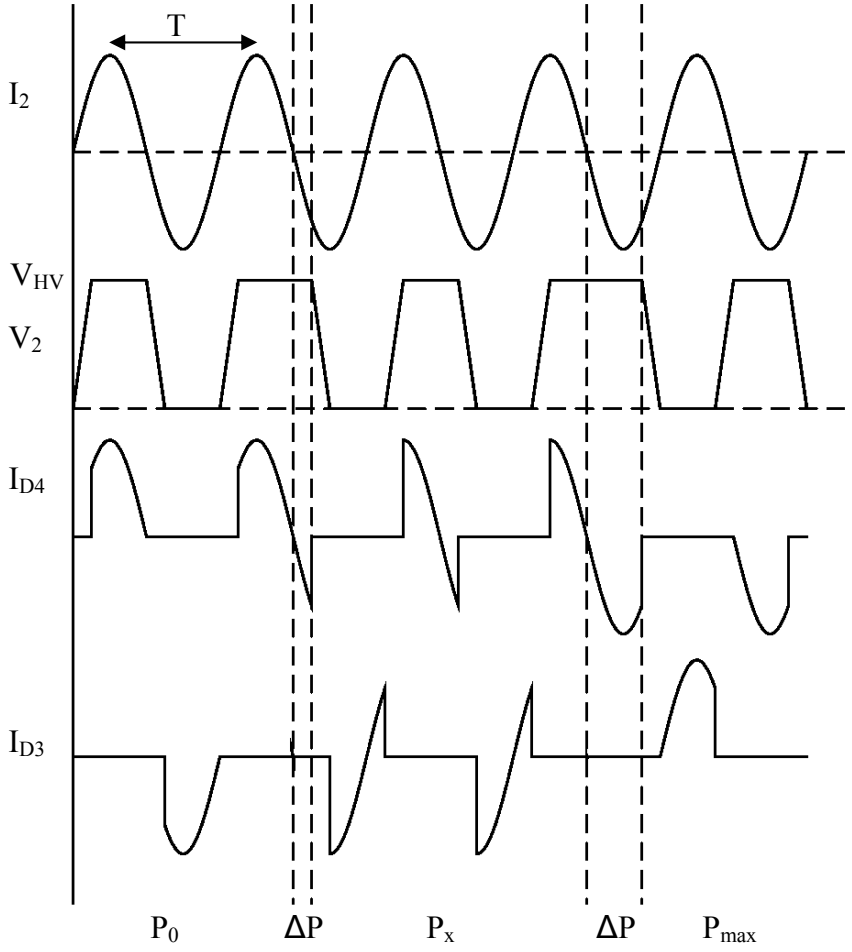


Figure 61: Principle wave forms of the bidirectional energy flow based on phase-shift.

The first section (P_0) illustrates the driver in normal operation with forward energy flow through the PT from the primary side to secondary side. Both the V_{HV} and I_{D4} are positive so according to equation (21) energy is transferred to the DEAP.

After the first section (P_0) a phase-shift (ΔP) is introduced to the control signals of the secondary switches. This prolongs the conduction time of the high side switch.

In the following section (P_x) the introduced phase-shift make the two secondary switches conduct a bit of reverse current before they turn off. The energy transferred to the DEAP can now be divided in two parts: Energy flowing into the DEAP when I_{D4} is positive and energy flowing out of the DEAP when I_{D4} is negative. The energy drawn out of the DEAP flows into the PT and is transferred back to the primary side.

By adding even more phase-shift (ΔP) to the control signals of the secondary switches one ends in the extreme case as seen in the last section (P_{max}). All the current in the high side switch (I_{D4}) is negative. Energy is only drawn from the DEAP in this section and flows back to the primary side. The driver operated in full reverse.

The relative phase-shift between the PTs output current (I_2) and the gate signals for the secondary sides switches determines; not only the direction of the net energy flow but also its magnitude.

A thorough description of the details about this invention is found in [A10].

4.3 Results – proof of concept

To prove the concept of a bidirectional driver a prototype has been developed with only one PT and active phase-shift control. The prototype is only meant as a *proof of concept* and therefore the output voltage is limited to avoid the challenges associated with half-bridge switching at 2.5 kV. Furthermore the size constraints regarding integration into the DEAP actuator are also omitted. Figure 62 shows a top view of the prototype with labels indicating the building blocks on the top of the PCB. The PT utilized for the bidirectional driver prototype is the more efficient interleaved thickness mode PT compared to the interleaved Rosen type PT utilized in the unidirectional driver.

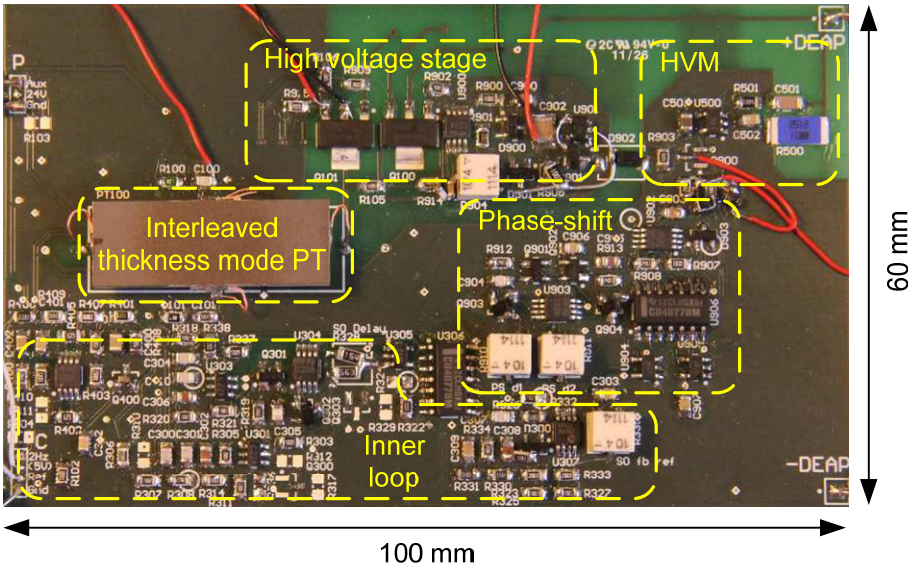


Figure 62: Proof of concept prototype of a bidirectional driver with phase shift control.

4.3.1 Efficiency measurements and comparison

Figure 63 illustrates the measurement setup for evaluating the efficiency of the bidirectional driver. Input voltage (V_{in}) and output voltage (V_{out}) are fixed at 24 volts and 300 volts respectively. Input current (I_{in}) and output currents (I_{out}) are measured at steady state operation. Table 5 lists the results of average power and efficiency for full forward energy flow and full reverse energy flow.

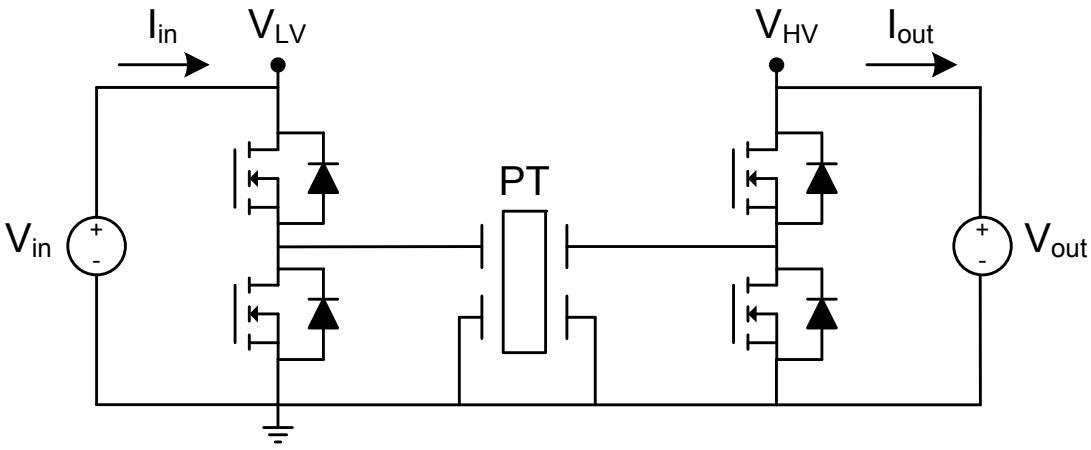


Figure 63: Setup used to evaluate the efficiency of the bidirectional prototype

Table 5: Measurements of efficiency for bidirectional prototype

Energy flow	Input	Output power	Efficiency
Full forward (η_f)	2.1 W	1.7 W	81 %
Full reverse (η_r)	-1.0 W	-1.4 W	71 %

The equivalent full cycle system efficiencies for the prototype connected to a DEAP actuator are calculated for unidirectional operation and bidirectional operation using equation (17) and (20) respectively. The results are listed in table 6 together with the improvement of bidirectional operation compared to unidirectional operation. The electromechanical coupling (k) of 2 % is a measured value of the DEAP actuator [64]. The improvement in system efficiency is more than a factor of two with bidirectional operation.

Table 6: Equivalent full system efficiencies for the bidirectional

Energy flow	η_f	η_r	$\eta_{Df} = \eta_{Dr}$	k	System efficiency
Unidirectional (η_{uni})	81 %	-	99.9 %	2 %	1.6 %
Bidirectional (η_{bi})	81 %	71 %	99.9 %	2 %	3.7 %
Improvement	-	-	-	-	131 %

4.4 High voltage bidirectional stage

The proof of concept prototype was designed with high voltage bidirectional stage limited in output voltage. Therefore a new high voltage bidirectional stage has been designed for operation up to 2.5 kV.

The power stage of the secondary side requires high voltage high frequency switching. Figure 64 illustrates one way of realizing the high voltage power stage: two switches in a half-bridge configuration and a half-bridge gate driver. The challenging parts of the high voltage high frequency power stage are the switches and the level-shifter for the gate driver.

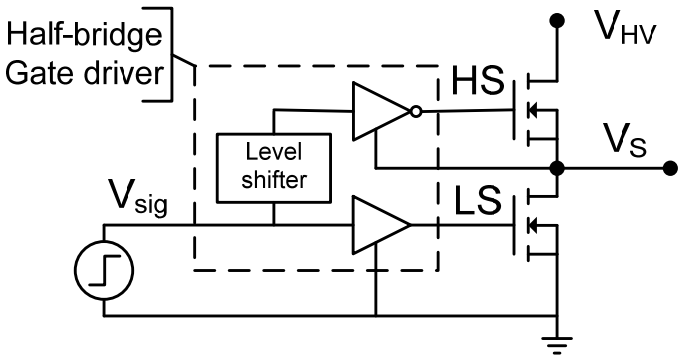


Figure 64: High voltage input stage in a half-bridge configuration with a half-bridge gate driver.

Each switch needs to handle voltage stresses of 2.5 kV. Furthermore the size of the switches has to be compact to be able to be integrated into the DEAP actuator. The best suitable switch found was a 2.5 kV MOSFET from IXYS: IXTV02N250S [65]

The level-shifter is a part of the half-bridge gate driver. A half-bridge gate driver consist of a level-shifter circuit and two ordinary gate driver circuits, one for the low side (LS) MOSFET and one for the high side (HS) MOSFET. The level-shifter circuit translate the logic ground referred input signal (V_{sig}) to an input signal for the HS gate driver with reference to the half-bridge voltage (V_S). The level-shifter must be non-magnetic, be compact, have low transition times, have low power consumption and be able to handle voltage stresses up to 2.5 kV.

A complete high voltage half-bridge stage based on a capacitive level shifter has been developed and operation is verified up to 2.44 kV with a 50 kHz switching frequency [A11]. Figure 65 illustrates the high voltage stage with capacitive level-shifter.

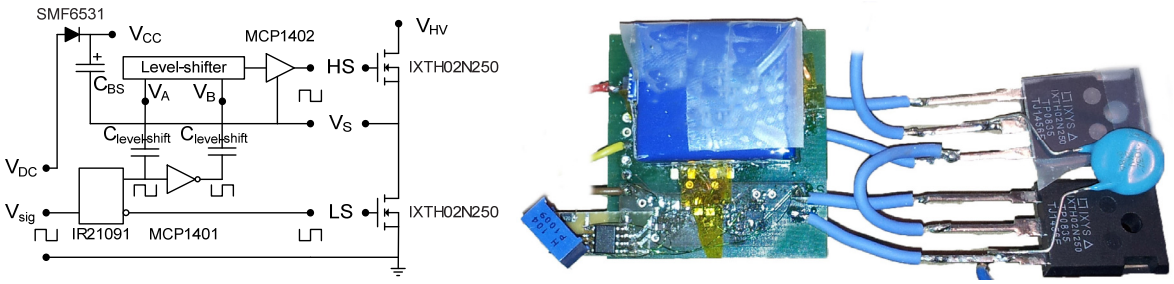


Figure 65: High voltage half-bridge stage verified up to 2.44 kV at 50 kHz switching frequency

The operation voltage of 2.44 kV was limited by the test power supply and not by the high voltage half-bridge stage itself. The upper switching frequency is limited to 700 kHz by the minimum dead time of the IR21091 chip. The total average current consumption of the gate driver including gate-source capacitance of MOSFETs is 3.6mA operating at 2.44kV@50kHz. The output capacitance of the gate driver alone is

around 4pF and mainly depended on the boot-strap diode and the physical volume of the high side circuit [A11].

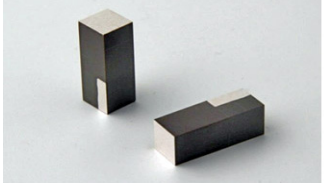
Chapter 5: Conclusion and future work

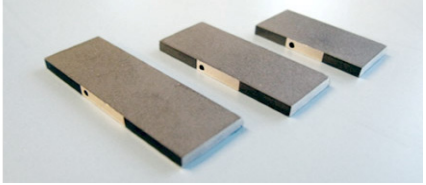
5.1 Conclusion

The work presented in this thesis and the associated publications are related to research within non-magnetic drivers for DEAP actuators. PT based drivers have proven to be feasible as a non-magnetic driver for DEAP actuators regarding size and efficiency compared to the existing driver based on an electromagnetic transformer (EMT).

5.1.1 Piezoelectric transformers

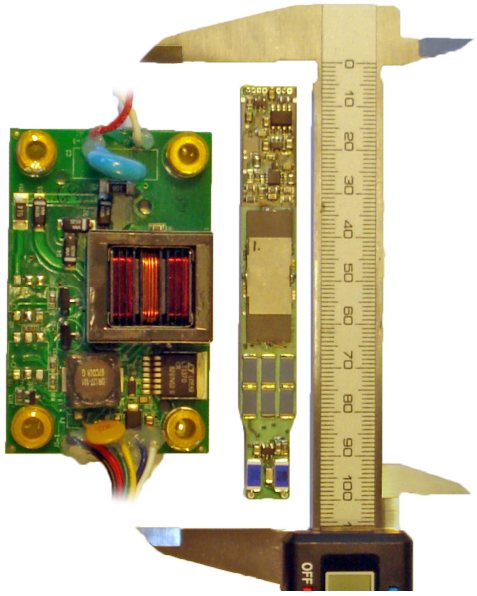
- Zero voltage switching (ZVS) is an essential part of high efficient PT based drivers. For a non-magnetic PT based driver the ZVS depends on the design of the PT itself. A better understanding of PTs and their electromechanical coupling, has lead to a more clear and transparent relation between a PT design and its ability to ZVS. As a result the soft switching capability of a specific PT design can be evaluated easily and directly from the lumped parameter model or the mechanic coupling coefficients.
- Piezoelectricity is a linear coupling between the electrical and mechanical domain, however temperature has influence on the piezoelectric material parameters and therefore nonlinear phenomena can be observed. A thermo-electric model has been derived to aid in a better understanding of these nonlinear phenomena which are more pronounced for PTs with high power density.
- FEM tools have been proven to be able to speed up the process of PT design. Methods to speed up FEM simulation of PT is derived based on dimension reduction and layer transformation.
- PT designs with high step-up ratios have been known for over 50 years since the Rosen type PT. Rosen type PTs are not able to ZVS and therefore very inefficient in a non-magnetic application. New PT designs with high step-up ratio have been developed with focus on efficiency and ZVS factor. The results are interleaved PT designs optimised for ZVS with high step-up ratios and high efficiency.





A nonmagnetic PT based driver is developed with improvements in volume, efficiency, loss, power density and conducted EMI.

Improvement of PT based vs. EMT based	
Box volume	89 % Smaller
Efficiency @ $Charge_{0\text{-}2kV}$	31 % Lower
Loss	43 % Lower
Power density	300 % Higher
EMI_{peak} @ f > 1 MHz	38 % Lower
Integratable	Yes
Non-magnetic	Yes



- To ensure high efficiency of the PT based driver a *self-oscillation* loop closed around the PT is utilized to maintain the PTs operation point of ZVS.
- To control the power flow of the unidirectional PT based driver an outer loop utilizing *burst mode technique* is implemented. Thereby the power flow is controlled without compromising efficiency but on the expense of more output voltage ripple.

5.1.3 World's first low voltage DEAP actuator

As a result of the compact size of the developed PT based driver it has been possible to integrate the driver into a tubular DEAP actuator. Thereby the high voltage interface to the DEAP actuator is removed and replaced with a 24 volts interface.

- The world's first low voltage DEAP actuator has been created.
- The low voltage DEAP actuator is fully functional, but with 12 % of performance reduction from internal friction between driver and the DEAP film.

5.1.4 Bidirectional PT based driver

A bidirectional driver is able to recycling the electric energy stored in the DEAP actuator instead of dissipating it as heat. By energy recycling the total system efficiency from electric energy to mechanic energy is increased.

- A bidirectional driver topology is developed. By introducing *active phase-shift control* of the secondary side high efficient bidirectional energy flow is obtained for the PT. Thus using only one PT in this topology.
- Total system efficiency from electric energy to mechanic energy is increased by a factor 2.3 with energy recycling.
- A nonmagnetic 2.5 kV half-bridge gate driver is developed to increase the output voltage of the bidirectional proof of concept prototype. The developed half-bridge gate driver is verified at 2.44 kV @ 50 kHz.

5.2 Perspective & Future work

- A nonmagnetic bidirectional driver with an output voltage up to 2.5 kV still needs to be demonstrated. One solution could be to combine the proof of concept prototype with the developed high voltage half-bridge stage.
- Major parts of the control circuit of the bidirectional driver might be merged in to an integrated circuit (IC). This IC together with naked dies versions of the high voltage MOSFTEs would reduce the size of the bidirectional driver. Integration with the DEAP actuator would then be possible.
- FEM modeling is a strong tool in the development of PT designs. The introduction of complex electrode arrangement (e.g. interdigitated electrodes (IDE)) leads to inhomogeneous material polarization. Further research into modeling of inhomogeneous material polarization would be beneficial in the development of PTs.
- Introduction of *active phase-shift control* to achieve bidirectional energy flow gives new perspectives within the design of PTs. *Active phase-shift control* increase the apparent ZVS factor of a PT. A combination of a PT design with a ZVS factor below zero and *Active phase-shift control* would be able to achieve ZVS. *Active phase-shift control* might lead to new design approaches of PTs, as the ZVS factor of a PT design is obtained at the expense of power density. Further research is needed before a conclusion can be drawn.

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Appendix A: Publication list

Overview of publications accomplished during this PhD study. The publications are located in appendix A.

[A1] **T. Andersen**, M. A. E. Andersen and O. C. Thomsen, "Simulation of piezoelectric transformers with COMSOL", submitted to COMSOL, 2012.

[A2] M. S. Rødgaard, **T. Andersen** and M. A. E. Andersen, "Empiric analysis of zero voltage switching in piezoelectric transformer based resonant converters", in PEMD, 2012.

[A3] M. S. Rødgaard, **T. Andersen**, K. S. Meyer and M. A. E. Andersen, "Design of interleaved multilayer Rosen type piezoelectric transformer for high voltage DC/DC applications", in PEMD, 2012.

[A4] M. S. Rødgaard, **T. Andersen**, K. S. Meyer and M. A. E. Andersen, "Design of Interleaved Interdigitated Electrode Multilayer Piezoelectric Transformer utilizing longitudinal and Thickness mode vibrations", submitted to PECON, 2012.

[A5] **T. Andersen**, M. A. E. Andersen O. C. Thomsen, M. P. Foster and D. A. Stone, "Nonlinear Effects in Piezoelectric Transformers Explained by Thermal-Electric Model Based on a Hypothesis of Self-Heating", submitted to IECON, 2012.

[A6] **T. Andersen**, M. S. Rødgaard and M. A. E. Andersen, "Active Match Load Circuit Intended for Testing Piezoelectric Transformers", in PEMD, 2012.

[A7] K. S. Meyer, M. S. Rødgaard, **T. Andersen** and M. A. E. Andersen, "Self-oscillating loop based piezoelectric power converter", US Patent, US application no. US61/638,883, 2012.

[A8] **T. Andersen**, M. S. Rødgaard, O. C. Thomsen and M. A. E. Andersen, "Low voltage driven dielectric electro active polymer actuator with integrated piezoelectric transformer based driver", in SPIE, 2011, p. 79762N.

[A9] **T. Andersen**, M. S. Rødgaard, M. A. E. Andersen, O. C. Thomsen, K. P. Lorenzen, C. Mangeot and A. R. Steenstrup, "Integrated high voltage power supply utilizing burst mode control and its performance impact on dielectric electro active polymer actuators", accepted for Actuator, 2012.

[A10] M. A. E. Andersen, K. S. Meyer, M. S. Rødgaard and **T. Andersen**, "Piezoelectric power converter with bi-directional power transfer", Patent, US application no. US61/567,924, and EU application no. EP11192356, 2011.

[A11] **T. Andersen**, M. A. E. Andersen O. C. Thomsen, M. P. Foster and D. A. Stone, "A capacitive level shifter for high voltage (2.5kV), accepted for IPMHV & submitted to IEEE Transactions on Power electronics, 2012.

Appendix: A1

T. Andersen, M. A. E. Andersen and O. C. Thomsen, "Simulation of piezoelectric transformers with COMSOL", submitted to COMSOL, 2012.

Simulation of Piezoelectric Transformers with COMSOL

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Abstract:

In this work COMSOL is utilized to obtain the Mason lump parameters for a piezoelectric transformer (PT) design. The Mason lump parameters are relevant in the design process of power converters. The magnitude of the impedance is simulated for a specific PT: interleaved multilayer thickness mode transformer. Interleaved indicates that the primary section of the PT has been interleaved into the secondary section. Furthermore the primary section is build with interdigitated electrodes (IDE). The PT design has been prototyped and the measurements results are compared with simulations.

Two methods for simplifying the PT model are given in order to decrease the simulation time.

This paper aims to aid electrical engineers with poor knowledge within the field of mechanics, to be able to simulate a PT design with COMSOL and extract the electrical key parameters.

Keywords: Model, Simplification, IDE, Mason, COMSOL Multiphysics 4.2a.

1. Introduction

Within power electronic electromagnetic transformers have been the dominating component for converting and transfer of power. The trend of power converters goes in the direction of higher efficiency and smaller volume. Research has shown that piezoelectric transformers (PT) can compete with traditional electromagnetic transformers on both efficiency and power density [1-4]. PTs are therefore an interesting field of research.

A PT utilizes two interconnected piezoelectric elements. One is set into motion, by the inverse piezoelectric effect, and the other is harvesting the energy from the motion by the direct piezoelectric effect. By proper design the PT is capable of transferring energy. The conversion ratio is given by geometry, polarization and placement of electrodes. The piezoelectric constitutive equations [5] in stress-charge form is given by equation (1) and (2). These equations describe the relation between the mechanical and the electrical. The symbols are explained in Table 1.

$$T = c^E \cdot S - e \cdot E \quad (1)$$

$$D = e \cdot S + \varepsilon^S \cdot E \quad (2)$$

Table 1 piezoelectric constitutive equation symbols

T	Stress	[N/m^2]
S	Strain	-
D	Electric displacement	[C/m^2]
E	Electric field	[V/m]
c^E	Elastic stiffness at const. electric field	[Pa]
e	Piezoelectric constant	[C/m^2]
ε^S	Permittivity at const. strain	[F/m]

From the constitutive equations analytic equations can be derived to solve piezoelectric problems e.g. PTs. In this work COMSOL 4.2a and the module "*Piezoelectric Devices*" (pzd) is utilized to solve the piezoelectric problem based on the constitutive equations.

This paper aims to aid electrical engineers with poor knowledge within the field of mechanics, to be able to simulate a PT design with COMSOL and extract the electrical key parameters.

2. Piezoelectric transformers

In this chapter the basic of PTs are revealed with focus on electrical parameters.

PTs are based on a piezoelectric material. This material has an electromechanical coupling and through this coupling a charge displacement is generated, which is proportional to the deformation of the material. A PT is basically two piezoelectric elements which is joined together to form a transformer. The primary side element is then exited by an electrical AC voltage, which induces a deformation of the two

joined elements. This deformation generates an output voltage on the secondary side element. With a proper design of the PT a desired voltage conversion can be obtained from the primary to the secondary side.

In order to convert power at a high efficiency, the PT is operated in one of its resonance modes [4, 6-8]. The PT resonates each time it is possible to generate a standing wave in the element. But the design is usually optimised for one specific resonance mode, in order to obtain the highest efficiency [6, 8].

The PT resembles a distributed network, but for simplicity and mathematical representation, only the resonance mode of interest is modelled. One of the most used PT models is the lumped parameter model, which was derived by Mason in 1942 [9] and is illustrated in Figure 1.

For a PT based converter-design's point of view the values of interest is the lump parameters of figure 1. The Mason lumped parameters can be calculated in the frequency domain from the primary's and secondary's magnitude of the input impedance [7, 10]. An example of a magnitude plot for the Mason equivalent with the secondary or the primary side shorted is illustrated in figure 2. Three points for each section (six in total) are necessary to calculate the lump parameters: a low frequency (f_0) magnitude (Z_0), far below the frequency of the first resonance mode, magnitude (R) at the resonance frequency (f_z) and the anti-resonance frequency (f_p). From these values the lump parameters are calculated using equation (3) to (10).

$$R = Z_{pri}\left(f_{z\,pri}\right) \tag{3}$$

$$C_{T_{pri}} = \frac{1}{2\pi f_{0\,pri} Z_{0\,pri}} \tag{4}$$

$$C_{T_{\sec}} = \frac{1}{2\pi f_{0_{\sec}} Z_{0_{\sec}}} \tag{5}$$

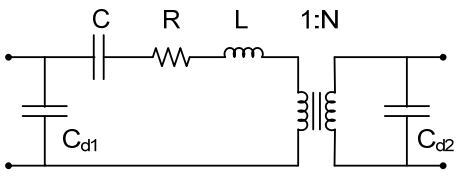

Figure 1 Lumped parameter model, which describes the behaviour of the PT in a narrow band around the operating resonance mode.

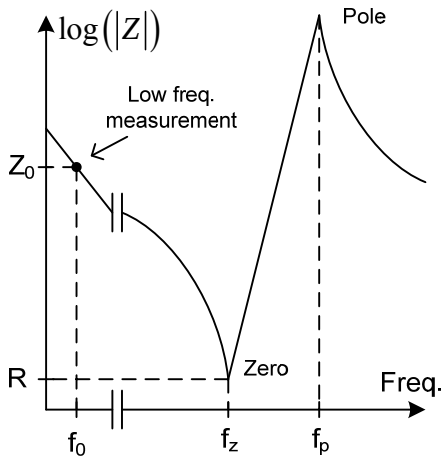

Figure 2 Magnitude plot of a PT around a resonance mode with either secondary or primary section shorted.

$$C_{d1} = C_{T_{pri}}\left(\frac{f_{z\,pri}}{f_{p\,pri}}\right)^2 \tag{6}$$

$$C_{d2} = C_{T_{\sec}}\left(\frac{f_{z_{\sec}}}{f_{p_{\sec}}}\right)^2 \tag{7}$$

$$C = C_{T_{pri}} - C_{d1} \tag{8}$$

$$L = \frac{1}{\left(2\pi f_{z\,pri}\right)^2 C} \tag{9}$$

$$N = \sqrt{\frac{1}{\left(2\pi f_{Z_{\sec}}\right)^2\left(C_{T_{\sec}} - C_{d2}\right)\cdot L}} \tag{10}$$

From the lump parameters other PT related properties can be calculated : resonance frequency (11), match load (12), efficiency in match load (13), soft switching factor or ZVS factor (14). Derivation of the equations can be obtained from the following references [11, 12].

$$f_r \approx \frac{1}{2\pi\sqrt{L\cdot C}} \tag{11}$$

$$R_m = \frac{1}{2\pi f_r C_{d2}} \tag{12}$$

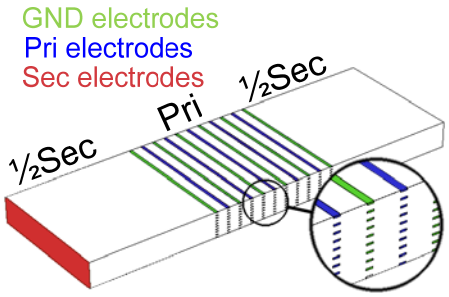

Figure 3 Sketch of the PT design with simplified primary section build-up:10 layer, 10 sheet.

$$\eta_m \approx 1 - \frac{2RC_{d2}N^2}{\sqrt{LC}} \qquad (13)$$

$$V_P' = \left(0.304 \cdot \frac{N^2 C_{d2}}{C_{d1}} + 0.538\right)\left(0.585 \cdot \eta + 0.414\right) \qquad (14)$$

3. PT geometry

In this chapter the geometry of the PT design is shown. The thoughts and calculations behind the geometry are out of the scope of this work and will not be discussed.

The specific PT design is indented for high voltage output applications. The design is an interleaved multilayer thickness mode transformer, indicates that the primary section of the PT has been interleaved into the secondary section. Furthermore the primary section is build with interdigitated electrodes (IDE) to allow tape casting manufacturing process. The transformer is build up by 60 piezoelectric ceramic sheets of 30µm in thickness after sintering, leading to a total height of about 2mm. Each sheet is printed with conducting IDE, the width of each electrode is 50µm, the distance between each electrode is 200µm and the edge margin is 0.33mm. The IDE divides the primary section into 40 layers with a primary section width of 10.07mm. The total width of the PT is 30.24mm and the depth is 10.0mm. A simplified sketch of the PT is shown at figure 3 with only 10 layers instead of 40 also electrode margin is not included.

The electrical equivalent of the PT design is basically the same as the Mason model. However the split secondary is model with a 2 winding center tap transformer on the secondary side. From the electrode arrangement the center tap is then grounded. Figure 4 illustrates the electrical equivalent of the interleaved PT design.

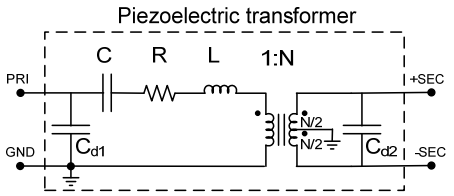

Figure 4 Electrical equivalent of the interleaved PT design.

Table 2 PT geometry specifications

W	30.0 [mm]	Total width
H	2.0 [mm]	Total height
D	10.0 [mm]	Total depth
Wp	10.1 [mm]	Primary section width
Lp	40	Primary layers
We	50 [µm]	Electrode width
He	8 [µm]	Electrode height
Wd	200 [µm]	Electrode distance
Lt	60	Tape layers
Ht	33 [µm]	Sintered tape thickness

4. COMSOL

In this chapter the impedance plots, necessary for obtaining the Mason lump parameters, are simulated in COMSOL for the specified PT geometry.

For simulating the PT design in COMSOL the "*Piezoelectric Devises (pzd)*" physics under structural mechanic is used. The study type required for a frequency sweep is the "*Frequency Domain*".

4.1 Material parameters

The piezoelectric material parameters are derived from Ferroperm's PZ26 [13]. Material parameters for the polarized material are shown in (15) (16) (17) and (18).

Losses for the material are included by adding "*Damping and Loss*" under the "*Piezoelectric Material Model*". Good experience is observed with Rayleigh damping with the value from (19).

4.2 Polarization

$$\rho = 7700\left[\frac{kg}{m^2}\right] \quad (15)$$

$$c^E = \begin{bmatrix} 16.8 & 11.0 & 7.85 & 0 & 0 & 0 \\ & 16.8 & 7.85 & 0 & 0 & 0 \\ & & 12.2 & 0 & 0 & 0 \\ & & & 3.01 & 0 & 0 \\ & & & & 3.01 & 0 \\ & & & & & 2.88 \end{bmatrix} \cdot 10^{10} \quad (16)$$

$$e = \begin{bmatrix} 0 & 0 & 0 & 0 & 9.86 & 0 \\ 0 & 0 & 0 & 9.86 & 0 & 0 \\ -2.8 & -2.8 & 17.7 & 0 & 0 & 0 \end{bmatrix} \quad (17)$$

$$\varepsilon^S_{relative} = \begin{bmatrix} 828 & & \\ & 828 & \\ & & 1282 \end{bmatrix} \quad (18)$$

$$\begin{aligned} \alpha_{dM} &= 0 \\ \beta_{dK} &= 1.11e-9 \end{aligned} \quad (19)$$

Before a material has piezoelectric behaviour the material needs to be polarized. The poling process usually implies a high electrical field to the material that will align the electric dipoles in the same direction and hence the electromechanical coupling arises [14].

The default polarization direction of piezoelectric material in COMSOL is along the z-axis. To change the poling direction it is necessary to define a new coordinate system under "*Definitions*". Figure 5 illustrates effect of different poling directions by applying a DC voltage across the material.

The poling directions of the PT are shown for a simplified 4 layer PT model in figure 8 together with electrodes. The blue and green volumes are space taken by piezoelectric ceramic and electrode material. However the piezoelectric ceramic in the blue and green-colored volumes are not able to be polarized and is referred to as inactive material. For inactive (not polarized) material the parameters of the piezoelectric material changes, however it is assumed that inactive material can be modeled as

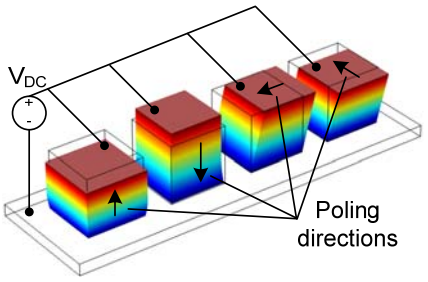

Figure 5 Simulation of four piezoelectric cubes on a conducting plate subjected to a voltage much lower than poling voltage. The electric potential is given by the colors. Deformation depends on the poling direction of the material.

polarized material except that the piezoelectric coupling matrix (17) is zero.

4.3 Electrode boundary conditions

For simulating the impedance of the primary side the electrode of the secondary (Sec) must be shorted. One way of connecting two or more electrodes together is by use of the "*Floating potential*" condition. The selected boundaries are then electrical connect without specifying an actual voltage. The ground (GND) electrodes are set by the "*Ground*" condition and the primary (Pri) electrodes are set by the "*Electrical potential*" condition.

For simulating the impedance of the secondary side the primary (Pri) and ground (GND) electrodes must be shorted together with the "*Floting potential*" condition. One of the secondary electrodes is connected to the "*Ground*" condition while the other is connected to the "*Electrical potential*" condition.

4.4 Model simplification and transformation

Simplification of a model in COMSOL can reduce the simulation time by decades with only little effect on the results. Simplification is therefore important. There are two major ways to simplify a PT design: Dimension reduction and layer reduction. Both reductions are done by transforming the geometry. The resulting impedance plots are then inverse-transformed to reflect the results of the non-transformed geometry.

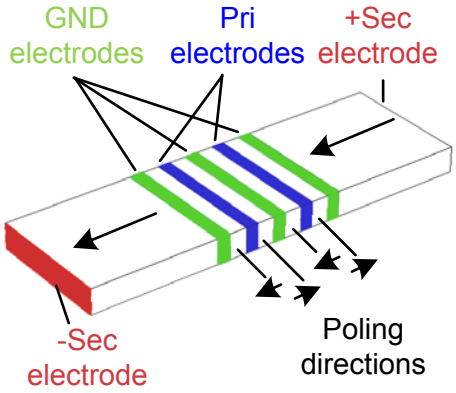

Figure 8 Simplified PT model with 4 primary layers, illustrating poling directions (arrows) and electrodes (gray area).

Dimension reduction is a 2-dimension model of 3-dimension geometry. In a 2-dimension model the third dimension of the PT is equal to one meter. To obtain the correct impedance plot (Z) the 2-D impedance plot (Z_{2D}) is divided by the actual depth (d_z) of the PT in the third dimension (20).

$$Z(f) = \frac{Z_{2D}(f)}{d_z} \tag{20}$$

Layer reduction is another way of simplify the geometry in order to speed up the simulation time. Layer reduction can be applied in both 3-D and 2-D models. Figure 8 illustrates an example of layer reduction applied for the primary section. The original design has 40 primary layers but is reduced to 4 primary layers. The impedance of a layer reduced section (Z_{LR}) is transformed to a full layer section impedance (Z) by the square of the ratio between the amount of layers in the reduced section (L_{LR}) and the amount layers without reduction (L) (21).

$$Z(f) = Z_{LR}(f) \cdot \left(\frac{L_{LR}}{L}\right)^2 \tag{21}$$

5. Results

In this chapter the results from measurements and simulations are compared for the PT design. The results of interest are the lump parameters of the Mason model (see figure 1) for the first mode of resonance. Impedance plots are measured and simulated for both primary and the secondary side in order to derive the lump parameters.

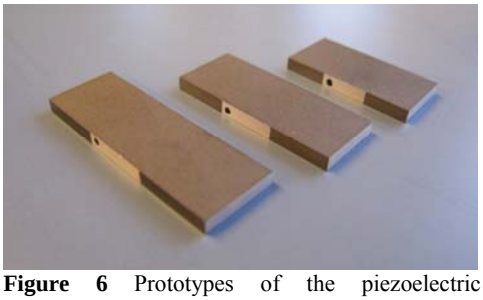

Figure 6 Prototypes of the piezoelectric interleaved multilayer thickness mode transformer of different sizes: 30 mm, 25mm and 20 mm.

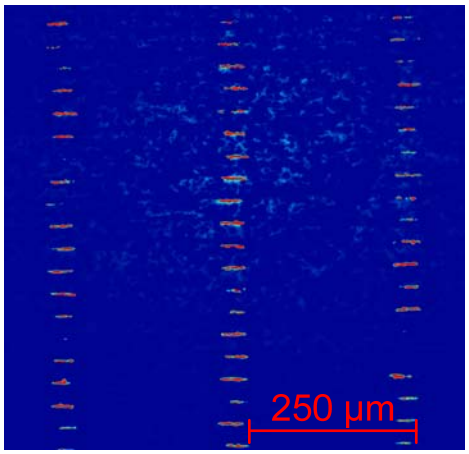

Figure 7 PT 30mm design: Cross-section view of primary electrodes under microscope. Image colors are post processed. Red colors are IDE electrodes.

Figure 6 show a picture of piezoelectric interleaved multilayer thickness mode transformer in three sizes. The PT to the right in the picture is designed after the specifications in Table 2. However the total width of the PT is 30.24 mm. This width is used for the later COMSOL simulations.

Figure 7 is a microscope image of the primary cross section, the red lines are the IDE electrodes. The image verifies the electrode width (We), electrode height (He) and electrode distance (Wd).

Figure 9 shows a simulation of the PT displacement at its first resonance mode. The displacement is exaggerated by a factor of 10^8 for the purpose of illustration. The dark blue area

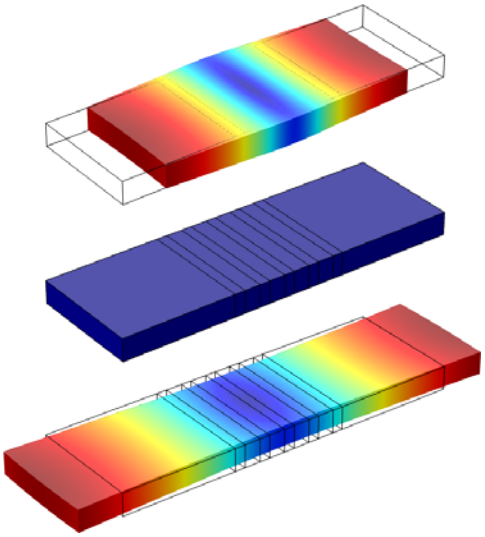

Figure 9 Simulation of displacement at first resonance mode 53.0kHz at phase 0° (top), 90° (middle) and 180° (bottom). Displacement is scaled by a factor of 10^8.

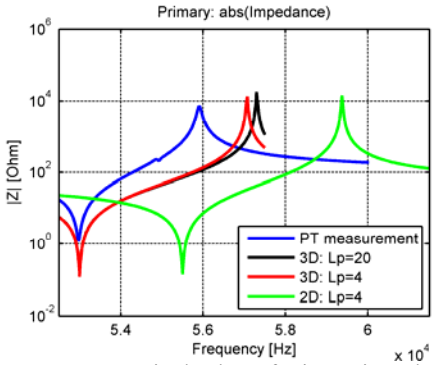

Figure 10 Magnitude plots of primary impedance.

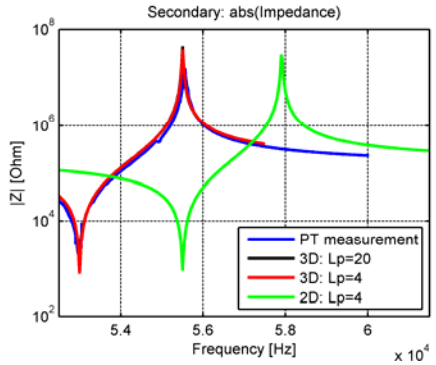

Figure 11 Magnitude plots of secondary impedance.

where movement is almost zero.

The impedance magnitude plot around resonance frequency is measured for the PT prototype with a network analyzer.

In COMSOL the impedance magnitude plots are obtained by simulating the magnitude of the ratio between voltage and current for the electrodes of interest over a range of frequencies. The electrode voltage (V) is defined by its boundary condition and for the same electrodes the current is calculated by a surface integral of the inward current ("*pzd.nJ*"). Equation (22) gives the magnitude of the impedance.

$$|Z| = abs\left(\frac{V}{\iint_{surface} pzd.nJ}\right) \qquad (22)$$

Magnitude of the primary impedance is plotted in Figure 10 and magnitude of the secondary is plotted in Figure 11, the low frequency measurement is not shown at the plots. In COMSOL the PT is simulated with different model simplifications:

No. 1. PT measurement
No. 2. 3D, 20 primary layers
No. 3. 3D, 4 primary layers
No. 4. 2D, 4 primary layers

The corresponding lump parameters are calculated in Table 3.

Table 3 Resulting lump parameters

	No. 1	No. 2	No. 3	No. 5
R [Ω]	1.19	0.12	0.12	0.14
C [nF]	2.71	8.98	9.10	8.01
L [mH]	3.33	1.00	0.99	1.03
C_{d1} [nF]	23.8	53.2	57.0	55.4
C_{d2} [pF]	15.1	14.4	14.4	14.0
N	42.5	80.3	80.8	80.4
f_r [kHz]	54.3	54.3	54.3	56.7
R_m [kΩ]	195	203	203	200
η_m [%]	97.9	99.2	99.2	99.1
V'_p [%]	99.0	153	145	143

6. Discussions

By comparing the results some general trends can be observed. Evaluating the results from the

magnitude of the impedance plots; Starting with the secondary side: a good correlation between measurement and the 3D simulations, however the 2D simulation is shifted a bit in frequency.

Comparing the magnitude of the primary impedance shows that the measurement and the 3D simulations share the same resonance frequency but the anti-resonance frequency is higher for the 3D simulations which is equivalent to a higher effective coupling factor [5]. Again, the 2D simulation is shifted in frequency compared to the 3D simulations. The magnitude at resonance frequency is to optimistic for all the simulations, a higher Rayleigh damping values (19) is required then. Also the number of primary layers has an effect on the anti-resonance frequency.

The results from the different simulation models are expected to be close to equal. The variation of the individual lump parameters are also below 8 % in worse case.

The higher deviation observed from secondary to primary is a combination of model complexity and material parameters. The primary section has a complex electric field distribution around the IDE electrodes which again leads to a non-constant and multi direction polarization of the material. The material parameters are affected by the "degree" of polarization therefore a much more complicated model of the PT and the material parameters are need to obtain better correlation of results.

7. Conclusions

A PT design is simulated using COMSOL with focus on extracting electric key parameters in order to construct the Mason equivalent model of the PT. Methods to simplify PT models in order to speed up simulation time is given. In this work the simplification errors is less than 8% in worse case. Experimental measurements indicate that care has to be taken about polarization and material parameters when simulating PTs with complex electrical field distributions.

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Appendix: A2

M. S. Rødgaard, **T. Andersen** and M. A. E. Andersen, "Empiric analysis of zero voltage switching in piezoelectric transformer based resonant converters", in PEMD, 2012.

EMPIRIC ANALYSIS OF ZERO VOLTAGE SWITCHING IN PIEZOELECTRIC TRANSFORMER BASED RESONANT CONVERTERS

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Keywords: Piezoelectric Transformer, inductor-less, converter, soft switching, ZVS factor

Abstract

Research and development within piezoelectric transformer (PT) based converters are rapidly increasing, as the technology is maturing and starts to prove its capabilities. High power density and high efficiencies are reported and recently several inductor-less converters have emerged [1][2][7][10][13], which demonstrates soft switching capabilities. The elimination of a bulky inductor, reduces size and price of the converter, but demands a soft switching optimised PT. Several attempts of expressing the soft switching capability have been made [5][12], with some shortcomings. The goal of this paper is to derive a simple expression of the maximal obtainable soft switching capability (ZVS factor), for a specific PT design, assuming a matched load. The expression has been derived through series of parametric sweep simulations of the inductor-less half-bridge topology, which revealed that a linearization of the maximal soft switching capability can be performed, in the area of interest. This expression is intended to form a basic tool for development of soft switching optimised PT's, which enables the utilisation of inductor-less topologies.

1 Introduction

Piezoelectric transformer (PT) based converters have been around for some time now, but within resent years PT based converters have emerged, that exploit an inductor-less topology [1][2][7][10][13]. The elimination of the bulky inductor reduces size and price of the converter. But the parasitic input capacitance of the PT usually prevents the utilisation of an inductor-less power stage and an external series inductance is typically inserted in order to achieve soft switching capabilities. In a simple half-bridge power stage the input capacitance can lead to hard switching losses in the same range as the output power, resulting in a very poor efficiency. This calls for other means in order to avoid large hard switching losses, obtain soft switching capabilities and efficient operation. This can be achieved by utilising an advantageous PT structure and optimised design. But in order to evaluate the properties of the PT, a better understanding of the PT and what factors influences the soft switching capability is required. Several attempts of deriving a mathematical expression of the soft switching capability, directly from the lumped parameter model Figure 1 [11], have been made [3][5][10][12]. Great progress has been achieved, but they still have some shortcomings.

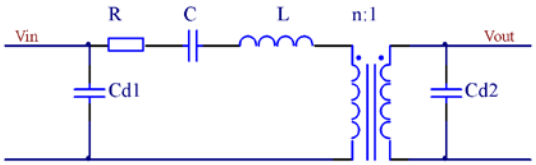

Figure 1: Lumped parameter model, which describes the behaviour of the PT in a narrow band around the operating resonance mode.

The approach in [5] has been to derive the full mathematical problem of the lumped parameter model, with respect to the input voltage, which should reach at least the half-bridge rail voltages, in order to soft switch. The result is a very precise expression of the soft switching capability. Its advantages are that it takes all the lumped parameters and the load resistance in to account, meaning that the soft switching capability can be calculated for any given PT and load, as well as the result is very accurate. The drawback of taking all the parameters and the load resistance in to account are a very complex expressing, making it quit computational heavy, as well as the expression still is a function of dead time and frequency. Furthermore there are no transparent relation between the parameters and the soft switching capability.
The approach in [12] has been to derive the expression in the frequency domain, as the lumped parameter model is of frequency domain nature. The derivation assuming matched load and has been accomplished by making a couple of assumptions. Equation 1 expresses the derived ZVS (zero voltage switching) factor, which is the maximal obtainable soft switching capability.

$$V_P' = \frac{1}{n^2}\frac{C_{d2}}{C_{d1}}\frac{32\sqrt{6}}{9\pi^2}\eta \qquad (1)$$

It has the advantages of being very short and handy, as well as being transparent, providing a very good relation between the parameters and the ZVS factor. And as it can be seen, it is only a few parameter of the model that affects the ZVS factor.

The drawback is that it is too optimistic. Through employment of the expression, within PT development and experimental work, it is found that a ZVS factor of at least 1.4 is needed in order to achieve soft switching.
The approach of this paper has been to perform a series of parametric sweep simulations of the lumped parameter model, searching for linearization opportunities in respect to the soft switching capability. The ZVS factor Equation (1) has been the starting point for the simulations and search, as it has demonstrated to relate to the soft switching capability, although it is optimistic. And as this paper will demonstrate, linearization opportunities were found in the area of interest. As a result a simple expression of the ZVS factor is derived, which demonstrates good accuracy and is only a function of the input and output capacitor ratio and the efficiency, just as Equation (1).

1.1 Piezoelectric transformer

PT's are based on piezoelectric materials, which usually is a ceramic material. This material has an electromechanical coupling and through this coupling a charge displacement is generated, that is proportional to the deformation of the material. A PT is basically two piezoelectric elements joined together to form a transformer. The primary side element is then exited by an electrical AC voltage, which induces a deformation of the two joined elements. This deformation generates an output voltage on the secondary side element and through a proper design of the PT, a desired voltage conversion can be achieved from the primary to the secondary side.
The PT is operated in one of its resonance modes, in order to convert energy at a high efficiency [6][8][9][10]. The PT resonates each time it is possible to generate a standing wave in the element, but the design is usually optimised for one specific resonance mode, in order to achieve the highest efficiency [8][10].
The PT resembles a distributed network, but for simplicity and mathematical representation, only the resonance mode of interest is modelled [8][9][10]. The lumped parameter model is one of the most frequently used PT models and was derived by Mason in 1942 [11]. The model is illustrated in Figure 1 and is basically a LCC resonance tank, as well as the behaviour of a PT based converter is quite similar to a traditional resonance converter [4].

3 Inductor-less half-bridge

Figure 2 illustrates the inductor-less half-bridge topology, where the absence of a series inductance and the parasitic input capacitor C_{d1}, calls for a soft switching optimised PT. The topology is quite simple, making it easy to understand the subject of soft switching. But the soft switching requirements of the PT for a bit more advance topologies, like the full-bridge, are the same. However for the more advanced topologies, like the PFC charge pump topologies [7], the requirements to the soft switching capability of the PT are higher, as the apparent parasitic input capacitance is increased.

The PT is loaded with a matched load as this maximises the power transfer of the resonance network, as well as this is the worst case condition for the soft switching capability [12].

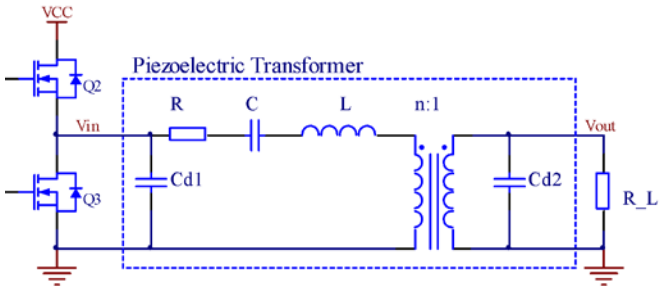

Figure 2: Schematical diagram of the inductor-less half-bridge topology and the PT equivalent lumped parameter model.

The target of soft switching is to achieve ZVS of the switches in the half-bridge. This can be achieved by operating the PT slightly above its resonance frequency, where the series resonance network becomes inductive and contains enough resonating energy to charge and discharge C_{d1}. And as it will be shown in the following section, there is an optimum where the resonance networks inductivity and energy is maximised, to make the largest energy transfer to C_{d1}. Furthermore there should be a certain dead time in between the two switches, in order to let the charge and discharge occur.

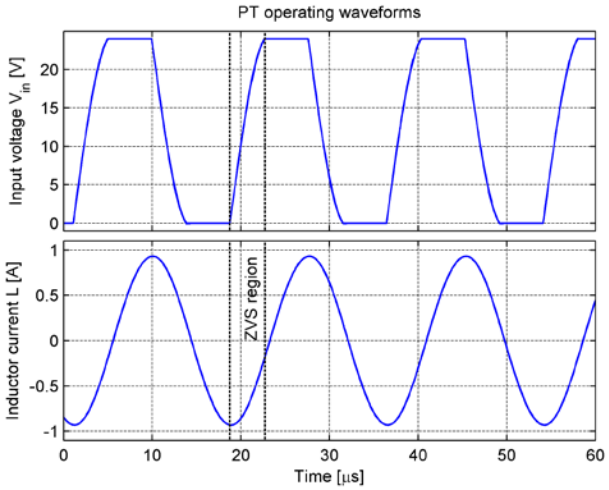

Figure 3: Input voltage and resonance current waveforms of the inductor-less half-bridge topology. From the input voltage it can clearly be seen that the half-bridge is operating under ZVS.

Figure 3 illustrates the operation of the inductor-less half-bride and as it can be seen the resonance current possesses sufficient phase shift and magnitude, to achieve ZVS. There is also sufficient dead time (ZVS region) in between the switches and it can clearly be seen that C_{d1} is charged and discharged, obtaining ZVS.

4 Soft switching factor

In the following section an expression of the maximal obtainable soft switching capability, also referred to as the soft switching factor or ZVS factor, is derived. The derivation is based on a series of parametric sweep time domain PSpice simulations of the inductor-less half-bridge, where the figures of Table 1 are the used lumped parameters. The figures origins from the interleaved multi layer Rosen-type PT design presented in [14], but as the lumped parameter mode is independent of PT design, the results should be general. The simulations have been preformed with at least 100 cycles before any measurements were made, in order to insure steady-state operation. Furthermore the simulated circuit utilises idealised switches and body diodes.

R	C	L	C_{d1}	C_{d2}	1/n
98mΩ	11.7nF	733µH	112nF	14.6pF	112

Table 1: FEM simulated PT equivalent lumped parameters obtained through impedance measurements.

From Equation (1) the ZVS factor of [12] can be calculated, as well as the match load and efficiency [12][14], as well as the resonance frequency. And as it can be seen from Table 2, the design possesses a ZVS factor which is sufficient to achieve soft switching.

$V'_{P\text{-}Old}$	R_{match}	H	f_R
1.43	198kΩ	0.987	55.2kHz

Table 2: FEM simulated PT equivalent lumped parameter model performance properties.

Equation (1) revealed that the soft switching capability is strongly dependent of the input and output capacitance. Figure 4 illustrates a frequency swept series of simulations, with the parameter of the input capacitance C_{d1} being swept as well.

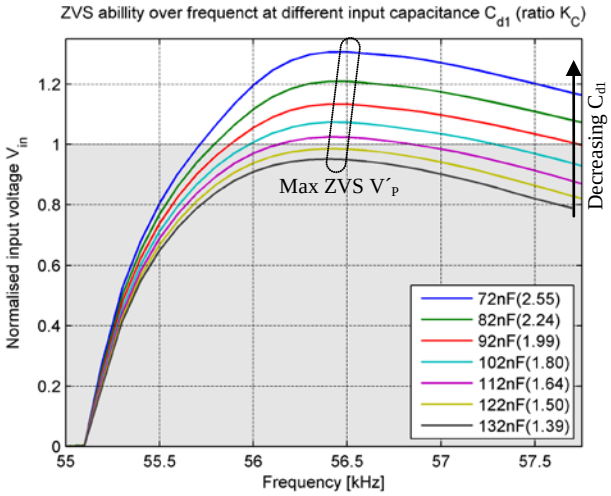

Figure 4: Simulated PT soft switching capability over frequency, with different input capacities Cd1 (capacitor ratio K_C).

As it can be seen the soft switching capability is strongly dependent of the input capacitance C_{d1} and the frequency. As for the shape of the curves there are a very good correlation to what were discovered in [5][12]. From the curves the maximal obtainable soft switching capability can be extracted, which is the parameter of interest. This ZVS factor can then be plotted in relation to the input capacitance C_{d1} or more interesting, in relations to the input and output capacitor ratio K_C Equation (2), which is illustrated in Figure 5.

$$K_C = \frac{1}{n^2}\frac{C_{d2}}{C_{d1}} \qquad (2)$$

The ZVS factors extracted from Figure 4 resemble the second topmost line in Figure 5. Moreover the series resistance R has been swept, creating several curves relating the ZVS factor to the PT efficiency.

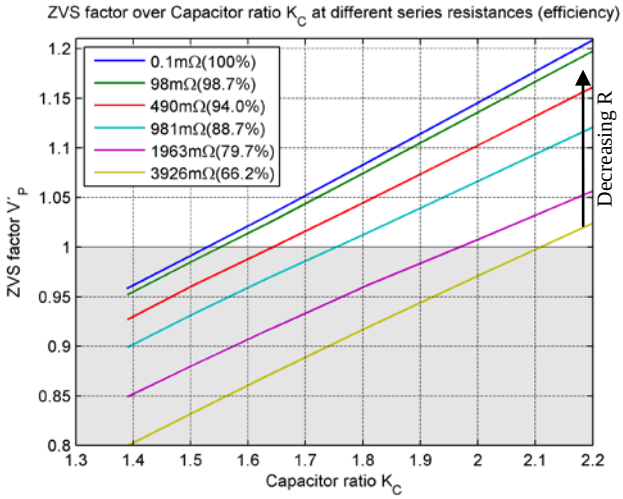

Figure 5: Simulated PT maximal soft switching capability (ZVS factor) in relation to the capacitor ratio K_C, at different efficiencies.

As Figure 5 reveals, there is a fine linear relation between the capacitor ratio K_C and the ZVS factor. By making a linear regression of the topmost line ($\eta \approx 100\%$), the most simplified expression of the ZVS factor is found Equation (3).

$$V'_{P\_100\%} = \left(0.304\frac{1}{n^2}\frac{C_{d2}}{C_{d1}} + 0.538\right) \qquad (3)$$

This expression is as simple as it gets, it is very handy and holds for high efficient PT's, which in the end is the ultimate goal of PT development.
But when working with less efficient PT's (< 97%), the efficiency should be taken in to account as well, in order to get a reliable result. Taking a look at Figure 5 it can be seen that the curves, which are lines of different efficiency, are nearly parallel. By taking a closer look at the curves it is found that they intersect the x-axis in roughly the same point, which indicates that the ZVS factor Equation (3) can be adjusted with an efficiency dependent factor.

Figure 6 illustrates how the ZVS factor is dependent on the efficiency at different capacitor ratios K_C and here as well the figure reveals a clear dependency of the efficiency. Although the dependency is not perfectly linear and differentiates a bit over the capacitor ratio K_C, a linear regression is made.

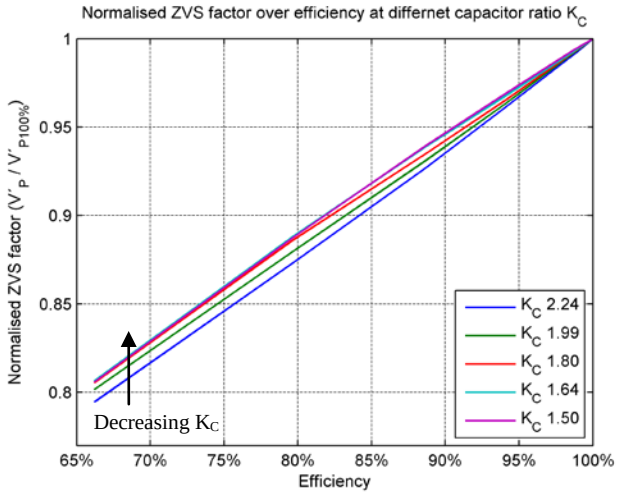

Figure 6: Simulated PT normalised maximal soft switching capability in relation to the efficiency.

The result is the correction factor Equation (4), which joined together with Equation (3) forms the final ZVS factor Equation (5).

$$K_\eta = (0.585\eta + 0.414) \qquad (4)$$

$$V_P' = \left(0.304\frac{1}{n^2}\frac{C_{d2}}{C_{d1}} + 0.538\right)(0.585\eta + 0.414) \qquad (5)$$

The expression is verified through comparison with the already simulated data of Figure 5 and as can be seen in Table 3 there are a very good correlation.

4 Experimental results

In order to fully validate the developed ZVS factor, the ZVS factor of a prototype PT has been measured.

The prototype PT is of the same design as the one simulated [14], with the exception of a bit different polarisation, which divides the turn's ratio (n) by two. Its properties are listed in Table 4 and Table 5, and as it can be seen it possesses a quit high ZVS factor.

η = 100%			**η = 94%**			**η = 80%**		
Sim	V'_P	**Δ**	Sim	V'_P	**Δ**	Sim	V'_P	**Δ**
0,96	0,96	**0,1%**	0,93	0,93	**-0,1%**	0,85	0,85	**-0,5%**
0,99	0,99	**0,2%**	0,96	0,96	**-0,2%**	0,88	0,88	**-0,6%**
1,03	1,03	**0,2%**	1,00	1,00	**0,0%**	0,92	0,91	**-0,6%**
1,08	1,08	**0,1%**	1,04	1,05	**0,1%**	0,96	0,95	**-0,5%**
1,14	1,14	**0,0%**	1,10	1,10	**0,2%**	1,01	1,01	**0,1%**
1,22	1,22	**-0,3%**	1,17	1,17	**0,1%**	1,07	1,07	**0,6%**

Table 3: Comparison between some of the simulated and calculated ZVS factors.

R	C	L	C_{d1}	C_{d2}	1/n
361mΩ	8.33nF	1052µH	129nF	93.2pF	55

Table 4: Prototype PT equivalent lumped parameters obtained through impedance measurements. The measurements have been performed with the PT mounted in the test circuit, including the additional parasitic.

$V'_{P\text{-}Old}$	V'_P	R_{match}	η	f_R
1.67	1.15	33.7kΩ	0.936	54.2kHz

Table 5: Prototype PT equivalent lumped parameter model performance properties.

By employing the inductor-less half-bridge, it is not directly possible to measure ZVS factors above 1, because of the clamping body diodes in the MOSFET's. Only ZVS factor below 1 is measurable, as the measurement shown in Figure 8. A diode could be placed in series with the top MOSFET and the input voltage (V_{in}) is thereby allowed to rise above supply voltage. This will enable a ZVS factor measurement, but it will also change the shape of the input voltage somewhat, changing the operation point.

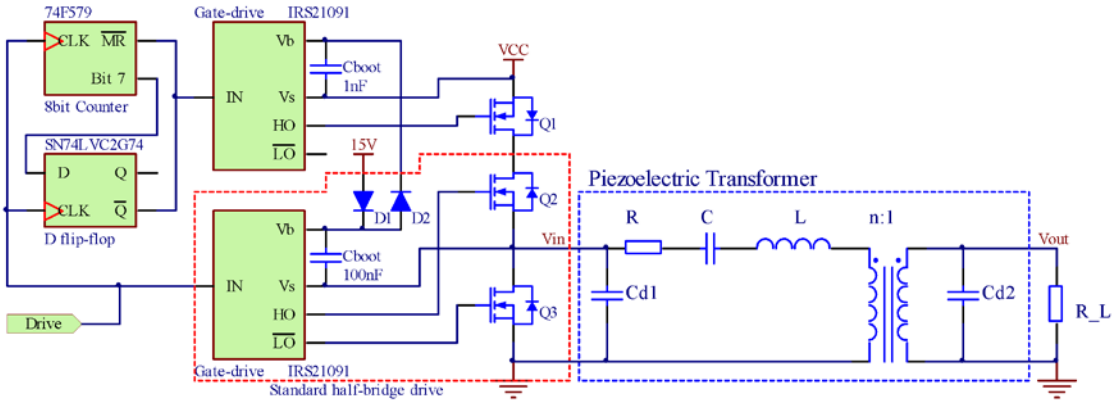

Figure 7: Schematical diagram of the inductor-less half-bridge, half-bridge driving circuit and the implemtatin of the soft switching capabability measurement circuit.

However by utilising a MOSFET instead of a diode, as in Figure 7 Q1, the input voltage is only allowed to rise above supply voltage once in a while. This is implemented as shown in Figure 7, with an N-channel MOSFET, a D flip-flop and an 8bit counter. The idea is to turn on Q1 and as Q2 and Q3 operates normally as a half-bridge, the counter counts the driving signal cycles. And when the counter reaches 256 cycles, the D flip-flop turns off Q1 for one cycle and resets the counter. In this manner the input voltage (V_{in}) is "released" and a ZVS factor higher than 1 can be measured, just as shown in Figure 9.

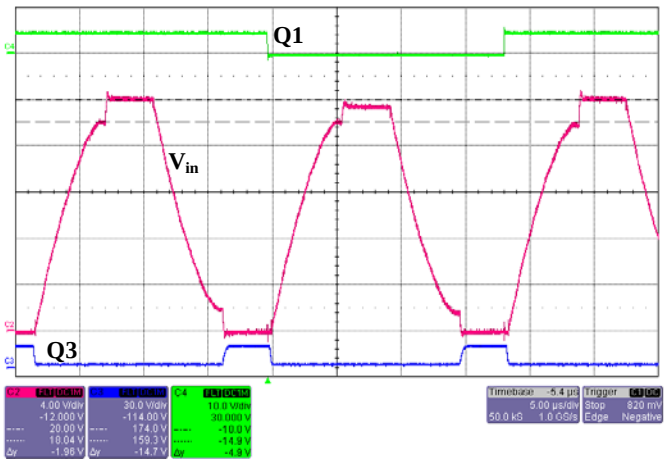

Figure 8: ZVS factor measurement of the prototype PT, with at capacitor ratio K_C of 1.38 (C_{d1} = 189nF). C3 and C4 shows gate signals, and C2 is the input voltage [4V/div].

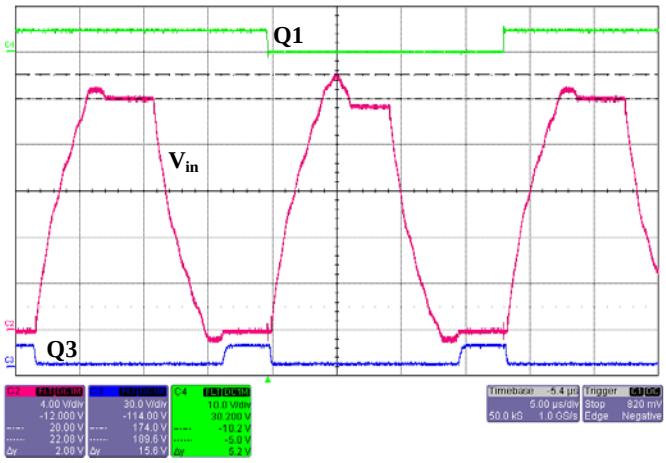

Figure 9: ZVS factor measurement of the prototype PT, with at capacitor ratio K_C of 2.16 (C_{d1} = 129nF). C3 and C4 shows gate signals, and C2 is the input voltage [4V/div].

Two sets of ZVS factor measurements have been collected through the experimental work. The approach in the experimental work has been to make a stepwise increment of the input capacitor C_{d1} and measure the drop in ZVS factor, just as the parametric sweep performed in the simulations. The tests have been performed with two different half-bridge supply voltages, 10V and 20V, as the increase in voltage should reflect a decrees in efficiency. This is due to the nonlinear nature of the piezoelectric loss.

Figure 10 illustrates the test results and it can be observed that the measurements are not as linear as anticipated, but the test setup also involved a certain measurement inaccuracy. But just as expected the ZVS factor drops when employing a higher half-bridge supply voltage.

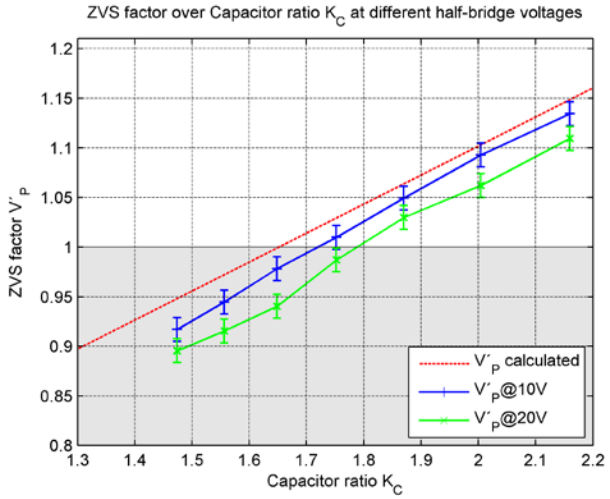

Figure 10: ZVS factor measurement of prototype PT in relation to the capacitor ratio K_C, compared with the ZVS factor equation.

5 Discussion

Comparing the predictions of the developed ZVS factor Equation (5) with the results extracted from the simulations, there is a very good correlation as illustrated in Table 3, where an accuracy below 1% is demonstrated. As for the results obtained through the experimental work Figure 10, it reveals that the ZVS factor is a bit more optimistic than the results. This is mainly due to the fact that the PT efficiency drops when the half-bridge voltage is increased. And as the lumped parameters of Table 4 are extracted from small-signal impedance measurements, the efficiency is also a measure of efficiency at small signals. The ZVS factor predictions of Figure 10 are based on this efficiency, so it is obvious that it will be a bit optimistic. Basically the efficiency used for the prediction should be modified as the working point changes to 10V and 20V. This is quite difficult though, because of the lack of a good and reliable efficiency measurement method. This is due to the high frequency AC load and standard power analysers are typically optimised for DC or low frequency 50/60Hz AC mains. Taking a closer look at Figure 10 it can be seen that the results are not as linear as expected, nor parallel to the predicted ZVS factor. However just looking at the result with a ZVS factor above 1, they are quite linear and parallel to the predicted ZVS factor. Some of the deviation could defiantly be due to measurement inaccuracy, as the measurements are extracted by hand, from oscilloscope plots as Figure 8 and Figure 9. Nonetheless the deviations could also origin from elements in the circuit, which is not include in the idealised simulation, such as the highly nonlinearities

of semiconductor parasitic capacitances. Although not taking the efficiency drop in to account, the developed ZVS factor manages to do a prediction within 3% of the 10V test results and within 6% of the 20V test results. As a final note it can be noted that a capacitor ration K_C of at least 1.55 is needed in order to achieve soft switching capability and a ZVS factor above 1.

6 Conclusion

Through a series of parametric sweep PSpice simulations an expression describing the maximal obtainable soft switching capability has been derived, also known as the ZVS factor. The expression is very simple and transparent, clearly stating the strong dependency of the input and output capacitor ratio, as well as the dependency of the efficiency. As a result the soft switching capability of a specific PT design can be evaluated easily and directly from the lumped parameter model. The ZVS factor forms a basic soft switching capability measuring tool, to assist through the development of ZVS optimised PT's. The developed ZVS factor has been evaluated up against the simulations as well as against a developed prototype DC/AC inductor-less half-bridge converter. It demonstrated below 1% accuracy compared to the simulations, validating its functionality. And a 3-6% accuracy compared to the prototype, bearing in mind that a too optimistic efficiency for calculating the ZVS factor were used.

Acknowledgements

Finally we would like to thanks Noliac A/S for supplying prototype PT's, as well as general PT design support.

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Appendix: A3

M. S. Rødgaard, **T. Andersen**, K. S. Meyer and M. A. E. Andersen, "Design of interleaved multilayer Rosen type piezoelectric transformer for high voltage DC/DC applications", in PEMD, 2012.

DESIGN OF INTERLEAVED MULTILAYER ROSEN TYPE PIEZOELECTRIC TRANSFORMER FOR HIGH VOLTAGE DC/DC APPLICATIONS

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Keywords: Piezoelectric transformer, step-up, converter, soft switching

Abstract

Research and development within piezoelectric transformer (PT) based converters are rapidly increasing as the technology is maturing and starts to prove its capabilities. Especially for high voltage and high step-up applications, PT based converters have demonstrated good performance and DC/AC converters are widely used commercially. The availability of PT based converters for DC/DC applications are very limited and are not that developed yet. I this paper an interleaved multi layer Rosen-type PT for high step-up and high output voltage is developed, for driving a 2.5kV dielectric electro active polymer actuator [17]. The targeted application utilises an inductor-less half-bridge driving topology, where the reward of eliminating the series inductor is a reduction in component count, size and price. The absence of a series inductance calls for other means to avoid large hard switching losses and obtain soft switching capabilities. This can be achieved by utilising an advantageous PT structure, which is the main advantage of the interleaved Rosen-type PT. Furthermore the design should be further optimised, in order to achieve soft switching capability. The goal of this paper is to develop a soft switching optimised PT, capable of generating output voltages higher than 2kV from a 24V supply voltage. Furthermore finite element method (FEM) has been the main tool through the PT development.

1 IntroductionThe piezoelectric transformer (PT) was originally developed by Rosen in 1957 [16] and utilises piezoelectric ceramics to convert electrical energy through mechanical vibrations. PT based converters have demonstrated good performance and DC/AC converters are widely used commercially, especially for high step-up and high voltage (HV) applications, like LCD backlighting. But they are still limited to these simple applications (with a constant and high frequency AC load) and the availability of PT based converters for DC/DC applications are very limited and are not that developed yet. However new applications, like electro active polymer (EAP) actuators [5][17], require a high and adjustable DC voltage and calls for DC/DC converters of high step-up and high output voltage.

EAP devices are based on polymer materials and change shape as a result of the electrostatic forces, generated by an applied voltage. The EAP technology has a wide potential in applications such as surgical tools, grippers for material handling and valve actuators for example. The EAP material is essentially just a thin film of polymer with an electrode on each side. It can be modulated as a HV capacitor with a very low leakage current and the force generated by the EAP is related to the applied voltage. The voltage required is dependent among others by the thickness of the EAP film. The EAP technology available today has a film thickness of around 80 µm [5][17], it has a maximum working voltage of 2.5 kV and requires a voltage above 2kV to fully utilise it as an actuator.

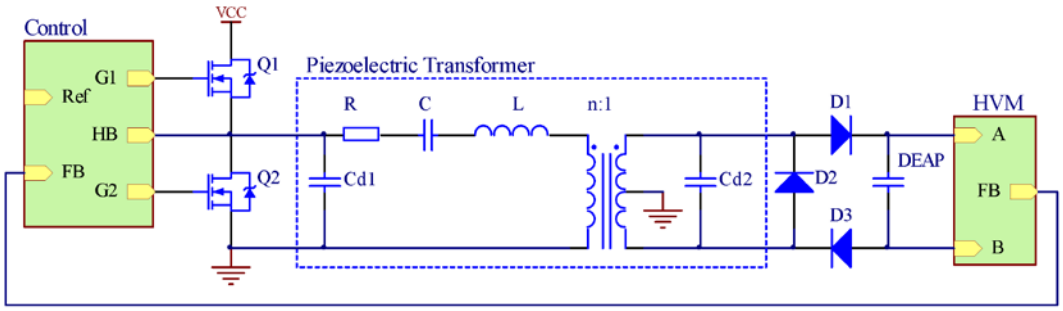

Figure 1: Schematical diagram of the inductor-less half-bridge topology and the PT equivalent lumped parameter model.

To date, conventional converters utilize electromagnetic components and are the only available HV sources for driven EAP actuators. However these HV converters have poor efficiency, are bulky and provide limited opportunities for miniaturization. PT based converters, on the other hand, are compact and offers high efficiency, especially for high step-up applications. This makes the PT based converter the perfect match for the EAP technology.
In the last decade a lot of research in to the area of PT's has improved Rosen's fist PT and new types of PT's have been developed [4][8][11][14][18]. I this paper an interleaved multi layer Rosen-type PT for high step-up and high output voltage is developed, for driving a 2.5kV EAP actuator [17]. The specific EAP actuator application is described in more detail in [1] and is similar to the one in [3]. Figure 1 illustrates a schematical diagram of the converter, which utilises an inductor-less half-bridge topology [2][13]. An inductor in series with the PT is usually necessary, in order to achieve soft switching and efficient operation. The absence of a series inductance calls for other means to avoid large hard switching losses and obtain soft switching capabilities. By utilising an advantageous PT structure, soft switching capability can be obtained, which is the main advantage of the interleaved Rosen-type PT. Furthermore the design should be optimised further, in order to obtain soft switching capability. This optimisation has been performed through iterative FEM simulations, as well as the optimisation of the gain and the PT properties in general. Due to the increasing complexity of PT structures and the complexity of the electromechanical behaviour in general, a pure mathematical solution of PT design problems is very challenging, as well as a high degree of knowledge of the electromechanical domain is needed. With today's multi physics FEM simulators, one can fine-tune PT structures, without having to rewrite the math every time.
As a result an interleaved Rosen-type PT, with a soft switching factor [13] of 1.43 and a gain of 68 has been developed.

2 Piezoelectric transformer

PT's are based on a piezoelectric material. This material has an electromechanical coupling and through this coupling a charge displacement is generated, which is proportional to the deformation of the material. A PT is basically two piezoelectric elements which is joined together to form a transformer. The primary side element is then exited by an electrical AC voltage, which induces a deformation of the two joined elements. This deformation generates an output voltage on the secondary side element and with a proper design of the PT, a desired voltage conversion can be obtained from the primary to the secondary side.
In order to convert power at a high efficiency, the PT is operated in one of its resonance modes [8][9][10][11]. The PT resonates each time it is possible to generate a standing wave in the element. But the design is usually optimised for one specific resonance mode, in order to obtain the highest efficiency [9][11].

The PT resembles a distributed network, but for simplicity and mathematical representation, only the resonance mode of interest is modelled [9][10][11]. One of the most used PT models is the lumped parameter model, which was derived by Mason in 1942 [12] and is illustrated in Figure 2.

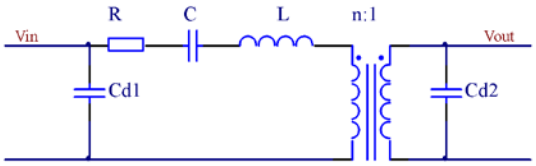

Figure 2: Lumped parameter model, which describes the behaviour of the PT in a narrow band around the opperating resonance mode.

The model is basically a LCC resonance tank and the behaviour of a PT based converter is also quite similar to a traditional resonance converter [6].

2.1 Piezoelectric transformer design

The PT developed for this application is essential an interleaved multi layer Rosen-type, meaning that the primary section of the PT has been interleaved into the secondary section. Figure 3 illustrates the structure of the PT, which consists of a primary section with 12 layers, of 166µm in thickness and one split secondary layer. For simplicity the figure only shows two primary layers and the arrows indicate the polarization direction. The PT is build using tape casting technology and the NCE46 piezoelectric material [15]. The PT has the dimensions of 25mm x 10mm x 2mm, but PT's of 20mm, 30mm and 35mm in length were also designed and produced in the same process.

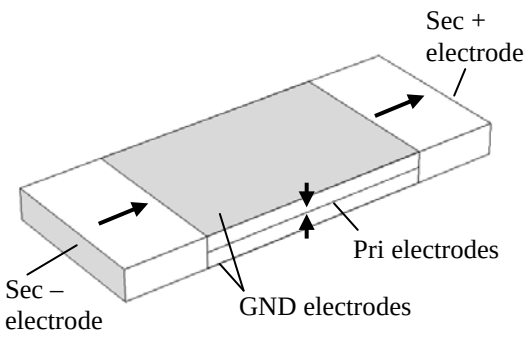

Figure 3: The interleaved multi layer Rosen-type PT structure, where the arrows indicate the polarization direction.

The PT design is quite similar to the one presented in [18], but differs with the polarization of the secondary being in the same direction, as well as it has been optimised for soft switching. Meaning that it is capable of operating the half-bridge under zero voltage switching (ZVS), without any added inductance in series with the PT. The operational vibration resonance is along the longitudinal direction and is generated through the electromechanical coupling factors k_{31} and k_{33}, primary and secondary respectively. In Figure 4 a

FEM simulation of the operational vibration resonance is shown. The PT operates in its first longitudinal mode shape and it can be seen it has a nodal line in the center of the structure.

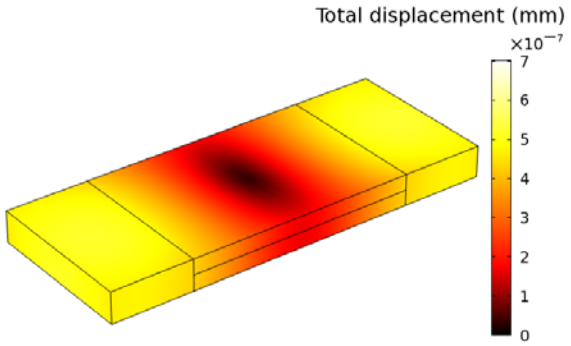

Figure 4: FEM simulation of the PT, operating in the first longitudinal mode shape, at 65.1 kHz. The colouring illustrates the total displacement, where dark colours refer to a low displacement and light colours to at high displacement, as the colour bar indicates.

One of the drawbacks of this design, for this application, is the split secondary. This results in a differential output voltage symmetrical around ground, which complicates the electronics somewhat. One could polarise the two half secondary layers in opposite directions, which results in a two layer secondary structure, obtaining a common voltage potential with reference to ground, as in [18]. But this approach would also divide the gain by two, because of two secondary layers, of half the thickness, instead of one full thickness secondary. For this application we need a very high gain, so the extra effort in the electronic is rewarded with a doubling in gain.

2.2 Piezoelectric transformer development

The major part of the development has been performed through iterative FEM simulations, where the two main design criteria have been a high gain and the capability of inductor-less operation. In order to utilise an inductor-less topology, the PT should poses soft switching capabilities. This is achieved through the relative location and size of the primary section. Furthermore the PT is operated slightly above the resonance frequency, where the series resonance network becomes inductive and contains enough resonating energy, to charge and discharge the input capacitance C_{d1}. The interleaving of the primary section is the main advantage of this design, as this increases the soft switching capability. This is due to the placement right in the middle of the stress curve, which is a half-wave sine wave for the first resonance mode. Furthermore the primary section size has been optimised in order obtain soft switching capability.
Rosen-type PT's has a native high gain, which is good for this application. The gain is mainly determined by the thickness of the primary layers, but of course the primary section size also affects the gain.

Figure 5 shows a frequency sweep of the primary and secondary impedance, around the operating resonance mode. In order to evaluate the electrical characteristics of the PT, the lumped parameter model should be created.

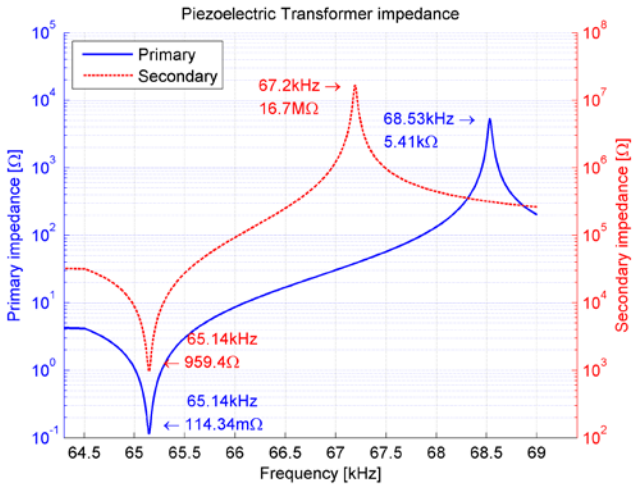

Figure 5: FEM simulation of the PT primary and secondary impedance magnitude, with the opposite side shorted.

The lumped parameters are calculated from the primary and secondary impedance resonance and anti-resonance, plus a DC impedance measurement, as described in detail in [13]. Trough the FEM simulation of the PT impedance Figure 5, the equivalent parameters of Table 1 are found.

R	C	L	C_{d1}	C_{d2}	1/n
114mΩ	9.8nF	609µH	91.7nF	17.5pF	93.5

Table 1: PT equivalent lumped parameters obtained through FEM simulations.

From the lumped parameters some more general performance properties of the PT can be calculated, as the soft switching factor, matched load, power in matched load, gain and efficiency.
The load is usually matched to the output capacitance C_{d2} of the PT, Equation (1), or the other way around, because this maximises the power transfer of the resonance network to the load. Furthermore all the following performance properties assume a matched load.

$$R_{match} = \frac{1}{C_{d2}\omega_r} \qquad (1)$$

Equation (2) expresses the soft switching factor or ZVS factor, which is derived in [13] and is a measure of the PT's soft switching capabilities. If the ZVS factor is more than 1, the PT is capable of performing ZVS at the half-bridge, operated with a matched load.

$$V_P' = \frac{1}{n^2}\frac{C_{d2}}{C_{d1}}\frac{32\sqrt{6}}{9\pi^2}\eta \qquad (2)$$

Through our own experience, this equation has its short comings, properly because of some of the assumption in the derivation, which is demonstrated in detail in [7]. But it has shown to predict soft switching when working with factors above approximately 1.4 and it is very simple and straight forward to use, compared to the one derived in [7].
Equation (2) is the maximal obtainable soft switching capability, which is located slightly above the resonance frequency, where the series resonance network becomes inductive and contains enough resonating energy, to charge and discharge C_{d1}, if the soft switching factor is above 1.4.
The efficiency Equation (3) is a small signal efficiency, because the FEM simulation is only a small signal simulation of the impedance. Furthermore the loss mechanisms of piezoelectric materials are not fully implemented in the FEM simulation, therefore the efficiency is mostly just a measure to compare between different designs.

$$\eta_{match} = 1 - \frac{2RC_{d2}}{n^2\sqrt{LC}} \qquad (3)$$

The following PT properties of Table 2 are found from the equivalent parameters of Table 1 and the index "ZVS" is referring to that the PT is operating at its maximum ZVS point.

V'_P	A_{ZVS}	P_{ZVS}	R_{match}	η	$V_{out,rms}$
1.45	75.3	3.79W	138kΩ	0.986	728V

Table 2: PT equivalent lumped parameter model performance properties.

Evaluating these properties it can be seen that it has a sufficient high ZVS factor of 1.45, which enables the inductor-less operation, a high efficiency and a high gain. The high gain results in a 728 V_{rms} output voltage, into a matched load, with a PT modulation voltage of 9.67V_{rms}. The PT modulation voltage is the first harmonic, of the 24V input voltage, as derived in [13].

3 Experimental results

In the following section the functionality and properties of the received prototype PT's are verified.

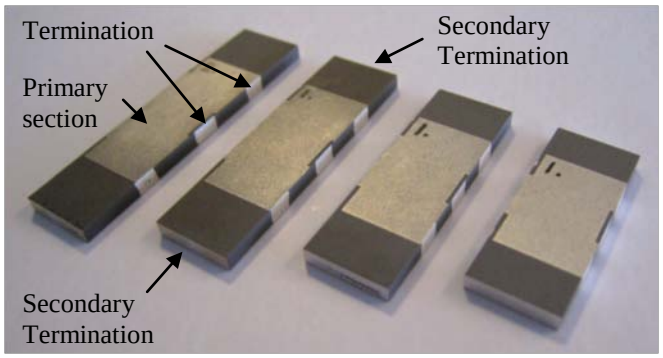

Figure 6: Picture of prototype PT's of different sizes (length from left: 35mm, 30mm, 25mm and 20mm).

Figure 7 shows an impedance measurement of one of the prototype PT's and from these measurements the equivalent lumped parameters of Table 3 and the performance properties of Table 4 are calculated.

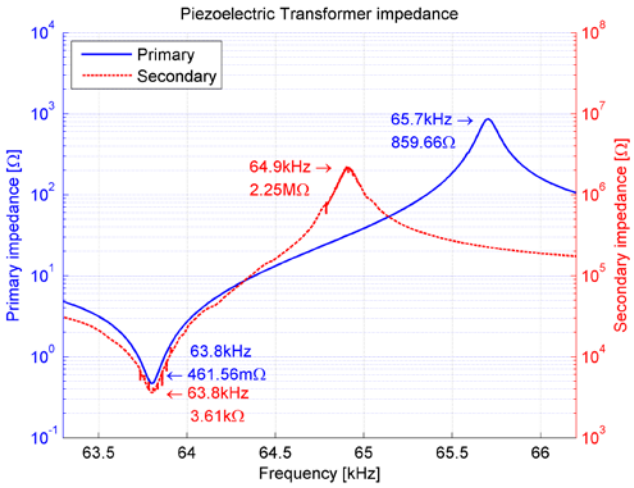

Figure 7: Measurement of prototype PT primary and secondary impedance magnitude, performed with a HP4194A impedance/gain-phase analyzer.

R	C	L	C_{d1}	C_{d2}	1/n
462mΩ	6.74nF	923µH	112nF	24.8pF	88.6

Table 3: Prototype PT equivalent lumped parameters obtained through impedance measurements.

V'_P	A_{ZVS}	P_{ZVS}	R_{match}	η	$V_{out,rms}$
1.43	67.5	4.23W	100kΩ	0.933	653V

Table 4: Prototype PT equivalent lumped parameter model performance properties.

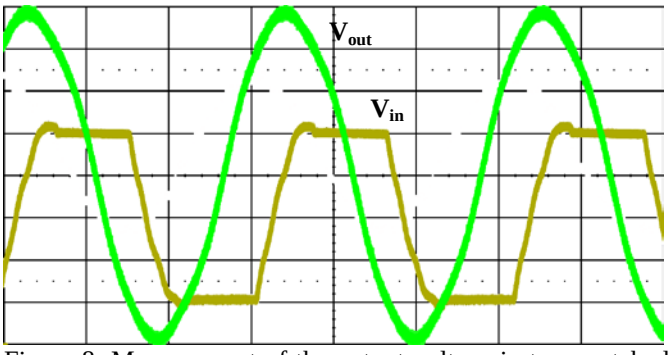

Figure 8: Measurement of the output voltage in to a matched load (green) and input half-bridge voltage (yellow), which clearly is operating under ZVS. Time base [5µs/div], output voltage [200V/div] and input half-bridge voltage [5V/div].

Figure 8 shows the PT operating with a half-bridge voltage of 20V and with a matched resistive load. From the input voltage waveform, it can clearly be seen that the half-bridge is operating under ZVS, which verifies the designs soft switching capability. Looking at the output voltage it resembles a nice sine wave, with a peak voltage of

approximately 780V, from which the gain of Equation (4) can be calculated.

$$A_{ZVS} = \frac{|V_{out}|}{|V_{in}|} = \frac{780V}{0.57 \cdot 20V} = 68.2 \qquad (4)$$

Where 0.57 is the approximate amplitude of the first harmonic of a trapezoidal waveform, as derived in [13]. When employing a rectifying voltage doubler instead of a matched load, voltages over 2kV can be achieved for DC/DC applications.

4 Discussion

Comparing measured figures (Table 3 and Table 4) with the FEM simulation obtained figures (Table 1 and Table 2), it can be seen that the gain (A_{ZVS}) is 10% lower than expected. This is partly because the prototype build-up were 2.1mm high, which is 0.1mm higher than expected, making the primary layers 5% higher and this results in a 5% decrease in gain. Furthermore there is some inactive piezoelectric material in the primary section, due to the termination of the primary electrodes on the side of the PT, as shown in Figure 6. For simplicity the termination is not included in the FEM simulation, which accounts for some of the remaining 5 % deviation. Hence there is a very good correlation between the FEM model and the prototype concerning the gain. Comparing the gain of Equation (4) with the calculated from the lumped parameters (Table 4), it can be seen that there is a very good correlation between a fully stressed PT and the small signal impedance measurement.
The correlation between the soft switching factors (V'_P) is also very good.
Looking at the capacitances C_{d1}, C_{d2} and the efficiency, the correlation is not that good. This is expected to be because of a bad correlation between the NCE46 material parameters in the FEM model and what they are in real life, as well as an incomplete loss model in the FEM simulation. Nevertheless the FEM simulation makes it possible to design soft switching optimised PT's for inductor-less operation, having a desired soft switching factor, a desired gain, as well as the possibility to compare the performance between different designs. For this specific case there is not a well defined resistive load and the load matching inaccuracy is therefore not a problem.

5 Conclusion

In this paper a new interleaved multi layer Rosen-type piezoelectric transformer (PT), optimised for soft switching, inductor-less operation and high output voltage has been developed. The development has been performed through iterative finite element method simulations, which has proven its capabilities as a good design tool for PT development. The measurements of the prototype PT showed a good correlation between the design and the prototype. The prototype PT has demonstrated to have a sufficiently high soft switching factor of 1.43 to operate in an inductor-less topology, as well as having a high gain of 68, enabling the generation of high output voltages.

Acknowledgements

Finally we would like to thanks Noliac A/S for the production of prototype PT's, as well as general PT design support. We would also like to thanks Danfoss PolyPower A/S for supplying the application and EAP actuators.

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Appendix: A4

M. S. Rødgaard, **T. Andersen**, K. S. Meyer and M. A. E. Andersen, "Design of Interleaved Interdigitated Electrode Multilayer Piezoelectric Transformer utilizing longitudinal and Thickness mode vibrations", submitted to PECON, 2012.

Design of Interleaved Interdigitated Electrode Multilayer Piezoelectric Transformer utilizing Longitudinal and Thickness Mode Vibrations

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***Abstract*— In applications of high voltage and low power capacitor charging, conventional magnetic based power converters often suffer from bulky components and poor efficiency. Piezoelectric transformer (PT) based converters however, are compact and efficient, especially for high step-up applications. I this paper an interleaved interdigitated electrode (IDE) multilayer PT utilizing longitude and thickness mode vibration for high step-up and high output voltage is developed, for driving capacitive loads of up to 2.5kV. The PT possesses soft switching capabilities, enabling the utilization of inductor-less topologies. One of the main advantages of the IDE's is that it enables the PT to operate in longitudinal vibration and thickness mode through the electromechanical coupling coefficient K_{33}. This also permits the realization of the PT through a low build-up height (below 2-4mm), which makes the production much easier and cheaper. As a result an interleaved IDE PT, with a soft switching factor of 1.00 and a gain of 38 has been developed.**

Keywords-component; Piezoelectric transformer, step-up, converter, soft switching, Interdigitated Electrode (IDE)

I. INTRODUCTION

The piezoelectric transformer (PT) developed in this work, is targeted for high voltage and low power capacitor charging applications. The application is of high step-up conversion and for this specific application [1] stepping-up from a 48V supply voltage, to voltages of up to 2.5kV, giving a step-up ration of around 50. Conventional power converters are built of magnetic transformers and inductors, but in high step-up and low power applications, as this one, they often suffer from bulky components and poor efficiency. PT based converters however, are compact and efficient, especially for high step-up applications.The PT was originally developed by Rosen in 1957 [2] and utilises piezoelectric ceramics to convert electrical energy through mechanical vibrations. PT based converters have demonstrated good performance and DC/AC converters are widely used commercially, such as for LCD backlighting. But PT based converters for DC/DC applications are still very limited and are not fully developed. Fig. 1 illustrates the PT based DC/DC converter, which utilises an inductor-less half-bridge topology [3-5] and the specific application is described in more detail in [1] and is similar to the one of [6].Usually an inductor in series with the PT is necessary, in order to achieve zero voltage switching (ZVS), avoid large hard switching losses and achieve efficient operation. The absence of a series inductance calls for other means to obtain soft switching capabilities, which can be achieved by utilising an advantageous and soft switching optimised PT structure.

I this paper an interleaved interdigitated electrode (IDE) multilayer PT utilizing longitude vibration for high step-up and high output voltage is developed, for driving a 2.5kV EAP actuator [7]. The main advantage of this interleaved PT structure is its native good soft switching capabilities. Another big advantage is the build-up with IDE's, which enables the PT to operate in longitudinal vibration and thickness mode through the electromechanical coupling coefficient K_{33}, where the direction of polarization and vibration are the same. This essential permits the realization of the PT through a low build-

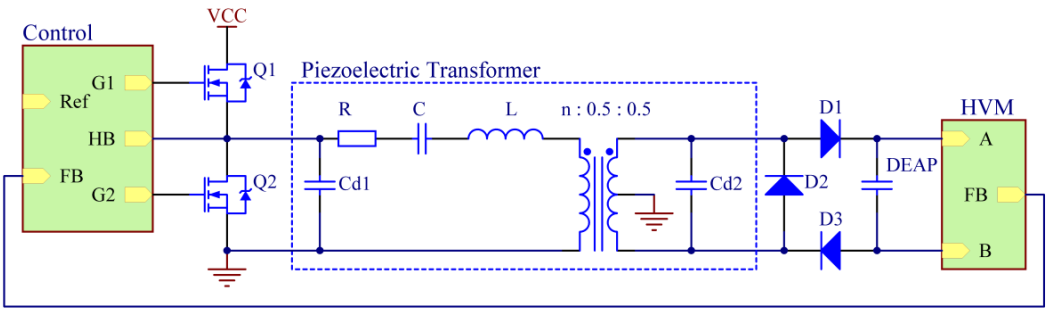

Figure 1. Schematical diagram of the inductor-less half-bridge topology and the PT equivalent lumped parameter model.

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up height (below 2-4mm), which makes the production much easier and cheaper. The PT design should be optimised further, in order to obtain a sufficient soft switching capability, which also is described and patented in [8]. As the complexity of PT structures increases, as well as the complexity of the electromechanical domain in general, the PT design optimisation has been performed through iterative FEM simulations. It is very challenging to derive a pure mathematical solution of PT design problems and with today's multi physics FEM simulators, one can fine-tune PT structures, without having to rewrite the mathematical problem.

A. The piezoelectric transformer

PT's are based on a piezoelectric material. This material has an electromechanical coupling and through this coupling a charge displacement is generated, which is proportional to the deformation of the material. A PT is basically two piezoelectric elements which is joined together to form a transformer. The primary side element is then exited by an electrical AC voltage, which induces a deformation of the two joined elements. This deformation generates an output voltage on the secondary side element and with a proper design of the PT, a desired voltage conversion can be obtained from the primary to the secondary side.

In order to convert power at a high efficiency, the PT is operated in one of its resonance modes [9-12]. The PT resonates each time it is possible to generate a standing wave in the element. But the design is usually optimised for one specific resonance mode, in order to obtain the highest efficiency [10, 12].

The PT resembles a distributed network, but for simplicity and mathematical representation, only the resonance mode of interest is modelled [10-12] . One of the most used PT models is the lumped parameter model, which was derived by Mason in 1942 [13] and is illustrated in Fig. 2. The model is basically a LCC resonance tank and the behaviour of a PT based converter is also quite similar to a traditional resonance converter.

II. PIEZOELECTRIC TRANSFORMER DESIGN

The PT developed is an interleaved IDE thickness mode PT, meaning that the primary section of the PT has been interleaved into the secondary section. Fig. 3 illustrates the structure of the PT, which consists of a primary section with 40 layers, with a layer thickness of 180µm and one split secondary layer. For simplicity the figure only shows two primary layers and the arrows indicate the polarization direction. The PT dimensions is 30x10x2mm, but PT's of 20x10x2mm, and 25x10x2mm were also designed and produced in the same

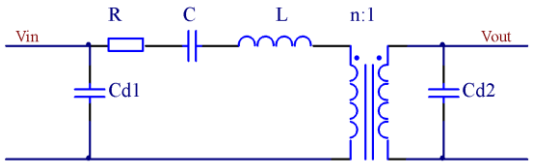

Figure 2. Lumped parameter model, which describes the behaviour of the PT in a narrow band around the operating resonance mode

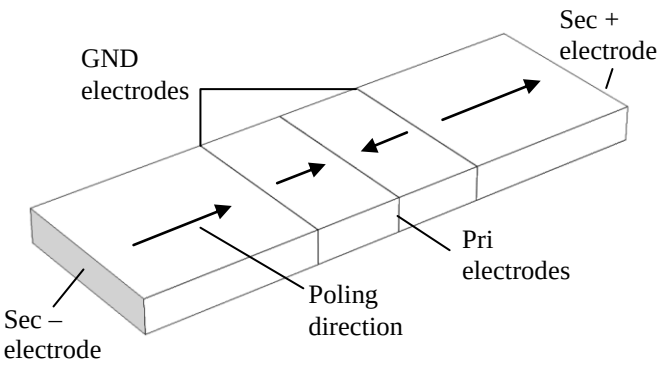

Figure 3. The interleaved multilayer PT structure, where the arrows indicate the polarization direction.

process.

One of the main advantages of this PT structure is that the operational vibration resonance is along the longitudinal direction and is generated through the electromechanical coupling coefficient k_{33} for both primary and secondary. This means that both sections are operating in thickness mode, which is the most efficient mode [10, 12, 14], as this mode has the highest electromechanical coupling, contrary to the Rosen type where only the secondary section is operating in thickness mode. Fig. 4 illustrate a FEM simulation of the operational vibration resonance of the PT operating in its first longitudinal mode shape, where it also can be noticed that it has a nodal line in the center of the structure.

One of the drawbacks of this design is the split secondary, which results in a differential output voltage symmetrical around ground. This complicates the electronics somewhat, compared to a ground referenced output. But for this application we need a very high gain, so the extra effort in the electronic is rewarded with a high gain.

The PT is build using tape casting technology, using the NCE46 piezoelectric material [15] and platinum electrode prints. Furthermore the design utilises IDE's, where a thin platinum line (70µm) is printed on every tape layer, resulting in a stack of lines placed on top on each other, as illustrated in Fig. 5. The lines are shorted through a termination on the side of the PT and form a vertical electrode. This essential permits the PT to be realized with a low build-up height (below 2-4mm), while enabling the thickness mode operation. Tape

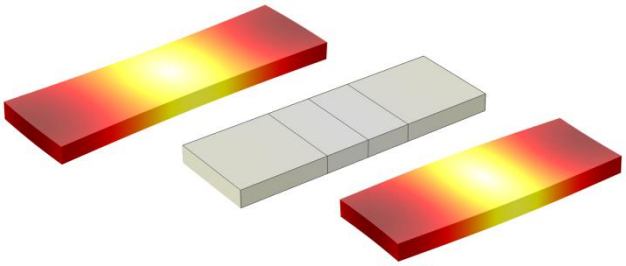

Figure 4. FEM simulation of the PT, operating in the first longitudinal mode shape, at 47.53 kHz. The colouring illustrates the total displacement, where light colours refer to a low displacement and dark colours to at high displacement.

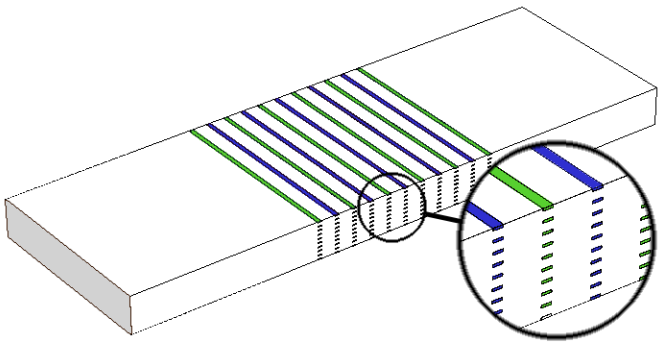

Figure 5. The interleaved multilayer PT structure, illustrating the IDE structure, with 10 primary layers and exaggerated electrode prints.

casting does not allow implementation of vertical electrodes, meaning that this design should have a build-up height of 30mm, when using traditional electrodes, making it almost impossible to produce. The IDE structure makes the production much easier and cheaper

The drawback of using IDE's is that the electrodes have a finite thickness of 70µm (line print width), compare to the negligible 2µm thickness of traditional electrodes. As there are production limits to how thin the IDE layers can be made, a certain part of the primary section is going to consist of the electrodes and hence inactive material. The percentage of inactive material is determined by the IDE thickness and the primary layer thickness. The percentage of inactive material is desired to be as low as possible, as it does not contribute with anything, except for losses, and will degrade the performance of the primary section. Furthermore the tape thickness should be small compared to the primary layer thickness, so that the IDE appears as a consistent vertical electrode. With a tape thickness of 33µm and a primary layer thickness of 180µm, the tape thickness is only 5.5 times smaller, but has shown to be sufficient.

III. PIEZOELECTRIC TRANSFORMER DEVELOPMENT

The major part of the development has been performed through iterative FEM simulations, due to the high complexity of PT structures, as well as the complexity of the electromechanical domain in general. The two main design optimization criteria have been a high gain and soft switching capabilities, as well as a reasonable high ratio of active and inactive material. In order to utilizes inductor-less topologies and utilize ZVS operation, the PT should possess soft switching capabilities. Furthermore the PT is operated slightly above the resonance frequency, where the series resonance network becomes inductive and contains enough resonating energy, to charge and discharge the input capacitance C_{d1}.

The main advantage of the interleaved primary section is its native good soft switching capabilities. This is due to the placement right in the middle of the excitation stress curve, which is a half-wave sine wave for the first resonance mode, as illustrated in Fig. 6. The primary section size has been optimized in order obtain sufficient soft switching capability. The gain is mainly determined by the primary and secondary layer thickness ratio, but it is also affected by the primary section size. And as a small primary layer thickness is desired,

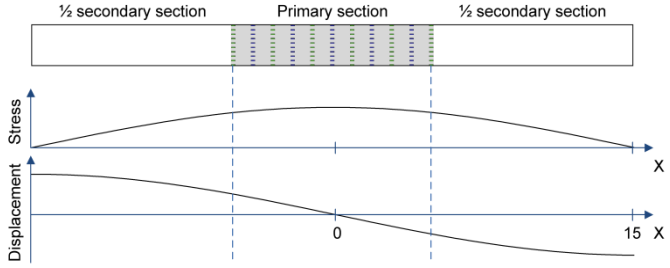

Figure 6. The interleaved multilayer PT structure, illustrating the stress and displacement in its first mode shape.

hence a high gain, the percentage of inactive material is pushed to its limits. So in the end this percentage has also been optimized, as well as it affects the soft switching capabilities and gain. In order to simplify the PT structure for the FEM simulation, the IDE's have been approximated by solid vertical electrodes, of inactive piezoelectric material with an electrode thickness of 70µm, as well as only a 2D simulation has been performed.

Fig. 7 shows a frequency sweep of the primary and secondary impedance of the resulting design, around the operating resonance mode. In order to evaluate the electrical characteristics of the PT, the lumped parameter has be calculated from the impedance measurements. From the primary and secondary impedances resonance and anti-resonance, plus a DC impedance measurement, the lumped parameters has be calculated, as described in detail in [4, 11, 16]. Through the FEM simulation of the PT impedances Fig. 7, the equivalent parameters of table I are found. The lumped parameters does not tell much about the performance of the PT, but some more general performance properties can be calculated, such as the soft switching factor, matched load,

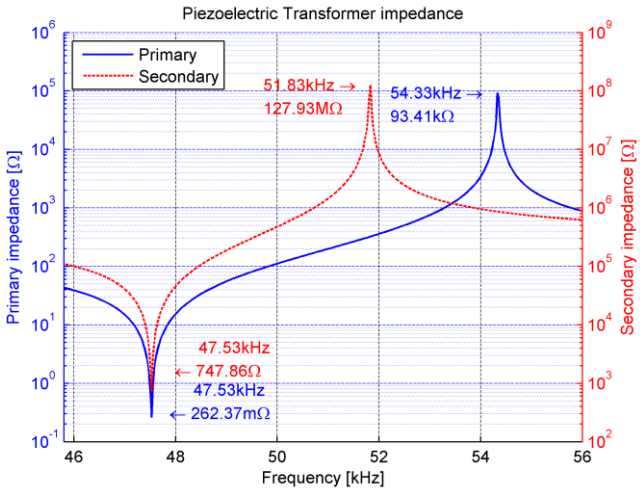

Figure 7. FEM simulation of the PT primary and secondary impedance magnitude, with the opposite side shorted.

TABLE I. PT EQUIVALENT LUMPED PARAMETERS OBTAINED THROUGH FEM SIMULATIONS.

R	C	L	C_{d1}	C_{d2}	1/n
262mΩ	4.56nF	2.46mH	14.85nF	8.23pF	54.1

power in matched load, gain and efficiency.

Usually the load is matched to the output capacitance C_{d2} of the PT, Equation (1), or the other way around, as the load matching maximises the power transfer of the resonance network to the load. Where ω_r is the operating frequency and can be approximated as the resonance frequency. Furthermore all the following performance properties assume a matched load.

$$R_{match} = \frac{1}{C_{d2}\omega_r} \tag{1}$$

Equation (2) expresses the soft switching factor or ZVS factor [5] which is a measure of the PT's soft switching capabilities. If the ZVS factor is greater than 1, the PT is capable of performing ZVS operation of the half-bridge, operated with a matched load, which is the worst case condition [4].

$$V'_P = \left(0.304\frac{1}{n^2}\frac{C_{d2}}{C_{d1}} + 0.538\right)(0.585\eta + 0.414) \tag{2}$$

The soft switching factor is an expression of maximum obtainable soft switching capability. This point of maximum soft switching capability is located slightly above the resonance frequency, where the series resonance network becomes inductive and if the soft switching factor is above 1, the network contains sufficient resonating energy, to charge and discharge C_{d1}.

Equation (3) expresses the efficiency of the PT, in to a matched load, with the simplified loss resistor R [4]. The loss resistor extracted from the FEM simulation is only a small signal simulation of the impedance and hence only results in a small signal efficiency. Furthermore the loss mechanisms of piezoelectric materials are not fully implemented in the FEM simulation, therefore this efficiency is more a relative measure to compare between different FEM designs.

$$\eta_{match} = 1 - \frac{2RC_{d2}}{n^2\sqrt{LC}} \tag{3}$$

The performance properties for the interleaved IDE PT design are calculated in table II. The gain A_{ZVS} from the first harmonic input to the output, output power P_{ZVS} and output voltage $V_{out,rms}$ [17], is the respective gain, power and voltage in to at matched load, at a 48V half-bridge voltage, when operating at the maximum ZVS point.

With a soft switching factor of 1.03 the PT possesses soft switching capabilities, which enables the inductor-less operation. It has a high efficiency and a high gain, that results in a $851V_{rms}$ output voltage, into a matched load, with a PT modulation voltage of $19.3V_{rms}$, which is the first harmonic, of the 48V half-bridge voltage [4]

TABLE II. PT EQUIVALENT LUMPED PARAMETER MODEL PERFORMANCE PROPERTIES.

V'_P	A_{ZVS}	P_{ZVS}	R_{match}	η_{match}	$V_{out,rms}$
1.03	44	1.78W	389kΩ	0.996	851V

A. *Volume optimization*

With 40 primary layers of 180µm and IDE thickness of 70µm, the primary section occupies 33% of the PT structure, where the IDE's occupies 27.7% of the primary section. In table III it can be seen that the primary section size has to be approximately 5% larger than a normal thickness mode structure (no inactive material). As the 27.7% of inactive material degrades the performance of the primary section and hence degrades the soft switching capability. Furthermore the ratio of the primary layer thickness and the tape thickness is shown and for a 20mm IDE PT design, this ratio is as low as 3.3 and the IDE's cannot be considered as solid electrodes any more. Furthermore the primary section size has to be increased from 33% to 36%, in order to achieve soft switching, with an astonishing 38% of the primary section is inactive material and this 20mm design is pushing the IDE PT structure beyond its limits.

B. *Power density*

Power density is a figure of merit with in power electronic to compare different topologies, designs and components [18]. By definition power density is the ratio between output power and volume (4). However the output power of the PT depends on a lot of external factors: Input amplitude, input wave shape (e.g. sinus or square), frequency, temperature and cooling, load condition and mechanical fixture, are all factors that have influence on the output power of the PT [4, 10, 12, 19-21].

$$\rho = \frac{P_o}{Vol} \tag{4}$$

For the volume parameter it is normal to only include the actual volume of the PT itself. The limiting factor of the power density is the ability to dissipate the power loss of the component. If the component is allowed to reach infinitely high temperatures, it would be possible to achieve infinitely high power densities. A temperature rise of 40ºC is at typical allowable temperature rise.

IV. EXPERIMENTAL RESULTS

Several prototypes were produced, as shown in Fig. 8, and in the following section the functionality and properties of the 30x10x2mm prototype PT is investigated.

A. *PT impedance and perfoamance*

Fig. 9 shows the impedance measurement of the prototype PT showing a clear resonance and anti-resonance of the

TABLE III. PT PRIMARY VOLUME AND SOFT SWITCHING CAPABILITY OPTIMIZATION.

	Thickness mode		**IDE structure**		
PT size	***30mm***	***30mm***	***30mm***	***20mm***	***20mm***
Pri vol.	30%	33%	33%	33%	36%
IDE vol. of Pri			**27.7%**	**41.6%**	**38.2%**
Pri th./Tape th.			5.5	2.9	3.3
V'_P	1.096	1.255	**1.028**	**0.955**	**1.039**

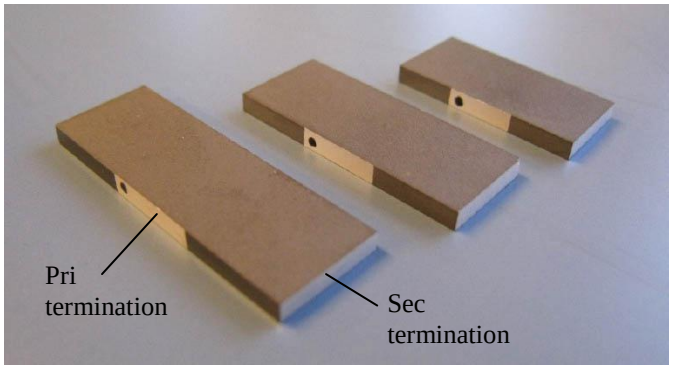

Figure 8. Picture of prototype PT's of different sizes (length from left: 30mm, 25mm and 20mm).

operational resonance mode. From the impedance measurements the equivalent lumped parameters of table IV and the performance properties of table V are calculated.

As it can be seen that the prototype PT is right on the boundary of soft switching capability and has shown to be insufficient to operate under ZVS with a matched load, as the half-bridge does add some parasitic capacitance. But when utilizing an output rectifying circuit, the matched load condition is not met and ZVS operation is possible, as illustrated in Fig. 10.

B. *Power density measurements*

The power density of the prototype PT have been measured

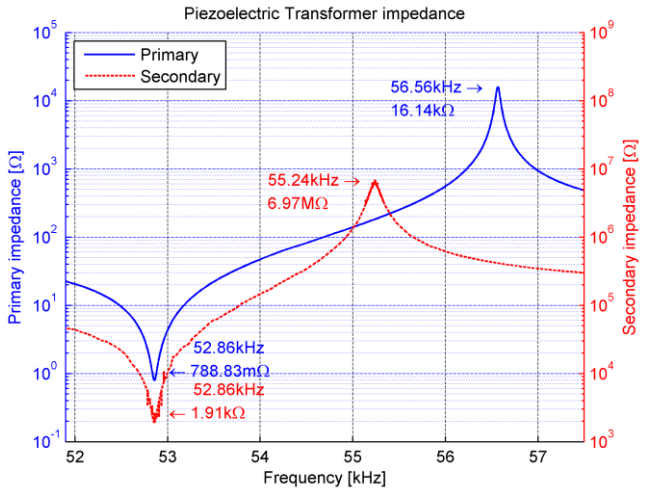

Figure 9. Measurement of the 30x10x2mm prototype PT primary and secondary impedance magnitude, performed with a HP4194A impedance/gain-phase analyzer.

TABLE IV. PROTOTYPE PT EQUIVALENT LUMPED PARAMETERS OBTAINED THROUGH IMPEDANCE MEASUREMENTS.

R	C	L	C_{d1}	C_{d2}	1/n
789mΩ	3.91nF	2.32mH	27nF	18.62pF	47.8

TABLE V. TABLE 1: PROTOTYPE PT EQUIVALENT LUMPED PARAMETER MODEL PERFORMANCE PROPERTIES.

V'_P	A_{ZVS}	P_{ZVS}	R_{match}	η_{match}	$V_{out,rms}$
1.00	38	3.37W	158kΩ	0.978	738V

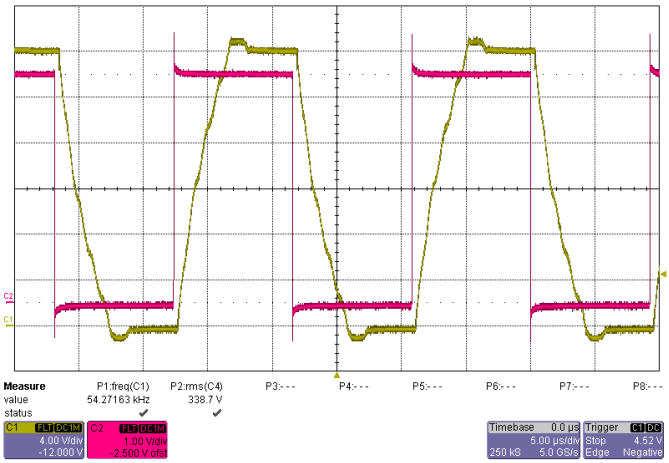

Figure 10. Measured driving PWM (red) and input half-bridge voltage (yellow), where the relative slow rising switching flanks (resonance current charges C_{d1}) and body-diode conduction voltage drop, when reaching the supply rails, clearly reveals ZVS operation. Time base [5µs/div], driving PWM [1V/div] and input half-bridge voltage [4V/div].

and as the Interleaved Rosen type PT of [22] has the exact same dimensions, giving them the same volume, surface and ability to dissipate power, they can be compared directly. The measurements have been performed with an applied AC excitation voltage and a matched load. The excitation voltage has been stepwise increased, increasing the output power, and the settling temperature rise has been measured. Furthermore the PT is excited at the frequency of maximal soft switching capability, in order to reflect the performance of the actual operation. The power density measurements of Fig. 11 show that a power density of 11W/cm^3, of the interleaved IDE PT, can be expected, with a temperature rise of 40ºC. The interleaved IDE PT also demonstrates close to 5 times better power density compared to the Interleaved Rosen type PT.

V. DISCUSSION

In order to evaluate the design the measured figures of table IV and V, is compared with the FEM simulation obtained

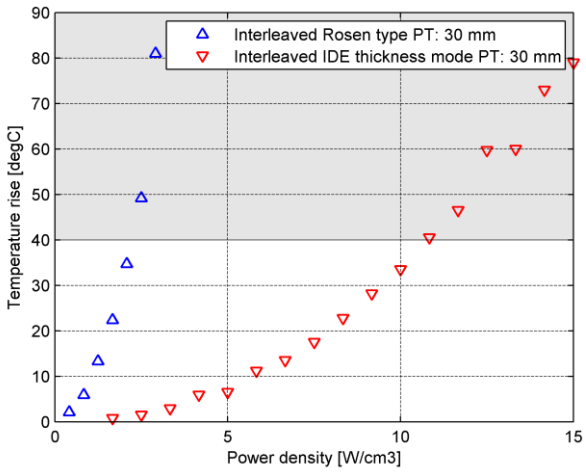

Figure 11. Power density measurement of the Interleaved IDE PT, compared with the Interleaved Rosen type PT [22], operated at the maximum soft switching frequency.

figures of table I and II. As it can be seen the correlation between the soft switching factors (V'_P) is also very good, despite it being too low to operate under ZVS at matched load condition. But it has shown to be sufficient when operating with a output rectifier. Looking at the lumped parameters C_{d1}, C_{d2} and the efficiency, the correlation is not that good. This is expected to be caused by a bad correlation between the NCE46 material parameters in the FEM simulation and what they are in real life, as well as the FEM simulation has an incomplete loss model for piezoelectric materials. Looking at the gain (A_{ZVS}) it is also 15% lower than expected. All in all the correlation between the FEM simulation and the prototype are not that good, except for the soft switching factor, but we did also face inconsistence results, when reproducing prototypes. The two most likely reasons for this, is the FEM simulation simplification of consistent vertical electrodes, instead of the real IDE structure, and with a primary layer thickness to tape thickness ratio as low as 5.5, this simplification does simply not reflect reality. The second reason is the physical consequences of such a low ratio, as the electrical fields of the IDE's do not produce a relative homogeneous field across the primary layers, which can result in a inefficient polarization, leading to even more inactive or inefficient material [23]. Nevertheless the interleaved IDE PT does demonstrate soft switching capabilities, as well as it demonstrates its potential in power density Fig. 11. If the IDE PT structure is to exploit its potential, a less aggressive design than the one presented here, should be used. The main concern is to have a higher primary layer to tape thickness ratio, preferably higher than 10, which can simply be achieved by decreasing the tape thickness for this design. It can obviously also be achieve by increasing the primary layer thickness, which could be accomplished by doubling the driving voltage, demanding half the PT gain, resulting in a doubling of the primary layer thickness. Furthermore the inactive material should be minimized, where the IDE thickness is primarily determined by production limitations. In the end the IDE PT structure might be better suited for other applications, with higher input voltage and lower gain requirements.

VI. Conclusion

I this paper an interleaved interdigitated electrode (IDE) multilayer piezoelectric transformer (PT) utilizing longitude and thickness mode vibrations has been developed. The PT is optimized for soft switching, inductor-less operation, high step-up and high output voltage, for driving a 2.5kV EAP actuator. The development has mainly been performed through iterative finite element method simulations. With a primary layer thickness to tape thickness ratio as low as 5.5, the simplified FEM model did have some shortcomings, resulting in a degrade correlation. Furthermore this low ratio is pushing the physical limits of the IDE PT structure, resulting in inconsistent prototypes, as well as a further degradation of the correlation. Nevertheless the developed 30x10x2mm prototype PT has demonstrated to just possess soft switching capabilities, with a soft switching factor of 1.00, which enables the utilization of inductor-less topologies, as well as having a high gain of 38. Furthermore it demonstrates its potential having a power density of 11W/cm^3.

Acknowledgements

Finally we would like to thanks Noliac A/S for the production of prototype PT's, as well as general PT design support. We would also like to thanks HTF for their financial support.

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Appendix: A5

T. Andersen, M. A. E. Andersen O. C. Thomsen, M. P. Foster and D. A. Stone, "Nonlinear Effects in Piezoelectric Transformers Explained by Thermal-Electric Model Based on a Hypothesis of Self-Heating", submitted to IECON, 2012.

Nonlinear Effects in Piezoelectric Transformers Explained by Thermal-Electric Model Based on a Hypothesis of Self-Heating

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***Abstract*- As the trend within power electronic still goes in the direction of higher power density and higher efficiency, it is necessary to develop new topologies and push the limit for the existing technology. Piezoelectric transformers are a fast developing technology to improve efficiency and increase power density of power converters. Nonlinearities in piezoelectric transformers occur when the power density is increased enough. The simple linear equations are not valid at this point and more complex theory of electro elasticity must be applied. In This work a simplified thermo-electric model is developed to explain nonlinearities as voltage jumps and voltage saturation and thereby avoid the complex theory of electro elasticity. The model is based on the hypothesis of self-heating and tested with measurements with good correlation.**

I. INTRODUCTION

A piezoelectric transformer (PT) is a highly resonant electromechanical component where energy is transferred by acoustical waves. Within power electronic PTs is an alternative to conventional electromagnetic transformers [1, 2] especially for high voltage applications [3-6].

In order to transfer energy through the PT it is operated close to one of its resonance frequencies. For each resonance frequency there is a corresponding acoustical standing wave in the PT. The PT resembles a distributed network however the high quality factor of PTs (Q > 1000) makes it possible to split the distributed network into different resonances modes. So for simplicity and mathematical representation, often only the resonance mode of interest is modeled [7-9]. One of the most used PT models is the lumped element parameter model, which was derived by Mason in 1942 [10] and is illustrated in Fig. 1.

The Mason model is a useful tool to understand the electrical behavior. However the model has its limitations.

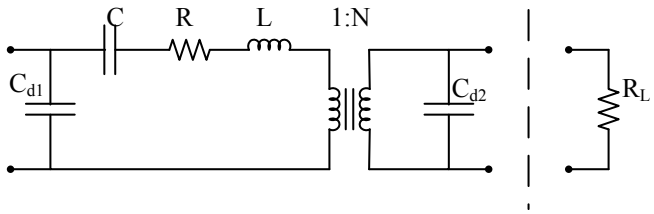

Fig. 1: Mason equivalent model of a piezoelectric transformer valid in the vicinity of a single resonance.

The model is only valid around the resonance frequency and it can only predict the linear behavior of a PT. The model is sufficient for power converter applications as long as the PT is kept within its linear region of operation. However the trend goes in a direction of smaller power converters and to keep up with the demand of higher power densities, PTs will be forces into the region of nonlinear operation. Therefore we need to understand the nonlinear effects of PTs to either prevent them by better PT designs or deal with them in the control circuit.

Two of the nonlinear effects of PTs are gain saturation and a phenomenon called voltage jumps. In the literature these nonlinear effects are associated with the relatively large mechanical deformation around resonance of a PT and are described by the nonlinear theory of electro elasticity [11, 12].

In this paper the nonlinear effects as gain saturation and voltage jumps are explained from a simple thermo-electric model of a PT based on measurements and the hypothesis of self-heating.

II. THEORY

To understand the nonlinear phenomena, we need to understand the linear behavior of a PT first. At low voltages there is a linear relation between input voltage and output voltage. This relation can be calculated from the Mason model [13] in Fig. 1 and is given by the gain as seen in equation (1). The equation is derived from the Mason model and is therefore only valid around the resonance frequency.

$$A = \frac{N\cdot(\alpha - R)(1 - jC_{d2}\cdot R_L\cdot\omega)}{\alpha + j\beta} \tag{1}$$

$$\alpha = R + \frac{R_L}{N^2\cdot\left((R_L\cdot C_{d2}\cdot\omega)^2+1\right)} \tag{2}$$

$$\beta = \omega\cdot L - \frac{1}{\omega\cdot C} - \frac{\omega\cdot C_{d2}\cdot R_L^2}{N^2\left((R_L\cdot C_{d2}\cdot\omega)^2+1\right)} \tag{3}$$

Gain is strongly frequency depended because of the high mechanical quality factor of a PT. A typically gain curve of a PT working in the linear region is illustrated in Fig. 2.

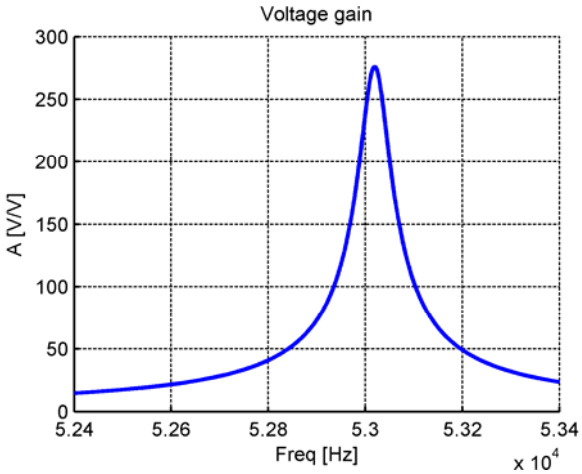

Fig. 2: Voltage gain curve derived from the Mason model. Independent of input voltage

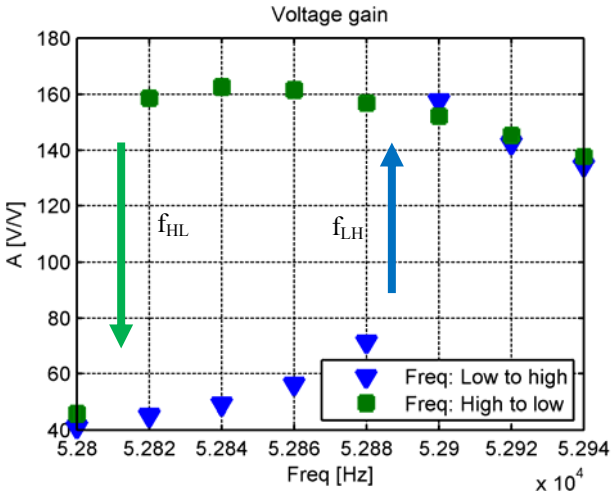

Fig. 3: Voltage gain curve obtained from measurements. Voltage jumps occur at different frequencies depending on sweep direction.

A. *Efficiency and losses*

There are generally three types of losses in a PT [14]; piezoelectric coupling, electrical and mechanical. The electrical losses are mainly dielectric losses in the material and can be model as to parallel resistors across C_{d1} and C_{d2} in the Mason model. The piezoelectric coupling loss and the mechanical vibration losses are summarized in the resistor R in the Mason model of Fig. 1. Research indicate that dielectric losses are small compared to the mechanical losses [15, 16]. However dielectric losses will not be considered in this paper and are assumed to be zero.

The efficiency of a PT with the assumption of no dielectric losses can be calculated using the Mason model connected with a load resistor [7, 13]. Equation (4) shows the relation.

$$\eta = \frac{R_L}{N^2 R \cdot \left(1+(\omega C_{d2} R_L)^2\right)+R_L} \tag{4}$$

Efficiency is not as dependent on frequency as the voltage gain of the PT.

B. *Nonlinear effects*

Increasing the input voltage forces the PT into the nonlinear region and effects like voltage jumps may occur. More specific a voltage jump occur when a high input voltage is applied and sweep across the resonance frequency of the PT. At some frequency the output voltage will suddenly jump, which is equivalent to a jump in the gain curve. However the jumps occur at different frequencies depending on the direction of the frequency sweep. Starting at low frequency below the resonance frequency and sweeping to a high frequency above the resonance frequency gives a voltage jump a one particular frequency (f_{LH}). But starting the sweep from the high frequency towards the low frequency gives a voltage jump at another particular frequency (f_{HL}). At Fig. 3 the situation of a nonlinear gain curve is sketched.Voltage jumps in the nonlinear gain curve has a hysteretic relation and cannot be explained from the Mason model.

III. Self Heating Theory

In the literature the voltage jump phenomena is described by the nonlinear theory of electro elasticity [11, 12]. Another hypothesis to describe this nonlinearity is by the fact of self-heating. A PT excided by a voltage will generate heat as a consequence of internal losses. The generated heat may have influence on the internal losses and thereby creating a feedback system.

A. *Temperature dependency*

From research we know that the temperature has impact on the PTs performance. Measurement shows that the mechanical quality factor of the PT material is decreasing as the temperature increases [15, 17]. Mechanical quality factor is related to the resistor R of the Mason model by equation (5)

$$Q_m = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{5}$$

Both the gain curve and the efficiency are depended on the loss resistor and are therefore affected by temperature changes. Another temperature related effect is the change in the PTs resonance frequency. As the temperature increases the resonance frequency decreases [15]. Resonance frequency is related to the ratio of L and C in the Mason model.

B. *Thermo-electric model*

The thermo-electric model links changes in temperature to changes in the loss resistance and indirectly the ratio between

L and C by a frequency shift. Furthermore it is assumed that temperature changes have a linear influence. The thermo-electric model is based on equations derived from the Mason

equivalent model and all the parameters in the Mason model are assumed constant with exception of the loss resistance.

The fact that temperature has a negative impact on the resonance frequency of the PT can be modeled by a change in the ratio between L and C. However for simplicities the change in resonance frequency is modeled by a shift in frequency assuming L and C constant at all time. Equation (6) assumes a linear relation between temperature change and frequency shift.

$$f_x = f \cdot (1 + K_1 \cdot \Delta T) \tag{6}$$

A positive temperature change resulting in a frequency shift of one percent is illustrated in Fig. 4 for a gain curve. As expected the rise in temperature shifts the resonance down in frequency.

With the assumption of L and C being constant the quality factor is inverse proportional with the loss resistor. Using an assumption of linear relation between temperature change and loss resistor gives the relation in equation (7).

For a positive temperature change resulting in an increase of the loss resistance R at 40 percent is illustrated in Fig. 5. As the temperature increases the loss resistance increases as well and a reduction in the gain curve is expected.

$$R_x = R_0 \cdot (1 + K_2 \cdot \Delta T), \qquad R_0 = R(T_0) \tag{7}$$

C. *Feedback*

temperature change caused by self-heating is due to power dissipation within the PT itself. The steady state change in temperature can be model by a thermal resistance to the surroundings when the power dissipation in the PT is known (8), neglecting nonlinear effects from thermal radiation and convection.

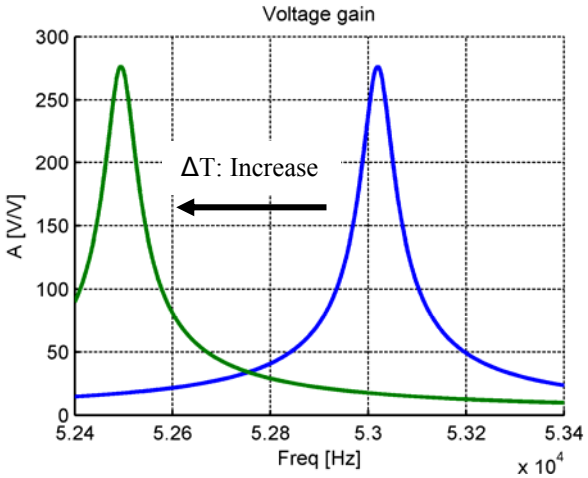

Fig. 4: Gain curve before and after a frequency shift of 1% from an increase in temperature.

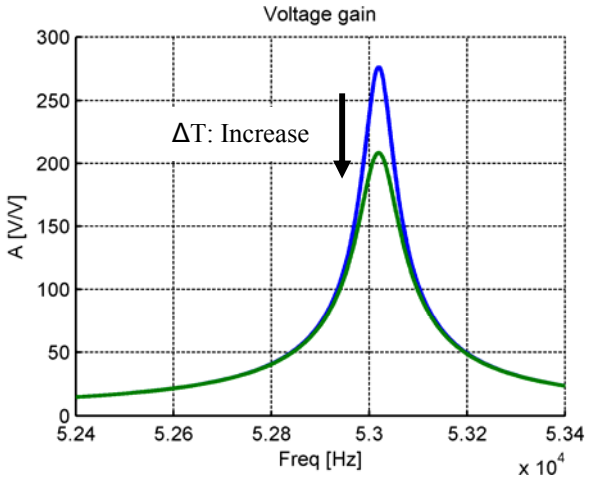

Fig. 5: Gain curve before and after an increase in loss resistance of 40% form an increase in temperature

$$\Delta T = R_{th} P_D \tag{8}$$

However the thermal capacitance of the PT is necessary to include as well, it brings stability in to the thermal-electric model and eliminate artificial oscillations. The thermal resistance together with the thermal capacitance forms a low pass filter in the feedback loop. Equation (9) shows the relation between temperature change and power dissipation for a given time step. Equation (9) approaches the steady state solution in equation (8) for time steps approaching infinity and artificial oscillations may then occur.

$$\Delta T = R_{th} P_D + (\Delta T_0 - R_{th} P_D) e^{\frac{-\Delta t}{C_{th} R_{th}}} \tag{9}$$

Power dissipation within the PT can be related to the output power of the PT. Output power is equivalent to the power dissipated in the load resistor. Equation (10) shows the relation between power dissipation, output power and the efficiency of the PT. From the Mason model the efficiency can be calculated for a given resistive load (4). Efficiency, is like the gain curve function (1), affected by changes in loss resistance. However the efficiency's dependency of frequency is not affected by temperature as the gain curve is.

$$P_D = P_L \cdot \left(\frac{1}{\eta(f, R_x)} - 1 \right) \tag{10}$$

Output power of the PT is equivalent to the power dissipated in the load resistor and is equal to the RMS value of the output voltage divided by the load resistance (11). For a resistive load the output voltage of the PT is sinusoidal and the RMS value is simply the square root of two, times the amplitude of the output voltage. Output voltage is related to

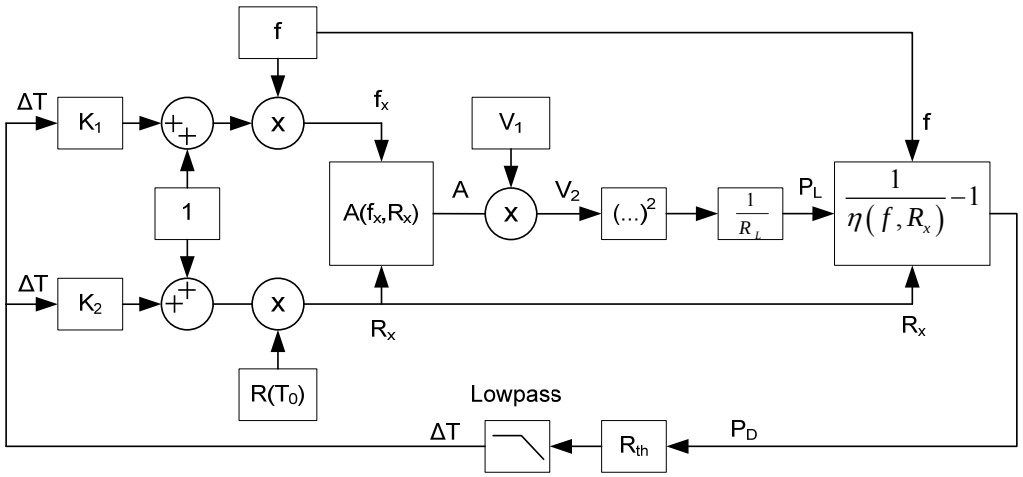

Fig. 6: Thermo-electric model of a PT with the effect of self-heating. Fixed parameters: L, C, Cd1, Cd2, N and R. Fitted parameters from measurements: K_1, K_2 and R_{th}. Variable input parameters: frequency (f) and input voltage (V1).

the input voltage by the temperature dependent gain function (12).

$$P_L = \frac{V_2^2}{2 \cdot R_L} \tag{11}$$

$$V_2 = V_1 \cdot A\left(f_X, R_X\right) \tag{12}$$

By equation (12) the feedback loop is closed. Combining all the equations gives the thermo-electric model of the PT. A block diagram representation of the equations in the thermo-electric model is illustrated in Fig. 6.

Table I
Summary of variables

Parameters	Units	Notes
f_x	Hz	Shifted frequency
f	Hz	Applied frequency to the PT
K_1	$(C°)^{-1}$	Constant
ΔT	$C°$	Temperature change
R_x	Ω	Temperature dependent loss resistor
R_0	Ω	Resistance at zero temperature change
K_2	$(C°)^{-1}$	Constant
T_0	$C°$	Ambient temperature
R_{th}	$C°/W$	Absolute thermal resistance to surroundings
P_D	W	Power dissipation in PT
ΔT_0	$C°$	Temperature change just before time step
Δt	s	Time step
P_D	W	Power dissipation in PT
P_L	W	Power dissipation in load
$\eta(f, R_x)$	-	Temperature dependent efficiency
P_L	W	Power dissipation in load
V_2	V	Output voltage
R_L	Ω	Load resistance
V_1	V	Input voltage
$A(f_x, R_x)$	-	Temperature dependent gain

IV. Results

All the parameters needed for the thermal-electric model are derived from measurements on a PT. The PT used in this work is an interleaved Rosen-type transformer indented for high step-up applications, with the dimentions: 30 mm x 10mm x 2 mm [18]. Fig. 7 shows 4 PTs of different length, where the second from the left is the 30 mm used in this work.

A. Measuring of Mason lump parameters

The Mason model parameters for the thermo-electric model are fixed values derived from impedance measurements of the PT at low power [8, 19]. Table II shows the Mason lump parameters obtained from measurement. In particular a HP4194A gain/phase analyzer is used to obtain the impedance plots of the PT to derive the lump parameters. From experience it is known that the lump parameters are very sensitive for any changes in the physical fixture of the PT. Especially the loss resistance and the resonance frequency. Therefore the parameters R and C are corrected to compensate for the change in the mechanical fixture of the PT from impedance measurements to voltage gain curve measurements.

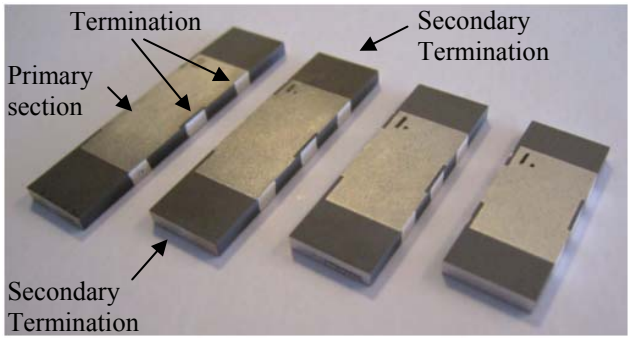

Fig. 7: Picture of interleaved Rosen-type prototype PT's of different sizes (length from left: 35mm, 30mm, 25mm and 20mm).

Table II
Mason lump parameters from measurements of the 30 mm PT. *Corrected to compensate for changes in mechanical fixture

R	R*	C	C*	L	C_{d1}	C_{d2}	N
325mΩ	460mΩ	9.26nF	9.31nF	971µH	132nF	19.4pF	106

B. *Thermal parameters*

Values of the temperature changes are not of interest in this work and no temperature measurements are performed. Thermal resistance to the surroundings (R_{th}) are estimated from related work [20]. Thermal capacitance of the PT (C_{th}) is based on the specific thermal capacity of the PTZ material (350 J/kg·K). However in the model the thermal capacity is modeled as a running average in the thermal-electric model. The thermal parameters K_1 and K_2 are fitted from measurements of the PTs gain curves at different input voltages. Therefore the ratios between the thermal parameters are not of relevance.

Table III

R_{th}	C_{th}	K_1	K_2
$40\,C°/W$	1.64J/K	$0.045(C°)^{-1}$	$825\cdot10^{-6}(C°)^{-1}$

C. *Measuring of voltage gain curves*

The setup for measure the voltage gain curves of the PT consist of a sinus generator with an amplifier for delivering the driving voltage for the input to the PT (V_1). The output of the PT (V_2) is loaded with a resistive load (R_L) in parallel with a capacitor (C_L). The capacitor is selected large compared to output capacitance (C_{d2}) and serve the purpose of neglecting the effects of change in (C_{d2}) and parasitic capacitance from measurement equipment. The resistive load is selected so the efficiency of the PT is very pure to increase the self heating effect of the PT. An oscilloscope is used to measure input (V_1) and output (V_2) voltages. Fig. 8 illustrates the measurement setup with the Mason equivalent for the PT.

Table IV

C_{d2}	C_L	C_{probe}	C_{eq}	R_L
19.4pF	228pF	8.8pF	256pF	159kΩ

The equivalent output capacitance (C_{eq}) of the PT is the sum of PT output capacitance (C_{d2}), load capacitance (C_L) and parasitic capacitance from measurement equipment (C_{probe})

Measurements are performed by sweeping the frequency of the sinus generator. Starting at a low frequency (52.80 kHz) and stepping up to a high frequency (53.75kHz) and then stepping back again (52.80kHz). Fig. 9, Fig. 10 and Fig. 11 plots the measured and simulated gain curves for three different input voltages: 13mV, 57mV and 290mV respectively.

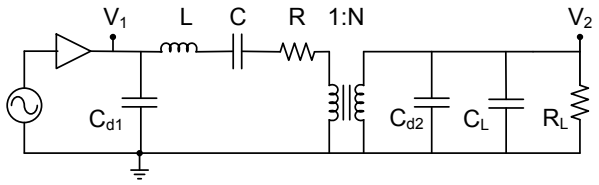

Fig. 8: Sketch of the measurement setup for obtaining voltage gain curves.

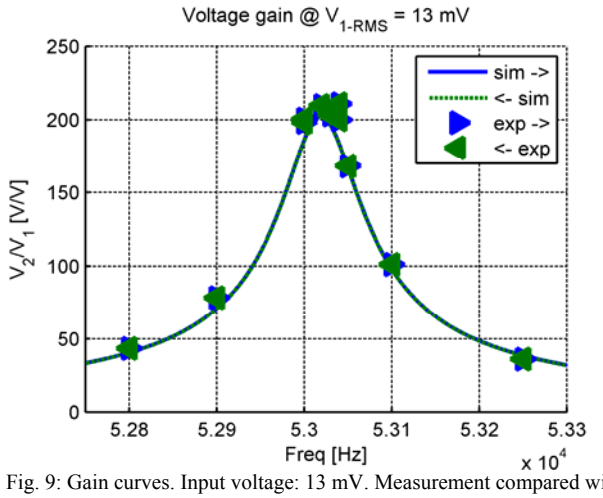

Fig. 9: Gain curves. Input voltage: 13 mV. Measurement compared with the thermo-electric model

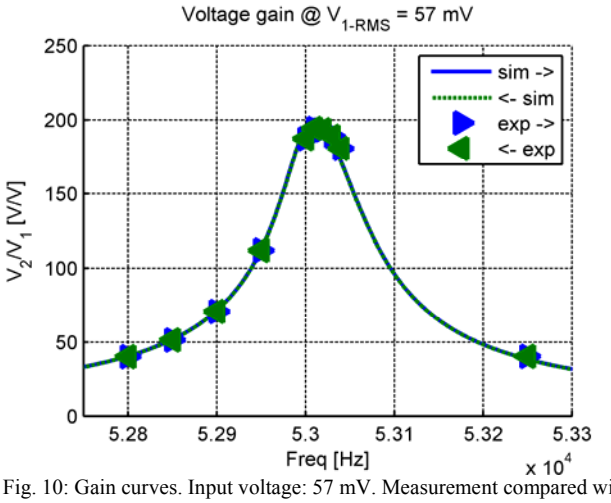

Fig. 10: Gain curves. Input voltage: 57 mV. Measurement compared with the thermo-electric model

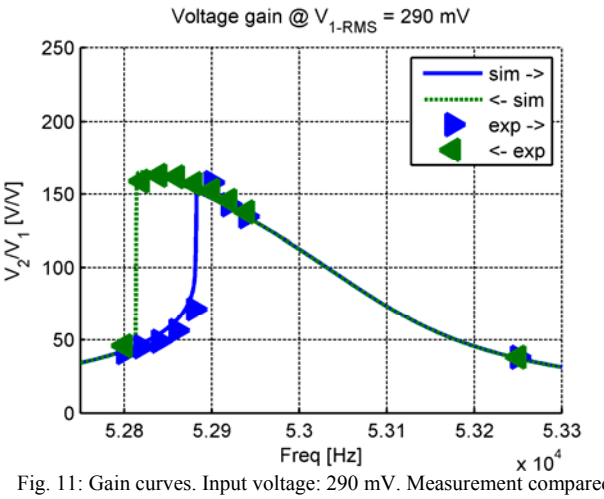

Fig. 11: Gain curves. Input voltage: 290 mV. Measurement compared with the thermo-electric model

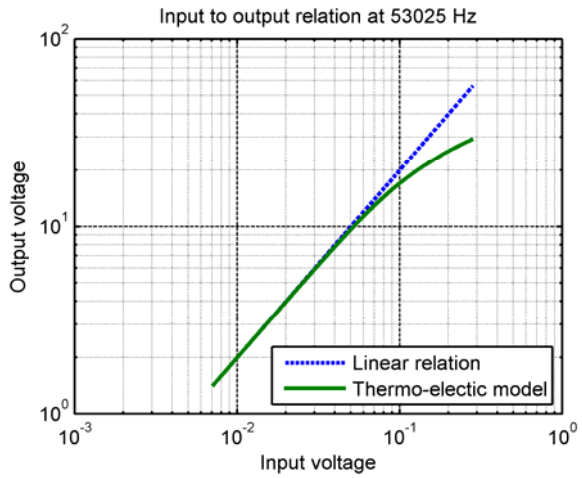

Fig. 12: Simulated relation between input and output voltage shows saturation behavior at higher voltages.

D. *Simulation of gain saturation*

Another nonlinear effect of PTs is gain saturation. The linear relation between input and output voltage is lost when the input voltage become too high. In literature this phenomena is described by nonlinear theory of electro elasticity [11, 12]. However the same phenomena can be simulated with the thermo-electric model. Fig. 12 shows a simulation of the relation between input and output voltage for the 30mm PT. In this simulation the frequency is kept constant and only the input voltage is changed. The simulation shows that saturation of the output voltage occurs for higher voltages.

V. Conclusion

A simple thermo-electric model based on the hypothesis of self-heating within the PT is constructed. The model is tested against a set of measurements of nonlinear voltage jumps. The correlation between the model and the measurements are good compared to the rough assumptions applied. The thermo-electric model should be seen as an aid in understanding the nature of PTs when the power density is increased beyond the PTs linear operation.

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Appendix: A6

T. Andersen, M. S. Rødgaard and M. A. E. Andersen, "Active Match Load Circuit Intended for Testing Piezoelectric Transformers", in PEMD, 2012.

Active Match Load Circuit Intended for Testing Piezoelectric Transformers

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Keywords: Piezoelectric transformer, Match load.

Abstract

An adjustable high voltage active load circuit for voltage amplitudes above 100 volts, especially intended for resistive matching the output impedance of a piezoelectric transformer (PT) is proposed in this paper. PTs have been around for over 50 years, were C. A. Rosen is common known for his famous Rosen type design back in the 1950s [1]. After the discovered of new piezoelectric materials and new PT designs have been invented, the PT based power converters are in the area where they can outperform tradition electromagnetic based converters in certain applications [2]. The performance of PTs can be measured and compared on its zero voltage switching (ZVS) factor [3-5], power density, and efficiency. Common for these three parameters are that they need to be measured with a match load connected at the output of the PT.

1 Introduction

A PT is a highly resonant electromechanical component where energy is transferred by acoustical waves. In order to transfer energy through the PT it is operated close to one of its resonant frequencies. For each resonance frequency there is a corresponding acoustical standing wave in the PT. The resonance frequencies are determined by the material, geometrical shape, temperature and its load conditions. Due to the relatively high quality factor of a PT (Q > 1000) the electrical behaviour around one of its resonance frequency can be described by the Mason model [6].

From the Mason equivalent model, figure 1, the efficiency of the transformer can be calculated for a given load [3, 7]. For a resistive load, the maximum efficiency is obtained if the load satisfied the match load condition as equation (1) and is

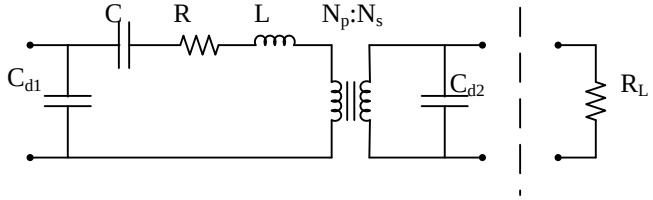

Figure 1: Mason model of a piezoelectric transformer valid only around the resonance frequency.

dependent on the operating frequency and the output capacitance C_{d2} [7].

$$R_{L,match} = \frac{1}{2\pi f \cdot C_{d2}} \approx \frac{1}{2\pi f_r \cdot C_{d2}} \qquad (1)$$

It can also be shown that the ZVS factor, the PTs ability to soft switch, has a global minimum at match load [3]. If the PT is capable of soft switching at mach load, it can soft switch for any resistive load. Measuring the power density of PTs is done where the efficiency is highest. Therefore a match load is connected at the output to obtain maximum efficiency.

Prior art within resistive match loading, has been to solder off-the-shelf ¼ watt leaded resistors together in a manner to obtain the correct resistive value as well as handle the power dissipation (< 20 watt) and voltage stress (< 1.2kV). Potentiometers that can handle the power and the voltages suffers from high parasitic inductions and can therefore not be used. Figure 2 show a typical example of a match load construction. A standard ¼ watt resistor has a voltage rating of 250V. It is a time consuming process of solder a match load, especially for high voltage and high power.

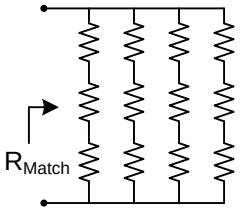

Figure 2: 4 by 3 matrixes of leaded ¼ watt resistors.

Each PT design usually requires a new match load design. It is also time consuming to adapt one match load matrix to another value.

2 Active match load

There is a need for an adjustable resistive load with low parasitic capacitance and parasitic inductance. The proposal in this paper is to control a MOSFET in its linear region to act as a resistor. In figure 3 the principle is illustrated. By measuring the voltage across the MOSFET as a reference signal and subtracting the current through the MOSFET an error signal is generated.

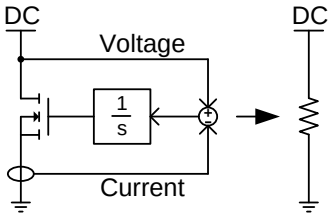

Figure 3: Simulated resistor by a MOSFET with feedback. Only valid for positive voltages.

The error signal is then integrating and the result is a current proportional with the voltage; a resistor. The principle in figure 3 only works for positive voltages. At negative voltages the body diode of the MOSFET becomes forward biased and the voltage across the MOSFET is clamped to the forward voltage drop of the body diode. At negative voltages the circuit acts as a diode and not as a resistor.

For the circuit to act as a resistor for both positive and negative voltages a full wave bridge rectifier is used. The voltage drop of the rectifier contributes to a non-resistor characteristic, especially at voltages comparable with the voltage drop of the rectifier. As the circuit is indented for sinus waveforms at amplitudes above 100 volts, it is of less concern. The output of the rectifier is a positive voltage with twice the frequency of the input. The principle circuit from figure 3 combined with a full wave bridge rectifier is illustrated in figure 4.

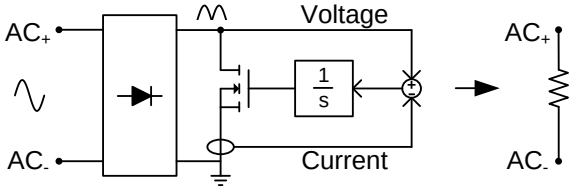

Figure 4: Simulated resistor for positive and negative voltages.

2.1 Voltage measurement

The voltage feedback signal is used as a reference signal for the current feedback. Ideally the voltage should be measured at the input terminals to the rectifier to avoid the voltage drop from the rectifier. Measuring the voltage on the input at the rectifier, require high common mode rejection to operate successfully, which complicates the voltage measuring circuit. As the circuit is indented for voltage amplitudes above 100 volts the induced error by measuring the voltage after the rectifier is of little concern. However sacrificing the precision of the measurement by measure the voltage after the rectifier greatly reduces the complexity of the circuit. A resistive voltage divider can then be used. Changing the ratio of the divider is an easy way of adjusting the value of the active load. A potentiometer is used for the adjusting.

2.2 Current measurement

The current can be measured in different ways. One method is to the sense the voltage across a resistor placed in series with the source pin of the MOSFET, see figure 5.

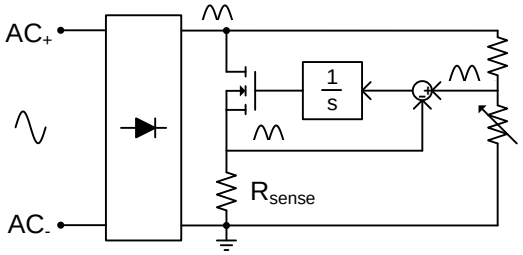

Figure 5: Simulated resistor using a sense-resistor (R_{sense}) in the MOSFETs source path to obtain the current feedback signal.

The benefit of a sense-resistor (R_{sense}) in the source path of the MOSFET is clear from a measuring point of view. It is a low impedance and low voltage measurement directly related to ground potential of the circuit. However from a control point of view the resistor is not only measuring the current running into drain of the MOSFET but also the current running through the parasitic gate-source capacitance. In application where a high ohmic load is preferred in combination with high frequency, the drain current becomes comparable with the current running through the gate-source capacitance. The sense resistor sums both currents and feed them back, resulting in an error estimation of the real current (drain current). To compensate for the contribution from the gate-source current an independent measurement of the gate-source current is needed and will complicated the overall current measurement circuit.

Another approach to measure the current is to use a current sense transformer (CST). With a CST the current in the drain path of the MOSFET can be measured even at high voltages. Measuring of the current at the input to the bridge rectifier can be done event at the high common mode voltages due to the low capacitive coupling between primary and secondary of a CST. Placing the CST at the input to the bridge rectifier ensures that non-linearity from the rectifier is measured. A block diagram is shown in figure 6. Measuring the current at the input has the drawback of complicating the measurement circuit compared to a drain current measurement. The input current is sinusoidal and therefore the output of the CST is also sinusoidal and cannot be used directly as a feedback signal before it has been rectified. A full wave bridge rectifier consisting of diodes cannot be used here, as the output voltages from the CST is lower or in best case comparable with the forward voltage drop of the rectifier itself. Instead an active rectification (ABS) circuit is used to rectifier the sinusoidal signal from the CST. Thereby the signal is rectified without any voltage drop.

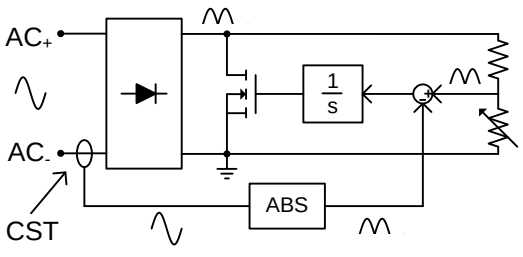

Figure 6: Simulated resistor using a current sense transformer (CST) together with an active rectifier (ABS).

3 Results

In this section the results from simulations as well as measurements will be conducted. Simulations are made in PSpice. Measurements are performed with a Rohde & Schwarz 2GHz RTO oscilloscope. A prototype is developed as illustrated in figure 7. Control together with ABS circuit is placed on the back of the PCB. Size of the PCB: 70mm x 40mm.

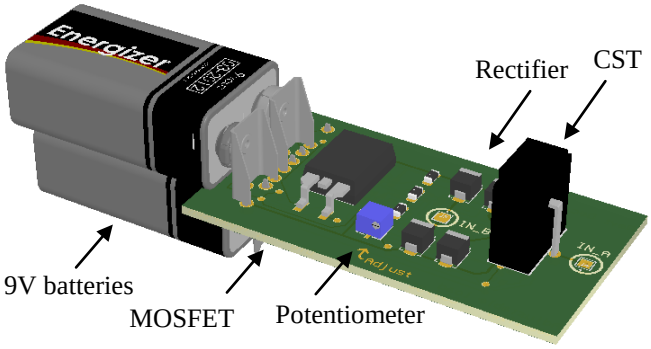

Figure 7: 3D model of the active load circuit. Control circuit is placed on the back of the PCB.

3.1 Measurement setup

For comparing the simulation and the measurement the setup illustrated in figure 8 is used. A tone-generator connected to an amplifier delivers a signal with maximum amplitude of 200 volt at a frequency of 50 kHz. The active load circuit is connected through a 100 ohms resistor. The resistor is used to measure the current through the active load. In this way a voltage across the sense resistor of 100 mV equals 1.0 mA. The rectifier diodes are rated to 50 mA, at that current the voltage across the sense resistor reached 5 volt.

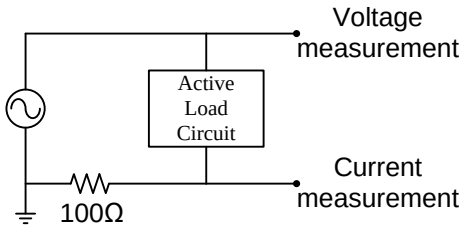

Figure 8: Setup used for measuring input voltage [1V/V] and input current [0.01A/V]

3.2 Simulations

The active load circuit has been simulated in PSpice. The result of the simulation is shown at figure 9. The sinus wave (blue) is the voltage across the active load and is perfectly sinusoidal with an amplitude of 200 volts as expected. The square-like graph (red) is a plot of the current.

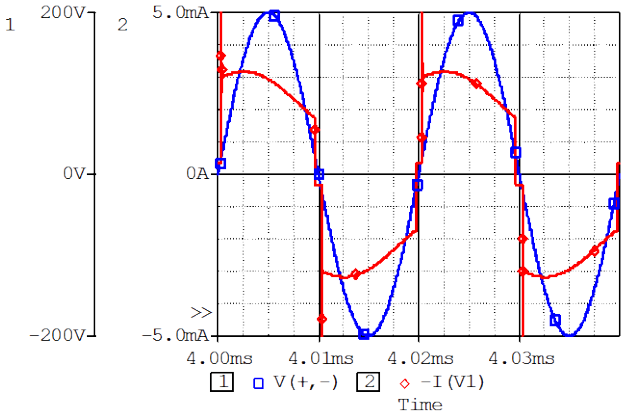

Figure 9: PSpice simulation of input voltage (blue) and input current (red) an active load. Input: ±200V@50kHz

3.3 Measurements

Measurements on the active load circuit are performed accordant to the measurement setup in figure 8. The result is shown in figure 10 as a plot from the oscilloscope (note: colours are changed and enhanced for better visibility). The blue graph is the input voltage across the active load with an amplitude close to 200 volts and a frequency of 50 kHz. The red graph is the voltage measured across a 100 ohms resistor and equivalent to the input current.

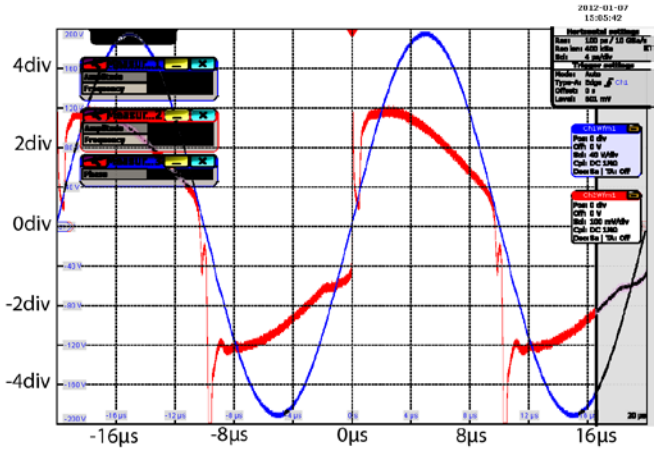

Figure 10: Oscilloscope plot (colours are changed) measurement on the prototype. Input voltage: 40V/div (blue). Input current: 1mA/div (red)

3.4 Discussion

The correlation between simulation and measurement is good. The current is in phase with the voltage indicating low parasitic capacitance and inductance. The asymmetry in the measured current is due to unmatched parasitic capacitance between the rectifier diodes as well as uneven influence from parasitic capacity from the surroundings to the circuit. Each time the voltage crosses zero a current peak is observed, this peak is caused by the parasitic capacitance in the diodes of the bridged rectifier.

Conclusion

A proposal for an active load circuit intended for resistive matching the output impedance of a PT is given. The correlation between simulation and measurement is good, however a more sinusoidal current shaped would have been preferred. The benefit compared with prior art is the ability to change the load simply by adjusting a potentiometer and thereby saving the time consuming process of construct a new resistor matrix.

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Appendix: A7

K. S. Meyer, M. S. Rødgaard, **T. Andersen** and M. A. E. Andersen, "Self-oscillating loop based piezoelectric power converter", US Patent, US application no. US61/638,883, 2012.

U.S. PROVISIONAL PATENT APPLICATION

FOR

SELF-OSCILLATING LOOP BASED PIEZOELECTRIC POWER CONVERTER

BY

KASPER SINDING MEYER
MARTIN SCHØLER RØDGAARD
AND
THOMAS ANDERSEN

SELF-OSCILLATING LOOP BASED PIEZOELECTRIC POWER CONVERTER

FIELD OF THE INVENTION

[0001] Aspects of the present disclosure relate to a piezoelectric power converter, and more particularly, to a self-oscillating loop-based piezoelectric power converter.

BACKGROUND OF THE INVENTION

[0002] Piezoelectric transformer based power converters have good potential to substitute traditional magnetics based power converters in numerous voltage or power converting applications such as AC/AC, AC/DC, DC/AC and DC/DC power converter applications. Piezoelectric power converters are capable of providing high isolation voltages and high power conversion efficiencies in a compact package with low EMI radiation. The piezoelectric transformer is normally operated in a narrow frequency band around its fundamental or primary resonance frequency with a matched load coupled to the output of the piezoelectric transformer. The optimum operating frequency or excitation frequency shows strong dependence on different parameters such as temperature, load, fixation and age. Hence, it is a significant challenge to maintain the excitation frequency applied to the input section of the piezoelectric transformer at the optimum frequency during operation of the power converter where the above-mentioned parameter changes. This is particularly pronounced if burst-mode modulation of the input drive signal is utilized because rapid lock-on to the intended excitation frequency is required to avoid large driver losses by intermediate time periods where the input driver fails to operate under ZVS.

[0003] This problem is particularly pronounced for power converters that employ a piezoelectric transformer with native ZVS properties, i.e. with a ZVS factor larger than 100%, and exploit this property to obtain ZVS in an input driver coupled directly to the primary section of the piezoelectric transformer. In this context “directly” means without an external inductor arranged in series or parallel between the input driver and the primary section of the piezoelectric transformer. ZVS operation of the input driver, typically based on a half-bridge or full-bridge MOS transistor circuit, of piezoelectric power converters has traditionally been achieved by adding such an external inductor in series with the input driver. The external inductor ensures that the input of the piezoelectric transformer appears inductive across a relatively large frequency range

such that capacitances at an output node of the input driver can be alternatingly charged and discharged in accordance with the input drive signal without inducing prohibitive power losses.

[0004] However, the external inductor occupies space, adds costs and conducts and radiates EMI in the power converter. It would therefore be advantageous to provide a power converter based on a piezoelectric transformer with native ZVS properties capable of reliable ZVS operation despite changes in operational parameters of the piezoelectric transformer such as temperature, load, fixation and age. This has been achieved in a piezoelectric power converter in accordance with the present invention by the presence of a feedback loop operatively coupled between the output signal at the output electrode of the piezoelectric transformer and the input driver to provide a self-oscillation loop around the primary section of the piezoelectric transformer. Electrical characteristics of the feedback loop are configured such that the excitation frequency of the self-oscillation loop lies within the ZVS operation range of the piezoelectric transformer.

[0005] The IEEE paper by J. Díaz et al. "A Double-Closed Loop DC/DC Converter Based On A Piezoelectric Transformer" describes a piezoelectric power converter which comprises a self-oscillating feedback loop. The input driver is, however, coupled to the input of a piezoelectric transformer via a separate external input inductor to ensure ZVS operation.

SUMMARY OF THE INVENTION

[0006] The present invention relates to a piezoelectric power converter comprising an input driver electrically coupled directly to an input or primary electrode of the piezoelectric transformer without any intervening series or parallel inductor. A feedback loop is operatively coupled between an output voltage of the piezoelectric transformer and the input driver to provide a self-oscillation loop around a primary section of the piezoelectric transformer oscillating at an excitation frequency. Electrical characteristics of the feedback loop are configured to set the excitation frequency of the self-oscillation loop within a zero-voltage-switching (ZVS) operation range of the piezoelectric transformer.

[0007] A first aspect of the invention relates to a piezoelectric power converter comprising a piezoelectric transformer which comprises an input electrode electrically coupled to an input or primary section of the piezoelectric transformer and an output electrode electrically coupled to secondary or output section of the piezoelectric transformer to provide a transformer output

voltage. An input driver is electrically coupled directly to the input electrode of the piezoelectric transformer without any intervening series or parallel inductor to supply an input drive signal to the input electrode. A feedback loop is operatively coupled between the output voltage of the piezoelectric transformer and the input driver to provide a self-oscillation loop around the primary section of the piezoelectric transformer, oscillating at an excitation frequency. Electrical characteristics of the feedback loop are configured to set the excitation frequency of the self-oscillation loop within a ZVS operation range of the piezoelectric transformer.

[0008] In accordance with the present invention, the zero-voltage-switching factor (ZVS factor) of the piezoelectric transformer is larger than 100%, preferably larger than 120%, such as larger than 150% or 200%. This means that the piezoelectric transformer has native ZVS properties or characteristics.

[0009] The ZVS factor is determined at a matched load condition as:

$$ZVS = \frac{\left(k_{eff\_S}^{-2}\right)-1}{\left(k_{eff\_P}^{-2}\right)-1} 0.882 \ ;$$

$k_{eff\_P,}$ being a primary side effective electromechanical coupling factor of the piezoelectric transformer,

$k_{eff\_S,}$ being a secondary piezoelectric transformer effective electromechanical coupling factor, in which:

$$k_{eff\_P} = \sqrt{1 - \frac{f_{res\_p}^2}{f_{anti-res\_p}^2}} \qquad k_{eff\_S} = \sqrt{1 - \frac{f_{res\_s}^2}{f_{anti-res\_s}^2}}$$

f_{res_p} = resonance frequency and frequency of a minimum magnitude of an impedance function at the input electrodes of the piezoelectric transformer with shorted output electrodes,

$f_{anti\text{-}res\_p}$ = anti-resonance frequency and frequency of a maximum magnitude of the impedance function at the input electrodes of the piezoelectric transformer with shorted output electrodes,

f_{res_s} = resonance frequency and frequency of a minimum magnitude of the impedance function at the output electrodes of the piezoelectric transformer with shorted input electrodes,

$f_{anti\text{-}res\_s}$ = anti-resonance frequency and frequency of a maximum magnitude of the impedance function at the output electrodes of the piezoelectric transformer with shorted input electrodes.

[0010] A number of highly useful piezoelectric transformers for the present piezoelectric power converters with both high power conversion efficiencies and native ZVS properties are disclosed in the applicant's co-pending European patent application No. 11176929.5.

[0011] The self-oscillating feedback loop around the native ZVS capable piezoelectric transformer with direct electrical coupling from the input driver to the input electrode without any intervening series or parallel inductor both dispenses with the external inductor. Instead ZVS operation of the input driver is ensured by the inductive behaviour of the piezoelectric transformer within the ZVS operation range of the piezoelectric transformer. Hence, the commonly employed external inductor, which occupies space, adds costs, conducts and radiates EMI as explained above, is avoided. In the direct coupling from the input driver to the input electrode, the inductance of the ordinary external inductor is replaced by the mechanical equivalent inductance already embedded in the vibratory mass of the piezoelectric transformer due to its native ZVS properties. Hence, the radiated EMI from the commonly employed external inductor is largely eliminated. Furthermore, because the ordinary external inductor often employs a ferrite core material the external inductor becomes prone to magnetic saturation from large static or dynamic magnetic fields for example in applications such as MRI scanners, power plants etc. Magnetic saturation of the ferrite core material may cause the piezoelectric power converter to malfunction. This problem is also removed by the eliminated of the ordinary external inductor. The self-oscillating feedback loop furthermore provides a mechanism for maintaining the optimum excitation frequency despite the strong dependence of electrical characteristics of the piezoelectric transformer on environmental parameters such as temperature, load, fixation and age.

[0012] The skilled person will understand that a parasitic wiring or cabling inductance naturally will be associated with the direct electrical coupling between an output of the input driver and the input electrode despite the lack of a separate input inductor. The power converter is preferably designed such that the wiring inductance from the output of the input driver to the input electrode of the piezoelectric transformer is smaller than 500 μH, preferably smaller than 100 μH, even more preferably smaller than 10 μH.

[0013] The electrical characteristics of the feedback loop are preferably configured to set the excitation frequency within the ZVS operation range of the piezoelectric transformer. The bandwidth of the ZVS operation range is typically narrow and located slightly above a fundamental resonance frequency of the piezoelectric transformer depending on specific characteristics of a design of the piezoelectric transformer. The bandwidth of the ZVS operation range of piezoelectric transformers may vary widely between different transformer topologies, modes of operation and physical dimensions. In some embodiments, the piezoelectric transformer is designed or configured with a bandwidth of the ZVS operation which lies between 1 % and 5% of a fundamental or primary resonance frequency of the piezoelectric transformer. In a number of useful embodiments, the electrical characteristics of the feedback loop are configured to set the excitation frequency to a frequency between 75 kHz and 10 MHz such as between 200 kHz and 20 MHz.

[0014] The phase-shift around the feedback loop must be an integer multiple of 360 degrees where the distribution of individual phase shifts between components and circuits of the feedback loop can be effected in numerous ways. The self-oscillation provided by the feedback loop ensures that the excitation frequency automatically tracks changing characteristics of the piezoelectric transformer and electronic circuitry of the input side of the power converter. This effect is particularly pronounced according to a preferred embodiment of the power converter wherein the feedback loop comprises a phase shifting circuit for example a frequency selective filter such as a high-pass, band-pass or a low-pass filter. According to this preferred embodiment, a slope or derivative of a phase response of a transfer function of the piezoelectric transformer is steeper than a slope or derivative of a phase response of the high-pass, band-pass or the low-pass filter within the ZVS operation range of the piezoelectric transformer. The high-pass, band-pass or the low-pass filter is preferably a low order filter such as a first or second order filter which exhibits a relative gentle slope of the phase response. In this way, the slope of the phase response of the piezoelectric transformer becomes much steeper than the slope of the phase response of the frequency selective filter. The predetermined excitation frequency will as a consequence become significantly more sensitive to changes to the frequency response characteristic of the piezoelectric transformer than to changes of the response of the frequency selective filter such that the self-oscillating feedback loop automatically maintains the predetermined excitation frequency at an optimum frequency or within an optimum frequency band.

[0015] According to one embodiment, the feedback loop comprises a cascade of a phase shifter and a comparator. The phase shifter is coupled for receipt of the feedback signal and configured to apply a predetermined phase shift to the feedback signal to provide a phase shifted feedback signal. The comparator is coupled for receipt of the phase shifted feedback signal to generate a square-wave feedback signal at a comparator output. The square-wave feedback signal is coupled to an input of the input driver so as to close the feedback loop.

[0016] The respective phase-shifts induced to the feedback signal by the phase shifter and the comparator may be adjusted in various ways to achieve a certain total phase shift complementing other signal phase shifts around the self-oscillating feedback loop. In one embodiment, the comparator comprises an inverting zero-crossing detector to provide square-wave feedback signal indicating zero-crossings of the phase-shifted feedback signal. In this manner, the inversion introduces a phase shift of at least 180 degrees in the self-oscillating feedback loop. The phase shifter may comprise a frequency selective filter and/or a time delay. The frequency selective filter may comprise a high-pass, band-pass or a low-pass filter with an appropriately tailored phase response. In the alternative, or in addition, the phase shifter may comprise an all-pass type of filter inducing a predetermined phase shift to the self-oscillating feedback loop without any frequency response filtration of the feedback signal.

[0017] The feedback signal to the feedback loop, which is operatively coupled between the output voltage of the piezoelectric transformer and the input driver, may be derived in numerous ways from the output voltage of the piezoelectric transformer. According to one embodiment, the feedback signal of the feedback loop is derived from the transformer output signal at the output electrode of the piezoelectric transformer. In this embodiment the feedback signal is derived directly from the existing output electrode(s) which also supplies power to a DC or AC output voltage node or terminal of the power converter. This embodiment is simple to implement because it uses existing signals and electrodes of the power convertor to provide the feedback signal. However, the feedback signal will be galvanically coupled to the output section of the piezoelectric transformer unless expensive and bulky precautions are taken such as the insertion of isolating optical couplers in the feedback loop. The output section of the piezoelectric transformer may have a very high voltage level for example at mains voltage (110 V to 230 V) or even higher voltages above 1 kV.

[0018] In an advantageous embodiment, the potential safety and regulatory problems caused by the galvanic coupling between the output section and output electrode and the input driver or input side by the feedback signal are avoided by adding a separate feedback output electrode to the output section or sections of the piezoelectric transformer. According to this embodiment, the feedback signal of the feedback loop is derived from a feedback output signal at the feedback output electrode arranged in one or more separate layer(s) of the output section of the piezoelectric transformer to galvanically isolate the feedback output electrode from the output electrode by the electrically insulating piezoceramic material of the transformer. The piezoelectric transformer may generally be configured such that a voltage gain, at the excitation frequency, from the input electrode to the output electrode is larger, substantially equal to, or smaller than a voltage gain from the input electrode to the feedback output electrode. In one embodiment, the voltage gain from the input electrode to the output electrode is between 2 and 50 times larger than the voltage gain from the input electrode to the feedback output electrode. This embodiment is particularly helpful if the output section of the piezoelectric transformer is at a very high voltage level such as at the mains voltage (110 V to 230 V) or higher as mentioned above. The level of the feedback output signal can be stepped down to a manageable level for example between 5 and 10 V such that galvanic isolation and a voltage level that is compatible with a voltage range of the electronic circuitry of the feedback loop is simultaneously provided. According to another embodiment, the voltage gain from the input electrode to the output electrode is between 2 and 50 times smaller than the voltage gain from the input electrode to the feedback output electrode. This embodiment is particularly helpful if the output section of the piezoelectric transformer operates at a relatively low voltage level such as CPU power supplies (e.g. 0.2 V to 5V DC). The level of the feedback output signal can then only be stepped down to a manageable level for example between 5 and 10 V such that galvanic isolation and a voltage level that is compatible with a voltage range of the electronic circuitry of the feedback loop is simultaneously provided.

[0019] In many applications, the feedback output electrode will not be required to deliver any significant power in comparison to the required load power at/from the output electrode. It may therefore be advantageous to design or construct the piezoelectric transformer such a volume of the separate layer of the output section enclosing the feedback output electrode is small-

er than a volume of layers of the output section enclosing the output electrodes, as the power output of an output electrode is proportional to the associated layer volume.

[0020] The skilled person will understand that separate feedback output electrode can be highly useful for galvanic isolation, and other purposes, in piezoelectric power converters which comprise the ordinary series or parallel inductor coupled between the input driver and the input electrode.

[0021] The feedback signal to the feedback loop can also be derived in an indirect manner from the input side of the piezoelectric power converter according to another preferred embodiment of the invention. Due to the lack of the ordinary series or parallel inductor between the input driver and the input electrode, the transformer resonance current cannot be directly monitored or detected at the input side of the power converter. However, the transformer resonance current can be estimated or derived from the input drive signal and a transformer input current. In this embodiment, the feedback signal of the feedback loop is derived by a transformer resonance current estimator from a combination of the input drive signal and the transformer input current running in the primary section of the piezoelectric transformer. This methodology may be applied to build or estimate a continuous transformer resonance current signal. This is preferably accomplished by differentiating the input drive voltage signal before adding/subtracting this signal from the transformer input current signal since the slope of rising and falling edges of the input drive signal indicates the transformer resonance current during time intervals of the input drive signal where the input driver is off. Consequently, the resonance current estimator preferably comprises:

- a first order differentiator coupled to the input drive signal to derive a first order derivative signal of the input drive signal,
- a current sensor, coupled in series with the primary section of the piezoelectric transformer, to supply a sensor signal representative of the transformer input current; and
- a subtractor configured to generate the feedback signal based on a difference between the first order derivative signal and the sensor signal.

[0022] The input current sensor may comprise a resistance arranged in-between a ground connection of the input driver and a ground connection of the piezoelectric transformer to supply a sensor voltage representative of the transformer input current. The first order differentiator may comprise a first order high-pass filter having an input coupled to the input drive signal and

an output supplying the first order derivative signal. A high-pass corner frequency of the first order high-pass filter is preferably larger than a fundamental resonance frequency of the piezoelectric transformer such as at least two times larger or preferably more than 10 times larger. In this manner, it is ensured that the high-pass corner frequency of the first order high-pass filter lies above the excitation frequency because the latter frequency typically is situated proximately to the fundamental resonance frequency of the piezoelectric transformer where the ZVS operation range is located, ensuring that the high-pass filter operates as a true differentiator at the excitation frequency. The subtractor may be implemented in various ways. One embodiment of the subtractor comprises a differential amplifier having a first differential input coupled to the first order derivative signal and the second differential input coupled to the sensor signal. The differential amplifier preferably comprises an operational amplifier either as a separate standard component or as sub-circuit of an ASIC integrating other types of electronic circuitry of the present piezoelectric power converter thereon.

[0023] According to another preferred embodiment of the invention, the piezoelectric power converter comprises a bi-directional switching circuit for reverse power transfer from the load at the output or secondary side of the power converter back to the input side. According to this embodiment, the piezoelectric power converter comprises:

- a bi-directional switching circuit coupled between the output electrode and an output voltage of the power converter,
- a controller adapted to control first and second states of the bi-directional switching circuit based on the input drive signal or the transformer output voltage such that:
- in a first state, forward current is conducted from the output electrode to the output voltage through the bi-directional switching circuit during a first period of a cycle time of the transformer output signal to charge the output voltage,
- in a second state, reverse current is conducted from the output voltage to the output electrode through the bi-directional switching circuit during a second period of the cycle time of the transformer output signal to discharge the output voltage and return power to the primary section of the piezoelectric transformer.

[0024] The presence of the second state wherein reverse current is conducted from the output voltage through the bi-directional switching circuit to the output electrode allows effective output voltage regulation without sacrificing efficiency of the piezoelectric based power converter.

This is because the reverse power is returned to the primary section or side of the piezoelectric transformer. The transmission of reverse current during the second period of the cycle time exploits he inherent bi-directional power transfer property of piezoelectric transformers such that power is transferred in opposite direction to the ordinary one, i.e. forward, power flow in the power converter. Surplus power at the output voltage is transmitted back to the input power source such as a DC supply voltage supplying power to the input driver. According to a preferred embodiment of the invention, the controller is in the second state further configured to control the switching circuit such that both forward current and reverse current is conducted during a single cycle of the transformer output signal. In this embodiment the forward current is conducted during the first period of the cycle time and reverse current is conducted during the second period of the same cycle of the transformer output signal. The second period may have a length corresponding to about one-half or less than the cycle time cycle time of the transformer output signal. The skilled person will appreciate that the degree of charge or discharge of the output voltage may be controlled in a step-wise or substantially continuous manner by a corresponding control of the relative length between the first and second periods of the same cycle of the transformer output signal. In this manner, the controller may provide effective output voltage control through adjustment of the length of the second period of the cycle time. Accordingly, by appropriately balancing the length of the first period of the cycle time relative to the second period of the same cycle, the bi-directional piezoelectric power converter may be adapted to transfer net power to the output voltage or to a load coupled thereto, transfer substantially zero power to the output voltage or transfer a negative power to the output voltage. The skilled person will understand that if the controller sets the length of the second period of the cycle time to zero, the bi-directional piezoelectric power converter conveniently transits from the second state to the first state wherein the bi-directional switching circuit conducts solely forward current so as to charge the output voltage during the first periods of the cycle times. This leads to an increasing level of output voltage e.g. the output voltage becomes more positive or more negative depending on the polarity configuration of the bi-directional switching circuit. In general, the controller may be adapted to terminate the second period of the cycle time, i.e. terminating the reverse conduction of current through the switching circuit, synchronously or asynchronously to the input drive signal or the transformer output signal. The controller preferably comprises an adjustable time delay circuit providing an adjustable duration of the second period

of the cycle time of the transformer output signal such that the amount of reverse power can be controlled. The controller is preferably configured to derive a synchronous state control signal from the input drive signal and apply the synchronous state control signal through the adjustable time delay circuit to a switch control terminal of the second controllable semiconductor switch and/or a switch control terminal of the first controllable semiconductor switch to control respective states of the first and second controllable semiconductor switches. In this manner, the switching circuit is responsive to the synchronous state control signal indicating the termination of the second period of the cycle time. The skilled person will understand that the synchronous state control signal may be derived directly or indirectly from the input drive signal. Indirectly if the synchronous state control signal is derived from another signal in the power converter that is synchronous to the input drive signal such as the transformer output signal. In one such embodiment, the synchronous state control signal is derived from a zero-crossing detector embedded in a self-oscillating feedback loop enclosing input section of the piezoelectric transformer.

[0025] The operation of the power converter during the second state of the bi-directional switching circuit where reverse power is transmitted can be improved in accordance with one embodiment of the invention. When reverse power is transmitted through the power converter the excitation frequency set by the feedback loop decreases. This leads to an increase of the transformer resonance current level and may be counteracted by adjustment of a time delay in the self-oscillating feedback loop. In one embodiment, the feedback loop comprises an adjustable time delay coupled in cascade with the phase shifter and the comparator to adjust the excitation frequency of the feedback loop. This embodiment may further comprise a current detector configured to determine the level of the transformer resonance current and a current limiter adapted to adjust the time delay of the adjustable time delay circuit to limit the transformer resonance current. In this manner an optimal operating point or excitation frequency of the feedback loop can be maintained during both forward power transmission and reverse power transmission of the bi-directional piezoelectric power converter.

[0026] The feedback loop may in certain situations be unable to induce a reliable start of the self-oscillation action due to amongst other factors the non-linear behaviour of the input driver which makes the latter insensitive to low level fluctuations of its input voltage. This may for example the situation if a bandwidth of the phase shifter is so low that noise signal components within the feedback loop are small. Consequently, an advantageous embodiment of the inven-

tion comprises a start-up circuit configured to inject a transient signal into the feedback loop at power-up of the power converter to initiate oscillation at the excitation frequency in the feedback loop. The skilled person will understand that the start-up circuit could be configured in a numerous ways to generate the desired transient signal. The transient signal could comprise a one or more signal pulses of predetermined waveform shape and duration. In another embodiment, the start-up circuit comprises an oscillator coupled into the feedback loop. The oscillator may be configured to generate an essentially continuous transient signal that is removed from the feedback loop by a suitable mechanism once self-oscillation has started. This may for example be controlled by an output impedance of the oscillator which is so large that the continuous transient signal is suppressed or eliminated once self-oscillation is initiated.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] Preferred embodiments of the invention will be described in more detail in connection with the appended drawings, in which:

[0028] Fig. 1 is a schematic block diagram of a piezoelectric power converter comprising a self-oscillating loop in accordance with a first embodiment of the invention,

[0029] Fig. 2a) is an electrical equivalent circuit of a piezoelectric transformer coupled to an input driver of a piezoelectric power converter in accordance with a first embodiment of the invention,

[0030] Fig. 2b) shown input drive voltage and input current waveforms of the piezoelectric transformer in accordance with the first embodiment of the invention,

[0031] Fig. 3 a detailed schematic block diagram of a transformer resonance current estimator coupled to an input section of a piezoelectric transformer of the piezoelectric power converter in accordance with the first embodiment of the invention,

[0032] Fig. 4 is a schematic block diagram of a piezoelectric power converter comprising a self-oscillating loop in accordance with a second embodiment of the invention,

[0033] Fig. 5 is a detailed schematic block diagram of a transformer output voltage detection circuit coupled to an output section of the piezoelectric transformer of the piezoelectric power converter in accordance with the second embodiment of the invention,

[0034] Fig. 6 is a simplified schematic block diagram of a piezoelectric power converter comprising a self-oscillating loop based on a separate feedback electrode in accordance with a third embodiment of the invention,

[0035] Fig. 7 is a simplified electrical equivalent circuit of the piezoelectric transformer of the piezoelectric power converter in accordance with the third embodiment of the invention; and

[0036] Fig. 8 is a schematic block diagram of a piezoelectric power converter comprising a self-oscillating loop and a bi-directional switching circuit for reverse power transfer in accordance with a fourth embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0037] The below appended detailed description of embodiments of the present invention comprises various types of self-oscillating loops for DC/DC voltage step-up or voltage step-down power conversion. However, the skilled person will understand that the below described embodiments are highly useful for other types of power converting applications such as AC/AC, AC/DC, DC/AC and DC/DC conversion, in particular conversion requiring high power conversion efficiency and compact dimensions by ZVS operation of the input driver without an external inductor at the input electrode.

[0038] Fig. 1 shows a schematic block diagram of a piezoelectric power converter 100 in accordance with a first embodiment of the invention. The bi-directional piezoelectric power converter 100 comprises a piezoelectric transformer, PT, 104. The piezoelectric transformer, PT, 104 has a first input electrode 105 electrically coupled to an input or primary section of the piezoelectric transformer 104, coupled to the input driver 103 of the piezoelectric power converter and a second input electrode connected to ground, GND. A first output electrode 107a and second output electrode 107b of the piezoelectric transformer 104 are electrically coupled to secondary or output section of the piezoelectric transformer 104 to provide a differential transformer output voltage or signal to a rectification circuit 108. The rectification circuit 108 may comprise a half or full wave rectifier and an output capacitor to provide smoothed DC voltage at the output node or terminal V_{OUT}.

[0039] The piezoelectric power converter 100 additionally comprises an input driver 103 electrically coupled directly to the input electrode 105 without any intervening inductor so as to apply an input drive signal to the input or primary section of the transformer 104. A driver con-

trol circuit 102 generates appropriately timed gate control signals for NMOS transistors M_2 and M_1 of the input driver 103. The input drive signal has a predetermined excitation frequency determined by parameters of a self-oscillating feedback loop operatively coupled between the output voltage of the piezoelectric transformer at output electrodes 107 and 107b and the input driver 103. In the present embodiment, the transformer output voltage is detected indirectly by estimating the transformer resonance current from a combination of the input drive signal supplied at input terminal 105 and a transformer input current running in the primary section of the piezoelectric transformer as explained in detail below in connection with Figs. 2 and 3 showing schematic and signal waveforms of a resonance current detector 118 performing this task. Electrical characteristics of the self-oscillating feedback are configured to set the excitation frequency of the self-oscillation loop within a ZVS operation range of the piezoelectric transformer. The self-oscillating feedback loop comprises a feedback leg 114 coupling a resonance current indicative signal I_{SENSE} which is proportional of the transformer output voltage back to the input driver through a cascade of low-pass filter 120 and a zero-crossing detector 122 such that the loop is closed around the input section of the transformer. The phase-shift around the self-oscillation loop feedback loop or simply feedback loop must be an integer multiple of 360 degree and the respective phase-shifts induced by the resonance current detector 118, the low-pass filter 120 and a zero-crossing detector 122 adjusted in an appropriate manner to achieve this goal.

[0040] It is furthermore desired to maintain a phase shift of approximately 55 degrees between the input drive signal and the transformer resonance current as set by the resonance current detector 118 because this phase difference ensures that the excitation frequency is located within a narrow frequency band above the fundamental resonance frequency of the piezoelectric transformer 104 where native ZVS operation is enabled. Within this narrow frequency band of ZVS operation, the piezoelectric transformer 104 exhibits the above-described ZVS factor larger than 100 % such as larger than 120 % and appears to possess inductive input impedance as seen from the output of the input driver 103. To reach the desired phase shift around the feedback loop on the integer multiple of 360 degrees, the zero-crossing detector 122 may be inverting to induce a further 180 degrees phase shift and a combined time delay of the input driver 103 and the driver control circuit 102 may amount to about 40 degrees of phase shift at the predetermined excitation frequency. These phase shifts add up to about 275 degrees such that the

electrical characteristics of the low-pass filter 120 are designed to induce a phase shift of 75 degrees at the predetermined excitation frequency. This can be achieved by selecting an appropriate cut-off frequency and order of the low-pass filter 120. The skilled person will understand that many other distributions of phase shifts between the circuits of the feedback leg 114 are possible. In one embodiment, the resonance current detector 118 is inverting to add another 180 degrees of phase shift. The low-pass filter 120 could be replaced by a band-pass filter or a pure time delay designed to provide the desired amount of phase shift.

[0041] At the secondary side of the PT 104, a rectifier or rectification circuit 108 is electrically coupled between a differential transformer output signal generated at the output electrodes 107a and 107b coupled to respective output sections of the PT 104. The rectification circuit 108 may be configured to provide half-wave or full-wave rectification of the transformer output signal supplied between the positive output electrode 107a and the negative, or opposite phase, output electrode 107b. The rectification circuit 108 preferably comprise a rectifier capacitor of appropriate capacitance (not shown) configured to generate a positive or negative DC output voltage V_{OUT} across the load resistance R_{LOAD} of the power converter 100. The load may of course comprise a capacitive and/or inductive component in addition to the depicted load resistor R_{LOAD}. During operation of the piezoelectric power converter 100 the level of the DC output voltage V_{OUT} is adjusted or controlled by a control mechanism or loop. The control loop comprises a DC output voltage detection or monitoring circuit 109 which supplies a signal to the output voltage control circuit 110 indicating an instantaneous level of the DC output voltage. A charge control circuit ΔQ compares the measured instantaneous level of the DC output voltage with a reference voltage V_{ref} which for example represents a desired or target DC output voltage of the power converter at V_{OUT}. The charge control circuit determines whether the level of the current DC output voltage is to increase or decrease based on the result of the comparison. The output voltage control circuit 110 generates an Active/Shut-down (A/S) control signal for the gate driver 101 such that the gate driver is disabled if the instantaneous level of the DC output voltage is larger than the reference voltage V_{ref}. If the instantaneous level of the DC output voltage is smaller than the reference voltage V_{ref} the gate driver is enabled and in this burst-mode manner power or energy is transferred to the converter output voltage through the rectification circuit 108.

[0042] Fig. 2a) is an electrical equivalent circuit of the piezoelectric transformer 104 coupled directly to the input driver 103 and to the rectification circuit 108 of the piezoelectric power converter 100 depicted on Fig. 1. As previously mentioned, the transformer output voltage across the first and second output electrodes 107a and 107b is detected indirectly by estimating the transformer resonance current I_L from a combination of the input drive signal V_p at input terminal 105 and the transformer input current I_{in} running through the primary section of the piezoelectric transformer 104. Since the input driver 103 is directly coupled to the input section of the piezoelectric transformer 104 without any external series or parallel inductor, the transformer resonance current cannot be measured through the external series or parallel inductor. The present embodiment of the invention utilizes a resonance current estimator instead to determine or estimate the transformer resonance current indirectly and derive a continuous resonance current signal I_{SENSE} which is supplied to the feedback loop to provide a feedback signal representative of the transformer resonance current. The estimated transformer resonance current is accordingly also representative of the transformer output voltage at the first and second output electrodes 107a and 107b. The resonance current estimator comprises a first order differentiator comprising series coupled capacitor C1 and resistor R1 coupled to the input drive signal V_p. The mid-point voltage V_{diff} at the coupling node between the series coupled capacitor C1 and resistor R1 supplies a first order derivative signal of the input drive signal V_p because a high-pass corner frequency of the first order differentiator is much larger than the fundamental resonance frequency of the piezoelectric transformer 104 such as at least two times larger e.g. 10 times larger.

[0043] The transformer input current I_{in} is detected in the resonance current detector 118 depicted in a detailed schematic diagram on Fig. 3 by a small series resistor R_S acting as a current sensor coupled in series with the primary section of the piezoelectric transformer 104. The series resistor R_S is coupled in a ground line or wire between the ground connection of the primary side of the piezoelectric transformer 104 and the ground connection of the first order differentiator. Hence, a voltage across the series resistor R_S represents, i.e. is proportional to, the transformer input current I_{in}.

[0044] The first order derivative signal V_{diff} and the transformer input I_{in} current signal are supplied to respective inputs of a differential amplifier of the resonance current detector 118. The differential amplifier comprises an operational amplifier 116 and gain setting resistors R2,

R3, R4 and R5 configured such that the gain from each of the inputs can be separately adjusted. The gain from V_{diff} to the resonance current signal I_{SENSE} is adjustable by R4 and R3 and the gain from the transformer input I_{in} current signal is adjustable by R5 and R2 such that convenient scaling between V_{diff} and I_{in} is provided. Furthermore the scaling can also be done trough the selection of R_S, R1 and C1. The function of the resonance current detector 118 is explained by reference to the measured input drive voltage waveform 161 at the lower graph 160 and the transformer input current waveform 151 depicted on the upper graph 150 of Fig. 2 b). The transformer input current waveform 151 is represented by the measured voltage across the series resistor R_S as explained above. The transformer input current I_{in} and the voltage across the series resistor R_S are zero during time periods where the input driver is off, i.e. its dead-time intervals indicated below the graph 160 as t2 and t4, because the output of the input driver at node V_P is charged by the resonance current of the piezoelectric transformer itself. However, the true transformer resonance current I_L is unavailable outside the physical structure of the piezoelectric transformer 104 because a large portion of the resonance current is conducted through the transformer input capacitance represented by parallel capacitor Cd1 of the equivalent diagram of Fig. 2a). However, by differentiating the up and down going transitions of the measured input drive voltage waveform 161 during the dead-time intervals t2 and t4, a scaled representation of the true transformer resonance current I_L is determined. Since the first order derivative signal V_{diff} of the measured input drive voltage waveform 161 is approximately zero (no slope) during on-periods of the input driver 103 as indicated by time periods t1 and t3 the first order derivative does not make any significant contribution to the resonance current signal I_{SENSE} during the latter time periods. During time periods t1 and t3 where the input driver 103 is active and conducting, the transformer resonance current flows through series resistor R_S and therefore generates a proportional sensed voltage which contributes to the resonance current signal $I_{SENSE.}$ This is indicated by the approximate sine shape of the transformer input current waveform 151 during time periods t1 and t3. Hence, the resonance current detector 118 generates a continuous loop feedback signal in form of the resonance current signal I_{SENSE} by combining the first order derivative signal V_{diff} 153 derived from the input voltage V_P 161 and the transformer input current I_{in} measured across the sense/series resistor R_S 151.

[0045] Since the resonance current signal I_{SENSE} for the feedback loop is generated from the input section of the piezoelectric transformer 104, the feedback signal is galvanic insulated from

the output section of the piezoelectric transformer 104. Hence, if the output section supplies high voltage signals because of the amplification characteristics of the piezoelectric transformer 104, the primary section is isolated from the high voltages enhancing safety and helps the power converter in complying with high voltage regulatory requirements.

[0046] Fig. 4 is a schematic block diagram of a piezoelectric power converter 400 comprising a self-oscillating loop in accordance with a second embodiment of the invention. The piezoelectric power converter 400 shares a large number of electrical characteristics and features with the above described first embodiment of the power converter and corresponding features have accordingly been provided with corresponding reference numerals to ease comparison. However, the way the feedback signal for the feedback leg 414 is derived from the piezoelectric transformer 404 differs in the present embodiment compared to the first embodiment. In the present embodiment, a differential transformer output voltage or signal for the feedback loop is derived from a first output electrode 407a and second output electrode 407b of the piezoelectric transformer 404. The first and second output electrodes 407a, 407b are in addition electrically coupled to respective secondary or output sections of the piezoelectric transformer 404 to provide the differential transformer output voltage to a rectification circuit 408. The rectification circuit 408 may comprise a half or full wave rectifier and an output capacitor to provide smoothed DC voltage at the output node or terminal V_{OUT}. An output voltage detection circuit 418 receives the differential transformer output voltage and generates a single-ended or differential sense signal, V_{SENS} which is transmitted to a low-pass filter 420 with similar characteristics to the low-pass filter of the first embodiment discussed above. Since, a potentially high transformer output voltage is fed back to the input section or primary side of the converter 400 there is not any galvanic isolation between the output side/voltage and the input side. However, in one preferred embodiment, the output voltage detection circuit 418 comprises a pair of small series capacitors that at least breaks any DC current path between the output side/voltage and the input side as described below in connection with Fig. 5. The skilled person will notice that the output voltage detection circuit 418 can be made less complex in the present embodiment compared to the resonance current detector 118 coupled to the primary transformer side of the piezoelectric transformer 104 in the first embodiment because a continuous transformer output voltage signal representing the transformer resonance current is directly available for the self-oscillating feedback loop in the present embodiment of the converter.

[0047] Fig. 5 is a detailed schematic block diagram of the transformer output voltage detection circuit 418 coupled to the output section of the piezoelectric transformer 404 (PT) of the piezoelectric power converter schematically depicted on Fig. 4. The rectifier 408 and the input driver 403 are also schematically indicated to ease comparison. The transformer output voltage detection circuit 418 comprises a first pF sized series capacitor C1 coupled in series with the first output electrode 407a (S1) and a second pF sized series capacitor C1 coupled in series with the second output electrode 407b (S2). A network of resistors R3 and R1 are configured to couple one phase of the transformer output signal from the series capacitor C1 to a matched pair of current mirror coupled transistors Q1. A corresponding coupling arrangement is connected to the other series capacitor C2. In effect, the single-ended feedback signal V_{SENS} is derived from the differential transformer output voltage. The feedback signal V_{SENS} is essentially a square wave signal in phase with the differential transformer output voltage. This feedback signal V_{SENS} is subsequently applied to the feedback leg 414 and phased shifted trough the low-pass filter 420 with similar characteristics to the low-pass filter of the first embodiment discussed above.

[0048] Fig. 6 is a simplified schematic block diagram of a piezoelectric power converter 600 comprising a self-oscillating loop based on a separate feedback output electrode 607c for supplying a feedback output signal to the self-oscillating loop in accordance with a third embodiment of the invention. The piezoelectric power converter 600 shares a large number of electrical characteristics and features with the above described second embodiment of the power converter 400 and corresponding features have accordingly been provided with corresponding reference numerals to ease comparison. However, the way the feedback signal for the feedback leg 614 is derived from the piezoelectric transformer 604 differs in the present embodiment compared to the second embodiment. In the present embodiment, a separate feedback output electrode 607c supplies a feedback output signal Fb representative of the differential transformer output voltage across the first and second output electrodes 607a, 607b to the output voltage detection circuit 618. The first and second output electrodes 607a, 607b electrically coupled to respective secondary or output sections of the piezoelectric transformer 604 and the differential transformer output voltage is transmitted to a rectification circuit 608 in a manner similar to the second embodiment described above. The rectification circuit 608 may accordingly comprise a half or full

wave rectifier coupled to an output capacitor(s) to provide a smoothed DC voltage at the output node or terminal V_{OUT}.

[0049] In the present embodiment, the piezoelectric transformer 604 is fabricated with the separate feedback output electrode 607c arranged or embedded in a separate layer of the output or secondary section of the piezoelectric transformer 604. The feedback signal supplied through the feedback path at the separate output electrode 607c is thereby galvanically isolated from the output sections or sides, output voltages such as V_{OUT} and electronic circuitry of the secondary side of the piezoelectric power converter 600. The skilled person will understand that the piezoelectric transformer 604 may comprise several separate feedback electrodes for example a dedicated feedback electrode in each of the output sections of the piezoelectric transformer 604 such that the illustrated feedback output signal Fb may comprise a differential feedback signal. A voltage gain, at the excitation frequency, from the input electrode 605 to the differential transformer signal across the first and second output electrodes 607a, 607b may be essentially equal to, larger than, or smaller than a voltage gain from the input electrode 605 to the feedback output electrode(s) 607c for example between 2 and 50 times larger or between 2 and 50 times smaller. In step up voltage conversion applications of the present piezoelectric power converter 600, a smaller voltage gain to the feedback output electrode(s) 607c may be preferable such that galvanic isolation and an appropriate voltage level for electronic components of the output voltage detector 618 simultaneously are achieved. Even if the voltage gain, at the excitation frequency, from the input electrode 605 to the differential transformer signal across the first and second output electrodes 607a, 607b is essentially equal to the voltage gain from the input electrode 605 to the feedback output electrode(s) 607c, the piezoelectric power converter 600 benefits from the galvanic isolation between the input side and output side circuitry.

[0050] According to one such embodiment, a volume of the separate layer of the output section which encloses the feedback output electrode 607c is smaller than a volume of layers of the output section(s) enclosing the output electrodes 607a, 607b. This can be achieved by embedding the feedback output electrodes i to a small portion of the secondary PT section, as it should only occupy a very small part of the output PT section (or input PT section if feedback is taken from the primary side) and will therefore not distort or degrade performance of the output section significantly. Depending on the specific piezoelectric transformer design and structure, embedding the feedback output electrode can be relatively straight-forward to implement. Embed-

ding can also be very convenient if the voltage level of the output section is appropriate for electronic components of the output voltage detector 618, as the feedback output electrode 607c will possess a similar voltage level, if small parts of the existing electrodes in the output section are used, so the feedback output electrodes have the same layer thickness.

[0051] The feedback output electrode 607c can also be implemented as a separate section of the piezoelectric transformer 604 if this is more convenient, practical or the transformer design does not allow embedding the feedback output electrode. In any case, it is preferred that the separate feedback section of the piezoelectric transformer occupies a very small part of the entire piezoelectric transformer 604 structure without distorting or degrading the transformer performance as described above. Depending on the piezoelectric transformer design and structure, a separate output section may from a practical perspective be simpler to implement than embedding. The separate output section may also be more convenient for piezoelectric transformer designs where none of the output or secondary transformer sections has an appropriate voltage level for the electronic components of the output voltage detector 618.

[0052] Fig. 7 illustrates a simplified electrical equivalent diagram inside dotted box 604 of the piezoelectric transformer 604 of the piezoelectric power converter 600 in accordance with the third embodiment of the invention. The simplified electrical equivalent diagram comprises a pair of separate secondary windings where the load is coupled to the upper secondary winding which also provides the positive DC output voltage V_{OUT}. The rectifier has been left out of the diagram for simplicity. The lower secondary winding corresponds to the separate feedback output electrode 607c and provides a feedback output signal V_{FB} to the output voltage detection circuit 618. As illustrated on the drawing, the lower secondary winding is galvanically isolated from the upper secondary winding and therefore not used to supply power to the load. Hence, the volume of the output section occupied by the separate feedback output electrode 607c can be much smaller than the volume of the output section(s) enclosing the output electrodes 607a, 607b.

[0053] Fig. 8 is a schematic block diagram of a piezoelectric power converter 800 comprising a self-oscillating loop and a bi-directional switching circuit 808 for reverse power transfer in accordance with a fourth embodiment of the invention. The piezoelectric power converter 800 shares a large number of electrical characteristics and features with the above described third embodiment of the power converter 600, in particular a separate feedback output electrode 807c

arranged or embedded in a separate layer of the output or secondary section of the piezoelectric transformer 804. The feedback signal from the feedback output electrode 807c is likewise supplied to the output voltage detection circuit 818 and further through a feedback path of the primary side such that the primary side circuitry becomes galvanic isolated from the secondary side.

[0054] At the secondary side of the PT 804, the bi-directional switching circuit 808 is electrically coupled between a single-ended transformer output signal generated at the output electrode 807 of the PT 804 and a positive DC output voltage V_{OUT} applied across a load capacitor C_{LOAD} of the power converter 800. The load may of course comprise a resistive and/or inductive component in addition to the depicted load capacitance C_{LOAD}. A controller or control circuit is adapted to control forward current conduction from the output electrode 807 to V_{OUT} through the bi-directional switching circuit 808 during a first period of the cycle time of the transformer output signal. The positive DC output voltage V_{OUT} is accordingly charged during the first period of the cycle time. This transformer output signal, oscillating at the excitation frequency set by the self-oscillating feedback loop around the feedback electrode 807c, is applied to a midpoint node between series coupled NMOS transistors M_4 and M_3 of the bi-directional switching circuit 808. The output section of the PT 804, oscillating at the excitation frequency, behaves largely as a current source injecting AC current into the midpoint node between series coupled M_4 and M_3 to generate the transformer output signal or voltage. Furthermore, the controller is adapted to control a second period of the cycle time of the transformer output signal wherein reverse current is conducted through the bi-directional switching circuit 808 to the output electrode 807 of the PT 804 such that V_{OUT} is discharged during the second period of the cycle time. During the second period of the cycle time power is returned to the primary section of the piezoelectric transformer through the output electrode 807 of the PT.

The skilled person will appreciate that M_3 and M_4 function as respective controllable semiconductor switches each exhibiting low resistance between an inlet and an outlet node (i.e. drain and source terminals) in the on-state and very large resistance in the off-state or non-conducting state. The on-resistance of each of M_3 and M_4 in its on-state/conducting state may vary considerably according to requirements of a particular application, in particular the voltage level at the DC output voltage V_{OUT} or load impedance. In the present high-voltage embodiment of the invention, each of the M_3 and M_4 is preferably selected such that its on-resistance lies between 50

and 1000 ohm such as between 250 and 500 ohm. The positive DC supply voltage V_{DD} may vary widely in accordance with the requirements of a particular application. In the present embodiment of the invention, the positive DC supply voltage V_{DD} is preferably selected to a voltage between 20 and 40 volt such as about 24 volt.

[0055] The bi-directional switching circuit 808 comprises a high-side semiconductor diode D_4 arranged or coupled across drain and source terminals of M_4 so as to conduct the forward current to the DC output voltage V_{OUT} in a first state of the bi-directional switching circuit 808. A low-side semiconductor diode D_3 is in a similar manner coupled across drain and source terminals of M_3 so as to conduct the reverse current through the output electrode 807 and output section of the PT 804 during at least a portion of the first state. In the first state, the forward current is conducted from the output electrode 807 of the PT 804 through the bi-directional switching circuit 808 to the DC output voltage V_{OUT} during a first period of a cycle time of the transformer output signal to charge the output voltage. This is accomplished by switching the high-side NMOS transistor M_4 to its on-state or conducting state by a self-powered high-side driver 806 which forms part of the controller. The self-powered high-side driver 806 or self-powered driver 806 is coupled between the control or gate terminal of M_4 and the output electrode 807 which supplies the transformer output signal. The timing of the state switching of M_4 is determined by the detection of forward current in D_4 by a current sensor (not shown) contained in the self-powered driver 806. This current sensor is preferably arranged in series with the high-side semiconductor diode D_4. In response to detection of forward current in D_4 the self-powered driver 806 switches M_4 to its on-state which effectively clamps D_4 such that a majority of the forward current flowing through the parallel connection of M_4 and D_4 to the DC output voltage V_{OUT} in reality flows through M_4. On the other hand, during a negative half-cycle of the transformer output signal in the first state of the bi-directional switching circuit 808, D_4 is reverse biased and M_4 switched to its off-state at expiry of a timer period setting of an associated timer circuit (not shown). However, current is now conducted from the negative supply rail, i.e. GND in the present embodiment, to the output electrode 807 of the PT 804 through the parallel connection of M_3 and D_3. Initially, D_3 will start to conduct forward current once it becomes forward biased by the negative transformer output voltage. M_3 is on the other hand, switched to its on-state or conducting state by a low-side driver 821 which forms part of the controller. The low-side driver 821 is coupled to the gate terminal of M_3 and configured to switch M_3 from its off-

state to its on-state and vice versa. However, while the timing of the state switching of M_3 from its off-state to the on-state is determined in a manner similar to M_4, the opposite state switching of M_3 is effected synchronously to input drive signal as explained below. M_3 is switched from the off-state to the on-state by a detection of forward current in D_3 by a current sensor (not shown) contained in the low-side driver 821. This current sensor is arranged in series with the low-side semiconductor diode D_3. At the detection of forward current in D_3 the low-side driver 821 switches M_3 to its on-state which effectively clamps D_3 such that a majority of the forward current flowing through the parallel connection of M_3 and D_3 in reality flows through M_3.

[0056] Consequently, in the first state the bi-directional switching circuit 808 functions as a half-wave rectifier or voltage doubler of the transformer output signal such that forward current is conducted from the output electrode 807 of the PT 804 through the high-side NMOS transistor M_4 and semiconductor diode D_4 to the DC output voltage V_{OUT} to charge V_{OUT}. In the negative half-periods of the transformer output signal, current is circulated around the secondary section of the PT 804 without charging the DC output voltage in the current embodiment which uses the half-wave rectification provided by the present bi-directional switching circuit 808. In comparison to a traditional diode-based half-wave rectifier, the bi-directional switching circuit 808 additionally comprises the NMOS transistors M_4 and M_3 of the bi-directional switching circuit 808 arranged for clamping of the high and low-side semiconductor diodes D_4 and D_3. During a second state and during a third state of the bi-directional switching circuit 808, the NMOS transistors M_3 and M_4 are controlled by the controller such that a flow of reverse power is enabled. Due to the inherent bi-directional transfer property of the PT 804 power applied to the secondary section through the output electrode 807 is transferred to the input section of the PT 804 in effect transferring power in opposite direction to the normal flow of power of the power converter 800.

[0057] In connection with the reverse current conduction during the second period of the cycle time, state switching of M_3 is controlled by the low-side driver 821 coupled to the gate terminal of M_3. The low-side driver 821 is responsive to a synchronous state control signal derived from the input drive signal supplied by an adjustable time delay circuit, control ΔT, of a phase controller 811. The phase controller comprises the adjustable time delay circuit, control ΔT, and a fixed time delay, ΔT circuit. The phase controller 811 receives s zero-crossing detector output signal 819 which switches states synchronously to the input drive signal and the transformer

output signal because this signal is derived from the self-oscillating feedback loop. Since the input drive signal and the transformer output signal oscillate synchronously to each other, the time delay imposed by the phase controller 811 to the zero-crossing detector output signal 819 sets a length or duration of the second period of the cycle time of the transformer output signal. M_3 is allowed to continue conducting current for the duration of the second period of the cycle time until the state transition of the synchronous state control signal turns off M_3 of the low-side driver 821. While the corresponding state switching of the high-side NMOS transistor M_4 from its on-state to its off-state in one embodiment is controlled by the synchronous state control signal albeit phase shifted about 180 degrees, the present embodiment of the invention uses a different turn-off mechanism provided the self-powered high-side driver 806. The self-powering of the high-side driver 806 is configured to terminate a reverse current conducting period of M_4 based on an internally generated state control signal supplied by an internal timer rather than the above-described synchronous state control signal supplied by the adjustable time delay circuit, control ΔT. The self-powered property of the high-side driver 806 is highly advantageous for high-voltage output PT based power converters where the DC output voltage may be above 1 kV. The self-powering property of the high-side driver 806 circumvents the need for raising the zero-crossing detector output signal 819 to a very high voltage level, i.e. matching the level of the DC output voltage, before being supplied to the high-side driver 806 to appropriately control the gate terminal of M_4. The skilled person will recognize that the gate terminal of M_4 must be raised to a level above the level of the DC output voltage signal to switch M_4 to its on-state. The self-powered high-side driver 806 is electrically coupled between the gate terminal of M_4 and the output electrode 807 carrying the transformer output voltage. During operation, the bi-directional piezoelectric power converter 800 comprises two distinct mechanisms for adjusting the level of the DC output voltage V_{OUT}. A first mechanism uses a DC output voltage detection or monitoring circuit 809 which supplies a signal to the output voltage control circuit 810 of the controller indicating the instantaneous level of the DC output voltage. A charge control circuit ΔQ compares the instantaneous level of the DC output voltage with a reference voltage which for example represents a desired or target DC output voltage of the power converter. The charge control circuit determines whether the current DC output voltage is to be increased or decreased based on this comparison and adjusts at least one of: {a modulation of a pulse width modulated input drive signal, a carrier frequency of the pulse width modulated input drive signal, a burst

frequency of a burst modulated input drive signal} in appropriate direction to obtain the desired adjustment of the DC output voltage. A second mechanism for adjusting the level of the DC output voltage V_{OUT} also uses the level signal from the DC output voltage detection circuit 809. In this instance the output voltage control circuit 810 adjusts the duration of the second period of the cycle time of the transformer output signal where M_3 conducts reverse current through the adjustable time delay circuit, control ΔT, of the phase controller 811. The corresponding adjustment of the second period of the cycle time as regards M_4 is preferably made by delaying the triggering time or point of the timer circuit included in the self-contained high-side driver 806. The delay of the triggering time of the timer circuit may be controlled dynamically during operation of the bi-directional power converter 800 by the controller by adjusting a delay of an adjustable time delay circuit, control ΔT, to reach a desired or target duration of the second period of the cycle time of the transformer output signal. The adjustable time delay circuit, control ΔT, allows the controller to adjust the duration of the second period of the cycle time of the transformer output signal wherein reverse current is conducted by the bi-directional switching circuit through the output electrode 807 back to the primary side of the PT 804. By this adjustment of the duration of the second period of the cycle time, the amount of generated reverse power can be effectively controlled allowing for the desired adjustment of the level of the DC output voltage V_{OUT} while conserving power.

[0058] The skilled person will appreciate that the degree of charge or discharge of the V_{OUT} may be controlled in a step-wise or substantially continuous manner by a corresponding control of the duration of the second period of the cycle time such that the level of V_{OUT} may be continuously increased or reduced as desired. The skilled person will understand that if the duration of the second period of the cycle time is set to zero by the controller, the bi-directional piezoelectric power converter 800 may be adapted to exclusively operate in the first state where the switching circuit charges the positive DC output voltage during the first period of cycle times of the transformer output signal. In this state, the NMOS transistors M_3 and M_4 are only conducting during the first period of the cycle time so to actively clamp the low-side and high-side semiconductor diodes D_3 and $D_{4,}$ respectively.

[0059] The self-oscillating feedback loop comprising comprises a resonance current control circuit 812 comprising a peak current detector 826 coupled to a current limiter 828. The resonance current control circuit 812 is configured to adjust a time delay of the adjustable time de-

lay circuit 824 arranged in the feedback leg 814. The resonance current level of the piezoelectric transformer 804 is determined based on the output signal of the output voltage detector 818, or, alternatively, from an output of a low-pass filter 820 coupled to the output voltage detector 818. The output voltage detector 818 may advantageously comprise a simple resistive load applied to the feedback signal from the feedback output electrode 807c. In this situation, the resonance current level of the piezoelectric transformer can be determined in a straightforward manner by the peak current detector 826 from the level of the feedback signal and the known resistance of the resistive load. The low-pass filter 820 may have similar electrical characteristics to the low-pass filter of the first embodiment discussed above. The zero-crossing detector 822 receives a low-pass filtered signal from the low-pass filter 820 and provides an essentially square wave shaped signal indicating zero-crossings of the filtered signal which possesses an approximate sine shaped waveform. The square wave signal is transmitted to an adjustable time delay circuit 824 which introduces a variable phase shift in the self-oscillating feedback loop such that the predetermined excitation frequency can be adjusted. An output signal of the adjustable time delay circuit 824 is coupled to the drive control circuit 802 such as to close the self-oscillating feedback loop around an input driver 803. A resonance current control circuit 812 detects a peak current from the output signal of the output signal of the voltage detector 818 as described above and adjusts a time delay of the adjustable time delay circuit 824 based thereon. This is useful to compensate for an increase of ac resonance current under reverse power transmission through the piezoelectric power converter, e.g. in the second state of the bi-directional switching circuit 808. The ac resonance current in the piezoelectric transformer increases under reverse power transmission and this condition is detected by the peak current detector 826 of the resonance current control circuit 812. The effect is compensated by limiting the ac resonance current by the current limiter 828 which makes an appropriate adjustment of the time delay in the adjustable time delay circuit 824 such that an optimal operation point of the self-oscillating feedback loop can be maintained during both forward power transmission and reverse power transmission of the bi-directional piezoelectric power converter 800. In the present embodiment of the invention where the input driver 803 is coupled directly to the input electrode 805 without any series or parallel inductor, the piezoelectric transformer 104 preferably possess a ZVS factor larger than 100 % such as larger than 120 %. In this manner ZVS operation of the input driver 103 is enabled both in a first state and a second state of a bi-directional switching circuit

808. The ZVS operation of the input driver 103 improves the power conversion efficiency of the bi-directional piezoelectric power converter 800. The predetermined excitation frequency is preferably selected in the manner already discussed above in connection with the first embodiment of the invention. The use of the self-oscillating feedback loop has considerable advantages because, the predetermined excitation frequency automatically tracks changing characteristics of the piezoelectric transformer 804 and electronic circuitry of the input side of the power converter like the drive control circuit 802. These characteristics will typically change across operation temperature and age but the self-oscillating feedback loop ensures changes are tracked by the excitation frequency because a slope of the phase response of the piezoelectric transformer 804 is typically much steeper than a slope of a phase response of the low-pass filter 820. In this manner, the predetermined excitation frequency will be significantly more sensitive to changes in frequency response characteristic of the piezoelectric transformer 804 such that the self-oscillating feedback loop automatically maintains the predetermined excitation frequency at an optimum frequency or within an optimum frequency band such as in the ZVS operation band of the piezoelectric transformer 804.

CLAIMS

1. A piezoelectric power converter comprising:
   - a piezoelectric transformer comprising an input electrode electrically coupled to an input or primary section of the piezoelectric transformer and an output electrode electrically coupled to secondary or output section of the piezoelectric transformer to provide a transformer output voltage,
   - an input driver electrically coupled directly to the input electrode without any intervening series or parallel inductor to supply an input drive signal to the input electrode,
   - a feedback loop operatively coupled between the output voltage of the piezoelectric transformer and the input driver to provide a self-oscillation loop around the primary section of the piezoelectric transformer, oscillating at an excitation frequency, wherein:
   - electrical characteristics of the feedback loop are configured to set the excitation frequency of the self-oscillation loop within a ZVS operation range of the piezoelectric transformer.

2. A piezoelectric power converter according to claim 1, wherein a feedback signal of the feedback loop is derived from the transformer output signal at the output electrode of the piezoelectric transformer.

3. A piezoelectric power converter according to claim 1, wherein a feedback signal of the feedback loop is derived from a feedback output signal at a feedback output electrode arranged in one or more separate layer(s) of the output section of the piezoelectric transformer to galvanic isolate the feedback output electrode from the output electrode.

4. A piezoelectric power converter according to claim 4, wherein a volume of the separate layer(s) of the output section enclosing the feedback output electrode is smaller than a volume of layers of the output section enclosing the output electrode.

5. A piezoelectric power converter according to claim 3, wherein a voltage gain, at the excitation frequency, from the input electrode to the output electrode is larger or smaller than a

voltage gain from the input electrode to the feedback output electrode, preferably between 2 and 50 times larger or between 2 and 50 times smaller.

6. A piezoelectric power converter according to claim 1, wherein a feedback signal of the feedback loop is derived by a transformer resonance current estimator from a combination of the input drive signal and a transformer input current running in the primary section of the piezoelectric transformer.

7. A piezoelectric power converter according to claim 6, wherein the resonance current estimator comprises:
- a first order differentiator coupled to the input drive signal to derive a first order derivative signal of the input drive signal,
- a current sensor, coupled in series with the primary section of the piezoelectric transformer, to supply a sensor signal representative of the transformer input current; and
- a subtractor configured to generate the feedback signal based on a difference between the first order derivative signal and the sensor signal.

8. A piezoelectric power converter according to claim 6, wherein the first order differentiator comprises a first order high-pass filter having an input coupled to the input drive signal and an output supplying the first order derivative signal;
wherein a high-pass corner frequency of the first order high-pass filter is larger than a fundamental resonance frequency of the piezoelectric transformer such as at least two times larger or preferably more than 10 times larger.

9. A piezoelectric power converter according to claim 6 or 7, wherein the subtractor comprises a differential amplifier having a first differential input coupled to the first order derivative signal and the second differential input coupled to the sensor signal.

10. A piezoelectric power converter according to claim 5 or 6, wherein the input current sensor comprises a resistance arranged in-between a ground connection of the input driver and a ground connection of the piezoelectric transformer.

11. A piezoelectric power converter according to any of claims 2-9, wherein the feedback loop comprises a cascade of:
- a phase shifter coupled for receipt of the feedback signal to apply a predetermined phase shift to the feedback signal to provide a phase shifted feedback signal,
- a comparator coupled for receipt of the phase shifted feedback signal to generate a square-wave feedback signal at a comparator output; wherein the square-wave feedback signal is coupled to an input of the input driver so as to close the feedback loop.

12. A piezoelectric power converter according to claim 11, wherein the phase shifter comprises a high-pass, band-pass, low-pass filter or a time delay.

13. A piezoelectric power converter according to claim 10 or 11, wherein the comparator comprises an inverting zero-crossing detector to provide square-wave feedback signal indicating zero-crossings of the phase-shifted feedback signal.

14. A piezoelectric power converter according to any of the preceding claims, comprising:
- a bi-directional switching circuit coupled between the output electrode and an output voltage of the power converter,
- a controller adapted to control first and second states of the bi-directional switching circuit based on the input drive signal or the transformer output voltage such that:
- in a first state, forward current is conducted from the output electrode to the output voltage through the bi-directional switching circuit during a first period of a cycle time of the transformer output signal to charge the output voltage,
- in a second state, reverse current is conducted from the output voltage to the output electrode through the bi-directional switching circuit during a second period of the cycle time of the transformer output signal to discharge the output voltage and return power to the primary section of the piezoelectric transformer.

15. A piezoelectric power converter according to claim 14, wherein the controller in the second state is further configured to control the switching circuit such that:

- both forward current and reverse current is conducted during a single cycle of the transformer output signal.

16. A piezoelectric power converter according to claim 14 or 15, wherein the switching circuit comprises a half-wave rectifier or a full-wave rectifier operatively coupled to the output electrode.

17. A piezoelectric power converter according to any of claim 14-16, wherein the feedback loop comprises an adjustable time delay coupled in cascade with the phase shifter and the comparator to adjust the excitation frequency of the self-oscillating loop.

18. A piezoelectric power converter according to claim 17, wherein the feedback loop comprises:
    - a current detector configured to determine a level of a transformer resonance current resonance of the piezoelectric transformer,
    - a current limiter adapted to adjust a time delay of the adjustable time delay circuit to limit the transformer resonance current.

19. A piezoelectric power converter according to any claims 12-18, wherein a slope or derivative of a phase response of a transfer function of the piezoelectric transformer is steeper than slope or derivative of a phase response of the band-pass, high-pass or low-pass filter within the ZVS operation range of the piezoelectric transformer.

20. A piezoelectric transformer according to any of the preceding claims, comprising a piezoelectric transformer with a zero-voltage switching factor (ZVS factor) larger than 100%, preferably larger than 120%, such as larger than 150% or 200%;

    in which the ZVS factor is determined at a matched load condition as:

$$ZVS = \frac{\left(k_{eff\_S}^{-2}\right)-1}{\left(k_{eff\_P}^{-2}\right)-1} 0.882 \text{ ;}$$

$k_{eff\_P,}$ being a primary side effective electromechanical coupling factor of the piezoelectric transformer,

$k_{eff\_S,}$ being a secondary piezoelectric transformer effective electromechanical coupling factor, in which:

$$k_{eff\_P} = \sqrt{1 - \frac{f_{res\_p}^2}{f_{anti-res\_p}^2}} \qquad k_{eff\_S} = \sqrt{1 - \frac{f_{res\_s}^2}{f_{anti-res\_s}^2}}$$

f_{res_p} = resonance frequency and frequency of a minimum magnitude of an impedance function at the input electrodes of the piezoelectric transformer with shorted output electrodes,

$f_{anti\text{-}res\_p}$ = anti-resonance frequency and frequency of a maximum magnitude of the impedance function at the input electrodes of the piezoelectric transformer with shorted output electrodes,

f_{res_s} = resonance frequency and frequency of a minimum magnitude of the impedance function at the output electrodes of the piezoelectric transformer with shorted input electrodes,

$f_{anti\text{-}res\_s}$ = anti-resonance frequency and frequency of a maximum magnitude of the impedance function at the output electrodes of the piezoelectric transformer with shorted input electrodes.

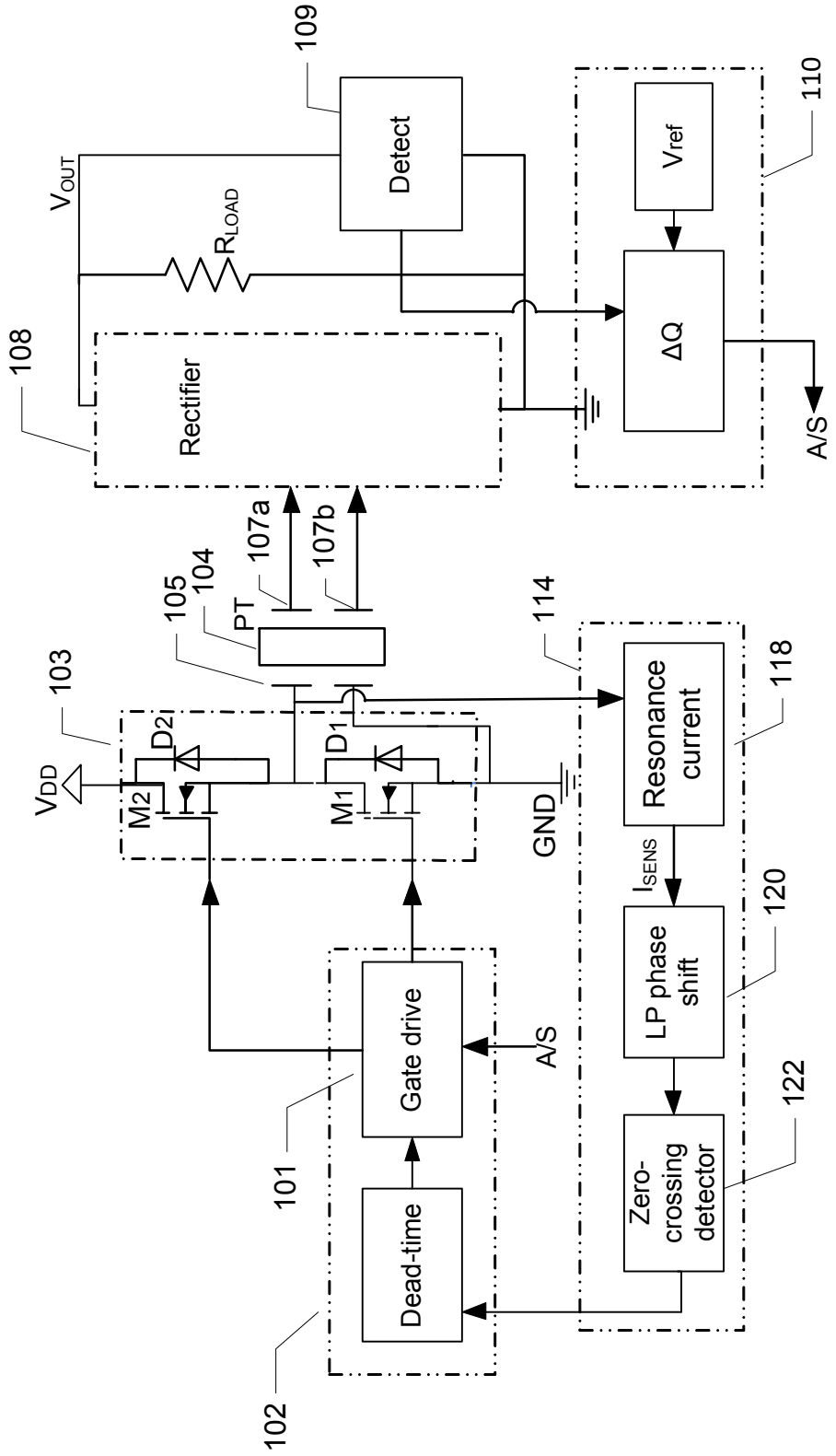
21. A piezoelectric power converter according to any of the preceding claims, wherein a bandwidth of the ZVS operation range of the piezoelectric transformer lies between 1% and 5% of a fundamental or primary resonance frequency of the piezoelectric transformer.

22. A piezoelectric power converter according to any of the preceding claims, wherein a wiring inductance at the output of the input driver to the input electrode is smaller than 500 µH, preferably smaller than 100 µH, even more preferably smaller than 10 µH.

23. A piezoelectric power converter according to any of the preceding claims, comprising a start-up circuit configured to inject a transient signal into the feedback loop at power-up of

the power converter to initiate oscillation at the excitation frequency in the feedback loop.

24. A piezoelectric power converter according to claim 23, wherein the start-up circuit comprises an oscillator coupled into the feedback loop.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102
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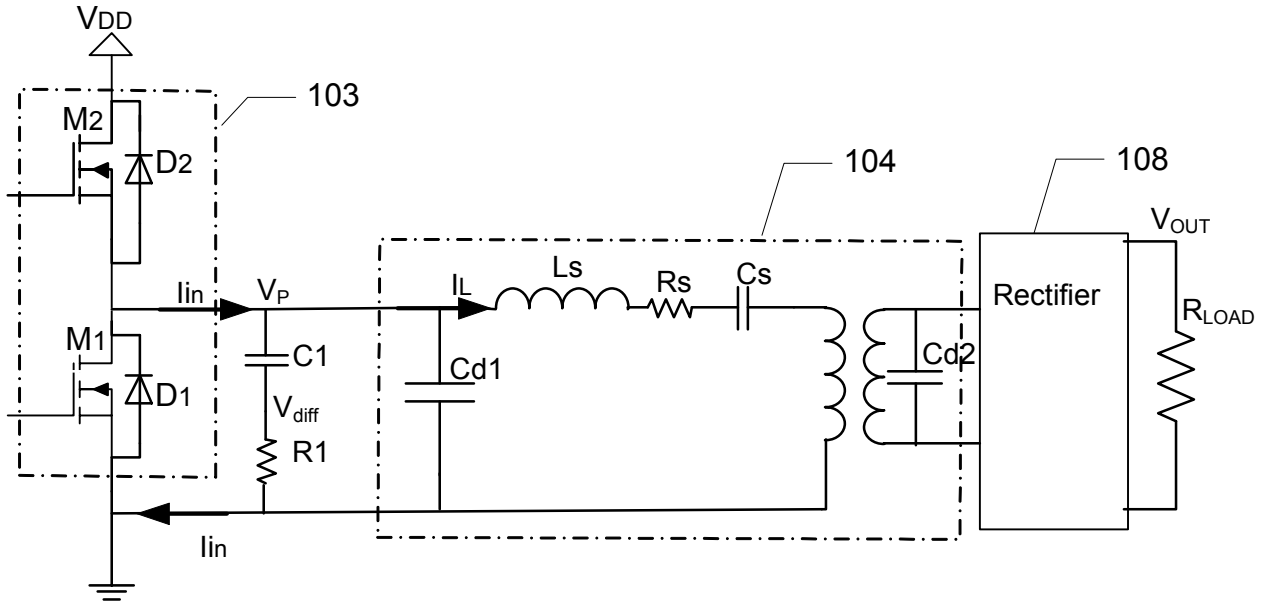
Dead-time
Gate drive
A/S
122
Zero-crossing detector
120
LP phase shift
I_{SENS}
118
Resonance current
114
GND
V_{DD}
103
M_2
D_2
M_1
D_1
105
104
PT
107a
107b
108
Rectifier
V_{OUT}
R_{LOAD}
109
Detect
110
V_{ref}
ΔQ
A/S

Fig. 1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M2
D2
M1
D1
Iin
VP
C1
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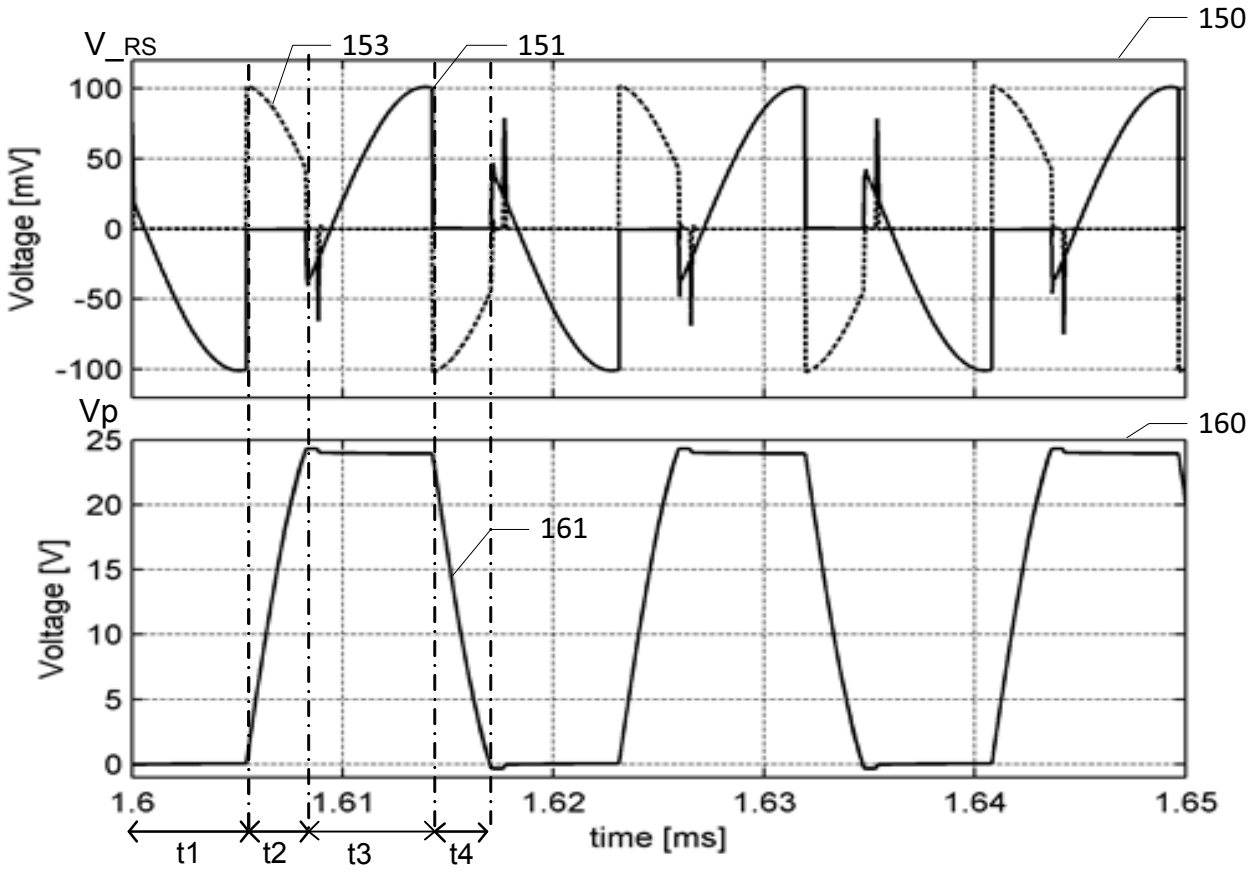
R1
Cd1
IL
Ls
Rs
Cs
104
Cd2
108
Rectifier
VOUT
RLOAD
Iin

a)


V_RS
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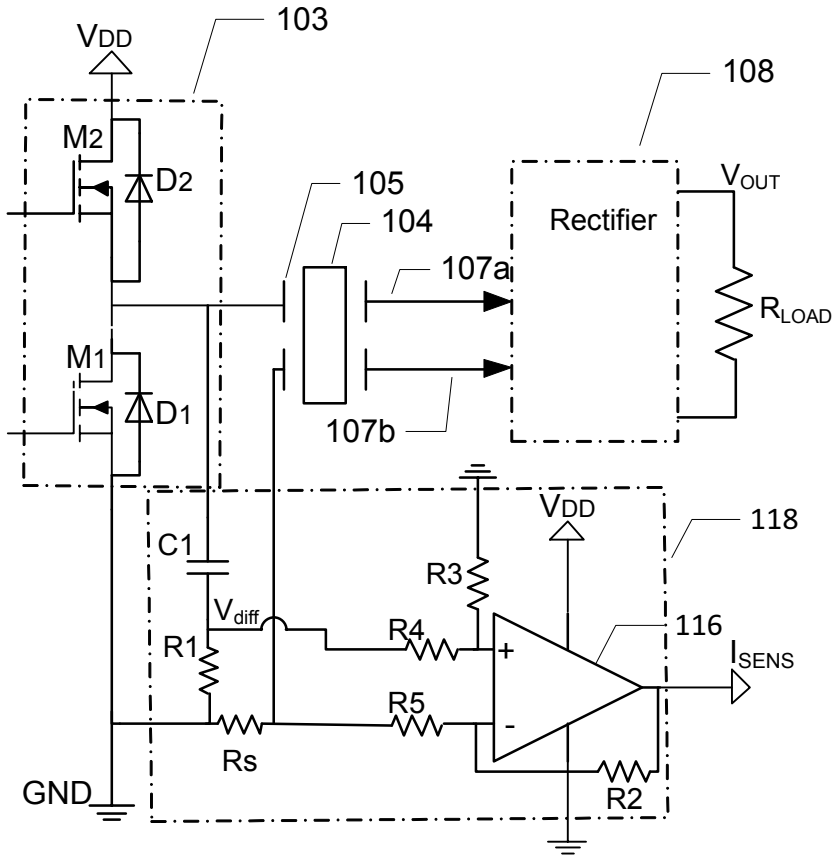
151
150
100
50
0
-50
-100
Voltage [mV]
Vp
160
161
25
20
15
10
5
0
Voltage [V]
1.6
1.61
1.62
1.63
1.64
1.65
time [ms]
t1
t2
t3
t4

b)

Fig. 2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108
M2
D2
105
104
Rectifier
VOUT
107a
RLOAD
M1
D1
107b
VDD
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Vdiff
R4
116
R1
+
ISENS
R5
-
Rs
GND
R2

Fig. 3

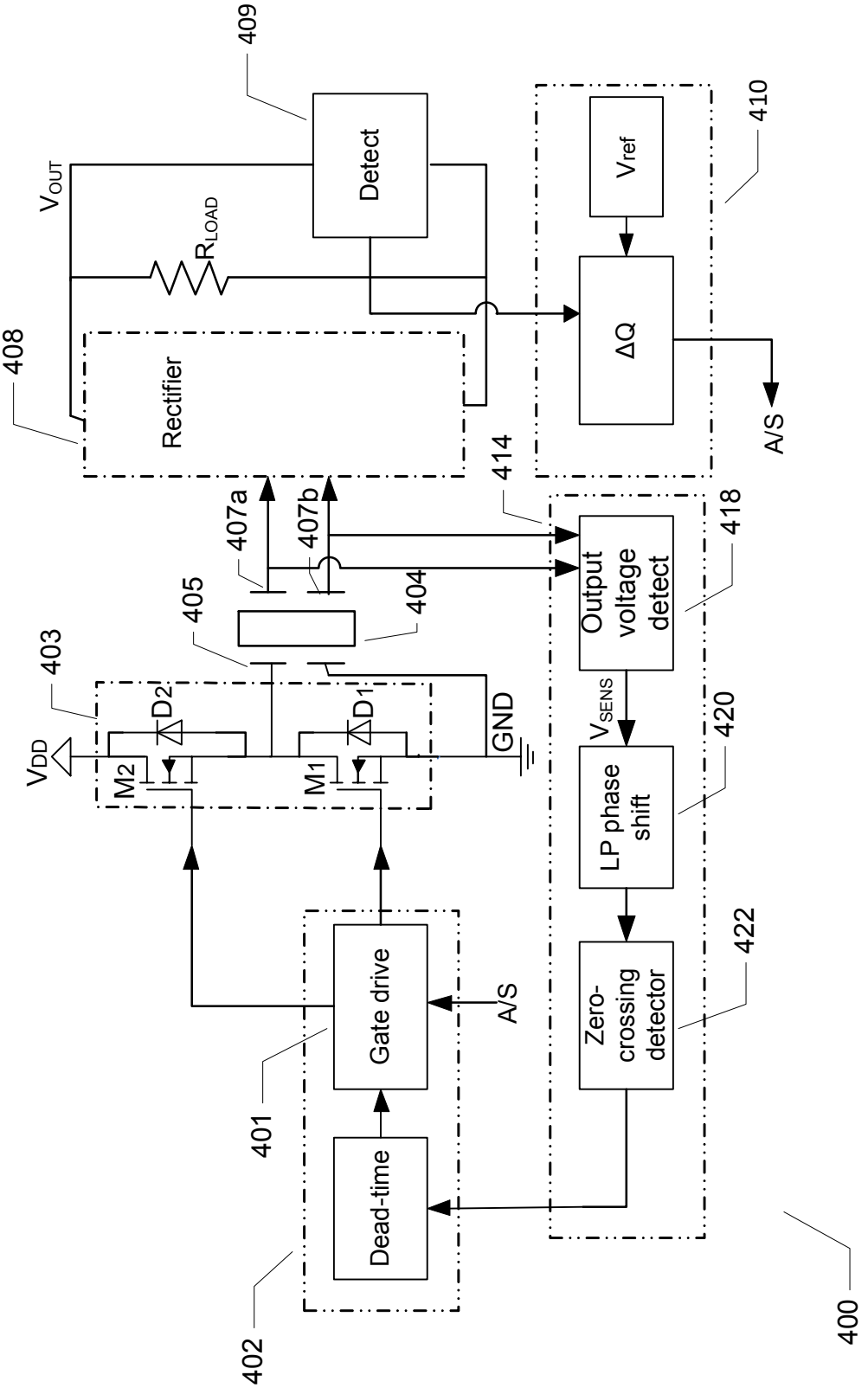
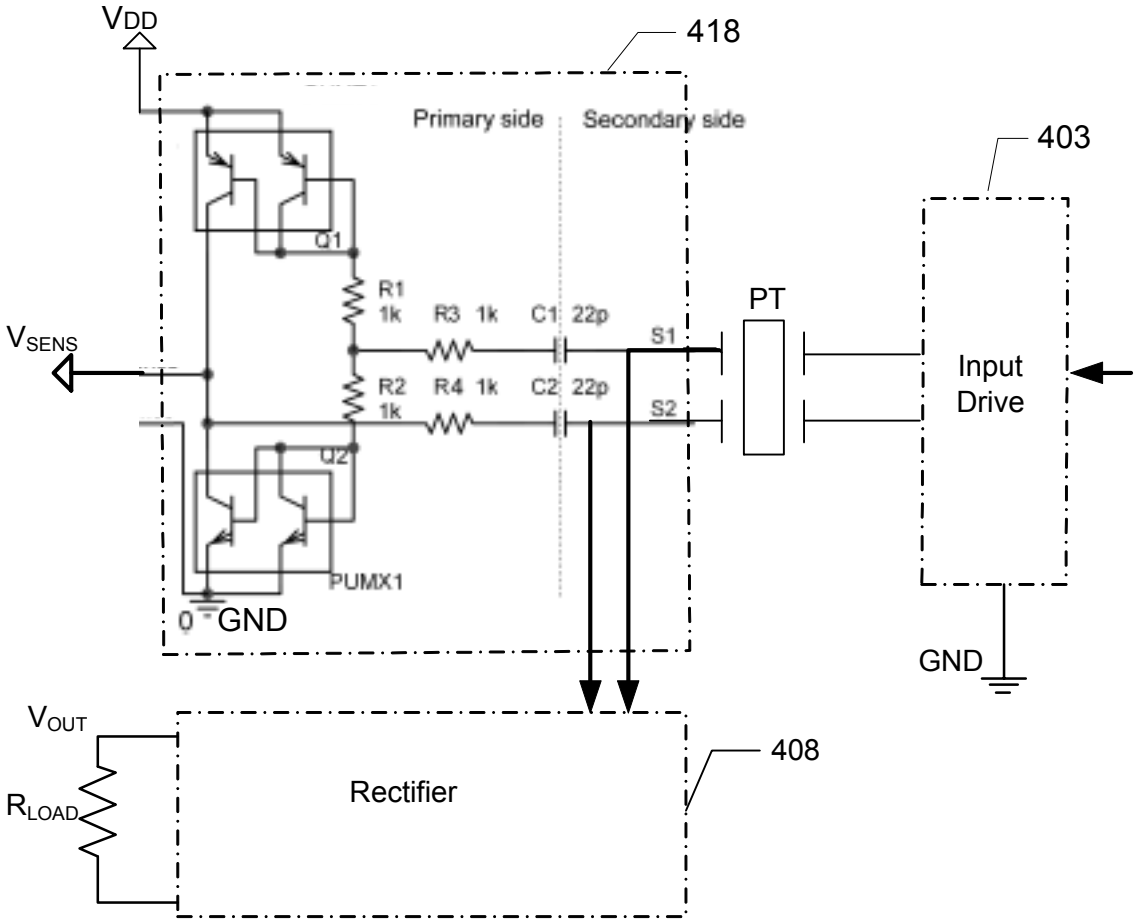

409
Detect
V_{OUT}
R_{LOAD}
408
Rectifier
410
Vref
ΔQ
A/S
414
407a
407b
404
405
403
418
Output voltage detect
V_{SENS}
420
LP phase shift
422
Zero-crossing detector
V_{DD}
D2
D1
GND
M2
M1
Gate drive
A/S
401
Dead-time
402
400

Fig. 4


VDD
418
Primary side
Secondary side
403
Q1
R1
1k
R3 1k
C1 22p
S1
PT
VSENS
R2
1k
R4 1k
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Input
Drive
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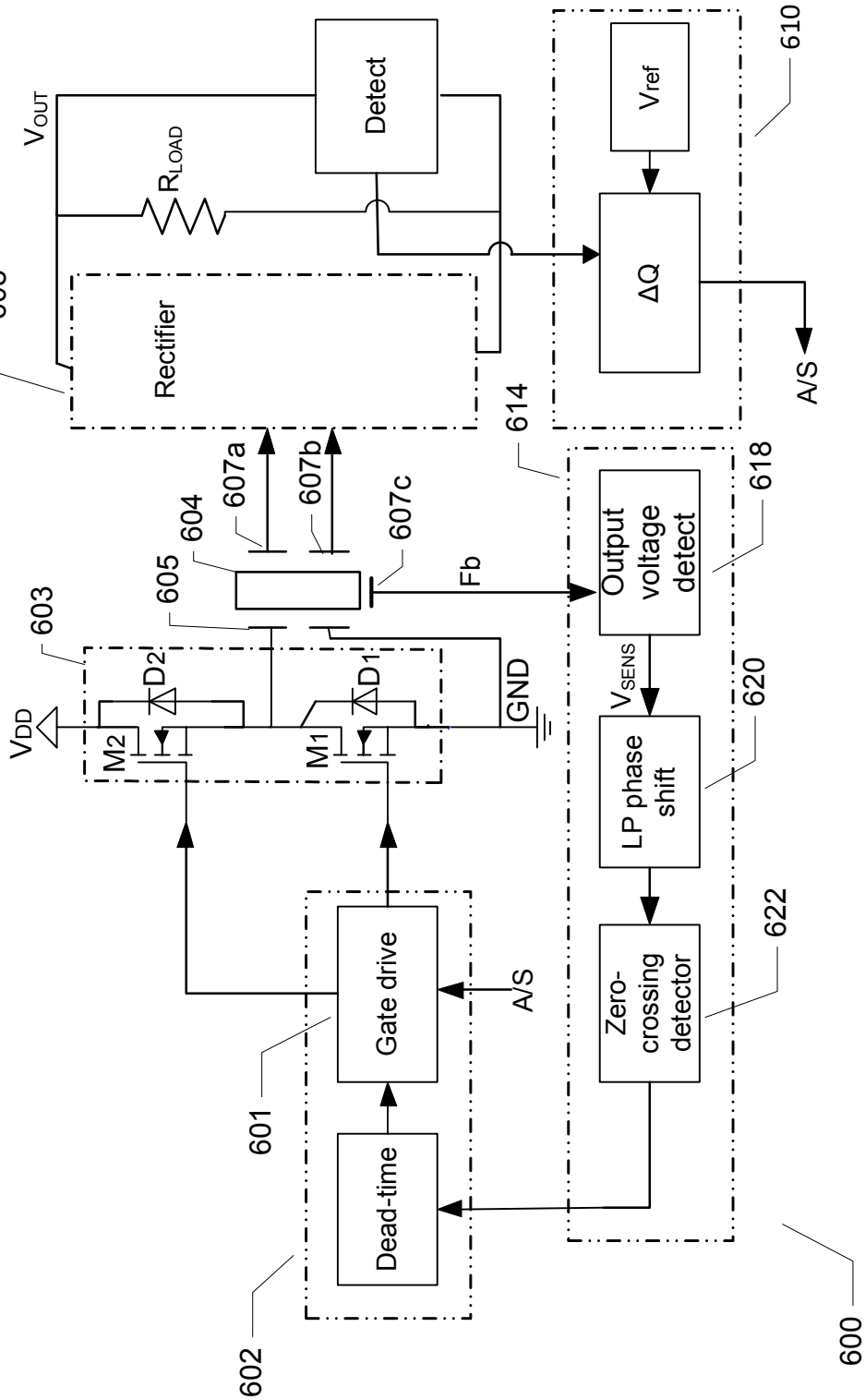
0
GND
GND
VOUT
RLOAD
Rectifier
408

Fig. 5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602
601
Dead-time
Gate drive
A/S
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Zero-crossing detector
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LP phase shift
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Output voltage detect
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Vref
ΔQ
A/S
608
Rectifier
Detect
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Fb
VSENS

Fig. 6

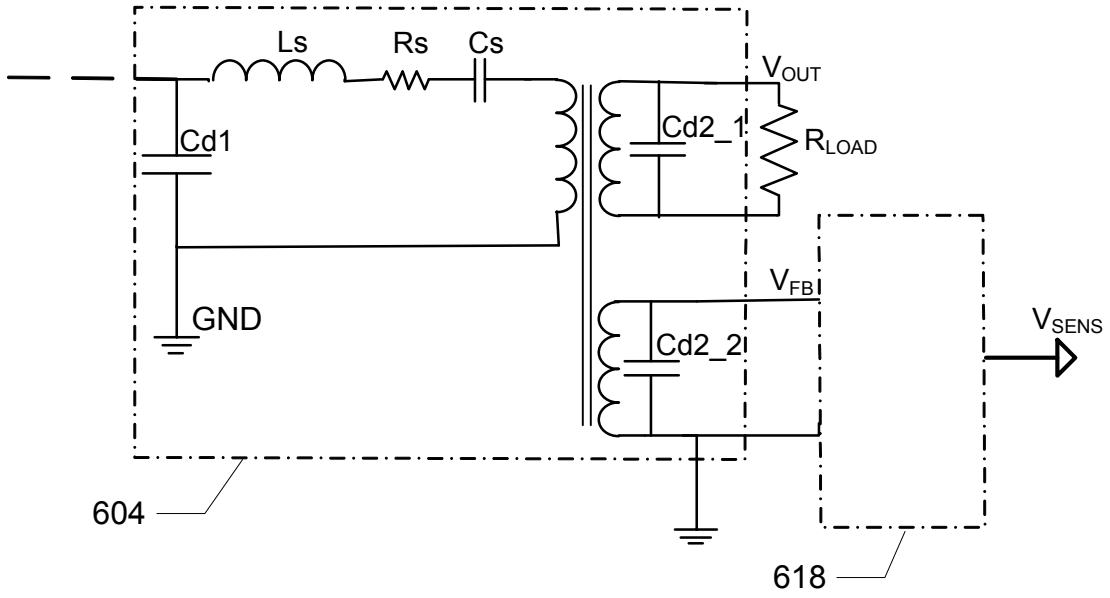
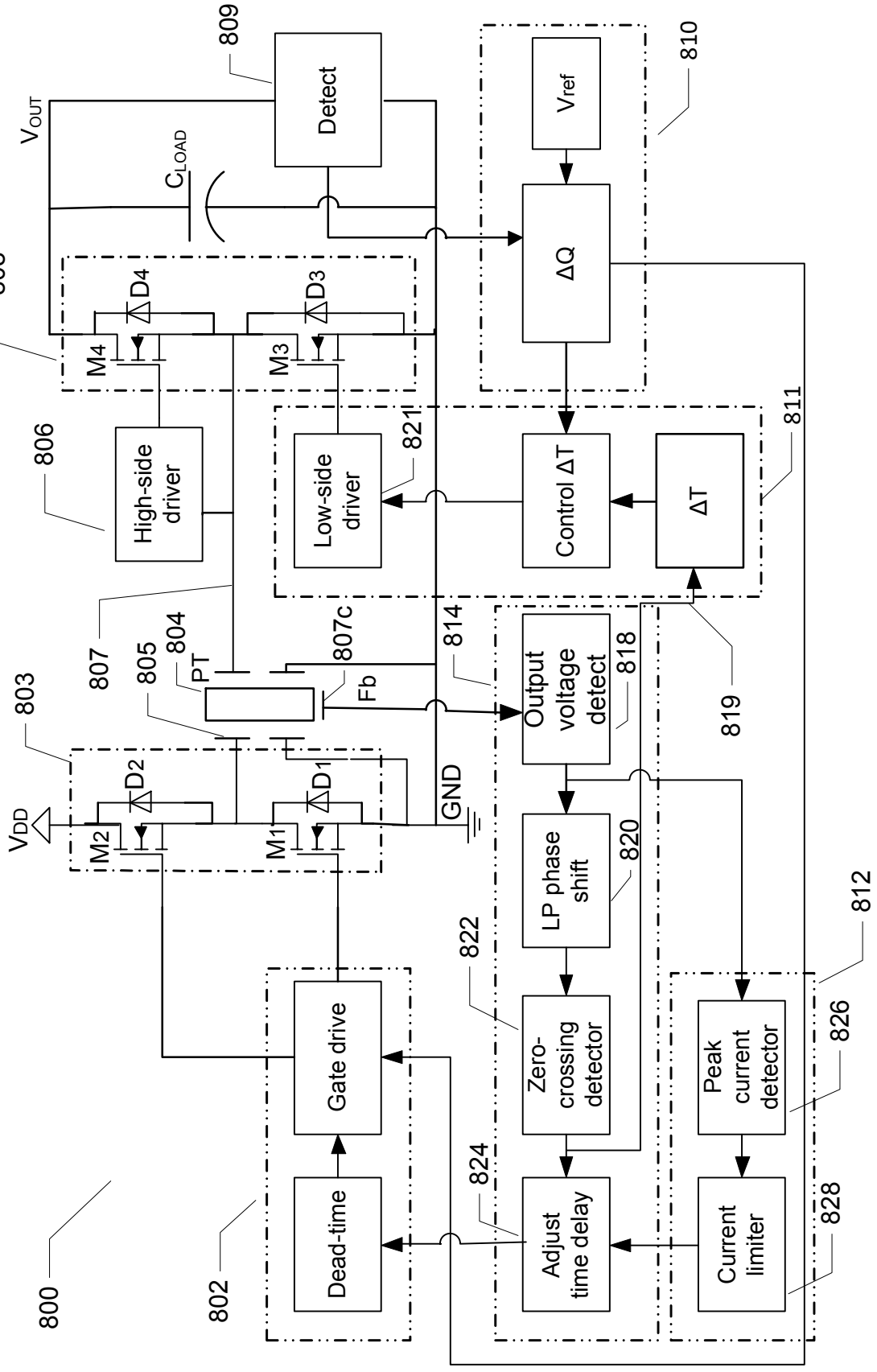


Fig. 7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828
Detect
V_{OUT}
C_{LOAD}
V_{ref}
ΔQ
ΔT
Control ΔT
High-side driver
Low-side driver
Output voltage detect
LP phase shift
Zero-crossing detector
Peak current detector
Adjust time delay
Current limiter
Gate drive
Dead-time
V_{DD}
GND
PT
Fb
D1
D2
D3
D4
M1
M2
M3
M4

Fig. 8

Appendix: A8

T. Andersen, M. S. Rødgaard, O. C. Thomsen and M. A. E. Andersen, "Low voltage driven dielectric electro active polymer actuator with integrated piezoelectric transformer based driver", in SPIE, 2011, p. 79762N

Low voltage driven dielectric electro active polymer actuator with integrated piezoelectric transformer based driver

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ABSTRACT

Today's Dielectric Electro Active Polymer (DEAP) actuators utilize high voltage (HV) in the range of kilo volts to fully stress the actuator. The requirement of HV is a drawback for the general use in the industry due to safety concerns and HV regulations.
In order to avoid the HV interface to DEAP actuators, a low voltage solution is developed by integrating the driver electronic into a 110 mm tall cylindrical coreless Push InLastor actuator. To decrease the size of the driver, a piezoelectric transformer (PT) based solution is utilized. The PT is essentially an improved Rosen type PT with interleaved sections. Furthermore, the PT is optimized for an input voltage of 24 V with a gain high enough to achieve a DEAP voltage of 2.5 kV. The PT is simulated and verified through measurements on a working prototype. With the adapted hysteretic based control system; output voltage wave forms of both impulse response and sinusoidal shapes up to 2.5 kV are demonstrated. The control system, together with a carefully designed HV output stage, contributes to low power consumption at a static DEAP force. The HV stage consists of a HV measurement circuit and a triple diode voltage doubler optimized for low leakage current drawn from the DEAP.
As a result, a 95 mm x 13 mm x 7 mm driver is integrated in a 110 mm x 32 mm actuator, forming a low voltage interfaced DEAP actuator.

Keywords: Piezoelectric Transformer, high voltage, Dielectric Electro Active Polymer, PolyPower, hysteretic control, integrate, actuator, converter

1. INTRODUCTION

DEAP devices are based on polymer materials and change shape as a result of the electrostatic forces, generated by an applied voltage. The DEAP technology has a wide potential in applications such as surgical tools, grippers for material handling and valve actuators for example. The DEAP material can be modulated as a high voltage capacitor with a very low leakage current, where the force from the DEAP is related to the applied voltage. The DEAP technology available today requires a high voltage (HV) to fully utilize it as an actuator. The voltage is dependent among other by the thickness of the DEAP film. The film thickness is around 80 µm [2][13] and has a maximum working voltage of 2.5 kV. One of the barriers for using these actuators commercial is the need of a HV source. The HV interface is undesirable for practical and safety reasons. The approach in this paper is to construct a DEAP actuator with a low voltage interface, by integrating a HV driver inside the actuator. This has some requirements for the DEAP actuator and the driver itself. The actuator need to be hollow to make space for the driver inside. For that purpose a coreless Push InLastor actuator [2][13] is used for prototyping the concept. As for the driver its primary goal is to be small enough to fit inside the actuator and to deliver adequate power.
The driver typically consists of a step-up switch mode power converter and trough out this paper, the driver is also referred to as a converter. To date, conventional converters utilize electromagnetic components for converting the energy and are the only available HV sources for driven DEAP actuators. However these HV converters have poor efficiency, are bulky and provide limited opportunities for miniaturization. Piezoelectric Transformer (PT) based converters, however, is compact and offers high efficiency, especially in high step up applications. The PT based converter is a perfect match for DEAP technology and offers the miniaturization possibilities needed to integrate it in to a core less DEAP actuator. PTs were originally developed by Rosen in 1957 [1] and uses piezoelectric ceramics to convert electrical

energy trough mechanical vibrations and are already commonly used for backlighting LCD displays, but are still limited to these simple applications (with constant high frequency AC load). In the last decade a lot of research in to the area of PTs has improved Rosen's fist transformer and new types of transformers has been designed [4][15][17][18][20].

2. PIEZOELECTRIC TRANSFORMER

A piezoelectric material is a material that has an electromechanical coupling. This coupling generates a charge displacement, which is proportional to the deformation of the material. A PT is basically two piezoelectric elements which is joined together to form a transformer. The primary side element is then exited by an electrical voltage, which induces a deformation of the two joined elements, that generates a voltage on the secondary side element. With a proper design of the PT, a desired voltage conversion can be obtained from the primary to the secondary side. In order to convert power at a high efficiency, the PT is operated in one of its resonance modes [14][16][17][20]. PT resonates each time it is possible to generate a standing wave in the element. However the design is usually optimized for one specific resonance mode in order to gain the highest efficiency [14][17].
The PT resembles a distributed network, but for simplicity and mathematical representation, only the resonance mode of interest is modeled [14][16][17]. One of the most used PT models is the lumped parameter model, which was first derived by Mason in 1942 [3] and is show in figure 1.

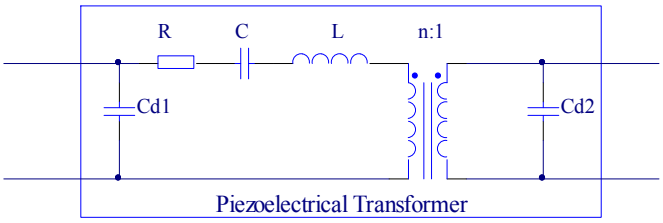

Figure 1: Lumped parameter model, which describes the behavior of the PT in narrow band around the resonance mode.

The circuit is basically a LCC resonance tank and the behavior of the PT based converter is also quit similar to a traditional resonance converter.

2.1 PT design

The Piezoelectric Transformer (PT) developed for this application is essential an interleaved multi layer Rosen-type, as the one presented in [4].
To the left in figure 2 the structure of the PT is shown, which consists of a primary section with 12 layers and one split secondary layer.

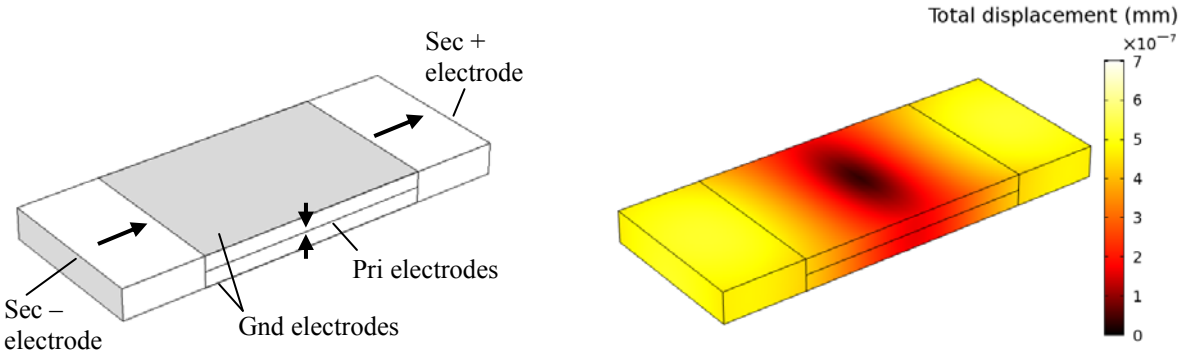

Figure 2: Left: PT structure, where the arrows indicate the polarization direction. Right: COMSOL finite element method simulation of the PT, operating in the first longitudinal mode shape, at 65.1 kHz. The coloring illustrates the total displacement, where dark colors refer to a low displacement and light colors to at high displacement, as the color bar indicates.

The figure only illustrates two primary layers, for simplicity, and the arrows indicate the polarization direction. The PT is build using tape casting technology. The piezoelectric material used is the NCE46 [19] and the PT has the following dimensions 25 mm x 10 mm x 2 mm.
The PT design is quite similar to one presented in [4], with the exception of the secondary polarization. The operational vibration resonance is along the longitudinal direction and is generated trough the electromechanical coupling factors k31 and k33, primary and secondary respectively. To the right in figure 2 a finite element method (FEM) simulation of the operational vibration resonance is shown. The PT operates in its first mode shape and it can be seen that it has a nodal line in the center of the structure.
One of the drawbacks of this design, for this application, is the split secondary. This results in a differential output voltage symmetrical around ground, which complicates the electronics somewhat, which is addressed in section 0. One could have polarized the two half secondary layers in opposite directions, which results in a two layer secondary structure, with a common voltage potential with reference to ground, as in [4]. But this approach would also half the gain of the PT, because of two secondary layers instead of one. For this application we need a high gain, so the extra effort in the electronic is rewarded with a doubling in gain.

In order to evaluate the electrical characteristics of the PT, the lumped equivalent parameters are found trough the method described in [5]. Trough a FEM simulation of the PT impedance the following equivalent parameters are found.

R	C	L	C_{d1}	C_{d2}	1/n
114 mΩ	9.8 nF	609 µH	91.7 nF	17.5 pF	93.5

Table 1: PT lumped equivalent parameter obtained trough FEM simulations.

From these equivalent parameters some more general performance properties of the PT can be calculated, as the matched load (1), efficiency (2) and gain (3).

When the load is matched to the PT output, the PT operates at its highest efficiency [5]. Match load condition (1) is depended on the terminal capacitance on the secondary side and the operating frequency.

The total loss mechanisms of piezoelectric materials are not fully implemented in the FEM simulation. The efficiency (2) is only a non stressed efficiency (derived in [5]), because the simulation is performed with small signals. Therefore this efficiency is generally a measure between different designs.

$$R_{match} = \frac{1}{C_{d2}\omega_r} \tag{1}$$

$$\eta_{match} = 1 - \frac{2RC_{d2}}{n^2\sqrt{LC}} \tag{2}$$

The gain (3) is the maximal obtainable gain, from the input of the PT to the split output. The maximum gain occurs at resonance.

$$A_{\max} = \frac{\sqrt{2}}{n}\eta \tag{3}$$

The following table contains the found PT properties.

A_{max}	R_{match}	η_{match}
130	138 kΩ	98.6 %

Table 2: PT performance properties calculated from FEM simulated equivalent parameters.

Evaluating these properties it can be seen that it has a high efficiency and a high gain, which results in a 1258 V_{rms} output voltage, in to a matched load, with a PT modulation of 9.67 V_{rms}. The PT modulation voltage is the first harmonic, of the 24 V input voltage, as derived in [5].

2.2 Prototype verification

After receiving the prototype PTs, the functionality and properties were verified. The following equivalent parameters and performance properties are found.

R	C	L	C_{d1}	C_{d2}	1/n
461 mΩ	6.74 nF	922.7 µH	111.7 nF	24.8 pF	88.6

Table 3: PT lumped equivalent parameter obtained trough prototype measurements.

A_{max}	R_{match}	η_{match}
116	100 kΩ	93.3 %

Table 4: PT performance properties calculated from prototype measured equivalent parameters.

Comparing these numbers, it can be seen that the gain are 10 % lower than expected. This is partly because the prototype buildup were 2.1 mm high, instead of the intended 2 mm, and therefore the primary layers are 5 % higher, which results in a 5 % decrease in gain. Furthermore there is some inactive piezoelectric material in the primary section, due to the termination of the primary electrodes on the side of the PT. This is not included in the FEM simulation and accounts for some of the remaining 5 % deviation. Hence there is a very good correlation between the FEM model and the prototype concerning the gain.
Looking at the capacitances C_{d1}, C_{d2} and the efficiency, the correlation is not very good. This is expected to be caused by a bad correlation between the NCE46 material parameters in the FEM model and what they in fact are in real life, as well as an incomplete loss model in the simulation. This problem will be addressed in a future paper. Nevertheless the FEM simulation makes it possible to design PTs with a desired gain, as well as the possibility to compare the efficiency between different designs. For this specific case there is not a well defined resistive load and therefore the matching inaccuracy is not a problem.

3. CONVERTER STRUCTURE

The converter structure contains several parts: control circuit, a power stage, the PT, a voltage doubler rectifier, discharge circuit and a high voltage measurement circuit. A block diagram is shown in figure 3 3 including a capacitor for modeling the DEAP. The PT based converter is essentially just a resonance converter, with some unique PT characteristics [12][14][16][17][18]. One of the characteristic of the PT is that the resonance network is of a high quality factor, hence giving it a very narrow bandwidth of operation. Therefore a good and precise control of the operating frequency is important, in order to maximize efficiency and ensure proper operation. The power stage of the converter is a typical half-bridge solution. The discharge of the DEAP is performed trough a resistive load controlled by the controller. The power stage and discharge circuit will not be addressed in this paper [14][21].

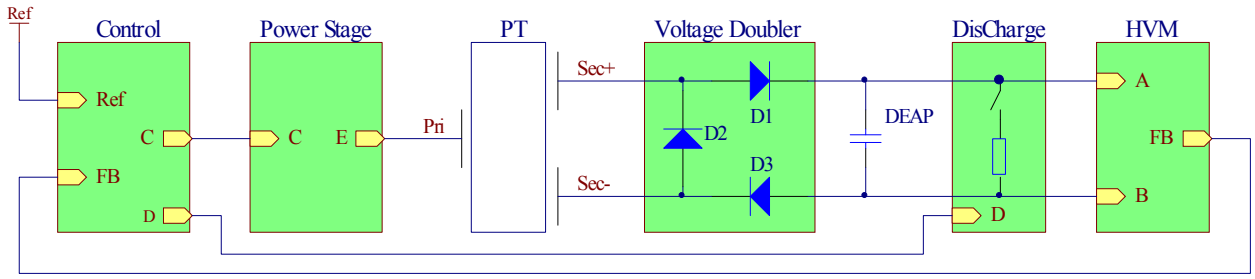

Figure 3: Block diagram of the PT based converter including the DEAP model.

4. VOLTAGE DOUBLER RECTIFIER

The sinusoidal output of the PT is rectified in a voltage doubler rectifier [8], which in this case consists of three diodes (D1, D2, D3) unlike the normal two (D1, D2). The extra diode (D3) is added to support the PTs split output, which produces a differential voltage symmetrical around ground. Without D3 one of the DEAP terminals would be connected directly to the PTs output, resulting in the DEAP bouncing up and down, with the potential of the PT output. Furthermore this would load the output of the PT with the DEAP's parasitic capacitance and lead to an increase in the common mode EMC. Beside a lower EMC, the third diode allows for the DEAP voltage to be steady around ground. This also has the advantage of lowering the current consumption in the high voltage measuring circuit, which is addressed in section 6.

5. CONTROL

As mentioned in section 3, the PT based converter is very sensitive to its operating frequency, thus a good and precise tracking of the resonance frequency is important, in order to compensate variations, caused by operating conditions and external influences. To insure this, a closed phase-loop is made, which is very similar to the one presented in [9]. This closed loop will tune itself to tracks the resonance frequency, ensuring optimal operation.
A second loop is closed around the output voltage, in order to control the output voltage. The measurement of the output voltage is not trivial and is described in detail in the section 6. Figure 4 illustrates the implementation of the charge and discharge control, which controls the output voltage.
The feedback signal (FB) is a 0 - 4 V feedback, which is proportional to the 0 - 2.5 kV variation of the output voltage and is compared to the reference voltage (Ref). R5 and C2 form a low-pass filter that limits the feedback bandwidth (BW) to 500 Hz, as well as it suppresses high frequency noise. The reference voltage is passed through a voltage divider (R3 and R4), that makes a 0 - 5 V reference voltage swing correspond to the 0 - 2.5 kV output voltage swing. Together with C1 they form a low-pass filter, which limits the reference voltage BW to 170 Hz. This is done to ensure an upper limit of operation, which should be at least 20 Hz.

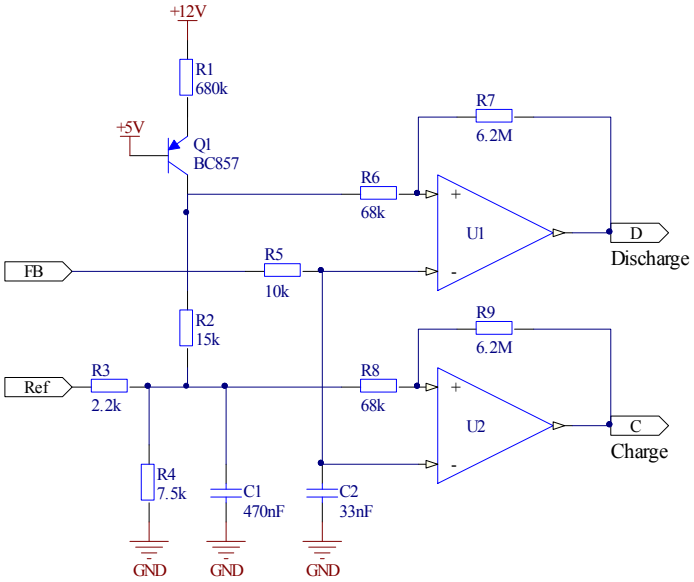

Figure 4: Hysteresis based control circuit, for the control of charge and discharge of the DEAP/output voltage, based on the HV measurement feedback.

The two comparators (U1 and U2) and their two associated resistors (R6, R7 and R8, R9) form two hysteresis windows of 55 mV, which corresponds to approximately 34 V on the output voltage. The lower comparator (U2) controls the charge cycle and when the feedback signal (FB) drops below the lower boundary of the hysteresis, the converter is turned on and charges the DEAP. The converter is then charging until the feedback hits the upper boundary, which would be a 34 V charge, if the reference voltage was kept constant. The same applies for the upper comparator (U1),

with the difference that it discharges the DEAP when the feedback hits the upper hysteresis boundary, until it reaches the lower boundary. The DEAP is simply discharge trough a resistive load, until it hits the lower boundary.
In order to separate these two hysteresis windows, R1, Q1 and R2 are added to the circuit. R1 and Q1 form a small current source, which generates a constant current. This current is passed through R2, resulting in a constant voltage across it, which separates the hysteresis windows with a constant voltage of approximately 150 mV, corresponding to 94 V on the output voltage.
Trough small bursts of charging and discharging, dependent on the reference voltage, the output voltage is kept within a limited range of the reference voltage. The separation voltage and hysteresis windows can be optimized further, in order to make the output voltage follow the reference even tighter.

6. HIGH VOLTAGE MEASUREMENT

The control circuit uses a feedback signal from a high voltage measurement circuit to regulate the output voltage. The high voltage measurement circuit has to handle voltages of at least 2.5 kV at frequencies below 20 Hz. The impendence of the measurement circuit becomes important in static operations, when a static force from the DEAP has to be maintained. In static operation the output voltage is maintained by the DEAP's capacitance, however the impedance of the measurement circuit together with the DEAP's leakage current will discharges the DEAP over time. The converter has to supply the current drawn from the DEAP to keep a constant output voltage. The overall power consumption in static operation depends on the current drawn from the DEAP. It is not in the scope of this paper to change the leakage current of the DEAP, it is therefore the objective to make the leakages current dominant compared to the current drawn by the measurement circuit. The leakage current of six DEAP samples is measured and spans from 14 nA to 959 nA, measured at 2 kV. For the DEAP leakages current to be dominant the total impedance of the measurement circuit has to be higher than: 143 GΩ - 2 GΩ (depending on the DEAP sample). For practical reasons it is not possible to work with physical small sized HV impedances in the 100 GΩ range, for comparison the volume resistivity of normal PCB is 1 - 1000 GΩ·cm depending on humidity, temperature, etc. [10].

6.1 Circuit analysis and design

The output of the PT is equivalent with two ground connected AC current sources each in parallel with a capacitor and then rectified to form a positive rail (A) and a negative rail (B). The two output rails are ideally symmetrical around ground and together forms the output voltage (A - B = V_{out}).The converters output stage equivalent is shown to the left of figure 5.

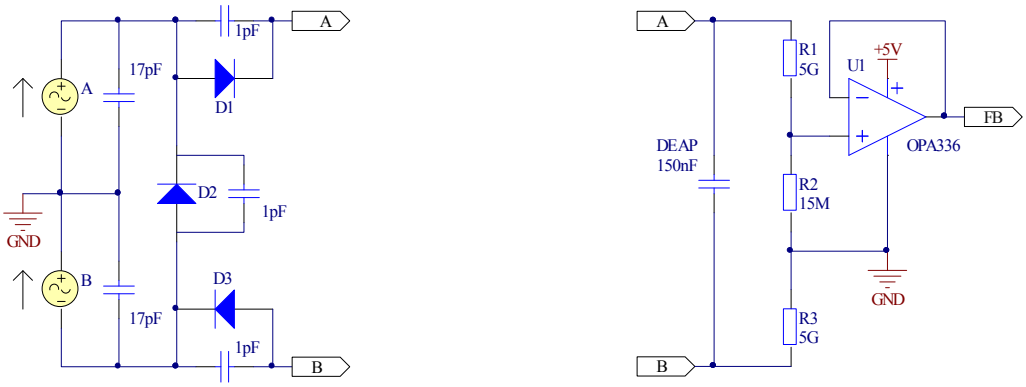

Figure 5: Left: Converter output stage equivalent circuit, with symmetric output voltage around ground. Right: High voltage measurement circuit, with resistive voltage divider, for low voltage ground referenced feedback signal.

To the right hand side of figure 5 a resistive high voltage measurement circuit together with the DEAP equivalent is shown. A resistive voltage divider from the positive to the negative rail (R1 & R2 & R3) gives a low voltage signal, referenced to ground, which is proportional to the output voltage. This signal is buffered by an operational amplifier with a very high input impedance (>10 TΩ) and is used as the feedback signal (FB) for the converters controller circuit. To keep the output voltage symmetric around ground, the resistance from the two rails to ground must be equal.

The low frequency relationship between the output voltage and the feedback signal for the circuit in figure 5 is given by the transfer function (4).

$$\frac{FB}{V_{out}} = \frac{R_2}{R_1 + R_2 + R_3} \tag{4}$$

For the circuit to handle dynamic measurements the parasitic capacitors in the circuit cannot be ignored. For this application the resistor values need to be comparable with the DEAP's leakage current, in order to minimize discharge of the DEAP. These high value resistors together with a highly compact circuit layout increase the impact from the parasitic capacitors on the transfer function, resulting in a frequency depended feedback signal. Furthermore the parasitic capacitance from the DEAP to the surroundings introduces significant noise on top of the high voltage rails from the 50 Hz mains. A model with the parasitic capacitors is seen to the left of figure 6. To eliminate the impact of the parasitic capacitors, without increasing the static discharge of the DEAP, a capacitive voltage divider is added. By using relatively large capacitors in the divider the impact from the parasitic capacitors is neglected. The transfer function for the combined resistive and capacitive voltage divider is given in (5) and is now frequency depended. By using the relation in (6) the transfer function becomes independent of frequency (7).

$$\frac{FB}{V_{out}} = \frac{\dfrac{R_2}{1 + j\omega R_2 C_2}}{\dfrac{R_1}{1 + j\omega R_1 C_1} + \dfrac{R_2}{1 + j\omega R_2 C_2} + \dfrac{R_3}{1 + j\omega R_3 C_3}} \tag{5}$$

$$R_1 C_1 = R_2 C_2 = R_3 C_3 \tag{6}$$

$$\frac{FB}{V_{out}} = \frac{R_2}{R_1 + R_2 + R_3} = \frac{\dfrac{1}{C_2}}{\dfrac{1}{C_1} + \dfrac{1}{C_2} + \dfrac{1}{C_3}} \tag{7}$$

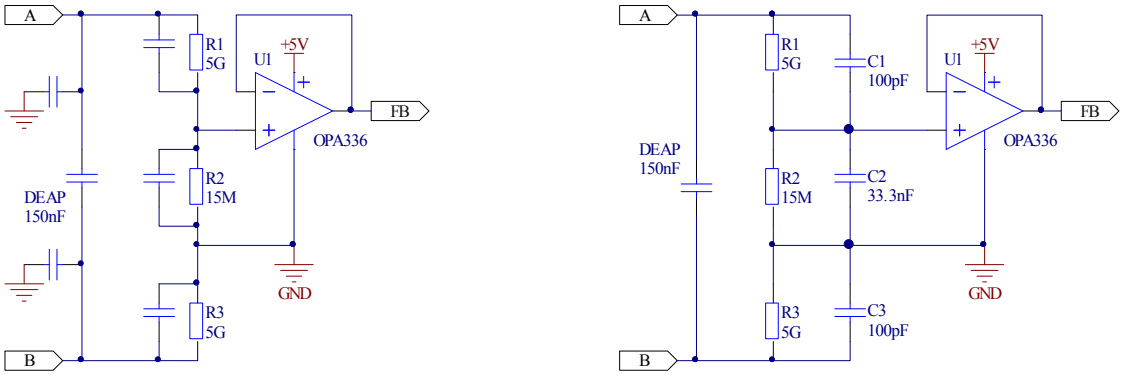

Figure 6: Left: High voltage measurement circuit including unknown parasitics. Right: High voltage measurement circuit with resistive and capacitive voltage divider to avoid the impact from parasitic components.

7. INTEGRATION

The integration of the electronics into the DEAP actuator has been a main concern right from the start. Therefore the physical size and shape of the driver has also been a significant part of the development, as well as the mechanical interface and incorporation of the driver in the actuator.
The actuator has a winding-insert in each end to support the coreless DEAP actuator. The cross-section area of the prototype converter is 12.8mm x 7.5mm and fits into the elliptical cross-section area of the winding-inserts, as seen to the left in figure 7.

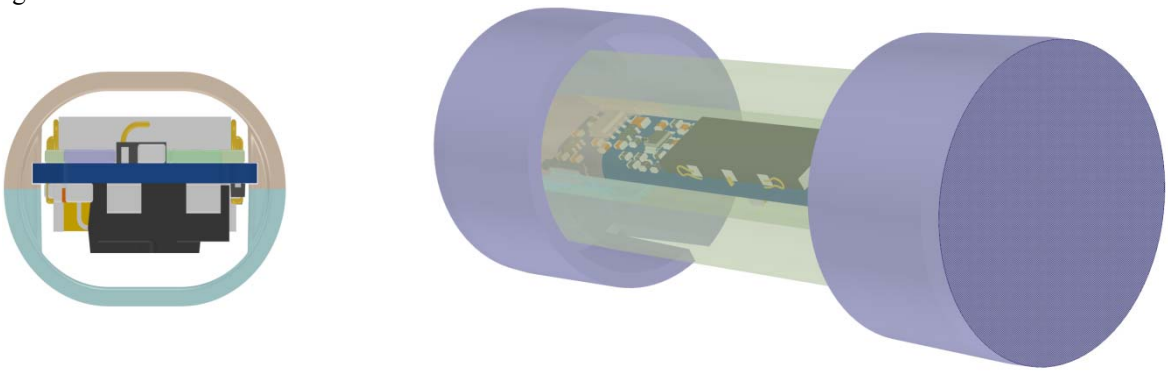

Figure 7: Left: Cross-section view of the converter surrounded by a winding-insert. Right: 3D view of the actuator with transparent DEAP material to illustrate how the converter is placed inside the actuator.

In one of the winding-inserts a set of grooves in each side provide two functions. The first function is to guide the converter straight into the actuator, when sliding in the PCB. The second function is to fix the driver in only one end of the actuator. In the opposite end the PCB is narrowed to avoid friction with the winding-insert, this ensures that the rest of the actuator can move freely. Each end of the actuator is encapsulated with an end fitting, made of plastic. A 3D view of the actuator with end-fittings is seen to the right in figure 7, were the DEAP material is transparent to illustrate how the converter is placed inside.

The physical size of the prototype driver is only 95 mm x 12.8 mm x 7.5 mm (L x W x H) and a photo of the prototype is seen in figure 8.

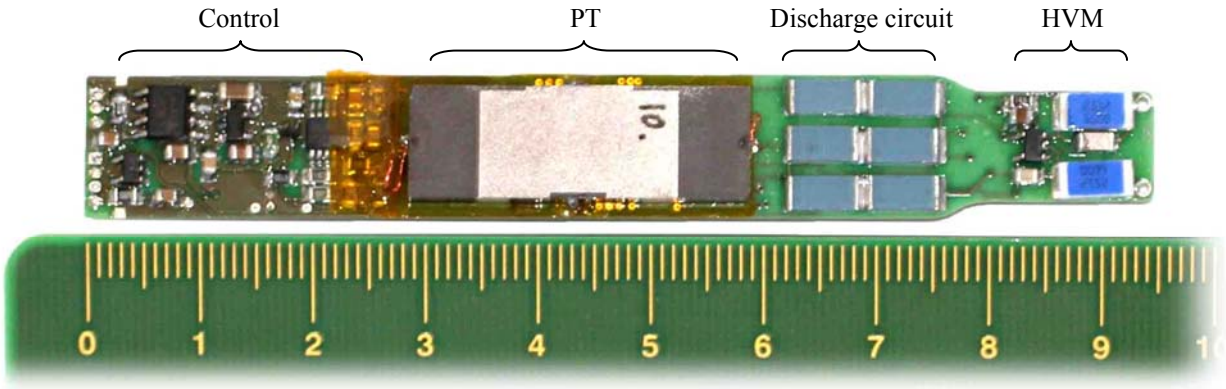

Figure 8: Prototype driver showing the control circuit, a 30 mm PT, resistive discharge array and the high voltage measurement circuit. The voltage doubler rectifier is placed on the opposite side, underneath the high voltage measurement circuit. The power stage is also placed on the opposite side of the PCB and is located underneath the PT.

The external size of the actuator is 110x32 mm and a picture of the final DEAP actuator with the integrated driver is seen in figure 9.

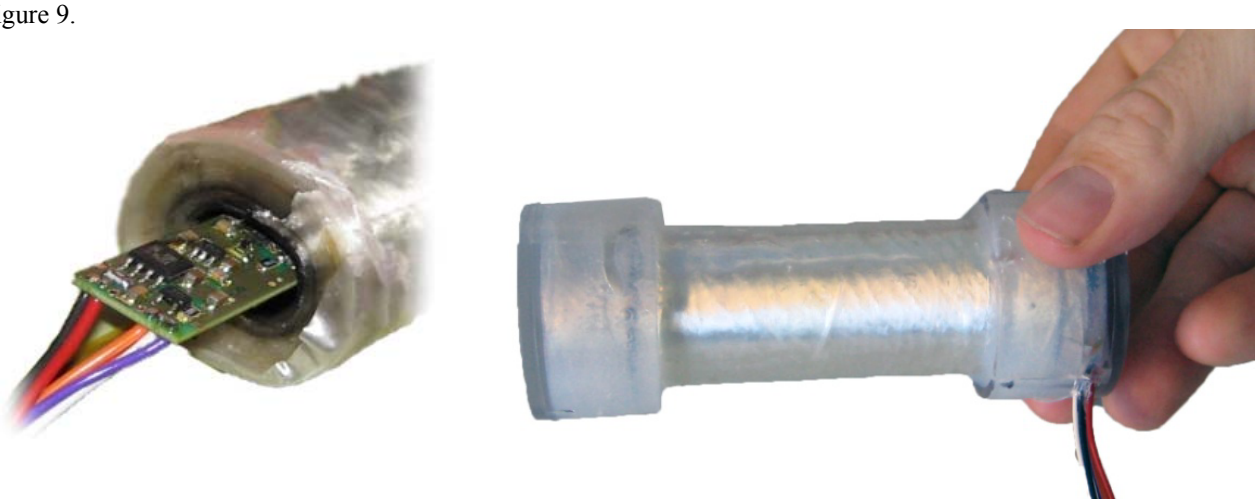

Figure 9: Left: Picture of the driver sliding into the DEAP actuator. Right: Picture of the final "low voltage" DEAP actuator.

8. EXPERIMENTAL RESULTS

8.1 High Voltage measurement

Practical experience revealed that care should be taken when selecting the high voltage capacitors (C1 & C3) referred to figure 6. Voltage dependent capacitance (DC-bias) destroys the relation in (6) and splits the transfer function for the feedback signal into a static and a dynamic gain (8). For this application ceramic multilayer capacitors are preferred because of their high volumetric capacitance, which allows small package size. The widely used ceramic for high volumetric capacitors are ferroelectric and therefore inhere strong voltage dependent capacitance. Increased capacity per volume for these capacitor types increases the voltage dependency. To avoid the voltage dependency of ceramic capacitors the ceramic type to use is paraelectricity. The main component of temperature compensation type (C0G, NP0, U2J, etc.) is paraelectricity and therefore the capacity does not vary with voltage [11].

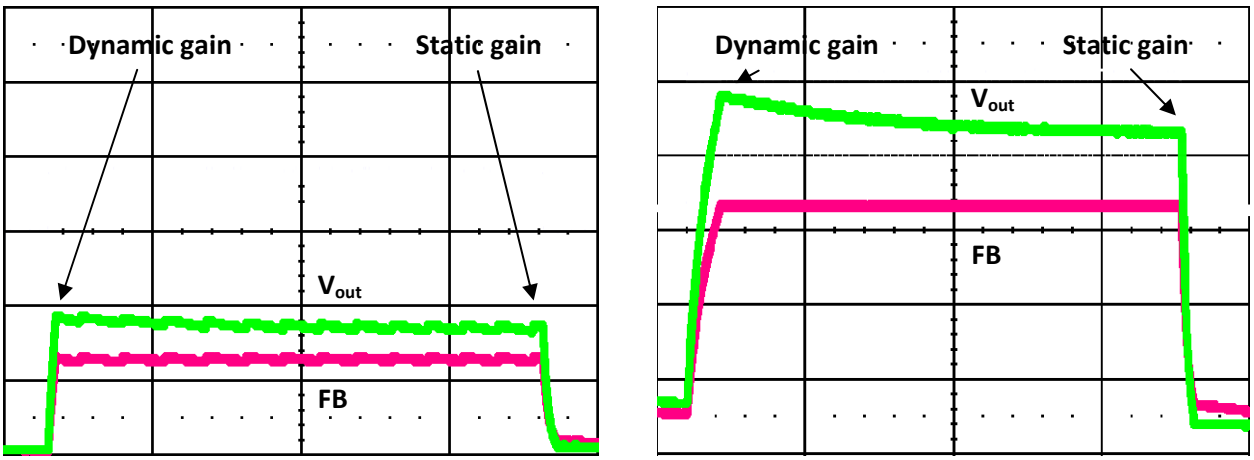

Figure 10: Measured illustration of the erroneous dynamic gain caused by non liner dielectric in HV capacitors C1, C3. Output voltage (V_{out}: 500 V/div & 500 ms/div) and the feedback signal (FB: 1 V/div & 500 ms/div) in closed loop at two different reference signals. Left: low voltage case. Right: high voltage case.

In figure 10 are the output voltage and the feedback signal measured with two different amplitude of a square wave reference input to the controller. The output voltage is adjusted by the converter so the feedback signal matched the square wave reference. C1 & C3 are both ceramic capacitors (100 pF– 2 kV) in category X7R. Table 5 compares the dynamic and static gain from the two measurements in figure 10. The dynamic gain is dominated by the capacitive voltage divider where as the static gain is dominated by the resistive divider. As the voltage increase the dynamic gain decreases because the capacitance of C1 & C3 decreases with applied voltage. This result agrees with the equation stated in (8).

$$\frac{FB}{V_{out}} = \begin{cases} \dfrac{R2}{R1+R2+R3} & \omega \to 0 \quad \text{Static} \\ \dfrac{\dfrac{1}{C2}}{\dfrac{1}{C1}+\dfrac{1}{C2}+\dfrac{1}{C3}} & \omega \to \infty \quad \text{Dynamic} \end{cases} \tag{8}$$

			Voltage	Gain	Deviation	Delta deviation
Low voltage case	Dynamic gain	V_{out}	940 V	1.43 mV/V	-4.8 %	Δ4.9
		FB	1.34 V			
	Static gain	V_{out}	860 V	1.50 mV/V	0.1 %	
		FB	1.29 V			
High voltage case	Dynamic gain	V_{out}	2405 V	1.39 mV/V	-7.1 %	Δ9.7
		FB	3.35 V			
	Static gain	V_{out}	2165 V	1.54 mV/V	2.6 %	
		FB	3.33 V			

Table 5: Comparison of dynamic and static gain in both a low and high voltage case, with voltage dependent capacities.

8.2 Control and operation

The fully functionality of the converter is demonstrated in figure 11. The left plot illustrates how the converter is capable of charging the DEAP, to a desired voltage and the keep the output voltage steady at this voltage, trough small bursts of operation.

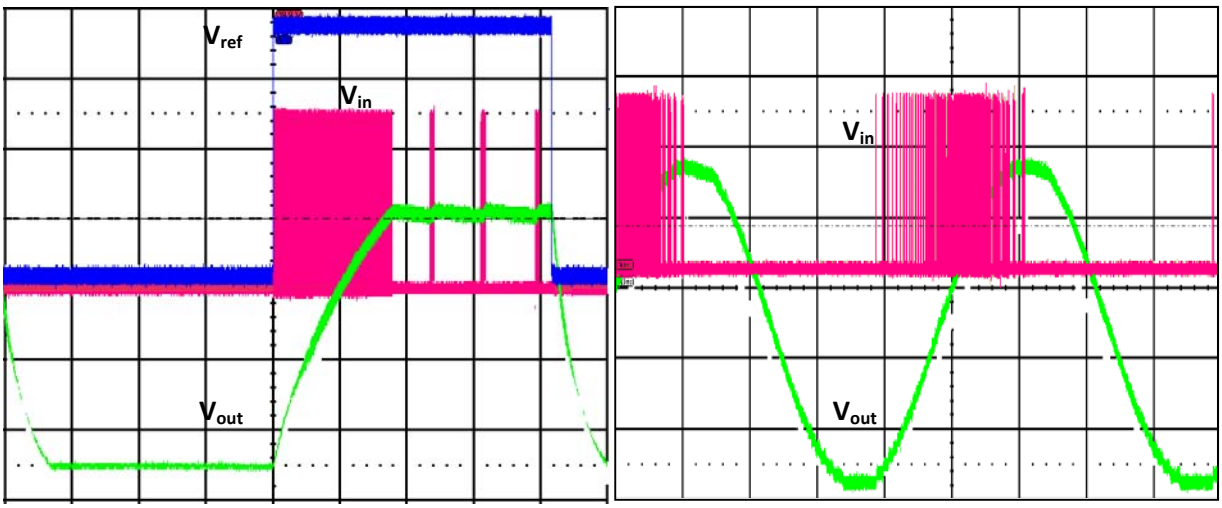

Figure 11: Measurement of the output voltage across the DEAP (green –500 V/div), reference voltage (blue – 1 V/div) and input voltage (red –10 V/div). Left: Square-wave reference signal. Time base 50 ms/div. Right: Sinusoidal reference signal. Time base 100 ms/div.

The first stage, where the DEAP is charged, the output voltage has a certain rise time, this is essential the impulse response of the converter. This is due to the limited power available from the converter, it will take some time to deliver the needed energy. In the second stage, the converter is operated in a burst mode manner. The bursts have a separation of less than 50 ms, which indicates a rapid discharge of the DEAP. This discharge is in fact caused by the oscilloscope's HV probe itself and is not a sign of a bad DEAP or HVM circuit. This is because of the impedance of the HV differential probes used, which has an impedance of 10 MΩ and accounts for a 162 mW discharge of the DEAP at 1.8 kV. Without the oscilloscope probes the only discharge of the DEAP, is caused by its own leakage, the leakage in the diodes and the HVM circuit. Without oscilloscope probes a burst-rate of 30 seconds separation has been observed. The third stage is the discharge of the DEAP and this is done trough a resistive load.
The right plot in figure 11 demonstrates how the converter is capable of following a sinusoidal reference voltage, with a frequency of approximately 2 Hz. It can be seen how the burst periods becomes denser as the slope of the output voltage increases. Furthermore the energy needed to charge the DEAP is dependent on the voltage squared, resulting in the largest burst periods at a point where the voltage and slope is high.

9. CONCLUSION

The world first low voltage DEAP solution is presented. By utilizing a piezoelectric transformer, it is succeeded to design and produce a driver small enough to be integrated into a coreless DEAP actuator. Piezoelectric transformer simulations is verified by measurements to ensure a gain, high enough to produce the needed output voltage of 2.5kV from input voltage of 24 V to fully stress the DEAP actuator.
There is a good correlation between the piezoelectric transformer prototype and finite element method simulations, concerning the gain. The correlation between the equivalent lumped parameters in general, could be improved. The presented control system only turns on the driver when necessary, in a burst-mode manner. That together with a careful design of the output stage, which minimizes the discharge current of the DEAP, the power consumption, at a static DEAP force is kept as low as possible.

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Appendix: A9

T. Andersen, M. S. Rødgaard, M. A. E. Andersen, O. C. Thomsen, K. P. Lorenzen, C. Mangeot and A. R. Steenstrup, "Integrated high voltage power supply utilizing burst mode control and its performance impact on dielectric electro active polymer actuators", accepted for Actuator, 2012.

Integrated high voltage power supply utilizing burst mode control and its performance impact on dielectric electro active polymer actuators

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Abstract:
Through resent years new high performing Dielectric Electro Active Polymers (DEAP) have emerged. To fully utilize the potential of DEAPs a driver with high voltage output is needed. In this paper a piezoelectric transformer based power supply for driving DEAP actuators is developed, utilizing a burst mode control technique. Controlling and driving a DEAP actuator between 250V to 2.5kV is demonstrated, where discrete like voltage change and voltage ripple is observed, which is introduced by the burst mode control. Measurements of the actuator strain-force reveal that the voltage ripples translates to small strain-force ripples. Nevertheless the driver demonstrates good capabilities of following an input reference signal, as well as having the size to fit inside a 110 mm x 32 mm cylindrical InLastor Push actuator, forming a "low voltage" DEAP actuator.

Keywords: Dielectric Electro Active Polymers, Driver, Power supply, Piezoelectric transformer

Introduction

The resent years emergence of new high performing DEAP materials, calls for higher performing drivers in order to fully utilize its potential. Figure 1 top illustrates the state of the art driver for driving the cylindrical InLastor Push actuator. The driver is electromagnetic transformer (EMT) based and converts the input DC voltage of 24 volt to an output voltage between 250V and 2.5kV depending on a control signal.

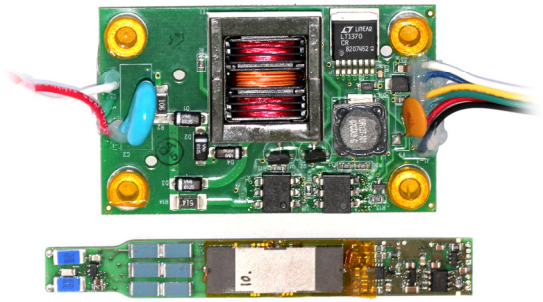

Figure 1: *Converters for driven DEAP actuators. Top: The state of the art electromagnetic (EMT) based driver. Bottom: Novel piezoelectric transformer (PT) based driver*

At the bottom of figure 1 the novel piezoelectric transformer (PT) based driver is illustrated. It utilizes an inductor less topology which enables operation in high external magnetic fields, as well as the elimination of bulky inductors reduces overall volume. The decrease in volume of the PT based driver allows the driver to be integrated into a cylindrical DEAP actuator, which is illustrated in figure 2. The benefits of integrating the driver into the DEAP are to avoid the high voltage interface. Issues regarding high voltage safety are avoided. The availability of low voltage power supplies is far greater than for high voltage.

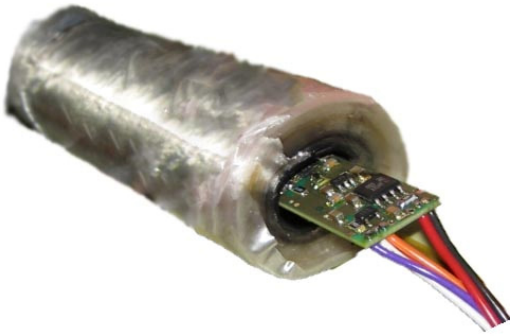

Figure 2: *Cylindrical DEAP actuator with integrated driver. The driver is pulled a bit out of the actuator for the purpose of illustration*

In this work the performance of the novel PT based driver is compared with the state of the art EMT based driver. The general design will be presented, as well as the basic operation and functionality. The efficiency and EMI performance will be compared and evaluated. Furthermore the performance of the resulting integrated cylindrical DEAP actuator is presented and evaluated.

Inductor-less PT based driver

The principle of an inductor-less PT based driver relies on a half-bridge driven PT topology [1]. The electrical equivalent of a PT, valid in the vicinity of a single resonance mode, can be modeled with the Mason lump parameter equivalent [2-4]. The Mason equivalent connected with a half-bridge is illustrated in figure 3. The capacitance C_{d1} is large, easily 100 times greater than the output capacitance of the two MOSFETs. The high capacity load on the half-bridge is a disadvantage. Each time the half-bridge voltage (V_1) is hard switched the stored energy in C_{d1} is dissipated in the MOSFETs.

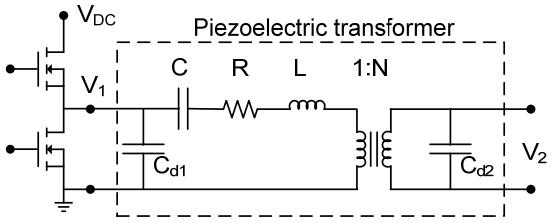

Figure 3: *Inductor-less PT topology. Half-bridge connected with the Mason equivalent model of a piezoelectric transformer*

To improve efficiency of the converter the half-bridge must be soft switched instead of hard switched. Soft switching is in this case referred to as zero voltage switching (ZVS) and occurs when the voltage across the MOSFET is zero when it turns on. ZVS can be obtained by the PT, however the PT and the control must be optimized for ZVS operation [1, 5-7].

The driver utilizes an interleaved multilayer Rosen type transformer [8], which is ZVS optimized. Figure 4 sketches the structure of the PT and the polarization directions and for simplification only two primary layers are shown.

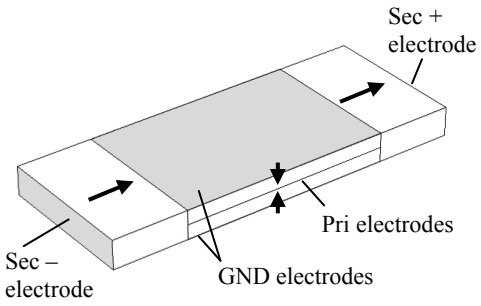

Figure 4: *The interleaved multi layer Rosen-type PT structure, where the arrows indicate the polarization direction. Size: 30mm x 10mm x 2mm*

The secondary sections of the transformer are polarized in the same direction. Thereby the output voltage of the two secondary electrodes is 180 degrees out of phase, which increase the gain of the transformer. The equivalent model of the PT is illustrated in figure 5. To further increase the overall step-up ratio of the converter a voltage doubler rectifier circuit is utilized at the output of the PT [9, 10]. However a three diode version is used instead of the standard two diode solution. This is necessary for the ground referred output voltage feedback circuit to work correctly, as well as avoiding a large common mode voltage signal over the actuator.

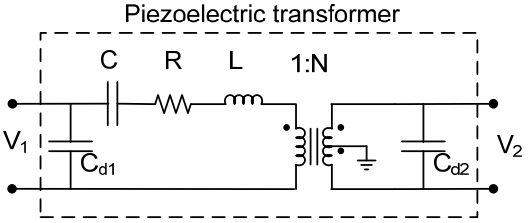

Figure 5: *Electrical equivalent of the interleaved Rosen type transformer, with both secondary sections polarized in the same direction*

To ensure high efficiency of the converter a inner closed-loop control circuit similar to [11] is used to maintain ZVS operation of the PT. An outer closed-loop is controlling the output voltage in a bust mode (quantum-mode) manner [11-13]. Feedback from the output voltage across the DEAP actuator closes the outer loop. Decrease of the output voltage is done by discharging the DEAP actuator through a resistive network. Figure 6 illustrates the driver with the DEAP connected.

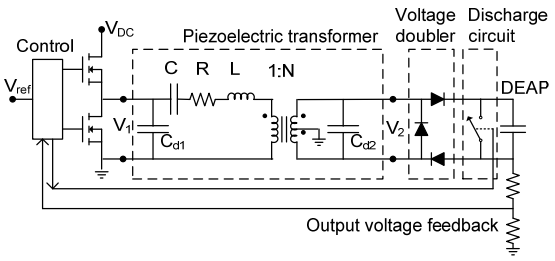

Figure 6: *Block diagram of inductor-less PT converter with voltage doubler rectifier, discharging circuit and DEAP actuator connected*

A reference signal (V_{ref}) is controlling the voltage across the DEAP actuator. When the output voltage feedback is below the reference signal the driver is turned on. When the output voltage feedback is above the reference signal the driver is turned off and the discharging circuit is turned on.
With a constant reference signal, the driver will charge the DEAP to the output voltage corresponding to the reference signal and then turn off the driver. The DEAP will retain the output voltage, however leakage current within the DEAP and the diodes together with the current drawn by

the output voltage feedback circuit is slowly discharging the DEAP. When the DEAP is discharge below a certain lower threshold of the reference signal, the driver is turned on again to charge the DEAP until a certain upper threshold of the reference signal. This control method is referred to as burst mode control. Figure 7 shows an oscilloscope plot of the PT driver in action. Notice that the voltage of the DEAP is attenuated by 1000 times. The time between each burst is determined by the discharge rate of the DEAP and the hysteretic window around the reference signal. The time length of each burst is controlled by adjusting the hysteretic window around the reference signal. The size of the hysteretic window is a trade-off between efficiency and output voltage ripple. As the hysteretic window goes towards zero the burst frequency and burst time length goes towards zero, decreasing the output voltage ripple. However efficiency will drop as the time length of each burst decreases. The explanation is that it takes time to build up the necessary resonance current within the PT for ZVS operation. Every start-up of the PT is therefore very inefficient compared to ZVS operation.

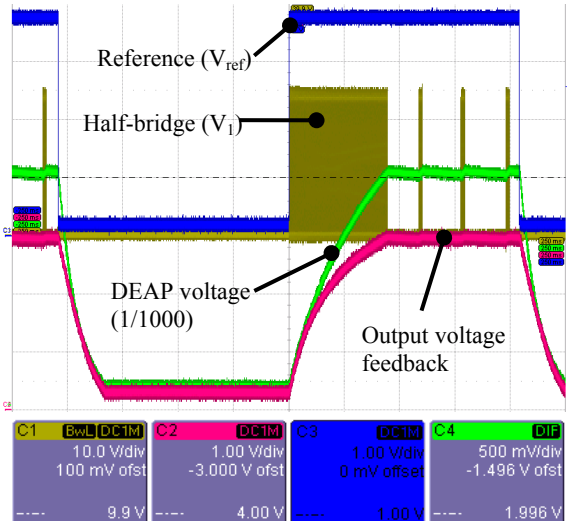

Figure 7: *Oscilloscope plot of the PT based driver with a square wave reference signal. Burst mode control of the half-bridge is observed. DEAP voltage is attenuated by x1000*

Driver performance

In this section the electrical properties of the PT based driver is compared to the state of the art EMT based driver.

Efficiency

The efficiency of the driver is defined as the ratio between energy stored in the DEAP and energy delivered to the driver (1). Figure 8 shows the used setup for measure the efficiency of the two drivers. Prior to the measurement output is discharged to zero volt. The input voltage is 24 volt and the DEAP is substituted with a fixed capacitance of 47nF. The input current is measured as the output capacity is charged from zero to 1.9kV.

$$\eta = \frac{E_{DEAP}}{E_{input}} = \frac{0.5 \cdot C_{DEAP} \cdot V_{DEAP}^2}{\int V_{DC} \cdot I_{in} \cdot dt} \qquad (1)$$

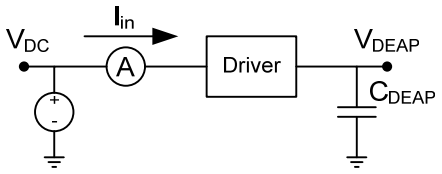

Figure 8: *Setup for measure efficiency of the driver*

The measured input current for the PT based and EMT based driver is plotted in figure 9. When the output voltage reached 1.9kV the control circuit turns off the half-bridge stage and the input current drops sudden and only auxiliary current consumption is left.

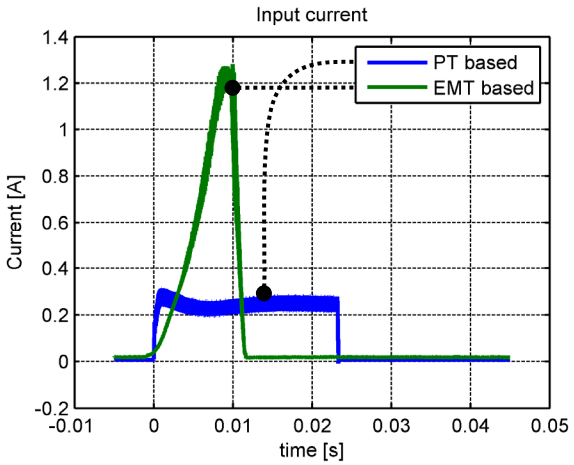

Figure 9: *Measurement of input current while charging the output voltage from 0V to 1.9kV*

From the measured input current and the definition (1) is the efficiency calculated for both drivers, see table 1.

Driver type:	E_{input} (24V)	E_{DEAP} (47nF)	Efficiency
PT based	138mJ	81.2mJ	58.8%
EMT based	182mJ	82.4mJ	45.3%

Table 1: *Efficiency of PT based and EMT based driver*

$$PT_{loss\,reduction} = \frac{E_{loss,EMT} - E_{loss,PT}}{E_{loss,EMT}} = 41\% \qquad (2)$$

The energy loss for PT based driver is reduced by 41% compared to the EMT based driver (2).

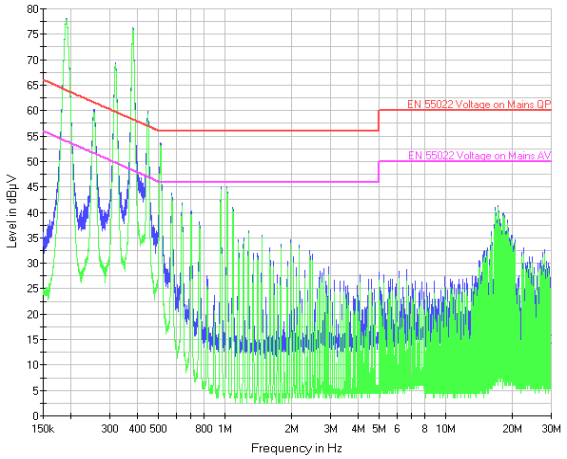

Figure 10: *EMI measurement of PT based driver at 4 watts output power*

EMI

As the PT based driver does not contain any magnetic components, the emitted magnetic fields are expected to be low. But this also means that the driver has no input filter to suppress the fundamental switching frequency. As the PT based driver is a soft switched resonance converter, the general EMI performance is expected to be good.

The setup used for the measurement the conducted EMI is illustrated in figure 11. The LISN network is connected to an EMC receiver. The utilized EMC receiver requires a steady state operation of the device under test in order to measure the EMI correct. The driver is therefore loaded with a resistive load (R_L) instead of a capacitive load.

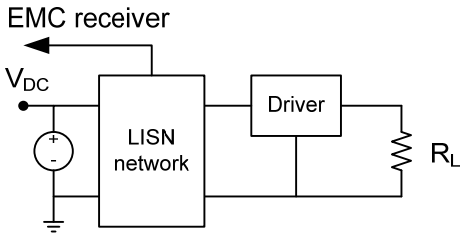

Figure 11: *Setup for measure conducted EMI*

The result of the EMC receiver is shown in figure 10 and figure 12 for the PT based and the EMT based driver respectively. Both measurements are performed with an output power of 4 watts. None of the drivers have any dedicated EMI filtering. As expected both drivers lacks the ability to suppress fundamental frequencies with a peak of around 80dBµV. However the PT based driver performs well in the high frequency region (above 1MHz) with a ≈25dBµV decrease between the peak values compared with the EMT based driver.

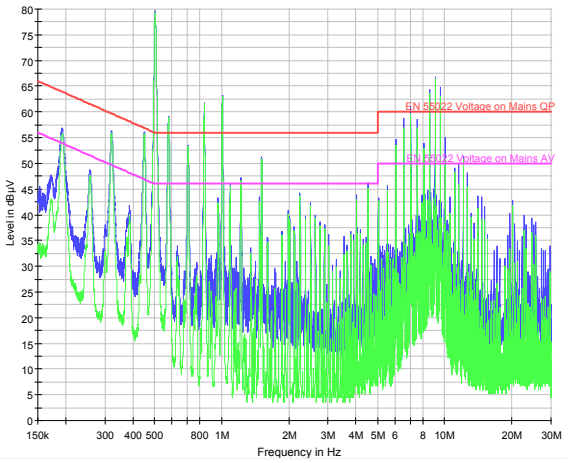

Figure 12: *EMI measurement of EMT based driver at 4 watts output power*

DEAP performance with integrated driver

The mechanical performance of the integrated DEAP actuator is evaluated trough a Stroke-Force measurement. The measurement is performed by prevent the movement of the actuator, when applying the voltage. The actuator is then slowly released, while the force and stroke is measured. Stroke-Force measurements of the DEAP actuator, with and without driver integration, are shown in figure 13.

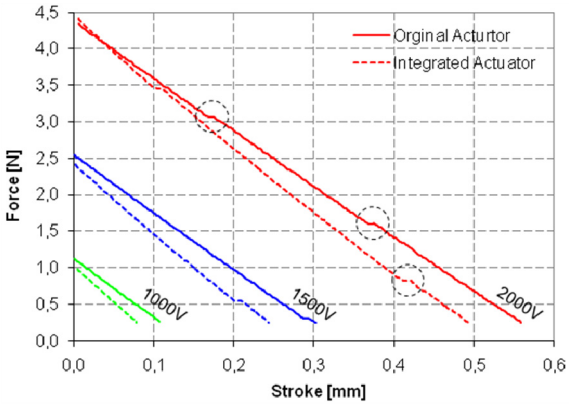

Figure 13: *Stroke-Force measurement of the DEAP actuator, with and without driver integration, at different DEAP voltages*

It can be seen that the integration do decrease the stroke performance somewhat. Approximately 12% decrease in stroke. This is due to increased tension and friction, as the PCB is attached in one end of the actuator and is sliding in a slot in the other end. Furthermore small jumps can be observed on the measurements. This is small burst from the driver, as the voltage drops due to the increase in capacitance, as the film is getting thinner. The driver will counteract this drop as it will maintain a constant output voltage.

Conclusion

The basic structure and operational functionality of the novel PT based DEAP actuator driver are presented in this work. Furthermore the performance is compared with the state of the art EMT based driver, as well as the performance of the resulting integrated DEAP actuator is evaluated. The PT based driver demonstrated a 14% point increase in efficiency, compared to the EMT based driver, resulting in a 41% loss reduction. The EMI performance of the PT based driver showed a good improvement of 25dBµV in the high frequency region (above 1MHz). Finally the resulting integrated cylindrical DEAP actuator demonstrated full functionality, with approximately 12% decrease in stroke performance, compared to the original actuator.

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Appendix: A10

M. A. E. Andersen, K. S. Meyer, M. S. Rødgaard and **T. Andersen**, "Piezoelectric power converter with bi-directional power transfer", Patent, US application no. US61/567,924, and EU application no. EP11192356, 2011.

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U.S. PROVISIONAL PATENT APPLICATION

FOR

PIEZOELECTRIC POWER CONVERTER WITH BI-DIRECTIONAL POWER TRANSFER

BY

MICHAEL ANDREAS ESBERN ANDERSEN

KASPAR SINDING MEYER

MARTIN SCHØLER RØDGAARD

AND

THOMAS ANDERSEN

PIEZOELECTRIC POWER CONVERTER WITH BI-DIRECTIONAL POWER TRANSFER

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FIELD OF THE PRESENT DISCLOSURE

[0002] The present invention relates to a bi-directional piezoelectric power converter comprising a piezoelectric transformer. The piezoelectric transformer comprises an input electrode electrically coupled to a primary section of the piezoelectric transformer and an output electrode electrically coupled to an output section of the piezoelectric transformer to provide a transformer output signal. A bi-directional switching circuit is coupled between the output electrode and a DC or AC output voltage of the power converter. Forward and reverse current conducting periods of the bi-directional switching circuit is based on the input drive signal or the transformer output signal such that a forward current is conducted from the output electrode through the bi-directional switching circuit to the DC or AC output voltage in a first state to charge the DC or AC output voltage. In a second state, a reverse current is conducted through the bi-directional switching circuit from the DC or AC output voltage to the output electrode to discharge the DC or AC output voltage and return power to the primary section of the piezoelectric transformer.

BACKGROUND

[0003] Traditional piezoelectric transformer based power converters are only capable of supplying power in one direction, from an input voltage/power source to a DC or AC output of the power converter. Furthermore, the piezoelectric transformer is normally operated in a narrow frequency band around its fundamental or primary resonance frequency with a matched load coupled to the output of the piezoelectric transformer. This is required to optimize power conversion efficiency of the power converter. The small optimum frequency band of operation and the need for a matched load make it difficult to provide output voltage regulation without sacrificing

efficiency of the piezoelectric based power converter. Instead of transferring surplus power to the load coupled to the secondary side of the power converter, the present power converter enables reverse transmission of power back to the input source to conserve energy.

[0004] Likewise in situations where the excitation frequency is substantially fixed, traditional output voltage control techniques based frequency modulation or pulse width modulation of the input drive signal cannot easily be adapted to control a DC or AC output voltage of the converter without causing considerable deterioration of the power conversion efficiency of the power converter.

[0005] Another challenge in the design of traditional piezoelectric transformer based power converters is to obtain zero-voltage-switching (ZVS) in an input driver, typically based on a half-bridge or full-bridge MOS transistor circuit, coupled to a primary or input section of the piezoelectric transformer. ZVS operation of piezoelectric transformers has traditionally been achieved by adding an external inductor in series or in parallel with the primary or input section of the piezoelectric transformer. The external inductor ensures that the input of the piezoelectric transformer appears inductive across a certain frequency range and such that an output node of the input driver can be charged/discharged in accordance with the input drive signal without inducing prohibitive power losses. However, the external inductor occupies space, adds costs and conducts and radiates EMI in the power converter. It would therefore be advantageous to provide a piezoelectric transformer based power converters capable of ZVS operation with good power conversion efficiency without the ordinary external inductor. ZVS operation of piezoelectric transformers is supported in accordance with one aspect of the invention by increasing an apparent ZVS factor of piezoelectric transformer of a power converter by conducting reverse current from the DC or AC output voltage to the secondary section of the piezoelectric transformer as described in further detail below. This methodology increases the apparent ZVS factor of a piezoelectric transformer which can be useful to transform a piezoelectric transformer design or construction without inherent ZVS capability to one with ZVS capability. In addition, even piezoelectric transformer designs with inherent ZVS capability, i.e. a ZVS factor above 100 %, can benefit from a further increase of apparent ZVS factor because it enlarges or broadens the frequency band supporting ZVS operation.

SUMMARY

[0006] A first aspect of the invention relates to a bi-directional piezoelectric power converter comprising:

- a piezoelectric transformer comprising an input electrode electrically coupled to an input or primary section of the piezoelectric transformer and an output electrode electrically coupled to secondary or output section of the piezoelectric transformer to provide a transformer output signal. An input driver of the bi-directional piezoelectric power converter is electrically coupled to the input electrode and arranged to supply an input drive signal with a predetermined excitation frequency to the input electrode. A bi-directional switching circuit is coupled between the output electrode and an output voltage of the converter and a controller is adapted to control first and second states of the bi-directional switching circuit based on the input drive signal or the transformer output signal such that:
- in a first state, forward current is conducted from the output electrode to the output voltage through the bi-directional switching circuit during a first period of a cycle time of the transformer output signal to charge the output voltage,
- in a second state, reverse current is conducted from the output voltage to the output electrode through the bi-directional switching circuit during a second period of the cycle time of the transformer output signal to discharge the output voltage and return power to the primary section of the piezoelectric transformer.

[0007] The presence of the second state wherein reverse current is conducted from the output voltage through the bi-directional switching circuit to the output electrode allows effective output voltage regulation without sacrificing efficiency of the piezoelectric based power converter because power is returned to the primary section of the piezoelectric transformer. The transmission of reverse current during the second period of the cycle time exploits an inherent bi-directional power transfer property of piezoelectric transformers such that power is transferred in opposite direction to the ordinary, i.e. forward, power flow in the power converter. Surplus power at the output voltage is transmitted back to the input power source such as a DC supply voltage supplying power to the input driver. According to a preferred embodiment of the invention, the controller is in the second state further configured to control the switching circuit such that both forward current and reverse current is conducted during a single cycle of the transformer output signal. In this embodiment the forward current is conducted during the first period of the

cycle time and reverse current is conducted during the second period of the same cycle of the transformer output signal. The second period may have a length corresponding to about one-half or less than the cycle time cycle time of the transformer output signal. The skilled person will appreciate that the degree of charge or discharge of the output voltage may be controlled in a step-wise or substantially continuous manner by a corresponding control of the relative length between the first and second periods of the same cycle of the transformer output signal. In this manner, the controller may provide effective output voltage control through adjustment of the length of the second period of the cycle time. Accordingly, by appropriately balancing the length of the first period of the cycle time relative to the second period of the same cycle, the bi-directional piezoelectric power converter may be adapted to transfer net power to the output voltage or to a load coupled thereto, transfer substantially zero power to the output voltage or transfer a negative power to the output voltage. The skilled person will understand that if the controller sets the length of the second period of the cycle time to zero, the bi-directional piezoelectric power converter conveniently transits from the second state to the first state wherein the bi-directional switching circuit conducts solely forward current so as to charge the output voltage during the first periods of the cycle times. This leads to an increasing level of output voltage e.g. the output voltage becomes more positive or more negative depending on the polarity configuration of the bi-directional switching circuit. In general, the controller may be adapted to terminate the second period of the cycle time, i.e. terminating the reverse conduction of current through the switching circuit, synchronously or asynchronously to the input drive signal or the transformer output signal. The controller preferably comprises an adjustable time delay circuit providing an adjustable duration of the second period of the cycle time of the transformer output signal such that the amount of reverse power can be controlled. The controller is preferably configured to derive a synchronous state control signal from the input drive signal and apply the synchronous state control signal through the adjustable time delay circuit to a switch control terminal of a second controllable semiconductor switch and/or a switch control terminal of the first controllable semiconductor switch of the switching circuit to control respective states of the first and second controllable semiconductor switches. In this manner, the switching circuit is responsive to the synchronous state control signal indicating the termination of the second period of the cycle time. The skilled person will understand that the synchronous state control signal may be derived directly or indirectly from the input drive signal. Indirectly if the synchronous state control signal

is derived from another signal in the power converter that is synchronous to the input drive signal such as the transformer output signal. In one such embodiment, the synchronous state control signal is derived from a zero-crossing detector embedded in a self-oscillating feedback loop enclosing input section of the piezoelectric transformer.

[0008] According to a preferred embodiment of the invention, the controller is adapted to sense a current through, or a voltage across, an electrical component of the bi-directional switching circuit. The controller initiates the forward current conduction in the first period of the cycle time in response to a sensed current or voltage so as to asynchronously initiate the forward current conduction. This embodiment simplifies the generation of an appropriately timed control signal or signals for the controller to the bi-directional switching circuit because the forward current conduction is automatically started without any need for a synchronous signal to indicate the correct phase of the transformer output signal. The electrical component may comprise a transistor, a diode or a resistor. In one embodiment, the electrical component comprises a series resistor coupled is series with a semiconductor diode coupled between the transformer output voltage and the output voltage. In this embodiment, the controller may be adapted to detect a flow of forward current by monitoring the polarity of a voltage drop across the series resistor since this polarity indicates the direction of current flow from the transformer output electrode to the output voltage. The flow of forward current through the switching circuit automatically starts when the transformer output signal exceeds the output voltage with approximately one diode voltage drop.

[0009] The predetermined excitation frequency is preferably selected or adjusted to a frequency which proximate to, or slightly above, a fundamental resonance frequency of the piezoelectric transformer depending on how the input driver is coupled to the input electrode of the primary section of the piezoelectric transformer. If the input driver is coupled to the primary section through a series/parallel inductor, the predetermined excitation frequency is preferably placed in proximity of the fundamental resonance frequency. The series/parallel inductor is adapted to provide so-called zero voltage switching (ZVS operation) of the input driver. If the input driver on the other hand is directly coupled to the input electrode of the piezoelectric transformer, i.e. without any series/parallel inductor, the predetermined excitation frequency is preferably placed within a selected frequency band or range placed slightly above the fundamental resonance frequency where the piezoelectric transformer may exhibit an intrinsic inductive input

impedance, i.e. possess a ZVS factor larger than 100 % such as larger than 120 % according to the below defined definition of the ZVS factor. The inductive input impedance in the selected frequency band or range enables ZVS operation of the input driver even in the first state of the bi-directional switching circuit so as to eliminate switching losses in the input driver. The setting of the predetermined excitation frequency depends on the fundamental resonance frequency of the piezoelectric transformer which may vary widely depending on its mode of operation and its physical dimensions. However, in a number of useful embodiments, the predetermined excitation frequency lies between 40 kHz and 1 MHz such as between 50 kHz and 200 kHz.

[0010] The bi-directional switching circuit preferably comprises one or more controllable semiconductor switches adapted to conduct the forward current from the output electrode to the output voltage during the first period of the cycle time. The one or more controllable semiconductor switches likewise conducts reverse current from the output voltage to the output electrode in the second state. The one or more controllable semiconductor switches preferably comprise(s) a semiconductor selected from the group of {MOSFET (metal-oxide-semiconductor field effect transistor), IGBT (insulated-gate bipolar transistor), bipolar transistor, Gate Turn-off thyristor (GTO)}. According to a preferred embodiment, each of the one or more controllable semiconductor switches preferably comprises a MOS transistor, such as a NMOS (n-channel metal oxide semiconductor) transistor, which is capable of bi-directional current flow between its source and drain terminals with a small on-resistance during both forward and reverse current conduction. The on-states and off-states of each of the MOS transistors are controllable by appropriate control of the drive voltage on a gate terminal of the MOS transistor. One embodiment based on the one or more controllable semiconductor switches comprises a first controllable semiconductor switch arranged between the output electrode and the output voltage and a second controllable semiconductor switch arranged between the output electrode and a negative supply voltage. The negatives supply voltage may be ground reference of the power converter. The controller is configured to alternatingly switch the first and second controllable semiconductor switches to respective on-states and off-states in a non-overlapping manner to control the forward and reverse current conduction. In the first state, this embodiment provides half-wave rectification of the transformer output signal by conducting the forward current to the output voltage through the first controllable semiconductor switch when transformer current out of the output electrode is positive. When the transformer current out of the output electrode is negative the second control-

lable semiconductor switch conducts and circulates current through the secondary side of the piezoelectric transformer. The skilled person will understand that the bi-directional switching circuit may comprise a full-wave rectification circuit such that a third controllable semiconductor switch is arranged between a second output electrode of the secondary side of the piezoelectric transformer and the output voltage and a fourth controllable semiconductor switch arranged between the second output electrode and the negative supply voltage.

[0011] According to an embodiment of the bi-directional piezoelectric power converter, the bi-directional switching circuit further comprises a first semiconductor diode coupled across inlet and outlet nodes of the first controllable semiconductor switch, e.g. drain and source terminals of the MOS transistor, to conduct forward current to the output voltage during at least a portion of a first period of the cycle time. A second semiconductor diode may be coupled across inlet and outlet nodes of the second controllable semiconductor switch, e.g. drain and source terminals of another MOS transistor, to conduct current during at least a portion of the cycle time of the transformer output signal. The first semiconductor diode or the second semiconductor diode may comprise a body/substrate diode integrally formed with the first or the second semiconductor switch, respectively. This reduces semiconductor substrate area consumption on a semiconductor die or substrate onto which the power converter may be integrated.

[0012] The on-set of flow of forward current through the first semiconductor diode is a convenient detection mechanism for the controller to asynchronously determine when the first controllable semiconductor switch must be switched to its on-state. In this manner, the controller may be configured to sense the forward current through, or the forward voltage across, the first semiconductor diode; and switch the first controllable semiconductor switch to its on-state in response to a sensed forward current or voltage so as to actively clamp the first semiconductor diode during the first period of the cycle time. In this manner, the first semiconductor diode conducts forward current to the output voltage during the portion of the first period of the cycle time and the first controllable semiconductor switch conducts the forward current during a major portion of the first period of the cycle time due to its lower impedance/forward voltage drop once activated.

[0013] According to another preferred embodiment of the invention, the controller comprises a self-powered driver coupled between the switch control terminal of the first controllable semiconductor switch and the output electrode of the output section. Furthermore, the self-

powered driver comprises a timer circuit configured to control the state of the first semiconductor switch in accordance with a timer period setting wherein the timer period setting is based on the cycle time of the transformer output signal. The termination of the second period of the cycle time is therefore controlled by the timer period setting rather than the previously discussed synchronous state control signal. The coupling of the self-powered or autonomous driver allows the driver to float and follow an instantaneous voltage of output electrode of the piezoelectric transformer. Since the instantaneous voltage of output electrode may rise to a level of several hundred volt or even several kilovolt for high-voltage piezoelectric power converters the lack of any need for supplying a switch control signal at the same voltage level to the self-powered driver for terminating the second period of the cycle time is a significant advantage. The self-powered driver preferably comprises a local energy storage component supplying power to the self-powered driver and a rectifying element is coupled between the local energy storage component and a power supply voltage of the power converter to energize the local energy storage component. The local energy storage component may comprise a capacitor or a rechargeable battery that is charged or energized during time intervals wherein the instantaneous voltage at output electrode is relatively small such as below a DC supply voltage of the power converter. The DC supply voltage may be a positive DC supply voltage between 10 and 50 volt such as about 24 volt. During time intervals wherein the instantaneous voltage at output electrode has a high magnitude such as above a positive DC supply voltage or below a negative DC supply voltage of the power converter, the local energy storage component is charged and delivers a local supply voltage to the self-powered driver including the timer circuit allowing these to operate as described above. The rectifying element preferably comprises a high-voltage diode having a break-down voltage larger than 200 V, or more preferably larger than 500 V or larger than 1000 V. In the latter embodiment, the high-voltage diode is preferably the only galvanic connection between the self-powered driver and the power supply voltages or rail of the power converter. The high-voltage diode is reverse biased during time intervals where the instantaneous voltage at output electrode has a high magnitude as described above such that the local energy storage component is the exclusive source of power for the self-powered driver during such time intervals. In one embodiment, the self-powered driver is configured to start the timer in response to a change of bias state of the rectifying element. Consequently, when the instantaneous voltage at output electrode exceeds the local supply voltage, the timer automatically initiates the second period of the cycle

time and sets this period substantially equal to the timer period setting. The timer period setting is preferably equal to 50 % of the cycle time of the transformer output signal but may be less in other embodiments such as less than 20 % or 10 % of the cycle time of the transformer output signal.

[0014] Power converters are often required to provide a specified or target AC or DC voltage as the output voltage within certain bounds or limits which generally require voltage regulation at the load. The present piezoelectric power converter is capable of providing output voltage regulation without sacrificing power conversion efficiency by transferring power back to the input energy source during the second period of the cycle time where the output voltage is discharged as previously described. The controller may be configured to control the switching between the first and second states of the bi-directional switching circuit based on a difference between the output voltage and a predetermined AC or DC reference voltage where the latter is the target AC or DC voltage. If the AC or DC reference voltage is larger than the current output voltage of the piezoelectric power converter, the controller may adapt the bi-directional switching circuit to exclusively operate in the first state to increase the output voltage. On the other hand if the current output voltage of the piezoelectric power converter is smaller the AC or DC reference voltage, the controller may adapt the bi-directional switching circuit to operate in the second state to decrease or discharge the output voltage during the second time periods of the cycle time and at the same time return power to the input power source through the primary section of the piezoelectric transformer.

[0015] In one embodiment, the predetermined excitation frequency of the input drive signal is set by a self-oscillating feedback loop arranged around the input driver and the piezoelectric transformer. The use of the self-oscillating feedback loop to set the predetermined excitation frequency or excitation frequency has considerable advantages because the excitation frequency automatically tracks changing characteristics of the piezoelectric transformer itself and electronic circuitry of the input driver. These characteristics will typically change across operation temperature and age of the piezoelectric power converter, but the feedback loop ensures such changes are tracked by the excitation frequency so as to maintain the excitation frequency at an optimum frequency or within an optimum frequency band. The optimum frequency band may be a frequency range wherein the piezoelectric transformer exhibits inductive behaviour with a ZVS factor higher than 100 % such that ZVS operation of the input driver can be achieved

even in the first state of the bi-directional switching circuit. In one embodiment the self-oscillating feedback loop comprises an adjustable time delay configured to adjust a phase response of the self-oscillating feedback loop whereby the predetermined excitation frequency is adjusted. . This is particularly useful in connection with the present bi-directional piezoelectric power converter wherein the impedance characteristics of the piezoelectric transformer changes at and proximate to the fundamental resonance frequency in response to the level of reverse power transmission. When reverse power is transmitted through the power converter, e.g. during the second state of the bi-directional switching circuit, the excitation frequency set by the self-oscillating feedback loop decreases and the ac resonance current in the piezoelectric transformer increases. This effect can be detected by a resonance current control circuit and compensated by an appropriate adjustment of the delay of the adjustable time delay such that an optimal operation point of the self-oscillating feedback loop can be maintained during both forward power transmission and reverse power transmission of the bi-directional piezoelectric power converter.

[0016] A second aspect of the invention relates to a piezoelectric power converter comprising:

- a piezoelectric transformer comprising an input electrode electrically coupled to an input or primary section of the piezoelectric transformer and an output electrode electrically coupled to secondary or output section of the piezoelectric transformer to provide a transformer output voltage,
- an input driver electrically coupled directly to the input electrode and arranged to supply an input drive signal to the input electrode,
- a feedback loop operatively coupled between the output electrode of the piezoelectric transformer and the input driver to provide a self-oscillation loop around the input section of the piezoelectric transformer oscillating at an excitation frequency. The electrical characteristics of the feedback loop are preferably configured to set the excitation frequency of the self-oscillation loop within a ZVS operation range of the piezoelectric transformer.

[0017] The piezoelectric power converter according to this second aspect of the invention benefits from the above-described advantages of the self-oscillating feedback loop arranged around the input driver and the piezoelectric transformer. The piezoelectric transformer preferably has a zero-voltage switching factor (ZVS factor) larger than 1.0 or 100 %, preferably larger than 1.2 or 120%, such as larger than 1.5 or 150%, or larger than 2.0 or 200 %;

[0018] in which the ZVS factor is determined at a matched load condition as:

$$ZVS = \frac{k_{eff\_S}^{-2} - 1}{k_{eff\_P}^{-2} - 1}\ 0.882 \quad (1)$$

[0019] k_{eff_P}, being a primary side effective electromechanical coupling factor of the piezoelectric transformer,

[0020] k_{eff_S}, being a secondary piezoelectric transformer effective electromechanical coupling factor, in which:

$$k_{eff\_P} = \sqrt{1 - \frac{f_{res\_p}^2}{f_{anti-res\_p}^2}} \qquad k_{eff\_S} = \sqrt{1 - \frac{f_{res\_s}^2}{f_{anti-res\_s}^2}}$$

[0021] f_{res_p} = a minimum magnitude of an impedance function at the input electrode of the piezoelectric transformer with shorted first and second output electrodes,

[0022] $f_{anti\_res\_p}$ = a maximum magnitude of the impedance function at the input electrode of the piezoelectric transformer with shorted first and second output electrodes,

[0023] f_{res_s} = a minimum magnitude of the impedance function at the first and second output electrodes of the piezoelectric transformer with shorted input electrodes,

[0024] $f_{anti\_res\_s}$ = a maximum magnitude of the impedance function at the first and second output electrode of the piezoelectric transformer with shorted input electrodes.

[0025] A third aspect of the invention relates to a method of increasing an apparent ZVS factor of a piezoelectric transformer of a power converter. The method comprising steps of:

- applying an input drive signal with a predetermined excitation frequency to an input electrode of the piezoelectric transformer,
- providing a bi-directional switching circuit coupled between a secondary or output section of the piezoelectric transformer and an output voltage of the power converter,
- conducting, in a first state, forward current from the output section to the output voltage through the bi-directional switching circuit during a first period of a cycle time of the transformer output signal to charge the output voltage,

- conducting, in a second state, reverse current from the output voltage to the output section through the bi-directional switching circuit during a second period of the cycle time of the transformer output signal to discharge the output voltage,
- adjusting the apparent ZVS factor of the piezoelectric transformer by adjusting a length of the second period of the cycle time.

[0026] As described above, when reverse power is transmitted through the power converter during the second period of the cycle time of the transformer output signal, the ac resonance current in the piezoelectric transformer increases in response thereto such that it appears more inductive as seen from the input driver coupled to the primary side of the piezoelectric transformer. The increase of apparent transformer input inductance is caused by the increasing energy storage capability of the piezoelectric transformer. This increase of apparent inductance of the piezoelectric transformer is highly useful to reduce the overall size and EMI radiation of the piezoelectric power converter. The higher apparent inductance of the piezoelectric transformer itself allows the input driver to be coupled directly to input electrode of the primary section without any of the normally used series or parallel inductors and still maintain zero-voltage switching conditions in the input driver, i.e. ZVS operation. Thereby, the present methodology of increasing the apparent ZVS factor of the piezoelectric transformer, and the corresponding bi-directional piezoelectric power converter, can utilize piezoelectric transformer types without native ZVS capability, i.e. having a ZVS factor below 100 %, and still allow ZVS operation of the input driver. The length of the second period of the cycle time may accordingly be adjusted to a value which provides ZVS operation of the input driver during operation of the power converter in the second state of the switching circuit.

[0027] A preferred embodiment of the present methodology comprises a further step of:

- conducting both forward current and reverse current during a single cycle of the transformer output signal. As previously explained, the net power transferred to the output voltage may be controlled in either a step-wise or in a substantially continuous manner by a corresponding control of the relative length between the first and second periods of the same cycle of the transformer output signal such that energy efficient and accurate output voltage regulation is possible. Since the amount of reversely transmitted power or energy through the piezoelectric transformer can be varied by adjusting the length of the second period of the cycle of the transformer output

signal the apparent ZVS factor of the piezoelectric transformer can be efficiently and accurately controlled.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] Preferred embodiments of the invention will be described in more detail in connection with the appended drawings, in which:

[0029] Fig. 1 is a schematic block diagram of a bi-directional piezoelectric power converter in accordance with a first embodiment of the invention,

[0030] Fig. 2 is a schematic block diagram of a self-powered high-side driver for a bi-directional piezoelectric power converter,

[0031] Fig. 3 is a schematic block diagram of a bi-directional piezoelectric power converter in accordance with a second embodiment of the invention,

[0032] Figs. 4a) – d) depict measured forward and reverse current waveforms through a bi-directional switching circuit at four different output power settings of the piezoelectric power converter depicted in Fig. 1,

[0033] Fig. 4e) shows measured forward and reverse power figures through the bi-directional piezoelectric power converter over a time period where these quantities are adjusted during operation of the power converter,

[0034] Fig. 5 is a schematic block diagram of a generic bi-directional switching circuit,

[0035] Fig. 6 is a schematic block diagram of a bi-directional switching circuit configured for half-wave rectification with either positive or negative DC output voltage; and

[0036] Fig. 7 is a schematic block diagram of a bi-directional switching circuit configured for full-wave rectification with positive DC output voltage.

DETAILED DESCRIPTION

[0037] The below appended detailed description of embodiments of the present invention relate to bi-directional piezoelectric power converters for voltage step-up or voltage multiplication aimed at generating high DC output voltages such as output voltages from several hundred Volts to several thousand Volts. However, the skilled person will understand that the below de-

scribed embodiments are highly useful for other types of applications such as step-down and low voltage power converters requiring high power conversion efficiency.

[0038] Fig. 1 shows a schematic block diagram of a bi-directional piezoelectric power converter 100 in accordance with a first embodiment of the invention. The bi-directional piezoelectric power converter 100 comprises a piezoelectric transformer, PT, 104. The piezoelectric transformer, PT, 104 has a first input electrode 105 electrically coupled to an input or primary section of the bi-directional piezoelectric power converter 100 and a second input electrode connected to ground, GND. A first output electrode 107 of the piezoelectric transformer 104 is electrically coupled to secondary or output section of the piezoelectric transformer 104 to provide a transformer output signal and a second output electrode is connected to ground, GND, like the second input electrode. The bi-directional piezoelectric power converter 100 additionally comprises an input driver 103 electrically coupled directly to the input electrode 105 so as to apply an input drive signal to the input or primary section. A driver control circuit 102 generates appropriately timed gate control signals for NMOS transistors M_2 and M_1 of the input driver 103. The input drive signal has a predetermined excitation frequency determined by parameters of a self-oscillating feedback loop arranged around or enclosing the input driver 103 and the piezoelectric transformer 104. The self-oscillating feedback loop comprises a feedback leg 114 coupling a resonance oscillation signal, having a frequency equal to the predetermined excitation frequency, detected in the piezoelectric transformer structure back to the driver control circuit 102. The self-oscillating feedback loop comprises a resonance current control circuit 112 comprising a peak current detector 126 coupled to a current limiter 128. The resonance current control circuit 112 is configured to adjust a time delay of the adjustable time delay circuit 124 arranged in the feedback leg 114. An AC resonance current in the piezoelectric transformer 104 is detected by a resonance current detector 118 coupled to either the primary side or secondary side of the piezoelectric transformer 104. A resonance current signal supplied by the detector 118 is transmitted to a low-pass or band-pass filter 120 which provides additional phase shift through the feedback loop and may attenuate or suppress certain harmonics components of the fundamental resonance frequency of the piezoelectric transformer 104. A zero-crossing detector 122 receives a filtered signal from the low-pass or band-pass filter 120 and provides an essentially square wave shaped signal indicating zero-crossings of the filtered signal which has an approximate sine shaped waveform. The square wave signal is transmitted to an adjustable time delay

circuit 124 which introduces a variable phase in the self-oscillating feedback loop such that the predetermined excitation frequency can be adjusted. An output signal of the adjustable time delay circuit 124 is coupled to the drive control circuit 102 such as to close the self-oscillating feedback loop around the input driver 103. A resonance current control circuit 112 detects a peak current from the output signal of the low-pass or band-pass filter 120 and adjusts a time delay of the adjustable time delay circuit 124 based thereon. This is useful to compensate for a decrease of the excitation frequency set by the self-oscillating feedback loop under reverse power transmission through the piezoelectric power converter, e.g. in the second state of the bi-directional switching circuit. The ac resonance current in the piezoelectric transformer increases under reverse power transmission and the change is detected by a peak current detector 126 of the resonance current control circuit 112. The effect is compensated by limiting the ac resonance current by the current limiter 128 which makes an appropriate adjustment of the time delay in the adjustable time delay circuit 124 such that an optimal operation point of the self-oscillating feedback loop can be maintained during both forward power transmission and reverse power transmission of the bi-directional piezoelectric power converter 100.

[0039] In the present embodiment of the invention where the input driver 103 is coupled directly to the input electrode 105 without any series or parallel inductor, the piezoelectric transformer 104 preferably possess a ZVS factor larger than 100 % such as larger than 120 %. In this manner ZVS operation of the input driver 103 is enabled both in a first state and a second state of a bi-directional switching circuit 108. The ZVS operation of the input driver 103 improves the power conversion efficiency of the bi-directional piezoelectric power converter 100. The predetermined excitation frequency is preferably selected or set to lie slightly above a fundamental resonance frequency of the piezoelectric transformer 104 within a frequency band or range where the piezoelectric transformer 104 exhibits the above-described ZVS factor larger than 100 % and appears possess inductive input impedance. The feedback leg 114 is coupled to the resonance current control circuit 112 that detects and limits the ac current flowing inside the piezoelectric transformer 104 as explained in further detail above. The use of the self-oscillating feedback loop has considerable advantages because, the predetermined excitation frequency automatically tracks changing characteristics of the piezoelectric transformer 104 and electronic circuitry of the input side of the power converter like the drive control circuit 102. These characteristics will typically change across operation temperature and age but the self-oscillating feedback loop

ensures changes are tracked by the excitation frequency because a slope of the phase response of the piezoelectric transformer 104 is typically much steeper than a slope of a phase response of the low-pass or band-pass filter 120. In this manner, the predetermined excitation frequency will largely be sensitive only to changes of electrical characteristics of the piezoelectric transformer 104 such that the self-oscillating feedback loop automatically maintains the predetermined excitation frequency at an optimum frequency or within an optimum frequency band such as in the ZVS operation range or frequency band of the piezoelectric transformer 104.

[0040] At the secondary side of the PT 104, a bi-directional switching circuit 108 is electrically coupled between a transformer output signal generated at the output electrode 107 of the PT 104 and a positive DC output voltage V_{OUT} applied across a load capacitor C_{LOAD} of the power converter 100. The load may of course comprise a resistive and/or inductive component in addition to the depicted load capacitance C_{LOAD}. A controller or control circuit is adapted to control forward current conduction from the output electrode 107 to V_{OUT} through the bi-directional switching circuit 108 during a first period of the cycle time of the transformer output signal. The positive DC output voltage V_{OUT} is accordingly charged during the first period of the cycle time. This transformer output signal, oscillating at the excitation frequency of the input signal, is applied to a midpoint node between series coupled NMOS transistors M_4 and M_3 of the bi-directional switching circuit 108. The output section of the PT 104, oscillating at the excitation frequency, behaves largely as a current source injecting AC current into the midpoint node between series coupled M_4 and M_3 to generate the transformer output signal or voltage. Furthermore, the controller is adapted to control a second period of the cycle time of the transformer output signal wherein reverse current is conducted through the bi-directional switching circuit 108 to the output electrode 107 of the PT such that V_{OUT} is discharged during the second period of the cycle time. During the second period of the cycle time power is returned to the primary section of the piezoelectric transformer through the output electrode 107 of the PT.

[0041] The skilled person will appreciate that M_3 and M_4 function as respective controllable semiconductor switches each exhibiting low resistance between an inlet and an outlet node (i.e. drain and source terminals) in the on-state and very large resistance in the off-state or non-conducting state. The on-resistance of each of M_3 and M_4 in its on-state/conducting state may vary considerably according to requirements of a particular application, in particular the voltage level at the DC output voltage V_{OUT} or load impedance. In the present high-voltage embodiment

of the invention, each of the M_3 and M_4 is preferably selected such that its on-resistance lies between 50 and 1000 ohm such as between 250 and 500 ohm. The positive DC supply voltage V_{DD} may vary widely in accordance with the requirements of a particular application. In the present embodiment of the invention, the positive DC supply voltage V_{DD} is preferably selected to a voltage between 20 and 40 volt such as about 24 volt.

[0042] The bi-directional switching circuit 108 comprises a high-side semiconductor diode D_4 arranged or coupled across drain and source terminals of M_4 so as to conduct the forward current to the DC output voltage V_{OUT} in a first state of the bi-directional switching circuit 108. A low-side semiconductor diode D_3 is in a similar manner coupled across drain and source terminals of M_3 so as to conduct the reverse current through the output electrode 107 and output section of the PT 104 during at least a portion of the first state. In the first state, the forward current is conducted from the output electrode 107 of the PT 104 through the bi-directional switching circuit 108 to the DC output voltage V_{OUT} during a first period of a cycle time of the transformer output signal to charge the output voltage. This is accomplished by switching the high-side NMOS transistor M_4 to its on-state or conducting state by a self-powered high-side driver 106 which forms part of the controller. The self-powered high-side driver 106 or self-powered driver 106 is coupled between the control or gate terminal of M_4 and the output electrode 107 which supplies the transformer output signal. The timing of the state switching of M_4 is determined by the detection of forward current in D_4 by a current sensor (not shown) contained in the self-powered driver 106. This current sensor is preferably arranged in series with the high-side semiconductor diode D_4. In response to detection of forward current in D_4 the self-powered driver 106 switches M_4 to its on-state which effectively clamps D_4 such that a majority of the forward current flowing through the parallel connection of M_4 and D_4 to the DC output voltage V_{OUT} in reality flows through M_4. On the other hand, during a negative half-cycle of the transformer output signal in the first state of the bi-directional switching circuit 108, D_4 is reverse biased and M_4 switched to its off-state at expiry of a timer period setting of the timer circuit 205 (refer to Fig. 2) as explained below in additional detail. However, current is now conducted from the negative supply rail, i.e. GND in the present embodiment, to the output electrode 107 of the PT 104 through the parallel connection of M_3 and D_3. Initially, D_3 will start to conduct forward current once it becomes forward biased by the negative transformer output voltage. M_3 is on the other hand, switched to its on-state or conducting state by a low-side driver 121 which forms part

of the controller. The low-side driver 121 is coupled to the gate terminal of M_3 and configured to switch M_3 from its off-state to its on-state and vice versa. However, while the timing of the state switching of M_3 from its off-state to the on-state is determined in a manner similar to M_4, the opposite state switching of M_3 is effected synchronously to input drive signal as explained below. M_3 is switched from the off-state to the on-state by a detection of forward current in D_3 by a current sensor (not shown) contained in the low-side driver 121. This current sensor is arranged in series with the low-side semiconductor diode D_3. At the detection of forward current in D_3 the low-side driver 121 switches M_3 to its on-state which effectively clamps D_3 such that a majority of the forward current flowing through the parallel connection of M_3 and D_3 in reality flows through M_3.

[0043] Consequently, in the first state the bi-directional switching circuit 108 functions as a half-wave rectifier or voltage doubler of the transformer output signal such that forward current is conducted from the output electrode 107 of the PT 104 through the high-side NMOS transistor M_4 and semiconductor diode D_4 to the DC output voltage V_{OUT} to charge V_{OUT}. In the negative half-periods of the transformer output signal, current is circulated around the secondary section of the PT 104 without charging the DC output voltage in the current embodiment which uses the half-wave rectification provided by the present bi-directional switching circuit 108. In comparison to a traditional diode-based half-wave rectifier, the bi-directional switching circuit 108 additionally comprises the NMOS transistors M_4 and M_3 of the bi-directional switching circuit 108 arranged for clamping of the high and low-side semiconductor diodes D_4 and D_3. During a second state and during a third state of the bi-directional switching circuit 108, the NMOS transistors M_3 and M_4 are controlled by the controller such that a flow of reverse power is enabled. The reverse current is conducted through the bi-directional switching circuit 108 from the DC output voltage V_{OUT} to the output electrode 107 of the PT 104 during a second period of the cycle time of the transformer output signal so as to discharge V_{OUT}. Due to the inherent bi-directional transfer property of the PT 104 power applied to the secondary section through the output electrode 107 is transferred to the input section of the PT 104 in effect transferring power in opposite direction to the normal flow of power of the power converter 100.

[0044] In connection with the reverse current conduction during the second period of the cycle time, state switching of M_3 is controlled by the low-side driver 121 coupled to the gate terminal of M_3. The low-side driver 121 is responsive to a synchronous state control signal de-

rived from the input drive signal supplied by an adjustable time delay circuit, control ΔT, of a phase controller 111. The phase controller comprises the adjustable time delay circuit, control ΔT, and a fixed time delay, ΔT circuit. The phase controller 111 receives the previously mentioned zero-crossing detector output signal 119 which switches states synchronously to the input drive signal and the transformer output signal because this signal is generated inside the self-oscillating feedback loop. Since the input drive signal and the transformer output signal oscillate synchronously to each other, the time delay imposed by the phase controller 111 to the zero-crossing detector output signal 119 sets a length or duration of the second period of the cycle time of the transformer output signal. M_3 is allowed to continue conducting current for the duration of the second period of the cycle time until the state transition of the synchronous state control signal turns off M_3 of the low-side driver 121. While the corresponding state switching of the high-side NMOS transistor M_4 from its on-state to its off-state in one embodiment is controlled by the synchronous state control signal albeit phase shifted about 180 degrees, the present embodiment of the invention uses a different turn-off mechanism provided by the self-powered high-side driver 106. The self-powering of the high-side driver 106 is configured to terminate a reverse current conducting period of M_4 based on an internally generated state control signal supplied by an internal timer rather than the above-described synchronous state control signal supplied by the adjustable time delay circuit, control ΔT. The self-powered property of the high-side driver 106 is highly advantageous for high-voltage output PT based power converters where the DC output voltage may be above 1 kV. The self-powering property of the high-side driver 106 circumvents the need for raising the zero-crossing detector output signal 119 to a very high voltage level, i.e. matching the level of the DC output voltage, before being supplied to the high-side driver 106 to appropriately control the gate terminal of M_4. The skilled person will recognize that the gate terminal of M_4 must be raised to a level above the level of the DC output voltage signal to switch M_4 to its on-state. The self-powered high-side driver 106 is electrically coupled between the gate terminal of M_4 and the output electrode 107 carrying the transformer output voltage as explained in further detail below in connection with Fig. 2.

[0045] During operation, the bi-directional piezoelectric power converter 100 comprises two distinct mechanisms for adjusting the level of the DC output voltage V_{OUT}. A first mechanism uses a DC output voltage detection or monitoring circuit 109 which supplies a signal to the output voltage control circuit 110 of the controller indicating the instantaneous level of the DC

output voltage. A charge control circuit ΔQ compares the instantaneous level of the DC output voltage with a reference voltage which for example represents a desired or target DC output voltage of the power converter. The charge control circuit determines whether the current DC output voltage is to be increased or decreased based on this comparison and adjusts at least one of: {a modulation of a pulse width modulated input drive signal, a carrier frequency of the pulse width modulated input drive signal, a burst frequency of a burst modulated input drive signal} in appropriate direction to obtain the desired adjustment of the DC output voltage. A second mechanism for adjusting the level of the DC output voltage V_{OUT} also uses the level signal from the DC output voltage detection circuit 109. In this instance the output voltage control circuit 110 adjusts the duration of the second period of the cycle time of the transformer output signal where M_3 conducts reverse current through the adjustable time delay circuit, control ΔT, of the phase controller 111. The corresponding adjustment of the second period of the cycle time as regards M_4 is preferably made by delaying the triggering time or point of a timer circuit included in the self-contained high-side driver 106 as explained below in connection with Fig. 2. The delay of the triggering time of the timer circuit may be controlled dynamically during operation of the bi-directional power converter 100 by the controller by adjusting a delay of an adjustable time delay circuit, control ΔT, to reach a desired or target duration of the second period of the cycle time of the transformer output signal. The adjustable time delay circuit, control ΔT, allows the controller to adjust the duration of the second period of the cycle time of the transformer output signal wherein reverse current is conducted by the bi-directional switching circuit through the output electrode 107 back to the primary side of the PT 104. By this adjustment of the duration of the second period of the cycle time, the amount of reverse power can be effectively controlled allowing for the desired adjustment of the level of the DC output voltage V_{OUT} while conserving power.

[0046] The skilled person will appreciate that the degree of charge or discharge of the V_{OUT} may be controlled in a step-wise or substantially continuous manner by a corresponding control of the duration of the second period of the cycle time such that the level of V_{OUT} may be continuously increased or reduced as desired. Furthermore, the length of the second period of the cycle time of the high-side NMOS transistor M_4 may be adapted to track the same for M_3 as explained below in connection with the detailed description of the operation of the self-powered high side driver 106. The skilled person will understand that if the duration of the second period

of the cycle time is set to zero by the controller, the bi-directional piezoelectric power converter 100 may be adapted to exclusively operate the first state where the switching circuit charges the positive DC output voltage during the first period of cycle times of the transformer output signal. In this state, the NMOS transistors M_3 and M_4 are only conducting during the first period of the cycle time so to actively clamp the low-side and high-side semiconductor diodes D_3 and D_4, respectively.

[0047] Fig. 2 is a schematic circuit diagram of the design of the self-powered high-side driver 106. The self-powered driver 106 comprising the above-mentioned timer circuit 205 or timer 205 coupled to the gate terminal of NMOS transistor M_4 through gate driver 207 so as to control the duration of its on-state, and possibly an off-state, of M_4 in accordance with a timer period defined by a timer period setting. The timer period or timer delay is preferably adjusted to about 50 % of the cycle of the transformer output signal as set by the excitation frequency controlled by the self-oscillating feedback loop. The self-powered driver 106 comprises a rectifying element in form of high-voltage diode 201 coupled in series with a pair of anti-parallel diodes D_{1a} and D_{1b} which are coupled to a local supply capacitor 203 C_{local}. The local supply capacitor 203 is acting as a rechargeable energy storage component which is charged (as indicated by charge current I_{boot}) with energy from the positive DC supply voltage V_{DD} during conduction periods of the high-voltage diode 201. The voltage $V_{\_local}$ on the local supply capacitor 203 C_{local} is coupled to voltage supply lines of the circuit blocks of the self-powered high-side driver 106 to supply operating power to these circuits during time periods where the self-powered driver 106 is decoupled from the residual portion of the power converter as described below. A Reset input R of the timer circuit 205 is coupled to a voltage level V_R at a circuit node in-between the high-voltage diode 201 and the anti-parallel diodes D_{1a} and D_{1b}. When the transformer output voltage at the output electrode 107 of the PT is raised above GND because the low-side NMOS transistor M_3 has been switched to its non-conducting state the AC current supplied by the PT through the output electrode 107 raises the voltage at the midpoint node between series coupled NMOS transistors M_4 and M_3 eventually leading to a forward biasing of the semiconductor di-

ode D_4, the voltage level at V_R will fall from approximately V_{DD} towards the local zero potential on node 107, Gnd_local. When the voltage level at V_R has dropped down to the local zero potential, the high-voltage diode 201 becomes reverse biased. The timer circuit 205 is triggered because V_R is conveyed to the Reset input R of the timer circuit 205. The output of the timer circuit 205 switches to its off state after expiry of the timer period, i.e. about one-half of the cycle time of the transformer output signal in the present embodiment. This state transition is then immediately conveyed to the gate input of M_4 by the gate driver 207. In response M_4 is accordingly switched to its off-state. Consequently, the state switching of M_3 from on-state to the off-state determines when the transformer output voltage at the output electrode 107 begins to increase from the ground level triggering the timer circuit 205 and initiating the timer period according to the timer period setting. Because, the state switching of M_3 from its on-state to its off-state is controlled by the above-described synchronous state control signal supplied by the adjustable time delay circuit, control ΔT, the turn-off timing or instant of M_3 indirectly controls or sets the delayed turn-off timing of M_4. Consequently, by adjustment of the time delay provided by the time delay circuit, control ΔT, the controller is able to adjust the length of the second period of the cycle time of the high-side NMOS transistor M_4 where reverse current is conducted. The current sense circuit is adapted to sense a forward current running through the semiconductor diode D_4 by monitoring a voltage drop across a sense resistor R and turn on M_4 through the gate driver 207 in response to a detection of forward current such that M_4 effectively clamps the semiconductor diode D_4 during the first period of the cycle time of the transformer output signal to establish a low-impedance path for the conduction of forward current through the bi-directional switching circuit to V_{OUT} to charge V_{OUT}.

[0048] Fig. 3 shows a schematic block diagram of a bi-directional piezoelectric power converter 300 in accordance with a second embodiment of the invention. Corresponding features have been provided with corresponding reference numerals in the first and second embodiments of the bi-directional piezoelectric power converter to ease comparison. Generally, the bi-directional piezoelectric power converter 300 has similar characteristics and features as those

explained in connection with the first embodiment, but the way the predetermined excitation frequency at the input driver 302 is set differs. In the first embodiment, the predetermined excitation frequency was set by loop parameters, including parameters of the PT 104, of the self-oscillating feedback loop formed around the piezoelectric transformer. However, in the present embodiment, the predetermined excitation frequency is set by an independent frequency generator or oscillator 317. The predetermined excitation frequency is preferably set to a value within a frequency range where the PT 304 exhibits inductive input impedance. Such inductive input impedance enables ZVS operation of the input driver 303 to improve its power conversion efficiency as explained above.

[0049] Figs. 4a) – d) depict measured forward and reverse current waveforms through the bi-directional switching circuit 108 during delivery of a positive, zero and negative net output power to the load capacitor $C_{LOAD.}$ The y-axis of all the upper graphs 402 depicts current in mA and the x-axes time in milliseconds such that the x-axis spans over a time period of about 100 µS. The dotted curve 403 of each of the upper graphs 402 of Figs. 4a)-d) shows measured current through the parallel connection of M_4 and D_4 to the DC output voltage V_{OUT} (refer to Fig. 1) such that V_{OUT} is charged during positive half-periods of the transformer output signal on the electrode 107. The full line curves 405 of the same graphs 402 of Figs. 4a)–d) show measured current through the parallel connection of M_3 and D_3 where current is conducted in opposite or negative half-periods of the cycle time of the transformer output signal. In the negative half-periods of the transformer output signal, the current is circulated around the secondary section of the PT 104 without charging the DC output voltage. The lower graphs 401 of Figs. 4a)-d) show the input drive voltage waveform 407 at the first input electrode 105 which is coupled to the input section of the PT. The y-axis of the lower graphs 401 depicts the input drive voltage in volt. The skilled person will understand that the corresponding transformer output voltage at the electrode 107 may have peak values above several hundred or even several kV due to the voltage gain of the PT 104.

[0050] In the depicted operation mode in Fig. 4a), the bi-directional switching circuit operates essentially in its first state where the circuit essentially acts as a traditional half-wave rectifier. The DC output voltage V_{OUT} is charged by the forward current running through the high-side rectifying element, comprising the parallel connection of M_4 and $D_{4,}$ to the DC output voltage in every positive half-period of the transformer output voltage. The current through the

parallel connection of M_4 and D_4 runs forward during the first period 403f of each of the cycle times of the transformer output signal as indicated schematically on the dotted current waveform curve 403. A positive net output power of 2.6 W is delivered to the load capacitor $C_{LOAD.}$

[0051] In Fig. 4b), the bi-directional switching circuit 108 has been switched to its second state and the positive output power to load capacitor C_{LOAD} is reduced from the above 2.6 W to 1.4 W by reverse conduction of power to the input side of the PT. This is visible by inspection of the dotted curve 403 of the upper graph 402 of Fig. 4b) which shows measured current through the high-side rectifying element, comprising the parallel connection of M_4 and $D_{4,}$ to the DC output voltage. The current through the parallel connection of M_4 and D_4 runs forward during a first period 403f of the cycle time of the transformer output signal such that the DC output voltage is charged. However, during a second period 403r of the same cycle of the transformer output signal, the current through the parallel connection of M_4 and D_4 runs in an opposite direction and becomes negative such that the DC output voltage is discharged rather than charged. The second period of the cycle of the transformer output signal, where reverse current is conducted, is introduced or caused by a delayed or phase-shifted turn-off timing of the NMOS transistor M_4 through the adjustable time delay circuit, control ΔT, of the phase controller 111 as previously explained. By comparison of the areas underneath the current waveform 403 during the first and second periods 403f, 403r of the same cycle of the transformer output signal it is apparent that net positive charge or power is transferred to the DC output voltage under the chosen conditions which is consistent with the measured positive output power of 1.4 W.

[0052] In Fig. 4c), the bi-directional switching circuit 108 also operates in its second state as was the case in Fig. 4b). However, the output power to the load capacitor C_{LOAD} is reduced from the above 1.4 W to 0.0 W by an increased delay of the turn-off timing of the NMOS transistor M_4 as explained above in connection with Fig. 2. The increased time shift leads to a longer duration of the second period of the transformer output signal where reverse current is conducted through M_4 such the DC output voltage is further discharged compared to the situation in Fig. 4b). This is visible by inspection of the dotted curve 403 of the upper graph 402 of Fig. 4c) which shows measured current through the high-side rectifying element, comprising the parallel connection of M_4 and $D_{4,}$ to the DC output voltage during consecutive cycle times of the

transformer output voltage. The current through the parallel connection of M_4 and D_4 runs forward during a first period 403f of the cycle time of the transformer output signal such that the DC output voltage is charged. However, during a second period 403r of the same cycle of the transformer output signal, the current through the parallel connection of M_4 and D_4 becomes negative as explained above such that the DC output voltage is discharged rather than charged in the second time period. By comparison of the areas underneath the current waveform 403 during the first and second periods 403f, 403r of the same cycle of the transformer output signal it is readily apparent that approximately zero net charge or zero net power is transferred to the DC output voltage during a cycle time of the transformer output voltage under the chosen conditions. This observation is also consistent with the measured output power of 0.0 W.

[0053] Finally, in Fig. 4d), the bi-directional switching circuit 108 continues to operate in the second state as was the case in Figs. 4b) and c). However, the net output power to the load capacitor C_{LOAD} is now negative at -2.4 W rather than positive or zero. This has been achieved by a further increase of the delay of the turn-off timing of the NMOS transistor M_4 as explained above in connection with Fig. 2. The increased time shift leads to a longer duration of the second period of the transformer output signal where reverse current is conducted through M_4 such the DC output voltage is further discharged compared to the situation in Fig. 4c). This is visible by inspection of the dotted curve 403 of the upper graph 402 of Fig. 4d) which shows measured current through the high-side rectifying element, comprising the parallel connection of M_4 and D_4 to the DC output voltage during consecutive cycle times of the transformer output voltage. The first period 403f of the cycle time of the transformer output signal is very small such that only a single short spike of forward current through the parallel connection of M_4 and D_4 is visible making the amount of charge or forward current transferred to the DC output voltage nearly zero during the first period 403f. However, the second period 403r has nearly a duration of an entire half-period of the cycle time or period of the transformer output signal such that a large amount of reverse current is conducted through the parallel connection of M_4 and D_4 leading to a substantial discharge of the DC output voltage. Consequently, by comparison of the areas underneath the current waveform 403 during the first and second periods 403f, 403r of the same cycle

of the transformer output signal it is readily apparent that substantial amount of negative net charge or negative net power is transferred to the DC output voltage during a cycle time of the transformer output voltage under the chosen conditions. This observation is also consistent with the measured output power of -2.4 W.

[0054] Fig. 4e) shows measured forward and reverse power figures through the bi-directional piezoelectric power converter over a time period of approximately 6 milliseconds where these quantities are dynamically adjusted in opposite direction during operation of the piezoelectric power converter. The upper graph 412 shows corresponding values of measured input power, curve 415, and output power, curve 416, over time. The lower graph 411 shows the delay of the turn-off timing of the NMOS transistor M_4 which is controlled by the turn-off timing of the low-side NMOS transistor M_3 through the adjustable time delay circuit, control ΔT, of the phase controller 111 as previously explained. The y-axis of the lower graph 411 depicts this time delay in μS. As illustrated, the controller of the present piezoelectric power converter enables both full forward transmission of power from the input to the output as illustrated at a time delay value of zero μS. In this operation state, substantially all input power of approximately 2.6 W is transferred to the load capacitor $C_{LOAD.}$ When the time delay is gradually increased from about 1 μS to about 6 μS over time depicted along the x-axis from about 6 mS to about 8 mS, the input power gradually becomes less and less positive and finally negative indicating that a continuously increasing amount of power is transmitted in reverse direction from the output voltage and back to the primary section of the piezoelectric transformer. The measured output power curve 416 has a mating shape indicating that a gradually decreasing output power and finally a negative output power is supplied to the load capacitor $C_{load.}$ Hence the load capacitor is discharged by reverse power transmission back to the primary section of the piezoelectric transformer. The skilled person will appreciate the efficient and flexible way the present bi-directional piezoelectric power converter can be adapted for both forward and reverse transmission of power by control of the first and second states of the bi-directional switching circuit. This property enables energy efficient and accurate output voltage regulation.

[0055] Fig. 5 is a schematic block diagram of a generic and highly versatile bi-directional switching circuit 508 coupled to a PT 504. The bi-directional switching circuit 508 can be programmed to provide a positive or negative output voltage across the load capacitor C_{load} and to

provide half-wave or full-wave rectification of the transformer output signal supplied between the positive output electrode 507 and a negative, or opposite phase, output electrode 507b. The different modes of operation can be obtained through appropriate programming or setting of respective control voltages on the gate terminals of the NMOS transistors M4A, M4B, M3A, M3B, M6A, M6B, M5A and M5B. The transformer output signal at the positive output electrode 507 is applied to a midpoint node of a first branch of cascaded NMOS transistors M4A, M4B, M3A and M3B wherein an upper leg or high-side leg comprises M4A and M4B while a lower leg comprises cascaded NMOS transistors M3A and M3B. The oppositely phased transformer output signal at the negative output electrode 507b is applied to a midpoint node of a second branch of cascaded NMOS transistors M6A, M6B, M5A and M5B wherein an upper leg or high-side leg comprises M6A and M6B while a lower leg comprises cascaded NMOS transistors M5A and M5B. The secondary side of the PT 504 acts as a current source through the positive and negative output electrodes 507, 507b, respectively.

[0056] With NMOS transistors M4A, M4B and NMOS transistors M5A, M5B in their respective on-states/conducting states, a positive output voltage V_{OUT} is applied to the output electrodes 507, 507b irrespective of the polarity of the current delivered by the secondary side of the PT 504 through the positive and negative output electrodes 507, 507b, respectively. With NMOS transistors M4A, M4B and NMOS transistors M6A, M6B in their respective on-states/conducting states, zero volts is applied to the output electrodes 507,507b irrespective of the polarity of the current delivered by the secondary side of the PT 504 through the positive and negative output electrodes 507, 507b, respectively. With NMOS transistors M3A, M3B and NMOS transistors M6A, M6B in their respective on-states/conducting states, a negative DC output voltage V_{OUT} is applied to the output electrodes 507,507b irrespective of the polarity of the current delivered by the secondary side of the PT 504 through the positive and negative output electrodes 507, 507b, respectively.

[0057] In this manner, the bi-directional switching circuit 508 enables a controlled bi-directional flow of power through the PT 504 for output voltages of any polarity. Some of the different modes of operation are described below in further detail.

[0058] Fig. 6 is a schematic block diagram of a bi-directional switching circuit 608 configured for half-wave rectification of the transformer output signal supplied between the positive and negative output electrode 607 and 607b, respectively. The present bi-directional switching

circuit 608 is capable of providing both positive and negative output voltages at V_{OUT} by appropriate programming or adaptation. By constantly holding the NMOS transistors M4B, M3B in their respective on-states or conducting states during operation of the switching circuit 608, M4A and M3A will act as a half-wave rectifier generating a positive voltage at V_{OUT} by adapting the control signals for these NMOS transistors in the manner described above in connection with the first embodiment of the invention. This mode of operation of the bi-directional switching circuit 608 is accordingly similar to the operation of the bi-directional switching circuit 308 described previously under the first embodiment of the invention. The bi-directional switching circuit 608 can however also be programmed to provide a negative output voltage at V_{OUT} by setting the NMOS transistors M4A and M3A constantly to their on-states. In this alternative mode of operation, M4B and M3B will act as a half-wave rectifier generating a negative DC output voltage when appropriate control signals are applied to their respective gate inputs.

[0059] The secondary side of the PT 604 acts as a current source through the positive and negative output electrodes 607, 607b, respectively as previously explained. With NMOS transistors M4A, M4B switched to their respective on-states/conducting states, a positive output voltage V_{OUT} is applied to the output electrodes 607 irrespective of the polarity of the current delivered by the secondary side of the PT 604 through the positive output electrode 607. With NMOS transistors M3A, M3B switched to their respective on-states/conducting states, zero volts is applied to the output electrodes 607 irrespective of the polarity of the current delivered by the secondary side of the PT 604 through the positive output electrode 607. In this manner, the bi-directional switching circuit 608 enables a controlled bi-directional flow of power through the PT 604 for positive output voltages at V_{OUT} in a first state and controlled bi-directional flow of power through the PT 604 for negative output voltages at V_{OUT} in a second state.

[0060] Fig. 7 is a schematic block diagram of a bi-directional switching circuit 708 configured for full-wave rectification of the transformer output signal supplied between the positive and negative output electrode 707 and 707b, respectively. The bi-directional switching circuit 708 is configured to generate a positive output voltage across the load capacitor e.g. a positive DC voltage. The secondary side of the PT 704 acts as a current source through the positive and negative output electrodes 707, 707b, respectively as previously explained. With NMOS transistors M4A, M5A switched to their respective on-states/conducting states, the voltage V_{OUT} is applied to the output electrodes 707, 707b irrespective of the polarity of the current delivered by

the secondary side of the PT 704 through the output electrodes 707, 707b. With NMOS transistors M4A, M6A switched to their respective on-states/conducting states, or NMOS transistors M3A, M5A switched to their respective on-states/conducting states, zero volts is applied to the output electrodes 707, 707b irrespective of the polarity of the current delivered by the secondary side of the PT 704 through the output electrodes 707, 707b. With NMOS transistors M3A, M6A switched to their respective on-states/conducting states, minus V_{OUT} ($-V_{OUT}$) is applied to the output electrodes 707, 707b irrespective of the polarity of the ac current delivered by the secondary side of the PT 704 through the output electrodes 707, 707b.

CLAIMS

1. A bi-directional piezoelectric power converter comprising:

- a piezoelectric transformer comprising an input electrode electrically coupled to an input or primary section of the piezoelectric transformer and an output electrode electrically coupled to secondary or output section of the piezoelectric transformer to provide a transformer output signal,

- an input driver electrically coupled to the input electrode and arranged to supply an input drive signal with a predetermined excitation frequency to the input electrode,

- a bi-directional switching circuit coupled between the output electrode and an output voltage of the converter,

- a controller adapted to control first and second states of the bi-directional switching circuit based on the input drive signal or the transformer output signal such that:

- in a first state, forward current is conducted from the output electrode to the output voltage through the bi-directional switching circuit during a first period of a cycle time of the transformer output signal to charge the output voltage,

- in a second state, reverse current is conducted from the output voltage to the output electrode through the bi-directional switching circuit during a second period of the cycle time of the transformer output signal to discharge the output voltage and return power to the primary section of the piezoelectric transformer.

2. A bi-directional piezoelectric power converter according to claim 1, wherein the controller in the second state is further configured to control the switching circuit such that:

- both forward current and reverse current is conducted during a single cycle of the transformer output signal.

3. A bi-directional piezoelectric power converter according to claim 1 or 2, wherein the controller is adapted to terminate the second period of the cycle time synchronously to the input drive signal or synchronously to the transformer output signal.

4. A bi-directional piezoelectric power converter according to any of claims 1-3, wherein the controller is adapted to initiate the first period of the cycle time synchronously to the input drive signal or synchronously to the transformer output signal.

5. A bi-directional piezoelectric power converter according to any of claims 1-3, wherein the controller is adapted to:

- sense a current in, or a voltage across, an electrical component of the bi-directional switching circuit,
- initiate the forward current conduction in the first period of the cycle time in response to a sensed current or voltage so as to asynchronously initiate the forward current conduction.

6. A bi-directional piezoelectric power converter according to any of the preceding claims, wherein the bi-directional switching circuit comprises:

- a first controllable semiconductor switch arranged between the output electrode and the output voltage,
- a second controllable semiconductor switch arranged between the output electrode and a negative supply voltage; wherein the controller is configured to alternatingly switch the first and second controllable semiconductor switches to respective on-states and off-states in a non-overlapping manner to control the forward and reverse current conduction.

7 A bi-directional piezoelectric power converter according to claim 6, wherein the bi-directional switching circuit further comprises:

- a first semiconductor diode coupled across inlet and outlet nodes of the first controllable semiconductor switch to conduct forward current to the output voltage during at least a portion of the first period of the cycle time.

8. A bi-directional piezoelectric power converter according to claim 7, wherein the controller is configured to sense the forward current through, or the forward voltage across, the first semiconductor diode; and

- switch the first controllable semiconductor switch to the on-state in response to a sensed forward current or voltage so as to actively clamp the first semiconductor diode during the first period of the cycle time.

9. A bi-directional piezoelectric power converter according to any of the preceding claims, wherein the controller comprises an adjustable time delay circuit providing an adjustable duration of the second period of the cycle time of the transformer output signal.

10. A bi-directional piezoelectric power converter according to claim 9, wherein the controller is configured to derive a synchronous state control signal from the input drive signal; and

- apply the synchronous state control signal through the adjustable time delay circuit to a switch control terminal of the second controllable semiconductor switch and/or a switch control terminal of the first controllable semiconductor switch to control respective states of the first and second controllable semiconductor switches.

11. A bi-directional piezoelectric power converter according to claim 10, wherein the controller comprises:

- a self-powered driver coupled between the switch control terminal of the first controllable semiconductor switch and the output electrode of the output section;

- the self-powered driver comprising a timer circuit configured to control the state of the first semiconductor switch in accordance with a timer period setting; said timer period setting being based on the cycle time of the transformer output signal.

12. A bi-directional piezoelectric power converter according to claim 11, wherein the self-powered driver comprises a local energy storage component supplying power to the self-powered driver; and

- a rectifying element coupled between the local energy storage component and a power supply voltage of the power converter to energize the local energy storage component.

13. A bi-directional piezoelectric power converter according to claim 12, wherein the rectifying element comprises a high-voltage diode having a break-down voltage larger than 200 V, or more preferably larger than 500 V or larger than 1000 V.

14. A bi-directional piezoelectric power converter according to claim 12 or 13, wherein the self-powered driver is configured to start the timer in response to a change of bias state of the rectifying element.

15. A bi-directional piezoelectric power converter according to claim 13 or 14, wherein the timer period setting substantially equals 50 % of the cycle time the of the transformer output signal.

16. A bi-directional piezoelectric power converter according to any of claims 6-15, wherein the first and/or the second semiconductor switch comprises a semiconductor selected from the group of {MOSFET, IGBT, bipolar transistor, Gate Turn-off thyristor (GTO)}.

17. A bi-directional piezoelectric power converter according to any of claims 6-15, wherein the first semiconductor diode and/or the second semiconductor diode comprises a body/substrate diode integrally formed with the first or the second semiconductor switch, respectively.

18. A bi-directional piezoelectric power converter according to any of the preceding claims, wherein the controller is configured to controlling the switching between the first state and the second state based on a difference between the output voltage and a predetermined AC or DC reference voltage.

19. A bi-directional piezoelectric power converter according to any of the preceding claims, comprising a self-oscillating feedback loop arranged around the input driver and the piezoelectric

transformer, wherein the self-oscillating feedback loop is adapted to set the predetermined excitation frequency of the input drive signal.

20. A bi-directional piezoelectric power converter according to claim 19, wherein the self-oscillating feedback loop comprises an adjustable time delay configured to adjust a phase response of the self-oscillating feedback loop whereby the predetermined excitation frequency is adjusted.

21. A bi-directional piezoelectric power converter according to claim 19 or 20, wherein the self-oscillating feedback loop comprises a zero-crossing detector configured to supply a synchronization signal to the controller, said synchronization signal being synchronous to the input drive signal or the transformer output signal.

22. A method of increasing an apparent ZVS factor of a piezoelectric transformer of a power converter, comprising steps of:

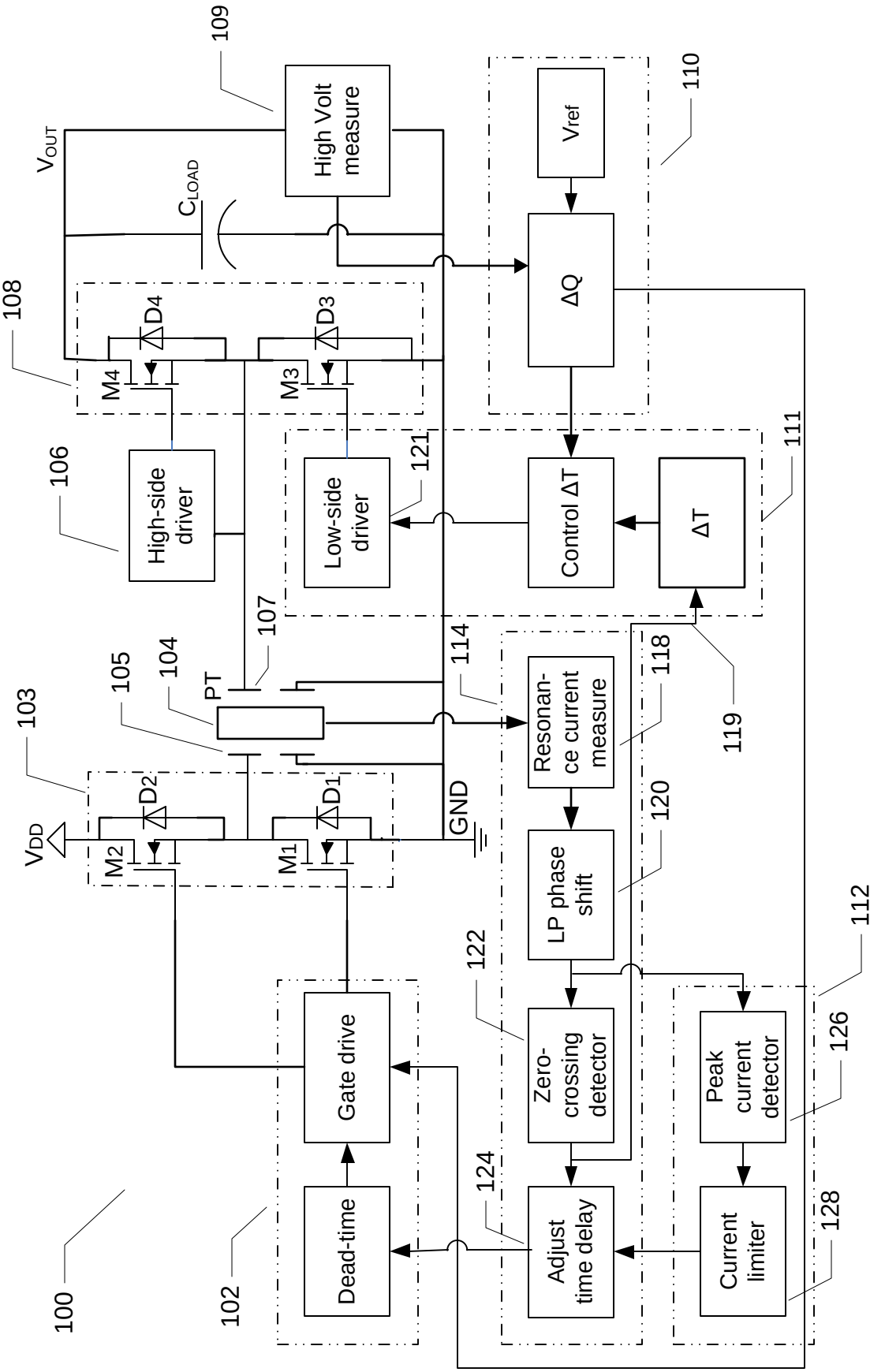
- applying an input drive signal with a predetermined excitation frequency to an input electrode of the piezoelectric transformer,
- providing a bi-directional switching circuit coupled between a secondary or output section of the piezoelectric transformer and an output voltage of the power converter,
- conducting, in a first state, forward current from the output section to the output voltage through the bi-directional switching circuit during a first period of a cycle time of the transformer output signal to charge the output voltage,
- conducting, in a second state, reverse current from the output voltage to the output section through the bi-directional switching circuit during a second period of the cycle time of the transformer output signal to discharge the output voltage,
- adjusting the apparent ZVS factor of the piezoelectric transformer by adjusting a length of the second period of the cycle time.

23. A method of increasing an apparent ZVS factor of a piezoelectric transformer of a power converter, comprising a further step of:

- conducting both forward current and reverse current during a single cycle of the transformer output signal.

ABSTRACT

A bi-directional piezoelectric power converter comprising a piezoelectric transformer. The piezoelectric transformer comprises an input electrode electrically coupled to a primary section of the piezoelectric transformer and an output electrode electrically coupled to an output section of the piezoelectric transformer to provide a transformer output signal. A bi-directional switching circuit is coupled between the output electrode and a DC or AC output voltage of the power converter. Forward and reverse current conducting periods of the bi-directional switching circuit is based on the input drive signal or the transformer output signal such that a forward current is conducted from the output electrode through the bi-directional switching circuit to the DC or AC output voltage in a first state to charge the DC or AC output voltage. In a second state, a reverse current is conducted through the bi-directional switching circuit from the DC or AC output voltage to the output electrode to discharge the DC or AC output voltage and return power to the primary section of the piezoelectric transformer.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102
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110
111
112
114
118
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120
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122
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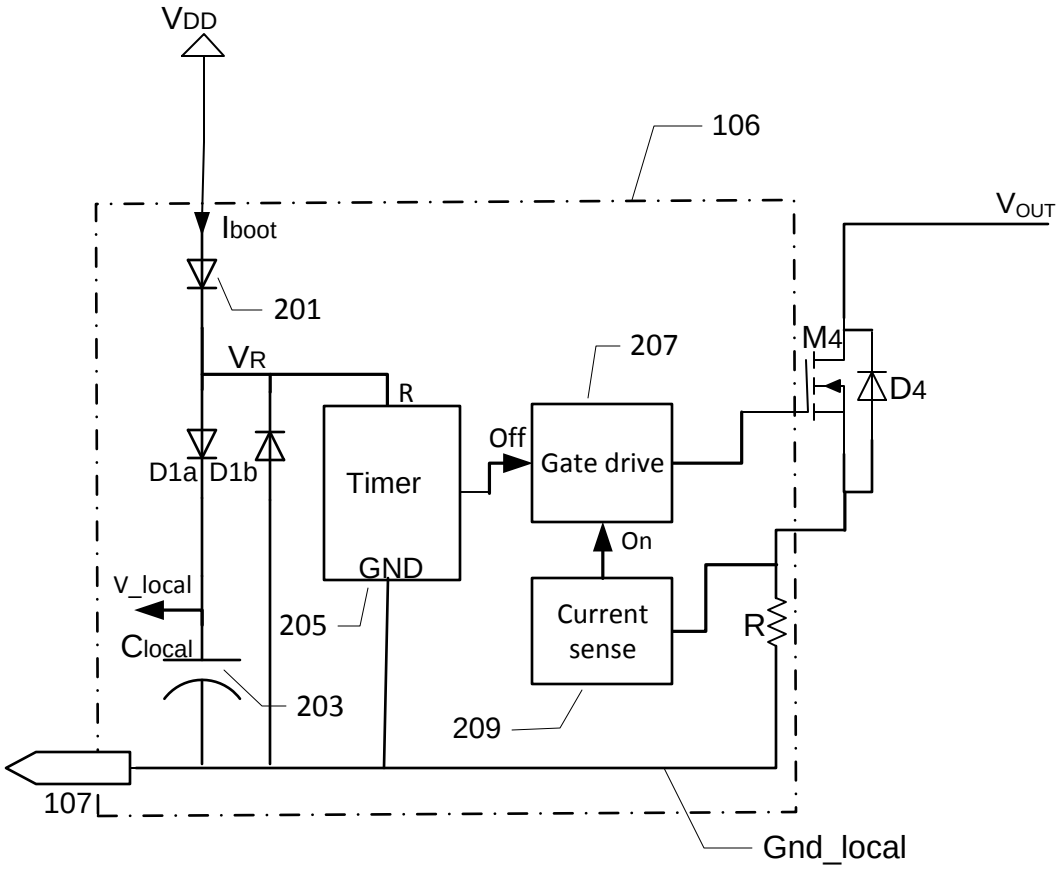
126
128
V_{OUT}
C_{LOAD}
V_{DD}
PT
GND
M1
M2
M3
M4
D1
D2
D3
D4
High Volt measure
Vref
ΔQ
Control ΔT
ΔT
High-side driver
Low-side driver
Resonan-ce current measure
LP phase shift
Zero-crossing detector
Peak current detector
Gate drive
Dead-time
Adjust time delay
Current limiter

Fig. 1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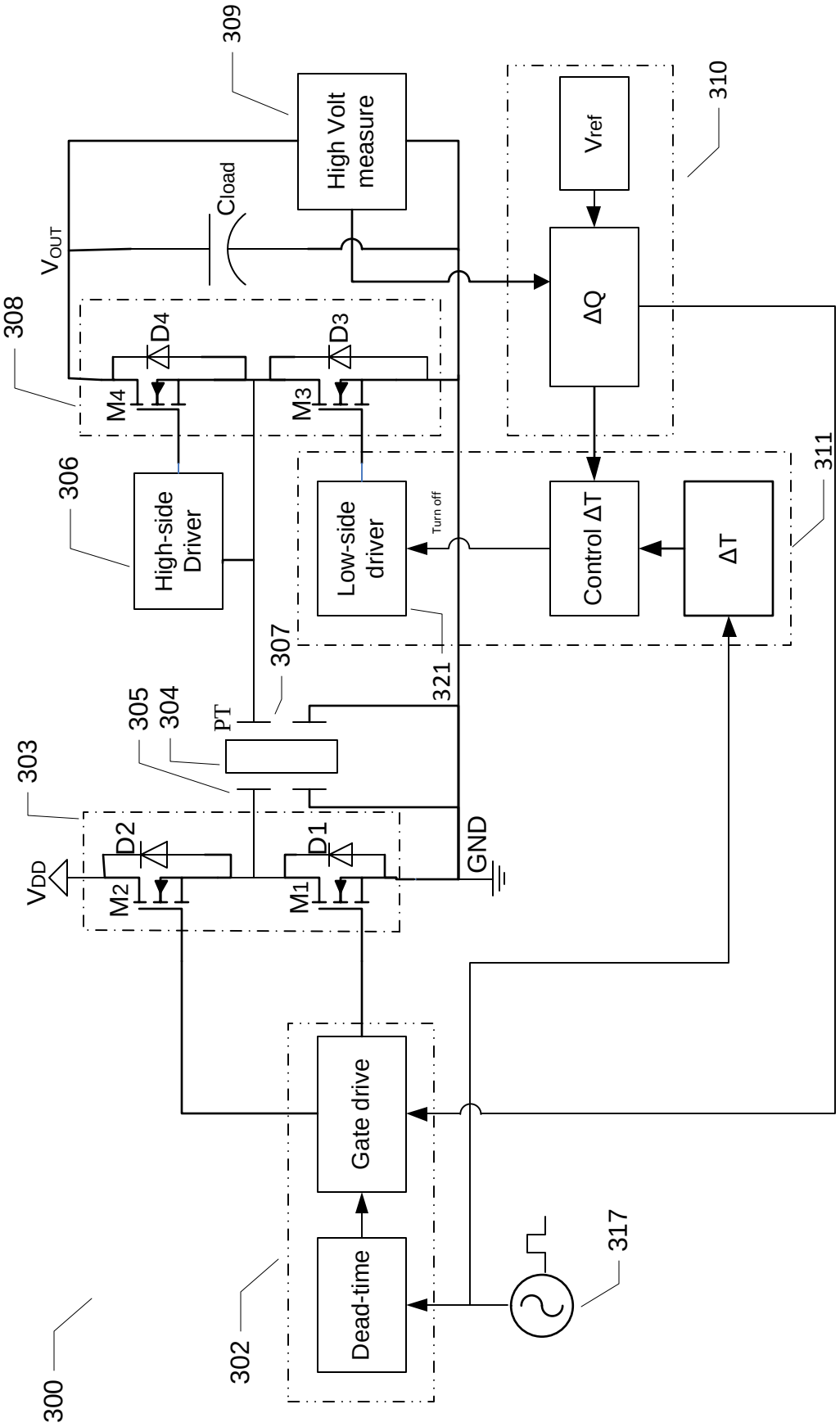
106
VOUT
Iboot
201
VR
207
M4
D4
R
D1a
D1b
Timer
Off
Gate drive
On
GND
V_local
205
Current sense
R
Clocal
203
209
107
Gnd_local

Fig. 2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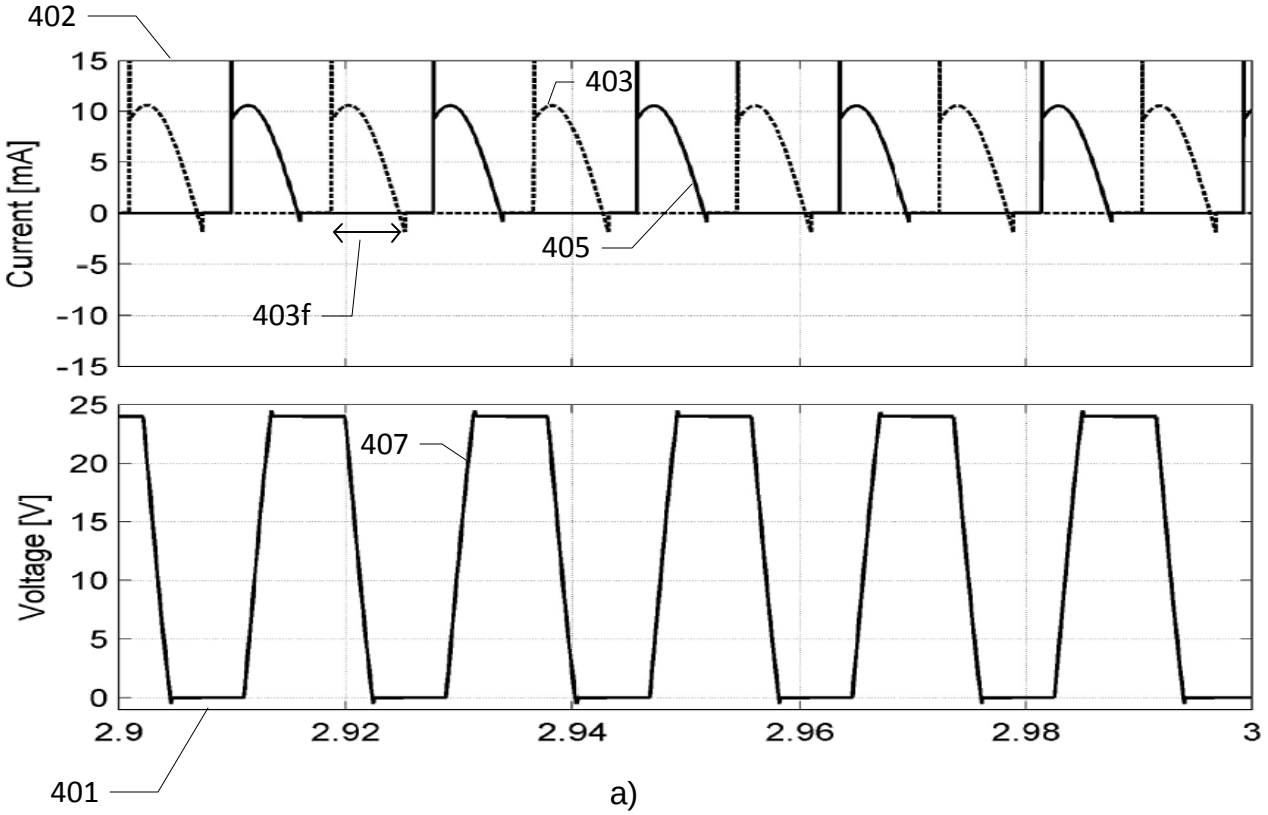
High Volt measure
Cload
V_{OUT}
310
V_{ref}
ΔQ
308
D4
D3
M4
M3
306
High-side Driver
Low-side driver
Turn off
Control ΔT
ΔT
311
307
321
305
304
PT
303
D2
D1
V_{DD}
M2
M1
GND
Gate drive
Dead-time
317
302
300

Fig. 3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403
405
403f
407
401
Current [mA]
Voltage [V]
15
10
5
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-5
-10
-15
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20
15
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5
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2.9
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2.94
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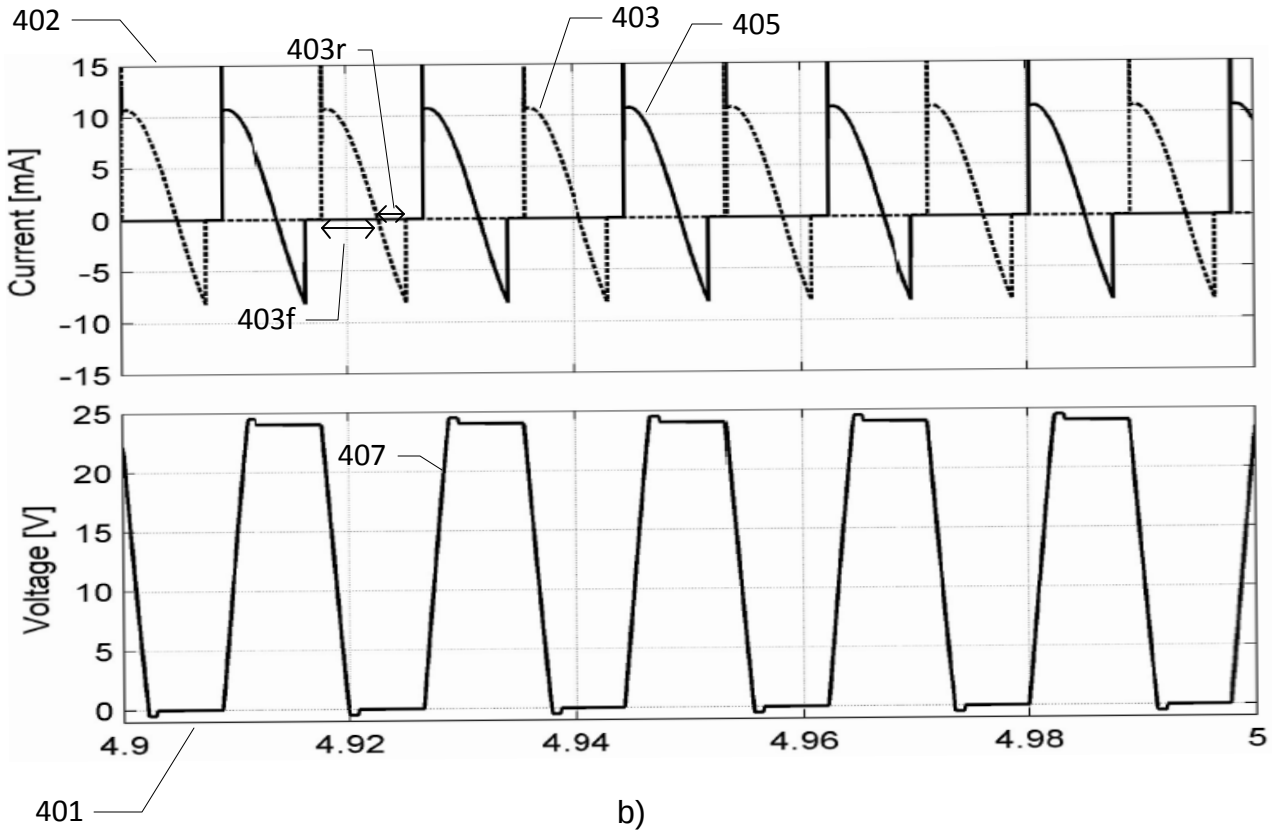
3

a)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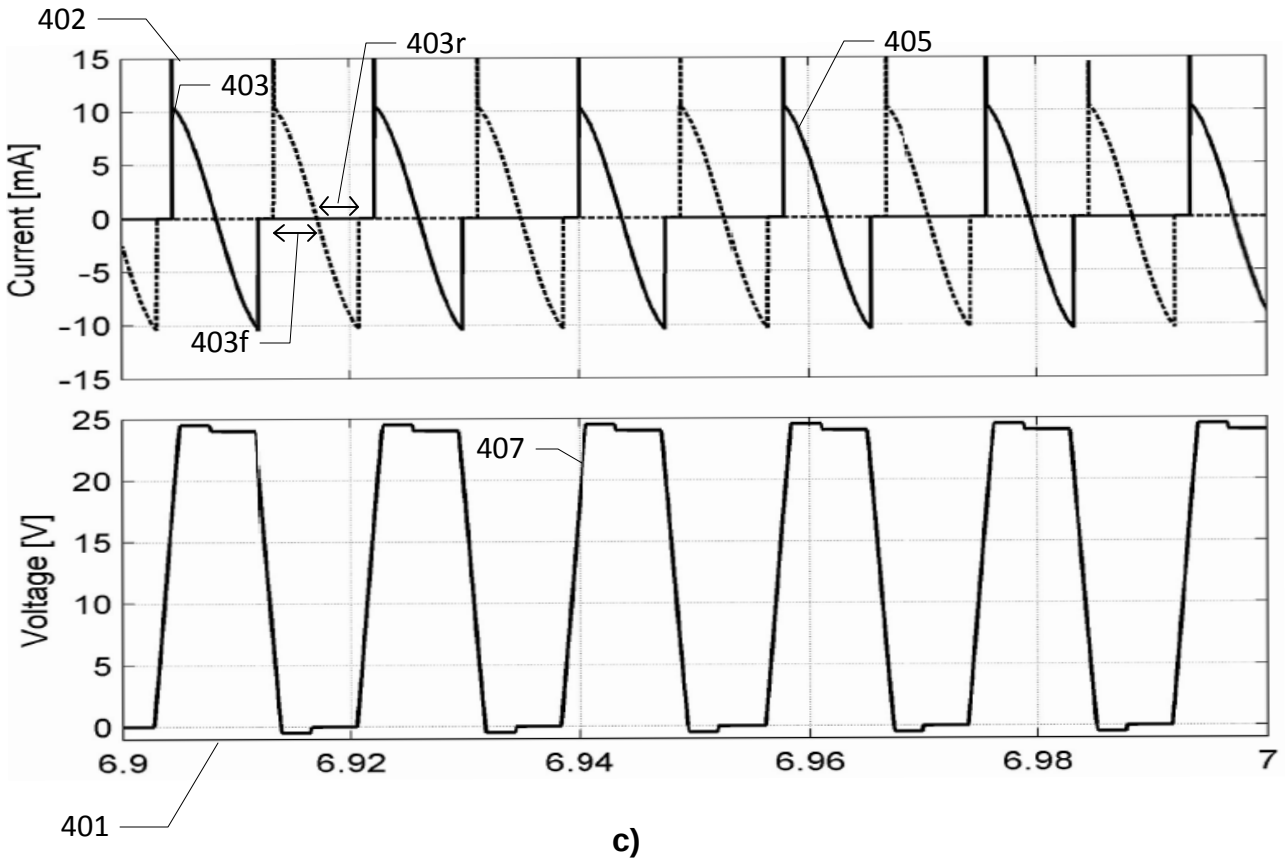
403r
403
405
403f
407
401
Current [mA]
Voltage [V]
15
10
5
0
-5
-10
-15
25
20
15
10
5
0
4.9
4.92
4.94
4.96
4.98
5

b)

Fig.4a)-b)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Current [mA]
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0
-5
-10
-15
407
Voltage [V]
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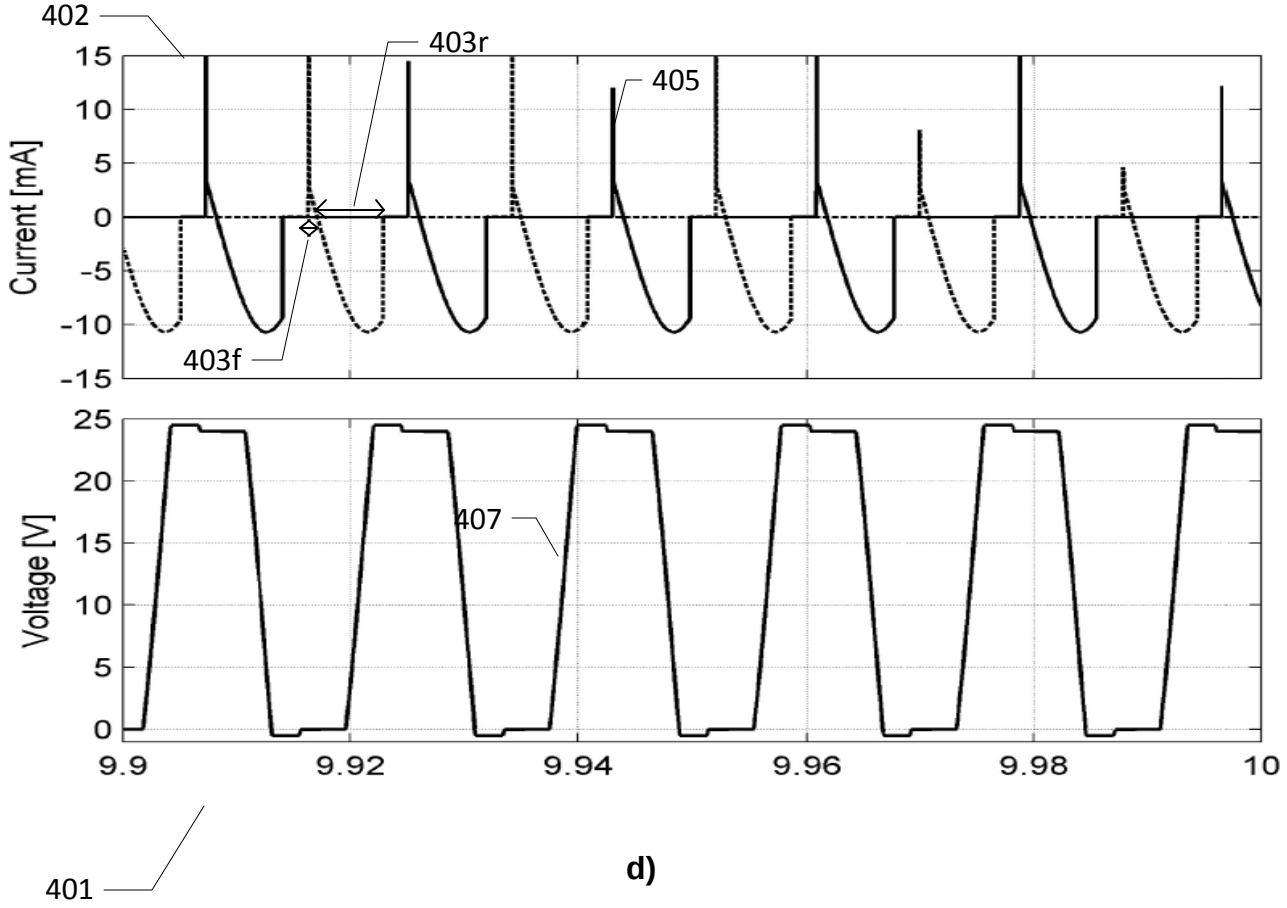
20
15
10
5
0
6.9
6.92
6.94
6.96
6.98
7
401

c)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Current [mA]
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10
5
0
-5
-10
-15
407
Voltage [V]
25
20
15
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5
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10
401

d)

Fig. 4 c)-d)

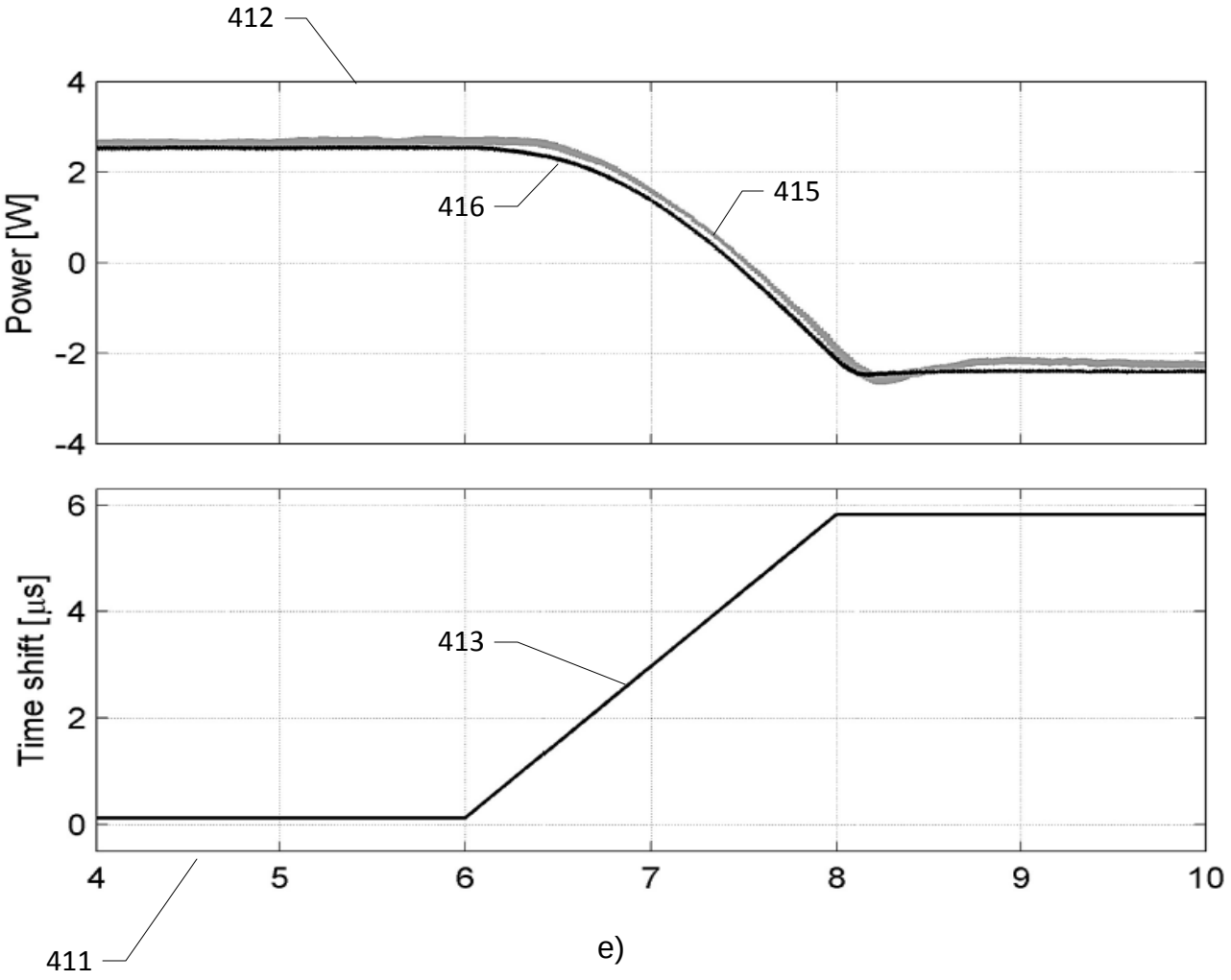
412
Power [W]
4
2
0
-2
-4
416
415
Time shift [µs]
6
4
2
0
413
4
5
6
7
8
9
10
411
e)

Fig. 4 e)

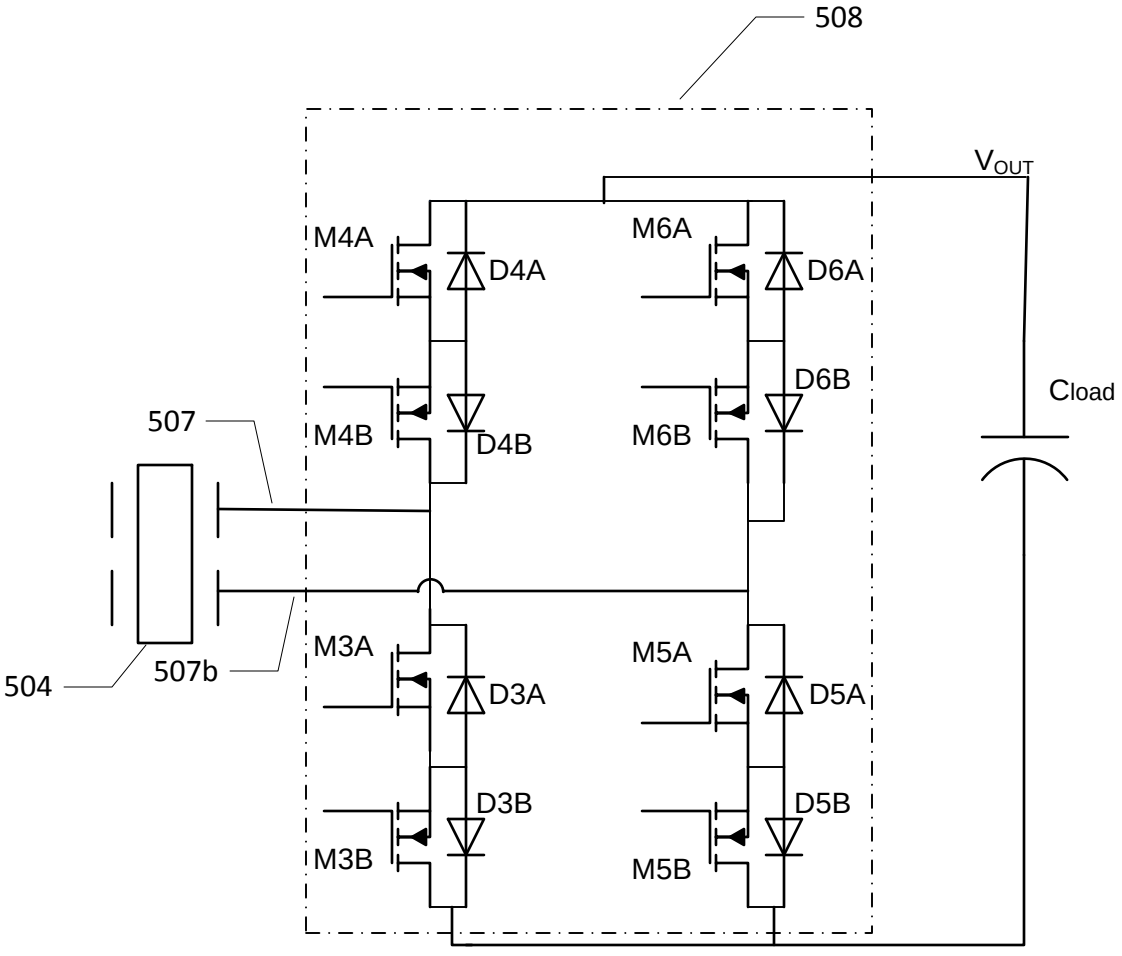
508
V_{OUT}
M4A
D4A
M6A
D6A
D6B
Cload
507
M4B
D4B
M6B
M3A
M5A
D3A
D5A
504
507b
D3B
D5B
M3B
M5B

Fig. 5

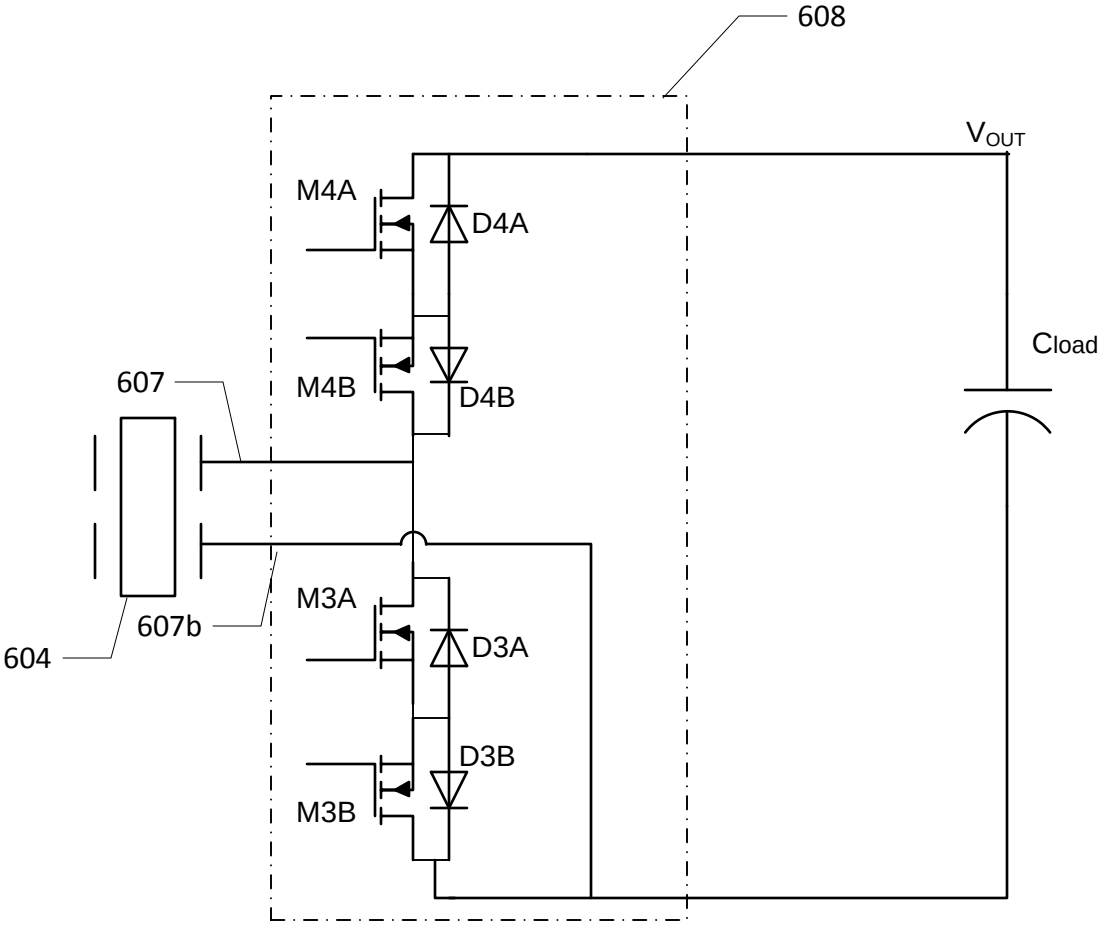

Fig. 6

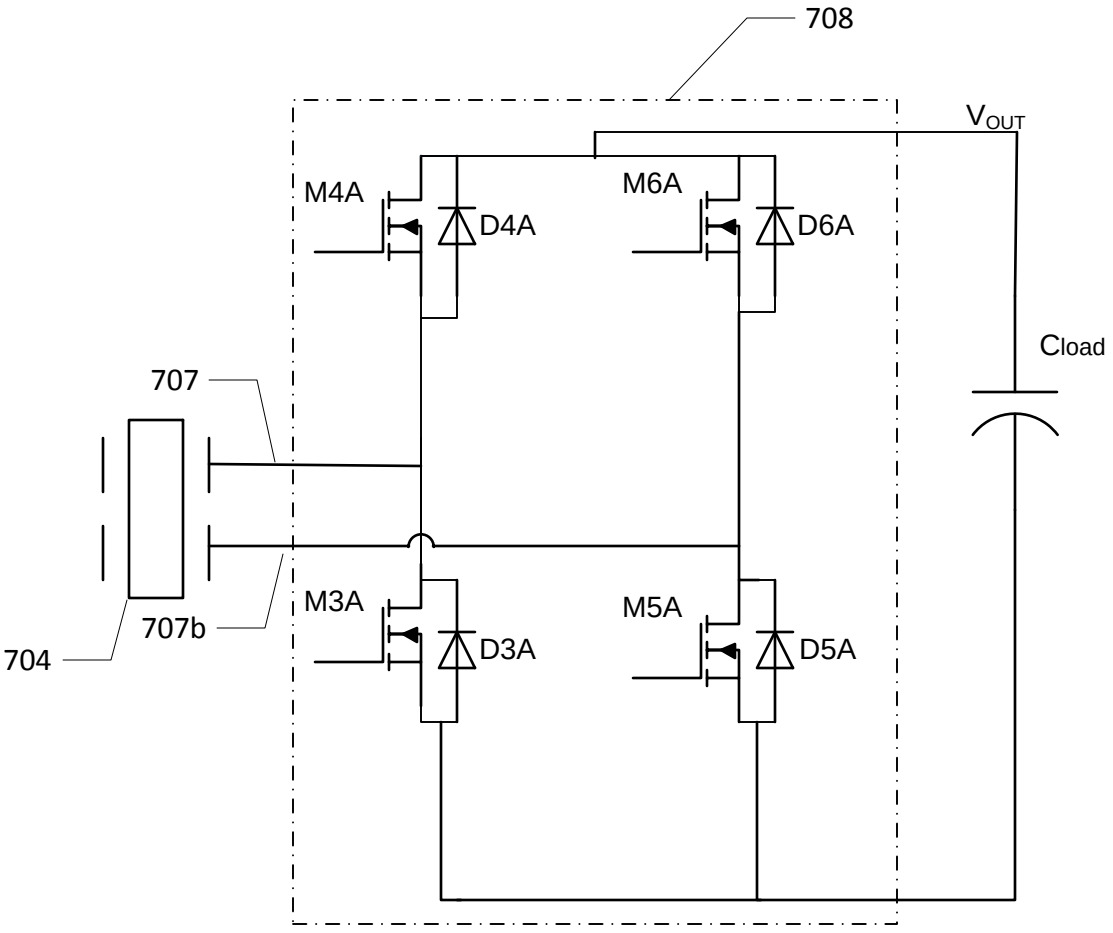

Fig. 7

Appendix: A11

T. Andersen, M. A. E. Andersen O. C. Thomsen, M. P. Foster and D. A. Stone, "A capacitive level shifter for high voltage (2.5kV), accepted for IPMHV & submitted to IEEE Transactions on Power electronics, 2012.

A capacitive level shifter for high voltage (2.5kV)

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Keywords: Half-bridge, gate driver, high side

Abstract

A capacitive level-shifter as a part of a high voltage half-bridge gate driver is presented in this work. The level-shifter utilizes a differential capacitor pair to transfer the information from low side to high side. A thorough evaluation of the critical parts of the level-shifter is presented with focus on low power consumption as well as low capacitive load between the floating half-bridge node and ground (output capacitance). The operation of the level-shifter is tested and verified by measurements on a prototype half-bridge gate driver. Results conclude stabile operation at 2.44kV, 50kHz with a current consumption of 0.5mA. Operation voltage was limited by test equipment. The output capacitance is 4pF@1.5kV.

1 Introduction

Within power electronics the trend goes for both smaller and more efficient power supplies. In modern switch mode power supplies the preferred switching element is the MOSFET. To achieve high efficiency it is necessary to control the MOSFET fast. Slow turn-on or turn-off increases losses and will decrease efficiency. MOSFETs are controlled by charging or discharging its gate-source capacitance. The turn-on time is then a function of the charge per time that can be delivered to the gate of the MOSFET. Special circuits intended for delivering these fast charges are known as gate driver circuits, which usual are controlled by a logic input signal.

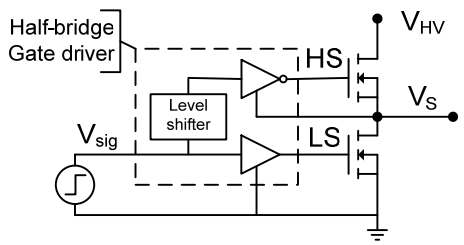

Figure 1: Principle of a half-bride gate driver with two ordinary drivers separated by a level-shifter circuit

MOSFETs are either of the N-channel type or the P-channel type. However the performance of N-channel devices is better than P-channel. Especially regarding devices for breakdown voltage above 400 volts the P-channel type is rarely to be found. In a half-bridge topology working above 400 volts this means a natural choice of two N-channel MOSFETs. The two MOSFETs can easily be controlled by a half-bridge gate driver circuit. A half-bridge gate driver consist of a level-shifter circuit and two ordinary gate driver circuits, one for the low side (LS) MOSFET and one for the high side (HS) MOSFET. The level-shifter circuit translate the logic ground referred input signal (V_{sig}) to an input signal for the HS gate driver with reference to the half-bridge voltage (V_S). Figure 1 illustrates the principle of the half-bridge gate driver.

The focus in this work is related to the level-shifter circuit. In particular intended for half-bridge gate driver applications but not limited thereby.

1.1 Level-shifter topologies

Within power electronic a level shifter is a circuit there is able to transfer a signal with one reference to another reference; a shift in reference level. A level shifter circuit can be made in many ways depending on application, frequency range, power consumption, voltage ranges and so on. Commercial available level-shifters are based on magnetic, semiconductor or optical solutions. However capacitive or piezoelectric [1, 2] solutions is also a possibility.

The semiconductor based level-shifter is used in the majority in all IC gate drivers. The benefits are high speed, low power consumption, small physical size and low cost [3-5]. However the breakdown voltage of silicium based semiconductors limits the working voltage of commercial half-bridge gate drivers to 1200 volts. For voltages above 1200 volts magnetic based level-shifters can be used [6]. Magnetic based level-shifters relies on an electromagnetic coupling e.g. like a transformer with or without a core [7-9]. A transformer solution can also provide power along with the level-shift and thereby function as high side power supply. An alternative is optical based level-shifters [10]. The isolation strength of optical solutions is better than the semiconductor based. However optical solutions are a trade-off between operating frequency, power consumption and price. Capacitive based level-shifters [11] are not common used as other alternatives exist for general propose applications. Other exotics solutions are based on piezoelectric coupled material and uses sound waves to perform the level shift.

The motivation for this research is the need for a half-bridge gate driver with the following specifications: Working voltage (V_{HV}) up to 2.5kV, no magnetic components are allowed, average current consumption of high side circuit below 5mA and a capacitive load between the floating half-bridge to ground below 5pF (output capacitance). However the gate driver is only intended to operate at 50% duty cycle at all time with a switching frequency of 50kHz. The specifications are summarized in table 1.

Parameter	Value	Symbol
Working voltage	2.5kV	V_{HV}
Magnetic components	no	-
High side consumption	< 5mA	I_{HS}
Output capacity	< 5pF	C_{output}
Switching frequency	50kHz	f
Duty cycle	50%	-

Table 1: Initial specifications for half-bridge gate driver

In this work the capacitive based level-shifter solution is investigated.

2 Level-shifter design

The level-shifter is based on a pair of capacitors providing the isolation barrier. A differential square wave signal is feed into the two capacitors to a voltage limiter on the high side. The voltage limiter protects the input of the differential amplifier. The single ended output of the differential amplifier is further buffered and amplified before a Schmitt-trigger converts the signal to a digital output. Figure 2 illustrates the principle of the capacitive level-shifter.

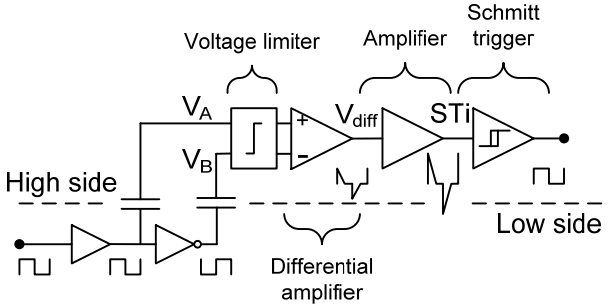

Figure 2: Principle diagram of a capacitive based level-shifter driven by a differential square wave signal

The level-shifter is based on a capacitive coupling between low side and high side. The high side circuitry has its reference to the half-bridge voltage (V_S). Any signal from the low side through the capacitive coupling, is by the high side, compared to V_S. However, the high side circuit is unable to distinguish between a changes in the low side signal and disturbance in V_S. Therefore a differential approach with two capacitors and a differential amplifier is used. Any change in V_S will still have an influence on the common mode potential however the differential (V_A-V_B) signal is unchanged.

In the following sub chapters each block from figure 2 of the level-shifter is discussed in details.

2.1 Differential capacitor pair

The differential capacitor pair is the main component in the level-shifter. The dielectric strength of the capacitors must exceed 2.5kV according to the application specifications (Table 1). The immunity to V_S disturbances depends on two parameters: First the common mode rejection of the differential amplifier and secondly the symmetry of the differential capacitor pair and the voltage limiter. Assuming the common mode rejection of the differential amplifier is sufficient for the input range, limited by the voltage limiter, the symmetry of the capacitor pair is alone responsible for the immunity to V_S disturbances.

Matched capacitors in the picofarad range with an absolute tolerance below 5% and rated for more than 2.5kV is not standard components. Instead of series connecting of bunch low voltage, low drifting, high precision, temperature stabile capacitors without mention voltage balance issues, it is decided to make a plate capacitor with standard 1.6mm PCB as dielectric material. According to the IPC-4101B/97 standard the dielectric breakdown is minimum 40kV for laminates above 0.5mm. The dielectric strength of the PCB is sufficient to withstand the 2.5kV.

Each capacitor consists of two round plates (pads) placed on each side of a PCB and then aligned on top of each other. The spacing is fixed by the thickness of the PCB. The capacity can be calculated by the simple equation for a parallel plate capacitor (1). C is capacitance, epsilon is permittivity, S is surface area and d is distance.

$$C_{simple} = \varepsilon_0 \varepsilon_r \frac{S}{d} \quad (1)$$

For a FR-4 class PCB the relative permittivity is approximate 4.7. The thickness of the PCB is 1.6mm. With a plate radius of 1.7mm the capacitance is calculated in equation (2).

$$C_{simple} = 8.85\frac{pF}{m} \cdot 4.7 \cdot \frac{2\pi(1.7mm)^2}{1.6mm} = 0.24pF \quad (2)$$

However the fringe field is not encountered in the simple equation for the parallel plate capacitor (1). A finite element analysis of the same problem, that encounters the fringe field, see figure 3. The result is given in equation (3). An increase of 23% compared to the capacitance calculated by the simple equation (2).

$$C_{FEM} = 0.31pF \quad (3)$$

The large difference in capacitance is due to relative small ratio between the plate's surface area and their separation distance. As this ratio becomes small the impact from the

fringe field becomes high and the standard equation (1) becomes more inaccurate.

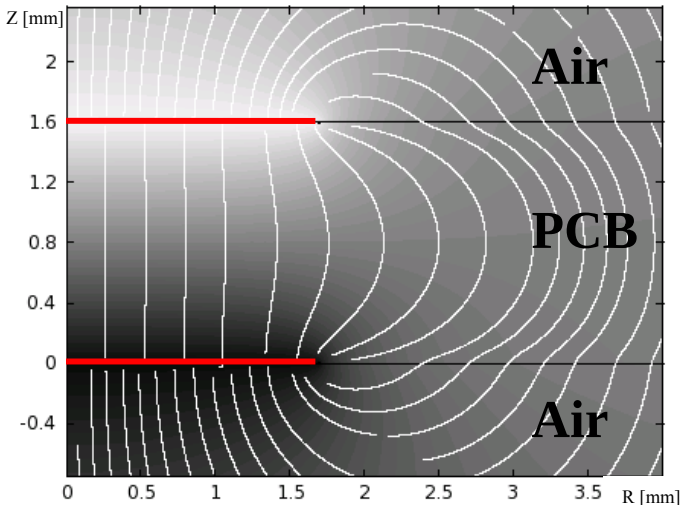

Figure 3: 2D axis-symmetric FEM simulation of two round plates with a radius of 1.7mm, separated by 1.6mm thick PCB (ε_r: 4.7), surrounded by air (ε_r: 1.0) and with a potential difference of 1 volt. Capacitance = 0.31 pF Gray-scale surface: electric potential, streamlines: Electric field.

2.2 Voltage limiter and anti-saturation

The function of the voltage limiter is to limit the input voltage to the differential amplifier to avoid saturation and to increase the symmetry of the two differential signal paths.

Saturation of the differential amplifier can indirect lead to an unwanted re-triggering of the high side. Re-triggering is when the output of the high side makes a transition and short after makes a transition back again. This results in a short transient instead of a constant signal at the output. At every transition the half-bridge voltage changes by up to 2500 volts (V_{HV}). Without a voltage limiter the common mode voltage at the input to differential amplifier (V_{diff}), referred to V_S, would be equal to (5) at every transition on the half-bridge. 2500 volts will both saturate and destroy the differential amplifier.

$$V_{diff} = V_A - V_B \tag{4}$$

$$V_{diff} - V_S = \pm\left(V_{HV} \pm V_{sig}\right) \tag{5}$$

The explanation for this high input voltage is the energy storage of differential capacitor pair. To limit the voltage a configuration of anti-parallel diodes are used as seen in figure 4. Ideally the two input voltages (V_A,V_B) to the differential amplifier would be limited equally for both positive and negative overvoltage. However tolerances and temperature affect the forward voltage drop of each diode and lead to a voltage difference when they limit the voltage. This voltage difference might lead to an unintended turn-off or turn-on of the high side switch.

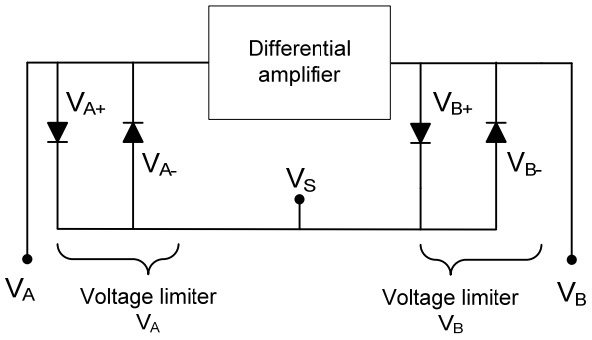

Figure 4: Anti-parallel diodes limits over- and under voltages

Six different situations exist dependent on V_S and the diodes individual forward voltage drop. The situations are divided into two groups for either a decrease or an increase in V_S.

Figure 5 sketch the situation where the low side switch turns on and pull V_S down. With an equal voltage limit for V_{B+} and V_{A+} the high side output (HS) is unaffected by the decrease in V_S. When $V_{B+} > V_{A+}$, a decrease in V_S will try to turn off HS, however HS is already turned off and nothing changes. When $V_{B+} < V_{A+}$, a decrease in V_S will try to turn on HS. If the Schmitt-trigger input (STi) is triggered, HS turns on and a fatal shoot-through occurs. To avoid shoot-through the forward voltage drop of V_{B+} has to be equal or greater than V_{A+}.

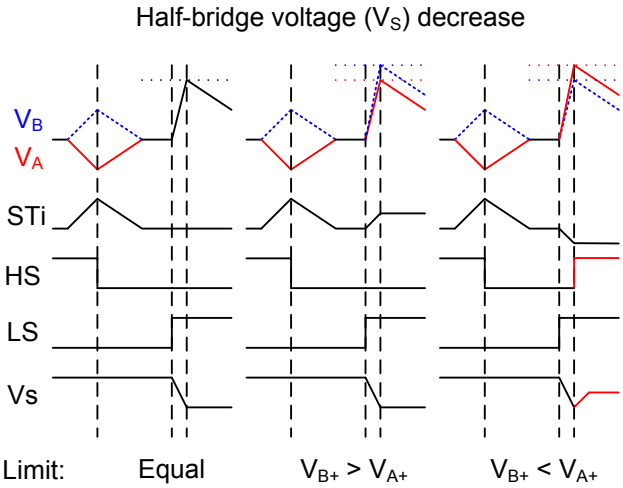

Figure 5: Simplified sketch of waveforms for different voltage limiter cases. In the $V_{B+} > V_{A+}$ case the high side is unintended turned on when the low side turns on and pull V_S down. As a result shoot-trough occurs.

Figure 6 sketch the situation where HS turns on and pull V_S up. With an equal voltage limit for V_{B-} and V_{A-}, HS is unaffected by the decrease in V_S. When $V_{B-} > V_{A-}$, an increase in V_S will try to turn off HS and the result is a short HS pulse. When $V_{B-} < V_{A-}$, an increase in V_S will try to turn on HS but HS is already turned on and nothing changes. However if the half-bridge gate driver is used in an zero voltage switching (ZVS) topology, the dead-time before HS turns on is used to

charges V_S. This increase in V_S turns HS on before the dead-time period is over and the ZVS is lost.

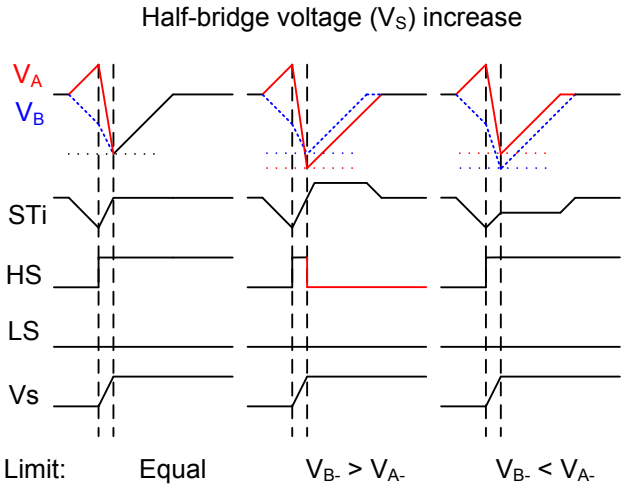

Figure 6: Simplified sketch of waveforms for different voltage limiter cases. In the $V_{B+} > V_{A+}$ case the high side is unintended turned on when the low side turns on.

The six situations for the voltage limiter are summarized in table 2.

V_S	Forward voltage drop	Notes:
Decrease *HS = OFF* *LS -> ON*	$V_{B+} = V_{A+}$	√
	$V_{B+} > V_{A+}$	√
	$V_{B+} < V_{A+}$	HS turn on
Increase *HS -> ON* *LS = OFF*	$V_{B-} = V_{A-}$	√
	$V_{B-} > V_{A-}$	HS turn off
	$V_{B-} < V_{A-}$	√ (ZVS issue)

Table 2: Summarize voltage limiter scenarios.

From the analysis of the relation between the diodes forward voltage drop an asymmetric configuration of the anti-parallel diodes prevent fatal shoot-through and neglect tolerances in the forward voltage drop for the positive overvoltage protecting diodes as seen in figure 7. The protection from negative overvoltage still relies on equal voltage forward voltage drop to ensure compatibility with ZVS topologies.

The asymmetric diode configuration introduces an uneven parasitic capacitance between V_A and V_B. To decrease the influence of the parasitic capacitance two matched capacitors (C_A and C_B) are placed parallel with the anti-parallel diodes.

Forward biasing of the diodes is a protecting state to prevent overvoltage. However the non-linear nature of the conduction diodes jams any signal from the differential capacitor pair. Therefore it is desired to get out of the non-linear protecting state. Two resistors (R_A and R_B) are placed in parallel with the anti-parallel diodes to discharge the junction capacitors of the diodes as well as the additional C_A and C_B. Furthermore the two resistors together with the differential capacitor pair acts as a high pass filter and suppress any low frequency variation from V_S including the transient from the half-bridge changes. This requires the low side differential square wave signals, fed into the differential capacitor pair, to have low rise and fall times otherwise the signal information is lost in the high pass filter.

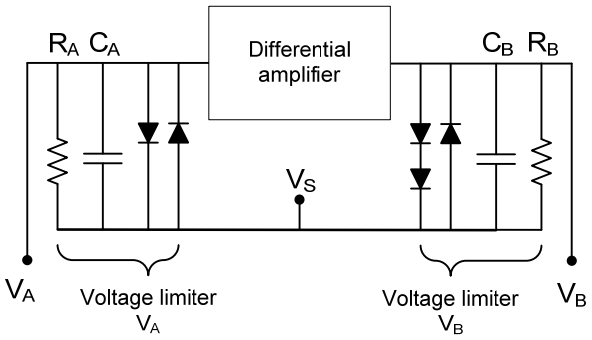

Figure 7: Voltage limiter circuit to avoid saturation and prevent shoot-through. V_A and V_B are connected to the differential capacitor pair.

2.3 Differential amplifier

The differential amplifier translates the differential input to a single ended output. The requirements are low power consumption and high speed. A discrete solution is selected and the schematic is shown in figure 8.

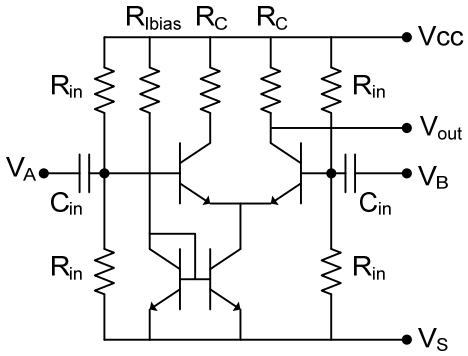

Figure 8: Schematic of differential amplifier.

The input capacitor (C_{in}) together with the bias resistors (R_{in}) creates a high pass filter. To avoid re-triggering the time constant of this filter (τ_{diff}) has to be larger than the time constant of the filter consisting of the differential capacitors pair and the voltage limiter ($\tau_{level\text{-}shift}$). Figure 9 illustrates the situation with a schematic of two high pass filters and a simulation of a 1 volt step response. The ratio between the two time constants is given by "K" (6). The step-response lead to a positive peak (not covered by figure 9) that triggers HS output to turns on. The positive peak is followed by a negative peak. The amplitude of the negative peak is depended on the ratio between the two time constants of the filters (K). If the ratio K is too small the negative under-shoot re-triggers HS output to turn off.

$$\frac{\tau_{diff}}{\tau_{level-shift}} = K \qquad (6)$$

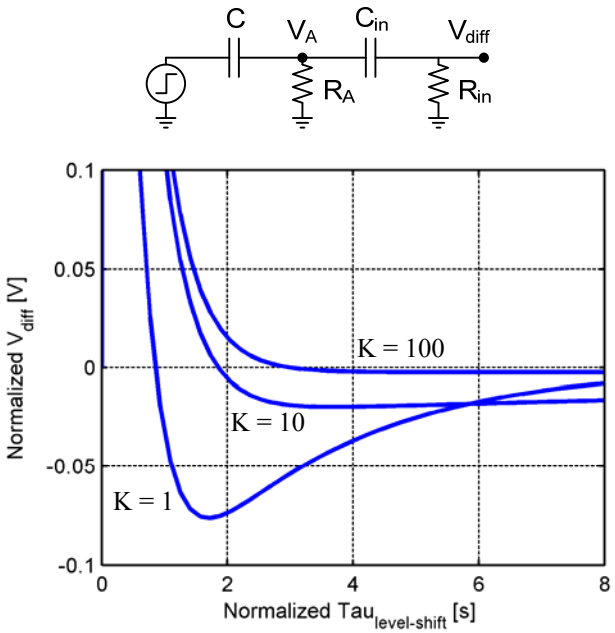

Figure 9: Interconnecting of filters lead to an under-shoot that can re-trigger the HS output. The amplitude of the under-shoot depends on the ratio between the time constants of the filters

The optimum value of K is a trade-off. A small K can lead to re-triggering, however a large values of K is equivalent to long time constants and therefore long start-up times to stabilize bias points for proper operation.

2.4 Gain amplifier

The differential amplifier output is a single ended signal with reference to V_S. The amplitude of the signal is to low and the output impedance to high to feed the signal directly to the Schmitt-trigger. A two stage amplifier is used to buffer and amplify the signal. A common collector stage with high input impedance buffers the signal and a common emitter stages amplify the signal. The two stages are separated by a capacitor (C_{eb}) in order for proper DC-biasing. The capacitor in combination with the bias resistors creates another high pass filter. To avoid any re-triggering the time constant of this filter (τ_{gain}) has to be equal or greater than the time constant of the differential amplifier (τ_{diff}). Figure 10 shows the schematic of the amplifier.

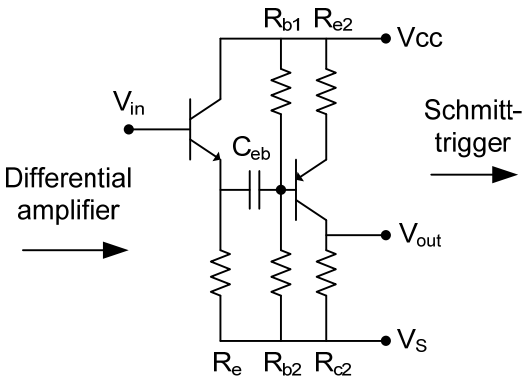

Figure 10: Two-stage amplifier schematic.

2.5 Schmitt-trigger

The output signal from the amplifier consists of a DC signal with positive and negative transients. Each transient signals a turn-on or turn-off depended on the polarity of the transients. However smaller unintended transients can occur e.g. from the fact of finite filter time constants, capacitive coupled EMI or insufficient common mode rejection in the differential amplifier. To suppress noise an upper and lower threshold, symmetric around the DC signal, is provided by the Schmitt-trigger circuit. Only transients with amplitudes greater than this threshold will trigger the HS output.

To get the thresholds of the Schmitt-trigger symmetric around the DC level, a biasing circuit of two resistors and a coupling capacitor is used. Again the time constant of the equivalent high pass filter has to be large enough to avoid re-triggering. For the prototype an integrated solution for the Schmitt-trigger is selected: SN74AUP1G14. It requires a supply voltage of approximately 3 volts. The supply circuit and the Schmitt-trigger circuit are illustrated separately in figure 11.

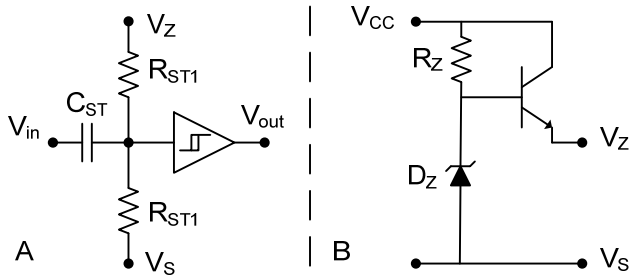

Figure 11: A: Schmitt-trigger circuit. B: Voltage supply circuit for Schmitt-trigger circuit

2.6 Level-shifter summary

An overview of the level-shifter with the individual circuits put together in the same circuit diagram is showed in figure 12.

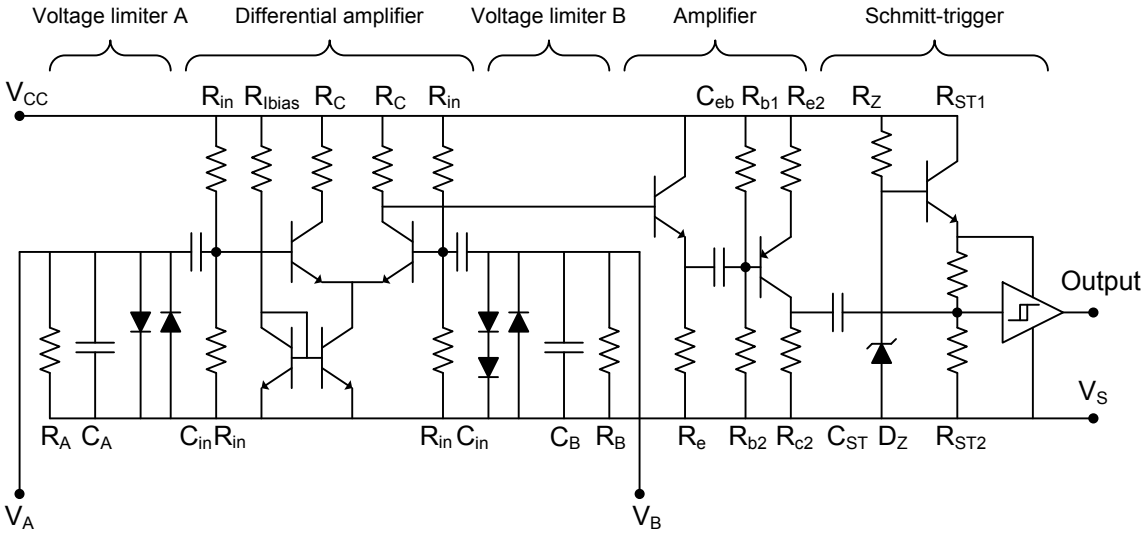

Figure 12: Schematic of the capacitive level-shifter circuit. The differential capacitor pair is not included in the schematic.

3 Half-bridge gate driver

Beside of the level-shifter circuit the half-bridge gate driver circuit consists of a signal conditioning circuit, a low side driver, a high side driver and a power transfer circuit to the high side circuitry.

The signal conditioning circuit provides dead time, compensates uneven propagation delays for high and low side and deliver the differential signal to the level-shifter. Propagation delay compensation is out of the scope of this work and will not be treated further. To implement equal dead-time for low and high side a commercial half-bridge driver IC is used: IR21091. The high side section of IR21091 is connected to ground. The output is two signals in antiphase with respect to ground and adjustable dead time. The inverted output signal is driving the low side MOSFET directly. The non-inverted output signal is driving an inverter (MCP1401) together with one of the differential capacitors. The output of the inverter (MCP1401) drives the other differential capacitors. Figure 13 illustrates how the low side circuit is connected.

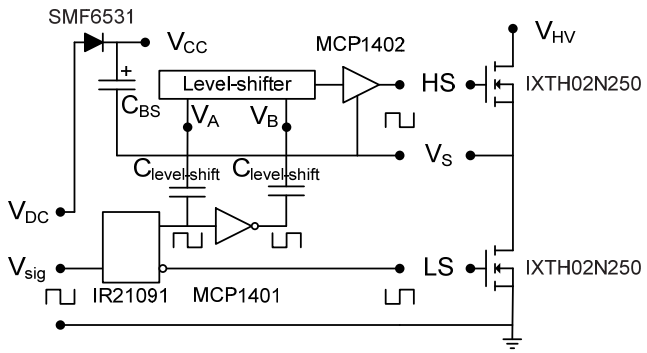

Figure 13: Block diagram of the half-bridge gate driver, implemented with capacitive level-shifter.

The output signal of the level-shifter is not designed to drive the gate of a MOSFET directly. A low side gate driver (MCP1402) with reference to V_S is used as buffer between the level-shifter and the high side MOSFET.

The high side circuitry requires energy to operate. The energy is transferred from the low side power supply via boot-strapping. The boot-strap diode is an essential part of the design to maintain a low output capacitance. The output capacitance is equivalent to the capacitance between high side and ground and is given by (7).

$$C_{output} = C_D + 2 \cdot C_{level-shift} + C_{surroundings} \qquad (7)$$

C_D is the parasitic capacitance parallel to the boot-strap diode. Furthermore, the breakdown voltage of the diode must be above 2.5kV. The selected diode for the prototype is a SMF6531 form VMI.

$C_{level\text{-}shift}$ is the capacitance of the differential capacitor pair given by (3). $C_{surroundings}$ is the capacitance of the high side circuit to the surroundings. Every conducting object has a capacitance to the surroundings. This capacitance depends on geometry, volume, materials and distance to ground.

4 Results

4.1 A word about measuring

In order to lower the power consumption of the high side circuit, the level-shifter is implemented with high impedances. As a result the high side circuit is easy disturbed by coupling through parasitic capacitance. Even high voltage oscilloscope probes (50MΩ, 6pF) influence the operation of the level-shifter. To prevent EMI and to insure proper operation, the entire high side circuitry is close to fully

shielded with a conducting case on top and cobber plane on bottom. Therefore a lot of the operation of the level-shifter relies on simulations and careful layout design. Only the final operation can be verified by measurements of the half-bridge voltage V_S. At voltages below 1.5kV it is possible to measure the high side gate voltage HS. Above 1.5kV the load of the probe (50MΩ, 6pF) drains too much energy from the boot-strap supply through the high side driver. As a result the ripple amplitude (ΔV) on the high side supply V_{CC} becomes high enough to disturb proper operation. An estimate of the ripple amplitude, if only an oscilloscope probe is connected to the boot-strap supply, can be obtained by consider the energy balance of the circuit (8).

$$\Delta V = V_{CC(dc)} - \sqrt{\frac{C_{BS} \cdot V_{CC(dc)}^2 - C_{probe} \cdot V_{HV}^2 - \frac{V_{HV}^2}{f \cdot R_{probe}}}{C_{BS}}} \quad (8)$$

For an oscilloscope probe (R_{probe} = 50MΩ, C_{probe} = 6pF) attached to the prototype circuit supply (C_{BS} = 1µF, V_{CC} ≈ 10V) in operation (V_{HV} = 2.5kV, f = 50kHz) results in a ripple amplitude of 2.25V. On top of the induced probe ripple comes additional ripple from the high side circuit itself under normal operation.

However, to verify that HS is triggered by the differential low side signal, and not from a V_S transition, an LED with a current limiting resistor is connected between HS and V_S (figure 14).

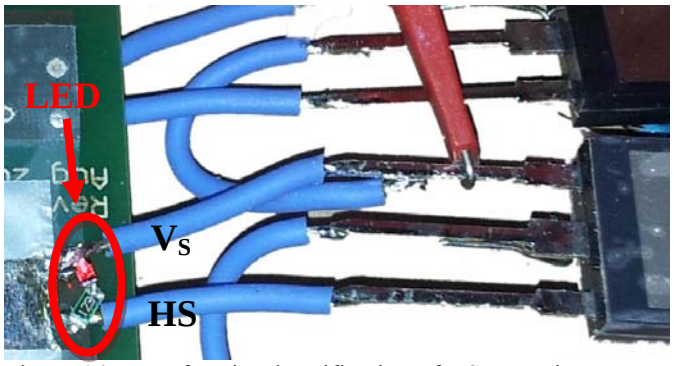

Figure 14: LED for visual verification of HS operation

The average intensity of the emitted light from the LED is proportional to the duty cycle of the high side. Utilizing a dead time of 25% and a V_S duty cycle of 50% the duty cycle of HS under normal operation is 25%. A continuing error: re-triggering or EMI triggering from V_S will result in a steady change of HS duty cycle (< 1% and ≈ 50% respectively). By visual inspection with the human eye a change in light intensity is easy spotted.

4.2 Half-bridge gate driver in operation

Figure 15 is an oscilloscope plot of the half-bridge gate driver in operation. The input voltage V_{DC} for the gate driver is 17 volts and the switching frequency is 50kHz with a duty cycle of 50%. In the plot the trace for the HS output (HS-V_S) is measured with a differential probe. Despite the asymmetry of the differential probe it can be verified that the level-shifter is only trigger by the differential signal and no re-triggering occurs.

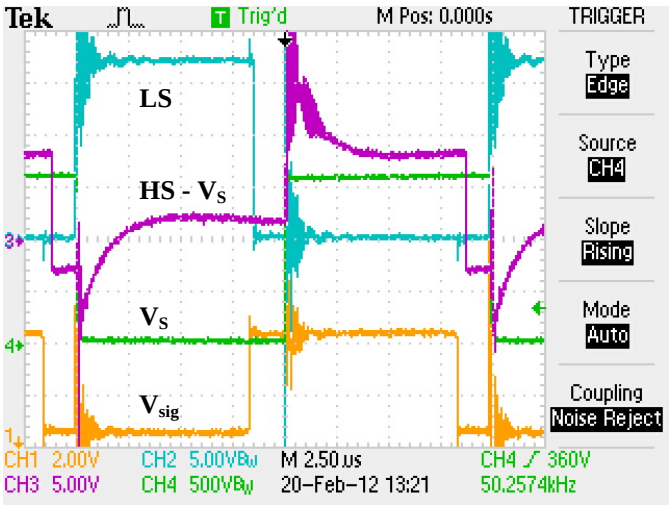

Figure 15: Half-bridge gate driver operating at 1.6kV@50kHz. HS output is trigger correct.

Figure 16 shows the half-bridge gate driver working at 2.44kV. The voltage is limit by the high voltage supply used in this measurement. At this voltage it is not possible to measure at HS output with an oscilloscope probe. A visual validation indicates correct operation.

4.3 Switch frequency and transition times

Exploring the limit of the gate drivers switching frequency is demanding for the high voltage power supply and the MOSFETs. The high voltage supply is limited to around 13 watts. Hard switching of V_S dissipates all the energy stored in the parasitic capacitance in the MOSFETs. To limit the power demand the output voltage is fixed to 1.5kV. To further increase the switching frequency without increasing the power demand a duty cycle of 15 % is used to simulate a 50% duty cycle of the high side at a 3.33 times higher switching frequency.

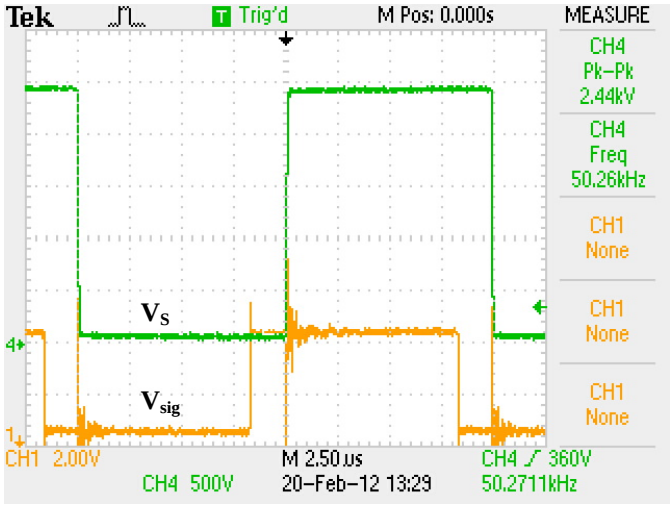

Figure 16: Half-bridge gate driver operating at 2.44kV@50kHz (limited by high voltage supply). HS output is verified by LED inspection.

The switching frequency is limited by the minimum dead time of the IR21091 chip. When the dead time period exceeds the on-period, no output transient occurs. At 220kHz and 15% duty cycle the on-period is equal the minimum dead time of IR21091: 680ns.
Figure 17 shows an oscilloscope plot of the half-bridge gate driver at 1.5kV with a switching frequency of 210kHz and a duty cycle of 15%. 210kHz and 15% duty cycle is equivalent to the high side switching at 700kHz at 50% duty cycle.

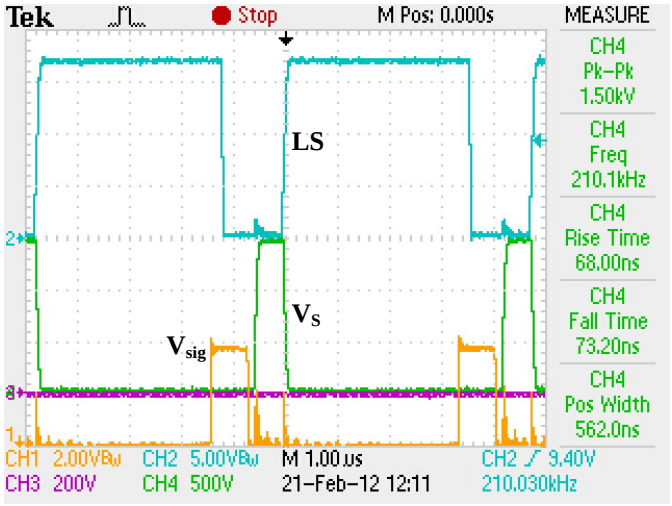

Figure 17: Half-bridge gate driver operating at 1.5kV with a switching at 210kHz, duty cycle: 15%. Equivalent to a high side duty cycle of 50% at 700kHz.

The transition times of the half-bridge voltage depend a lot on the MOSFETs themselves. The rise and fall time at different voltages of V_{HV} is plotted in figure 18. The half-bridge node is only loaded by the oscilloscope probe (50MΩ, 6pF). At 2.5kV the transition times are both below 100ns given a dv/dt > 25kV/µs.

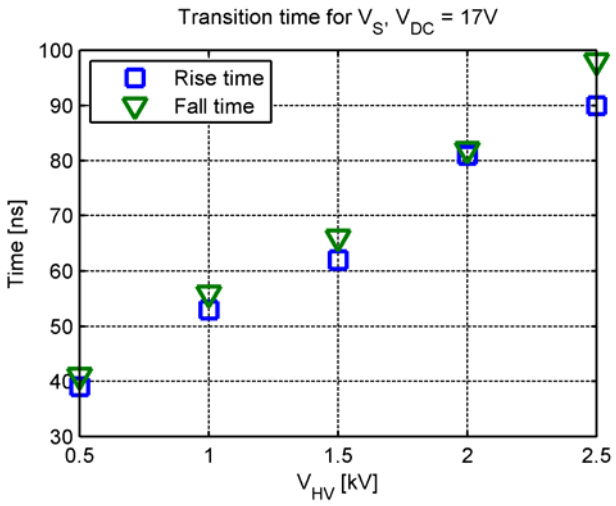

Figure 18: Rise and fall times for the unloaded prototype

4.4 Current consumption

The static current consumption distribution of the high side is measured with V_S = 0V and the result is visualized in figure 19. The static current consumption of the level-shifter alone is approximately 500µA and is independent of the state of HS.

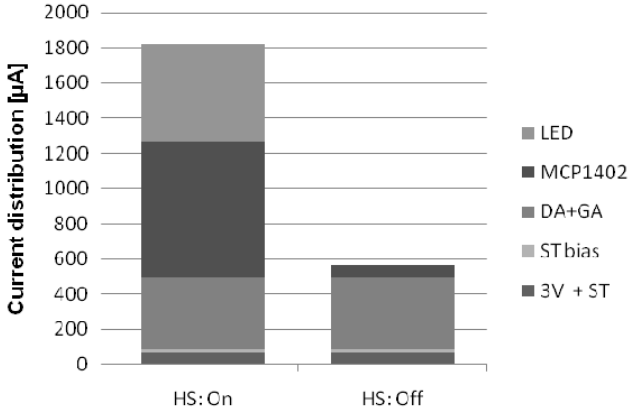

Figure 19: Static current consumption distribution of the high side circuit, V_S = 0V, V_{DC} =12V (V_{CC} ≈ 10.2V)

The dynamic current consumption of the entire half-bride gate driver in action at various voltages is plotted in figure 20.

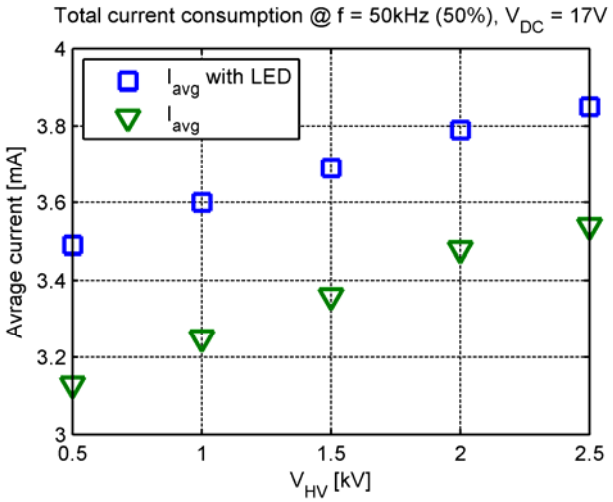

Figure 20: Average current consumption of half-bridge gate driver included drive of MOSFETs as a function of operating voltage. Frequency: 50kHz, Duty cycle: 50%, V_{DC}: 17V

At 2.5kV and a switching frequency of 50kHz the average current consumption is below 3.6mA including drive of MOSFETs (C_{iss}=120pF).

4.5 Output capacitance

The output capacitance is defined as the capacitance between the high side circuitry and ground. The output capacitance is evaluated in equation (7) and for readability repeated in (9). The junction capacitance of the boot-strap diode (C_D) is stated in the datasheet to 2pF measured at 25V, however junction capacitance is voltage depended and non-linear with voltage and the diode is operated up to 2.5kV. Therefore a lower capacitance than 2pF is expected. The level-shift capacitance is calculated in (3).

$$C_{output} = C_D + 2 \cdot C_{level-shift} + C_{surroundings} \quad (9)$$

$C_{surroundings}$ is the capacitance of the high side circuit to the surroundings. It is complicated to calculate the exact capacitance even with FEM simulations, because of the complex geometries involved. However, an approximate measure of the minimum capacitance can be estimated by assuming the volume of the high side circuitry is spherical with an infinity distance to the surround ground. The minimum capacitance is then calculated from the infinity spherical capacitor equation (10) [12].

$$C = 4\pi\varepsilon R \quad (10)$$

R is the radius of the sphere. The resulting capacitance is the absolute minimum capacitance a given conduction sphere can have. The volume of the high side (Vol) is equal to the volume enclosed by the shielding case, see figure 21.

$$Vol = 27.6mm \cdot 23.8mm \cdot 12.6mm = 8.28\mu m^3 \quad (11)$$

The equivalent radius for a sphere with the same volume is given by equation (12).

$$R = \sqrt[3]{\frac{3 \cdot Vol}{4\pi}} = 12.55mm \quad (12)$$

The resulting capacitance (13) is equal to the minimum obtained capacitance for a sphere with same volume as the shielded high side circuit.

$$C_{surroundings} \geq 1.40\,pF \quad (13)$$

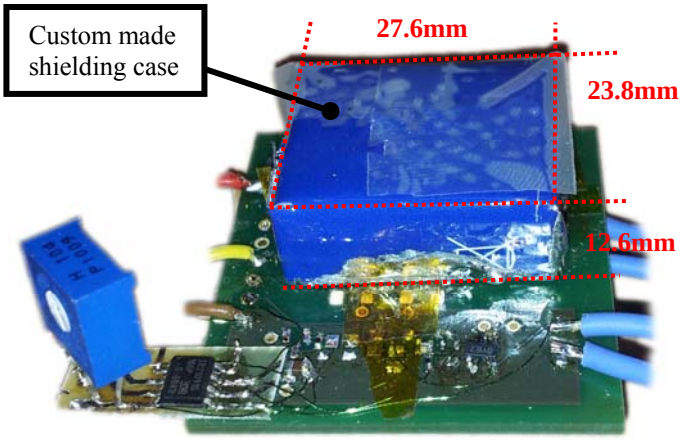

Figure 21: 2.5kV Half-bridge gate driver prototype. PCB size 38mm x 38mm. High side circuitry shielded with metal case to prevent EMI.

The output capacitance (C_{output}) is not easy to measure directly at >1kV. Instead the total capacitance (C_{total}) is measured which include the capacitance of both MOSFETs (C_{MOSFET}). The measurement setup is illustrated in figure 22. By knowing the switching frequency, input voltage and input current to the unloaded half-bridge the total capacitance connected to half-bridge node can be calculated.

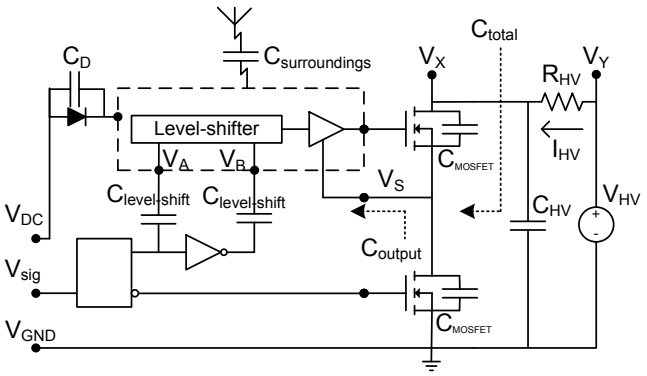

Figure 22: Setup for measuring output capacitance

To simplify the measurement a DC current through R_{HV} is obtained by connecting C_{HV} to supply the AC current for the

bridge. The total capacitance is calculated by equation (14). Even though the measurement of the V_X will increase the current I_{HV} through R_{HV}, this increase is insignificant with a standard oscilloscope probe.

$$C_{total} = \frac{I_{HV}}{V_X \cdot f} = \frac{V_Y - V_X}{R_{HV} \cdot V_X \cdot f} \quad (14)$$

$$C_{total} = \frac{1.93kV - 1.50kV}{270k\Omega \cdot 1.50kV \cdot 50kHz} = 21.2\,pF \quad (15)$$

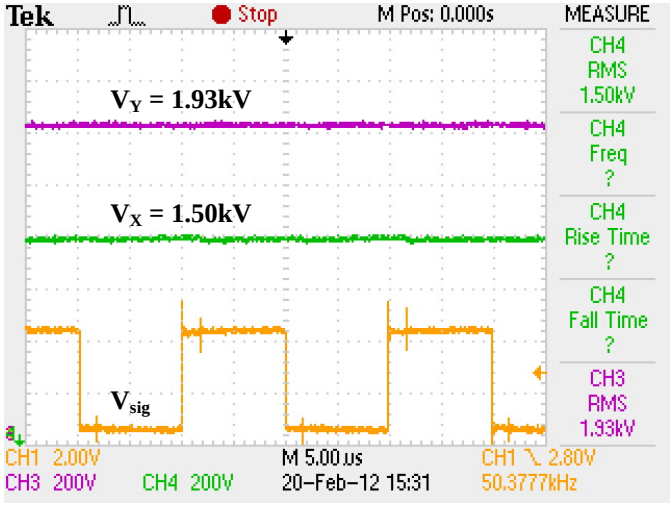

Figure 23: Voltage measurement across R_{HV} of 270kΩ at 50kHz

The total capacitance (C_{total}) at V_S is equal to the sum of the MOSFETs output capacitance (C_{MOSFET}) and the output capacitance of the gate driver (C_{output}) (16). From the datasheet the stated output capacitance of the MOSFET IXTH02N250 is 9pF measured at 25 volts, however the MOSFETs are operated at 1.5kV so it is expected that the actual capacitance is lower. Table 3 summarizes measured and estimated capacitances values.

$$C_{total} = C_{output} + 2 \cdot C_{MOSFET} \quad (16)$$

	Measured	Estimated	Notes
C_D	-	< 2.0pF	@ 50 volts
2 x $C_{level\text{-}shift}$	-	0.62pF	
$C_{surroundings}$	-	> 1.4pF	@ infinitive space
$C_{output,estimeret}$	-	4.0pF	
2 x C_{MOSFET}	-	< 18.0pF	@ 25 volts
C_{total}	21.2pF	22.0pF	

Table 3: Summary of measured and estimated capacitance.

The difference between measured and estimated values is 3.8% and is due to the uncertain capacity of the MOSFETs and the boot-strap diode at 1.5kV and the fact that the capacitance to the surroundings assumes infinitive space. The approximated output capacitance of the gate driver is given in (17) based on measurement and MOSFETs output capacitance. Equation (18) is based on the estimated values.

$$C_{output,measured} \approx 21.2\,pF - 2 \cdot 9\,pF = 3.2\,pF \quad (17)$$

$$C_{output,estimated} \approx 2pF + 0.62pF + 1.4\,pF = 4.0\,pF \quad (18)$$

The distribution of the estimated output capacitance is illustrated in figure 24. It shows that the differential capacitor pair occupies 16% of the total output capacitance and that the boot-strap diode is the most critical part regarding the total output capacitance. However the physical volume of the high side circuitry is not irrelevant either.

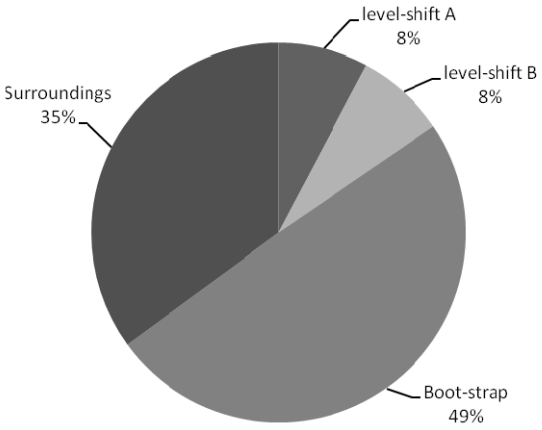

Figure 24: Distribution of the estimated half-bridge gate driver output capacitance: $C_{output,estimeret}$ = 4.0pF

Conclusion

A capacitive level-shifter is presented. No magnetic components are used. The level-shifter is tested as a part of a half-bridge gate driver. A prototype is developed and operation is verified at 2.44kV with a 50kHz switching frequency. The operation voltage was limited by the power supply and not by the prototype itself. The upper switching frequency is limited to 700kHz by the minimum dead time of the IR21091 chip and not limited by the level-shifter. The current consumption of the level-shifter alone is 500µA. The total average current consumption of the gate driver including gate-source capacitance of MOSFETs is 3.6mA operating at 2.44kV@50kHz. The output capacitance of the gate driver alone is around 4pF and mainly depended on the boot-strap diode and the physical volume of the high side circuit.

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