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A 1.2-V 165-μW 0.29-mm^2 Multibit Sigma-Delta ADC for Hearing Aids Using Nonlinear DACs and With Over 91 dB Dynamic-Range

José R. Custódio, João Goes, *Senior Member, IEEE*, Nuno Paulino, *Member, IEEE*, João P. Oliveira, *Member, IEEE*, and Erik Bruun, *Senior Member, IEEE*

***Abstract*—This paper describes the design and experimental evaluation of a multibit Sigma-Delta ($\Sigma\Delta$) modulator ($\Sigma\Delta$M) with enhanced dynamic range (DR) through the use of nonlinear digital-to-analog converters (DACs) in the feedback paths. This nonlinearity imposes a trade-off between DR and distortion, which is well suited to the intended hearing aid application. The modulator proposed here uses a fully-differential self-biased amplifier and a 4-bit quantizer based on fully dynamic comparators employing MOS parametric pre-amplification to improve both energy and area efficiencies. A test chip was fabricated in a 130 nm digital CMOS technology, which includes the proposed modulator with nonlinear DACs and a modulator with conventional linear DACs, for comparison purposes. The measured results show that the $\Sigma\Delta$M using nonlinear DACs achieves an enhancement of the DR around 8.4 dB (to 91.4 dB). Power dissipation and silicon area are about the same for the two cases. The performance achieved is comparable to that of the best reported multibit $\Sigma\Delta$ ADCs, with the advantage of occupying less silicon area (7.5 times lower area when compared with the most energy efficient $\Sigma\Delta$M).**

***Index Terms*—Hearing aids, multibit, nonlinear digital-to-analog converter (DAC), parametric amplification, self-biasing, sigma-delta modulator.**

I. Introduction

THE rapid advancements in medical science have urged the development of advanced portable electronic medical devices and have created a strong demand for a new generation of energy-efficient analog-to-digital converters (ADCs). Targeting micro-power medical devices, it is necessary to have ADCs operating with very low power dissipation [1], while delivering high performance suitable for applications such as hearing aids. Moreover, due to fabrication cost reasons, the required silicon area should be minimized.

Ideally, a hearing aid should be able to process signals corresponding to sound pressure levels (SPL) ranging from the threshold of hearing to the level of discomfort. For a normal hearing person this corresponds to a dynamic range (DR) of about 120 dB [2], [3]. For a person with a hearing loss the audible range is reduced, but still the signal processing in the hearing aid should be able to handle the full dynamic range. One of the challenges for the signal processing in a hearing aid is to compress the full sound pressure range into the range which is audible to the hearing impaired person. This range varies among individuals but a representative value would be 60 dB [2], [3].

The signal processing path in a hearing aid would normally comprise a transmitter front-end (TFE) interfacing with the microphone, a digital signal processing unit (DSP), and a receiver front-end (RFE) interfacing the speaker [4]. The TFE comprises a microphone preamplifier and an ADC, interfacing the DSP. This paper is concerned with the design of the ADC for a TFE with a high DR. A DR of 120 dB is very challenging for a preamplifier and an ADC, especially when considering that a hearing aid application also imposes strict limitations on the power consumption, and in order to achieve the large DR, it is necessary to take advantage of the fact that the output dynamic range of the hearing aid can be limited to about 60 dB. This implies that the signal-to-noise-plus-distortion-ratio (SNDR) at the output of the TFE does not need to be more than 60 dB. Also, a variable gain amplifier can be employed as the microphone preamplifier [4], alleviating the requirements for the input DR of the ADC. Therefore, in this work a data converter architecture has been considered, aiming at a DR of at least 90 dB with a peak SNDR of at least 60 dB. The signal bandwidth (BW) is designed to be 20 kHz and this is a specification which could be relaxed as a bandwidth of about 10 kHz would suffice, even for high-end hearing aids [3]. The fact that the signal-to-noise-ratio (SNR) does not need to be as large as the DR can be utilized by designing the ADC to have a signal dependent quantization error, i.e., a large quantization error for large inputs and a small quantization error for small inputs. This also implies that the power dissipation can be reduced since less power is needed for large inputs where a higher noise can be tolerated. Also, the limited

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SNDR of the output range implies that the ADC does not need to have a high linearity (10 bits would suffice) so a trade-off between linearity and DR is possible.

For the overall architecture of the ADC a sigma-delta modulator ($\Sigma\Delta$M) followed by a decimation filer has been chosen. $\Sigma\Delta$M's are frequently used in hearing aid applications, and also adaptive architectures permitting a trade-off between SNR and power consumption have been presented [5]. In [5], the adaptation is achieved by a combination of different clock frequencies and configurations. In the present work, the adaptation of the $\Sigma\Delta$M to the input signal amplitude is achieved by a non-linearity introduced in the feedback path and the sampling frequency is fixed. In order to limit the power dissipation the sampling frequency should be as low as possible, i.e., the over-sampling ratio (OSR) should be low. This is usually achieved in a $\Sigma\Delta$M either by increasing the order or by using multibit quantization. This last option normally requires dynamic element matching (DEM) to enhance the linearity of the digital-to-analog converter (DACs) in the feedback-loop [6], [7]. Since with advanced CMOS technologies it is possible to obtain capacitor matching errors at the 10 bit level, the use of DEM can be avoided for the intended application. Therefore, it is preferable to reduce the sampling frequency by increasing the number of bits of the $\Sigma\Delta$M instead of increasing its order. In particular, a second order $\Sigma\Delta$M with 5 bits and an OSR as low as 32 can achieve the desired DR. However, it is difficult to design the comparators in the 5-bit quantizer with more than 4 bits of accuracy due to power and stringent offset constraints.

In order to increase the DR while using 4-bit quantization, it is only necessary to improve the SNR for input signals with low amplitudes. As theoretically proposed in [8], the DACs can have a nonlinear transfer characteristic with a smaller conversion step (least-significant-bit, LSB) for low amplitude signals and a larger LSB for high amplitude signals. This increases the distortion for high amplitude signals, which is acceptable for the intended application. Hence, a multibit second-order modulator using nonlinear DACs can extend the DR either without the need of increasing the resolution of the quantizer or increasing the OSR, resulting in a $\Sigma\Delta$M with lower sampling frequency and lower complexity.

Alternative techniques to extend the DR have been proposed in [9], [10], based on non-uniform [9] or semi-uniform [10] quantization. Using this technique, the nonlinear steps are obtained in the quantizer, implying that the comparators in the quantizer should have a very low offset in order to precisely define the smallest steps. This leads to higher power dissipation. With the nonlinear characteristic embedded in the DAC, the precision of the nonlinear steps depends only on the capacitor matching in the DAC, and this does not increase the power. Therefore, our approach has some practical advantages, namely reduced spread and better matching of the capacitances (since they can be laid out together, using unit capacitors, in the same capacitor-array) and simpler design of the comparators in the multibit quantizer because of the use of uniform quantization.

Reported single-bit $\Sigma\Delta$Ms [11]–[14] and multibit $\Sigma\Delta$Ms [15]–[23], have shown slow improvements in energy efficiency over the years (only recently a significant improvement was achieved, by replacing the multibit quantizer by a single fast comparator with variable threshold levels [22]). One reason is the power required by the amplifiers in the integrators and by the comparators used in the multibit quantizer. Hence, to achieve high energy efficiency, we propose to use a fully-differential inverter-based self-biased amplifier together with a 4-bit quantizer based on low-offset, fully dynamic comparators, employing embedded discrete-time MOS parametric amplification (MPA).

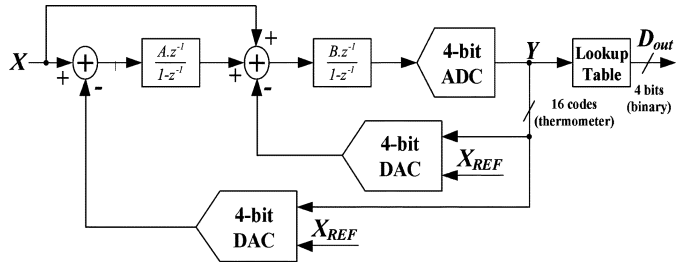

Fig. 1. Architecture of the 2nd-order $\Sigma\Delta$M with feed-forward, a 4-bit quantizer and 4-bit nonlinear DACs ($\Sigma\Delta\mathrm{M}-1$) or 4-bit linear DACs ($\Sigma\Delta\mathrm{M}-2$).

In Section II, we investigate the optimum nonlinear DAC characteristic. Section III deals with the architecture of the integrated 2nd -order 4-bit $\Sigma\Delta$M employing either linear or nonlinear DACs. Section IV discusses the implementation tradeoffs, especially power dissipation and thermal noise. In order to assess the advantage of using nonlinear DACs, a $\Sigma\Delta$M circuit using linear DACs has been implemented in the same IC for comparison purposes. Section V presents the experimental results and compares these with those of the best multibit $\Sigma\Delta$Ms reported in the literature. Finally, in Section VI, the main conclusions are drawn.

II. Nonlinear DACs

The selected architecture is based on a 4-bit second-order $\Sigma\Delta$M, as shown in Fig. 1. For comparison purposes two versions of this architecture have been implemented: $\Sigma\Delta\mathrm{M}-1$ using nonlinear 4-bit DACs and $\Sigma\Delta\mathrm{M}-2$ using linear 4-bit DACs. $\Sigma\Delta\mathrm{M}-1$ comprises two delayed switched-capacitor (SC) integrators, a 4-bit (uniform) flash quantizer ADC followed by a digital look-up table and two nonlinear 4-bit DACs, also implemented by SC circuits. A $\Sigma\Delta$M has a negative feedback path that subtracts the quantized output of the modulator from the input signal. This subtraction is followed by a block with a large gain in the signal band. Assuming that the modulator is not saturated, the difference between the input signal and the quantized output is almost zero [7]. This means that the output of the DAC tracks the input signal, while its input is basically a distorted version due to the nonlinear transfer characteristic.

Therefore, the ADC output is easily corrected by a digital look-up table with 16 values stored in digital memory. This look-up table is not required for the linear modulator ($\Sigma\Delta\mathrm{M}-2$) since it uses two linear 4-bit DACs.

The nonlinear DAC transfer characteristic determines the modulator's small LSB interval when the input signal amplitude is small in order to limit the quantization noise power. Therefore, the multibit nonlinear DAC must have small steps for input codes close to the middle of the range and larger steps for input codes in the extremes of the range, as shown in Fig. 2.

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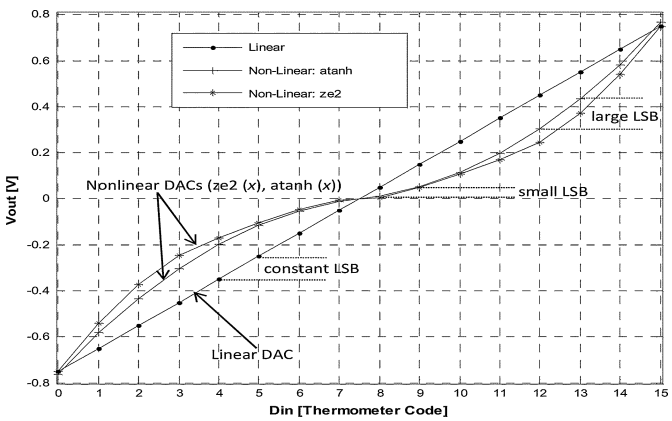

Fig. 2. Conversion steps and DAC conversion characteristics for three different cases (with a linear and two nonlinear 4-bit DAC transfer functions).

The nonlinear transfer function results in a reduction of the quantization noise power for small amplitude input signals. As a consequence, the DR is extended. Since the SNR is defined as the ratio between the signal power and the noise power, and there is both quantization and thermal noise, there is a limit to the possible extension of the DR, which is set by the thermal noise power.

The nonlinear function in the DAC must provide a smooth transition between the smaller conversion steps in the center to the large conversion steps at the extremes of the characteristic. After running comprehensive high level (MATLAB) simulations of the modulator with different mathematical functions, e.g., $\mathrm{atan}(x), \mathrm{atanh}(x), \mathrm{sigmoid}(x) = 1/(1+\exp(-x)), \mu\text{–law}(x)$, etc., the $\mathrm{atanh}(x)$ function was selected.

A systematic and simulation-based approach has been followed. For each DAC function and, for different sets of coefficients, we swept the input signal amplitude from 0 to -120 $\mathrm{dB_{FS}}$ at the input of the model of modulator and computed the peak SNDR and the peak DR.

In order to improve the performance of the modulator, each of the 16 voltage levels produced by the $\mathrm{atanh}(x)$ function has been also slightly adjusted, resulting in a new nonlinear function for the DAC. This 'modified' DAC function (shown in Fig. 2), which we named $ze2(x)$, has the advantage that it can be realized using small unit capacitances laid out in the same capacitor-array. In the remainder of this paper, whenever nonlinear transfer function is mentioned, it refers to this $ze2(x)$ function.

The 4-bit DACs are implemented using a SC topology comprising 15 different unit capacitors. The value of each capacitor is adjusted to obtain the conversion characteristic in Fig. 2. The mismatch errors among the unit capacitors affect the overall converter distortion, since they create a difference between the non-linearity of the DAC and the digital look-up table. When using a linear DAC, the effect of the capacitor mismatch in the distortion can be reduced using the referred DEM techniques. However, due to relaxed distortion requirements for the intended hearing aid application, a $\Sigma\Delta\mathrm{M}$ with a linear DAC without DEM is a valid option.

The 4-bit 2nd-order modulators, with and without nonlinear DACs, were modeled in MATLAB to quantify the impact of the random capacitor mismatch (assuming a 2% and 0.2% standard-deviation, $\sigma(\Delta C/C)$, for smaller and larger capacitors, respectively). The model included thermal noise in both integrators, and all the remaining blocks were considered as ideal. Due to practical feasibility reasons in the selected 130 nm technology, a minimum capacitance value of 49 fF was considered. The simulated results show that, for different input signal amplitudes, the SNDR of the output signal does not degrade more than 1 dB when compared with the ideal case without considering mismatch errors. When the input amplitude is small, only the LSB is changing in the quantizer meaning that only the corresponding LSB capacitor in the DAC is switching. Hence, the $\Sigma\Delta\mathrm{M}$ is operating as a single-bit modulator and, in this case, the circuit is not sensitive to mismatches. When the input amplitude is large, all the bits in the quantizer change and the capacitors in the DAC are switching. However, since the capacitance values associated with the most-significant bits (MSBs) are large, the associated mismatch errors are small and, consequently, the distortion is smaller than the distortion caused by the non-linear feedback function.

TABLE I
CAPACITANCE RATIOS USED IN THE 4-BIT NONLINEAR DACS

Capacitor in the DAC	Capacitance ratio
$C_0 = C_{14}$	$17\times C_U$
$C_1 = C_{13}$	$14\times C_U$
$C_2 = C_{12}$	$10\times C_U$
$C_3 = C_{11}$	$6\times C_U$
$C_4 = C_{10} = C_5 = C_9$	$5\times C_U$
$C_6 = C_8$	$4\times C_U$
C_7	C_U

Each bit of the thermometer code of the 4-bit quantizer is associated to DAC capacitors, which were sized to produce the characteristic in Fig. 2. These capacitors are numbered from C_0 to C_{14}; C_7 corresponds to the mid-scale step and C_0 and C_{14} correspond to the larger steps at the low and high extremes of the input range, respectively. Notice that C_7 is the smallest capacitor used in the DACs. For the 4-bit nonlinear DACs, and after choosing a unit capacitor value of $C_U = 49$ fF, the remaining capacitance ratios are summarized in Table I.

The linear 4-bit DACs use 15 equal sized unit capacitors of $C_0 = C_1 = \cdots = C_{14} = C_U = 400$ fF, giving approximately the same total capacitance value of $C_{\mathrm{DAC}} = 6$ pF (similar total capacitance value for the 4-bit nonlinear DACs).

III. 4-BIT $\Sigma\Delta$ MODULATORS

A. Architecture of Both Linear and Nonlinear $\Sigma\Delta\mathrm{M}$s

The architecture shown in Fig. 1 is described by the following equation:

$$Y(z) = E_Q + \frac{B\cdot z^{-1}}{1-z^{-1}} \cdot \left(X(z) - Y(z) + \frac{A\cdot z^{-1}}{1-z^{-1}} \cdot (X(z) - Y(z)) \right). \quad (1)$$

Coefficients A and B are set to 1/2 and 2, respectively, leading to the following transfer function:

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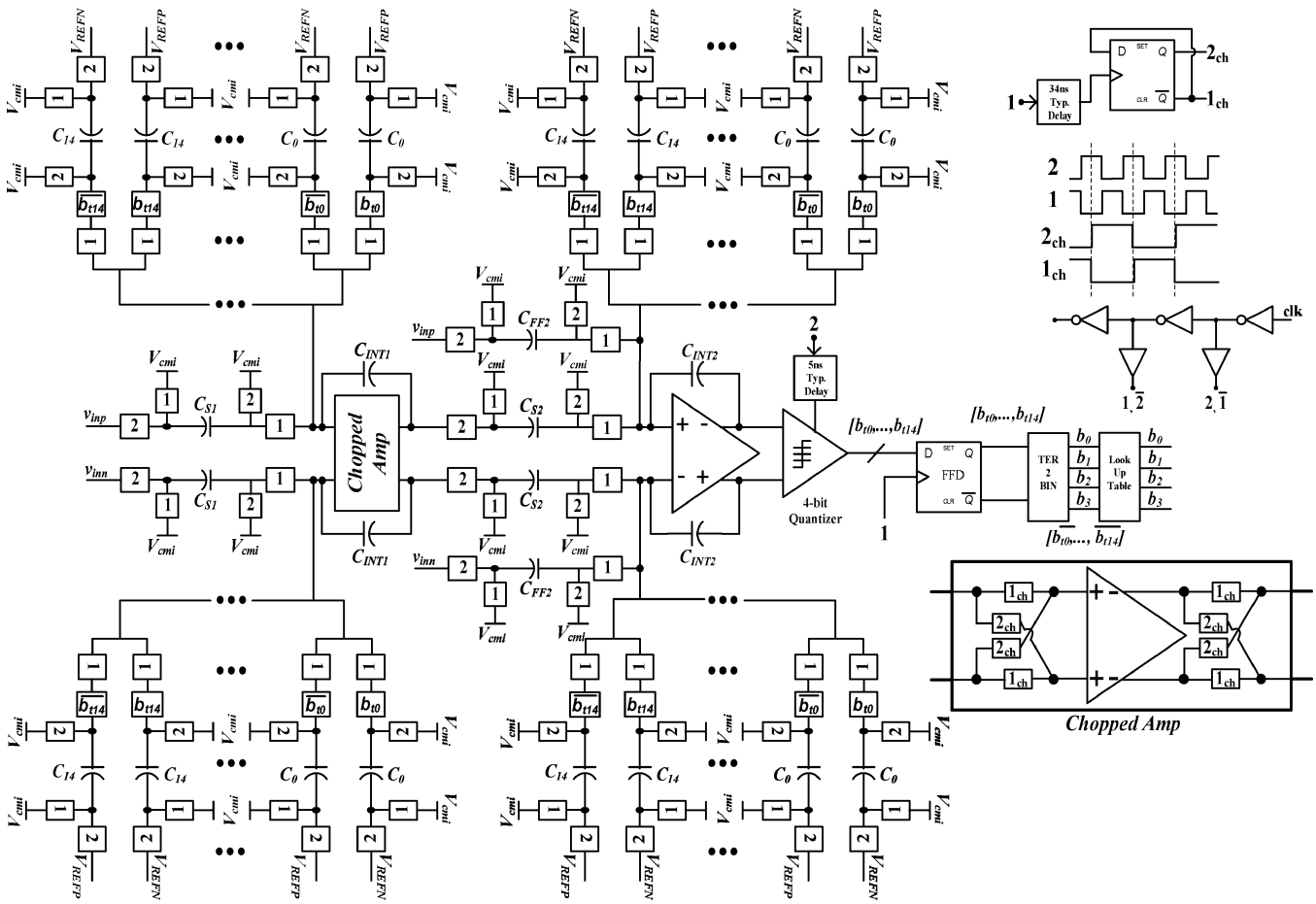

Fig. 3. Complete electrical schematic of the second-order 4-bit $\Sigma\Delta$Ms either with linear or nonlinear 4-bit DACs.

$$Y(z) = [2z^{-1}\cdot(1-z^{-1})+z^{-2}]\cdot X(z)+(1-z^{-1})^2\cdot E_Q. \quad (2)$$

It can be shown that the modulator implements the required noise transfer function, i.e., $\mathrm{NTF}(z) = (1-z^{-1})^2$, and that the signal transfer function, given by $\mathrm{STF}(z) = 2z^{-1}\cdot(1-z^{-1})+z^{-2}$ has a double-delay component and a highpass term due to the scaling and feed-forward. The highpass term can be simply compensated in the digital domain, by using a first order filter with a transfer function equal to $H(z) = z^{-1}/(1-2z^{-1})$.

Fig. 3 shows the complete electrical schematic of both 4-bit $\Sigma\Delta$Ms, which operate with a nominal power supply of 1.2 V. The differential reference voltage (V_{REFD}) is defined to be nominally equal to 0.7 V ($V_{\mathrm{REFP}} = 0.85$ V and $V_{\mathrm{REFN}} = 0.15$ V). The OSR is 32 and the nominal BW is 20 kHz ($F_{\mathrm{CLK}} = 1.28$ MHz). Input and output common-mode (CM) voltages, V_{CMI} and V_{CMO}, respectively, are set to approximately $V_{\mathrm{DD}}/2$. The full-scale (FS) input signal is set to $1\ \mathrm{V_{pp}}$, corresponding to 0 $\mathrm{dB_{FS}}$.

Fig. 4(a) shows a plot of the simulated SNDR (using the MATLAB model) as a function of the input signal amplitude. As it can be observed, using the nonlinear 4-bit DACs it is possible to increase the DR by, approximately, 9 dB when compared to the same modulator using linear 4-bit DACs. As expected, the achievable peak SNDR is reduced to about 70 dB. This graph shows a discontinuity in the SNDR curve around input amplitudes of -44 dB for the case of the nonlinear DACs. This discontinuity occurs because the input amplitude becomes large enough to enable more than the LSB in the quantizer. For smaller input amplitudes, the modulator is essentially a single-bit modulator and it is inherently linear, as shown in Fig. 4(b). However, for larger input amplitudes, the non-linear characteristic of the DACs increases the feedback gain. As a result, the quantization noise of the modulator increases, resulting in the observed degradation of the SNDR.

B. The Amplifier

Both $\Sigma\Delta$Ms use scaling and a feed-forward path since this is an effective way of relaxing the requirements in terms of the output dynamic range and DC gain variability of the op-amp [22], [23]. The selected $\Sigma\Delta$ architecture does not require high gain amplifiers. Therefore, single-stage cascode or two-stage amplifiers are not required. A new fully-differential inverter-based self-biased OTA [Fig. 5(a)] is proposed in this paper and used in the integrators to reduce power. The obvious advantage of using inverters is that both input devices $(\mathrm{M}_2, \mathrm{M}_3)$ contribute with their transconductances to the gain-bandwidth product (GBW) at the expense of a single current branch. Another advantage is that no biasing circuitry is needed.

A single-ended version of a self-biased amplifier was proposed in [24]. It is known that self-biasing makes some of the

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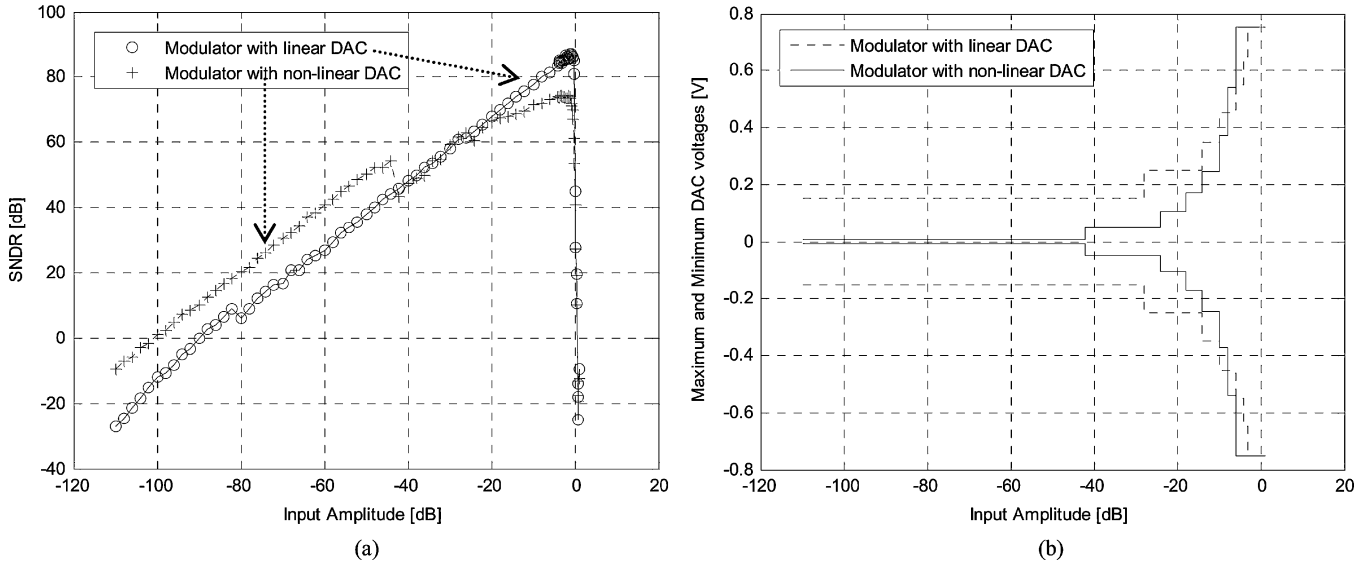

Fig. 4. (a) SNDR versus input amplitude graphs of the two $\Sigma\Delta$Ms obtained using MATLAB. (b) Maximum and minimum output DAC voltages versus input amplitude.

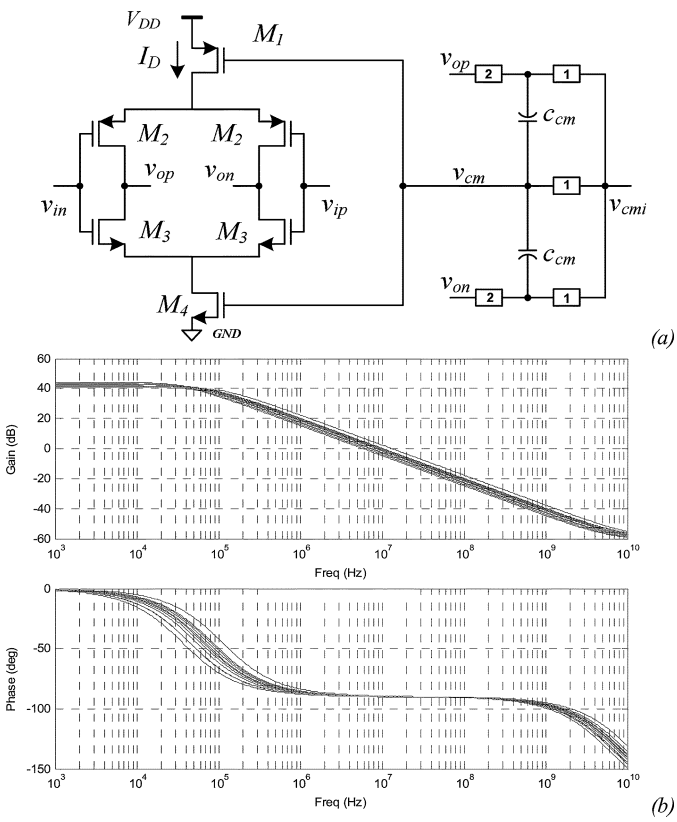

Fig. 5. (a) Schematic of the fully-differential single-stage inverter-based self-biased amplifier with SC CMFB circuit. (b) Bode diagrams obtained by simulation of the proposed amplifier over 10 PVT corners.

performance parameters of the circuits insensitive to process, supply and temperature (PVT) variations. Similar circuits have been proposed by other authors [25], [26], but either they rely on more complex and pseudo-differential schemes [25] or they require active common-mode feedback (CMFB) [26]. The proposed OTA comprises two CMOS inverters and two voltage controlled resistors (VCR) M_1 and M_4, biased in the boundary of the saturation and triode regions. A simple SC CMFB circuit comprising only two capacitors (C_{cm}) and five switches is used to adjust the output common-mode voltage to about $V_{\mathrm{DD}}/2$ and to provide closed-loop control (self-biasing) of the amplifier. VCRs, M_1 and M_4, have their gate voltages controlled by the output of the SC CMFB circuit, V_{CM}. They provide a negative feedback loop which reduces the sensitivity of the amplifier's DC gain to PVT variations. For example, if V_{DD} increases, the source-gate voltage in PMOS device M_1, V_{SGP1}, also increases producing an increase in the bias current I_D. Hence, the current in the two inverters and the output CM voltage increase. The CMFB circuit produces higher V_{CM} (assuming that V_{CMI} is constant and provided by a bandgap reference circuit) forcing V_{GSP1} to remain constant, thus compensating the V_{DD} variation. Process and temperature variations are similarly compensated by the negative-feedback loop. The DC gain, A_{V0}, is approximately the ratio between a transconductance and an output conductance, g_m/g_{ds} and is maintained constant because variations in $g_m(\pm 30\%)$ are accompanied by similar variations in g_{ds}: their ratio varies less than 7% with PVT variations.

The amplifier's transfer function is approximately equal to that of a standard inverter. Fig. 5(b) shows the AC simulation results of the proposed amplifier over 10 different PVT corners ($\{\mathrm{tt}, \mathrm{ss}, \mathrm{ff}\}$ for process, $\{-40, 27, 85\}$ for temperature, and $1.2\ \mathrm{V} \pm 5\%$ for supply voltage) plus typical conditions. It can be observed that the low-frequency gain is always higher that 41 dB and the variability over PVT is limited to ± 1.5 dB.

High level simulations show that a minimum DC gain of 36 dB is required for the first integrator to reach the targeted DR above 90 dB (due to the use of feed-forward). Therefore, a safety margin of about 3 dB was considered in the design. From electrical transient simulations of the complete modulator it was found that a minimum GBW product of about 4 MHz was required to avoid a degradation of the peak SNDR (below 72 dB and without considering any mismatch errors). Since PVT vari-

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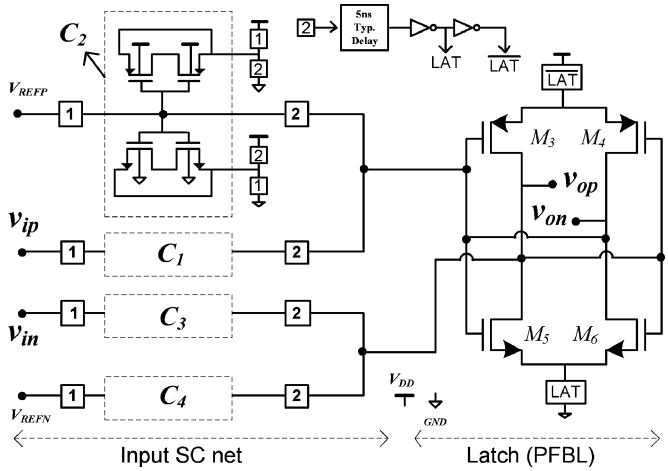

Fig. 6. Schematic of the comparator with MPA embedded in the input SC sampling network.

ations have to be considered, a typical GBW higher than 8 MHz was used. In this condition, this amplifier dissipates less than 42.5 μW.

C. The 4-Bit Flash Quantizer

The 4-bit quantizer comprises a bank of 15 comparators and D-type flip-flops (D-FFs) followed by an output encoder to provide both the 4-bit code and 15-bit thermometer-code (to drive the 4-bit DACs). The necessary 15 threshold levels, (in our case of $\pm 7\ V_{\mathrm{REFD}}/8, \pm 6V_{\mathrm{REFD}}/8, \pm 5V_{\mathrm{REFD}}/8, \pm V_{\mathrm{REFD}}/2, \pm 3V_{\mathrm{REFD}}/8, \pm 2V_{\mathrm{REFD}}/8, \pm V_{\mathrm{REFD}}/8$ and 0) are defined by an input SC network included in each comparator. Each comparator is shown in Fig. 6, which comprises an input SC network followed by a positive-feedback latch (PFBL).

To eliminate static power, pre-amplification was embedded into the input SC network by employing MOS parametric amplification (MPA) [29]. The circuit operates with two clock phases and each capacitor is implemented by means of a parametric MOSCAP made of two MOS transistors (either NMOS or PMOS) as shown also in Fig. 6. Hence, all eight MOS capacitors change from inversion during phase 1, into depletion during phase 2, thus providing amplification. Then, approximately 5 ns after phase 2 is enabled, the PFBL is latched (by enabling LAT phase).

The threshold level does not depend on the load capacitance and it is simply set by the ratio of C_1 and C_2 during phase 1. The detailed design of each individual comparator is given in [27]. If it is decided not to use MPA, the comparator may be designed without any pre-amplifier. However, to keep the random offset below the 5-bit level (4-bit quantizer), the input devices used in the PFBL should have larger areas $(W.L)$.

IV. Circuit Implementation Details

A. Switches

The majority of the switches in the modulators are ATGs (asymmetrical transmission gates) with bulk-switching (BS) in the larger PMOS devices (all switches in the signal paths), and STGs (symmetrical transmission gates) in the switches

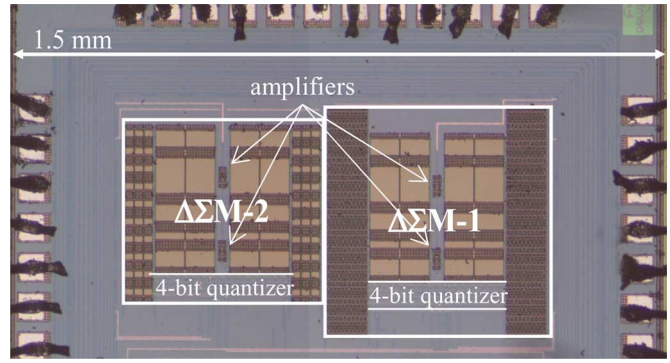

Fig. 7. Die photo of the test chip with both $\Delta\Sigma$Ms.

connected to the common-mode voltages and to the inputs of the amplifiers. Since ATG with BS are used for both the input switches and for the feed-forward input switches, it was found unnecessary to employ clock-bootstrapping techniques. For all switches in the DACs, either PMOS or NMOS devices are used, depending on whether the plate of the capacitor is being connected to V_{REFP} or to V_{REFN}, respectively. All remaining switches in the modulators are simply STGs.

B. Single-Phase Clocking Technique

All switches in all SC blocks are driven by complementary clock phases ϕ_1 and $\phi_{1\mathrm{n}}$ [13]. However, it is necessary to guarantee that the sampling phase of the first integrator (ϕ_1) should start slightly earlier than the sampling phase of the second integrator $(\phi_{1\mathrm{n}})$ The circuit used to generate these two complementary clock phases, depicted in Fig. 3, comprises 3 inverters plus 2 digital buffers (7 inverters in total). The two required chopping phases are created with a simple divide-by-two scheme.

C. Digital Circuitry

The digital part of the modulators consists of a bubble detector circuit, 17 D-FFs, an encoder to transform the output of the 4-bit quantizer after the bubble detector into a thermometer code (necessary to address the 4-bit DACs), 19 medium-sized buffers, and three delays (two of about 5 ns and one of 34 ns, in typical conditions). This arrangement provides the delayed phase necessary to guarantee the required minimum pre-amplification time (for the MPA) in the comparators.

D. Noise and Capacitance Values

The capacitances of the modulator have to be sized in order to reach the desired DR. The $\Sigma\Delta$M with nonlinear 4-bit DACs $(\Sigma\Delta\mathrm{M}-1)$ should have a dynamic performance above 15 bits (DR of more than 90 dB). Assuming that the $\Sigma\Delta$M overloads for input signal amplitudes larger than -2 dB$_{\mathrm{FS}}$, it is necessary to have a total maximum input referred noise power below $\overline{v_{\mathrm{th}}^2} = (9.908\ \mu\mathrm{V})^2$ to obtain the desired DR. This noise power includes quantization and thermal noise. We chose to assign 75% of the total noise budget to thermal noise, which corresponds to a noise power of $\overline{v_{\mathrm{Nthermal}}^2} = (8.581\ \mu\mathrm{V})^2$. Using the method described in [28], the first integrator sampling capacitance, C_{S1}, is obtained in a straightforward way. The remaining capacitance values ($C_{S2}, C_{\mathrm{INT1,2}}$ and C_{FF}) are easily obtained through the values of the coefficients. The resulting values are:

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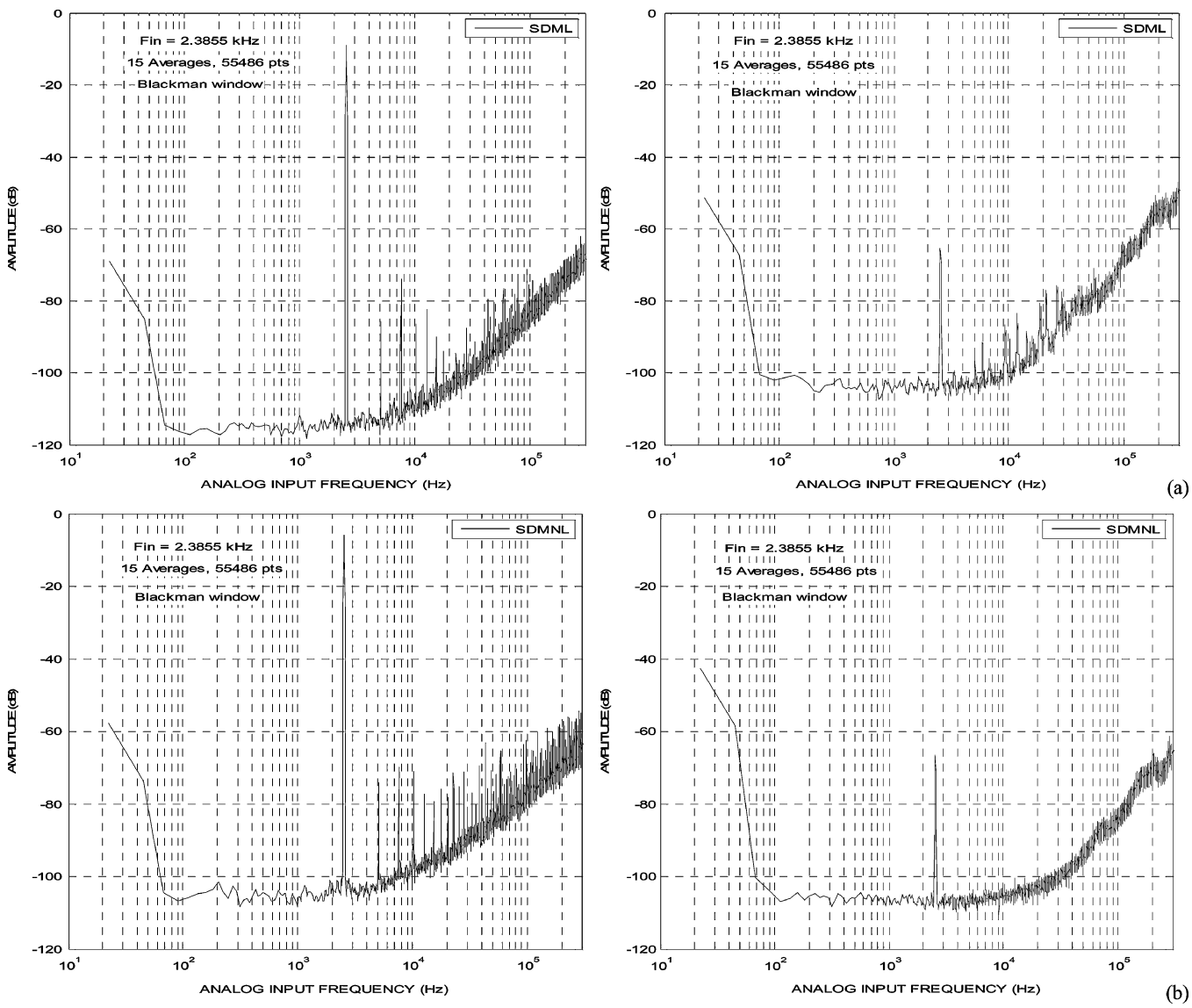

Fig. 8. Measured FFT comparison of the $\Delta\Sigma$M employing: (a) linear DACs for -7 dB$_{\rm FS}$ and for -64 dB$_{\rm FS}$ input signal; (b) nonlinear DACs for -7 dB$_{\rm FS}$ and for -64 dB$_{\rm FS}$ input signal.

$C_{S1} = C_{S2} = C_{\rm DAC1} = C_{\rm DAC2} = 6$ pF, $C_{\rm INT1} = 12$ pF, $C_{\rm INT2} = 3$ pF and $C_{\rm FF} = 6$ pF.

As in [22], chopper stabilization is used for the first stage op-amp to suppress in-band flicker noise. The chopped amplifier, shown in Fig. 3, consists of the proposed amplifier plus 8 switches. The input chopping switches are STGs, while the output chopping switches are ATGs, to accommodate the varying voltage added to 0.55 V common-mode at the output.

E. Power Dissipation

The total power dissipation, $P_{\rm TOT}$, for both modulators is $P_{\rm TOT} = P_{\rm INT1,2} + P_{\rm 4b_Quantizer} + P_{\rm Digital}$, where $P_{\rm INT1,2}, P_{\rm 4b_Quantizer}$ and $P_{\rm Digital}$ are the static and dynamic power dissipated by the two integrators, the dynamic power dissipated by the 4-bit quantizer and the power dissipated by the remaining digital circuitry, respectively. The last term is due mainly to the clock generator and digital buffers at the 15 digital outputs of the 4-bit quantizer (thermometer-code); these are needed to drive the switches in the 4-bit DACs. This power dissipation can be reduced significantly by minimizing, in the layout, all parasitics in the metal lines (e.g., using metals above metal-4) that connect the quantizer outputs to the DAC inputs.

The static and dynamic power dissipated by the two integrators comprise, respectively, the static power dissipation of the two amplifiers, the clock-frequency, the sum of the 15 capacitances in the two DACs (either linear or nonlinear) and the feed-forward capacitances. For the selected amplifier topology, a nominal bias current as small as 30 μA, in typical conditions, (corresponding to a static power dissipation of 36 μW) can be used in the first integrator (a slightly higher value of 42.5 μW was used for safety). The power dissipated in the 4-bit quantizer is dynamic contribution, since the comparators do not have static pre-amplifiers but, rather, MPA.

There is an obvious trade-off between noise and power dissipation. Lower noise (higher SNR and higher DR) requires higher capacitances, but this leads to higher power.

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V. Integrated Prototypes and Measurement Results

A prototype IC with the two $\Delta\Sigma$Ms has been fabricated in a 130 nm standard CMOS process using MiM capacitors. Only standard (1.2 V) NMOS and PMOS devices have been used.

A. Integrated Prototypes and Layout Related Issues

Four major concerns were taken into account in the layout of the modulators: 1) the threshold voltage of each comparator in the 4-bit quantizer was carefully adjusted, through extracted layout simulations, in order to minimize any systematic offset voltage. This was critical to guarantee that the parasitic capacitances associated with the MOS parametric capacitors would not affect the threshold level beyond a couple of mV (systematic offsets); 2) the power dissipation of the digital circuitry has been minimized. For example, buffers were optimum-sized also through extracted layout simulations, in order to properly drive the large parasitic capacitances of the 2×15 metal lines connecting the 4-bit quantizer to the two 4-bit DACs; 3) the capacitor-arrays of the DACs were laid out in common-centroid way to provide immunity to cross-chip gradients and to improve matching; 4) finally, to reduce switching noise coupling, three separated digital, mixed-mode, and analog supplies were used. The die photograph of the chip with the two modulators is shown in Fig. 7. The active area of the $\Sigma\Delta$Ms is 0.24 mm^2 and 0.29 mm^2, respectively, for the linear ($\Sigma\Delta\mathrm{M} - 2$) and for the nonlinear modulators ($\Sigma\Delta\mathrm{M} - 1$).

B. Measurement Results

The SNR and SNDR of the two $\Sigma\Delta$Ms were measured for different input signal amplitudes. The following equipment was used:—ATS-2 Audio Analyzer to generate the double balanced inputs;—PS2521G programmable power supply from Tektronix;—AWG510 waveform generator from Tektronix to generate the clock;—Agilent 16702B logic analyzer to acquire the 4-bit outputs to be processed in MATLAB.

Fig. 8 shows, for the two $\Sigma\Delta$Ms, the measured FFT spectrum for input signal amplitudes of -7 dB$_{\mathrm{FS}}$ and -64 dB$_{\mathrm{FS}}$. For large amplitudes, the in-band distortion is worse for the $\Sigma\Delta\mathrm{M}$ with nonlinear DACs, but for small amplitudes, the SNR is much better. The different quantization noise floor for the two $\Sigma\Delta$Ms with two input signals are perfectly visible.

Input signals ranging from 20 μVrms (-94 dB$_{\mathrm{FS}}$) to 675 m Vrms (-3.4 dB$_{\mathrm{FS}}$) were applied to two samples of the $\Sigma\Delta$Ms.

Both SNDR and SNR plots are for FFTs with 55486 points using 15 averages and the Blackman window. The SNDR measurements are with input frequency of 2.4 kHz and, for the SNR measurements, with the input frequency of 10.4 kHz. The measured results in Fig. 9 show that $\Delta\Sigma\mathrm{M}-1$ has enhanced the DR by 8.4 dB (achieving a peak DR of 91.4 dB) when compared to $\Delta\Sigma\mathrm{M}-2$. The power dissipation is about the same for both circuits. The peak SNDRs are 72.5 dB and 61.5 dB and the peak SNRs are 74.7 dB and 70.2 dB, respectively for the $\Sigma\Delta\mathrm{M} - 1$ and $\Delta\Sigma\mathrm{M} - 2$.

Neither data-weight-averaging (DWA) nor DEM were used in the modulators, since a peak SNDR of 60 dB is sufficient for hearing aids. The key measurement results and a comparison between the two modulators are summarized in Table II.

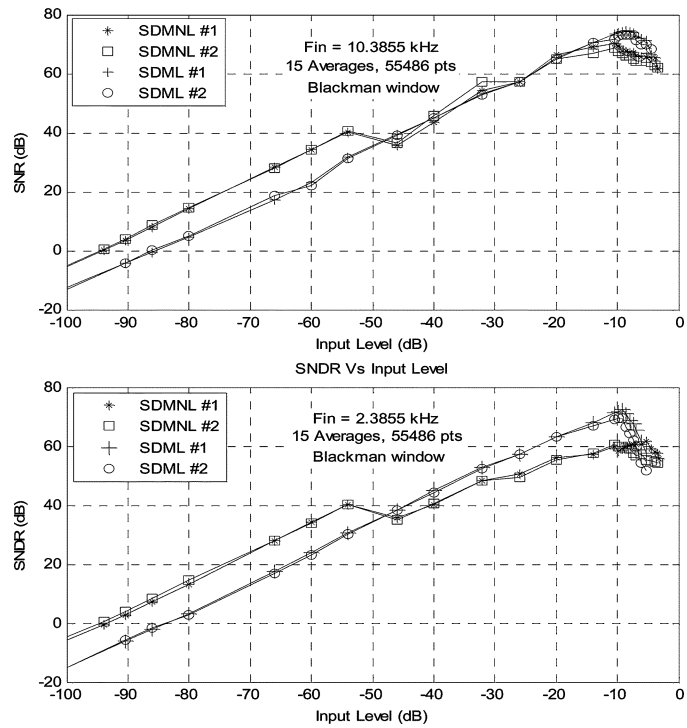

Fig. 9. Measured SNR and SNDR versus input level for two different IC samples of the two $\Delta\Sigma$Ms (with and without nonlinear DACs).

TABLE II
Key Features and Measured Results

	ΔΣM−1 (w/ nonlinear DACs)	**ΔΣM−2** (w/ linear DACs)
Nominal power supply voltage	1.2 V	
Sampling frequency	1.28 MHz	
OSR	32	
Analog and mixed-mode power dissipation	151 µW	
Digital power dissipation	14 µW	
Reference voltage	0.7 V	
Peak SNR	70.2 dB	74.7 dB
Peak SNDR	61.5 dB	72.5 dB
DR	91.4 dB	83.0 dB
FOM	172.2	163.8
Modulator area	0.29 µm^2	0.24 µm^2
Technology	0.13 µm 1P8M Logic CMOS with MiMs	

Using true audio signals representing voice (with a few seconds of duration), and apart from some minor differences in signal and noise levels, we could not notice any audible pops, clicks, idle tones or distortion. Moreover, a sine-wave signal with a frequency value sweeping from 100 Hz to 16 kHz was also digitized by the circuit. Neither audible distortion nor idle tones could be listened in the post-processed sound.

C. Performance Comparison With Other Multibit $\Sigma\Delta$Ms

To compare the measured performance of our $\Sigma\Delta\mathrm{M}$ circuit with other multibit $\Sigma\Delta$Ms, the usual figure-of-merit (FOM) based on the measured DR, BW and dissipated power, P, and defined by $\mathrm{FOM} = \mathrm{DR}_{\mathrm{dB}} + 10\log(\mathrm{BW}/P)$ [6] is used. Table III shows the comparison for multibit $\Sigma\Delta$Ms. The proposed $\Sigma\Delta\mathrm{M}$ employing nonlinear DACs has a FOM similar to that of the $\Sigma\Delta\mathrm{M}$ in [22]. When compared with the best $\Delta\Sigma\mathrm{M}$

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TABLE III
PERFORMANCE COMPARISON WITH THE MEASURED RESULTS OF THE PROPOSED $\Sigma\Delta$M WITH OTHER REPORTED $\Sigma\Delta$Ms (MULTIBIT ONLY)

Paper Reference	VDD (V)	Process (µm)	DR (dB)	BW (kHz)	Power (µW)	Area (mm^2)	FOM
This Work (nonlinear DACs)	1.2	0.13	91	20	165	0.29	172
This Work (linear DACs)	1.2	0.13	83	20	165	0.24	164
[15]	5	0.35	114	20	68000	5.62	169
[16]	1.3	0.09	78	200	2100	0.4	158
[17]	1.2	0.25	96	1250	87000	8.6	168
[18]	2.6	0.35	98	0.05	60	0.7	157
[19]	1.2	0.065	80	2000	4520	0.084	166
[20]	1.2	0.065	95	20	2200	0.149	165
[22]	0.7	0.18	100	25	870	2.16	175
[23]	1.8	0.18	86	2200	13800	2.32	168

reported in [22] ($\mathrm{FOM} = 174.6$) with similar BW and with a DR higher than 90 dB, our $\Delta\Sigma\mathrm{M} - 1$ achieves a FOM of 172.2, i.e., only 2.4 (dB) worse, but the core of the modulator in [22] occupies an area 7.5 times larger (in 180 nm CMOS). Although the first integrator in [22] uses about 50% of the area of the modulator (since a DR of 100 dB was targeted), the 4-bit quantizer and the digital logic (also associated with the DWA) occupy roughly 40 % of the overall area (about 20 % each). This means that the area of the 4-bit quantizer in [22] represents, by itself, 1.5 times the area of our $\Delta\Sigma\mathrm{M} - 1$. Moreover, the single-bit $\Sigma\Delta$Ms with the best performance reported in [11] and [12] have a FOM of 170 and 172, respectively. This is slightly lower than for the best multibit converters.

VI. CONCLUSION

This paper describes the design of a multibit $\Sigma\Delta\mathrm{M}$ for hearing aids in a 130 nm CMOS technology, with enhanced DR obtained by using nonlinear DACs. It was shown that an extended DR is obtained with a slightly larger distortion. It was experimentally demonstrated that the $\Sigma\Delta\mathrm{M}$ with nonlinear DACs achieves a 8.4 dB enhancement of the DR when compared with its circuit replica employing linear DACs, while dissipating the same power and occupying about the same area. Furthermore, a fully-differential inverter-based self-biased amplifier together with a 4-bit quantizer based on dynamic comparators employing embedded MPA were used to obtain similar energy efficiency when compared with the best $\Sigma\Delta\mathrm{M}$ ADCs reported to date. The achieved FOM of 172 is slightly inferior to the 175 value in [22], but the proposed $\Sigma\Delta\mathrm{M}$ has the advantage of occupying 7.5 times smaller area.

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