

High Efficiency PFC Frontend for Class-D Amplifiers

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Qingnan Li

High Efficiency PFC Frontend for Class-D Amplifiers

PhD thesis, March 2012

Ph.D. Thesis

High Efficiency PFC Frontend for Class-D Amplifiers

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Preface

This thesis is submitted in partial fulfilment of the requirements for obtaining the PhD degree at the Technical University of Denmark, DTU Elektro, Electronics Group. The Ph.D. project was carried out during the period from the period from March 2009 through March 2012 and was conducted in cooperation with Technical University of Denmark and Bang & Olufsen ICEpower.

The Ph.D. project was supervised by Professor Michael A. E. Andersen and Associate Professor Ole C. Thomsen at Technical University of Denmark and Lars B. R. Hansen and Mads P. Frium at Bang & Olufsen ICEpower.

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- My supervisors, Michael A. E. Andersen, Ole C. Thomsen, Lars B. R. Hansen and Mads P. Frium for giving me this opportunity and their support, encouragement and endless confidence in me.
- All of my colleagues for their help, support, and precious discussions.
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Abstract

This thesis investigates the design of high efficiency Power Factor Correction (PFC) converter for Class-D amplifier at universal line and 3.5kW power range.

The work starts with an overview on different high efficiency Bridgeless PFC topologies and investigates their applicability with respect to the given specifications in Chapter 1. Based on the conclusions of Chapter 2, the single-phase Two-Boost-Circuit Bridgeless PFC converter topology is considered the most promising to start with regarding the achievable converter efficiency and the EMI performances.

The subsequent Chapters discuss the method to optimize and improve the performance of Two-Boost-Circuit BPFC converter in detail.

Chapter 3 explains the working principle of the Two-Boost-Circuit BPFC converter firstly. And then, an optimized design procedure is implemented to achieve an useful compromise between efficiency and power density. Where, impacts of the Boost inductor design is analyzed carefully.

Chapter 4 firstly presents a novel interleaved BPFC (IBPFC) topology, which can be consider as the extension version of traditional Two-Boost-Circuit BPFC in Chapter 3 for EMI improvement. And then, the IBPFC's EMI model is used to study the insight of the relationship of EMI reduction and the number of interleaved stages. Moreover, an multi-objective optimization design procedure is proposed for designing a high efficiency, high power density and low EMI IBPFC system. Finally, frequency dithering technique is researched and implemented for the proposed IBPFC to gain further EMI attenuation.

Chapter 5 analyzes the measurement accuracy of the efficiency results presented in this thesis in Chapter 4, which makes the efficiency measurement in this report more convictive.

Chapter 6 summarizes the obtained results and concludes this work. Furthermore, an outlook regarding future researches in the IBPFC converter is presented.

Resumé

Denne afhandling undersøger design af høj effektivitet Power Factor Correction (PFC) konverter for klasse-D forstærker på universel linje og 3.5kW effektområde.

Arbejdet starter med en oversigt over forskellige høj effektivitet uden bro PFC topologier og undersøger deres anvendelighed i forhold til de givne specifikationer i kapitel 1. Baseret på konklusionerne i kapitel 2, enkelt-fase to-Boost-Circuit uden bro PFC konverter topologi betragtes som den mest lovende at starte med om opnåelige konverterens virkningsgrad og EMI forestillinger.

De efterfølgende kapitler diskuterer metode til at optimere og forbedre effektiviteten af to-Boost-Circuit BPFC konverter i detaljer.

Kapitel 3 forklarer arbejder princippet om to-Boost-Circuit BPFC konverter først. Også er en optimeret design procedure gennemføres for at nå et nyttigt kompromis mellem effektivitet og effekttæthed. Hvor er konsekvenserne af den Boost spole design analyseret grundigt.

Kapitel 4 For det første præsenterer en ny interleaved BPFC (IBPFC) topologi, som kan betragte som en udvidelse version af traditionelt to-Boost-Circuit BPFC i kapitel 3 for EMI forbedring. Og derefter bliver IBPFCs EMI model anvendt til at undersøge den indsigt af forholdet af EMI reduktion og antallet af sammenflettede trin. Endvidere er en multi-mål optimering design foreslåede metode til at designe en høj effektivitet, høj effekttæthed og lav EMI IBPFC system. Endelig er frekvensen dithering teknik forsket og gennemført den foreslåede IBPFC at få yderligere EMI dæmpning.

Kapitel 5 analyserer målenøjagtighed af de effektiviseringsgevinster resultater, der præsenteres i denne afhandling i kapitel 4, hvilket gør den høje effektivitet måleresultater i denne rapport mere convictive.

Kapitel 6 sammenfatter de opnåede resultater og konkluderer dette arbejde. Desuden er en prognose om den fremtidige forskning i IBPFC konverter præsenteret.

Contents

Preface	i
Acknowledge	iii
Abstract	v
Resumé	vii
1 Introduction	1
1.1 Scope	1
1.2 Background and Motivation	2
1.3 Specifications	3
1.4 Project Objectives and Contributions	4
1.5 Project Plan and Content	5
1.6 Thesis Structure	5

2	State of the Art	9
2.1	Derivation of Bridgeless PFC Converters	10
2.2	BPFC Topologies Overview	10
2.2.1	Basic BPFC System	10
2.2.2	BPFC with Two Boost Circuits	11
2.2.3	Basic BPFC with Bidirectional Switch	12
2.2.4	Pseudo Totem-pole BPFC	14
2.2.5	Totem-pole BPFC	15
2.3	Summary of State-of-the-art Analysis	16
3	Design of the High Efficient BPFC - Boost Inductor Optimization	19
3.1	Topology Basic Operation	19
3.2	High Efficiency Boost Inductor Design	21
3.2.1	Conventional Boost Inductor Design Procedure	21
3.2.2	Optimized Design Procedure	23
3.2.3	Mathematical Modelling	25
3.2.4	Inductance vs. Semiconductor Losses	28
3.2.4.1	Semiconductor Losses	28
3.2.4.2	Inductance Optimization vs. Semiconductor Losses	30
3.2.5	Efficiency and Volume Optimization	31
3.2.5.1	Cores Selection	31
3.2.5.2	Winding Losses	32

3.2.5.3	Core Losses	33
3.3	Experiment Results from a 3.2kW Bridgeless PFC	36
3.4	Conclusions on the Design of High Efficient Boost Inductors	38
4	EMI Analysis and Suppression	39
4.1	EMI Modelling	39
4.2	EMI Suppression	40
4.2.1	EMI Reduction Using Interleaving Technique	41
4.2.2	Multi-Interleaved Stages and EMI Cancellations	41
4.2.3	Novel High Efficient Interleaved BPFC Converter Design using Multi-Objective Design Optimization Procedure	46
4.2.3.1	Definition of MDOP	47
4.2.3.2	The MDOP Design Flow Chart for IBPFC System	47
4.2.4	Experimental Results	50
4.3	EMI Reduction Using Frequency Dithering	52
4.3.1	Operation Principles	53
4.3.2	Advantages and Limitations	56
4.3.2.1	Advantages of Frequency Dithering	57
4.3.2.2	Limitations of Frequency Dithering	58
4.3.3	Conclusions on Frequency Dithering and EMI Reductions	59
4.4	EMI Filter Design Considerations	60
4.5	Experimental Results	63
4.6	Conclusions of EMI Analysis and Suppression	64

5 Accuracy Analysis	69
5.1 Experiment Set Up	69
5.2 Accuracy Analysis	70
5.2.1 Accuracy of Measured P_{in} and P_o	71
5.2.2 Accuracy of Measured Efficiency	72
5.2.3 Estimation of Worst-case Accuracy of Efficiency	72
6 Conclusions and Future Works	75
6.1 Summary and Conclusions	75
6.2 Future Works	77
Bibliography	77
A Publications	87
A.1 PEDS2009 Published	87
A.2 ECCE Asia 2011 Published	94
A.3 ACEMP 2011 Published	103
A.4 APEMC 2012 Published	109
A.5 ECCE Asia 2012 Published	114
A.6 ECCE Asia 2012 Published	121
A.7 Transactions on Industrial Electronics Paper Submitted	127
B C++ Code Fragment	139
B.1 Common Header	139

B.2 Header for Magnetic Core	139
B.3 Function for Magnetic Core	142
B.4 Loop 1	149
B.5 Loop 2	150
B.6 Loop 3	152
B.7 Model of losses	154

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List of Figures

1.1	Block diagram of typical power supply configuration for supplying Class-D amplifiers system from the AC mains	2
1.2	Passive single-phase diodes rectifier and its characteristic waveforms	3
1.3	Ph.D. Project Overview	6
1.4	Ph.D. Thesis Structure	7
2.1	Basic BPFC and Conventional Boost PFC Topologies	10
2.2	Voltage Waveforms Between Neutral and Output Power Ground [27]	11
2.3	Two-Boost-Circuit BPFC	12
2.4	Basic BPFC with Bidirectional Switch	13
2.5	Pseudo Totem-pole BPFC	14
2.6	Totem-pole BPFC	15
3.1	Two-Boost-Circuit BPFC with good efficiency and low conducted EMI	20

3.2	Operation principles of the Two-Boost-Circuit BPFC	20
3.3	Optimization procedure of inductor design in CCM for Two-Boost-Circuit BPFC with balance of efficiency and power density	24
3.4	Boost inductor current waveform in a switching cycle in CCM	25
3.5	Boost inductor current waveform in a switching cycle in DCM	27
3.6	Semiconductor Losses Ratio vs. Boost Inductance and Output Power	30
3.7	Increase of layer copper losses proximity effect as a factor φ and MMF force ratio m [37]	33
3.8	Inductor Winding Losses vs. Thickness of Copper Foil and Inductance. The core is Kool Mu E core 5528E90 from <i>Magnetics</i> [®]	34
3.9	Core Losses vs. Boost Inductance for All Qualified Kool Mu E cores from <i>Magnetics</i> [®]	35
3.10	Total inductor losses vs. Boost inductance for different qualified Kool Mu E cores from <i>Magnetics</i> [®] when $h=0.13\text{mm}$	36
3.11	Efficiency comparison of Two-Boost-Circuit BPFC at $220V_{ac}$ input and 390V output using core 5528E090	37
3.12	Input voltage and current waveforms from Two-Boost-Circuit at $220V_{ac}$ input and 390V output using core 5528E090	37
4.1	DM EMI Modeling Process of the Two-Boost-Circuit BPFC	40
4.2	CM EMI Modelling of the Two-Boost-Circuit BPFC	41
4.3	Proposed novel 2-stage Two-Boost-Circuit IBPFC	42
4.4	Possible architecture of multi-stage IBPFC system	43
4.5	DM (left) and CM (right) EMI modeling of the N-stage Two-Boost-Circuit IBPFC	43

4.6	DM (right) and CM (left) EMI comparison of 2-stage interleaved (red) and non-interleaved (blue) Two-Boost-Circuit BPFC at 3.5kW with improper switching frequency at 75kHz	46
4.7	The MDOP design flow chart of IBPFC system	48
4.8	Minimal single (blue) and total (red) inductor's volume comparison of interleaved and non-interleaved Two-Boost-Circuit BPFCs	49
4.9	Efficiency comparison of 2-stage IBPFC at different input voltages	50
4.10	Key components' losses distribution at 3.5kW	51
4.11	Input voltage and current waveforms of 2-stage IBPFC at 3.5kW, PF=99%	51
4.12	Thermal measurement comparison of the proposed IBPFC system	52
4.13	EMI comparison at one eighth of full power and $230V_{ac}$ input without EMI filter	53
4.14	Harmonic Current vs Class D Standard	54
4.15	Harmonic Current vs Class D Standard	55
4.16	Harmonics' reduction vs. dithering factor γ when harmonics' order n changes from 1 to 4	57
4.17	Harmonics' spectrum comparison [67]	59
4.18	Harmonics' spectrum comparison for frequency dithering PWM (green) and standard PWM (blue), the red line is the filter's attenuation characteristic	60
4.19	Simplified heterodyne measurement chain and QP detection model of a test receiver[80]	62
4.20	Upper and lower envelope of the characteristic of the resolution bandwidth (RBW) filter as specified in CISPR 16 and filter characteristic used when modeling the RBW filter [80]	62
4.21	Input voltage (yellow, C1) and current (red, C2);output voltage (blue, C3) and current (green, C4) waveforms of the proposed frequency dithering IBPFC	63

4.22	Conducted EMI comparison of standard IBPFC and proposed frequency dithering IBPFC without filter at $110V_{ac}$ input and 1 over 8 peak power	65
4.23	Detailed EMI comparison of 4 highest harmonics in Fig.4.22 . . .	66
4.24	The schematic of the EMI filter	66
4.25	Conducted EMI comparison of standard IBPFC and proposed frequency dithering IBPFC at $110V_{ac}$ and 1/8 peak power with the same filter	67
5.1	Simplified diagram of efficiency measurement set up	70
5.2	Accuracy analysis procedure	71
5.3	Measurement Accuracy Prediction	72

List of Tables

1.1	PFC Specification	4
2.1	Comparison of five popular BPFC systems and the traditional Boost PFC system	17
3.1	Dimensions of The Kool Mu E Cores from <i>Magnetics</i> [®]	34
4.1	EMI Comparison of Critical Harmonics	64
5.1	Accuracy Specification of <i>N4L</i> [®] Precision Power Analyzer PPA5530[85]	70

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CHAPTER 1

Introduction

1.1 Scope

The scope of this thesis is to present the results obtained in the Ph.D. project “High Efficiency PFC front-end for Class-D Amplifiers”, performed by the author during the period from March 2009 through March 2012. Many of the scientific results obtained in the project have been or will be published in the form of conference papers and peer reviewed journal. The published and future published papers forming an integral part of this thesis are included in appendix [A1]-[A7].

The objective of this thesis is to supplement the already or future published information in [A1]-[A7] by placing the published papers in the context of the overall project and thereby present a more coherent and complete overview of the whole work and results obtained.

Furthermore, the author hopes that this thesis can serve as a small condensed “Designer’s Theoretical Handbook” on key fundamental issues related to the design and optimization of high efficient PFC for audio applications.

1.2 Background and Motivation

Due to the higher efficiency compared to linear audio amplifiers, the class-D amplifiers make it possible for more compact and high-power audio applications [1]. The power supply for the class-D amplifiers system from the AC mains is usually carried out in two stages (Fig.1.1): the single-phase main AC voltage is first converted into a DC voltage and then adapted to the load voltage level with a DC-DC converter with or without galvanic isolation. The simplest way of the rectification can be done by implementing unidirectional diode rectifier with DC capacitors smoothing of the output voltage (Fig.1.2(a)). Although this concept has its advantages of low complexity and high robustness, its disadvantages of relatively high effects of current distortion on AC mains and an unregulated output voltage directly dependent on the mains voltage level must be considered together. According to the guidelines to the harmonics current emission

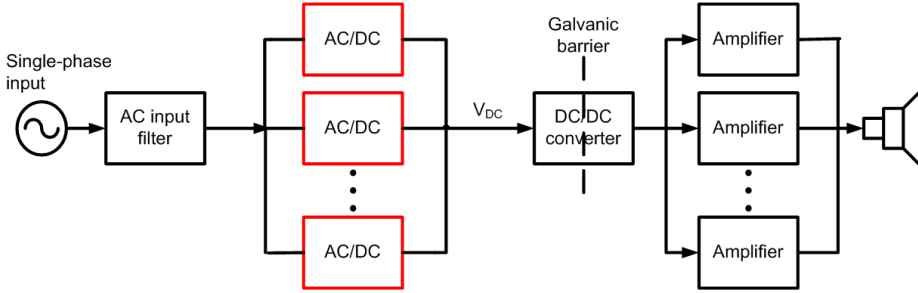
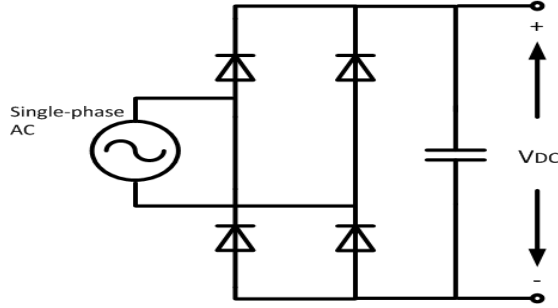
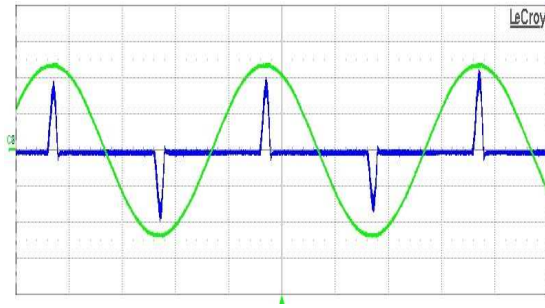


Figure 1.1: Block diagram of typical power supply configuration for supplying Class-D amplifiers system from the AC mains

limitation standard EN61000-3-2[2], the main behavior of a power converter can be characterized in general by the power factor (PF) and the input current harmonic emissions. The conduction state of the passive rectifier shown in Fig.1.2(a) is essentially determined by the mains line-to-line voltages, whereby only two diodes carry current at the same time when the input voltage higher than the output voltage on the DC capacitor. This means that each diode of the positive and negative bridge carries current only for a very short period (Fig.1.2(b)). Hence, the phase difference of input current and input voltage is huge, the PF is very low and the harmonic current emissions of input current is far above the EN61000-3-2 limitation. In order to avoid the low PF and high current harmonic emissions problems, the active PFC Converter must be built inside the rectifier system. Furthermore, for maintaining the natural advantage of high efficiency of class-D amplifiers, as its front-end, the PFC system is required to have an outstanding efficiency in a wide output power range.



(a) Passive single-phase diodes rectifier



(b) Input voltage (green) and current (blue) waveforms

Figure 1.2: Passive single-phase diodes rectifier and its characteristic waveforms

1.3 Specifications

The specifications of the PFC converter investigated in this work (Table.1.1) have been compiled in collaboration with our industry partner. The PFC system comprises of a DC voltage output with the terminal voltage V_o equals to 390V and universal AC line voltage input V_{in} ($85V \leq V_{in} \leq 265V$). An output peak power P_o of 3.5 kW is required. Moreover, the system is expected to achieved as high efficiency as possible.

Another important design parameter need to be defined in this project is the switching frequency f_s . The author selected f_s equals to 65kHz based on the consideration of system EMI optimization. Detailed analysis on switching frequency selection will be presented in Chapter 4 in this thesis.

Table 1.1: PFC Specification

Parameter	Value	Comments
Output Power P_o	3.5 kW	Maximum achievable power in single-phase PFC converter
Output voltage V_o	$390V_{dc}$	As required
Input Voltage V_{in}	85-265 V_{ac}	Universal line input
Maximum Efficiency η	$\geq 98\%$	At high line $230V_{ac}$
Input Harmonic Current Emissions	EN61000-3-2, Class D	Measurement required to take under one eighth of the peak power
Switching Frequency f_s	65kHz	For better EMI performance

1.4 Project Objectives and Contributions

The primary objectives of this project regarding the selection and design of the single-phase PFC converter are:

- Converter peak efficiency $> 98\%$ at the high line operating condition ($V_{in} = 230V$);
- Converter efficiency $> 90\%$ under universal line input at peak power ($P_o \leq 3.5kW$);
- High power density;
- Suggestions for cost-efficient EMI suppression.

The contributions of this work are:

- A overview on Bridgeless PFC converter topologies, includes a detailed comparison to judge which one should be the best suitable to fulfil the specifications in Table.1.1 (Chapter 2);
- An optimization for high efficient Two-Boost-Circuit BPFC converter based on high efficiency and high power density Boost inductor design (Chapter 3);
- A simplified EMI modelling process is used to predict the EMI performances of the BPFC converter (Chapter 4);

- A novel Interleaved BPFC(IBPFC) topology is proposed, the insight of EMI suppression versus the number of interleaved stages is investigated (Chapter 4);
- A multi-objective optimization design procedure (MDOP) is implemented to find the optimal parameters for the novel IBPFC system to achieve high efficiency, low EMI and high power density at the same time (Chapter 4);
- A detailed research on frequency dithering modulation based on its advantages and limitations is carried out for further reducing the EMI emissions of the novel IBPFC topology (Chapter 4).

1.5 Project Plan and Content

A flow chart presents the work packages carried out in the course of this Ph.D. project (Fig.1.3). Six conference papers have been published and one journal has been submitted for peer reviewed. Additionally, the flow chart also illustrates how the publications relate to the key parts of the Ph.D. project.

1.6 Thesis Structure

The structure, organization and content of this Ph.D. thesis in the flowing chapters are presented (Fig.1.4). The conference papers and journal paper in [A1]-[A7] form an integral part of this Ph.D. thesis and are appended. Because the purpose of this thesis is to complement the already and future published papers by providing a condensed and coherent presentation of the overall project and its results, special focus will be devoted to presenting a coherent derivation of the key fundamental theoretical aspects of this project.

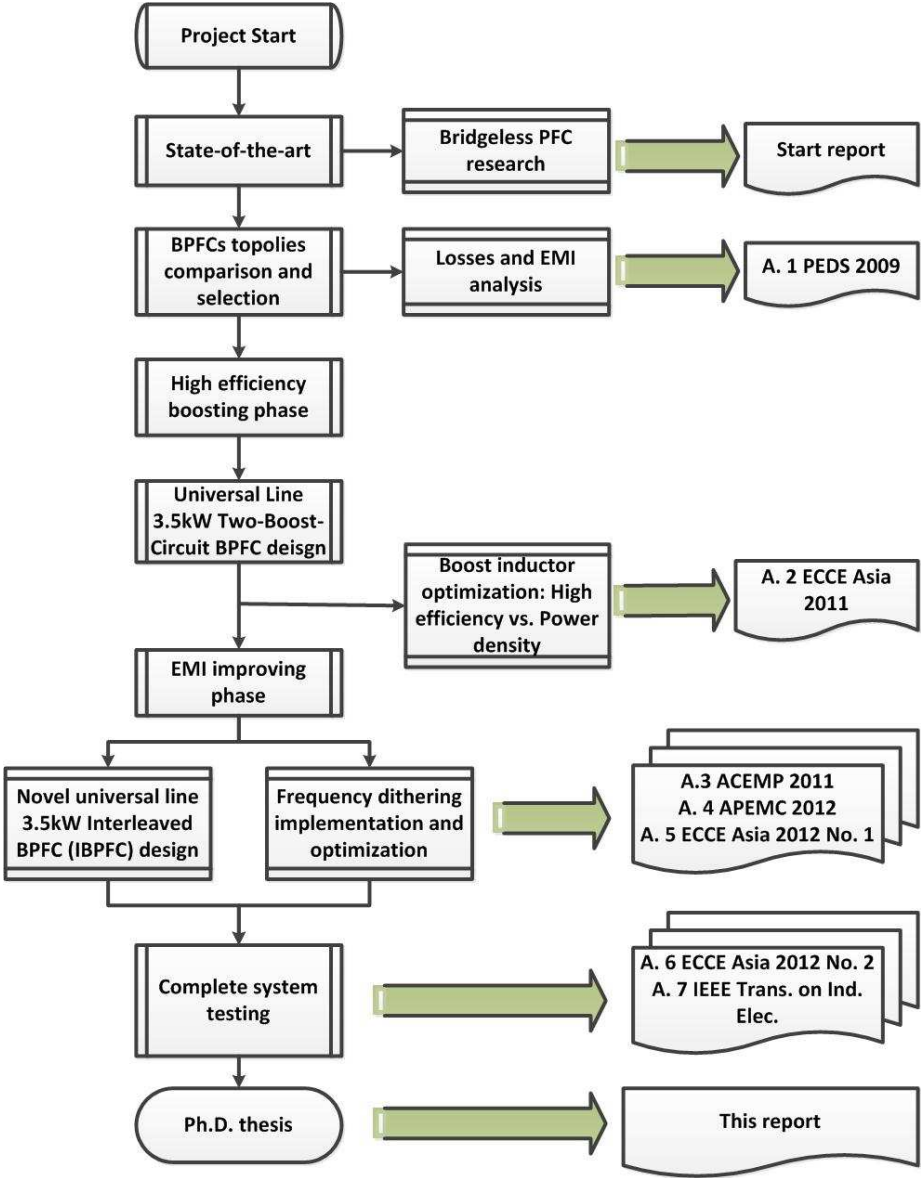


Figure 1.3: Ph.D. Project Overview

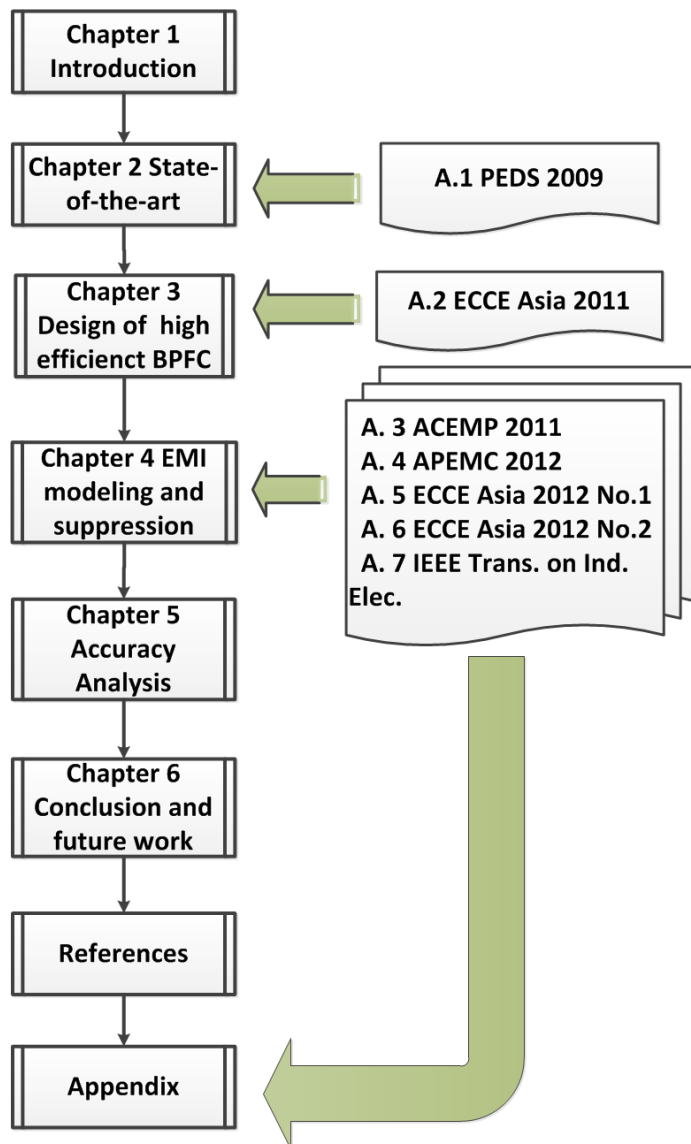


Figure 1.4: Ph.D. Thesis Structure

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CHAPTER 2

State of the Art

As it has been emphasized in Chapter 1, the major task of the PFC design in this work is efficiency optimization. However, due to the traditional single-phase PFCs usually have full-wave rectifiers in the input side, which contribute a large part of the semiconductor losses; recently, a new PFC family named Bridgeless PFCs (BPFCs) has been proposed to achieve higher efficiency by removing the full-wave AC rectifiers in front. Therefore, in this work, the author mainly interested in the high efficiency BPFC topologies.

However, may the BPFC topologies be suitable for this work, is unclear. Moreover, beyond their high efficiency characteristics, the electromagnetic interference (EMI) of the BPFCs need to be weighed as well.

The purpose of this Chapter is to present an overview of the high performance state-of-the-art BPFC converters. The recent published literatures primarily in the form of journal papers and conference papers has been researched and analyzed. Main focus has been devoted to compare and evaluate their efficiency and EMI together and to select the most proper BPFC topology to meet the overall specifications of this project in Chapter 1 (Table.1.1).

Furthermore, for each compared BPFC solution, a short description of the operation principle is given, too.

In additional, the paper published as part of this project is also included in the state-of-the-art analysis(appendix A1).

2.1 Derivation of Bridgeless PFC Converters

The idea of the basic Bridgeless PFC (BPFC) converters (Fig.2.1(a)) goes back to eighties [3]. Comparing to the traditional most popular Boost type PFC (Fig.2.1(b)), this smart concept improves PFC's efficiency by removing the bridge rectification system in front of it. During the last decades, researches of the BPFC converters were taken not only to analyse the operation principles but also to investigate its performances in different aspects [4–26]. With the

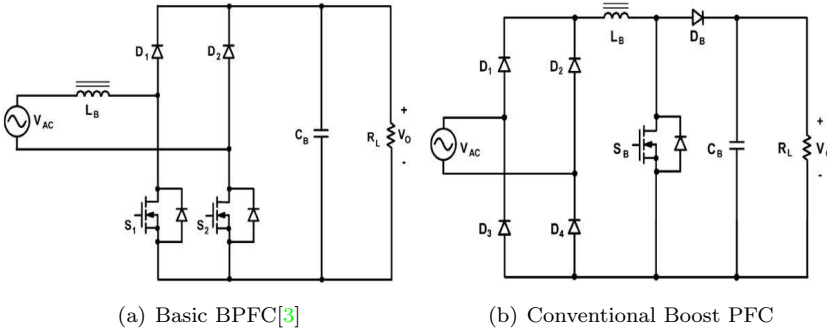


Figure 2.1: Basic BPFC and Conventional Boost PFC Topologies

increasing demands on energy saving, in recent years the implement of BPFC system have became more and more attractive. The collection below lists five classic published BPFC solutions for high efficiency applications. And in each selected BPFC converter, the brief descriptions of the topology and its merits and disadvantages are provided.

2.2 BPFC Topologies Overview

2.2.1 Basic BPFC System

The basic BPFC system shows in Fig.2.1(a). Compare to the conventional Boost PFC (Fig.2.1(b)), the most important advantage of it is that it doesn't need four

line frequency diodes operating as voltage rectifier.

Operation principles: Due to the basic BPFC works symmetrically, only half of the AC line period is considered here. For example, in the positive AC line period, when MOS S_1 is on, the Boost inductor is charged by S_1 and the body diode of MOS S_2 . When MOS S_1 is off, the Boost inductor is discharged through Boost diode D_1 and the body diode of MOS S_2 .

Merits:

Compared to the Boost PFC, the basic BPFC has one less line frequency diode in current flowing path, which reduces the semiconductor losses and enhance the system efficiency.

Disadvantages:

However, compare to the conventional Boost PFC, the output ground of basic BPFC has high frequency voltage pulses in the negative AC line period due to it doesn't connect to the positive terminal of AC source directly (Fig.2.2). These voltage pulses can induce high CM EMI noises which may affect system stability and bring difficulties to EMI filter design.

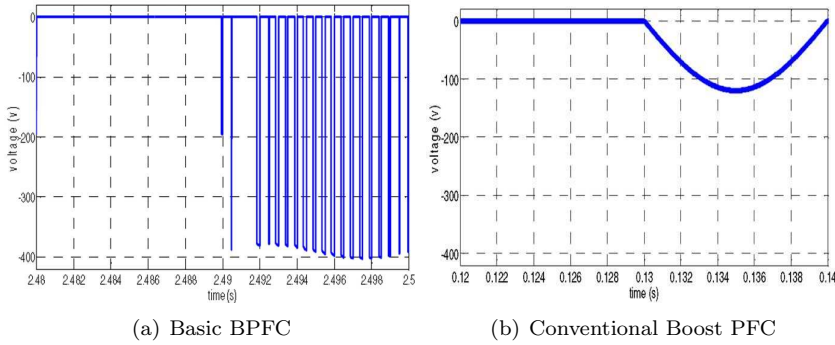


Figure 2.2: Voltage Waveforms Between Neutral and Output Power Ground [27]

2.2.2 BPFC with Two Boost Circuits

The Two-Boost-Circuit BPFC in Fig.2.3(a) is an EMI improved version of basic BPFC.

Operation Principles:

Due to the Two-Boost-Circuit BPFC works symmetrically, only half of the AC line period is considered here. For example, in the positive AC line period, when

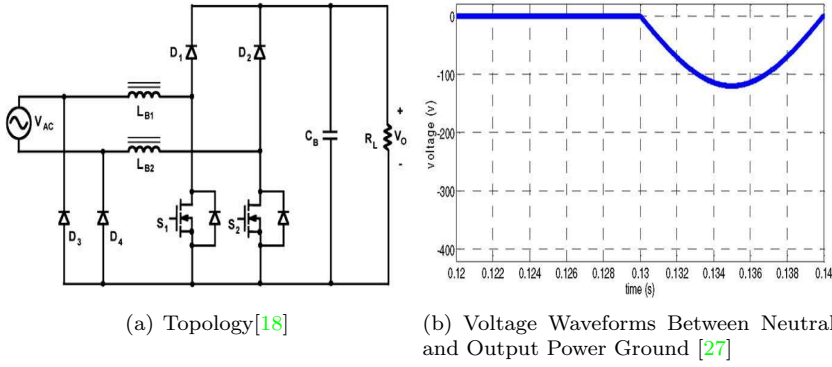


Figure 2.3: Two-Boost-Circuit BPFC

MOS S_1 is on, the Boost inductor is charged by S_1 and line frequency diode D_4 . When MOS S_1 is off, the Boost inductor is discharged through Boost diode D_1 and the line frequency diode D_4 .

Merits:

By implementing two line frequency diodes D_3 and D_4 , the output ground is connected to the terminals of AC mains directly in the whole AC line period, which stabilizes voltage potential of output ground and reduces CM EMI generation (Fig.2.3(b)). In addition, instead of using the relatively high forward voltage MOS's body diodes as a part of the current flowing path, using normal line frequency diodes D_3 and D_4 helps to improve system efficiency.

Disadvantages:

Due to the two extra line frequency diodes D_3 and D_4 and the one extra Boost inductor L_{B2} , this topology has higher cost and volume than the basic BPFC.

In publication [25], a 1kW universal line Two-Boost-Circuit BPFC is presented. The output DC voltage is 400V. The maximum measured efficiency reaches 97% at $220V_{ac}$ input and 600W.

2.2.3 Basic BPFC with Bidirectional Switch

Fig.2.4(a) is an modification of Two-Boost-Circuit BPFC (Fig.2.3(a)) by disconnecting the sources of MOSs S_1 and S_2 from output ground.

Operation Principles:

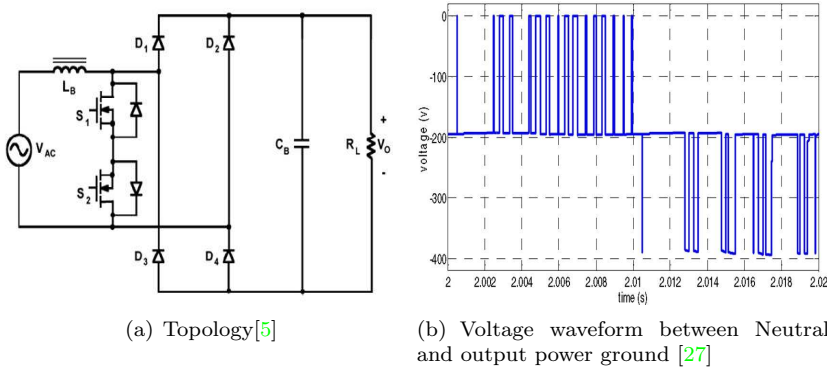


Figure 2.4: Basic BPFC with Bidirectional Switch

Due to the BPFC with bidirectional switch works symmetrically, only half of the AC line period is considered here. For example, in the positive AC line period, when MOS S_1 is on, the Boost inductor is charged by S_1 and the body diode of MOS S_2 . When MOS S_1 is off, the Boost inductor is discharged through Boost diode D_1 and D_4 .

Merits:

By removing one Boost inductor L_{B2} , this topology has lower cost and volume than the Two-Boost-Circuit BPFC in Fig.2.3(a).

Disadvantages:

It should be noticed in Fig.2.4(a), all the diodes are fast recovery diodes, however, in Fig.2.3(a), only D_1 and D_2 are fast recovery diodes, D_3 and D_4 are line frequency diodes because each of them conducts in half of the AC line period. Normally, at the same voltage and current rating, the forward voltage drop of the line frequency diodes are lower than the fast recovery diodes, which means, with the same forward current, the line frequency diodes has lower conduction losses than fast recovery diodes. Therefore, if other semiconductors are the same, the total semiconductors' conduction losses of the Two-Boost-Circuit can be expected lower than the basic BPFC with bidirectional switch.

Furthermore, compare to the Two-Boost-Circuit BPFC and basic BPFC, the output ground of basic BPFC with bidirectional switch has high frequency voltage pulses in the whole AC line period due to it doesn't connect to the terminals of AC mains directly all the way (Fig.2.4(b)). These voltage pulses will induce high CM EMI noises and bring difficulties to EMI filter design. Besides, the BPFC in Fig.2.4(a) requires a complex control and drive circuit, due to the sources of MOSs do not connect to the output ground.

2.2.4 Pseudo Totem-pole BPFC

Pseudo totem-pole BPFC (Fig.2.5(a)) can be considered as another modification of Two-Boost-Circuit BPFC (Fig.2.3(a)).

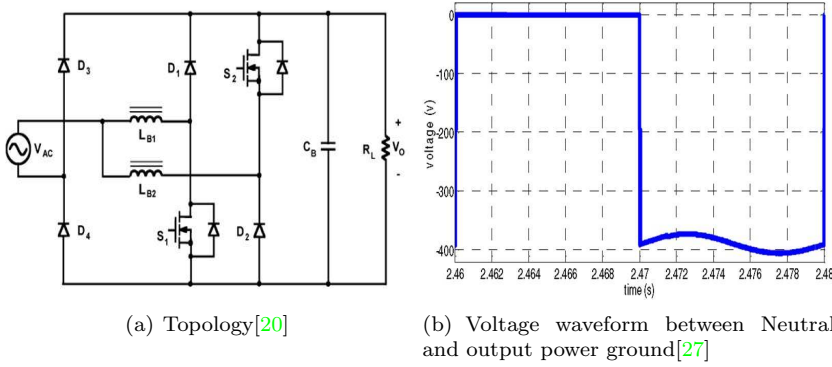


Figure 2.5: Pseudo Totem-pole BPFC

Operation principles:

Due to the Pseudo totem-pole BPFC works symmetrically, only half of the AC line period is considered here. For example, in the positive AC period, Boost inductor L_{B1} is charged by MOS S_1 and diode D_4 , and discharged through diodes D_1 and D_4 . Therefore, the same as Fig.2.3(a), diode D_1 should be the fast recovery diode and diode D_4 is the normal line frequency diode due to it conducts in the whole positive AC line period.

Merits:

By implementing two line frequency diodes D_3 and D_4 , the voltage positional of output ground is stabilized in the whole AC period which reduces CM EMI generation (Fig.2.5(b)).

Disadvantages:

However, this BPFC also requires a complex control and drive circuit, due to the source of MOS S_2 does not connect to the ground. Besides, comparing to basic BPFC (Fig.2.1(a)), the Pseudo totem-pole BPFC asks for one more Boost inductor, which increase the system volume.

2.2.5 Totem-pole BPFC

Fig.2.6(a) is a modification of Basic BPFC (Fig.2.1(a)). by exchanging the position of Boost diode D_1 and MOS S_2 .

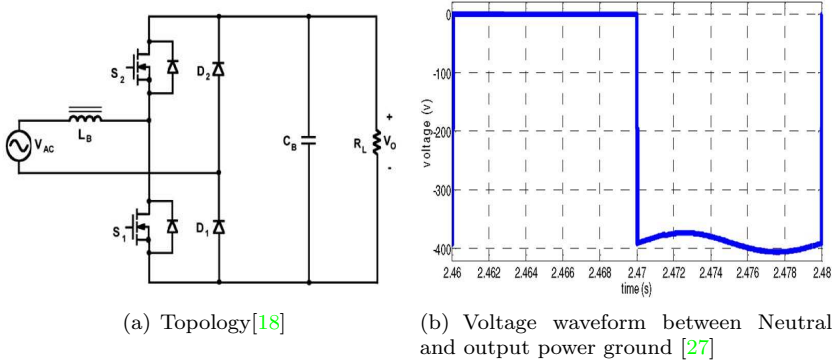


Figure 2.6: Totem-pole BPFC

Operation Principles:

Due to the Totem-pole BPFC works symmetrically, only half of the AC line period is considered here. For example, during the positive AC period, when MOS S_1 and diode D_1 conduct, the Boost inductor is charged. When MOS S_1 turns off, the Boost inductor is discharged through body diode of MOS S_2 and D_1 .

Merits:

Due to the output ground is directly connected to the terminal of AC source by D_1 in the positive line period and the terminal of Boost inductor by the body diode of S_1 in the negative line period, the CM EMI generation problem from basic BPFC can be solved.

Disadvantages:

However, the reverse-recovery performance of the body diodes of the switches makes continuous current mode (CCM) operation of this BPFC (Fig.2.6(a)) impractical. Furthermore, compare to the basic BPFC, although they have the same semiconductor numbers in the current flowing path, in the Totem-pole BPFC, each MOS's body diode conducts in the switching frequency. For normal MOSs, their body diodes are very slow, which are not good for fast recovery application. Additionally, the Totem-pole BPFC requires a complex control and drive circuit, due to the source of MOS S_2 doesn't connect to ground.

In publication [28], an optimized 500W universal line Totem-pole BPFC is presented. The output DC voltage is 380V. The maximum measured efficiency reaches 96.8% at $220V_{ac}$ input and 500W. In publication [29], a 800W universal line interleaved Totem-pole BPFC is presented. The output DC voltage is 400V, the maximum measured efficiency reaches 97.8% at $264 V_{ac}$ input and 800W.

2.3 Summary of State-of-the-art Analysis

In this Chapter, the derivation of BPFC is introduced firstly. And then, five popular BPFC systems are selected for detailed comparison. Their operation principles, advantages and disadvantages are analysed. The summary of their performances are given in Table.2.1. Where, the type and number of semiconductors operating in each half line period are shown, the system peak efficiency and EMI performance are highlighted.

According to the information from Table.2.1, the conclusions can be drawn as below:

1. In these classic BPFC topologies, very few of them are verified by experiments;
2. The designs of Two-Boost-Circuit BPFC and Totem-pole BPFC are achieved only in low and medium power and their peak efficiency are 97% and 97.8% respectively;
3. There are lack of researches based on high power universal line BPFC design and optimization;
4. The Two-Boost-Circuit BPFC can be a very useful topology for this work due to it has the possibility to run in a high power level with good efficiency, relatively lower EMI and less complex control and gate drive systems.

Table 2.1: Comparison of five popular BPFC systems and the traditional Boost PFC system

Topology	Inductor Opera- tion	No.of D_F^a	No.of D_L^b	No.of MOS	No.of D_{MOS}^c	Total No.	Power Level	CM EMI	Peak Effi- ciency
Boost PFC	Charge	0	2	1	0	3	High	good	_d
	Discharge	1	2	0	0				
Basic BPFC	Charge	0	0	1	1	2	Medium	poor	-
	Discharge	1	0	0	1				
Two-Boost-Circuit BPFC	Charge	0	1	1	0	2	High	good	97%
	Discharge	1	1	0	0				
Basic BPFC with Bidirectional Switch	Charge	0	0	1	1	2	Medium	poor	-
	Discharge	2	0	0	0				
Pseudo totem-pole BPFC	Charge	0	1	1	0	2	Medium	good	-
	Discharge	1	1	0	0				
Totem-pole BPFC	Charge	0	1	1	0	2	Low-Medium	good	97.8%
	Discharge	0	1	0	1				

^a D_F means fast recovery diode

^b D_L means line frequency diode

^c D_{MOS} means the body diode of MOS

^d Symbol '-', means no data available

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CHAPTER 3

Design of the High Efficient BPFC - Boost Inductor Optimization

In this Chapter, a useful design procedure is presented for Two-Boost-Circuit Bridgeless PFC (BPFC) converter based on Boost inductor optimization, which can be utilized to gain high efficiency and high power density at the same time.

3.1 Topology Basic Operation

Chapter 2 discussed the basic performances of five BPFC topologies. These topologies can be expected to have higher efficiency than traditional Boost PFC due to the reduction of semiconductor numbers in current flowing path. According to its conclusion, the Two-Boost-Circuit BPFC (Fig.3.1) shows better performances than others due to system efficiency improvement without inducing EMI problems.

The Two-Boost-Circuit BPFC has a symmetric structure. During the positive AC line, diode D_1 operates when MOS S_1 turns off, and Boost inductor L_1

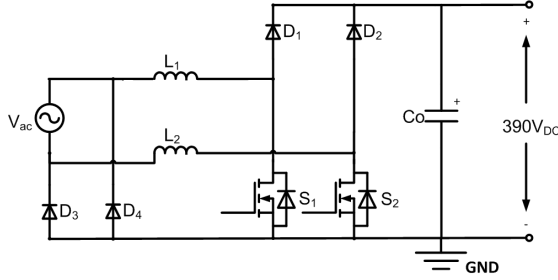


Figure 3.1: Two-Boost-Circuit BPFC with good efficiency and low conducted EMI

discharges, meanwhile gives energy to load. When MOS S_1 turn on, Boost inductor is charged, and diode D_1 is off. The output capacitor discharges and transfers energy to load. Line frequency diode D_3 returns current from output ground to neutral and stabilize its voltage potential. In the negative AC line, the BPFC works symmetrically. Its operation principles are shown in Fig. 3.2. And it is easy to see that the BPFC in Fig.3.1 is equal to two normal Boost PFCs, one works in positive line period and the other works in negative line period.

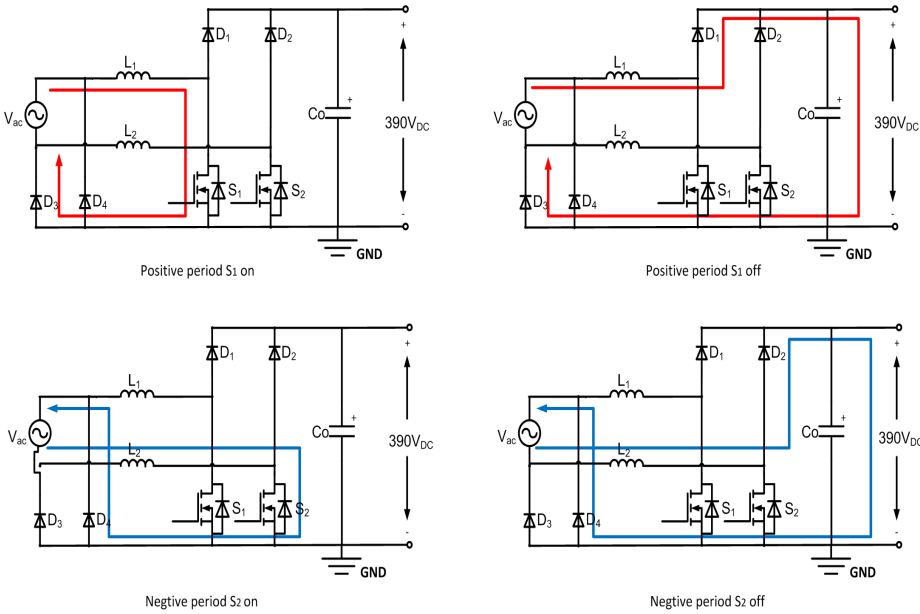


Figure 3.2: Operation principles of the Two-Boost-Circuit BPFC

In our application, the BPFC works at 3.5kW power level. In order to reduce the core losses from Boost inductors, the BPFC runs in the continuous current mode (CCM). Because the average energy stored in Boost inductors in each switching cycle is approximately zero in steady states, the input and output transfer function of the selected Two-Boost-Circuit BPFC (Fig.3.1) is the same as normal Boost PFC, which can be expressed as:

$$V_o = \frac{\sqrt{2}V_{in,rms}|\sin(2\pi f_L t)|}{1 - d(t)} \quad (3.1)$$

Where V_o is output voltage, $V_{in,rms}$ is the input RMS voltage, f_L is line frequency and $d(t)$ is the instantaneous switch on duty cycle.

3.2 High Efficiency Boost Inductor Design

The Boost inductor design is tough and important for any Boost type PFC converters, due to a good design can reduce not only the losses but also the volume of the system. In order to optimize the Boost inductor and improve the efficiency in the Two-Boost-Circuit BPFC, the questions below should be taken into considerations at the very beginning:

1. Is there any reasonable region for Boost inductance selection?
2. How to choose windings and cores to minimize the magnetic losses while still maintaining high power density?

By answering these questions, in this Section, a useful balance between efficiency and power density of the Boost inductor design in a Two-Boost-Circuit BPFC is achieved through using the optimized design procedure.

3.2.1 Conventional Boost Inductor Design Procedure

Generally speaking, it is typical to design the Boost inductor based on its inductance and average current. It is well known that the peak inductor current ripple limitation and the inductor operating condition determine the minimal value of the Boost inductance together [30].

Since the worst-case peak inductor current occurs at low line and maximum load, which is:

$$\hat{I}_{L,max} = \hat{I}_{in,max} + 0.5\hat{I}_{ripple,max} \quad (3.2)$$

Where, ‘max’ means maximum value and symbol $\hat{}$ means the peak value. Therefore, $\hat{I}_{L,max}$ means the peak value of maximum inductor current, $\hat{I}_{in,max}$ means the peak value of maximum input current, and $\hat{I}_{ripple,max}$ means the peak value of maximum inductor ripple current.

Many design cookbooks claims that a good compromise between the peak inductor current ripple and its peak current is to allow a 20% current ratio. Assuming:

$$\hat{I}_{ripple,max} = 0.2\hat{I}_{in,max} \quad (3.3)$$

Hence, the minimal inductance to meet the peak current ripple limitation can be calculated as:

$$L_{min1} = \frac{\hat{V}_{in,min}D_{worst}}{\hat{I}_{ripple,max}f_s} \quad (3.4)$$

Where, ‘min’ means minimal value and ‘ D_{worst} ’ is the worst-case on duty ratio which is 0.69.

Since the BPFC in this work is designed to operate in CCM mode, the inductance should also be big enough to avoid the inductor current dropping to zero during its discharge period in each switching cycle. So, at any switching period:

$$\begin{aligned} I_{L,min}(n) &= I_{in}(n) - 0.5I_{ripple,max}(n) > 0 \downarrow \\ \frac{2P_{in}}{\hat{V}_{in}} \sin(\frac{n}{N}\pi) &> \frac{1}{2} \frac{\hat{V}_{in}}{L} \sin(\frac{n}{N}\pi) (1 - \frac{\hat{V}_{in}}{V_o} \sin(\frac{n}{N}\pi)) T_s \downarrow \\ L &> \frac{\hat{V}_{in}^2 T_s \eta}{4P_o} \left(1 - \frac{\hat{V}_{in}}{V_o} \sin(\frac{n}{N}\pi) \right) \end{aligned} \quad (3.5)$$

Where, ‘N’ means the total number of sample points, ‘n’ means sample step, T_s is switching period, ‘ η ’ means system efficiency.

The boost inductor L in Eq.3.5 reaches maximum value when:

$$\sin(\frac{n}{N}\pi) \rightarrow 0 \quad (3.6)$$

Hence,

$$L_{min2} > \frac{\hat{V}_{in}^2 T_s \eta}{4P_o} \quad (3.7)$$

According to Eqs.(3.4) and (3.7), the minimal Boost inductance should satisfy the following condition:

$$L_{min} > \{L_{min1}, L_{min2}\}_{max} \quad (3.8)$$

When the selection of inductance is ready, suitable cores and windings can be chosen based on the maximum DC and RMS current flowing through the inductor. Normally, the core and winding selection processes can be quickly done by following the guideline provided by the magnetic manufacturers, such as: [31–33].

It is obviously that using the inductor design method above will lead to a quick design and short the development period. However, this design method almost come from experiences, whether it have been optimized is doubtful. For example: considering the amount of input current ripple, on one hand, allowing more current ripple will reduce the inductance, this may reduce the size of the inductor due to the inductor's volume is in direct proportion to its inductance. However, on the other hand, it will increase the input line noise, ripple current in the Boost inductors and the peak current through the diodes and MOSs. These may not only increase the difficulties of EMI filter design, but also lead to higher core losses, AC winding losses and higher semiconductor losses. Furthermore, the reason for using the 20% peak to peak ripple to peak current ratio is unclear.

Because the Boost PFC inductor design has been ambiguous for long, the discussion below will firstly focus on how to improve the system efficiency by optimizing the Boost inductance. And then, the detailed study on system volume optimization will be presented. In order to avoid including too much critical issues at one time, the EMI is not discussed in this Chapter.

3.2.2 Optimized Design Procedure

The optimization procedure below (Fig.3.3) is carried out based on high efficiency Two-Boost-Circuit BPFC in Fig.3.1 operating in CCM. And basically any Boost type PFCs working in CCM could be considered in this procedure as well.

In the optimization, the switching frequency is limited to 65kHz. The start point of this procedure is the specifications definition, which including all the fixed critical parameters in the main circuit. For example: input and output voltages, output peak power, output capacitors, inner parameters of the semiconductors and so on. Next, the important initial starting values of the BPFC variables are

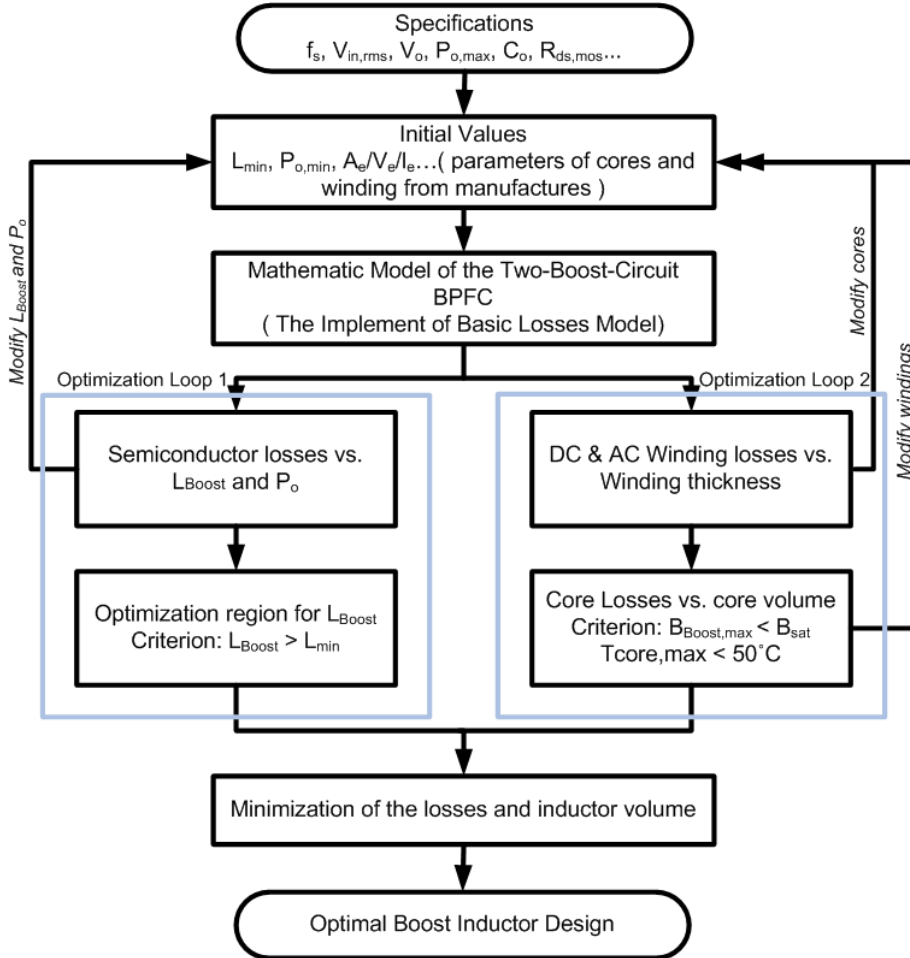


Figure 3.3: Optimization procedure of inductor design in CCM for Two-Boost-Circuit BPFC with balance of efficiency and power density

set. Such as: minimal CCM Boost inductance L_{min} , starting minimal output power $P_{o,min}$, parameters of cores and windings from manufactures. After finishing defining all the specifications and initial values, the mathematical BPFC model will be used to calculate the RMS and average currents flowing through all the components in the circuit, finally semiconductor losses and inductor losses can be predicted.

There are two inner optimization loops in the procedure. Inner optimization loop 1 seeks the characteristics of semiconductor losses versus Boost inductance

and output power, which will give a most suitable region of Boost inductance at certain power level. And inner optimization loop 2 gets a compromise of volume and efficiency of the inductor. Both of the two optimization loops will be explained in detail in the later sections. The optimal design can be realized by running optimization loop 1 and 2 together.

3.2.3 Mathematical Modelling

In order to predict the performances of Boost inductors, the mathematical model should be able to show the RMS and average currents of the BPFC for calculating losses and choosing magnetic components. In the derivations below, the normalization has been taken in order to make the modelling process more clear. For more details please refers to Appendix A.2.

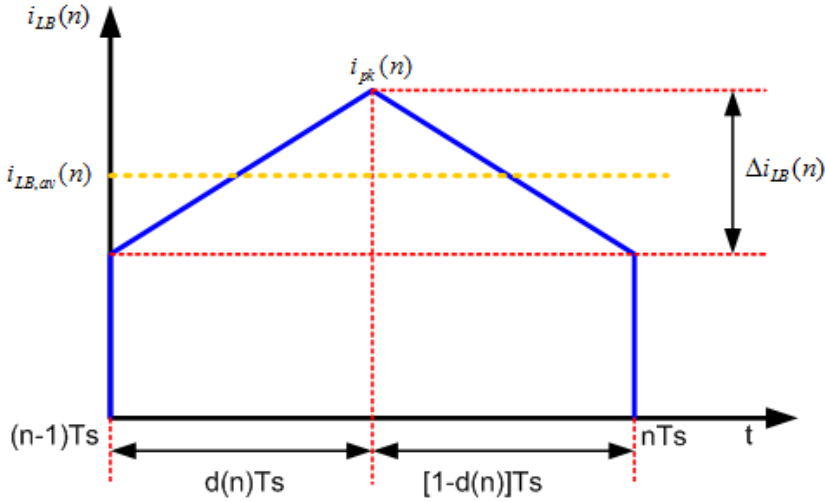


Figure 3.4: Boost inductor current waveform in a switching cycle in CCM

Starting from the Boost inductor, its current waveform during a switching cycle can be approximated as in Fig.3.4. The normalized average Boost inductor current in the n th switching cycle is:

$$i_{LB,av,n}(n) = |i_{in}(n)|/I_o = \hat{I}_{in,n} |\sin(2\pi nT_s/T_L)|, n = 1, \dots, N \quad (3.9)$$

Where, subscript n means normalized, subscript av means average and T_L is the AC line period.

The current ripple in Boost inductor in the n th switching cycle is determined

as:

$$\Delta i_{LB,n}(n) = \frac{|v_{in}(n)|}{I_o L_B(n)} d(n) T_s \quad (3.10)$$

$$= \frac{|v_{in,n}(n)|(1 - |v_{in,n}(n)|)}{L_{B,n}} \quad (3.11)$$

Where, d is the switching on duty ratio. In CCM mode, its discrete time function is:

$$d(n) = 1 - \frac{|v_{in}(n)|}{V_o} = 1 - |v_{in}(n)| \quad (3.12)$$

And,

$$L_B = L_{B0} \frac{A_{L,effi}}{A_{L,0}}, A_{L,effi} = f(M i_{in}) \quad (3.13)$$

L_B is the Boost inductance with DC bias. It is a function of number of turns M and input current i_{in} due to the DC magnetizing force. $A_{L,0}$ is the initial nominal inductance, and $A_{L,effi}$ is the nominal inductance with DC bias which can be calculated based on the data sheet of the core. For example, reference [34] shows the DC bias performance of Kool Mu cores from *Magnetics*®.

The relevant RMS and average currents for Boost inductor and semiconductor losses calculations under CCM in the n th switching cycle are listed below:

$$\begin{aligned} i_{LB,rms,n}(n) &= \frac{|I_{in}(n)|}{I_o} \sqrt{1 + \frac{1}{3} \left(\frac{\Delta i_{LB}(n)}{2i_{in}(n)} \right)^2} \\ &= \sqrt{i_{in,n}(n)^2 + \frac{\Delta i_{LB,n}(n)^2}{12}} \end{aligned} \quad (3.14)$$

$$\begin{aligned} i_{S1,rms,n}(n) &= \frac{|I_{in}(n)|}{I_o} \sqrt{1 + \frac{1}{3} \left(\frac{\Delta i_{LB}(n)}{2i_{in}(n)} \right)^2} \sqrt{d(n)} \\ &= \sqrt{d(n) \left(i_{in,n}(n)^2 + \frac{\Delta i_{LB,n}(n)^2}{12} \right)} \end{aligned} \quad (3.15)$$

$$i_{D1,av,n}(n) = (1 - d(n)) \frac{|i_{in}(n)|}{I_o} = (1 - d(n)) |i_{in,n}(n)| \quad (3.16)$$

$$i_{D3,av,n}(n) = \frac{|i_{in}(n)|}{I_o} = |i_{in,n}(n)| \quad (3.17)$$

Where, subscript *av* means average.

It should be noticed that even in the CCM condition, around the zero crossing of the line voltage, during a few switching cycles, the BPFC operates in DCM

mode inevitably. The DCM periods are also taken into consideration during the calculation in order to obtain a more precise prediction.

The CCM and DCM boundary condition happens when:

$$i_{in,n}(n) = 0.5\Delta\hat{i}_{LB,n}(n) \quad (3.18)$$

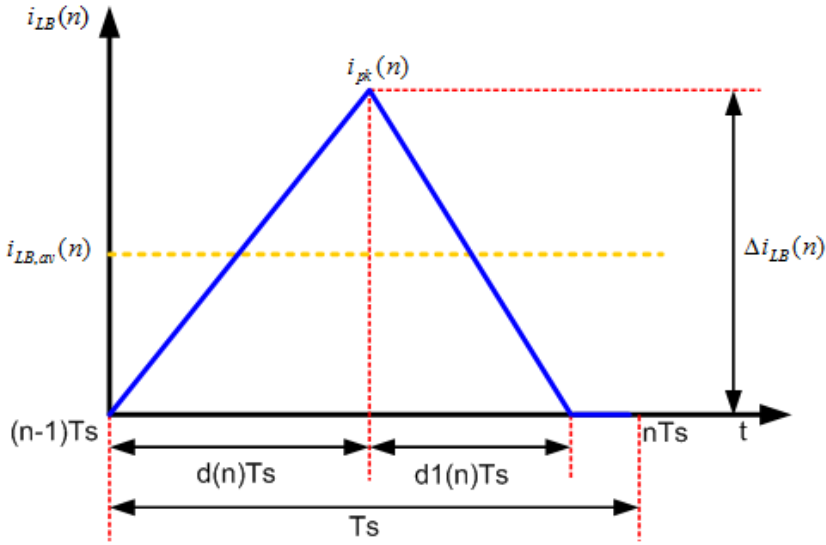


Figure 3.5: Boost inductor current waveform in a switching cycle in DCM

The same as the previous procedure, in DCM operations, the current waveform of Boost inductor during a switching cycle can be approximated as in Fig.3.5. The normalized average Boost inductor current in the n th switching cycle is the same as Eq.(3.9).

In DCM condition, MOSFET's duty ratio is:

$$d(n) = \sqrt{\frac{2(1 - |v_{in,n}(n)|)|i_{in,n}(n)|}{|v_{in,n}(n)|}} L_{B,n} \quad (3.19)$$

And d_1 is the conduction duty ratio of the Boost diodes:

$$d_1(n) = \sqrt{\frac{2|v_{in,n}(n)|i_{in,n}(n)|}{(1 - |v_{in,n}(n)|)}} L_{B,n} \quad (3.20)$$

The $\hat{i}_{LB,n}$ is the normalized peak inductor current in DCM.

$$\hat{i}_{LB,n}(n) = \sqrt{|i_{in,n}(n)| \frac{2|v_{in,n}(n)|(1 - |v_{in,n}(n)|)}{L_{B,n}}} \quad (3.21)$$

The relevant RMS and average currents for Boost inductor and semiconductor losses calculations under DCM in the n th switching cycle are listed below:

$$i_{LB,rms,n}(n) = \sqrt{\frac{d(n) + d_1(n)}{3}} \hat{i}_{LB,n}(n) \quad (3.22)$$

$$i_{S1,rms,n}(n) = \hat{i}_{LB,n}(n) \sqrt{\frac{d(n)}{3}} \quad (3.23)$$

$$i_{D1,av,n}(n) = d_1(n) \frac{\hat{i}_{LB,n}(n)}{2} \quad (3.24)$$

$$i_{D3,av,n}(n) = \frac{i_{in}(n)}{I_o} = |i_{in,n}(n)| \quad (3.25)$$

The corresponding normalized RMS and average currents during a half line period are as below:

$$I_{X,rms,n} = \sqrt{\frac{1}{N'} \sum_{n=1}^{N'} i_{X,rms,n}(n)^2} \quad (3.26)$$

$$I_{Y,av,n} = \frac{1}{N'} \sum_{n=1}^{N'} i_{Y,av,n} \quad (3.27)$$

Where, X symbolizes MOSs and Boost inductors and Y represents Boost diodes and return diodes. N' is the number of sampling data in half line period.

3.2.4 Inductance vs. Semiconductor Losses

In this section, the insight of Boost inductance versus semiconductor losses is presented. It shows the method to evaluate the system efficiency affected by Boost inductance and gives the most suitable region for Boost inductance selection.

3.2.4.1 Semiconductor Losses

The basic losses model is implemented in this section to predict the semiconductor losses. The key semiconductors' data of the BPFC are:

1. MOSs:IPW60R045CP from *Infineon*[®]
2. Boost diodes:STPSC1206 SiC diode from *ST*[®]
3. Current return diodes: STTH6004W from *ST*[®]

For all calculations and measurements in this Chapter, a reference ambient temperature ($T = 25^\circ\text{C}$) has been used.

MOSFET Losses The calculation of the power dissipated in the switches considers two different losses mechanisms: conduction losses and switching losses. The RMS currents through the switches determine the respective conduction losses.

According to Eq.(3.26), in half line period, the switch generates the total conduction losses:

$$P_{Rds} = (I_{S1,rms,n} I_o)^2 R_{S1} \quad (3.28)$$

Where R_{S1} is the on resistance of MOS.

The calculation of the switching losses is more complex, since it not only depend on the selected power MOS's intrinsic parameters, but also the parasitic parameters (e.g. PCB stray inductances). In this thesis, all the switches operate in hard switching mode, the accrue switching loss is due to high current and high voltage being present in the device simultaneously for a short period. It can be calculated approximately as below [35]:

$$P_{sw} = \frac{V_{DS} \cdot I_{DS}}{2} \times \frac{t_2 + t_3}{T_s} \quad (3.29)$$

$$t_2 = (C_{GS} - C_{RSS}) \frac{V_{GS,Miller} - V_{TH}}{I_{G2}} \quad (3.30)$$

$$I_{G2} = \frac{V_{DRV} - 0.5 \cdot (V_{GS,Miller} + V_{TH})}{R_{gate}} \quad (3.31)$$

$$t_3 = C_{RSS} \cdot \frac{V_{DS}}{I_{G3}} \quad (3.32)$$

$$I_{G3} = \frac{V_{DRV} - V_{GS,Miller}}{R_{gate}} \quad (3.33)$$

Where, R_{gate} is gate resistor, $V_{GS,Miller}$ is the miller plateau level, V_{TH} is the threshold voltage, V_{DRV} is gate drive voltage, C_{GS} is the capacitor formed by the overlap of the source and channel region by the gate electrode, C_{RSS} is the capacitance from gate to drain.

Therefore, the total losses dissipate on MOS is:

$$P_{MOS,tot} = P_{Rds} + P_{sw} \quad (3.34)$$

Diode Losses In the BPFC prototype, both of the Boost diode and line frequency diode are implemented with Silicon carbide (SiC) diodes. Their switching losses can be neglected due to they do not suffer from reverse recovery.

According to Eq.(3.27), in half line period, the conduction losses of Boost diode and line frequency diode are:

$$P_{DB,con} = (I_{DB,av,n} I_o) V_{F,DB} \quad (3.35)$$

$$P_{DL,con} = (I_{DL,av,n} I_o) V_{F,DL} \quad (3.36)$$

Where, *DB* means Boost diode and *DL* means line frequency diode, $V_{F,DB}$ and $V_{F,DL}$ are the forward voltages of Boost diodes and line frequency diodes.

3.2.4.2 Inductance Optimization vs. Semiconductor Losses

Fig.3.6 displays the semiconductor losses ratio (including conduction and switching losses) in function of the output power and Boost inductance when the input voltage is $220V_{ac}$ and output voltage is $390V$. From Fig.3.6, it can be seen:

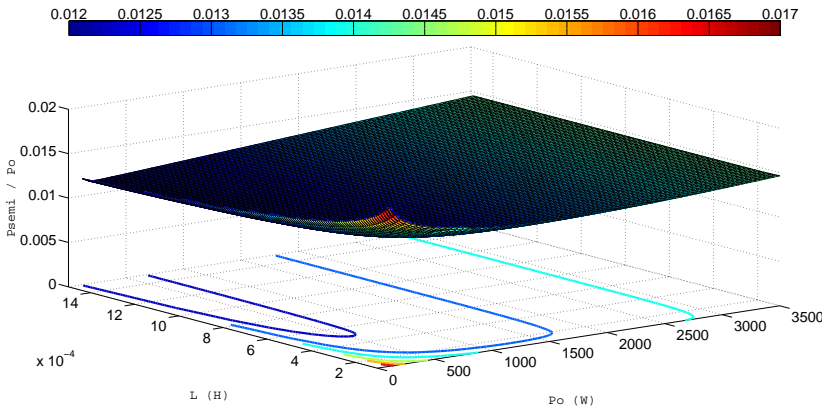


Figure 3.6: Semiconductor Losses Ratio vs. Boost Inductance and Output Power

- For constant output power, considering the Boost inductance starts to increase from CCM limitation value L_{min} . At the beginning, semiconductor losses ratio reduces significantly, while the Boost inductance increases. However, as soon as the Boost inductance reaches the value around 0.6mH, the losses ratio reduction vs. Boost inductance is not evident any more. That means: it is not necessary to use a very large Boost inductor to reduce the semiconductor losses and improve system efficiency in Two-Boost-Circuit BPFC.
- If the BPFC operates in variable output power, take the audio application as an example, there will be a best region for Boost inductance with relatively low and stable semiconductor losses ratio and higher power density.

As what has been shown in Fig.3.6, the inductance from 0.2mH to 0.6mH should be the best suitable region from 300W up to 3.2kW application. This optimized inductance range will do benefit to reduce magnetic volume, which will be shown in the next section.

3.2.5 Efficiency and Volume Optimization

Boost inductors occupies the majority of the volume in BPFC converters. In order to make a compact BPFC converter, the inductor design should be paid high attention. Besides, the power losses in the inductors are function of inductors' volumes as well. In optimization loop 2, a useful compromise between size and efficiency of a Boost inductor can be achieved.

3.2.5.1 Cores Selection

The inductor losses come from core losses and winding losses. In order to predict the total inductor losses, the first step is choosing the core. A suitable core for Boost inductor must have high flux saturate limitation, low core losses and acceptable price. On the magnetic manufacturers' website, there will be very specific information about each core's shape and its material. In this work, the author chose the Kool Mu E cores because of their advantages of high saturation level, relatively low core losses and cheaper price [36]. And all the details of every Kool Mu E core are defined as the initial values at the beginning of the optimization procedure.

3.2.5.2 Winding Losses

Considering the winding losses, the DC losses part usually keeps constant in fixed power level when the type and length of the winding is given; however the AC losses is more complex due to the skin and proximity effects. In this design, copper foil is used in order to decrease the proximity effect. Eqs. (3.37) - (3.40) give the functions of winding losses, switching frequency, layers and copper foil thickness [37]. Where, h is the thickness of copper foil, δ is skin depth, and φ is the ratio between copper thickness and skin depth.

$$P_W = \varphi \left[G_1(\varphi) + \frac{2}{3}(M^2 - 1)[G_1(\varphi) - 2G_2(\varphi)] \right] \times P_{dc} \quad (3.37)$$

$$\varphi = \frac{h}{\delta} = \frac{h\sqrt{f_s}}{7.5} \quad (3.38)$$

$$G_1(\varphi) = \frac{\sinh(2\varphi) + \sin(2\varphi)}{\cosh(2\varphi) - \cos(2\varphi)} \quad (3.39)$$

$$G_2(\varphi) = \frac{\sinh(\varphi)\cos(\varphi) + \cosh(\varphi)\sin(\varphi)}{\cosh(2\varphi) - \cos(2\varphi)} \quad (3.40)$$

According to the equations above, Fig.3.7 shows the increase of layer copper losses producing by proximity effect vs. φ and MMF force ratio m . It can be found in Fig.3.7, with the factor φ and layer m increasing, the AC losses increase significantly.

Assuming the switching frequency is 65kHz, and all the simulations are under the same condition: 220V_{ac} input and 390V output on 3.2kW. Because the trend of winding losses' increase independents on the core size, in Fig. 3.8, the inductor winding losses vs. thickness of copper foil and inductance are given using Kool Mu E core 5528E090 from *Magnetics*®. It can be found that at the same inductance, when the copper foil's thicknesses increase, the total winding losses reduce due to DC winding losses reduction. But the maximum inductance which can be wound on the core decreases as well. However the inductance dropping will not enhance the semiconductor losses ratio as long as carefully choosing the suitable inductance according to what has been mentioned in previous section. Therefore, h varies from 0.1mm to 0.15mm could be a good range for copper foil selection in order to gain low winding losses.

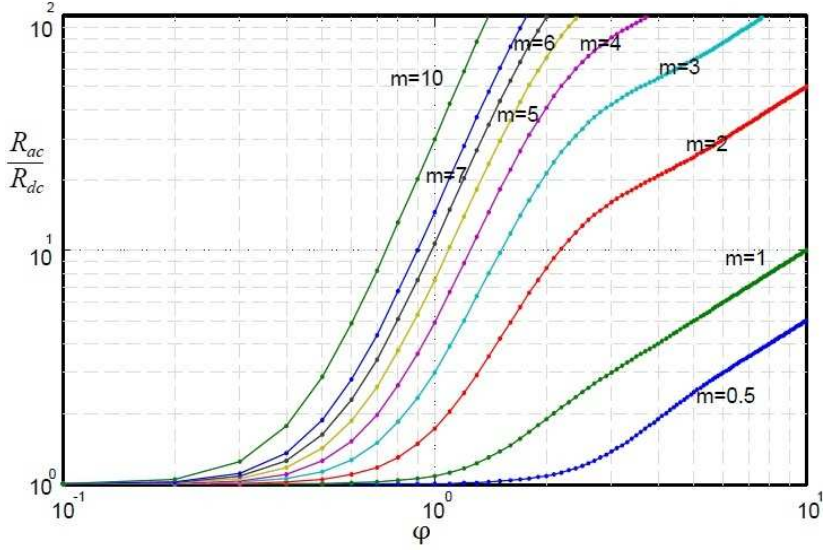


Figure 3.7: Increase of layer copper losses proximity effect as a factor φ and MMF force ratio m [37]

3.2.5.3 Core Losses

Eq.(3.41) gives the function of core losses, flux density, switching frequency and the volume of the Kool Mu cores [38].

$$P_{core} = K_H f_s^\beta B_{av}^\alpha V_e \quad (3.41)$$

Where K_H , α and β are constant parameters, which are determined by the material of the core. V_e is the volume of the core. B_{av} is the average flux density in the core during half line period. It can be calculated as below:

$$B_{av} = \frac{1}{N'} \sum_{n=1}^{N'} \frac{v_L(n)d(n)}{2MA_e f_s} \quad (3.42)$$

Where the $v_L(n)$, $d(n)$ are the instant value of inductor voltage and switch duty circle at each switching cycle. M is the number of turns of the inductor and A_e is cross section of the core. N' is the number of switching cycles in a half line cycle, which is the greatest integer of $\frac{f_s}{2f_L}$.

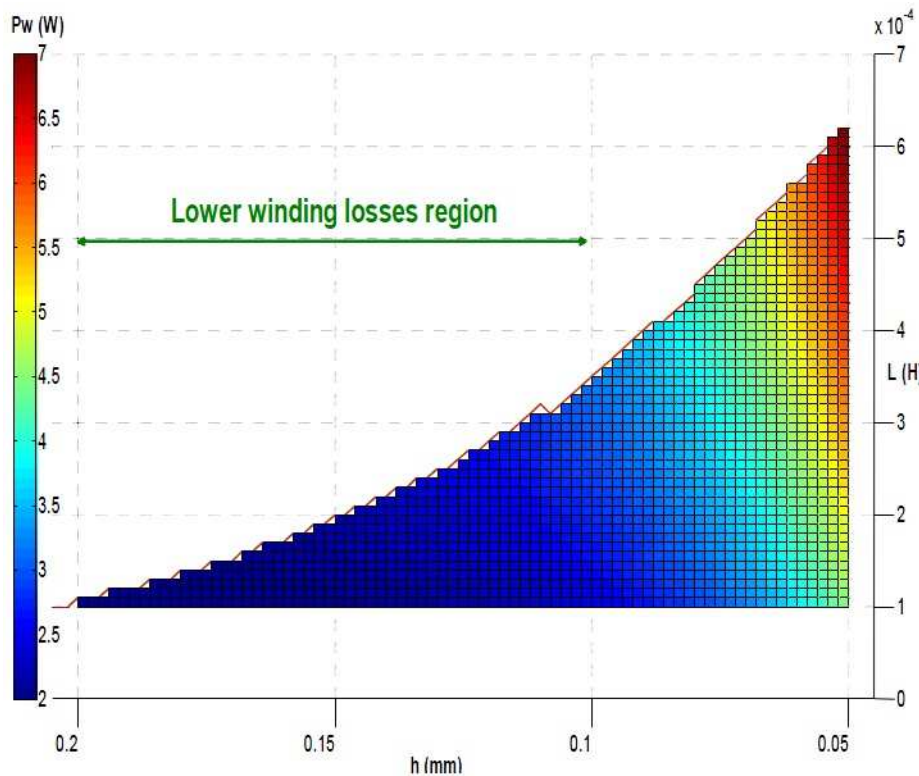


Figure 3.8: Inductor Winding Losses vs. Thickness of Copper Foil and Inductance. The core is Kool Mu E core 5528E90 from *Magnetics*[®]

Core Type	Volume ^a	A ^b	B ^b	C ^b	D ^b	F ^b	L ^b	M ^b
00K5528E090	43100	54.86	27.56	20.62	18.50	16.76	8.38	10.29
00K7228E060	50300	72.39	27.94	19.05	17.75	19.05	9.52	16.89
00K5530E090	51400	54.86	27.56	24.61	18.50	16.76	8.38	10.29
00K8020E040	72100	80.01	38.10	19.81	28.02	19.81	9.91	19.81
00K8020E060	72100	80.01	38.10	19.81	28.02	19.81	9.91	19.81
00K6527E060	79400	65.15	32.50	27.00	22.20	19.65	10.0	12.1
00K8044E026	80912	80.01	44.58	19.81	34.36	19.81	9.91	19.81
00K160LE026	212000	160.0	38.1	39.62	28.1	19.81	9.9	59.28
00K130LE026	237000	130.3	32.51	53.85	22.2	19.81	10.0	44.2

^a Unit: mm^3

^b Unit: mm, parameters describe the dimensions of the cores, the meanings can be found in the datasheet [34]

Table 3.1: Dimensions of The Kool Mu E Cores from *Magnetics*[®]

From Eqs.(3.41) and (3.42), Fig.3.9 shows the core losses vs. Boost inductance for all the qualified Kool Mu E cores from *Magnetics*[®]. In the legend on the right side, the cores were ranked by size, the topper the smaller. The volume of the cores are listed in table 3.1. According to this figure, it is clear that when the inductance increases, the core losses decrease due to the increasing of turns.

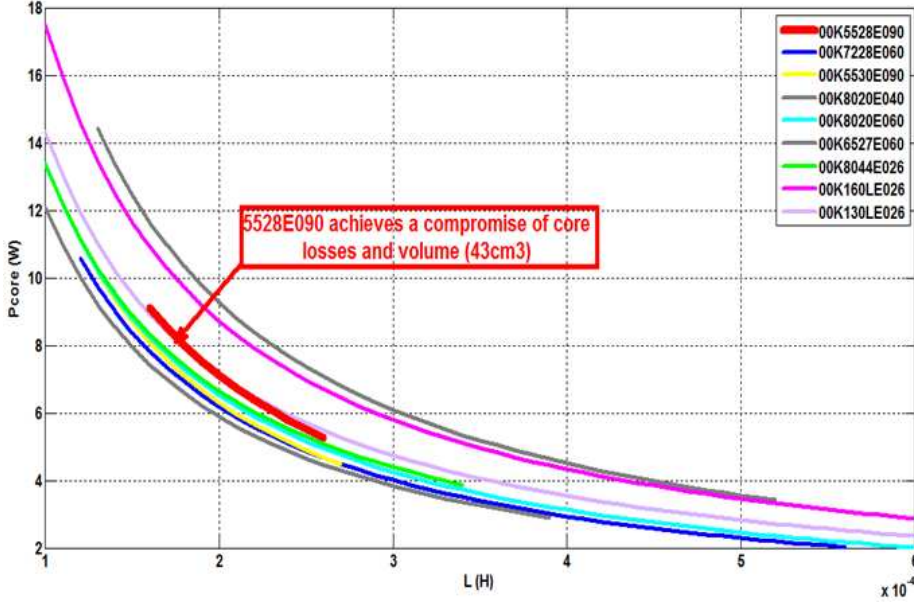


Figure 3.9: Core Losses vs. Boost Inductance for All Qualified Kool Mu E cores from *Magnetics*[®]

Fig.3.10 shows the total Boost inductor losses vs. inductance for different qualified Kool Mu E cores (see table 3.1) from *Magnetics*[®] when h equals to 0.13mm. From Fig.3.10, comes the conclusion that:

- At a certain power level, the Boost inductor losses have its minimal value when the inductance changes.
- The minimal inductor losses are different depending on cores. However, the relationship is not exactly the same as: the bigger the core, the lower the losses. It depends on several factors. Such as geometry of core, permeability, DC bias performance and temperature rising. For example, core 5528E090 (51.4cm³) is smaller than 8020E060 (72.1cm³), but its inductor losses are lower due to its higher permeability.

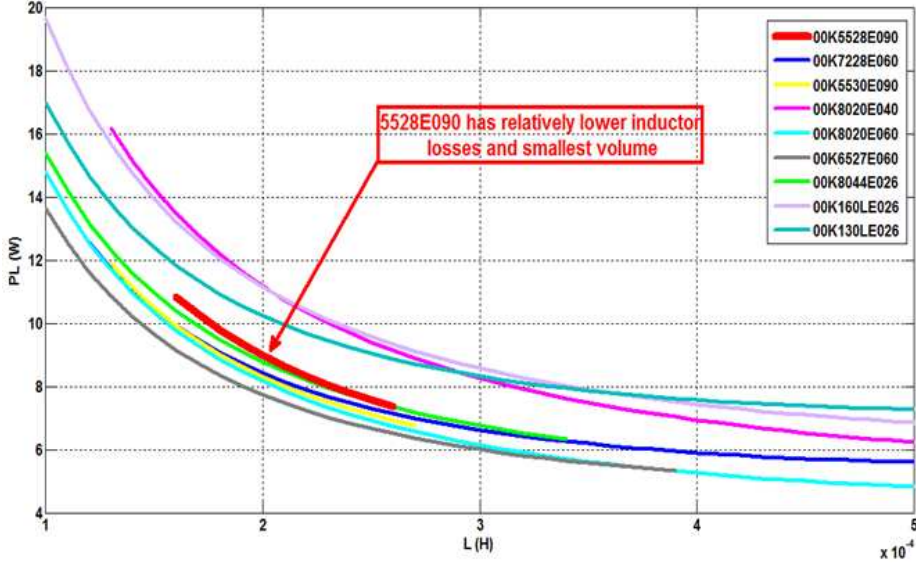


Figure 3.10: Total inductor losses vs. Boost inductance for different qualified Kool Mu E cores from *Magnetics*[®] when $h=0.13\text{mm}$

It should be noticed that in Fig. 3.10, the total inductor losses drop with the inductance increasing. This is due to in the range of inductance from 0.1mH to 0.5mH , the core losses dominate the total inductor losses. So, when the inductance increases, the core losses reduce because of the higher number of turns. If the inductance keeps on increasing, the winding losses will increase. Finally, the winding losses will dominate the total losses, and then, the inductor losses will start to increase.

According to section 3.2.4 and 3.2.5, the expectable Boost inductor parameters for the Two-Boost-Circuit BPFC in Fig.3.1 at 3.2kW and $220V_{ac}$ input can be: $L=0.23\text{mH}$, the copper foil is 0.13mm , using Kool Mu E core 5528E090 (volume is 43.1cm^3) for high efficiency and power density application.

3.3 Experiment Results from a 3.2kW Bridgeless PFC

Efficiency comparison of the simulations based on the optimization design procedure and the measurement results of the proposed Two-Boost-Circuit BPFC

system is given in Fig.3.11. It output power range is from 300W to 3.2kW. Fig.3.12 gives the measured input voltage and current waveforms of this BPFC at 3.2kW and 220V_{ac}.

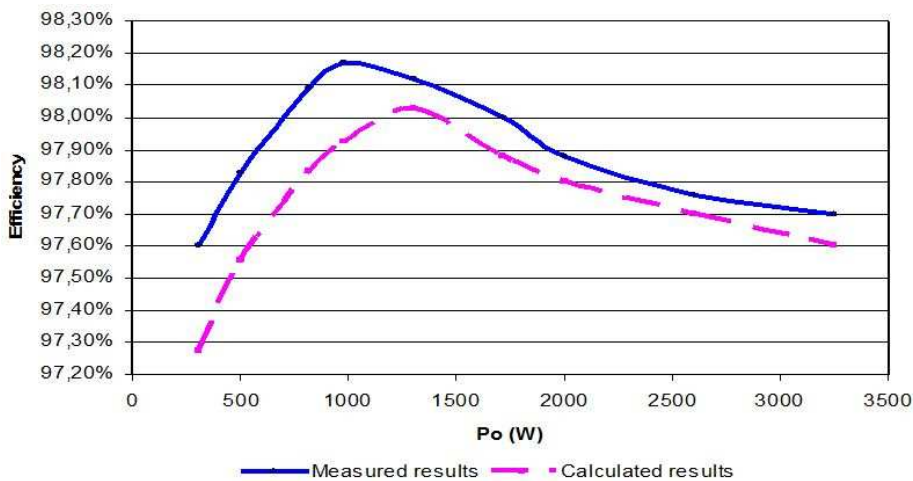


Figure 3.11: Efficiency comparison of Two-Boost-Circuit BPFC at 220V_{ac} input and 390V output using core 5528E090

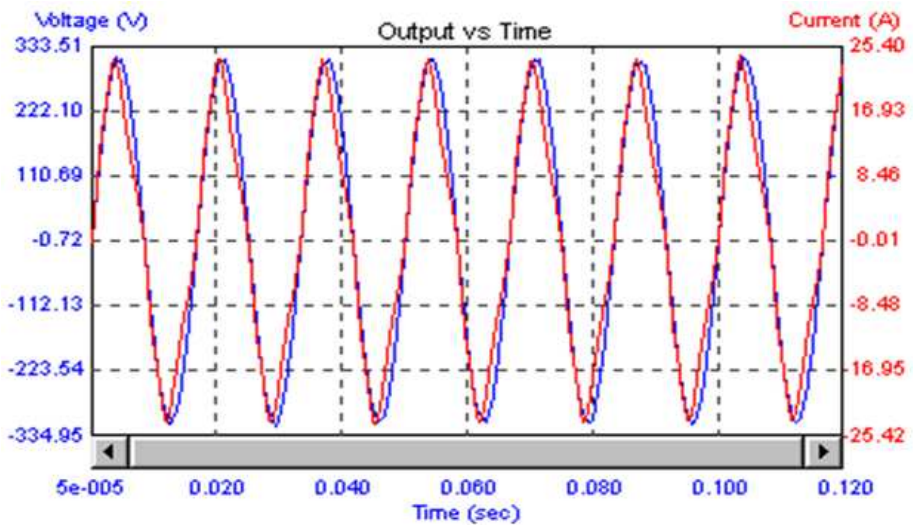


Figure 3.12: Input voltage and current waveforms from Two-Boost-Circuit at 220V_{ac} input and 390V output using core 5528E090

According to Fig.3.11 and 3.12, it can be concluded that the calculated values from the optimization design procedure predict the performances of the Two-Boost-Circuit BPFC correctly and give an optimized design of the Boost inductor.

3.4 Conclusions on the Design of High Efficient Boost Inductors

According to the discussions in this Chapter, the key point for high efficiency and high power density BPFC design is the Boost inductor optimization. In order to achieve as high efficiency as possible, the Boost inductance should be selected carefully based on the BPFC's power level and semiconductor losses. Furthermore, there should be a best value for boost inductance at a constant power. Additionally, it is not necessary to use very large inductance to reduce semiconductor losses.

In conclusion, in order to best compromise the inductor losses and its volume for the high power Two-Boost-Circuit BPFC system, the proposed optimization procedure is a useful method for implementation.

CHAPTER 4

EMI Analysis and Suppression

Working as an electronic pollution eliminator, the PFC's own Electromagnetic Interference (EMI) problems have been blocking its performance improvement for long. In this Chapter, a systematic research on the generation of EMI in the selected Two-Boost-Circuit Bridgeless PFC in Chapter 3 is presented. And two cost-efficient methods for EMI reduction are discussed. Furthermore, a novel BPFC topology is proposed for EMI improvement.

4.1 EMI Modelling

To better explain how exactly the EMI generating from the Two-Boost-Circuit BPFC, this section starts from analyzing and modelling the common mode (CM) and differential mode (DM) noises of this BPFC firstly. Because it is well known that the real EMI performances typically depend strongly on the circuit layout, semiconductor characteristics, gate drivers, operating currents, voltages and temperature and parasitic elements, the actual EMI performances above 1MHz are very difficult to simulate. In order to avoid to push the research into unlimited complexity, in this section, only the noises frequency below 1MHz are taken into consideration. Besides, the model of EMI receiver is not considered at this section neither.

Start from DM noise modelling, the basic key steps are given in Fig.4.1.

- Using the symmetrical operation structure to simplify the topology. As the discussions in previous Chapters, due to the converter operates symmetrically, only the positive AC line period needs to be considered. In the negative AC line period, the operation principles are the same.
- Because the output filter capacitor can be considered as a short circuit in high frequency, and the return diode D_3 is always conducted in the positive AC line period, these two components can be simplified.
- Simplify the MOS, Boost diode and the Boost inductor. In high frequency domain, the Boost inductors charge and discharge through MOS S_1 and Boost diodes D_1 , therefore, it can be considered as a triangle current source.

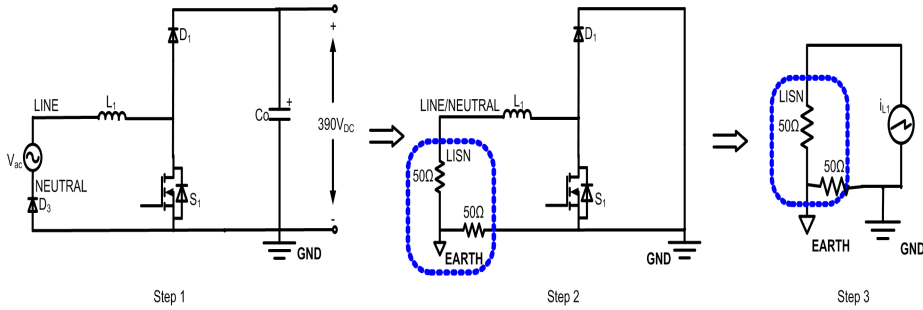


Figure 4.1: DM EMI Modeling Process of the Two-Boost-Circuit BPFC

Following the same modelling concept above, the CM model of the BPFC is shown in Fig.4.2. Where the capacitor C_{s1} is the sum of the parasitic capacitors between the MOS to the earth, which offers a high frequency noise current loop from BPFC to the AC mains. Through Fig.4.1 and Fig.4.2, it can be concluded that for the proposed BPFC in Chapter 3, its DM and CM model are equivalent to a triangle current source and a pulse voltage source respectively.

4.2 EMI Suppression

With the increasing demands on environment-friendly power electronics, research and development on EMI reduction are attracting more and more attentions. During the last decades of years, plenty of researchers presented their

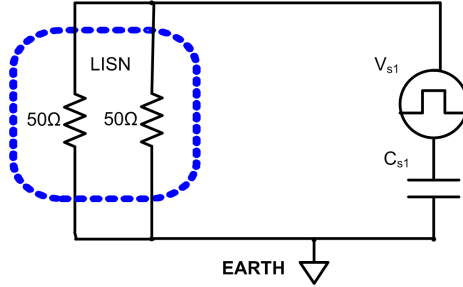


Figure 4.2: CM EMI Modelling of the Two-Boost-Circuit BPFC

contributions in EMI and EMC field [39–58]. Generally speaking, the previous studies on EMI suppression can be classified into two types: suppressing EMI from the noise source and blocking the conducting loop of EMI. In the following sections, the author offers two methods to reduce the EMI of the traditional Two-Boost-Circuit BPFC from noise sources inside the converter. Both of the proposed methods are analyzed in details and approved by experimental verifications.

4.2.1 EMI Reduction Using Interleaving Technique

With the increasing requirement of high power application, instead of simply paralleling several BPFCs together, interleaved BPFC (IBPFC) is investigated in this Section. The publications [A3] and [A5] related to this work give the optimal design of a high efficient 2-stage IBPFC in Fig.4.3. This novel topology can be expected to have better EMI performance comparing to the non-interleaved BPFC due to the inner EMI cancellations caused by phase shift.

Taking the general multi-stage IBPFC in Fig.4.4 as an example, the detailed analysis on how can the interleaved stages help EMI cancellation in IBPFC systems is presented in the rest of this section.

4.2.2 Multi-Interleaved Stages and EMI Cancellations

Similarly, because the N-stage IBPFC in Fig.4.4 works symmetrically, only the positive AC period is considered here. In the positive half line period, Boost inductors $L_{1,i}$, MOSs $S_{1,i}$ and Boost diodes $D_{1,i}$ work interleaved with D_6 returning current to AC source. Where, i symbolized the number of interleaved stages ranging from 1 to N. One of the major reasons for using IBPFC is EMI

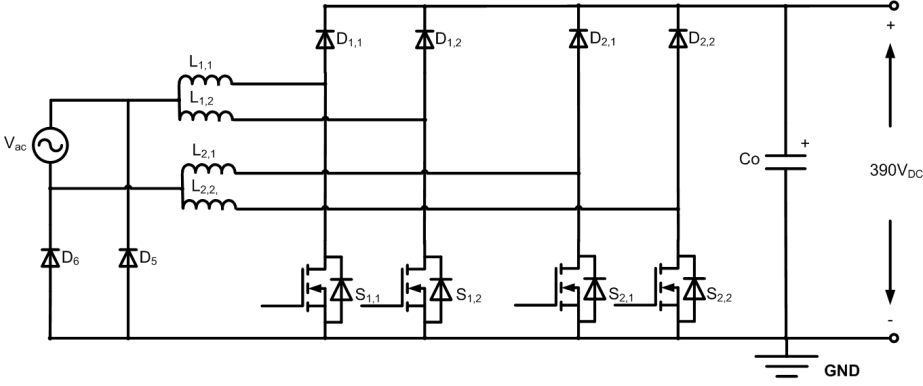


Figure 4.3: Proposed novel 2-stage Two-Boost-Circuit IBPFC

cancellation. However, since the BPFC converter has variable on duty ratios, the input ripple current can not cancel completely all the time. To give the insight on the relationship between number of interleaved stages and EMI cancellations, the DM and CM EMI modelling of the multi-stage IBPFC system in Fig.4.4 can be achieved by generalized the DM and CM EMI models (Figs.4.1 and 4.2) from the normal BPFC in Chapter 3.1, due to the multi-stage IBPFC system is an extended version from the traditional BPFC.

The EMI models of the multi-stage IBPFC can be drawn in Fig.4.5. All of the DM (CM) noise sources are $360^\circ/N$ phase shift. Where, N is the number of multi-stage interleaved modules. The normal non-interleaved BPFC has an N equals to 1. To predict the internal affect from each noise source and give a numerical explanation on the complete system, the mathematical derivation of the CM and DM noise sources in Fig.4.5 are as followed.

Assuming the n th order CM and DM noise of the first interleaving stage are defined as:

$$V_{CM,1}(n\omega_0) = A_n e^{j\varphi_n} \quad (4.1)$$

$$V_{DM,1}(n\omega_0) = \frac{B_n}{N} e^{j\Phi_n} \quad (4.2)$$

Where, the ω_0 is the fundamental angular frequency, A_n and B_n are the CM and DM harmonics' amplitudes of non-interleaved BPFC, and φ_n and Φ_n are the initial phases of the n th harmonics. Therefore, the n th order CM and DM

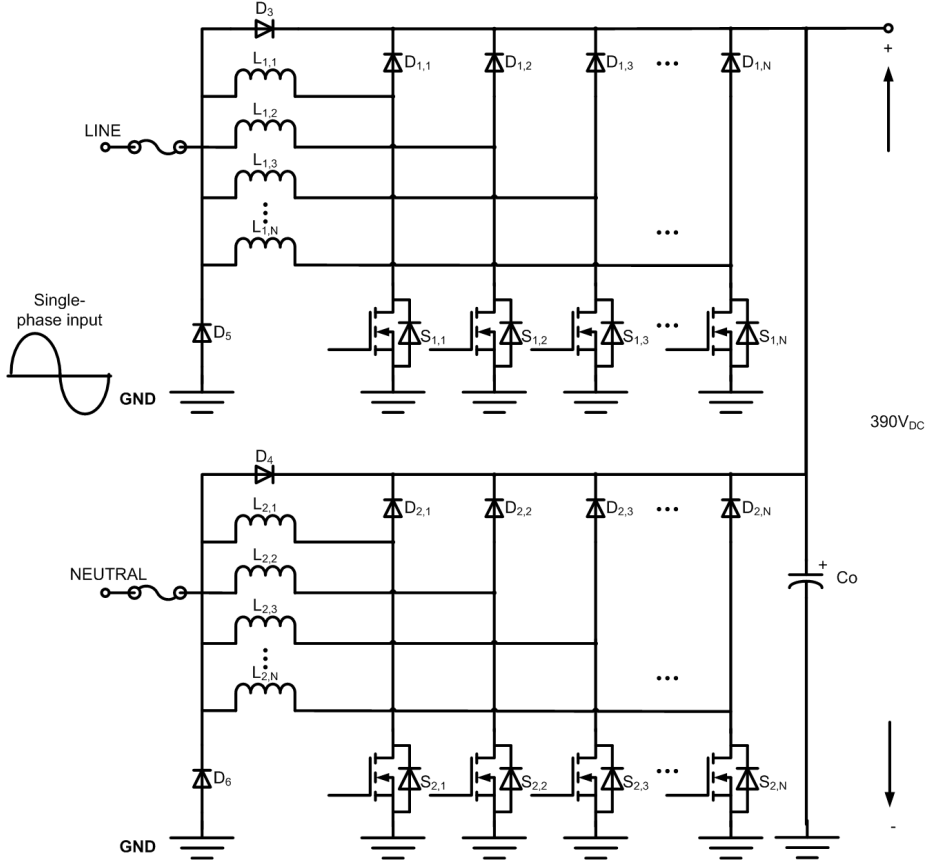


Figure 4.4: Possible architecture of multi-stage IBPFC system

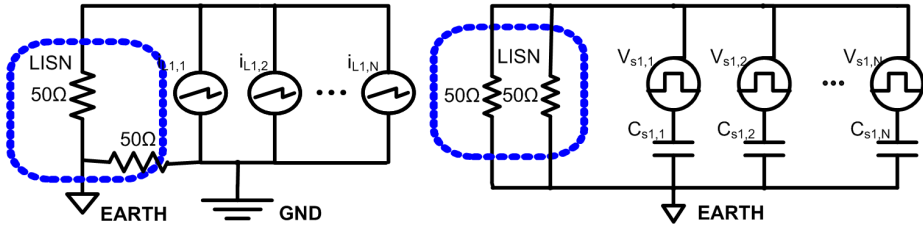


Figure 4.5: DM (left) and CM (right) EMI modeling of the N-stage Two-Boost-Circuit IBPFC

noise sources of the Nth interleaving stage are:

$$V_{CM,N}(n\omega_0) = A_n e^{j\varphi_n} \frac{2\pi n(N-1)}{N}$$

$$V_{DM,N}(n\omega_0) = \frac{B_n}{N} e^{j\Phi_n} \frac{2\pi n(N-1)}{N} \quad (4.3)$$

According to the superposition principle [59], the sum of the n th order CM (DM) noises from the N -stage IBPFC can be expressed as

$$\begin{aligned} V_{CM,tot}(n\omega_0) &= \frac{1}{N} \sum_{i=1}^N V_{CM,i}(n\omega_0) \\ &= \frac{A_n}{N} \left[\sum_{k=1}^N \cos\left(\Phi_n - \frac{2\pi n(k-1)}{N}\right) + j \sum_{k=1}^N \sin\left(\Phi_n - \frac{2\pi n(k-1)}{N}\right) \right] \end{aligned} \quad (4.4)$$

$$\begin{aligned} I_{DM,tot}(n\omega_0) &= \sum_{i=1}^N I_{DM,i}(n\omega_0) \\ &= \frac{B_n}{N} \left[\sum_{k=1}^N \cos\left(\varphi_n - \frac{2\pi n(k-1)}{N}\right) + j \sum_{k=1}^N \sin\left(\varphi_n - \frac{2\pi n(k-1)}{N}\right) \right] \end{aligned} \quad (4.5)$$

Assuming $\varphi_n = \Phi_n = 0$, Eqs 4.4 and eqs 4.5 can be simplified as:

$$V_{CM,tot}(n\omega_0) = \frac{A_n}{N} \left[\sum_{k=1}^N \cos\left(\frac{2\pi n(k-1)}{N}\right) - j \sum_{k=1}^N \sin\left(\frac{2\pi n(k-1)}{N}\right) \right] \quad (4.6)$$

$$I_{DM,tot}(n\omega_0) = \frac{B_n}{N} \left[\sum_{k=1}^N \cos\left(\frac{2\pi n(k-1)}{N}\right) - j \sum_{k=1}^N \sin\left(\frac{2\pi n(k-1)}{N}\right) \right] \quad (4.7)$$

From Eqs (4.1) and (4.6), the amplitude ratio of n th order CM noise of the N -stage interleaved and non-interleaved BPFC is:

$$\begin{aligned} \alpha(n\omega_0) &= \left| \frac{V_{CM,tot}(n\omega_0)}{V_{CM,non}(n\omega_0)} \right| \\ &= \frac{1}{N} \left| \sum_{k=1}^N \cos\left(\frac{2\pi n(k-1)}{N}\right) - j \sum_{k=1}^N \sin\left(\frac{2\pi n(k-1)}{N}\right) \right| \end{aligned} \quad (4.8)$$

Similarly, from Eqs (4.2) and (4.7), the amplitude ratio of n th order DM noise of the N -stage interleaved and non-interleaved BPFC is:

$$\begin{aligned} \beta(n\omega_0) &= \left| \frac{I_{DM,tot}(n\omega_0)}{I_{DM,non}(n\omega_0)} \right| \\ &= \frac{1}{N} \left| \sum_{k=1}^N \cos\left(\frac{2\pi n(k-1)}{N}\right) - j \sum_{k=1}^N \sin\left(\frac{2\pi n(k-1)}{N}\right) \right| \end{aligned} \quad (4.9)$$

Where, $V_{CM,tot}(n\omega_0)$ and $V_{DM,tot}(n\omega_0)$ are the n th order CM and DM harmonics of the N -stage IBPFC; $V_{CM,non}(n\omega_0)$ and $V_{DM,non}(n\omega_0)$ are the n th order CM and DM harmonics of non-interleaved BPFC.

By using the Orthogonality principle [60]

$$\begin{aligned}\alpha(n\omega_0) &= \beta(n\omega_0) = 0, n \neq c \cdot N \\ \alpha(n\omega_0) &= \beta(n\omega_0) = 1, n = c \cdot N\end{aligned}\quad (4.10)$$

Where c is the positive integer serials starting from 1.

Hence, the amplitudes of high switching frequency noises from both CM and DM sources in the N -stage IBPFC can be solved as below:

$$\begin{aligned}|V_{CM,tot}(n\omega_0)| &= 0, n \neq c \cdot N \\ |V_{CM,tot}(n\omega_0)| &= |V_{CM,non}(n\omega_0)|, n = c \cdot N\end{aligned}\quad (4.11)$$

$$\begin{aligned}|I_{DM,tot}(n\omega_0)| &= 0, n \neq c \cdot N \\ |I_{DM,tot}(n\omega_0)| &= |I_{DM,non}(n\omega_0)|, n = c \cdot N\end{aligned}\quad (4.12)$$

From Eqs. (4.11) and (4.12), it can be concluded that:

- Interleaved stages help to improve both CM and DM EMI.
- In an N -stage IBPFC, except the $c \cdot N$ times fundamental frequencies, all the rest harmonics can be reduced due to the phase shift.
- The more interleaved stages the IBPFC has, the more high frequency harmonics will be reduced.
- The switching frequency f_s affects the design of the EMI filter of IBPFC due to the noises cancellation do NOT happen at $c \cdot N$ times fundamental frequencies.

In order to maintain the EMI advantage of IBPFC, it is better to select its switching frequency based on the range of conduction EMI standard. Implementing the European Standard EN55013 as an example, the disturbance voltages at mains terminals in the frequency range from 150kHz to 30MHz need to be attenuated to fulfil the EMI limitation [61]. Therefore, the first harmonic of the IBPFC, which locates inside the range of the conducted EMI standard should be better NOT to equal to $c \times N$ times of fundamental frequencies. The mathematic expression is:

$$\lceil \frac{150kHz}{f_s} \rceil \neq c \cdot N \quad (4.13)$$

Where f_s is the switching frequency, and $\lceil x \rceil$ is a ceiling function, which returns the smallest integer not less than x . From Eq. (4.13) it can also be found that the IBPFCs usually allow higher cut-off frequency of the EMI filter comparing to the non-interleaved one with the same EMI attenuations when f_s is higher than 150kHz.

Fig.4.6 shows the simulations of DM and CM EMI comparison between a 2-stage interleaved and a non-interleaved Two-Boost-Circuit BPFC, when the switching frequency f_s was chosen improperly at 75kHz. Because the 2nd harmonic (150kHz) is the first harmonic which locates inside the frequency range of EMI limitation, and it cannot be cancelled by interleaved stages. (150kHz equals to the $c \times N$, when c is 1.) Therefore, the same as Eq. (4.13) has proved, the cut-off frequency of the EMI filter in this 2-stage IBPFC requires the same as the non-interleaved BPFC and the EMI reduction advantages of interleaving technique can not display at all.

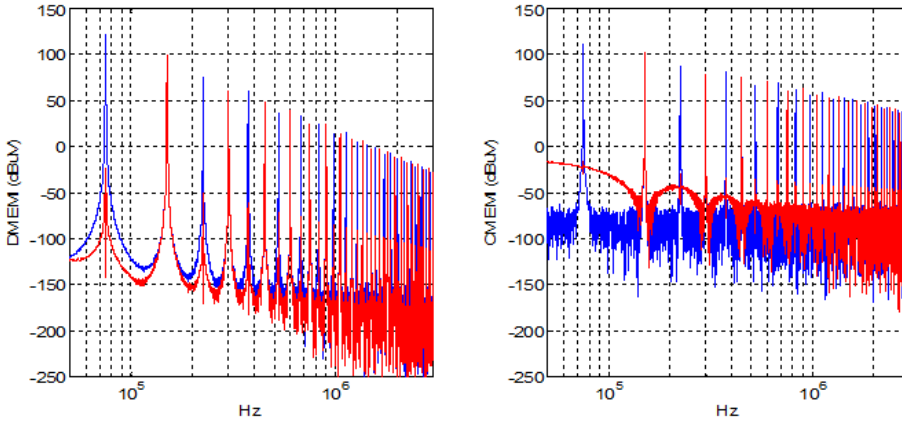


Figure 4.6: DM (right) and CM (left) EMI comparison of 2-stage interleaved (red) and non-interleaved (blue) Two-Boost-Circuit BPFC at 3.5kW with improper switching frequency at 75kHz

4.2.3 Novel High Efficient Interleaved BPFC Converter Design using Multi-Objective Design Optimization Procedure

Since the proposed novel IBPFC topology is an extension version of normal BPFC in Chapter 3 Fig.3.1, comparing to the non-interleaved version, the design process for all the components are the same. Therefore, in this section, the

author would like to focus on the Multi-objective Design Optimization Procedure (MDOP) introduction, which is a useful concept for engineers to optimize the performances of the converters in order to best match their desires.

4.2.3.1 Definition of MDOP

Nowadays, in the development of power electronics systems, the reduction of initial cost and total power losses and the improvement of power density and EMI performance have been of primary concern. However, these important elements conflict with each other sometimes. For instance, low initial cost may come together with low performance magnetic components and high losses semiconductors, which will do harmful to system total losses. And in order to improve EMI performance, extra components often need to be added in the converter, such as EMI filter, which increase the volume and complexity of the system. For meeting the multi-objective requirements in the future power electronics field, reference [62, 63] firstly presented an intended multi-objective improvement of main performance indices of power electronics in a very specific way and give a useful solution to meet both of the efficiency and power density requirements.

Inspired by them, in this section, the author will present her idea for designing an high performance IBPFC system with good compromise of EMI, efficiency, power density and design complexity by using a self-developed MDOP routine. Although the initial cost is very important for industrial applications, it is out of the main scope of this study and will not be included here.

4.2.3.2 The MDOP Design Flow Chart for IBPFC System

Comparing to the non-interleaved BPFC in Chapter 3.1, one main disadvantage of IBPFC system(Fig.4.4) is that it increases the number of magnetic components. By adding one interleaved stage, two extra Boost inductors will be needed. Facing the most important issues in power electronics today - efficiency and power density - the compromise of power density, efficiency and EMI must be taken into consideration together.

The proposed MDOP design procedure consists of three optimization loops (Fig.4.7). Loops 1 and 2 are used to optimize the efficiency and power density of the IBPFC based on Boost inductor optimization. The functions of these two loops are the same as what has been explained in Chapter 3.2.2. The new optimization loop 3 is used to analyze EMI reduction. By combine the three loops together, a balance among EMI reduction, system volume and power density

can be achieved.

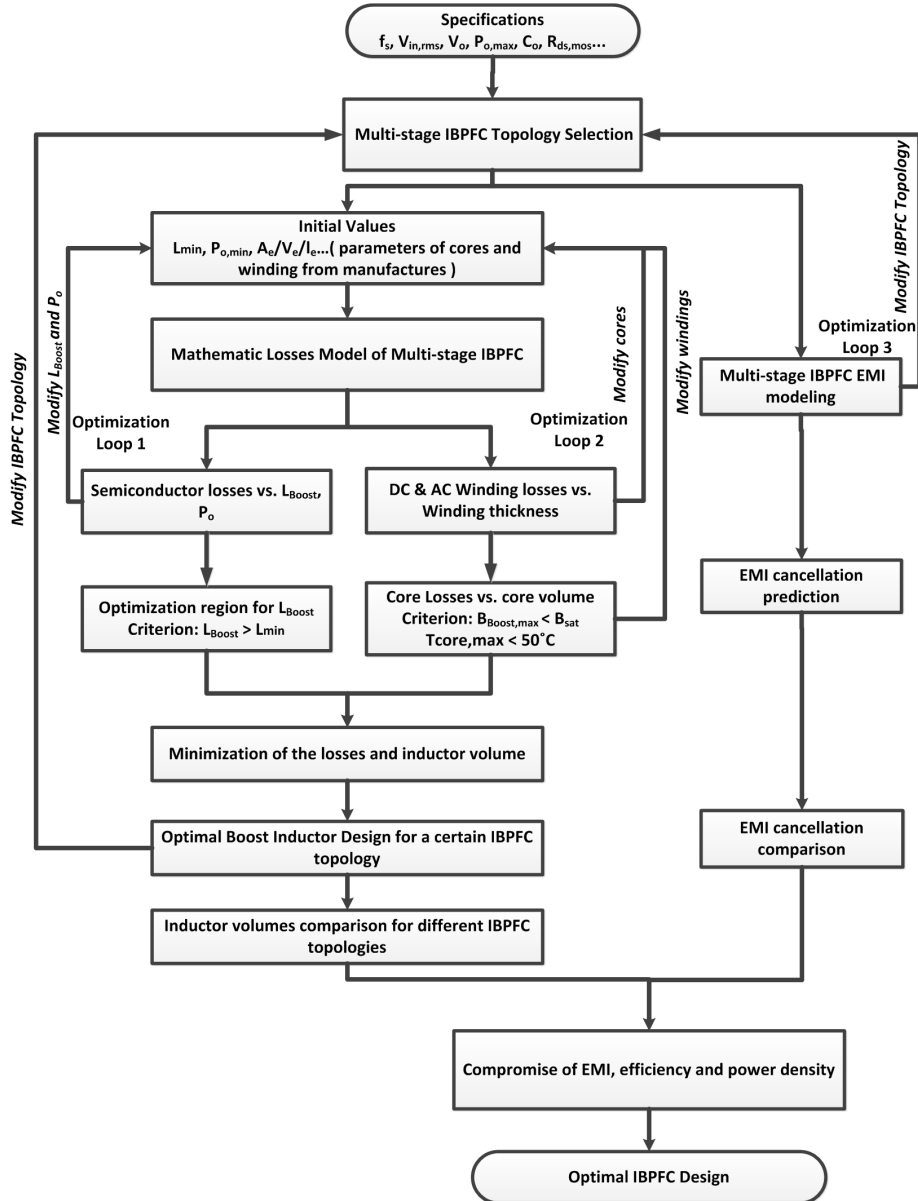


Figure 4.7: The MDOP design flow chart of IBPFC system

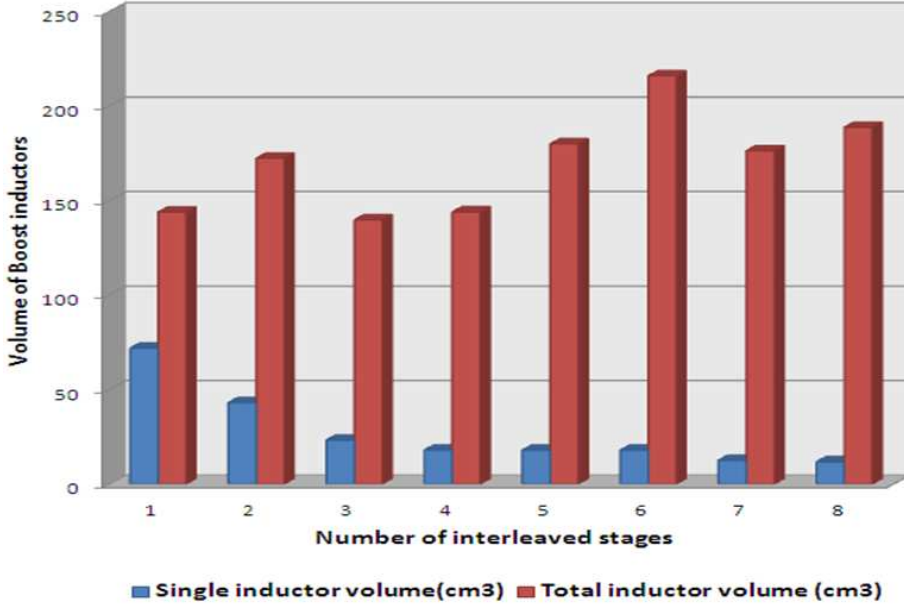


Figure 4.8: Minimal single (blue) and total (red) inductor's volume comparison of interleaved and non-interleaved Two-Boost-Circuit BPFCs

Implementing the optimization in Fig.4.7, Fig.4.8 gives the comparison of the minimal single and total volumes of Boost inductors in interleaved and non-interleaved Two-Boost-Circuit BPFC with a compromise of high efficient and high power density, when the interleaved stage N varying from 2 to 8 at 3.5kW and $85V_{ac}$ input. The same as Chapter 3, in this optimization process, Kool Mu E cores from *Magnetics*[®] were chosen. And, comparing with the traditional round winding, copper foils were selected to reduce the winding losses.

From Fig.4.8, it can be concluded:

1. With the number of interleaved stages increasing, the single Boost inductor's volume reduces significantly.
2. Due to the number of inductors increasing, except the 3-stage interleaved BPFC, the total inductors' volumes of the IBPFC systems are higher than the non-interleaved BPFC with the same inductance.
3. 3-stage and 4-stage IBPFC has lower total inductor volume among all the IBPFCs. However, if comparing these two IBPFC converters, the first one has smaller system volume, and the second one has better EMI.

4. Comparing to 3 or 4 stages IBPFC, the 2-stage IBPFC has slightly higher volume and less harmonics' reductions, but less complexity and shorter development period, which is good to start.

In this work only the 2-stage IBPFC converter is built for testing and verifications.

4.2.4 Experimental Results

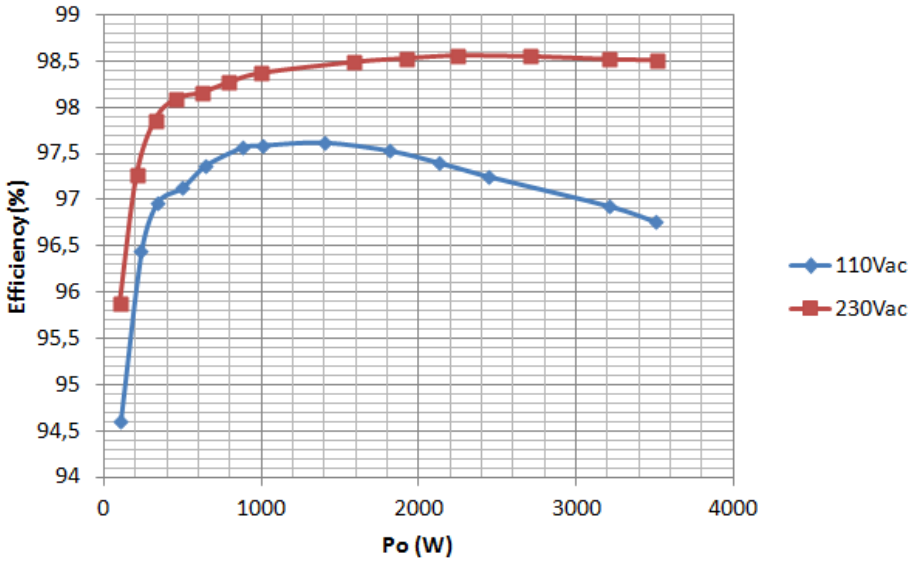


Figure 4.9: Efficiency comparison of 2-stage IBPFC at different input voltages

After carefully design [A3 and A5], a 65kHz 2-stage IBPFC prototype is accomplished. The data of the key components are the same as what have given in 3.2.4.1. Comparison of the system efficiency, which were measured by precise power analyzer PPA5530 from *N4L*[®] at different line voltages, are drawn in Fig.4.9. The system's key components losses distributions at 3.5kW in 110V_{ac} 230V_{ac} input are given in Fig.4.10. Fig.4.11 gives the measured input voltage and current waveforms of the IBPFC at 3.5kW in 110V_{ac} and 230V_{ac} input. And Fig.4.12 shows the thermal measurements of the proposed 2-stage IBPFC system at 3.5kW with 110V_{ac} and 230V_{ac} input respectively.

According to the requirement from audio application, as a PFC front-end for class D amplifiers, it is only necessary to test its input current harmonics and

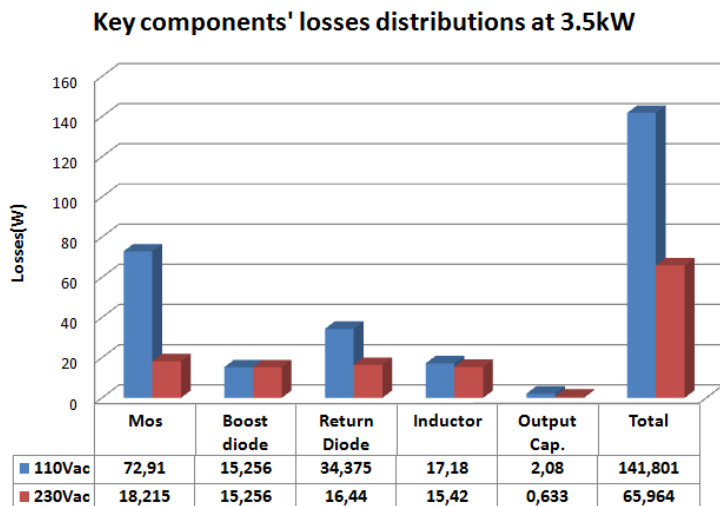


Figure 4.10: Key components' losses distribution at 3.5kW

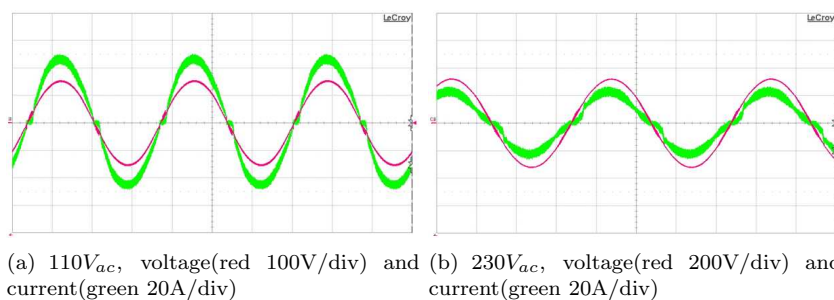
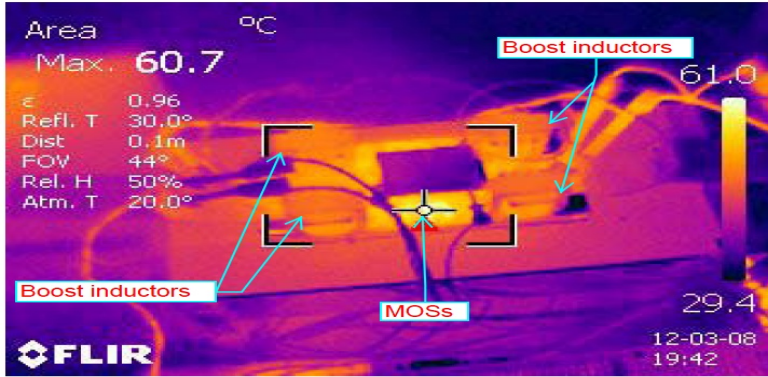
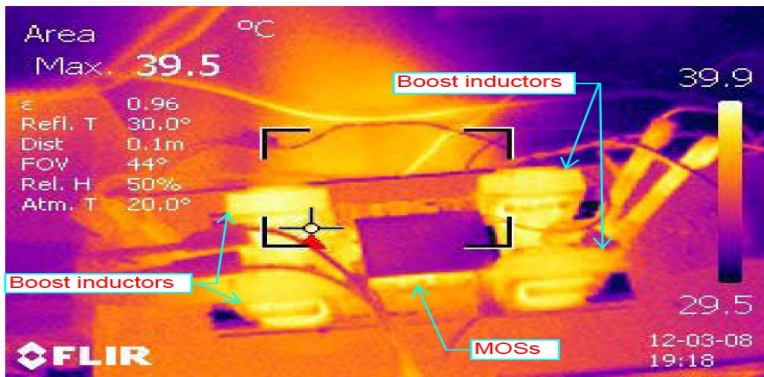


Figure 4.11: Input voltage and current waveforms of 2-stage IBPFC at 3.5kW, PF=99%

EMI performances at average power, which is usually around one over eight of the peak power (around 440W). Therefore, Figs. 4.13 give the conducted EMI comparison of the 2-stage IBPFC and the normal BPFC at 440W in 230Vac input.

From Fig. 4.13, it can be seen that in the 2-stage IBPFC, the odd harmonics can be reduced by phase shift. However, it should be noticed that according to Eqs.(4.11) and (4.12), in the 2-stage IBPFC, the odd harmonics should be completely cancelled. The partial cancellation could be due to the tiny difference between the 2 interleaved Boost inductances, which brings unbalance into the

(a) $110V_{ac}$ at 3.5kW(b) $230V_{ac}$ at 3.5kW**Figure 4.12:** Thermal measurement comparison of the proposed IBPFC system

interleaved stages.

Figs. 4.14 and 4.15 give the input current harmonics measurements of the 2-stage IBPFC and the traditional BPFC at 440W in $230V_{ac}$ and $110V_{ac}$ input separately.

4.3 EMI Reduction Using Frequency Dithering

It is also commonly agreed that the EMI of the switching converters could be improved by using carrier-frequency modulation (CFM) techniques [64, 65]. The

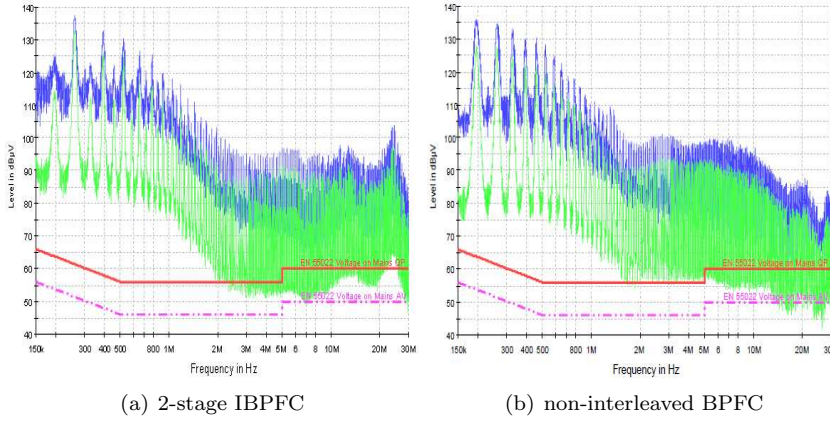


Figure 4.13: EMI comparison at one eighth of full power and 230V_{ac} input without EMI filter

CFM techniques can be classified as periodic CFM (PCFM) and random CFM (RCFM) [66]. In this section, some important characteristics of PCFM regarding to EMI suppression will be discussed. RCFM is out of the scope of this research.

4.3.1 Operation Principles

Considering the PCFM system, that means the switching frequency dithers with a small amplitude variation around a central frequency. Assuming a standard PWM pulse signal $G(t)$ with a duty ratio D and switching frequency f_s . If $G(t)$ has a high level A and a low level 0 , implementing the Fourier series, $G(t)$ can be expressed as:

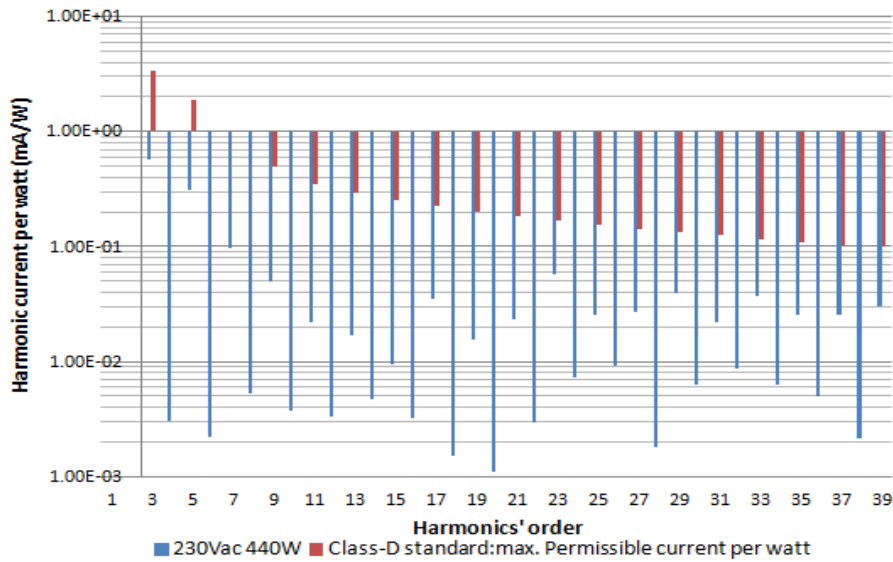
$$G(t) = \sum_{n=-\infty}^{\infty} C_n e^{j\theta n} \quad (4.14)$$

Where, C_n and θn are the n th series coefficients, which contain the magnitude and phase information of the n th harmonic. And C_n and θn can be calculated by:

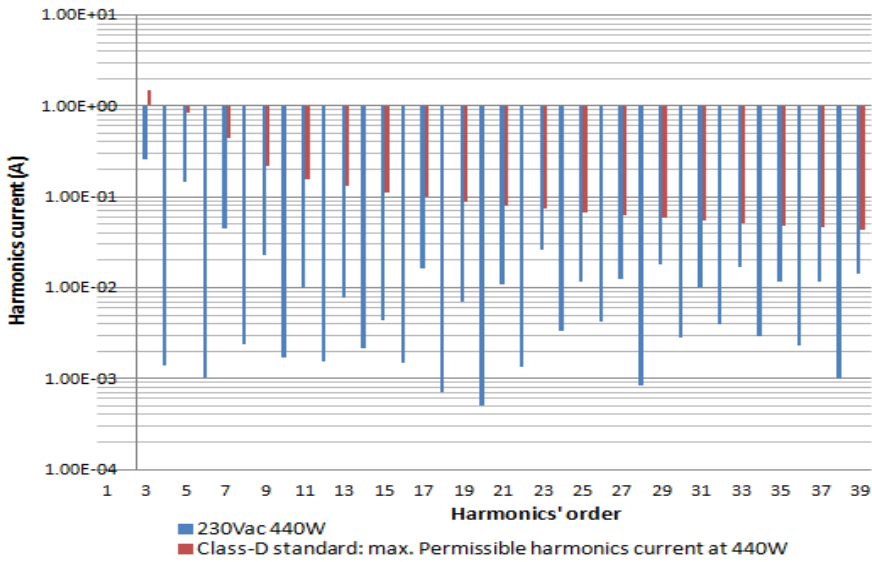
$$C_n = \frac{1}{T} \int_{-T_s/2}^{T_s/2} G(t) e^{-j2\pi f_s n t} dt = \frac{A j}{2\pi n} (e^{-j2\pi n D} - 1) \quad (4.15)$$

$$\theta_n(t) = 2\pi n f_s t \quad (4.16)$$

When the switching frequency is modulated by a co-sinusoidal function with a dithering amplitude δf_s and a dithering rate f_m , the instantaneous frequency



(a) Harmonic Current Per Watt



(b) Harmonic Current

Figure 4.14: Harmonic Current vs Class D Standard

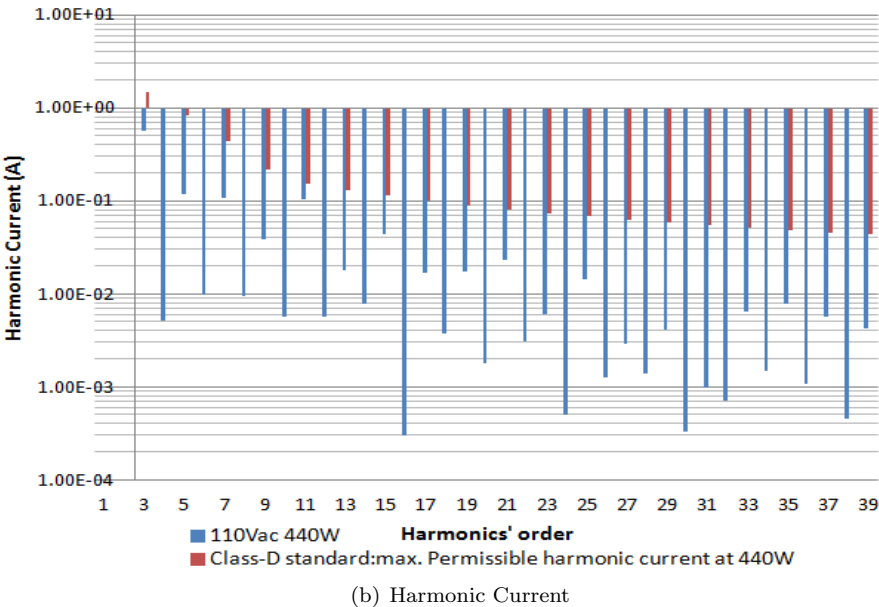
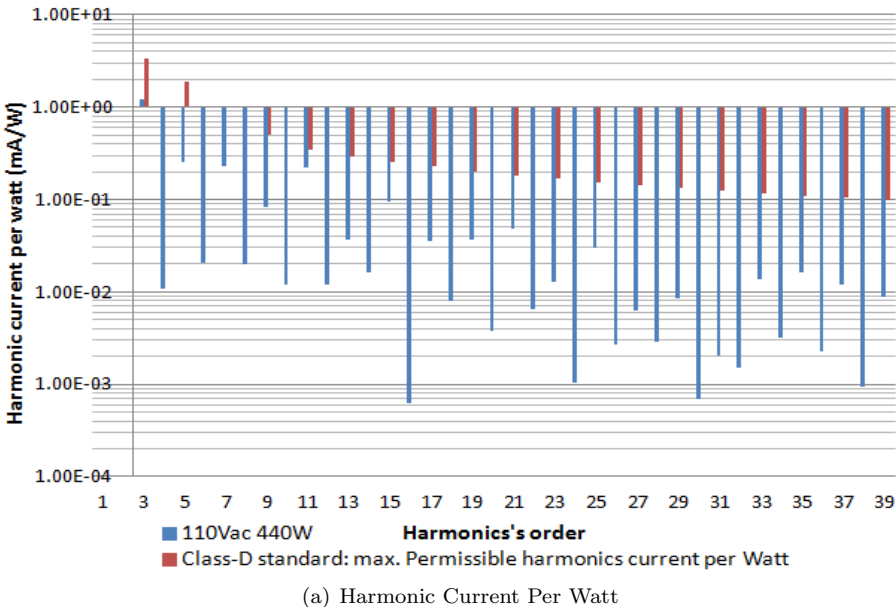


Figure 4.15: Harmonic Current vs Class D Standard

and angular rotation of the dithering PWM signal are:

$$f_{ds}(t) = f_s + \Delta f_s \cos(2\pi f_m t) \quad (4.17)$$

$$\theta_{ds}(t) = 2\pi n \int_0^t f_{ds}(t) dt = 2\pi f_s t + \gamma \sin(2\pi f_m t) \quad (4.18)$$

Where, γ is the dithering factor. It symbolizes the ratio of dithering amplitude and dithering rate. And it is defined as:

$$\gamma = \frac{\Delta f_s}{f_m} \quad (4.19)$$

Similarly as before, by applying the Fourier series, the dithering PWM signal can be expressed as:

$$G_d(t) = \sum_{n=-\infty}^{\infty} C_n e^{j\theta_{ds,n}} = \sum_{n=-\infty}^{\infty} C_n e^{j[\theta_n + \gamma \sin(2\pi f_m t)]} \quad (4.20)$$

With the derivation results from [65], Eq. (4.20) can be rewritten into:

$$\begin{aligned} G_d(t) &= \sum_{n=-\infty}^{\infty} C_n \left\{ \sum_{i=0}^{\infty} J_i(n\gamma) [e^{j(\theta_n + \theta_{m,i})} + (-1)^i e^{j(\theta_n - \theta_{m,i})}] \right\} \\ &= \sum_{n=-\infty}^{\infty} C_n e^{j\theta_n} \left\{ \sum_{i=0}^{\infty} J_i(n\gamma) [e^{j\theta_{m,i}} + (-1)^i e^{-j\theta_{m,i}}] \right\} \end{aligned} \quad (4.21)$$

Where $\theta_{m,i}$ is the phase angular induced by frequency dithering and can be written as:

$$\theta_{m,i}(t) = 2\pi i f_m t \quad (4.22)$$

And $J_i(\cdot)$ is the i th order Bessel function:

$$J_i(n\gamma) = \left(\frac{n\gamma}{2}\right)^i \sum_{j=0}^{\infty} \frac{(-1)^j \cdot \left(\frac{n\gamma}{2}\right)^{2j}}{j! \cdot (j+i)!} \quad (4.23)$$

4.3.2 Advantages and Limitations

Many researchers before have presented that using frequency dithering, it is possible to gain extra EMI reductions [67–77]. However, none of them has ever claimed how to predict these reductions. Besides, there are other researchers they believed that frequency dithering can only change the noise spectrum, if considering the EMI reduction, this technique is not as beneficial as is commonly perceived [78, 79]. Because these two viewpoints are somehow against each other, in order to judge them fairly, both of the positive and negative effects on EMI induced by frequency dithering should be weighed.

4.3.2.1 Advantages of Frequency Dithering

From Eq. (4.21) one can see, the harmonics reduction at multiples of central switching frequency f_s can be predicted by setting i equals to 0. Under this condition, $J_0(\cdot)$ can be written as:

$$J_0(n\gamma) = \sum_{j=0}^{\infty} \frac{(-1)^j \cdot \left(\frac{n\gamma}{2}\right)^{2j}}{(j!)^2} \quad (4.24)$$

Therefore, the absolute value of $J_0(\cdot)$ in Eq. (4.24) shows: comparing to the

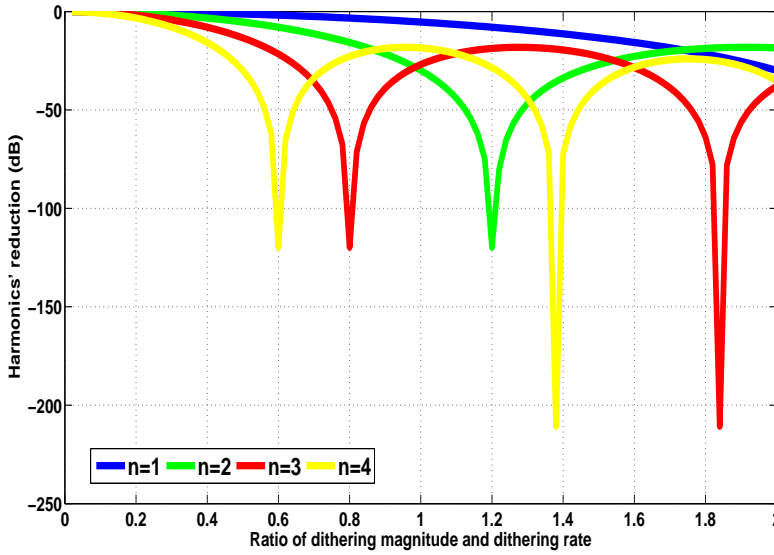


Figure 4.16: Harmonics' reduction vs. dithering factor γ when harmonics' order n changes from 1 to 4

standard PWM in Eq. (4.14), the harmonics reductions at multiples of central switching frequency of dithering PWM in Eq. (4.20). It is easy to see, the harmonics' reduction factor $|J_0(\cdot)|$ is a function of dithering factor γ and the harmonic's order n . The reductions' trends of some low order harmonics versus the dithering factor γ are given in Fig.4.16, when n changes from 1 to 4. From Fig.4.16, one can conclude that:

- Dithering PWM has lower amplitudes at multiples of central switching frequency compared to standard PWM.

- With the same dithering factor, the reductions vary from harmonic to harmonic.
- When the dither factor changes, each harmonic has its maximum reduction point.

4.3.2.2 Limitations of Frequency Dithering

According to reference [67] has proved, the power spectrum of dithering PWM signal in Eq. (4.20) in positive frequency range can be expressed as:

$$\begin{aligned}
 S_d(f, \gamma) &= S(f, \gamma) + \Delta S(f, \gamma) \\
 &= 2 \left| \sum_{n=1}^{\infty} C_n [J_0(n\gamma) \cdot \delta(f - nf_s)] \right|^2 \\
 &\quad + 2 \left| \sum_{n=1}^{\infty} C_n \left\{ \sum_{i=1}^{\infty} J_i(n\gamma) [\delta(f - nf_s - if_m) + (-1)^i \delta(f - nf_s + if_m)] \right\} \right|^2
 \end{aligned} \tag{4.25}$$

Where $S(f, \gamma)$ is the original power spectrum of standard PWM signal and $\Delta S(f, \gamma)$ is the spread spectrum caused by frequency dithering.

The Limitations of Central Harmonics Reductions Through Fig.4.16 and Eq. (4.25), it is not difficult to find out that in the dithering PWM, the central harmonics' reductions are limited by γ . Furthermore, in a fixed γ frequency dithering system, it is more reasonable to expect large harmonics' reductions only happening at certain frequencies not in the whole frequency range.

Spectrums Overlapping and Redistribution According to paper [67], the dithering will also lead upper and lower sidebands at multiples of central switching frequency f_s and the bandwidth of the n th harmonic can be approximately calculated by:

$$B_n = 2(n\gamma + 1)f_m = 2(n\Delta f_s + f_m) \tag{4.26}$$

Fig.4.17 shows the harmonics' spectrum comparison of a standard PWM and a frequency dithering PWM. Assuming the sum of the right and left bandwidths of the n th and $(n+1)$ th harmonics is:

$$B_{sum} = \frac{1}{2}(B_n + B_{n+1}) = (2n + 1)\Delta f_s + 2f_m \tag{4.27}$$

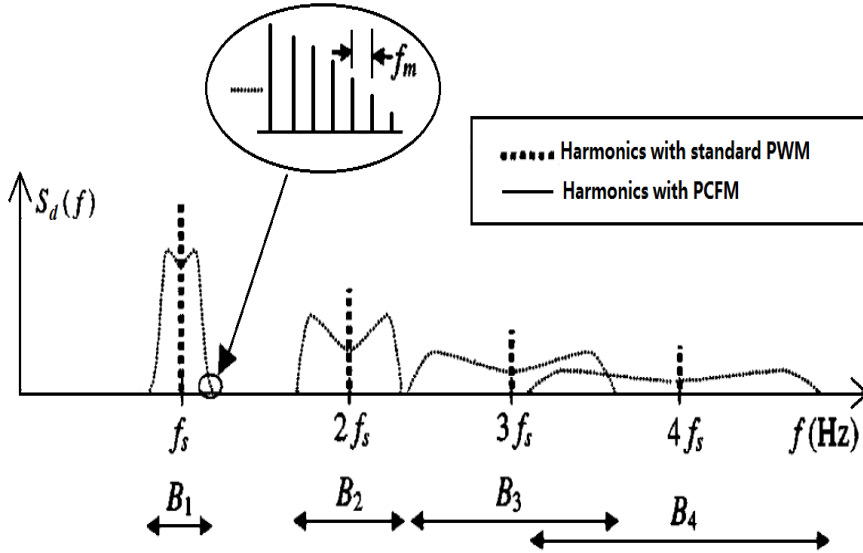


Figure 4.17: Harmonics' spectrum comparison [67]

Therefore, when B_{sum} is larger than f_s , these two sidebands will overlap each other. And the same as what has shown in Fig.4.17, the harmonics' power in the overlapping area of dithering PWM will be higher than standard PWM. This means, the smaller the f_s is, the larger the overlapping areas could be and the more power from the $(n+1)$ th harmonic's lower sidebands will be pushed into the higher sidebands of n th harmonic. This is why normally when measuring the EMI from a frequency dithering system, compare to the non-dithering system, the dithering system usually pushes the EMI from the high frequency domain into the low frequency domain.

4.3.3 Conclusions on Frequency Dithering and EMI Reductions

From the discussions of Section 4.3.2 it can be concluded that:

- Frequency dithering can do help to reduce the harmonics' amplitudes at central and multiples of central switching frequency.
- For a fixed frequency dithering system, the reduction for each individual

harmonic is different and depends on the harmonic's order.

- Usually, it is not possible to gain large harmonics' reductions in the whole frequency range after implementing frequency dithering.
- Normally when one measures the EMI from a frequency dithering system, comparing to the constant frequency system, in the frequency dithering system, the EMI often concentrates in the relatively low frequency range.

4.4 EMI Filter Design Considerations

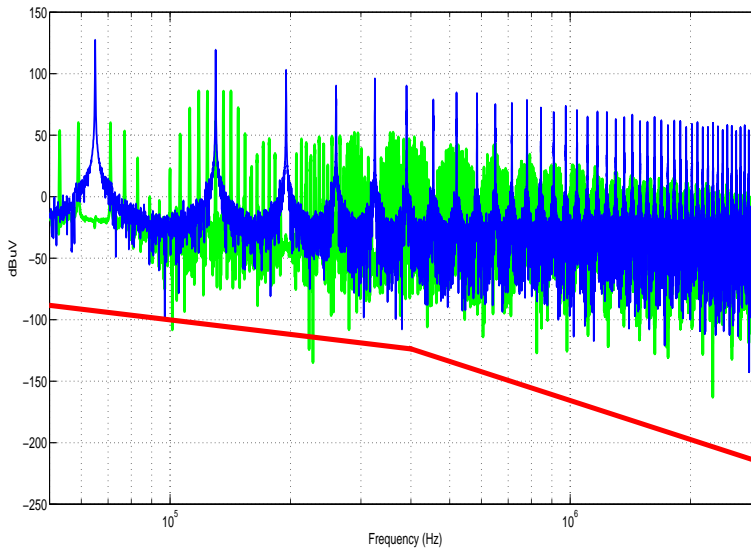


Figure 4.18: Harmonics' spectrum comparison for frequency dithering PWM (green) and standard PWM (blue), the red line is the filter's attenuation characteristic

According to what has been mentioned in Section 4.3, the limitations of frequency dithering will definitely harm its EMI performance and impact the EMI filter design. Considering the harmonics spectrums of a standard PWM and a frequency dithering PWM in Fig.4.18, the filter's attenuation characteristic is shown as the red line. If the cut-off frequency of the filter at minus 20dB/dec frequency band is f_c , for standard PWM, the filter's attenuation at multiples

of switching frequency nf_s is as below:

$$\alpha_n = -20\zeta \lg \frac{nf_s}{f_\zeta} - A_\zeta \quad (4.28)$$

Where ζ is related to filter's type, it is a function of filter's order and structure, and A_ζ is the filter's attenuation at f_ζ .

Therefore, after filtering, the harmonics' amplitude of standard PWM at nf_s is:

$$X_n = 20 \lg |C_n \cdot J_0(n\gamma)| + \alpha_n \quad (4.29)$$

Similarly, in the frequency dithering PWM, the filter's attenuations around multiple of switching frequency nf_s can be calculated as:

$$\beta_{n,k} = -20\zeta \lg \frac{nf_s + f_mk}{f_\zeta} - A_\zeta \quad (4.30)$$

Where k symbolizes the spread spectrum caused by frequency dithering. According to Eqs. (4.20) and (4.25), each spread spectrum has a frequency interval of f_m . By utilizing Eq. (4.26), the parameter k varies from:

$$-\lfloor n\gamma + 1 \rfloor \sim \lfloor n\gamma + 1 \rfloor \quad (4.31)$$

Therefore, after filtering, the harmonics amplitude of frequency dithering PWM around nf_s becomes:

$$Y_{n,k} = 20 \lg (|C_n \cdot J_{|k|}(n\gamma)|) + \beta_{n,k} \quad (4.32)$$

Due to the EMI receiver has impact on the EMI measurement result of frequency dithering system, it is not reasonable to determine the attenuation of any EMI filter apart from the impact of the EMI receiver. According to what has been analyzed in reference [80], the model of any EMI receiver can be expressed in Fig.4.19. The bandwidth of the band-pass filter (RBW filter) differs with dependency on the frequency band of interest. In CISPR 16 it is defined as RBW = 9 kHz at -6 dB for frequencies in the range 150kHz to 30MHz as shown in Fig.4.20, it also shows a simplified filter characteristic which is employed for numerical simulations of the EMI test receiver. The fixed value MB denotes the band-pass center frequency.

And it should be precise enough to predict the measured EMI result at each frequency by only considering the harmonics located inside the $\pm 10dB$ inner band pass filter of the EMI receiver. Set Z equals to the maximum value of k which satisfies that:

$$\frac{9kHz}{Z \cdot f_m kHz} \geq 1 \quad (4.33)$$

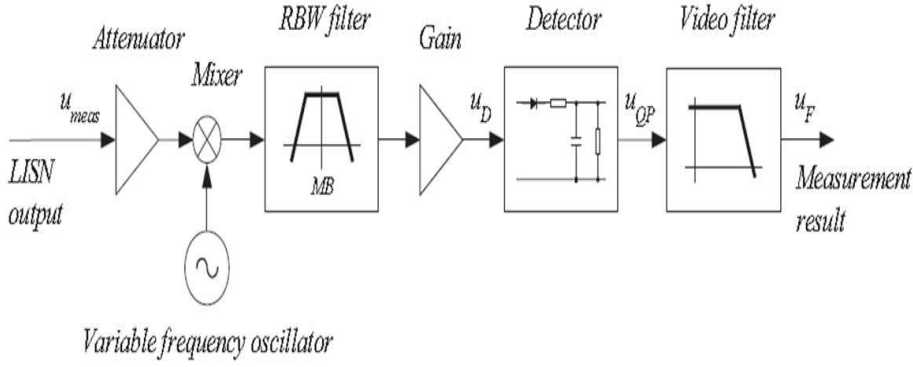


Figure 4.19: Simplified heterodyne measurement chain and QP detection model of a test receiver[80]

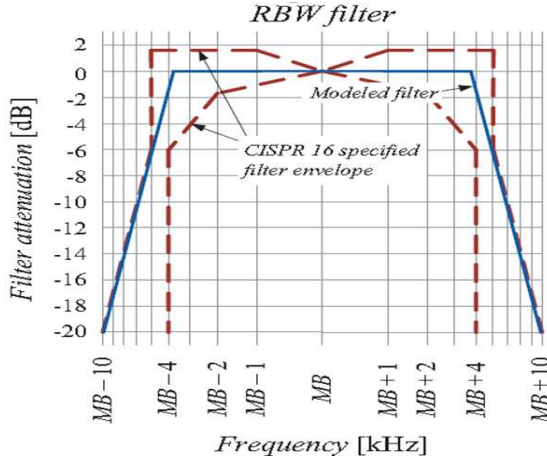


Figure 4.20: Upper and lower envelope of the characteristic of the resolution bandwidth (RBW) filter as specified in CISPR 16 and filter characteristic used when modeling the RBW filter [80]

The measured peak and average harmonics' amplitudes of dithering PWM displayed at nf_s can be predicted as below:

$$\hat{Y}_{n,Pk} = \{Y_{n,k}\}_{max}, k \leq |Z| \quad (4.34)$$

$$\tilde{Y}_{n,Av} = \frac{1}{2Z} \sum_{k=-Z}^Z Y_{n,k} \quad (4.35)$$

Where, Pk. means peak value and Av. means average value. Compare Eqs. (4.29), (4.34) and (4.35), after filtering significant harmonics' reduction from

dithering PWM may exhibit if $\tilde{Y}_{n,Av}$ far below X_n .

4.5 Experimental Results

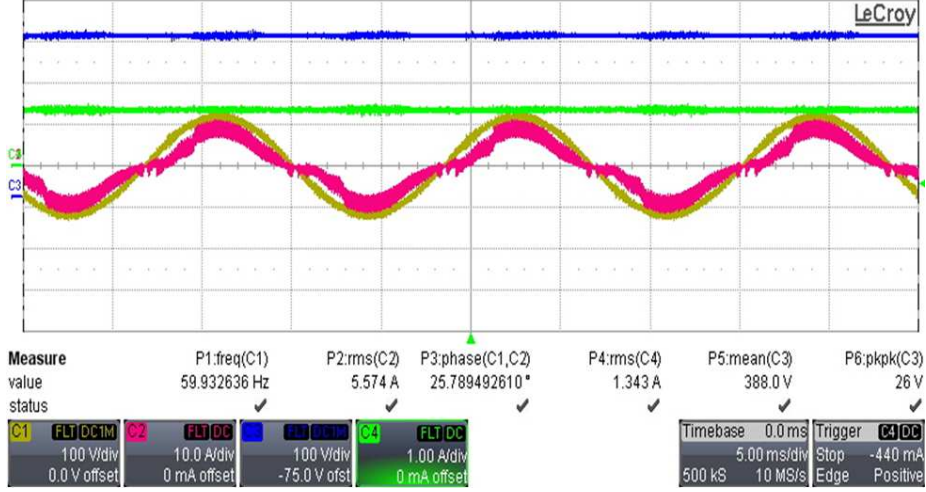


Figure 4.21: Input voltage (yellow, C1) and current (red, C2); output voltage (blue, C3) and current (green, C4) waveforms of the proposed frequency dithering IBPFC

As what has been proved in Section 4.2.2, in order to show the advantage of EMI reduction comparing to non-interleaved BPFC, a useful central switching frequency f_s was set at 65kHz. According to the conducted EMI standard, the highest harmonic's amplitude which needs to be attenuated locates at 260kHz (the 4th order harmonic) [61]. As what shows in Fig.4.16, for further reducing the attenuation at 260kHz, a dithering amplitude Δf_s of 7.55kHz and dithering rate f_m of 6.1kHz are selected. This leads a dithering factor γ at 1.24, and will give a 33.15dB reduction at the 4th harmonic. Due to the aim of this IBPFC design is for audio application, we only interested in the EMI performance at average power, which is around 440W. Therefore, the experimental results below were all taken at 440W.

Fig.4.21 shows the waveforms of the input voltage, input current, output voltage and output current of proposed frequency dithering IBPFC system at $110V_{ac}$.

Fig.4.22 shows the EMI measurements of the 2-stage IBPFC in Fig.4.3 with and without frequency dithering at $110V_{ac}$. Additionally, in Fig.4.23, there is the detailed amplitudes' comparison of 4 highest harmonics in Fig.4.22.

Table 4.1: EMI Comparison of Critical Harmonics

Harmonics' Frequency (kHz)		260		390		520		650	
EMI Detector		Pk.	Av.	Pk.	Av.	Pk.	Av.	Pk.	Av.
Dither IBPFC (dBuV)	P.	125	124	121	116	115	107	112	109
	M.	126	122	123	116	118	111	116	107
Prediction error (dBuV)		-1	2	-2	0	-3	-4	-4	2

Implementing the derived mathematical expressions in Section 4.3 and 4.4, Table.4.1 gives the harmonics' amplitudes comparison in Fig.4.22 between experiments and theoretical predictions of the frequency dithering IBPFC. Where, P. means predicted value and M. means measured value.

From Table.4.1, it can be proved that using the mathematical method mentioned in Section 4.3 and 4.4, the EMI performances of the frequency dithering IBPFC can be predicted approximately.

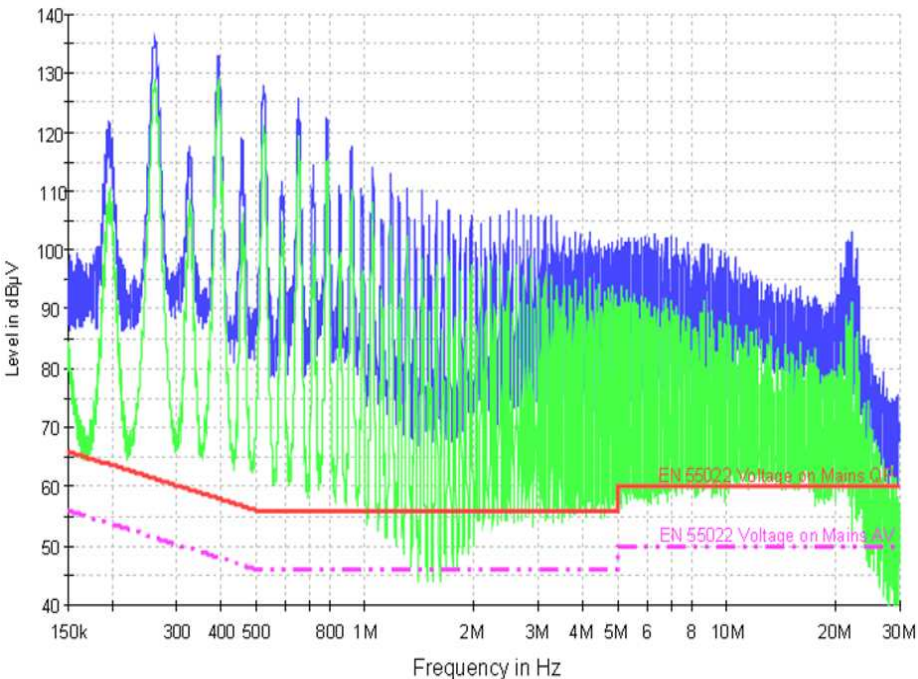
Fig.4.25 gives the Conducted EMI comparison of standard IBPFC and proposed frequency dithering IBPFC at $110V_{ac}$ and $1/8$ peak power with the same EMI input filter. The schematic of the EMI filter is shown in Fig.4.24.

Figs.4.22 and 4.25 shows that the EMI generated by frequency dithering PWM is lower and easier to attenuate by EMI filter than traditional IBPFC. And by combining of interleaving and frequency dithering techniques, further EMI reduction can be achieved.

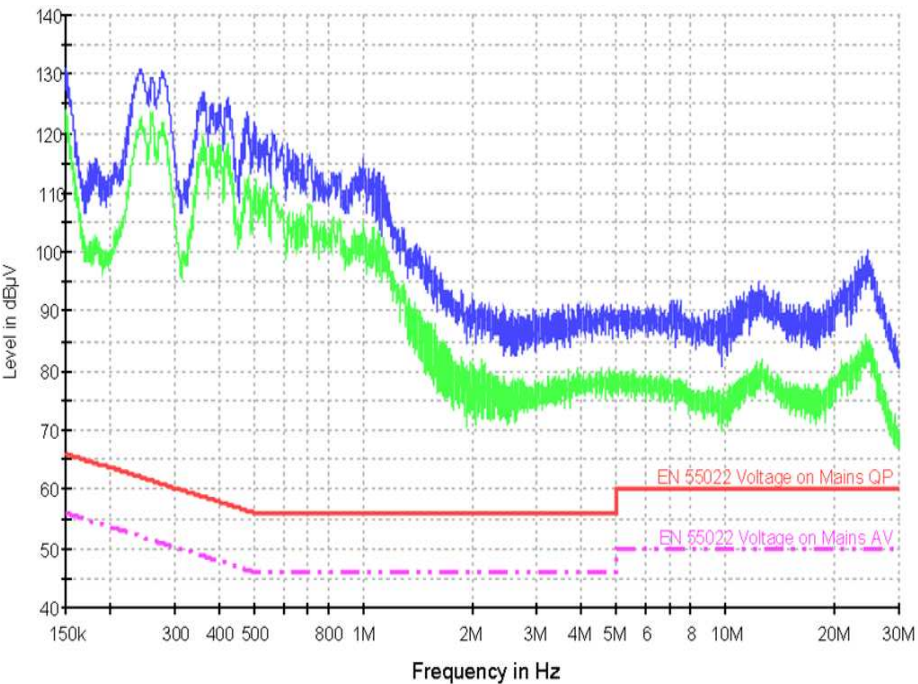
4.6 Conclusions of EMI Analysis and Suppression

From the discussions above, the conclusions for EMI analysis and suppression can be drawn as below:

- Interleave technique is a useful method for EMI suppression, by implementing 2-stage interleaved BPFC, compare to the non-interleaved BPFC, a maximum -10dB attenuation can be gain at 195kHz (the 3rd harmonics).
- Extra EMI reduction can be gain by carefully design frequency dithering.



(a) Standard IBPFC, Pk. value in blue, Av. value in green



(b) Proposed frequency dithering IBPFC, Pk. value in blue, Av. value in green

Figure 4.22: Conducted EMI comparison of standard IBPFC and proposed frequency dithering IBPFC without filter at 110V_{ac} input and 1 over 8 peak power

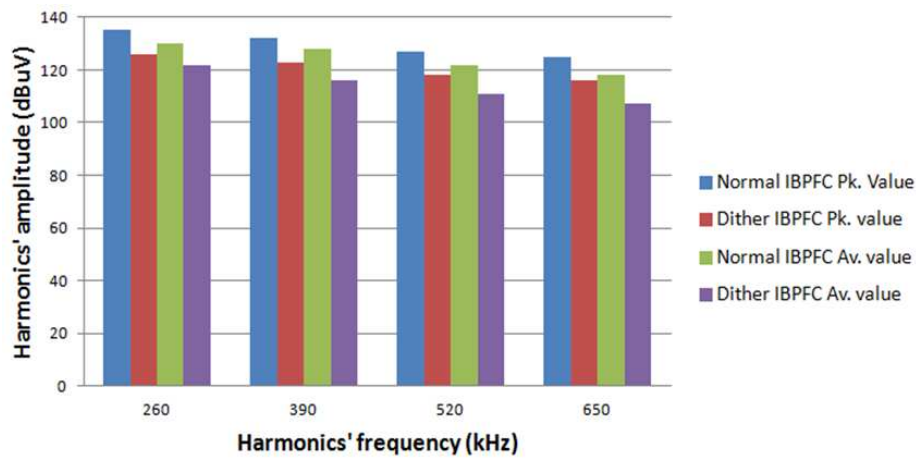


Figure 4.23: Detailed EMI comparison of 4 highest harmonics in Fig.4.22

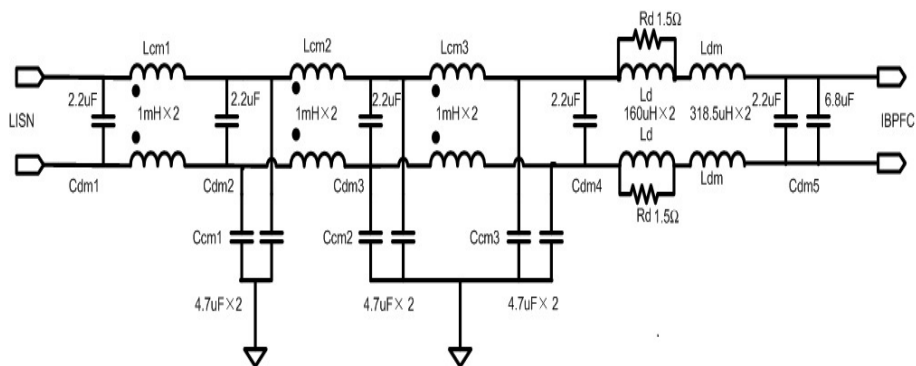
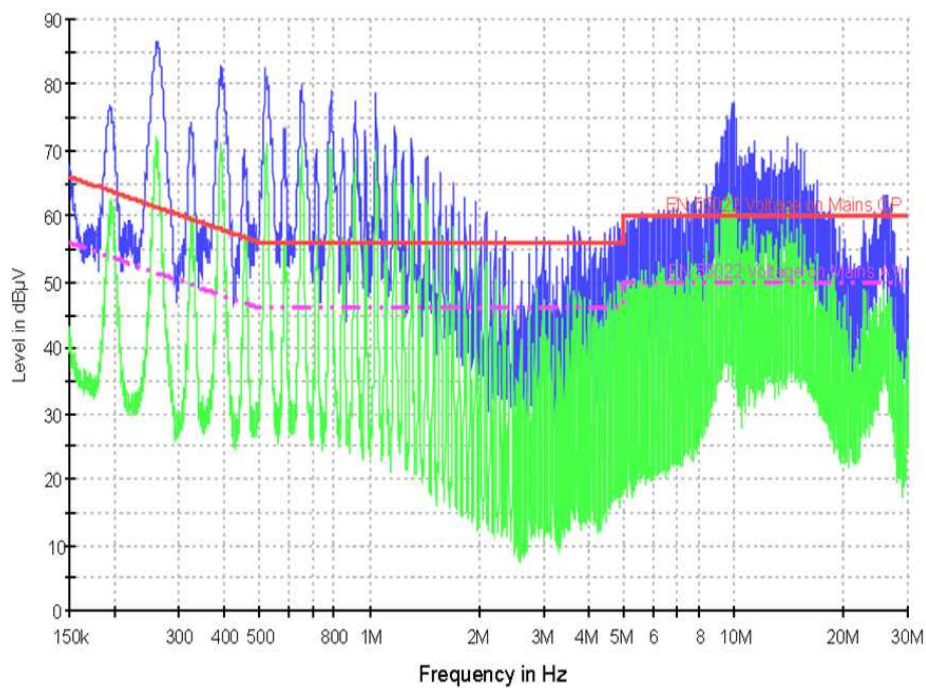
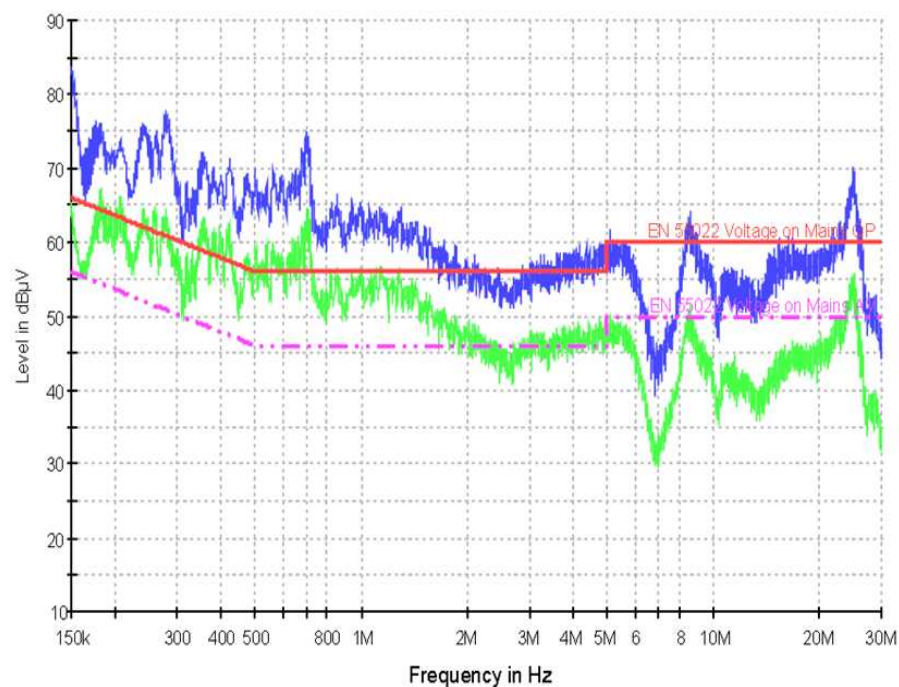


Figure 4.24: The schematic of the EMI filter



(a) Standard IBPFC, Pk. value in blue, Av. value in green



(b) Proposed frequency dithering IBPFC, Pk. value in blue, Av. value in green

Figure 4.25: Conducted EMI comparison of standard IBPFC and proposed frequency dithering IBPFC at $110V_{ac}$ and $1/8$ peak power with the same filter

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Accuracy Analysis

With the increasing demands on high efficient power converter design, during recent years, more and more researchers write papers about their super high efficiency PFC converters. In these publications, the converter's peak efficiency is varying from 98.3% to 99.3% [81–84]. However, none of these paper explains how accurate their measurement is. In this Chapter, the author will take her own measurement results of the high efficient 2-stage IBPFC in Chapter 4 as an example and clarify the accuracy of its efficiency measurement briefly.

5.1 Experiment Set Up

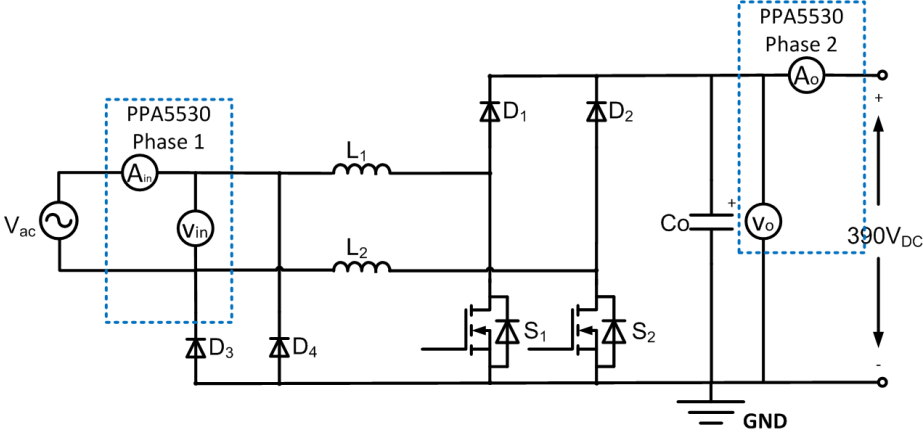
In order to measure the system's efficiency precisely, the simplified diagram of experiment set up is shown in Fig.5.1. Both of the input and output voltage meters are put very close to the BPFC's terminals to avoid measuring the voltage drops from the connecting cables. As the measurements were taken by Precision Power Analyzer PPA5530 made by *N4L*[®], its accuracy specifications are given in Table 5.1.

Table 5.1: Accuracy Specification of N4L[®] Precision Power Analyzer PPA5530[85]

AC Voltage Accuracy	$0.02\% \times R_{dg}^a + 0.04\% \times R_{ng}^b + 0.04\% \times kHz + 1mV$
AC Current Accuracy	$0.02\% \times R_{dg} + 0.04\% \times R_{ng} + 0.04\% \times kHz + 100uA$
DC Voltage Accuracy	$0.1\% \times R_{dg} + 0.1\% \times R_{ng} + 10mV$
DC Current Accuracy	$0.1\% \times R_{dg} + 0.1\% \times R_{ng} + 1mA$
Phase Accuracy	5 millidegrees + 10 millidegrees \times kHz
CM Rejection: Total CM and noise effect on current channels	Applied 250V@50Hz — Typical 1mA (150dB)
	Applied 100V@100kHz — Typical 3mA (130dB)

^a R_{dg} means reading data.

^b R_{ng} means reading range.

**Figure 5.1:** Simplified diagram of efficiency measurement set up

5.2 Accuracy Analysis

The basic idea of the accuracy analysis is to figure out how precise the PPA5530 is when the measurements are affected by different interference. The analysis procedure (Fig.5.2) is proposed and taken into consideration. By measuring the input voltage and current harmonics and output voltage and current harmonics separately through the N4L PPA5530, implementing the voltage and current accuracy equations in Table 5.1, the input and output power accuracy can be predict firstly, and then, the total efficiency accuracy can be calculated. It is easy to see, this procedure predicts the possible worst accuracy of the measurement.

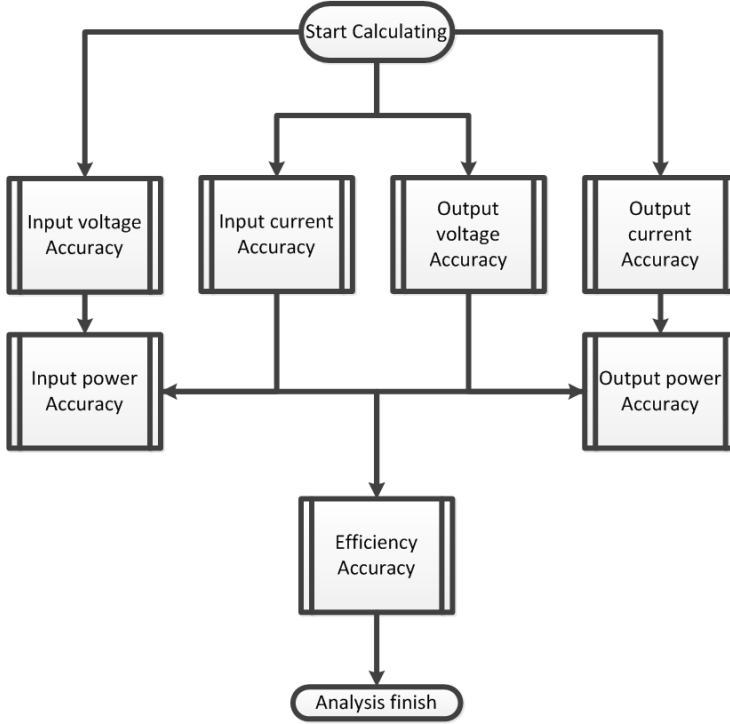


Figure 5.2: Accuracy analysis procedure

5.2.1 Accuracy of Measured P_{in} and P_o

The accuracy of P_{in} and P_o can be calculated from the accuracy of voltage and current:

$$\begin{aligned}
 \Delta P &= |P - P_{meas}| \Rightarrow \\
 \Delta P &= |V \cdot I - (V \pm \Delta V)(I \pm \Delta I)| \Rightarrow \\
 \Delta P_{max} &= |(\Delta V \cdot I + \Delta I \cdot V) + \Delta V \Delta I| \Rightarrow \\
 \Delta P_{max} &\simeq |\Delta V| \cdot I + |\Delta I| \cdot V \Rightarrow \\
 \Delta P_{max} &\simeq |\Delta V| \cdot I_{meas} + |\Delta I| \cdot V_{meas}
 \end{aligned} \tag{5.1}$$

Where, P , V , I is the real value of power, voltage and current. P_{meas} is the measured value of power, V_{meas} is the reading value of voltage, I_{meas} is the reading value of current, ΔP is error of measured power, ΔP_{max} is maximum error of measured power, ΔV is maximum error of measured voltage, ΔI is maximum error of measured current.

5.2.2 Accuracy of Measured Efficiency

Then, the maximum error of efficiency can be found by:

$$\begin{aligned}
 \Delta\eta &= |\eta - \eta_{meas}| \Rightarrow \\
 \Delta\eta &= \left| \frac{P_o}{P_{in}} - \frac{P_o \pm \Delta P_o}{P_{in} \pm \Delta P_{in}} \right| \Rightarrow \\
 \Delta\eta_{max} &= \left| \frac{P_o \cdot \Delta P_{in} + P_{in} \cdot \Delta P_o}{P_{in} \cdot (P_{in} - \Delta P_{in})} \right| \Rightarrow \\
 \Delta\eta_{max} &\simeq \left| \frac{P_{o,meas} \cdot \Delta P_{in} + P_{in,meas} \cdot \Delta P_o}{P_{in,meas}^2} \right| \quad (5.2)
 \end{aligned}$$

η is the real value of efficiency, η_{meas} is the reading value of efficiency, $\Delta\eta$ is error of measured efficiency, $\Delta\eta_{max}$ is the maximum error of measured efficiency. ΔP_{in} and ΔP_o are maximum error of input and output power, $P_{in,meas}$ and $P_{o,meas}$ are reading value of input and output power.

5.2.3 Estimation of Worst-case Accuracy of Efficiency

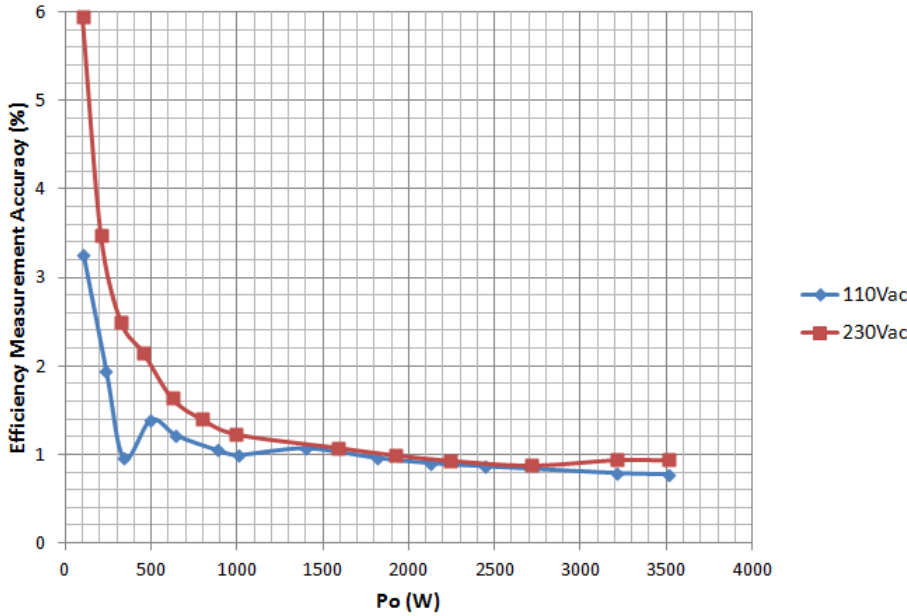


Figure 5.3: Measurement Accuracy Prediction

Fig.5.3 shows the prediction measurement accuracy of the efficiency measurement results in Chapter 4 Fig.4.9 according to eq.5.1 and 5.2.

From Fig.5.3, it can be seen that: the efficiency measurement error at light load is larger than the heavy load, especially in a power range lower than 250W. That is because in the light load, the input power is lower, and according to Eq. (5.2), the efficiency accuracy is proportional to the inverse of square of input power.

According to Fig.5.3, it can be concluded that with the output power increasing the measurement error is reducing and finally the measurement accuracy is stable around $\pm 0.9\%$ at $230V_{ac}$ and $\pm 0.8\%$ at $110V_{ac}$.

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Conclusions and Future Works

6.1 Summary and Conclusions

A state-of-the-art analysis has been performed to give an overview of the five popular Bridgeless PFC converters. And the analysis reveals that:

1. As the newly invented topologies, many BPFC converters are only verified by theory and simulations;
2. The designs of Two-Boost-Circuit BPFC and Totem-pole BPFC were achieved only in low and medium power, their peak efficiency are 97% and 97.8% respectively;
3. There are lack of research based on high power universal line BPFC design and optimization;
4. The Two-Boost-Circuit BPFC can be a very useful topology for high power application due to its higher efficiency, relatively lower EMI generation and less complex control and drive systems.

In order to verify and optimize the Two-Boost-Circuit BPFC, and try to gain as high efficiency as it can be, a detailed analysis on Boost inductor optimization

(including efficiency and power density analysis) have been conducted. The analysis and experiments reveals that:

1. For constant output power, it is not necessary to use a very large Boost inductor to improve system efficiency in the Two-Boost-Circuit BPFC;
2. If the BPFC often operates in variable output power, there will be a best region for Boost inductance with relatively flat and high efficiency and good power density.

In order to improve the EMI performance while maintaining the high efficiency merit of the traditional Two-Boost-Circuit BPFC converter, the novel 2-stage interleaved BPFC (IBPFC) system is proposed and designed based on the multi-objective optimization procedure. The analysis and experiments reveals that:

1. Interleaved stages help to improve both CM and DM EMI;
2. In an N-stage IBPFC, except the $c \times N$ times fundamental frequencies, all the rest harmonics can be reduced due to the phase shift;
3. The more interleaved stages the IBPFC has, the more high frequency harmonics will be reduced;
4. In order to maintain the EMI advantage of IBPFC, it is better to select its switching frequency based on the range of conduction EMI standard. It is recommended that the first harmonic of the IBPFC, which locates inside the range of the EMI limitation, should not be equal to $c \times N$ times of fundamental switching frequencies.

After finishing the high efficiency 2-stage IBPFC design, frequency dithering technique was implemented to further improve the EMI of the this system. Both of its advantages and limitations have been discussed. The analysis and experiments reveals that:

1. Frequency dithering can do help to reduce the harmonics' amplitudes at central and multiples of central switching frequency;
2. For a fixed frequency dithering system, the EMI reduction for each individual harmonic is different and depends on harmonic's order;
3. Usually, it is not possible to gain large harmonics' reductions in the whole frequency range by implementing fixed frequency dithering, however, it can be expected to use frequency dithering to mitigate the amplitude of harmonic at a certain frequency;

4. Normally when one measures the EMI of a frequency dithering system, comparing to the same non-frequency-dithering system, its EMI will concentrate in a relative low frequency range, therefore in the high frequency domain, the harmonics' amplitudes become lower.

Furthermore, based on the measurement set up of the 2-stage IBPFC system, the measurement accuracy is given to make the experimental results more convictive.

Therefore, according to the summary above, in this project, an Boost inductor optimization procedure based on high efficiency Two-Boost-Circuit BPFC converters has been presented and verified firstly. And then, a novel interleaved Two-Boost-Circuit BPFC is proposed and designed based on a multi-objective-optimization procedure to achieve a useful compromise of efficiency, power density, EMI reduction and system complexity. Furthermore, both of the optimized non-interleaved and interleaved BPFCs achieve maximum efficiencies above 98%. Finally, two possible cost-efficient solutions - interleaving and frequency dithering - for EMI suppression have been proposed, investigate and verified.

6.2 Future Works

According to the nature advantages of the 3-stage and 4-stage IBPFC systems mentioned in section 4.2.3.2, they are also worth to be investigated in the future.

Furthermore, from the discussions in section 4.4, it can be seen: a proper design of the input filter may improve the EMI reductions of the frequency dithering system. So, additional research and development efforts can also be put forward to invest the possible optimal design for EMI filter under frequency dithering condition in order to achieve better EMI reduction and lower filter's volume together.

The possible future works indicated above can be very useful for industrial applications.

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APPENDIX A

Publications

A.1 PEDS2009 Published

Conduction Losses and Common Mode EMI Analysis on Bridgeless Power Factor Correction

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Abstract—In this paper, a review of Bridgeless Boost power factor correction (PFC) converters is presented at first. Performance comparison on conduction losses and common mode electromagnetic interference (EMI) are analyzed between conventional Boost PFC converter and members of Bridgeless PFC family. Experiment results are given to validate the efficiency analysis and EMI model building.

Keywords—conduction losses; EMI; bridgeless; power factor correction (PFC)

I. INTRODUCTION

With demands on improving electromagnetic compatibility and reducing loss in power supplies in industrial applications, research on maximizing power transmission turns out to have significant impact. Innovation and optimization of power factor correction (PFC) technology would be an important method to achieve higher efficiency and low electromagnetic interference (EMI) power supplies.

Traditional Boost PFC in Fig. 1 cannot avoid some natural power loss because of the drawbacks of their structures with full-wave rectifier in the input. Recently, a new PFC family called Bridgeless PFC (BLPFC) family has been proposed to realize high efficiency PFC converters by more or less eliminating the ac rectifier of traditional Boost PFC [1~3]. However, whether all the members belonging to BLPFC family have high efficiency is doubtful, besides many researchers have shown that some of the BLPFC topologies have bad EMI performance due to their circuit structures [4~5].

In this paper, a systematic review of BLPFC family is presented; conduction losses and common mode (CM) EMI performances are analyzed comparing with conventional Boost PFC. Simulation and experiment results shows that low EMI and high efficiency PFC can be realized by a certain BLPFC topology.

II. REVIEW OF BRIDGELESS BOOST PFC CONVERTERS

A. Five Bridgeless Boost PFC Topologies for Comparison

Five different type of BLPFC topologies are discussed in this section. The basic one in Fig. 2, called Dual Boost PFC, which has been shown to have higher efficiency than conventional Boost PFC in Fig. 1, because of the reduced semiconductor numbers in line current path [6]. However, this

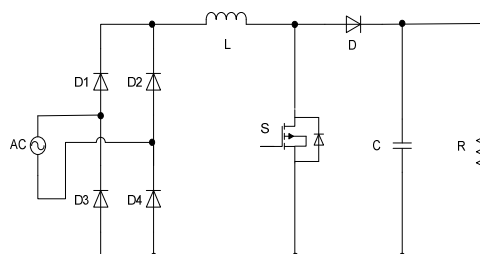


Figure 1. Conventional Boost PFC

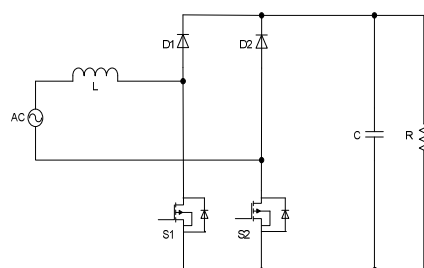


Figure 2. Dual Boost PFC

PFC rectifier has significantly larger CM noise than the conventional Boost PFC. The reason is that: in the conventional boost PFC, the output ground is always connected to the ac source through full-bridge rectifier, whereas, in the Dual Boost PFC, the output ground is connected to the ac source only during positive half-line cycle through the body diode of switches. So large pulse current from high frequency switches will flow through parasitic capacitors and brings EMI problems.

Fig. 3 is a Bidirectional Switches BLPFC [7] using two additional fast diodes. This leads to increase conduction losses of the circuit. Because in the negative half-line period, in traditional Boost PFC, there is only one high frequency diode and two low frequency diodes conducting, but in Fig. 3, there are two high frequency diodes conducting together.

In Fig. 4, there are two Boost circuits in the BLPFC [8~9]. One can expect higher efficiency than Boost PFC with the same reason as Dual Boost PFC. And its EMI will be lower than Boost PFC, because not only the low frequency diodes D3 and D4 connect the output ground to the ac source but the symmetric Boost inductors operate as a CM filter which can be expected to achieve higher CM EMI reduction.

Fig. 5 is called Pseudo Totem-pole BLPFC, because of the position of switches [10]. This topology also has only 2 semiconductors in series on its current path no matter the MOSFET is on or off. So it has the same benefit in conduction losses reduction as which in Fig. 2 and Fig. 4.

Finally, Fig. 6 shows a modification of the basic BLPFC Boost rectifier from Fig. 2, which is obtained by exchanging the position of the diode and switch in Fig. 2.

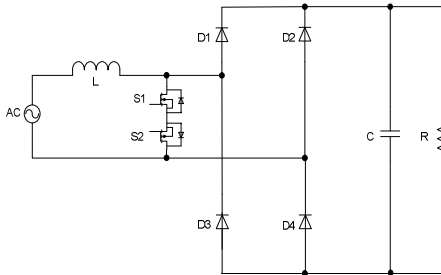


Figure 3. Bidirectional Switches Boost PFC

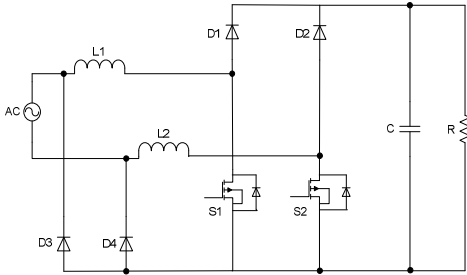


Figure 4. Two-boost-circuit PFC

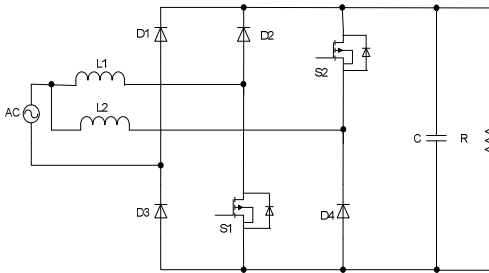


Figure 5. Pseudo Totem-pole PFC

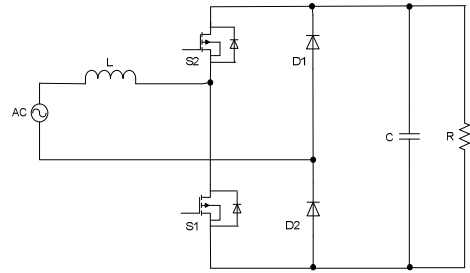


Figure 6. Totem-pole PFC

B. Conduction Losses Calculation

It is well known that what dominate the power loss in PFC converters are semiconductor losses. Table 1 gives the semiconductor numbers in current flow path of each PFC topology during line positive ac period. Where, On/Off means on time and off time of MOSFET; D_F symbolizes fast diode; D_L symbolizes line frequency diode; M is for MOSFET and D_M is the body diode of MOSFET. It shows that the BLPFCs respectively have lower semiconductor numbers comparing with conventional Boost PFC, which will bring benefits on decreasing conduction losses of the whole systems.

For making a fair comparison, all the MOSFETs of different PFC topologies operated in hard switching condition.

The simulation parameters are choosing as below:

$$P_o = 3.5 \text{ kW} ; V_o = 400 \text{ V}_{dc} ; V_{in} = 85 \sim 265 \text{ V}_{ac} ; \text{ the}$$

TABLE I. SEMICONDUCTOR NUMBERS IN CURRENT FLOW PATH IN THE SIX PFC TOPOLOGIES

PFC topology	On/Off	D_F	D_L	M	D_M	Total Number
Boost PFC	On	0	2	1	0	3
	Off	1		0		
Dual Boost PFC	On	0	0	1	1	2
	Off	1		0		
Bidirectional Switches PFC	On	0	0	1	1	2
	Off	2		0	0	
Two-boost-circuit PFC	On	0	1	1	0	2
	Off	1		0		
Pseudo Totem-pole PFC	On	0	1	1	0	2
	Off	1		0		
Totem-pole	On	0	1	1	0	2
	Off			0	1	

Boost inductor $L = 3\text{mH}$; MOSFET: STW45NM50; Fast Diodes: RHRP-3060.

Fig. 7 shows the efficiency columns of six PFC topologies based on simulation results when only the conduction losses are taken into account. Totem-pole PFC in Fig. 6, Two-boost-circuit PFC in Fig. 4 and Pseudo Totem-pole in Fig. 5 has better efficiency comparing with other topologies. These are according with what has been discussed theoretically in part A and which are shown in Table 1. It should be noticed that Fig. 3 may not be a high efficient topology without choosing circuit components carefully, because it has two fast diodes working together when the MOS is off.

Fig. 8 shows the voltage waveforms between power ground and the neutral of ac source from Fig. 1 to 6 during one ac

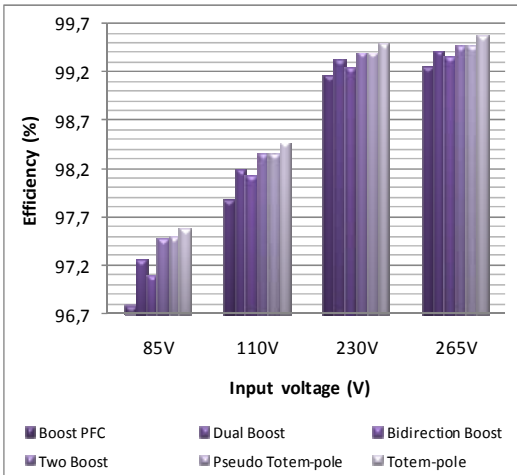


Figure 7. Efficiency comparison only for conduction losses among six PFC topologies based on simulation.

period. Since the CM noise is induced by the internal noise voltage between the ground reference point and the cable connection, which mostly comes from the high frequency switch operation of the PFC converter [11]. Therefore, this figure shows the possible CM EMI problems in the six PFC topologies, because in this way, we consider the neutral as a ground reference and take the power ground as the cable connection point. And it is not only easy to find out that traditional Boost PFC in Fig. 1 and the BLPFC topologies in Fig. 4 and 5 all have lower EMI comparing with other PFC topologies, because of there is no pulse voltage in their waveforms during line negative period; but also easy to get that BLPFC in Fig. 5 has worse EMI than Boost PFC in Fig. 1 and BLPFC in Fig. 4, since its quasi-square wave will bring lots of high frequency noise components, which may decrease its EMI performance. It should be noticed that although there is no pulse voltage show in Fig. 8(f), this does not mean the Totem-pole Bridgeless PFC has better EMI performance. That's because during the line negative period, the boost inductor will bring lots of switching frequency pulses between power ground and the line, which will cause serious EMI problem, too.

Through Fig. 7 and 8, in order to remain the same CM EMI performance as traditional Boost PFC, it can be concluded that only BLPFCs in Figs. 4 and 5 are needed to be further considered. In next sections, Two-boost-circuit BLPFC in Fig.4 is selected for EMI model building and further discussion, for its high efficiency and low EMI comparing with other BLPFCs. Furthermore, its gate drives are referenced to ground and easier to realize for industrial application.

III. EMI MODEL BUILDING AND CM NOISE ANALYSIS

A. EMI Model Building

If we take the Boost PFC as a noise source and consider the ac source as a load, it was proved that the EMI model of the Boost PFC converter equals to a high frequency pulse source [12]. In order to make a precise EMI analysis of BLPFC family, the EMI model is needed to be built. Take Two-boost-

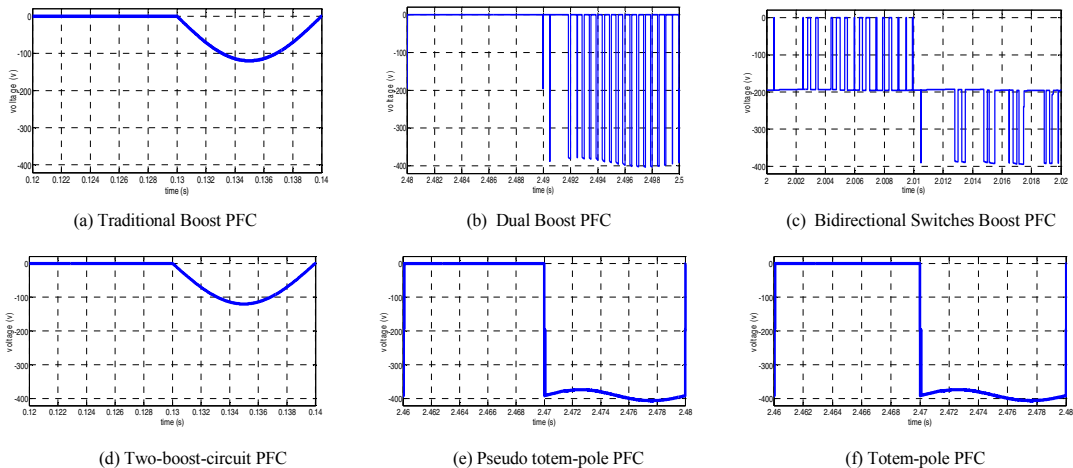


Figure 8. CM voltage waveforms between power ground and the neutral of ac source showing the EMI comparison among the six PFC topologies

circuit PFC as an example; since it's a symmetrical circuit for both positive and negative part of ac source, we only consider the positive ac period. Ignore the limited noise current flows through the body diode of S2 and L2 [13], analysis of generate the EMI model of the topology is showed in Fig. 9.

- Step 1: Using the symmetrical operation structure to simplify the topology.
- Step 2: Because the output filter capacitor can be considered as a short circuit in high frequency, and the boost inductor can be considered as an open circuit, these two components can be ignored.
- Step 3: Simplify the semiconductor components. In high frequency domain, the fast diode can be simplified as a capacitor and the MOSFET can be considered as a pulse source.
- Step 4: Deduction of circuit using Thevenin's Theory.

As the result, the Two-boost-circuit BL PFC in the positive ac source can be equal to a pulse voltage source V_{eq} in series with a capacitor C_{eq} .

$$V_{eq} = -V_{ds} \times C_{s1} \times C_{eq}^{-1} \quad (1)$$

$$C_{eq} = C_{s1} + C_{s2} + C_b \quad (2)$$

Where, C_{s1} and C_{s2} are the parasitic capacitances of MOSFETs, C_b is the capacitance between output ground and the power earth. Normally, C_b is 10 to 20 times bigger than C_{s1} and C_{s2} [14], so if there is any pulses voltage across it, it will bring a significant extra CM current flow through it and lead to CM EMI problems. However, from (1) and Fig. 9(c), one can find that C_b is connected directly between the source of the MOS (which connected to the neutral) and the earth. This will cause no pulses voltage draw on C_b , therefore the CM current of the circuit will be reduced.

EMI model of this topology in the negative period of ac source is the almost the same as the former one in (1), but:

$$V_{eq} = -V_{ds} \times C_{s2} \times C_{eq}^{-1} \quad (3)$$

Assuming $C_{s1} = C_{s2} = C_s$, the EMI model for the whole ac period can be written as:

$$V_{eq} = -V_{ds} \times C_s \times C_{eq}^{-1} \quad (4)$$

$$I_{eq} = -V_{ds} \times \omega C_s \quad (5)$$

Equation (4) shows that although the switching operation generates high frequency pulses inside the Two-boost-circuit PFC, they will not impact the voltage waveform between power ground and neutral. Because of the line frequency return diodes D3 and D4 in Fig. 4, the power ground is connected to the neutral for the whole ac period and all the pluses voltages go into the earth through the parasitic capacitances C_s of the MOS, which gives a continuous and smooth waveform between power ground and the neutral, just like what has been shown in Fig. 8(d). Equation (5) shows that the CM current will only flow through the parasitic capacitance of MOS.

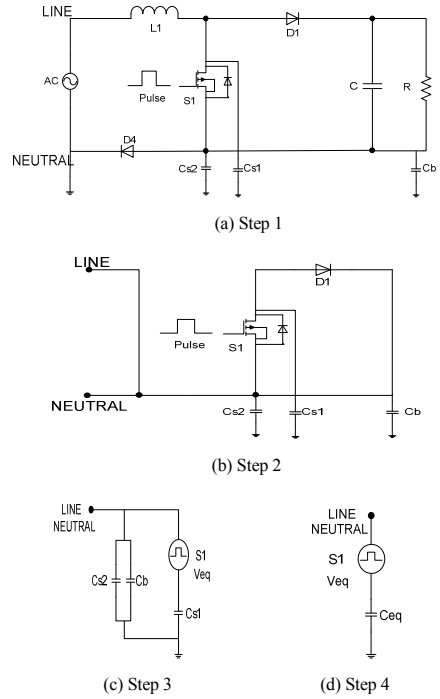


Figure 9. EMI model building for two-boost-circuit PFC

Using the same way to analysis, all the EMI models among Figs. 1 to 6 can be calculated mathematically.

B. CM Noise Analysis

CM noise is a very important issue, which not only affects the design of EMI filter but also influences the stability of the circuit. Fig. 8 shows that traditional Boost PFC, Tow-boost-circuit PFC and Pseudo totem-pole PFC have lower EMI comparing with other PFC topologies. Dual Boost PFC and Totem-pole PFC have higher EMI in line negative period because the neutral is separated from output ground by the

TABLE II. EMC AND EFFICIENCY COMPARISON AMONG SIX PFC TOPOLOGIES

PFC topology	Efficiency Rank	CM Voltage Rank	CM Current Rank
Boost PFC	6	1	1
Dual Boost PFC	4	5	5
Bidirectional Switches PFC	5	5	5
Two-boost-circuit PFC	2	1	1
Pseudo Totem-pole PFC		3	3
Totem-pole	1	3	3

boost inductor, which will require larger EMI filter to meet the EMC standard. Obviously, Dual boost PFC and Totem-pole PFC are not suitable for industrial application without improvement. Especially in Dual boost and Totem-pole PFC, because C_b is connected between the drain of the MOS and the earth and its impedance is too small, it will increase the CM current and a part of it will flow through control circuit by stray capacitor connected between MOSFET and control loop. This will lead an unstable factor to the whole system and bring problems in converter design [15].

Table 2 gives the CM EMC and efficiency comparison among conventional Boost PFC and five BLPFs. From this table, it comes to a conclusion that the Two-boost-circuit PFC shows higher efficiency and lower EMI performances, which is worth for industrial application and further improvement.

IV. EXPERIMENT RESULTS

The performance comparison of the Boost PFC and Two-boost-circuit PFC shown in Fig. 1 and 4, was evaluated on the same prototype hardware, which is a 65kHz switching frequency, 350W output power circuit operating from a universal ac-line input (85–260Vrms) and delivering up to 0.9A at 390V output. The schematics of both PFCs are shown in Fig. 10 and 11. Since the drain voltage of boost switches is

clamped to bulk capacitor, the peak voltage stress on each boost switch is approximately 390V. The peak current stress on boost switches, which occurs at full-load and low line, is approximately 5.4A. Therefore, SPW47N60C3 MOSFET from Infineon was used for each PFC converter. Boost diodes were implemented with IDT04S60C SiC diode from Infineon, and two diodes of bridge rectifier in traditional PFC, 1N5406 from Multicomp, were used as the return diodes D3 and D4 in two-boost-circuit PFC. The cores of the boost inductors L are 77083-A7 (high flux Kool-Mu core from Magnetics. A magnet wire (AWG#19) was used for each winding. Finally, two high voltage aluminum capacitors (270 μ F, 400VDC) were used for bulk capacitor.

UCC28019 (an eight-pin continuous-conduction-mode PFC controller) from Texas Instrument was used in the experimental prototype circuit because it does not require line voltage sensing. It should be noted that switches S1 and S2 in both Dual Boost and Two-circuit-boost PFC are operated simultaneously by the same gate signal from the controller. Although both switches are always gated, only one switch, on which the positive input voltage is induced, carries positive current and delivers the power to the output. The other switch, on which the negative input voltage is induced, does not influence the operation since its body diode conducts.

To compare the efficiency of the two PFC converters fairly, two SPW47N60C3 MOSFETs connected in parallel were used as boost switch, while two IDT04S60C SiC diodes connected in parallel were used as boost diode in conventional Boost PFC. A full-bridge rectifier built with four 1N5406 from Multicomp was used as an input-bridge rectifier.

Fig. 12 shows the measured efficiency of the traditional Boost PFC (dashed line) and the Two-boost-circuit PFC (solid line) as functions of the output power, when the ac input is 85V. As can be seen in Fig. 10, the bridgeless rectifiers have higher conversion efficiency than the conventional Boost PFC rectifier over the entire measured power range. Fig. 13 shows the simulation results of conduction losses and percent of output power comparison between Boost PFC and Two-boost-circuit PFC at 85 Vac input and 350W power level. The simulation result shows one can gain 1.22% efficiency improvement with Two-boost-circuit PFC, which is almost according with the measurement results 1.58% in Fig. 12. The small difference may come from the switching losses (since we use two MOS

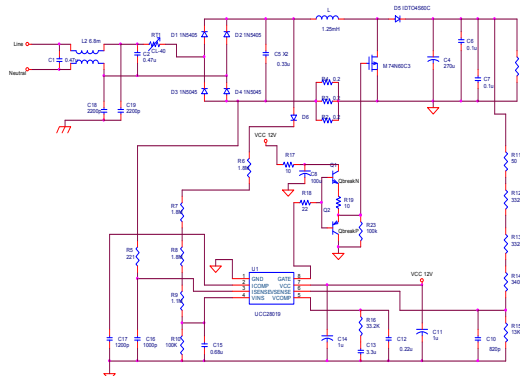


Figure 10. Schematic of conventional Boost PFC

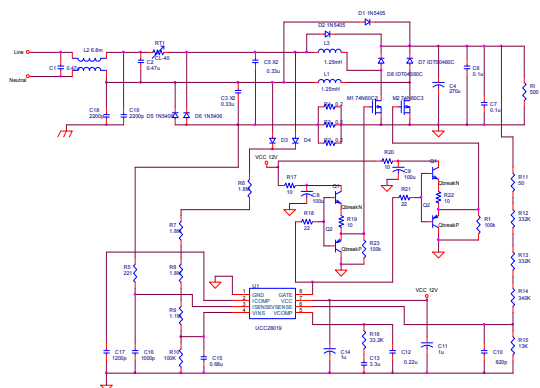


Figure 11. Schematic of Two-boost-circuit PFC

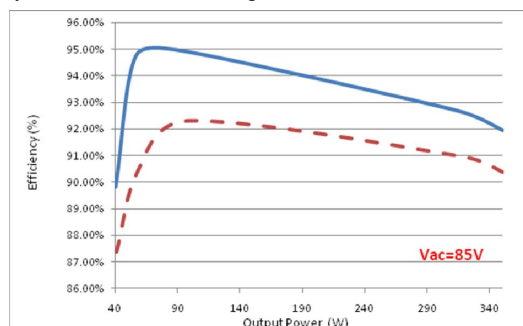


Figure 12. Efficiencies measurement at 85Vac input of conventional Boost PFC (dashed line) and Two-boost-circuit PFC rectifier (solid line) as functions of output power.

parallel in Boost PFC) and the inductor loss.

Fig. 14 and 15 show the measured peak and average EMI of the conventional Boost PFC and the Two-boost-circuit PFC with the same EMI input filter respectively. As it can be seen from Fig. 14 the measured EMI value of the Boost PFC cannot satisfy the EN55022 requirements over the frequency range from 436kHz to 1.2MHz in low frequency domain. But can be seen from Fig. 15, the Two-boost-circuit PFC exhibits EMI

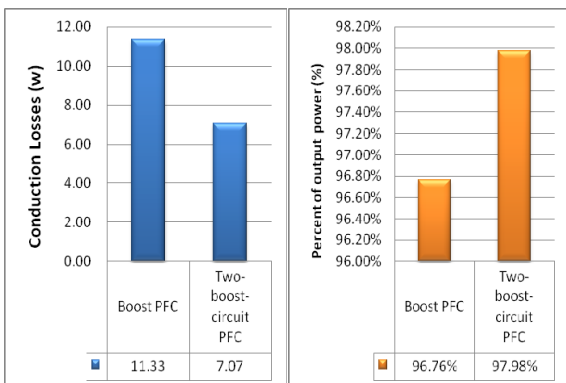


Figure 13. Simulation results of conduction losses and percent of output power at 85Vac input and 350W. Conduction losses (blue), percent of output power (orange).

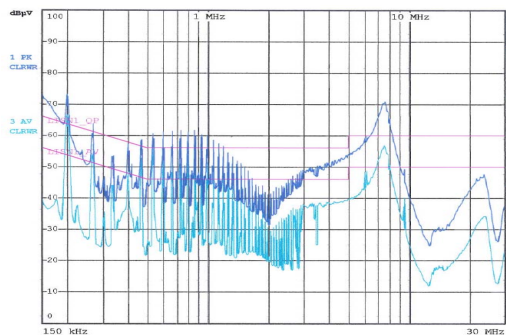


Figure 14. EMI measurement of conventional Boost PFC.

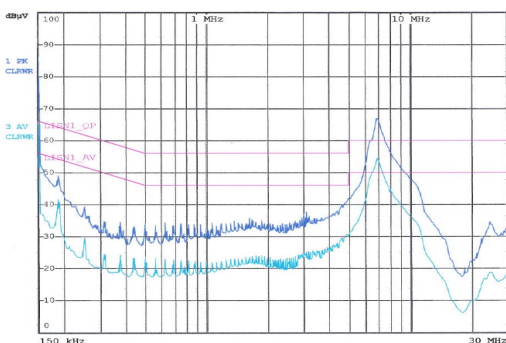


Figure 15. EMI measurement of Two-boost-circuit PFC.

reduction over the entire measured frequency range. Specifically, the measured peak EMI shows more than $10\text{dB} \leq V$ margin from the requirements over the entire

frequency range below 3MHz. This is because the two boost inductors in Two-boost-circuit PFC operate as a CM filter and reduce the CM noise.

V. CONCLNSION

In this paper, a review of Bridgeless Boost power factor correction (BLPFC) converters is presented. Performance comparison, including conduction losses analysis and common mode electromagnetic interference (EMI) argumentation, is analyzed between traditional Boost PFC converter and six members of Bridgeless PFC family. The simulation and experiment results show the advantages and disadvantages of all the Bridgeless PFC topologies clearly. It also shows the valid Bridgeless PFC topologies for industrial application.

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Research on Power Factor Correction Boost Inductor Design

Optimization – Efficiency vs. Power Density

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Abstract-- Nowadays, efficiency and power density are the most important issues for Power Factor Correction (PFC) converters development. However, it is a challenge to reach both high efficiency and power density in a system at the same time. In this paper, taking a Bridgeless PFC (BPFC) as an example, a useful compromise between efficiency and power density of the Boost inductors on 3.2kW is achieved using an optimized design procedure. The experimental verifications based on the optimized inductor are carried out from 300W to 3.2kW at 220Vac input.

Index Terms-- Boost Inductor; Optimization; Bridgeless PFC; Efficiency; Power Density

I. INTRODUCTION

With the increasing demands on Green Power Electronics in the global-world, more and more countries have been requiring the power supplies to meet certain standards in order to reduce their Electronics Pollutions to the Grid. Therefore, Power Factor Correction (PFC) converters have been picked up momentum, and novel Bridgeless PFC (BPFC) topologies have been invented to improve the performances and power density [1]–[5]. However, because of the native advantages - such as - easy circuit and system design, low cost, nice reduction of line harmonics currents, the Boost cell BPFCs still receive most attentions among all the BPFC topologies which came out during recent years.

Boost Inductors play a critical role in Boost type PFC converters. On one hand, it affects system efficiency through increasing or reducing semiconductor and magnetic losses depending on its value. On the other hand, assuming a fixed energy store, in the optimized design, the maximum flux density and the winding factor of the core are both on the boundary of limitations; therefore the volume of the inductor, which dominates power density of a PFC, will be determined by the inductance. Facing the biggest challenge in PFC design today – high efficiency vs. high power density, it is necessary to investigate the PFC inductor's operating characteristics and find out how it affects system's efficiency and power density. However, this has been difficult all the time, due to the lack of an effective way for designers to evaluate the overall performances of PFC inductors.

In order to optimize the inductor design in PFC converters, the questions below should be taken into consideration:

1. Is there any reasonable region to limit the Boost inductance for a certain PFC topology?

2. How to select windings and cores to minimize the magnetic losses while maintain high power density?

By answering these questions, in this paper, a useful balance between efficiency and power density of Boost inductor in a Two-Boost-Circuit BPFC is achieved using an optimized design procedure. Generally, based on this procedure, designers will be able to make a reasonable inductor design for any Boost type PFC topologies.

Section II is a brief introduction of high efficiency BPFC topologies. The design procedure is firstly illustrated and showed in a flowchart in section III. In section IV, functions between inductance and semiconductor losses are given with mathematical demonstration. Section V shows the method of getting a compromise of volume and efficiency of a Boost inductor. The relationship of inductance, inductor's volume and power losses is exhibited to clarify the method. In order to demonstrate and validate the procedure, the optimized Boost inductors were tested in the CCM Two-Boost-Circuit BPFC with an output power range from 300W to 3.2kW in section VI. Measured data of system efficiency are compared with those from the calculation based on the optimized design procedure. Section VII comes up with the conclusion.

II. HIGH EFFICIENCY BRIDGELESS PFC TOPOLOGIES

The idea of BPFC goes back to eighties [6]. Reference [7] shows the basic performances of some BPFC topologies. These topologies can be expected having higher efficiency than traditional Boost PFC due to the reduction of semiconductor numbers in current flowing path. Reference [8] gives a systematic comparison of five popular Boost-cell BPFCs and a conventional Boost PFC converter. Figs. 1 and 2 from reference [8] shows the EMI and efficiency performances of six PFC topologies based on simulation. According to its conclusion, Two-Boost-Circuit BPFC in Fig. 3 shows better performances than others due to the system efficiency improvement without inducing EMI problems.

In the Two-Boost-Circuit BPFC, during the positive AC line, diode D_1 operates when MOS S_1 turns off, and Boost inductor L_1 discharges, meanwhile giving energy to load. When MOS S_1 turns on, Boost inductor is charged, and diode D_1 is off. The output capacitor discharges and transfers energy to load. Line frequency diode D_3 returns the current from output to neutral and reduces common mode (CM) noise. In the negative AC line, the PFC works symmetrically.

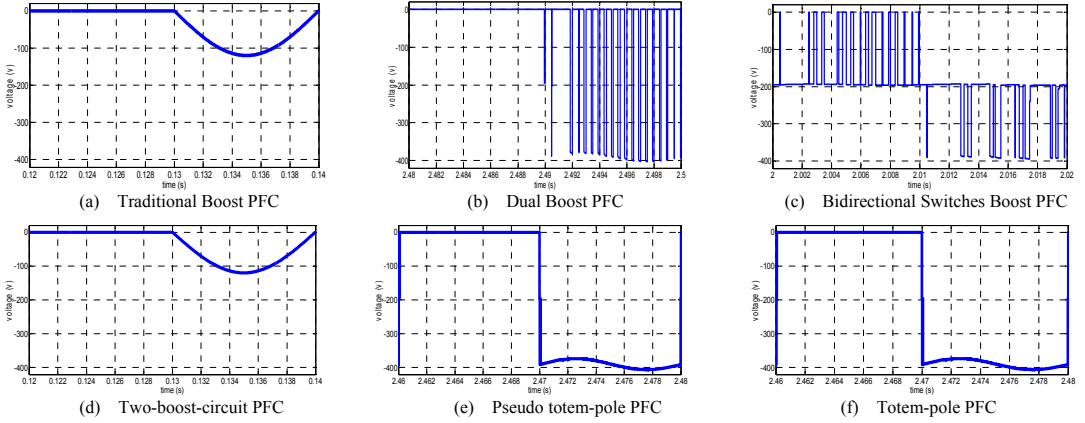


Fig. 1. CM voltage waveforms between power ground and the neutral of ac source showing the EMI comparison among the six PFC topologies [8].

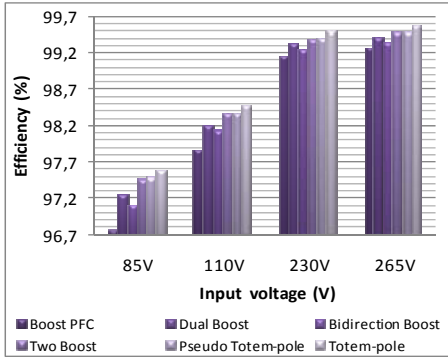


Fig. 2. Efficiency comparison only for conduction losses among six PFC topologies based on simulation [8].

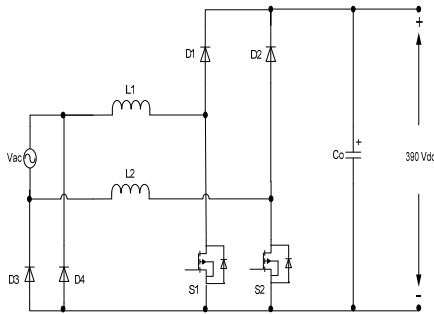


Fig. 3. Two-Boost-Circuit BPFC

If the PFC runs in continuous current mode (CCM), the average changing energy stored in the Boost inductors in each switching cycle should be approximate zero in steady states. So the input and output transfer function of BPFC in Fig. 3 is the same as a normal Boost PFC:

$$V_o = \frac{\sqrt{2} \times V_{in,rms} \times \sin(2\pi f_s t)}{1 - d(t)} \quad (1)$$

Where V_o is output voltage, $V_{in,rms}$ is AC rms input voltage, f_s is switching frequency and $d(t)$ is duty ratio varied with time.

III. BOOST INDUCTOR OPTIMIZATION PROCEDURE

Magnetic design is always a critical and complex part of PFC converters. A proper inductor design will not only increase the efficiency of whole system, but give a more compact and reliable PFC. However, the method for Boost PFC inductor design has been ambiguous for a long time due to the lack of effective way to evaluate the overall performances of PFC inductors. References [9] and [10] are application notes for various PFC inductors design from different well known manufacturers. In these materials, the design methods contain many experiential equations. Following these application notes will certainly lead to a quick PFC inductor design, but it is doubtable whether they have been optimized or not.

Reference [11] introduced another easy design method for PFC inductors using the “PL Product Curves”. Where, “PL” is the product of output power and Boost inductance. In this paper, the writer neglected some detailed magnetic factors which affect system performances for sure and also used many experiential results. Therefore, even this method made the inductor design easier; it is unclear if the “PL Curves” will help to get a suitable inductor design.

In order to overcome this tough problem, an optimization routine is carried out based on the high efficiency Two-Boost-Circuit BPFC in Fig. 3 operating in CCM. Its flowchart is in Fig. 4. Basically this routine can be used for any Boost type PFCs working in CCM as well.

In the optimization, considering the EMI requirement, it is a good idea to limit the switching frequency to a region from 50kHz to 70kHz to reduce the size of the EMI filter, as the filter’s size is mostly proportional to the peak amplitudes of harmonics with frequencies higher than 150kHz. Because the harmonics’ amplitudes attenuate with frequencies, it could be better to leave the maximum amplitudes of the harmonics (the first and second harmonics) with frequencies lower than 150kHz, beyond the frequency range of the EMI standard. In this way, the size of the EMI filter will be reduced with no doubt.

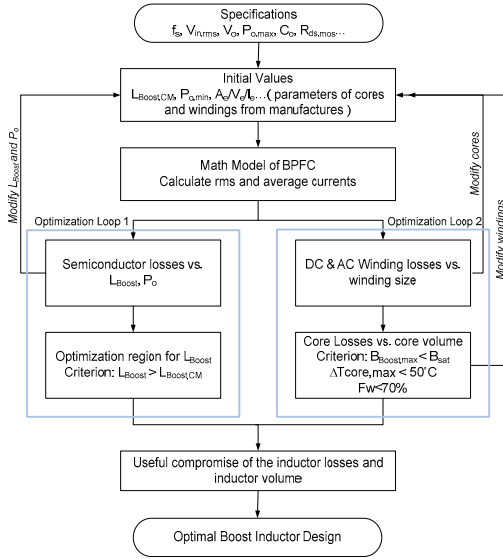


Fig. 4. Optimization procedure of inductor design in CCM for Two-Boost-Circuit BPFC with a balance of efficiency and power density.

The start point of this procedure is the specifications, which defining every fixed parameters in the main circuit. For example: input and output voltages, output peak power, output capacitors, inner parameters of the semiconductors and so on. Next, the important initial starting values of the PFC variables are set. Such as: minimal CCM Boost inductance $L_{B,CM}$, starting output power $P_{o,min}$, parameters of cores and windings from manufacturers. With all the specifications and initial values, the mathematical BPFC model will calculate the necessary rms and average currents flowing through all the components in the circuit, therefore semiconductor losses and inductor losses can be predicted.

Furthermore, inner optimization loop 1 seeks the characteristics of semiconductor losses vs. Boost inductance and output power, which will give a suitable region of Boost inductance at certain power level. And inner optimization loop 2 gets a compromise of volume and efficiency of the inductor. Both of the optimization loops will be explained in details in section IV and V. The optimal design can be realized by running optimization loop 1 and 2 together.

IV. OPTIMIZATION LOOP 1 – INDUCTANCE OPTIMIZATION

The mathematical model should be able to predict the rms and average currents of the BPFC for calculating losses. In Table I, the necessary normalized average and rms currents in one switching cycle running through the semiconductors of the BPFC in Fig. 3 are summarized under CCM and DCM conditions. Normalization process has been taken in order to make the comparison more clear. The normalization standards are given in Table II according to what were proposed in references [12] and [13]. Where the subscript “ n ” means normalized, T_L and T_s are line period and switching period, v and i are instant voltage and current in the PFC. Because the PFC is

working symmetrical, only the currents running in S_1 , D_1 and D_3 are discussed here. The derivations are described in details in the Appendix.

In Table I: d is the MOSFET on duty ratio; d_1 is the conduction duty ratio of the Boost diodes in DCM; $\Delta i_{L,n}$ is the inductor ripple current; the $i_{pk,n}$ is the peak inductor current in DCM; $i_{in,n}$ and $v_{in,n}$ are the normalized instant line current and voltage.

From Table I and II it can be seen: the semiconductor losses are as the functions of Boost inductance.

Fig. 5 displays the semiconductor loss ratio (including conduction and switching losses) as a function of the output power and Boost inductance when the input voltage is 220Vac and output voltage is 390V. Fig. 5 shows:

1. When increasing Boost inductance, at the beginning, the semiconductor losses reduce significantly. However, as soon as the Boost inductance reaches 0.6mH, the losses reduction vs. Boost inductance is not evident any more.
2. If the PFC operates in the variable load application, there will be a suitable region for Boost inductance selection. Inside this region, the PFC system should have relatively lower semiconductor losses and higher power density.

According to Fig. 5, we can see: it is not needed to use a very large Boost inductor to reduce semiconductor losses and components' stresses in Two-Boost-Circuit BPFC. An inductance range from 0.2mH to 0.6mH should be a suitable region for 300W up to 3.2kW application, because it will achieves a good balance between semiconductor losses and inductor volume. As the inductor's volume is approximately proportional to the inductance when the stored energy is constant [14]:

$$V_L = 0.5\alpha_V L I_L^2 \quad (1)$$

Where V_L is the inductor volume, α_V is a technical factor of the inductance and relates the volume to the stored energy.

TABLE I. CURRENTS OF SEMICONDUCTORS IN ONE SWITCHING CYCLE IN CCM AND DCM CONDITIONS FOR LOSSES CALCULATIONS

	$i_{S1,rms,n}$	$i_{D1,av,n}$	$i_{D3,av,n}$
CCM	$\sqrt{d(n) \left(i_{in,n}^2(n) + \frac{\Delta i_{L,n}^2(n)}{12} \right)}$	$(1-d(n)) i_{in,n}(n) $	$ i_{in,n}(n) $
DCM	$i_{pk,n} \cdot \sqrt{\frac{d(n)}{3}}$	$d_1(n) \frac{i_{pk,n}(n)}{2}$	$ i_{in,n}(n) $

TABLE II. NORMALIZED VOLTAGE, CURRENT AND INDUCTANCE

$v_n = \frac{v}{V_o}$	$i_n = \frac{i}{I_o}$	$L_n = L \frac{I_o}{V_o T_s}$
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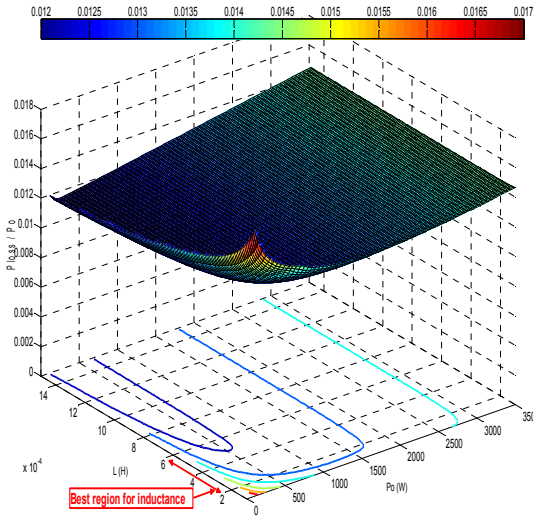


Fig. 5. Semiconductor loss ratio vs. Boost inductance and output power level

V. OPTIMIZATION LOOP 2 – INDUCTOR EFFICIENCY AND VOLUME OPTIMIZATION

Boost inductors occupies the majority of volume in PFC converters. In order to make a compact PFC converter, the inductor design should be paid high attention. Furthermore, the power losses in the inductors have a relationship with the inductors' size as well. In optimization loop 2, an optimized compromise between size and efficiency of a Boost inductor can be achieved.

A. Cores Selection

It is well known that the inductor losses come from core losses and winding losses. In order to predict the inductor losses, the first step is the core selection. A good core for Boost inductor must have high flux saturate limitation, low core losses and acceptable price. On the magnetic manufacturers' website, there will be very specific information about each core and its material, which can be used as references. In this design procedure, the Kool Mu E cores were chosen because of their advantages of high saturation level, relatively low core losses and cheaper to get. All the details of Kool Mu E cores will be defined as initial values at the beginning of the optimization procedure.

B. Winding Losses

Considering the winding losses, the DC part will keep the same in a constant power if the size and length of the winding is fixed; however the AC losses is more complex due to the skin and proximity effects. In this design, copper foil was used in order to decrease the proximity effect. Eqs. (2) - (5) give the functions of winding losses, switching frequency, layers and copper foil thickness [15]. Where, h is the thickness of copper foil, δ is skin depth, and ϕ is the ratio between copper thickness and skin depth.

$$P_w = \phi \cdot \left[G_1(\phi) + \frac{2}{3}(M^2 - 1)[G_1(\phi) - 2G_2(\phi)] \right] \times P_{dc} \quad (2)$$

$$\phi = \frac{h}{\delta} = \frac{h\sqrt{f_s}}{7.5} \quad (3)$$

$$G_1(\phi) = \frac{\sinh(2\phi) + \sin(2\phi)}{\cosh(2\phi) - \cos(2\phi)} \quad (4)$$

$$G_2(\phi) = \frac{\sinh(\phi)\cos(\phi) + \cosh(\phi)\sin(\phi)}{\cosh(2\phi) - \cos(2\phi)} \quad (5)$$

According to the equations above, Fig. 6 shows the increase of layer copper losses producing by proximity effect vs. ϕ and MMF force ratio m .

It can be seen in Fig. 6, with the factor ϕ and MMF ratio m increasing, the AC losses increase significantly. Therefore, copper foil can limit AC losses comparing to round windings due to the reduction of factor ϕ .

Since the methods for decreasing AC and DC losses are against each other - low AC losses asks for thin copper foils, but low DC losses requires thick copper foils, it is useful to find out which affects winding losses more. Assuming the switching frequency is 65kHz, and all the simulations are under the same condition: 220Vac input and 390V output at 3.2kW. Because the variation trend of inductor winding losses are independent on the cores, in Fig. 7, the inductor winding losses vs. thickness of copper foil (symbolized by h) and inductance are given for Kool Mu E core 5528E090 from Magnetics® as an example.

It can be seen that at the same inductance: on one hand, when the copper foil thicknesses increase, the total winding losses reduce due to DC losses reduction. That means in high power BPFC, DC winding losses dominate total winding losses. But on the other hand, the maximum inductance which can be wound on the core decreases as h getting thicker, that's because of the windows area limitation. However this will not worsen the semiconductor losses as long as carefully choosing the suitable inductance according to what has been mentioned in section IV.

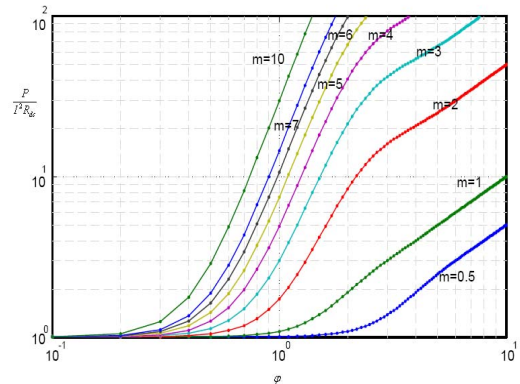


Fig. 6. Increase of layer copper losses producing by proximity effect as a factor ϕ and MMF force ratio m [14].

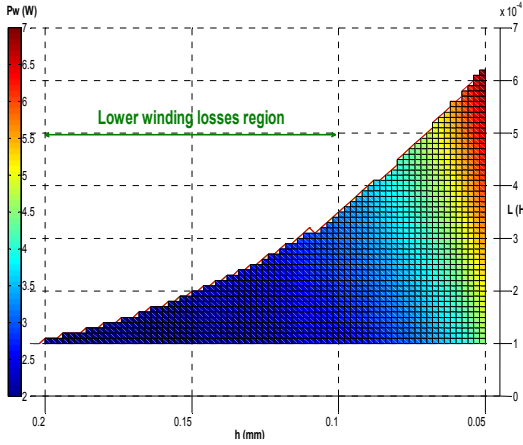


Fig. 7. Inductor winding losses vs. thickness of copper foil and inductance. The core is Kool Mu E core 5528E090 from Magnetics®.

Since the variation trend in winding losses will keep the same in different cores, considering the total amount of AC and DC losses reduction, h varies from 0.1mm to 0.2mm can be a good range for keeping lower winding losses.

C. Core losses

Eq. (6) gives the function of core losses, flux density, switching frequency and the volume of the Kool Mu E cores [16].

$$P_{core} = K_H f_s^\beta B_{av}^\alpha V_e \quad (6)$$

Where K_H , α and β are constant parameters, which are determined by the material of the core. V_e is the volume of the core.

B_{av} is the average flux density in the core during half line period. It can be calculated as below:

$$B_{av} = \frac{1}{N'} \sum_{n=1}^{N'} \frac{v_L(n) \cdot d(n)}{2N_e f_s} \quad (7)$$

Where the $v_L(n)$, $d(n)$ are the instant values of inductor voltage and switch duty ratio at each switching cycle. N is the turns of the inductor and A_e is cross section of the core. N' is the number of switching cycles in a half line cycle, which is the greatest integer of $f_s/2f_L$.

From Eqs. (6) and (7), Fig. 8 shows the core losses vs. Boost inductance for all the qualified Kool Mu E cores from Magnetics® [17]. In the legend on the top right corner, the cores were ranked by their sizes, the topper the smaller.

According to Fig. 8, it is clear that when the inductance increases, the core losses decrease due to the increase of turns.

Fig. 9 shows the total Boost inductor losses vs. inductance for different qualified Kool Mu E cores from Magnetics® when h equals to 0.13mm. From Fig. 9, comes to the conclusion:

1. At a constant power, the inductor losses have its minimal value while inductance increases.

2. The minimal inductor losses are affected by the cores. However, this relationship is not exactly the same as: the bigger the core, the lower the losses. It depends on several factors. Such as geometry of core, permeability, DC bias performances and temperature rising. For example, at the same inductance, core 5528E090 (43.1cm³) is smaller than 8020E040 (72.1cm³), but its inductor losses are lower due to its higher permeability.
3. Using core 5528E090 and 0.13mm copper foil, the highest power density and relatively low inductor losses can be achieved in the same system.

Table III shows the volumes of all the qualified E cores, their minimal inductor losses and power density at 3.2kW in Fig. 8. It should be noted; cores 7228E060 and 5530E090 could be also nice choices for higher efficiency but slightly lower power density applications. However, because they were very hard to get and cost too much, we didn't select them.

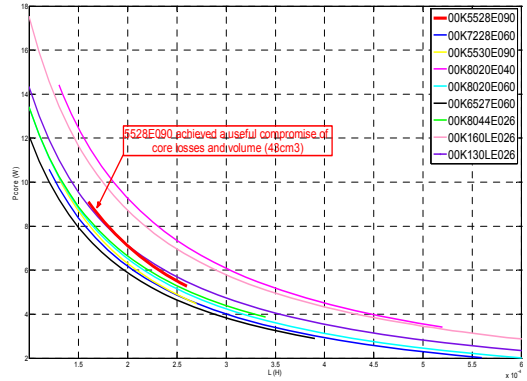


Fig. 8. Core losses vs. Boost inductance of all the qualified Kool Mu E cores from Magnetics®.

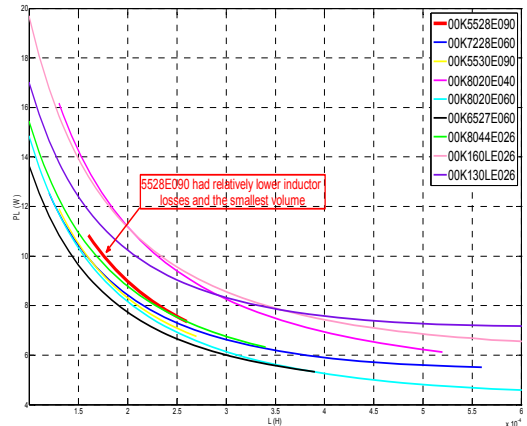


Fig. 9. Total inductor losses vs. Boost inductance for all the qualified Kool Mu E cores from Magnetics® when $h=0.13$ mm.

TABLE III. VOLUMES, LOSSES AND POWER DENSITY OF QUALIFIED KOOL MU E CORES FROM MAGNETICS®

Core Number	Volume (cm ³)	Min. P _L (W)	Power Density (W/cm ³)
00K5528E090	43.1	7.4	37.1
00K7228E060	50.3	5.5	31.8
00K5530E090	51.4	6.8	31.1
00K8020E040	72.1	6.1	22.2
00K8020E060	72.1	4.6	22.2
00K6527E060	79.4	5.3	20.2
00K8044E026	80.9	6.3	19.8
00K160LE026	212.0	6.6	7.5
00K130LE026	237.0	7.2	6.8

VI. EXPERIMENTAL VERIFICATION

According to section IV and V, the optimized Boost inductor parameters for the Two-Boost-Circuit BPFC in Fig. 3 at 3.2kW and 220Vac input can be: $L=0.23\text{mH}$, the copper foil is 0.13mm, using Kool Mu E core 5528E090 (volume is 43.1mm^3) for both high efficiency and high power density application. In experimental verification, MOSs were IPW60R045CP from Infineon®; Boost diodes were implemented with STPSC1206 SiC diode from ST®, and diodes STTH6004W from ST® were used as the return diodes. Compare the calculation data to the measurement results, the efficiency curves are given in Fig. 10 from 300W to 3.2kW. Fig. 11 gives the measured input voltage and current waveforms of this BPFC at 3.2kW.

In Fig. 10, the measured results match the calculated results very well above 1500W. However, in the low power level, the calculated efficiency is a little lower than measurement. That mainly comes from the inductor DC bias characteristics simulation. Because when the input power reduces, the Boost inductance increases due to its lower DC bias, which will cause semiconductor losses reduction. However, it is very difficult to achieve the exact DC bias curve of 5528E090, because of the insufficient core's information from manufacturer. The lower Boost inductance we predict in light load, the worse efficiency we get.

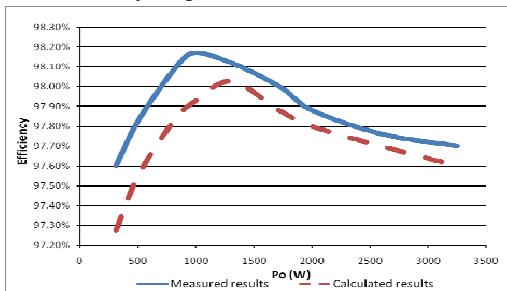


Fig. 10. Efficiency comparison of Two-Boost-Circuit BPFC at 220Vac input and 390V output using core 5528E090 from Magnetics®.

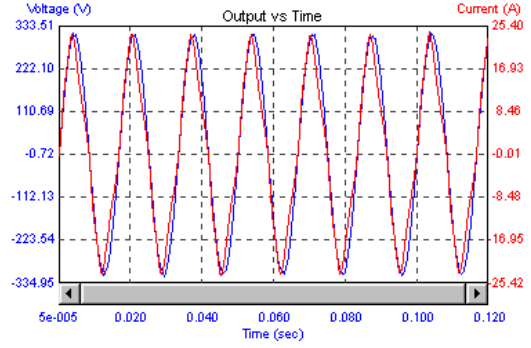


Fig. 11. Input voltage and current waveforms from Two-Boost-Circuit at 220Vac input and 390V output using core 5528E090 from Magnetics®. (PF=98.2%, Volt THD=1.1%)

It should be noted, although there were efficiency mismatches in Fig. 10, nevertheless, it can be concluded according to Fig. 10 and 11: the calculated data from the optimization design procedure will be valid to evaluate the performances of the Two-Boost-Circuit BPFC and give an optimized design between efficiency and power density of the Boost inductor.

VII. CONCLUSION

In this paper, an insight into the relationship of power, semiconductor losses, inductor losses and volumes based on a BPFC converter is given. The proposed optimization procedure is beneficial to properly compromise the efficiency and power density for Boost inductor design. Experimental verification from a 3.2kW Two-Boost-Circuit BPFC proved that the theoretical optimization procedure is applicable and can do benefits to a professional PFC design.

APPENDIX

In order to calculate system losses, the first step is to obtain the current waveform of Boost inductor. In CCM operation, its waveform during a switching cycle can be approximated as in Fig. 12. The normalized average Boost inductor current in the n th switching cycle is:

$$i_{LB,av,n}(n) = |i_{in,n}(n)| / I_o = I_{in,pk,n} \left| \sin(2\pi n \frac{T_s}{T_L}) \right| \quad (8)$$

$n = 1, \dots, N'$

Where T_s is the switching period, T_L is the line period.

The current ripple in Boost inductor in the n th switching cycle is determined as:

$$\begin{aligned} \Delta i_{LB,n}(n) &= \frac{|v_{in}(n)|}{I_o L_B(n)} \cdot d(n) \cdot T_s \\ &= \frac{|v_{in,n}(n)|(1 - |v_{in,n}(n)|)}{L_{B,n}} \end{aligned} \quad (9)$$

Where, d is the MOSFET on duty ratio. In CCM, the discrete time function is:

$$d(n) = 1 - \frac{v_{in}(n)}{V_o} = 1 - v_{in,n}(n) \quad (10)$$

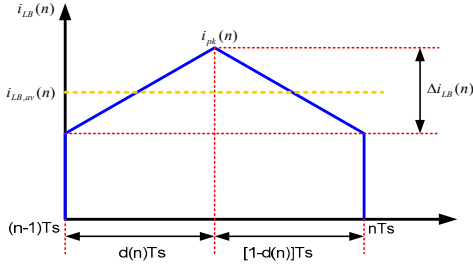


Fig. 12. Current waveform of Boost inductor in a switching cycle in CCM.

And,

$$L_B = L_{B0} \cdot \frac{A_{L,effi}}{A_{L,0}}, A_{L,effi} = f(Ni_{in}) \quad (11)$$

is the Boost inductance in different power. It is as a function of turns and input current due to the DC bias performance, which can be found in the data sheet of the cores [17].

The relevant rms and average currents for semiconductor losses calculation in CCM in the n th switching cycle are listed below:

$$i_{LB,rms,n}(n) = \frac{|i_{in}(n)|}{I_o} \cdot \sqrt{1 + \frac{1}{3} \left(\frac{\Delta i_{LB}(n)}{2i_{in}(n)} \right)^2} \quad (12)$$

$$= \sqrt{i_{in,n}^2(n) + \frac{\Delta i_{LB,n}^2(n)}{12}}$$

$$i_{S1,rms,n}(n) = \frac{|i_{in}(n)|}{I_o} \cdot \sqrt{1 + \frac{1}{3} \left(\frac{\Delta i_{LB}(n)}{2i_{in}(n)} \right)^2} \cdot \sqrt{d(n)}$$

$$= \sqrt{d(n) \left(i_{in,n}^2(n) + \frac{\Delta i_{LB,n}^2(n)}{12} \right)} \quad (13)$$

$$i_{D1,av,n} = (1-d(n)) \cdot \frac{|i_{in}(n)|}{I_o} = (1-d(n)) \cdot |i_{in,n}(n)| \quad (14)$$

$$i_{D3,av,n} = \frac{|i_{in}(n)|}{I_o} = |i_{in,n}(n)| \quad (15)$$

The same as the previous procedure, in DCM operation, its waveform during a switching cycle can be approximated as in Fig. 13. The normalized average current of Boost inductor in the n th switching cycle is the same as Eq. (8).

The MOSFET on duty ratio becomes:

$$d(n) = \sqrt{\frac{2(1-v_{in,n}(n)) \cdot i_{in,n}(n)}{v_{in,n}(n)}} \cdot L_{B,n} \quad (16)$$

And d_1 is the conduction duty ratio of the Boost diodes:

$$d_1(n) = \sqrt{\frac{2v_{in,n}(n) \cdot i_{in,n}(n)}{1-v_{in,n}(n)}} \cdot L_{B,n} \quad (17)$$

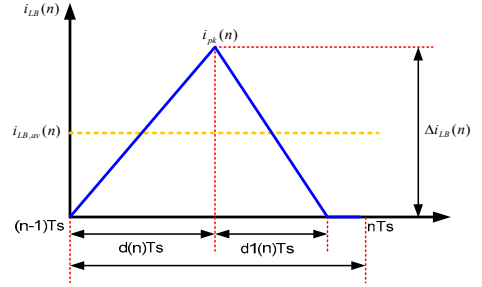


Fig. 13. Current waveform of Boost inductor in a switching cycle in DCM.

The $i_{pk,n}$ is the peak inductor current in DCM:

$$i_{pk,n}(n) = \sqrt{|i_{in,n}(n)| \cdot \frac{2|v_{in,n}(n)|(1-|v_{in,n}(n)|)}{L_{B,n}}} \quad (18)$$

The relevant rms and average currents for semiconductor losses calculation in DCM in the n th switching cycle are listed below:

$$i_{LB,rms,n}(n) = \sqrt{\frac{d(n)+d_1(n)}{3}} \cdot i_{pk,n}(n) \quad (19)$$

$$i_{S1,rms,n}(n) = i_{pk,n} \cdot \sqrt{\frac{d(n)}{3}} \quad (20)$$

$$i_{D1,av,n} = d_1(n) \cdot \frac{i_{pk,n}(n)}{2} \quad (21)$$

$$i_{D3,av,n} = \frac{|i_{in}(n)|}{I_o} = |i_{in,n}(n)| \quad (22)$$

For both CCM and DCM, the rms current flow through output capacitor is:

$$i_{Co,rms,n} = \frac{\sqrt{i_{LB,rms,n}^2(n) - i_{S1,rms,n}^2(n) - I_o^2}}{I_o} \quad (23)$$

And the corresponding normalized rms and average currents during a half line cycle are as below:

$$I_{X,rms,n} = \sqrt{\frac{1}{N'} \cdot \sum_{n=1}^{N'} i_{X,rms,n}^2(n)} \quad (24)$$

$$I_{Y,av,n} = \frac{1}{N'} \cdot \sum_{n=1}^{N'} i_{Y,av,n}(n) \quad (25)$$

Where, X symbolizes MOSs, Boost inductors and output capacitor, and Y represents Boost diodes and return diodes.

It should be noted that, since SiC Boost Diodes were used in our application, due to its excellent turn on and turn off characteristics, the switching losses can be ignored. Furthermore, even in the CCM condition, around the zero crossing of the line voltage, during a few switching cycles, the PFC operates in DCM inevitably, which was also taken into consideration during calculation in order to obtain a more precise prediction.

The CCM and DCM boundary condition happens when:

$$i_{in,n}(n) = 0.5\Delta i_{pk,n}(n) \quad (26)$$

Therefore, the time difference from the zero crossing of line voltage to DCM and CCM borderline position is also a function of inductance.

Besides, effects from temperature and current increasing which could change semiconductor and output capacitor losses were taken into consideration as well. The necessary functions can be found in the data sheet of each component [18] - [20].

ACKNOWLEDGMENT

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A Novel Bridgeless Power Factor Correction with Interleaved Boost Stages in Continuous Current Mode

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Abstract— The operation and trade-off of Bridgeless Power Factor Correction (BPFC) circuit with interleaved Boost stages are investigated. By using interleaved BPFC, an overall reduction of the size of EMI filter can be achieved without increasing the switching frequency of the converter. And higher efficiency can be expected in interleaved BPFC through the universal line input comparing with traditional BPFC. Furthermore, an optimization procedure is implemented to improve system power density. Analysis and simulation results taken from a 3.5kW peak interleaved BPFC completed this paper.

Keywords — Interleaved; Bridgeless; Power Factor Correction

I. INTRODUCTION

Bridgeless Power Factor Correction (BPFC) is a popular technique to achieve both unity power factor and high efficiency nowadays. Since the BPFC topologies have fewer semiconductors through current flowing path comparing to conventional Boost PFC, higher efficiency can be reached [1-3]. Paper [4] gives a systematic comparison of five most popular BPFCs and a normal Boost PFC, the Two-Boost-Circuit BPFC has better performances than all the other topologies by reducing its EMI without increasing semiconductor losses too much. Therefore, nowadays the Two-Boost-Circuit BPFC is the new favorite of many PFC designers.

Then main goal of this paper is to investigate the operation and design trade-offs of the Two-Boost-Circuit BPFC based on interleaved cells operating in continuous inductor current mode (CCM). In section II, the schematic and operating principles of the proposed 2-cell interleaved BPFC is given. Because the interleaved stages ask for 2 more Boost inductors than non-interleaved BPFC, section III implements an optimization routine to maximally reduce the size of each Boost inductor while maintaining high efficiency. Section IV analyzes and compares difference system performances of the non-interleaved BPFC and 2-cell interleaved BPFCs. It shows, the application of interleaved Two-Boost-Circuit BPFC results in an overall size reduction of differential mode (DM) EMI filter without reducing the system efficiency. Simulations taken from a 3.5kW peak interleaved Two-Boost-Circuit BPFC are given to complete this paper in section V. Section VI comes up with the conclusion.

II. SCHEMATIC AND OPERATING PRINCIPLES

Fig. 1 gives the traditional Two-Boost-Circuit BPFC. In Fig. 2, the extended topology of Fig. 1 is shown: a 2-cell interleaved Two-Boost-Circuit BPFC. And the characteristic waveforms of the circuit are in Fig. 3. In the

positive half line period, Boost inductor L_1 , L_2 , MOSs S_1 , S_2 and Boost diodes D_1 , D_2 work interleaved with a low frequency return diode D_5 returning current to Vac. In the negative half line period, the converter works symmetrically. Boost inductor L_3 , L_4 , MOSs S_3 , S_4 and Boost diodes D_3 , D_4 work interleaved with a low frequency return diode D_6 returning current to Vac. This topology can be expected higher efficiency than both Boost PFC and non-interleaved Two-Boost-Circuit BPFC, because: firstly, it doesn't need the freewheeling diodes rectifier and has 1 semiconductor less than Boost PFC in current flowing path; secondly, it uses multiple interleaved switching cells, which will reduce the MOS's conduction losses half of the non-interleaved one with the same power level. That is because interleaved cells share the input current.

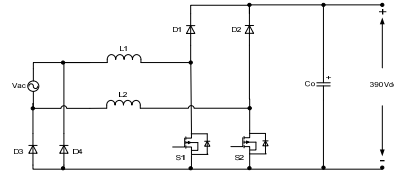


Figure 1: Non-interleaved Two-Boost-Circuit BPFC

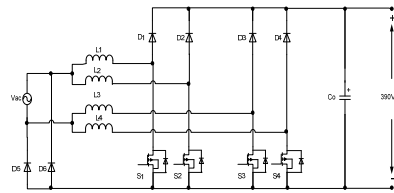


Figure 2: Interleaved Two-Boost-Circuit BPFC

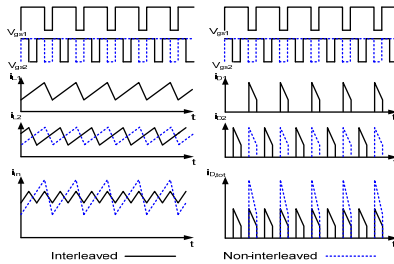


Figure 3: Switch states, inductor current and Boost diode current waveforms of interleaved and non-interleaved BPFC

III. OPTIMIZATION OF BOOST INDUCTORS

Magnetic component is always an important part of any kind of PFCs, and its performance will mainly dominate the reliability, efficiency and power density of the system [5]. Furthermore, due to the increased amount of Boost inductors in interleaved BPFC, in order to optimize the magnetic design to achieve the best balance between power density and system efficiency, an optimization routine for Boost inductor design is implemented.

A. Optimization Procedure

According to reference [6], a flow chart of the developed procedure for optimizing the Boost inductor for Two-Boost-Circuit BPFC systems is shown in Fig. 4. By implementing this simple and effective method, a compromise design of the volume and losses of the inductors can be reached for the 2-cell interleaved Two-Boost-Circuit BPFC in Fig. 2.

The start point of this procedure is the specifications, which defining every fixed parameters in the main circuit. For example: input and output voltages, output peak power, output capacitors, inner parameters of the semiconductors and so on. Next, the important initial starting values of the PFC variables are set. Such as: minimal CCM Boost inductance L_{BCM} , starting output power $P_{o,min}$, parameters of cores and windings from manufacturers. With all the specifications and initial values, the mathematical BPFC model will calculate the necessary RMS and average currents flowing through all the components in the circuit, therefore semiconductor losses and inductor losses can be predicted. Furthermore, inner optimization loop 1 seeks the characteristics of semiconductor losses vs. Boost inductance and output power, which will give a suitable region of Boost inductance at certain power level. And inner optimization loop 2 gets a compromise of volume and efficiency of the inductor. The optimal design can be realized by running optimization loop 1 and 2 together.

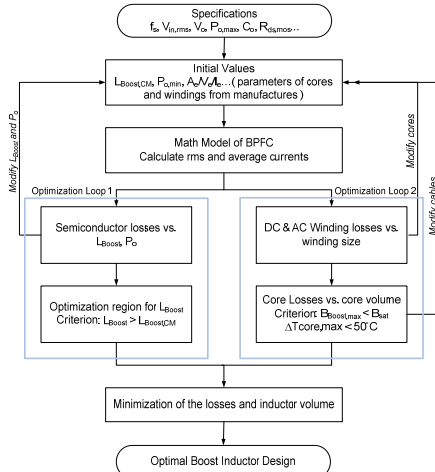


Figure 4: Flow chart of the optimization procedure of Boost inductor for trading off efficiency and power density [6]

B. Simulation results of optimization

Because the interleaved BPFC is working in a wide output power range from less than 500W up to 3.5kW for audio applications, it is important that the inductance reduction with power increasing will not affect the system efficiency a lot. This also means it will be very interesting to find out the relationship of Boost inductance and semiconductor losses in different power levels. Using the optimization procedure, Fig. 5 shows the relationship of Boost inductance versus semiconductor losses as a function of output power at low line: 85Vac input.

From Fig. 5, it can be seen: at the low line, after 500W, for a fixed power level, the increasing of inductance can not reduce semiconductor loss ratio anymore. That is because: comparing to the input current, the variance of input ripple current is too small, it will not affect the semiconductor loss ratio very much. However, since the light load operation power is below 500W, the inductance at low power should be bigger enough to limit the semiconductor losses increasing when the Boost inductance reducing. Therefore, to select an inductance about 0.2mH at 300W is a good choice to gain lower semiconductor losses in a wide output power range.

It is well known, winding losses include DC losses and AC losses [5]. To further reduce the winding losses, copper foils were used. Using the same derivation method in paper [6], Fig. 6 gives the winding losses versus the thickness of copper foil and Boost inductance at 3.5kW output and 85Vac input. Fig. 6 tells: firstly, the winding losses are dominated by DC winding losses; secondly, the most useful thickness of the copper foil can be from 0.15mm to 0.2mm. Thicker copper foil is not very necessary, due to it occupies lots of window areas in the core but cannot reduce the winding losses very much.

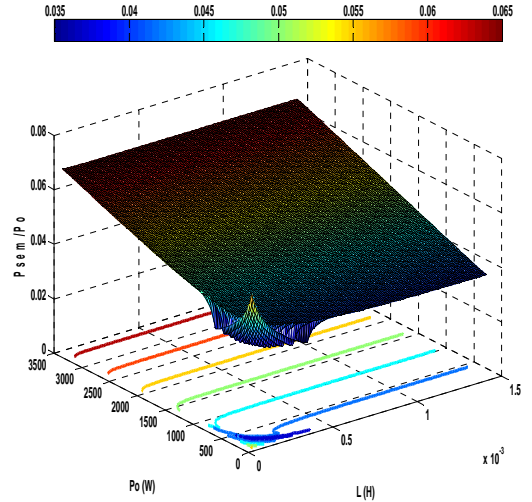


Figure 5: Semiconductor losses vs. input voltage and Boost inductance of interleaved BPFC

Take the relatively low core-loss Kool Mu cores as an example, Fig. 7 shows the total inductor losses vs. Boost inductance for all the qualified Kool Mu E cores from Magnetics®, when the thickness of copper foil h is 0.15mm and 85Vac input at 3.5kW. In the legend on the top right corner, the cores were ranked by their sizes, the topper the smaller.

Take both of the efficiency and power density requirements into consideration, the optimized parameters for the 2-cell interleaved Two-Boost-Circuit BPFC Boost inductor design are listed in Table I. Where, P_{core} is core losses and $P_{winding}$ means winding losses.

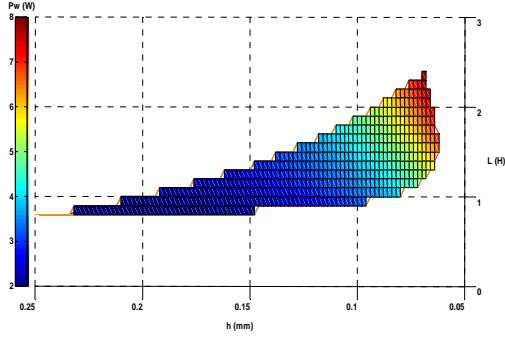


Figure 6: Winding losses vs. copper foil thickness and Boost inductance of interleaved BPFC

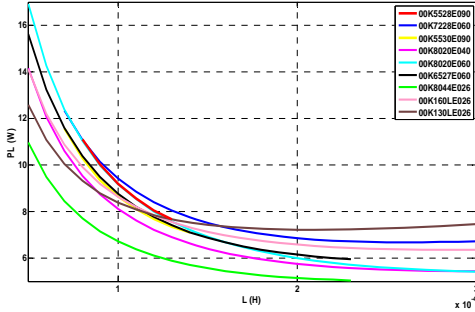


Figure 7: Inductor losses vs. output power and Boost inductance of interleaved BPFC

Table I. One of the optimized parameters for Boost inductor design with high efficiency and power density

Core No.	Copper foil h (mm)	$P_{core}/P_{winding}$ at 3.5kW	Temp- Rapture rise (°C)	Inductance at 300W (mH)
5528E090	0.15	62.32%	60	0.22

IV. INTERLEAVED AND NON-INTERLEAVED BPFCs PERFORMANCES COMPARISON

Since the currents in the converter mainly dominate the system performances such as EMI and efficiency, one can simply judge the advantages and disadvantages of a system by its currents. Table II gives the RMS currents of the Boost inductor, MOS, Boost diode and the high-frequency (HF) line current in the 2-cell interleaved Two-

Boost-Circuit BPFC, non-interleaved Two-Boost-Circuit BPFC with equal inductance and non-interleaved Two-Boost-Circuit PFC with equal HF RMS current according to the system parameters below:

$$V_{in,rms} = 85V \quad L_1 = L_2 = L_3 = L_4 = 0.13mH$$

$$V_o = 390V \quad P_o = 3.5kW \quad f_s = 65kHz \quad f_{line} = 50Hz$$

Table II. Different RMS currents in interleaved and non-interleaved Two-Boost-Circuit BPFC topologies

PFC topologies	Interleaved BPFC (case 1)	Non- interleaved with equal inductance (case 2)	Non- interleaved with equal HF RMS current (case 3)
Boost inductance (mH)	0.13	0.13	0.19
MOS current (A)	17.71	35.39	35.39
Diode current (A)	10.54	21.07	21.06
Inductor current (A)	20.61	41.19	41.18
HF line current (A)	4.63	6.83	4.63

From Table II, it is obviously to find out that:

1. At the same inductance, the HF RMS line current of the non-interleaved BPFC is 1.48 times greater than that of the interleaved BPFC, which means that: the EMI filter of non-interleaved BPFC must provide higher attenuation at switching frequency than interleaved BPFC.
2. At equal HF RMS line current, the inductance value of the non-interleaved BPFC is 1.46 times greater than that of interleaved BPFC. If the design of the inductor has been optimized, increasing the inductance will certainly lead a higher volume for non-interleaved BPFC [2] and [6].
3. The semiconductor conduction losses of the interleaved BPFC are always lower than non-interleaved BPFC due to it shares the current between the two stages. Therefore, interleaving stages will increase the system efficiency.

It would be also nice to point out that: although papers [7-8] have presented that more interleaved stages, larger range of duty ratios experiencing near-total input current ripple cancellation; unless it is really necessary, by increasing the number of stages, it will quickly enlarge the size of the whole system, the limited reduction of magnetic and filter volumes may disappear. On the other hand, increasing interleaved stages will also be accompanied with increasing circuit complexity and leading to higher cost and reducing system reliability as well.

V. SIMULATION RESULTS

According to the system parameters shown in section IV, simulate the BPFCs without input filters at 3500W and 85V input. Fig. 8 gives the line voltage and current of the interleaved BPFC in case 1. Fig. 9 gives the spectrum

of input current ripple of interleaved BPFC in case 1 and non-interleaved BPFC in case 2. Fig. 10 shows the input current ripple of both interleaved BPFC in case 1 and non-interleaved BPFC with equal inductance in case 2 in half line period. From Figs. 9 and 10, it can be seen, the interleaved stages reduce the input ripple current, which will do benefit to DM EMI filter reduction.

After carefully choosing the components, Fig. 11 shows the system efficiency comparison of the three BPFCs in Table II, when the output power increases from 200W to 3.5kW. Where, MOSs are IPW60R045CP from Infineon[®]; Boost diodes are implemented with STPSC1206 SiC diode from ST[®], and diodes STTH6004W from ST[®] are used as the return diodes. The Magnetics cores for the Boost inductors L are 5528E090 (volume: 43.1cm³) in interleaved BPFC in case 1, 5530E090 (volume: 51.4cm³) in non-interleaved BPFC in case 2 and 82020E060 (volume: 72.1cm³) for non-interleaved BPFC in case 3. The 0.15mm copper foil was used for winding. Finally, the high voltage aluminum capacitor (1000 μ F, 400VDC) is used for bulk capacitor. It should be noted that: although the interleaved BPFC in case 1 has higher number of Boost inductors, it will not increase the total core size a lot comparing to the non-interleaved BPFC. That is because: the inductor current of the non-interleaved BPFC is two times higher than which in 2-cell interleaved BPFC in case 1. Therefore, the higher inductor losses and temperature rising enlarge the core size significantly.

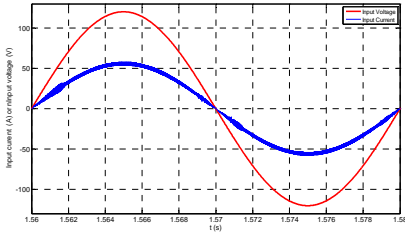


Figure 8: Input voltage (red 50V/div), input current (blue 50A/div) of the interleaved BPFC

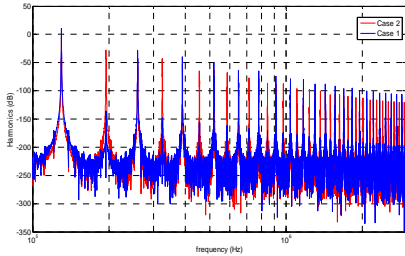


Figure 9: Spectrum of input current ripple of the interleaved BPFC in case 1 (blue) and non-interleaved BPFC in case 2 (red)

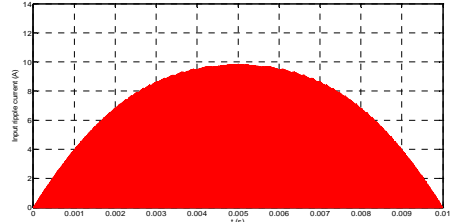
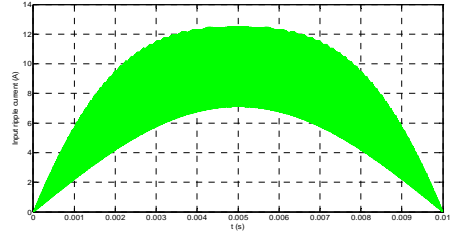


Figure 10: Input ripple current of interleaved BPFC in case 1 (green), non-interleaved BPFC equals inductance in case 2 (red)

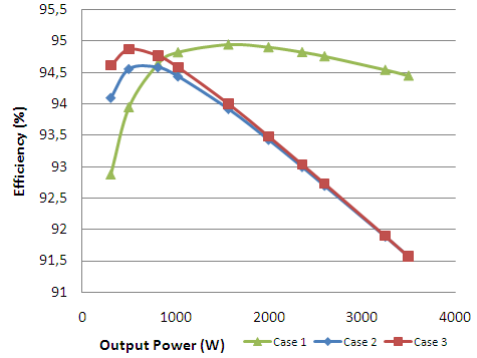


Figure 11: Efficiency comparison for three BPFCs in Table II

In Fig. 11, it can be seen that the interleaved Two-Boost-Circuit BPFC has higher efficiency comparing with the non-interleaved BPFCs after 1kW due to the semiconductor losses dominate the total system losses in high power level.

VI. CONCLUSION

Interleaving BLPFC is a useful novel topology, which can increase the power density of the converter by reduction the size of EMI filter without increasing system losses dissipation. With the properly designing of the magnetic components in the interleaved BPFC converter, a trade off between high efficiency and high power density can be achieved.

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Research on EMI Reduction of Multi-stage Interleaved Bridgeless Power Factor Corrector

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Abstract— Working as an electronic pollution eliminator, the Power Factor Corrector's (PFC) own Electromagnetic Interference (EMI) problems have been blocking its performance improvement for long. In this paper, a systematic research on EMI generation of a multi-stage Two-Boost-Circuit Interleaved Bridgeless PFC (IBPFC) is presented. The insight into relationship of interleaving stages, switching on/off oscillations and EMI reduction is discussed. Finally, a 3.5kW universal input 2-stage IBPFC prototype was built to verify the theoretical analysis. Experimental results show that significant EMI reductions at odd harmonics can be achieved by carefully designing the BPFC using interleaving technique.

I. INTRODUCTION

In order to develop the environment-friendly power electronics and reduce their pollutions to power grid, the active Power Factor Corrector (PFC) is always implemented in front of kinds of power converters. As one of the major optimal solutions of power quality improvement nowadays, the high efficient Bridgeless Power Factor Corrector (BPFC) have attracted lots of attentions [1-5]. For reducing the high electromagnetic pollution of BPFC due to fast switching on and off of the semiconductors, the interleaved BPFCs (IBPFCs) have recently been researched [6-8]. One possible architecture of IBPFC system is shown in Fig. 1, which is an extension version from Two-Boost-Circuit BPFC in Fig. 2. It is well-known that using interleaved technique, the EMI emission can be reduced. However, how much attenuation the BPFC can gain from interleaving stages is unclear. This work presents the insight into relationship of number of interleaved stages, switching on/off oscillations and EMI cancellation is discussed and proved by both simulation and experimental results. Furthermore, although the analysis is only based on Two-Boost-Circuit IBPFC, the idea can be extended to any other PFCs.

In the paper, the main advantages of IBPFC converters are firstly briefly introduced in Section II. In order to predict the EMI performances correctly, the common-mode (CM) and differential-mode (DM) EMI generation models for an N -stage IBPFC are derived in Part A of Section III. The discussion on EMI reduction relates to number of interleaved stages and switching on/off oscillations is presented in Part B and C in Section III. Experimental results are carried out in Section IV. Finally, Section V comes to the conclusion.

II. IBPFC INTRODUCTION

The very popular BPFC topologies goes back to eighties [9]. References [3, 4] showed the basic performances of several well-known BPFC topologies. According to what has been proved in reference [4], compare to the traditional Boost PFC, one line frequency diode can be omitted in the current flowing path of BPFCs. Paper [4] also gave the detailed comparisons on EMI and semiconductor losses of five popular BPFCs and a conventional Boost PFC. In its conclusion, the Two-Boost-Circuit BPFC in Fig. 2 shows better performances than others due to enhancing system efficiency without increasing EMI.

With the requirement of increasing power level, instead of simply paralleling several BPFCs together, during recent years, interleaved BPFCs is becoming more and more common. The latest publications [7] and [8] give the optimal design of a high efficient 2-stage IBPFC in Fig. 3. This novel topology can be expected to have better EMI performance comparing to the non-interleaved BPFC due to EMI cancellation.

Taking the multi-stage IBPFC in Fig. 1 as an example, the rest sections will give the detailed analysis on how do the interleaved stages and switching oscillations affect EMI cancellation in IBPFC systems.

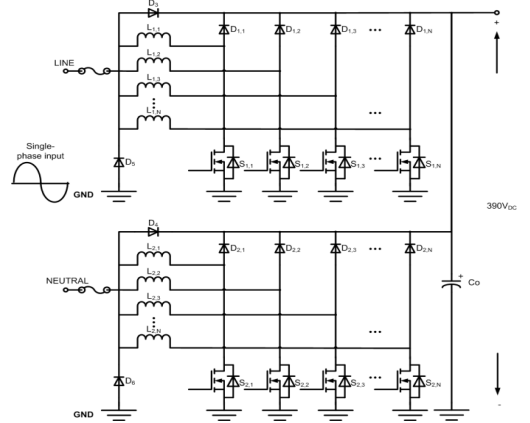


Fig. 1 Possible architecture of multi-stage IBPFC system

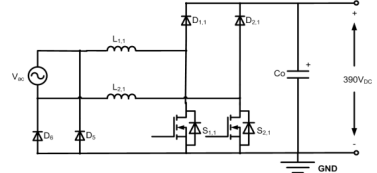


Fig. 2 Traditional non-interleaved Two-Boost-Circuit BPFC

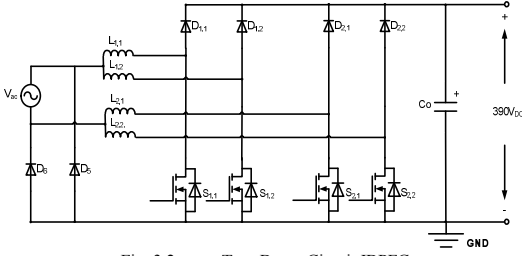


Fig. 3 2-stage Two-Boost-Circuit IBPFC

III. MULTI-STAGE INTERLEAVED BPFC

A. EMI Noise Sources Modelling

Because the N -stage interleaved BPFC (IBPFC) in Fig. 1 works symmetrically, only the positive ac period is considered here. In the positive half period, Boost inductors $L_{1,i}$, MOSs $S_{1,i}$ and Boost diodes $D_{1,i}$ work interleaved with D_0 returning current to V_{ac} . Where, i symbolized the number of interleaved stages ranging from 1 to N . One of the major reasons for using IBPFC is EMI cancellation. However, since the PFC converter has variable on duty ratios, the high frequency ripple current can NOT cancel completely all the time [10]. In order to explain how exactly the EMI reduction varies with the number of interleaved stages increasing, it is better to analysis the CM and DM noises of the interleaved BPFC separately. However, it should be noticed that the real EMI performances typically depend strongly on the circuit layout, semiconductor characteristics, gate drivers, operating currents, voltages and temperature and parasitic elements. The actual EMI performances above 1MHz are very difficult to simulate. Therefore, in this paper, only the frequency noises below 1MHz are taken into consideration. Furthermore, the model of EMI receiver is not considered neither.

Start from the 2-stage IBPFC in Fig. 3, steps of DM EMI modeling of a multi-stage IBPFC is given in Fig. 4.

- Step 1: Using the symmetrical operation structure to simplify the topology.
- Step 2: Because the output filter capacitor can be considered as a short circuit in high frequency, and the return diode D_0 is always on in the positive AC period, the two components can be ignored.
- Step 3: Simplify the semiconductor components and the Boost inductors. In high frequency domain, the Boost inductors charge and discharge through MOSs and Boost diodes, therefore, they can be considered as 2 triangle current sources.
- Step 4: Extend the DM EMI model from 2-stage to N -stage by interleaving N DM noise sources together. All the triangle current sources are $360^\circ/N$ phase shift. Where, N is the number of multi-stage interleaved modules. **When N equals to 1, it symbolizes the non-interleaved BPFC.**

Following the same steps, the CM model of the N -channel IBPFC is shown in Fig. 5.

B. EMI Cancellation Analysis

The mathematical derivation of the CM and DM noise sources in Fig. 4 and 5 are as follows. Assuming the n th order CM and DM noise of the first interleaving stage have a function of:

$$\begin{cases} V_{CM,1}(n\omega_o) = A_n e^{j\varphi_n} \\ I_{DM,1}(n\omega_o) = \frac{B_n}{N} e^{j\Phi_n} \end{cases} \quad (1)$$

Where, the ω_o is the fundamental angular frequency, A_n and B_n are the CM and DM harmonics' amplitudes of non-interleaved BPFC, and φ_n and Φ_n are the initial phases of the n th harmonics. Therefore, the n th order CM and DM noise sources of the N th interleaving stage are:

$$\begin{cases} V_{CM,N}(n\omega_o) = A_n e^{j(\varphi_n - \frac{2\pi n(N-1)}{N})} \\ I_{DM,N}(n\omega_o) = \frac{B_n}{N} e^{j(\Phi_n - \frac{2\pi n(N-1)}{N})} \end{cases} \quad (2)$$

According to the superposition principle, the sum of the n th order CM and DM noises from the N -stage IBPFC can be expressed as:

$$V_{CM,tot}(n\omega_o) = \frac{1}{N} \sum_{i=1}^N V_{CM,i}(n\omega_o) \quad (3)$$

$$= \frac{A_n}{N} \left[\sum_{k=1}^N \cos(\varphi_n - \frac{2\pi n(k-1)}{N}) + j \sum_{k=1}^N \sin(\varphi_n - \frac{2\pi n(k-1)}{N}) \right]$$

$$I_{DM,tot}(n\omega_o) = \sum_{i=1}^N I_{DM,i}(n\omega_o) \quad (4)$$

$$= \frac{B_n}{N} \left[\sum_{k=1}^N \cos(\Phi_n - \frac{2\pi n(k-1)}{N}) + j \sum_{k=1}^N \sin(\Phi_n - \frac{2\pi n(k-1)}{N}) \right]$$

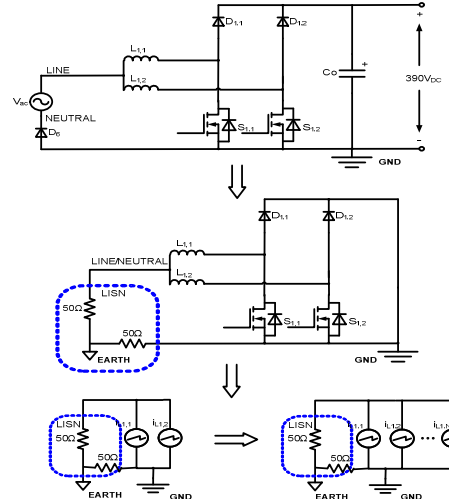


Fig. 4 DM EMI modelling process of the N -stage Two-Boost-Circuit IBPFC

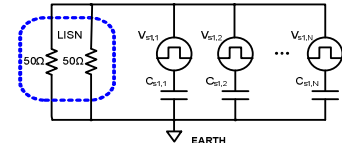


Fig. 5 CM EMI modelling of the N -stage Two-Boost-Circuit IBPFC

Assuming $\Phi_n = \varphi_n = 0$, Eqs. (3) and (4) can be simplified as:

$$V_{CM,tot}(n\omega_o) = \frac{1}{N} \sum_{i=1}^N V_{CM,i}(n\omega_o) \quad (5)$$

$$= \frac{A_n}{N} \left[\sum_{k=1}^N \cos\left(\frac{2\pi i(k-1)}{N}\right) - j \sum_{k=1}^N \sin\left(\frac{2\pi i(k-1)}{N}\right) \right]$$

$$I_{DM,tot}(n\omega_o) = \sum_{i=1}^N I_{DM,i}(n\omega_o) \quad (6)$$

$$= \frac{B_n}{N} \left[\sum_{k=1}^N \cos\left(\frac{2\pi i(k-1)}{N}\right) - j \sum_{k=1}^N \sin\left(\frac{2\pi i(k-1)}{N}\right) \right]$$

From eqs. (1) and (5), the amplitude ratio of n th order CM noise of the N -stage interleaved and non-interleaved BPFC is:

$$\alpha(n\omega_o) = \frac{|V_{CM,tot}(n\omega_o)|}{|V_{CM,non}(n\omega_o)|} \quad (7)$$

$$= \frac{1}{N} \left| \sum_{k=1}^N \cos\left(\frac{2\pi i(k-1)}{N}\right) - j \sum_{k=1}^N \sin\left(\frac{2\pi i(k-1)}{N}\right) \right|$$

similarly, from Eqs. (1) and (6), the amplitude ratio of n th order DM noise of the N -stage interleaved and non-interleaved BPFC is:

$$\beta(n\omega_o) = \frac{|V_{DM,tot}(n\omega_o)|}{|V_{DM,non}(n\omega_o)|} \quad (8)$$

$$= \frac{1}{N} \left| \sum_{k=1}^N \cos\left(\frac{2\pi i(k-1)}{N}\right) - j \sum_{k=1}^N \sin\left(\frac{2\pi i(k-1)}{N}\right) \right|$$

Where, $V_{CM,tot}(n\omega_o)$ and $V_{DM,tot}(n\omega_o)$ are the n th order CM and DM harmonics of the N -stage IBPFC; $V_{CM,non}(n\omega_o)$ and $V_{DM,non}(n\omega_o)$ are the n th order CM and DM harmonics of non-interleaved BPFC.

By using the Orthogonality principle:

$$\begin{cases} \alpha(n\omega_o) = \beta(n\omega_o) = 0, n \neq c \cdot N \\ \alpha(n\omega_o) = \beta(n\omega_o) = 1, n = c \cdot N \end{cases} \quad (9)$$

Where c is the positive integer serials starts from 1.

Hence, the amplitudes of high switching frequency noises from both CM and DM sources can be solved as below:

$$\begin{cases} |V_{CM,tot}(n\omega_o)| = 0, n \neq c \cdot N \\ |V_{CM,tot}(n\omega_o)| = |V_{CM,non}(n\omega_o)|, n = c \cdot N \end{cases} \quad (10)$$

$$\begin{cases} |I_{DM,tot}(n\omega_o)| = 0, n \neq c \cdot N \\ |I_{DM,tot}(n\omega_o)| = |I_{DM,non}(n\omega_o)|, n = c \cdot N \end{cases} \quad (11)$$

From Eqs. (10) and (11), it can be concluded that:

1. Interleaved stages help to improve both CM and DM EMI.
2. In an N -stage IBPFC, except the $c \times N$ times fundamental frequencies, all the rest harmonics reduced due to the phase shift.
3. The more interleaved stages the IBPFC has, the more high frequency harmonics will be reduced.
4. The switching frequency f_s affects the design of the EMI filter of IBPFC due to the noises cancellation do

NOT happen at $c \times N$ times fundamental frequencies. In order to maintain the EMI advantage of IBPFC, it is better to select its switching frequency based on the range of conduction EMI measurement. Implementing the European Standard EN55013, the disturbance voltage at mains terminals in the frequency range from 150kHz to 30MHz needs to be attenuated to fulfill the EMI limitation [11]. **Therefore, the first harmonic of the IBPFC, which locates inside the range of the standard, should be better not to equal to $c \times N$ times of fundamental frequencies.** The mathematic expression is:

$$\left\lceil \frac{150\text{kHz}}{f_s} \right\rceil \neq c \cdot N \quad (12)$$

Where f_s is the switching frequency, and ' $\lceil x \rceil$ ' is the ceiling function, which returns the smallest integer not less than x . From Eq. (12) it can also be found, the IBPFCs usually require higher cut-off frequency of the EMI filter comparing to the non-interleaved one with the same EMI attenuations when f_s is higher than 150kHz.

Fig. 6 is the simulations of CM and DM EMI comparison between a 2-stage interleaved and a non-interleaved Two-Boost-Circuit BPFC, when the f_s is 75kHz. Because the 2nd harmonic (150kHz) is the first harmonic which locates inside the EMI standard's frequency range, and it cannot be cancelled by interleaving. (150kHz equals to the $c \times N$, when c is 1.) Therefore, the same as Eq. (12) has proved, the cut-off frequency of the EMI filter in this 2-stage IBPFC requires the same as the non-interleaved BPFC.

C. Switching on/ off and Oscillation Analysis

In the previous EMI models in part B, both of the rise/fall times and the oscillations of the switching are neglected. However, in the real power electronics systems, these effects normally cannot be avoided. Consider the oscillating drain to source single of MOS (the blue curve) in Fig. 7, and assume rise time equals to fall time. The real V_{DS} signal can be defined with:

$$V_{DS}(t) = \begin{cases} \frac{V_{DS}}{t_r} t, & 0 \leq t \leq t_r \\ V_{DS} + V_{pp} e^{-\gamma} \sin[2\pi f_o(t - t_r)], & t_r < t \leq \delta T_s \\ \frac{-V_{DS}}{t_r} (t - \delta T_s - t_r), & \delta T_s < t \leq \delta T_s + t_r \\ -V_{pp} e^{-\gamma(t - \delta T_s - t_r)} \sin[2\pi f_o(t - t_r - \delta T_s)], & \delta T_s + t_r < t \leq T_s \end{cases} \quad (13)$$

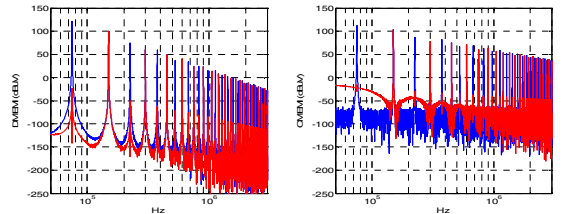


Fig. 6 DM (left) and CM (right) EMI comparison of 2-stage interleaved (red) and non-interleaved (blue) Two-Boost-Circuit BPFC at 75kHz and 3.5kW

Where t_r is the switching rise and fall time, V_{DS} is a 390V constant drain to source voltage on MOS, T_s is switching period, V_{pp} is the oscillating peak voltage, γ is attenuation factor of the oscillation, δ is MOS's on duty ratio and f_o is the oscillating frequency. Implement Fast Fourier Transform (FFT), the frequency spectrums of Fig. 7 is shown in Fig. 8. From Fig. 8, it can be seen: the switching rise/fall times and oscillations rarely affect the EMI emission before the oscillating frequency and will not do harm to the low frequency EMI reduction caused by interleaved stages.

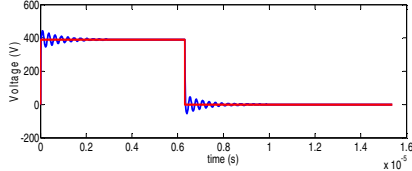


Fig. 7 Comparison of the oscillating V_{DS} (blue) and the ideal V_{DS} (red) when: $t_r = 20\text{ns}$; $\delta = 0.41$; $\gamma = 1.25\text{ MHz}$; $V_{pp} = 0.15V_{DS}$; $f_o = 3.6\text{ MHz}$.

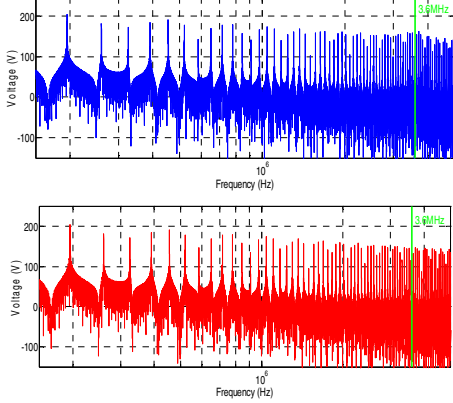


Fig. 8 Comparison of FFT of the oscillating V_{DS} (blue) and the ideal V_{DS} (red)

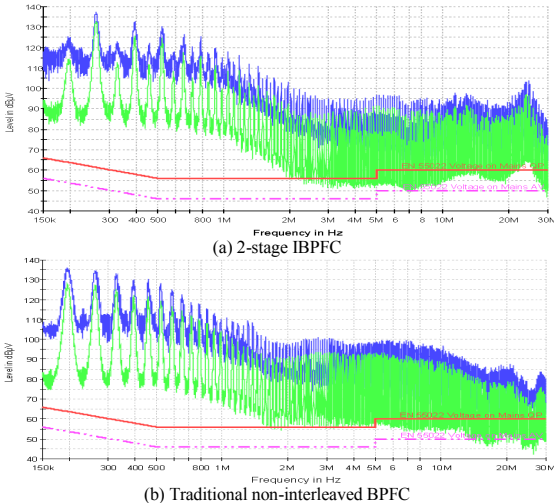


Fig. 9 EMI comparison of 2-stage IBPFC and non-interleaved BPFC at one eighth of full power and 230Vac input

IV. EXPERIMENTAL VERIFICATION

Considering the design complexity and cost of multi-stage IBPFCs, a 2-stage 65kHz 390Vdc IBPFC for audio application was built for experimental verification. According to the special EMI requirement from audio systems, Fig. 9 gives the EMI measurement results of the 2-stage IBPFC and a traditional BPFC at one eighth of the full power. In order to make a fair comparison, all the components and testing equipments selected for the 2 topologies are the same. From Fig. 9, it is clear that in the 2-stage IBPFC, all the peak amplitudes of odd order harmonics have been reduced due to phase shift. However, according to what have been proved in Eqs. (10) and (11) in Section III, in the 2-stage IBPFC, all the odd harmonics should be completely cancelled, not only reduced. One reason for the difference between calculation and measurement is that: in the calculation, we don't consider the affect of EMI receiver. In the real measurement, the EMI receiver has a 9kHz resolution bandwidth (RBW) filter, which collects all the harmonics' amplitudes around the sweeping frequencies within the 9kHz bandwidth. So, it is impossible for the equipment to measure the exactly amplitude of any harmonic at one frequency point. But in the mathematical analysis in Section III, all the calculations relate to one frequency point. Anyhow, the 2-stage IBPFC still shows significant EMI reduction at odd harmonics.

V. CONCLUSIONS

In this paper, a systematic research on EMI generation of multi-stage IBPFC is presented by modeling its CM and DM noises. The insight into relationship of interleaving stages, switching on/off oscillations and EMI reduction based on the Two-Boost-Circuit IBPFC is discussed. Furthermore, a 3.5kW universal input 2-stage IBPFC prototype was built and experimental results show that 10dB EMI reductions on odd order harmonics can be achieved by carefully designing the BPFC using interleaving technique.

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Research on High Efficient Single-Phase Multi-Stage Interleaved Bridgeless PFC Frontend for Class-D Amplifiers

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Abstract—In this paper, a 3.5kW single-phase high efficient interleaved Bridgeless PFC (IBPFC) is proposed for class-D amplifiers. This topology achieves a relatively higher efficiency performance in a wide output power range, which helps to reduce the energy consuming of the whole system. In addition, a detailed analysis is given to reach a compromise of IBPFC's volume, efficiency and EMI reduction. A 3.5kW 2-stage IBPFC prototype covering universal input (from 85Vac to 265Vac) and with 390Vdc output is built and optimized. The experiment verifications show that a good Power Factor (PF) and excellent maximum efficiency of 98.6% at 230Vac with the switching frequency 65kHz and a 2.22kW load.

Keywords—high efficient; bridgeless PFC; interleaved; class-D amplifiers

I. INTRODUCTION

Due to its higher efficiency compared to linear audio amplifiers, class-D amplifier makes it possible for more compact and high-power audio applications [1]. In order to keep this natural advantage of class-D amplifiers, as its frontend, the PFC system is required to have an outstanding efficiency in a wide output power range. Architecture of class-D amplifier system with high efficient single-phase PFC frontend for universal line input is proposed in Fig. 1. In order to achieve higher efficiency from main to output, many research have been done to improve the performance of the PFCs. Among them, topology development and innovation is always an important method. Nowadays, the Bridgeless PFC (BPFC) topologies have attracted the most attentions since they reduce the number of semiconductors in current flowing path, and reduce the system conductor losses [2-4]. A latest publication reports a interleaved BPFC (IBPFC) with peak efficiency of 98.5% [4] at 220Vac, however, below 1kW, the system efficiency drops rapidly while output power decreases especially in the low line. This is not good for audio application, because the audio load is always dynamic in a wide range. Furthermore, none of the recent papers presented the BPFC's performance at full load in the low line [2-5].

In this paper, an optimal design of a nearly 98.6% efficiency, 390Vdc output, 3.5kW single-phase interleaved Bridgeless PFC (IBPFC) is presented at universal line for audio application. In Section II, discussions on multi-stage IBPFC are carried out focusing on the EMI mitigation and system optimization. And then, a useful 2-stage IBPFC topology is presented to compromise the EMI reduction, volume optimization and system's complexity. Detailed design considerations of the proposed 2-stage IBPFC is presented in Section III. Section IV verified the analysis and simulations in

Sections II and III by experimental measurements. Finally, The conclusion is made in Section V.

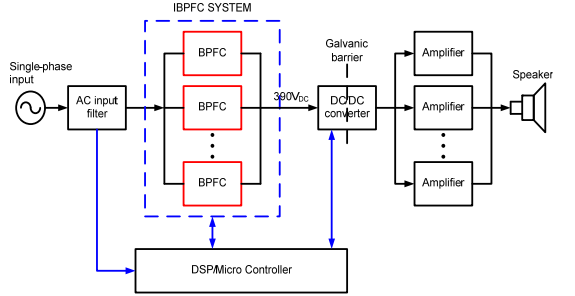


Fig. 1: Proposed IBPFC system for audio application

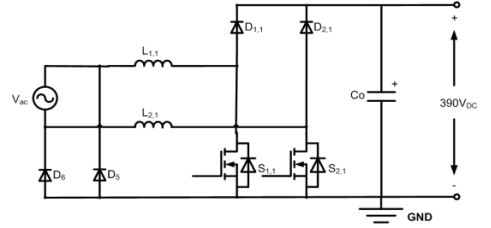


Fig. 2: Traditional non-interleaved Two-Boost-Circuit BPFC

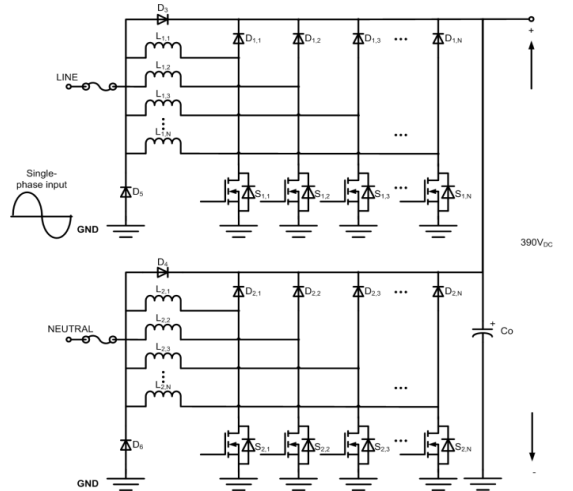


Fig. 3: Possible architecture of multi-stage IBPFC system

II. DISCUSSION ON MULTI-STAGE IBPFC

The idea of BPFC goes back to eighties [6]. Reference [2] not only showed the basic performances of five well-known BPFC topologies, but also gave a systematic comparison of these popular BPFCs and the conventional Boost PFC converter. According to its conclusion, the usage of Two-Boost-Circuit BPFC in Fig. 2 would allow having higher efficiency without harming the EMI performance compared to the traditional Boost PFC. Fig. 3 is an extended application of Fig. 2. It consists of multi-stage interleaved BPFC modules. In the positive half line period, Boost inductors $L_{1,i}$, MOSs $S_{1,i}$ and Boost diodes $D_{1,i}$ work interleaved with D_6 returning current to V_{ac} . Where, i symbolized the number of interleaved stages, ranging from 1 to N . In the negative half line period, the converter works symmetrically. This topology can be expected to have lower EMI than non-interleaved Two-Boost-Circuit BPFC with the same inductances, due to its lower input current ripples.

A. EMI Modeling and Suppression

Comparing to the simply paralleled BPFC systems to distribute power flowing, one major reason for using the IBPFC system is EMI reduction. In order to analyze the EMI suppression relates to multi-interleaved stages precisely, the common-mode (CM) and differential-mode (DM) noises of the IBPFC are modeled separately. Start from the 2-stage interleaved Two-Boost-Circuit BPFC in Fig. 4, since it has a symmetrical circuit structure for both positive and negative period of ac line, only half of the ac period is considered here. Procedure of generating its DM EMI model is showed in Fig. 5. The model of N -stage interleaved DM noise sources can be easily achieved by extending the existing DM model from 2 stages into N stages. It should be noticed that all the triangle current sources are $360^\circ/N$ phase shift. Where, N is the number of interleaved stages. **And when N equals to 1, it symbolizes the traditional non-interleaved BPFC in Fig. 2.**

Following the same steps, the CM model of the N -stage IBPFC is given in Fig. 6. It equals to interleave N pulses voltage sources, each of them is in series with an equivalent stray capacitor $C_{s1,i}$. Similarly, each pulse source is $360^\circ/N$ phase shift. The equivalent stray capacitor $C_{s1,i}$ mostly comes from the parasitic capacitor connecting between drain of the MOS and the ground.

Implementing the Discrete Fourier Transform (DFT), the amplitudes of high switching frequency noises from both CM and DM sources can be solved as below [7]:

$$\begin{cases} |V_{CM,int.}(n)| = 0, n \neq k \cdot N \\ |V_{CM,int.}(n)| = |V_{CM,non.}(n)|, n = k \cdot N \end{cases} \quad (1)$$

$$\begin{cases} |V_{DM,int.}(n)| = 0, n \neq k \cdot N \\ |V_{DM,int.}(n)| = |V_{DM,non.}(n)|, n = k \cdot N \end{cases} \quad (2)$$

Where, $V_{CM,int.}(n)$ and $V_{DM,int.}(n)$ are the n -order CM and DM harmonics of N -stage IBPFC; $V_{CM,non.}(n)$ and $V_{DM,non.}(n)$ are the n -order CM and DM harmonics of non-interleaved BPFC; k is a positive integer starting from 1.

From eqs. (1) and (2), it can be concluded that:

1. Interleaved stages help to suppress both CM and DM noises.

2. In an N -stage IBPFC, except the $k \cdot N$ times fundamental frequencies, all the rest harmonics cancelled due to the phase shift.
3. The more interleaved stages the IBPFC has, the more high frequency harmonics will be cancelled.
4. The switching frequency affects the design of the EMI filter of IBPFC due to the noises cancellation do NOT happen at $k \cdot N$ times fundamental frequencies. In order to maintain the EMI advantage of IBPFC system, it is better to select the switching frequency based on the range of conduction EMI measurement. According to the European Standard EN55013, the disturbance voltage at mains terminals in the frequency range from 150kHz to 30MHz needs to be attenuated to fulfill the EMI limitation [8]. **Therefore, the first harmonic of the IBPFC, which locates inside the range of the standard, should not equal to $k \cdot N$ times fundamental frequencies.** The mathematic expression is:

$$\left\lceil \frac{150kHz}{f_s} \right\rceil \neq k \cdot N \quad (3)$$

Where f_s is the switching frequency, and ' $\lceil x \rceil$ ' is the ceiling function, which returns the smallest integer not less than x . From Eq. (3) it can be found, the IBPFCs usually require higher cutoff frequency of EMI filters comparing to the non-interleaved one with same EMI attenuations, when the switching frequency is higher than 150kHz., which may do benefit to EMI filter's volume optimization.

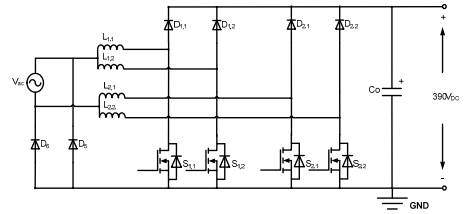


Fig. 4: 2-stage Two-Boost-Circuit IBPFC

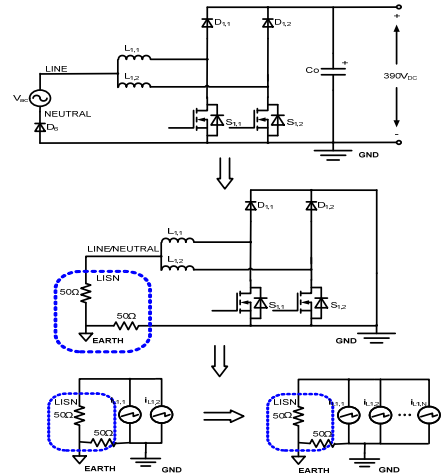


Fig. 5: DM EMI modeling of N -stage interleaved Two-Boost-Circuit BPFC

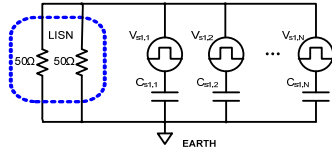


Fig. 6: CM EMI modeling of N -stage interleaved Two-Boost-Circuit BPFC

Fig. 7 gives the CM and DM EMI comparison between a 2-stage interleaved and a non-interleaved Two-Boost-Circuit BPFC, when the switching frequency f_s is improperly selected at 75kHz. Their 2nd harmonics at 150kHz are the first harmonics which locate inside the range of EMI limitation, and they almost have the same values. Because that 150kHz equals to the $k \times N$, when k is 1. Therefore, the same as Eq. (3) has proved, the cutoff frequency of EMI filter in this 2-stage IBPFC should be the same as the non-interleaved BPFC. Therefore, the EMI advantage of this IBPFC cannot display.

It should be noticed that in the simulations of Fig. 7, the model of EMI receiver is not considered. Furthermore, the real EMI performances typically depend strongly on the circuit layout, semiconductor characteristics, gate drivers, operating currents, voltages and temperature and parasitic elements. The actual waveforms above 3MHz are very difficult to predict. Therefore, in the following simulations, only the frequency noises below 3MHz are taken into consideration.

B. Efficiency and Power Density Analysis

At light load operating condition, comparing to the non-interleaved BPFC, one main disadvantage of IBPFC is that it increases the number of magnetic components. By adding one interleaved stage, two extra Boost inductors will be needed. Facing the most important issues in power electronics today – efficiency and power density – the compromise of power density, efficiency and EMI must be taken into consideration. Since the system's volume is mainly dominated by magnetic components, assuming equal inductances, the energy storage comparison of Boost inductors between N -stage IBPFC and non-interleaved BPFC appears as below [9]:

$$\frac{E_{int.N}}{E_{non}} = \frac{0.5 L_{int} \left(\frac{I}{N}\right)^2 N}{0.5 L_{non} I^2} = \frac{1}{N} \quad (4)$$

Eq. (4) shows that: although the number of boost inductors of N -stage IBPFC is $2N$ times larger than those of non-interleaved BPFC, the energy storage on each interleaved inductor is N^2 times smaller, which may do benefits on inductor volume reduction.

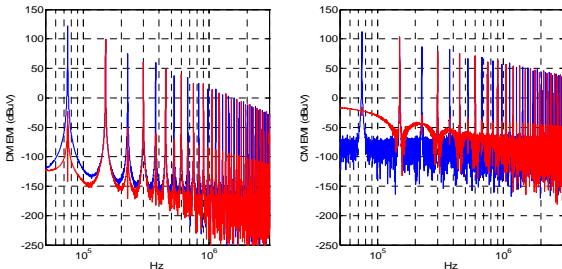


Fig. 7: DM (left) and CM (right) EMI comparison of 2-stage interleaved (red) and non-interleaved (blue) Two-Boost-Circuit BPFC at 3.5kW

A multi-objective Boost inductor optimization procedure is illuminated in the flowchart in Fig. 8. It takes both the volume and efficiency of the N -stage IBPFC into considerations and searches for a useful compromise between efficiency and power density. By implementing the optimization procedure, Fig. 9 gives the comparison of minimal volume of Boost inductors in interleaved and non-interleaved Two-Boost-Circuit BPFC with high efficient performance, when the interleaved stage N varying from 2 to 8 at 3.5kW and 85Vac input. It should be noticed, in this optimization, Kool Mu E cores from Magnetics® were chosen because of their high saturation level, low core losses and cheap price. And, comparing with the traditional round winding, copper foils were selected to reduce the ac winding losses. Moreover, the thickness of the winding was optimized in order to further increase the inductor's efficiency.

From Fig. 9, it can be concluded:

1. With the number of interleaved stages increasing, the single Boost inductor's volume reduces significantly.
2. Due to the number of inductors increasing, except the 3-stage interleaved, the total inductors' volume of IBPFC is always higher than the non-interleaved BPFC with the same inductance.
3. 3-stage and 4-stage IBPFC has lower total inductor volume among all the IBPFCs. The first one has smaller system volume, and the second one has better EMI.
4. Comparing to 3 or 4 stages IBPFC, the 2-stage IBPFC has slightly higher volume and EMI, but lower cost and less control complexity.

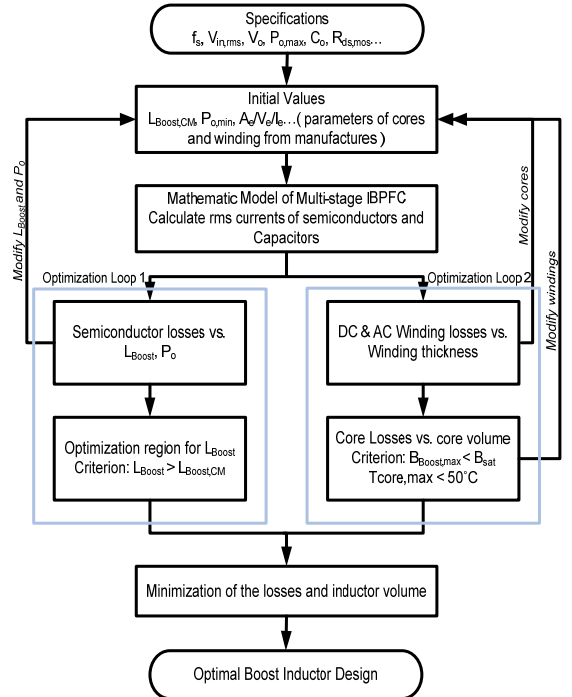


Figure 8: Flow chart of the optimization procedure of Boost inductor for trading off efficiency and power density

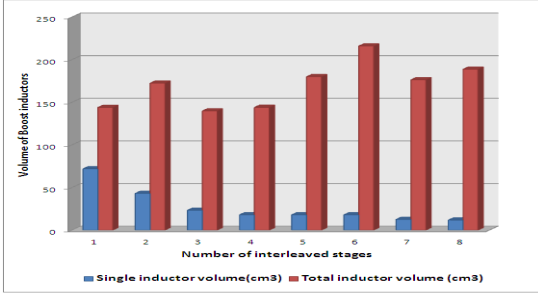


Fig. 9: Minimal single (blue) and total (red) inductor's volume comparison of interleaved and non-interleaved Two-Boost-Circuit IBPFCs

III. OPTIMIZED DESIGN OF A 2-STAGE IBPFC

A. Optimize Semiconductor Losses in Wide Output Range

According to what has been discussed in Section II Part B, only the 2-stage IBPFC is analyzed in this Section. Because of the audio application, the IBPFC works in a wide output power range from less than 500W up to 3.5kW, in order to have a relatively flat and high efficiency performance, it is important that the inductance reduction caused by DC bias will not increase the semiconductor losses a lot. Implement the mathematic model of BPFC in reference [10], Fig. 10 shows the relationship of Boost inductance versus semi-conductor losses ratio as a function of output power at 85Vac input.

From Fig. 10, it can be seen that: at the beginning, with the inductance increasing, the semiconductor losses ratio reduces significantly due to the decreasing of input current ripple; however, when the inductance is around 0.2mH, further increasing it will not help to reduce the semiconductor losses ratio anymore.

Therefore, according to Fig. 10, a Boost inductance of 0.2mH at 300W is a good selection to gain lower semiconductor losses in a wide output power range.

B. Optimize Boost Inductors

To optimize Boost Inductors, we start from winding losses prediction. It is well known, winding losses include DC losses and AC losses [9]. To further reduce the winding losses, copper foils were used here. Using the same derivation method in paper [10], Fig. 11 gives the winding losses versus the thickness of copper foil and Boost inductance at 3.5kW output and 85Vac input. It shows that: firstly, in high power applications, the winding losses are dominated by DC losses; secondly, for this paper, the most useful thickness of the copper foil ranges from 0.15mm to 0.2mm. The thicker copper foil is not very necessary, due to it occupies more window areas in the core but cannot reduce the winding losses very much.

Using the relatively low core-loss Kool Mu cores as an example, Fig. 12 shows the total inductor losses vs. Boost inductance for all the qualified Kool Mu E cores from Magnetics®, when the thickness of copper foil h is 0.15mm. In the legend on the top right corner, the cores were ranked by their sizes, the top the smaller.

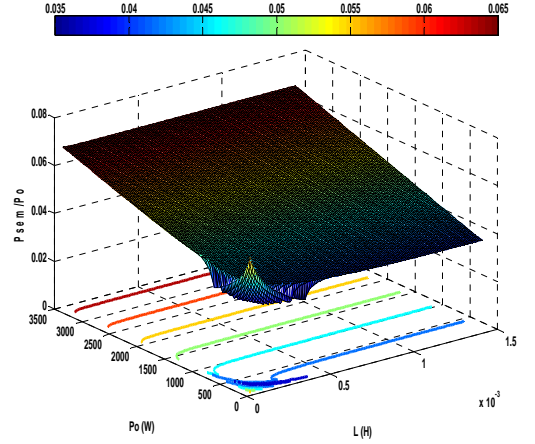


Fig. 10: Semiconductor losses ratio vs. output power and Boost inductance of 2-stage IBPFC

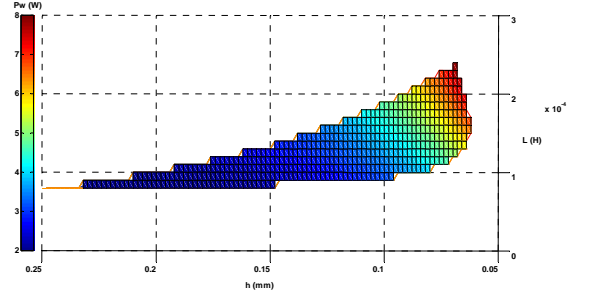


Fig. 11: Winding losses vs. copper foil's thickness and Boost inductance of proposed 2-stage IBPFC

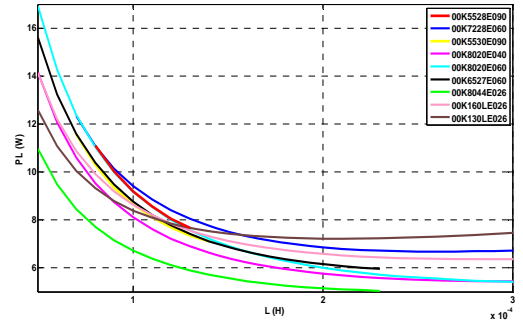


Fig. 12: Inductor losses vs. Boost inductance of proposed 2-stage IBPFC

TABLE I. OPTIMIZED PARAMETERS OF BOOST INDUCTOR WITH HIGH EFFICIENCY AND POWER DENSITY FOR 2-STAGE IBPFC

Core No.	Winding h (mm)	P_c/P_L at 3.5kW	ΔT (°C)	L at 300W (mH)
5528E090	0.15	62.32%	60	0.22

Where, P_c means core losses, P_L is total inductor losses.

Considering both of the efficiency and power density, the optimized parameters of Boost inductor for the 2-stage Two-Boost-Circuit IBPFC are listed in Table I.

IV. EXPERIMENTAL VERIFICATION

After carefully design the 65kHz 2-stage IBPFC, the key components' information is provided in Table II. Comparison of the system's efficiency, which were measured by the precision power analyzer PPA5530 from N4L[®], at different line voltages are drawn in Fig. 13. Fig. 14 and 15 gives the measured input voltage and current waveforms of the IBPFC in 3.5kW at 110Vac and 230Vac input. According to the requirement from the audio application, the EMI measurement should be done at one over eight of the full power. So, Fig. 16 gives the EMI performances of the 2-stage IBPFC and a traditional BPFC at one eighth of full power without EMI filter in front. In order to make a fair comparison, all the components and testing equipments selected for the 2 topologies are the same.

TABLE II. KEY COMPONENTS USED IN THE 2-STAGE IBPFC PROTOTYPE

Device	Part No.	No. of devices
Fast Diode	STPSC1206	4
Return Diode	STTH6004W	2
MOSFET	IPW60R045CP	4
Inductor	5528E090 core	4

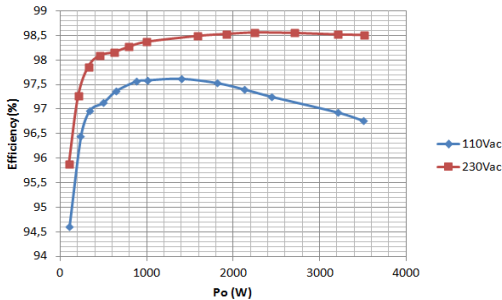


Fig. 13: Efficiency comparison of 2-stage IBPFC at different input voltages

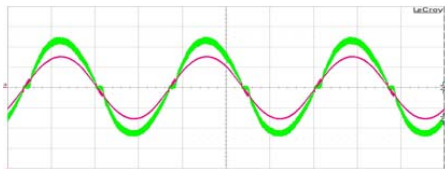


Fig. 14: Input voltage (red 100V/div) and current (green 20A/div) waveforms from 2-stage IBPFC at 3.5kW and 110Vac, PF=99%

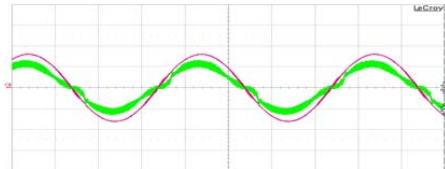
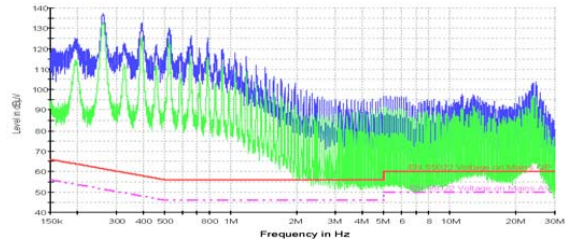
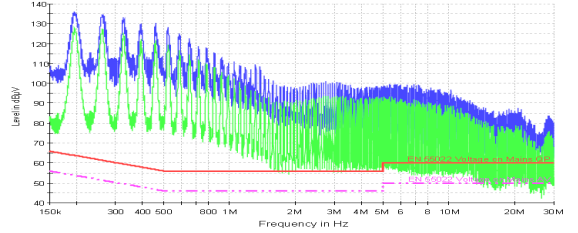


Fig. 15: Input voltage (red 200V/div) and current (green 20A/div) waveforms from 2-stage IBPFC at 3.5kW and 230Vac, PF=99%



(a) 2-stage IBPFC



(b) Traditional non-interleaved BPFC

Fig. 16: EMI comparison of 2-stage IBPFC and non-interleaved BPFC at one eighth of full power and 230Vac input

Fig. 16 shows that in the 2-stage IBPFC, the odd harmonics can be partly cancelled due to phase shift.

V. CONCLUSION

As shown in this paper, a 3.5kW single-phase 2-stage IBPFC of peak efficiency 98.6% is proposed for audio application. The EMI model of the multi-stage IBPFC is made to analysis the insight of EMI cancellation relates to number of interleaved stage. Furthermore, the multi-objective optimization is implemented to achieve a useful balance of system efficiency, volume and EMI reduction in the design.

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Research on EMI Reduction of Interleaved Bridgeless Power Factor Corrector using Frequency Dithering

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Abstract - This paper proposes a cost-efficient method to reduce the electromagnetic interference (EMI) of interleaved BPFC (IBPFC) system in a wide frequency range by carefully designing and utilizing frequency dithering. In this work, a valuable frequency dithering designing concept is implemented for a 3.5kW universal line 2-stage IBPFC. Detailed evaluations of impacts on EMI reduction from frequency dithering are carried out through both of the theoretical and experimental analysis. Furthermore, the effects on attenuations of EMI filter based on frequency dithering is also researched through mathematical derivations. Experiments prove that with a proper design, it is possible to gain an useful EMI reduction in the IBPFC system by frequency dithering.

Keywords- EMI reduction; interleaved Bridgeless PFC; frequency dithering; filter

I. INTRODUCTION

In order to comply with the International Regulations, active Power Factor Corrector (PFC) is widely used to limit the AC line harmonic currents generated by switching mode power supplies. Nowadays, with the increasing global interest of energy saving and efficiency boosting, by removing the passive bridge rectifier added in front of the traditional PFCs, the Bridgeless PFC (BPFC) converters act as an optional solution for the front-end of high-efficient AC to DC converters.

In recent years, the BPFCs' developments are mainly related to topology improvement [1-6] and magnetic components' optimization [7-8]. Especially, in the latest BPFC version from last year [4-5], interleaving technique was implementing, which shows excellence on electromagnetic interference (EMI) attenuation. Additionally, paper [9] claims that: although part of the noise harmonics can be suppressed by properly using interleaving stages, there will always be some noises containing certain frequency components which cannot be suppressed due to the natural restriction of interleaved topology. However, in all the publications until now, the BPFCs operate in constant switching frequency, and the very high dv/dt at diodes and MOSFETs are the major noise generators of common-mode (CM) EMI. To meet the world conducted EMI limitations, suitable line filter is needed to implement, and it occupies a significant amount of volume in the BPFC system.

This paper proposes a cost-efficient method to reduce the CM EMI of interleaved BPFC (IBPFC) system in a wide frequency range through carefully designing and utilizing frequency dithering. In this work, a valuable frequency dithering concept is dug for a 3.5kW peak power universal line 2-stage IBPFC system in Fig. 1 for audio applications. Details of its operation principles are presented in papers [4-5].

Evaluations of impacts on EMI reduction is carried out through both of the theoretical and experimental analysis. Additionally, how will the frequency dithering affect the design of EMI filter is also discussed briefly. And possible future works for further investigations are put forward.

The article is organized as follows. Section II presents the principles of frequency dithering for EMI suppression. In order to get a complete analysis, the main advantages and limitations of frequency dithering technique are discussed. Subsequently, for industrial considerations, the inner relation of frequency dithering versus EMI filter's design is proposed in Section III. Furthermore, a fair comparison between the proposed IBPFC with and without frequency dithering is obtained by experimental verifications in Section IV. Finally, the conclusion and the outlook of future works for promoting investigations are shown in Section V.

II. FREQUENCY DITHERING AND EMI SUPPRESSION

It is well known that frequency dithering belongs to carrier-frequency modulation (CFM) technique, which can be classified as periodic CFM (PCFM) and random CFM (RCFM) [10-13]. In this section, the important characteristics of frequency dithering regarding to EMI suppression will be discussed.

A. Reductions of noise harmonics under cosine frequency dithering function

In this part, the research focuses on PCFM. That means the switching frequency dithers with a small amplitude variation around a central frequency. Considering a standard PWM pulse signal $G(t)$ with a duty ratio D and switching frequency f_s . Assuming $G(t)$ has a high level A and a low level 0 , implementing the Fourier series, $G(t)$ can be expressed as:

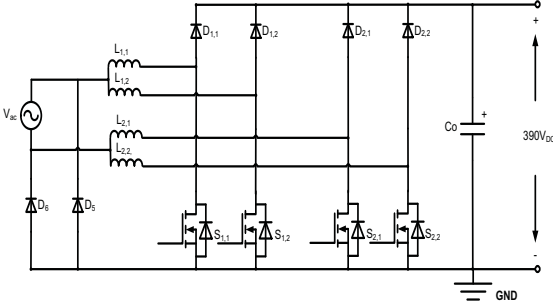


Fig. 1: Interleaved 2-stage Two-Boost-Circuit BPFC [5]

$$G(t) = \sum_{n=-\infty}^{+\infty} C_n e^{j\theta_n} \quad (1)$$

Where, C_n and θ_n are the n th series coefficients, which contain the magnitude and phase information of the n th harmonic. And C_n and θ_n can be calculated by:

$$C_n = \frac{1}{T_s} \int_{-\frac{T_s}{2}}^{\frac{T_s}{2}} G(t) e^{-j2\pi f_s n t} dt = \frac{A_j}{2\pi n} (e^{-j2\pi n D} - 1) \quad (2)$$

$$\theta_n(t) = 2\pi n f_s t \quad (3)$$

When the switching frequency is modulated by a sinusoidal function with a dithering amplitude Δf_s and a dithering rate f_m , the instantaneous frequency and angular rotation of the dithering PWM signal are:

$$f_{ds}(t) = f_s + \Delta f_s \cos(2\pi f_m t) \quad (4)$$

$$\theta_{ds}(t) = 2\pi \int_0^t f_{ds}(t) dt = 2\pi f_s t + \gamma \sin(2\pi f_m t) \quad (5)$$

Where, γ is the dithering factor. It symbolizes the ratio of dithering amplitude and dithering rate. And it is defined as:

$$\gamma = \frac{\Delta f_s}{f_m} \quad (6)$$

Similarly, by applying the Fourier series, the dithering PWM signal can be expressed as:

$$G_d(t) = \sum_{n=-\infty}^{+\infty} C_n e^{j\theta_{ds,n}} = \sum_{n=-\infty}^{+\infty} C_n e^{j[\theta_n + \gamma \sin(2\pi f_m t)]} \quad (7)$$

With the derivation results from [13], Eq. (7) can be rewritten into:

$$\begin{aligned} G_d(t) &= \sum_{n=-\infty}^{+\infty} C_n \left\{ \sum_{i=0}^{+\infty} J_i(n\gamma) \left[e^{j(\theta_n + \theta_{m,i})} + (-1)^i e^{j(\theta_n - \theta_{m,i})} \right] \right\} \\ &= \sum_{n=-\infty}^{+\infty} C_n e^{j\theta_n} \left\{ \sum_{i=0}^{+\infty} J_i(n\gamma) \left[e^{j\theta_{m,i}} + (-1)^i e^{j(-\theta_{m,i})} \right] \right\} \end{aligned} \quad (8)$$

Where $\theta_{m,i}$ is the phase angular induced by frequency dithering and can be written as:

$$\theta_{m,i}(t) = 2\pi i f_m t \quad (9)$$

And $J_i(\cdot)$ is the i th order Bessel function:

$$J_i(n\gamma) = \left(\frac{n\gamma}{2} \right)^i \sum_{j=0}^{+\infty} \frac{(-1)^j \cdot \left(\frac{n\gamma}{2} \right)^{2j}}{j!(j+i)!} \quad (10)$$

From Eq. (8) one can see, the harmonics reduction at multiples of central switching frequency f_s can be predicted by setting i equals to 0. And $J_0(\cdot)$ can be written as:

$$J_0(n\gamma) = \sum_{j=0}^{+\infty} \frac{(-1)^j \cdot \left(\frac{n\gamma}{2} \right)^{2j}}{(j!)^2} \quad (11)$$

Therefore, the absolute value of $J_0(\cdot)$ in Eq. (11) shows: comparing to the standard PWM in Eq. (1), the harmonics reductions at multiples of central switching frequency of dithering PWM in Eq. (8). It is easy to see, the harmonics' reduction factor $|J_0(\cdot)|$ is a function of dithering factor γ and the harmonic's order n . The reductions' trends of the harmonics versus the dithering factor γ are given in Fig. 2, when n changes from 1 to 4.

From Fig. 2, one can conclude that:

1. Dithering PWM has lower amplitudes at multiples of central switching frequency compared to standard PWM.
2. With the same dithering factor, the reductions vary from harmonic to harmonic.
3. When the dither factor increases, each harmonic has its maximum reduction.

B. Limitations of frequency dithering

According to reference [14] has proved, the power spectrum of dithering PWM signal in Eq. (8) in positive frequency range can be expressed as:

$$\begin{aligned} S_d(f, \gamma) &= S(f, \gamma) + \Delta S(f, \gamma) = 2 \left| \sum_{n=1}^{\infty} C_n [J_0(n\gamma) \cdot \delta(f - nf_s)] \right|^2 \\ &+ 2 \left| \sum_{n=1}^{\infty} C_n \left\{ \sum_{i=1}^{\infty} J_i(n\gamma) \cdot [\delta(f - nf_s - if_m) + (-1)^i \delta(f - nf_s + if_m)] \right\} \right|^2 \end{aligned} \quad (12)$$

Where $S(f, \gamma)$ is the original power spectrum of standard PWM signal and $\Delta S(f, \gamma)$ is the spread spectrum caused by frequency dithering.

a) The limitations of central harmonics reductions

Through Fig. 2 and Eq. (12), it is not difficult to find out that in the dithering PWM, the central harmonics' reductions are limited by γ . Furthermore, in a fixed γ dithering system, it is more reasonable to expect large harmonics' reductions only happening at certain frequencies not in the whole frequency range.

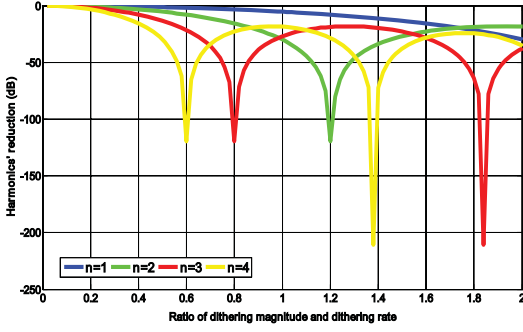


Fig. 2: Harmonics' reduction vs. dithering factor γ when harmonics' order n changes from 1 to 4

b) Spectrums overlapping and redistribution

According to paper [14], the frequency dithering will also lead upper and lower sidebands at multiples of central switching frequency f_s and the bandwidth of the n th harmonic can be approximately calculated by:

$$B_n = 2(n\gamma + 1) \cdot f_m = 2(n\Delta f_s + f_m) \quad (13)$$

Fig. 3 shows the harmonics' spectrum comparison of a standard PWM and a dithering PWM [14].

Assuming the sum of the right and left bandwidths of the n th and $(n+1)$ th harmonics is:

$$B_{sum} = \frac{1}{2}(B_n + B_{n+1}) = (2n+1)\Delta f_s + 2f_m \quad (14)$$

Therefore, when B_{sum} is higher than f_s , these two sidebands will overlap each other. The same as what has shown in Fig. 3, the harmonics' power in the overlapping area of dithering PWM will be higher than standard PWM. This means, the smaller the f_s is, the larger the overlapping areas could be and the more power from the $(n+1)$ th harmonic's lower sideband will be pushed into the higher sideband of the n th harmonic. This is why normally when one measures the EMI from a frequency dithering system, comparing to a constant frequency system, the frequency dithering system usually pushes the EMI from the high frequency domain into the low frequency domain.

III. EMI FILTER DESIGN CONSIDERATIONS

According to what has been mentioned in Section II, the limitations of frequency dithering technique will definitely harm its EMI performance and impact the EMI filter design. Considering the harmonics spectrums of standard PWM and dithering PWM in Fig. 4, the filter's attenuation character is given in the red line. If the cutoff frequency of the filter at minus 20dB/dec frequency band is f_ζ , for standard PWM,

the filter's attenuation at multiple of switching frequency nf_s is as below:

$$\alpha_n = -20\zeta \lg \frac{nf_s}{f_\zeta} - A_\zeta \quad (15)$$

Where ζ is related to filter's type, it is a function of filter's order and structure, and A_ζ is the filter's attenuation at f_ζ .

Therefore, after filtering, the harmonics' amplitude at nf_s is:

$$X_n = 20 \lg |C_n \cdot J_0(n\gamma)| + \alpha_n \quad (16)$$

Similarly, in the dithering PWM, the filter's attenuations around multiple of switching frequency nf_s can be calculated as:

$$\beta_{n,k} = -20\zeta \lg \frac{nf_s + f_m \cdot k}{f_\zeta} - A_\zeta \quad (17)$$

Where k symbolizes the spread spectrums caused by frequency dithering. According to Eqs. (8) and (12), each spread spectrum has a frequency interval of f_m . By utilizing Eq. (13), the parameter k varies from $-\lfloor n\gamma + 1 \rfloor$ to $\lfloor n\gamma + 1 \rfloor$. And ' $\lfloor x \rfloor$ ' is the floor function, which returns the smallest integer not larger than x .

Therefore, after filtering, the harmonics' amplitudes around nf_s becomes:

$$Y_{n,k} = 20 \lg |C_n \cdot J_{N+k}(n\gamma)| + \beta_{n,k} \quad (18)$$

Where N equals to $\lfloor n\gamma + 1 \rfloor$.

Unlike the constant frequency system, due to the EMI receiver has impact on the final EMI measurement results of a frequency dithering system through its inner resolution bandwidth (RBW) filter [15]. In order to predict the EMI performance of a frequency dithering system correctly, the model of EMI receiver cannot be neglected. Reference [16] presented a very details procedure for EMI receiver modeling, according to its conclusions, it should be precise enough to predict the measured EMI results at each frequency by only considering the harmonics located inside the 9kHz inner RBW filter of the EMI receiver.

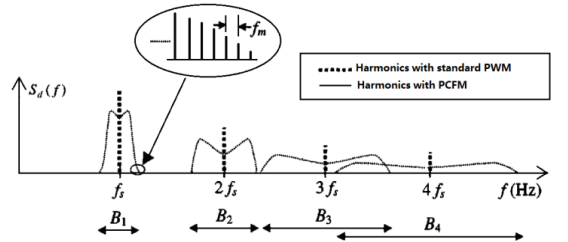


Fig. 3: Harmonics' spectrum comparison [14]

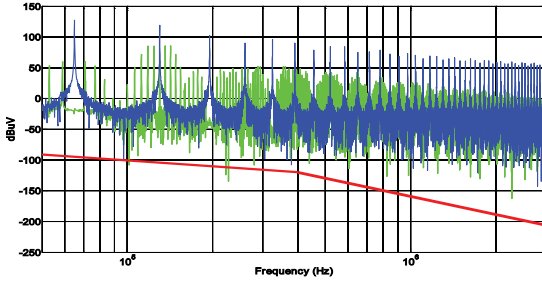


Fig. 4: Harmonics' spectrum comparison, dithering PWM (green) and standard PWM (blue), the red line is the filter's attenuation characteristics Set X equals to the maximum value of k which satisfies that:

$$\frac{9kHz}{X \cdot f_m kHz} \geq 1 \quad (19)$$

Therefore, the measured peak and average harmonics' amplitudes of dithering PWM at nf_s display on EMI receiver can be predicted as below:

$$\hat{Y}_{n,Pk} = \{Y_{n,k}\}_{\max}, (k \leq |X|) \quad (20)$$

$$\tilde{Y}_{n,Av} = \frac{1}{2X} \sum_{k=-X}^X Y_{n,k} \quad (21)$$

Where, Pk. means peak value and Av. means average value. Compare Eqs. (16), (20) and (21), after filtering significant harmonics' reduction from dithering PWM may exhibit if $\tilde{Y}_{n,Av}$ far below X_n .

IV. EXPERIMENTAL VERIFICATIONS

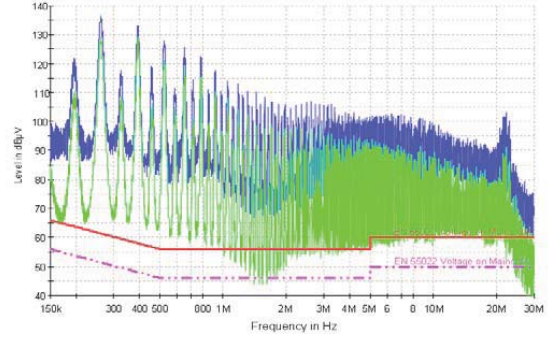
According to references [5] and [8], the key components selected for a high efficient 2-stage interleaved Two-Boost-Circuit BPFC at 3.5kW and universal line are listed in Table I.

As what has been proved in paper [9], in order to show the advantage of EMI reduction comparing to non-interleaved BPFC, a useful central switching frequency f_s was set at 65kHz. According to the conducted EMI standard, the highest harmonic's amplitude which needs to be attenuated locates at 260kHz (the 4th order harmonic) [9]. As what shows in Fig. 2, for further increasing the attenuation at 260kHz, a dithering amplitude Δf_s of 7.55kHz and dithering rate f_m of 6.1kHz are selected. This leads a dithering factor γ at 1.24, and will give a 33.15dB reduction at the 4th harmonic. Due to the aim of this IBPFC design is for audio application, we only interested in the EMI performance at average power, which is 1 over 8 of the peak power. Therefore, the experimental results below are all taken under the average output power.

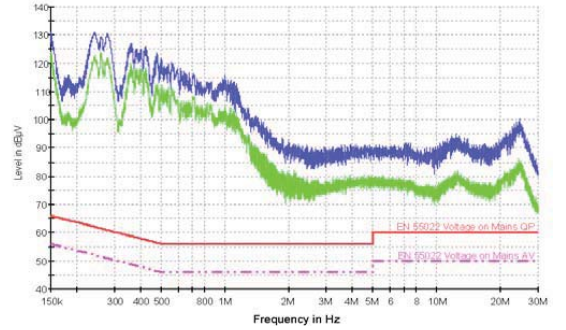
Fig. 5 shows the conducted EMI comparison of the 2-stage IBPFC in Fig. 1 with and without frequency dithering and no input filter. Additionally, in Fig. 6, there are the detailed harmonics' amplitudes comparison of 4 highest harmonics in Fig. 5.

TABLE I. KEY COMPONENTS USED IN THE 2-STAGE IBPFC

Device	Part #	# of devices
Fast Diode	STPSC1206	4
Return Diode	STTH6004W	2
MOSFET	IPW60R045CP	4
Inductor Cores	5528E090 Magnetics®	4



(a) Standard IBPFC, Pk. value in blue, Av. value in green



(b) Proposed IBPFC, Pk. value in blue, Av. value in green

Fig. 5: Conducted EMI comparison of standard IBPFC and proposed frequency dithering IBPFC at 110Vac input and 1 over 8 full power without input EMI filter

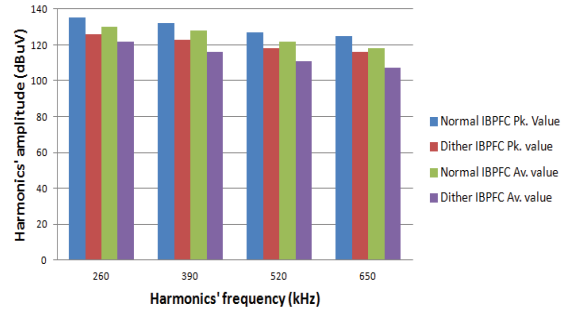


Fig. 6: Detailed EMI comparison of 4 highest harmonics in Fig. 5

Implementing the derived mathematical expressions in Sections II and III, Table II gives the harmonics' amplitudes comparison in Fig. 6 between experiments and theoretical prediction of the frequency dithering IBPFC. Where, P. means predicted value and M. means measured value.

TABLE II. EMI COMPARISON OF CRITICAL HARMONICS

Harmonics' frequency (kHz)		260		390		520		650	
EMI detector		Pk.	Av.	Pk.	Av.	Pk.	Av.	Pk.	Av.
Dither IBPFC (dBuV)	P.	125	124	121	116	115	107	112	109
	M.	126	122	123	116	118	111	116	107
Prediction error (dBuV)		-1	2	-2	0	-3	-4	-4	2

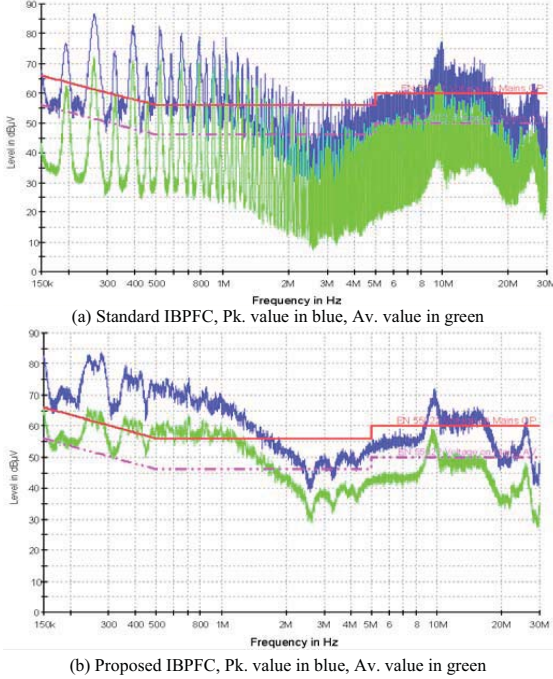


Fig. 7: Conducted EMI comparison of standard IBPFC and proposed frequency dithering IBPFC at 110Vac and 1/8 peak power with the same filter

From Table II, it can be proved that using the mathematical method mentioned in Sections II and III, the EMI performances of the frequency dithering IBPFC can be predicted approximately.

Fig. 7 shows the conducted EMI comparison of the 2-stage IBPFC in Fig. 1 with and without frequency dithering using the same input filter. Compare Figs. 5 and 7, it can be concluded that the EMI generated by frequency dithering PWM is lower and easier to attenuate by EMI filter than the traditional IBPFC. And by combining of interleaving and frequency dithering, further EMI reduction can be achieved.

V. CONCLUSIONS AND FUTURE WORKS

In this paper, a systematic research on EMI reduction of the IBPFC based on frequency dithering is given. And the insight into the limitations of EMI suppression using frequency dithering is presented. Moreover, the experiments prove that useful EMI reductions can be expected by carefully designing the frequency dithering together with interleaving technique.

According to the discussion in Section III, in the future, it will be useful to invest how to make an optimized design of EMI filter under frequency dithering condition to achieve both maximum EMI reduction and low filter' volume. This will be a good combination of both research and industrial application.

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A.7 Transactions on Industrial Electronics Paper Submitted

Analysis of Optimal Design of High Efficient Multi-stage Interleaved Bridgeless PFC Converter for Class-D Amplifiers

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Abstract—This paper proposes a systemic approach to design the high efficient 3.5kW single-phase universal line (from 85Vac to 265Vac) PFC converter for class-D amplifiers based on the optimal multi-stage Interleaved Bridgeless PFC topology. By implementing the multi-objective optimization procedure, this PFC design achieves a relatively higher efficiency performance in a wide output power range without losing power density. Furthermore, a cost-efficient solution is presented for EMI mitigation by carefully designing and utilizing frequency dithering. The simulations and experimental results demonstrate the validity of the study.

Index Terms—Efficiency, multi-stage Interleaved Bridgeless PFC, multi-objective optimization, EMI mitigation

I. INTRODUCTION

DUE to the higher efficiency compared to linear audio amplifiers, class-D amplifiers make it possible for more compact high-power audio applications [1]. For keeping the advantage of class-D amplifiers, as its front-end, the PFC system is required to have an outstanding efficiency in a wide output power range. Recent years, the *Bridgeless PFCs* (BPFCs) are becoming a promising option for volume and loss reduction, because these PFC topologies do not need the diodes rectification system in front of them and have less semiconductor losses than the conventional PFCs [2-5]. The architecture of class-D amplifiers system with high efficient single-phase PFCs front-end is proposed in Fig. 1.

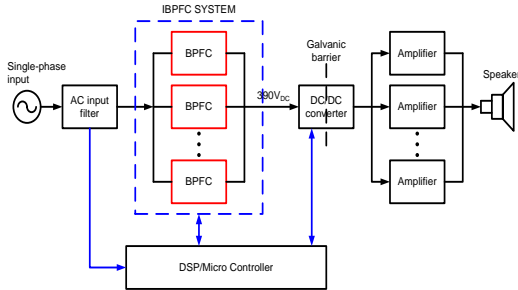


Fig. 1: Architecture of class-D amplifiers system with high efficient single-phase BPFCs front-end

In order to achieve as high efficiency as possible from mains to output, studies such as topology innovation and optimization have been done to improve the performances of the BPFCs. Recent publications [5-8] report some latest super efficient BPFC systems with maximum efficiencies above 98.4% at 230Vac and below 3.5kW. However, in these BPFCs, their efficiencies drop rapidly while output power decreases especially in the low line, which is not good for audio application since the audio load is always dynamic in a wide range. Besides, none of these papers presented the BPFC's performances at full load in the low line. In additionally, the EMI discussions were not taken into considerations neither.

In this paper, an optimal design of a nearly 98.6% efficient, 390Vdc output, 3.5kW single-phase *Interleaved Bridgeless PFC* (IBPFC) is presented at universal line for audio application. The procedure is based on a generic optimization approach, which guarantees a useful compromise of low volume, high efficiency and expectable EMI mitigation.

The article is organized as follows. In Section II, discussions on multi-stage IBPFC are carried out focusing not only on the EMI modeling and suppression, but also on volume and efficiency optimization of the whole system. And then, a useful 2-stage IBPFC topology is presented to compromise the common multi-objective requirements on EMI reduction, volume-efficiency optimization and system's complexity. Detailed analysis on efficiency boosting phase of the proposed optimal 2-stage IBPFC is presented in Section III. Section IV analyzes the possibility to further reduce the EMI of the IBPFC by implementing frequency dithering. In order to achieve a complete analysis, the main advantages and limitations of frequency dithering technique are discussed together. Additionally, for the industrial application considerations, the insight of frequency dithering versus EMI filter's design is proposed in Section V. Subsequently, Section VI verifies the analysis results in previous Sections by experimental measurements. Finally, the conclusions and outlook of future works for deeper investigations are presented in Section VII.

II. DISCUSSION ON MULTI-STAGE IBPFC

The idea of BPFC goes back to eighties [9]. Reference [10] not only showed the basic performances of five classic BPFC topologies, but also gave a systematic comparison of them and a conventional Boost PFC converter. According to its conclusion,

utilizing the Two-Boost-Circuit BPFC in Fig. 2 would allow having higher efficiency without losing the EMI performance compared to the traditional Boost PFC.

Fig. 3 is an extended application of Fig. 2. It consists of multi-stage interleaved BPFC modules. In the positive half line period, Boost inductors $L_{1,i}$, MOSs $S_{1,i}$ and Boost diodes $D_{1,i}$ work interleaved with D_6 returning current to V_{ac} . Where, i symbolized the number of interleaved stages, ranging from 1 to N . In the negative half line period, the converter works symmetrically. This topology can be expected to have lower EMI than non-interleaved Two-Boost-Circuit BPFC with the same inductances, due to its lower input current ripples.

A. EMI Modeling and Suppression

Comparing to the simply paralleled BPFC system, to distribute power flowing, one major reason for using the IBPFC system is EMI reduction. In order to analyze the EMI suppression relates to multi-interleaved stages precisely, the common-mode (CM) and differential-mode (DM) noises of the IBPFC are modeled separately. Start from a 2-stage interleaved Two-Boost-Circuit BPFC in Fig. 4, since it has a symmetrical

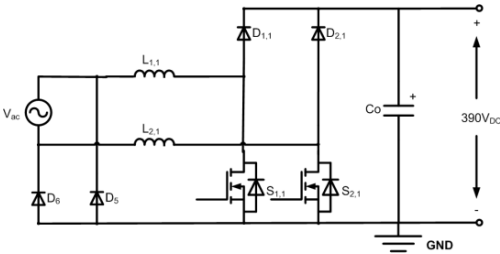


Fig. 2. Traditional non-interleaved Two-Boost-Circuit BPFC.

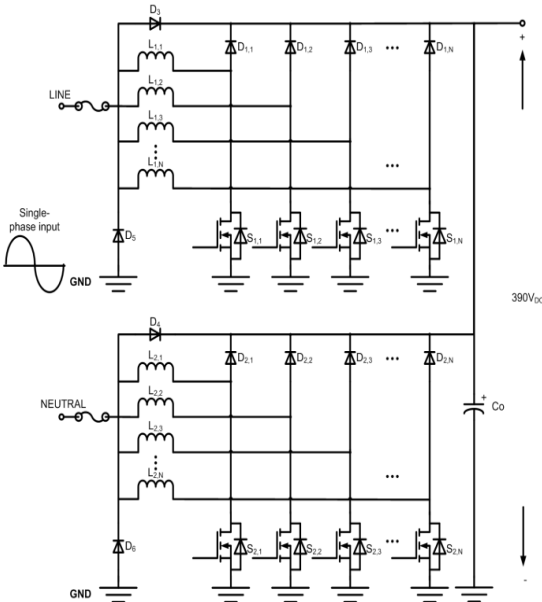


Fig. 3. Possible architecture of multi-stage IBPFC system.

circuit structure for both positive and negative period of ac line, only half of the ac period is considered here. Procedure of generating its DM EMI model is showed in Fig. 5 [11]. The model of N -stage interleaved DM noise sources can be easily derived by extending the existing DM model from 2 stages into N stages. It should be noticed that all the triangle current sources are $360^\circ/N$ phase shift. Where, N is the number of interleaved stages. **And when N equals to 1, it symbolizes the traditional non-interleaved BPFC in Fig. 2.**

Following the same steps, the CM model of the N -stage IBPFC is given in Fig. 6. It equals to interleave N pulses voltage sources, each of them is in series with an equivalent stray capacitor $C_{s1,i}$. Similarly, each pulse source is $360^\circ/N$ phase shift. The equivalent stray capacitor $C_{s1,i}$ mostly comes from the parasitic capacitor connecting between drain of the MOS and the ground.

Implementing the Discrete Fourier Transform (DFT), the amplitudes of high switching frequency noises from both CM and DM sources can be solved as below [11]:

$$\begin{cases} |V_{CM,int.}(n)| = 0, n \neq k \cdot N \\ |V_{CM,int.}(n)| = |V_{CM,non}(n)|, n = k \cdot N \end{cases} \quad (1)$$

$$\begin{cases} |V_{DM,int.}(n)| = 0, n \neq k \cdot N \\ |V_{DM,int.}(n)| = |V_{DM,non}(n)|, n = k \cdot N \end{cases} \quad (2)$$

Where, $V_{CM,int.}(n)$ and $V_{DM,int.}(n)$ are the n -order CM and DM harmonics of N -stage IBPFC; $V_{CM,non}(n)$ and $V_{DM,non}(n)$ are the n -order CM and DM harmonics of non-interleaved BPFC; k is a positive integer starts from 1.

From eqs. (1) and (2), it can be concluded that:

1. Interleaved stages help to suppress both CM and DM noises.
2. In an N -stage IBPFC, except the $k \times N$ times fundamental frequencies, all the rest harmonics cancelled due to the phase shift.
3. The more interleaved stages the IBPFC has, the more high frequency harmonics will be cancelled.
4. The switching frequency affects the design of the EMI filter of IBPFC due to the noises cancellation do *NOT* happen at $k \times N$ times fundamental frequencies. In order to maintain the EMI advantage of IBPFC system, it is better to select the switching frequency based on the range of conduction EMI limitations. According to the European Standard EN55013 [12], the disturbance voltage at mains terminals in the frequency range from 150kHz to 30MHz needs to be attenuated to fulfill the EMI limitation. **Therefore, the first harmonic of the IBPFC, which locates inside the range of the EMI limitations, should not be equal to $k \times N$ times fundamental frequencies.** The mathematic expression is:

$$\left\lceil \frac{150kHz}{f_s} \right\rceil \neq k \cdot N \quad (3)$$

Where f_s is the switching frequency, and ' $\lceil x \rceil$ ' is the ceiling function, which returns the smallest integer not less than x . From Eq. (3) it can be found, the IBPFCs usually allow higher cutoff frequency of EMI filters comparing to the non-interleaved one with same EMI attenuations, when the switching frequency is higher than 150kHz., which may do benefit to filter's volume optimization.

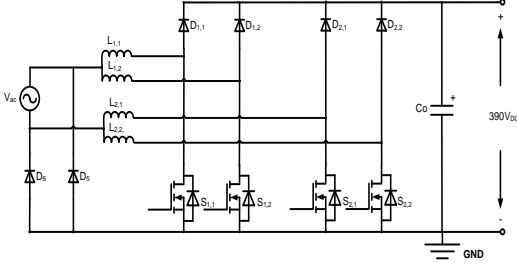


Fig. 4. 2-stage Two-Boost-Circuit IBPFC.

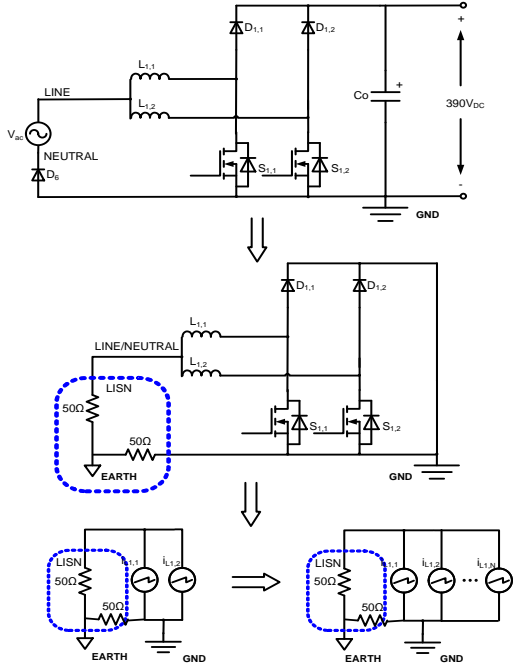


Fig. 5. DM EMI modeling of N -stage interleaved Two-Boost-Circuit BPFC.

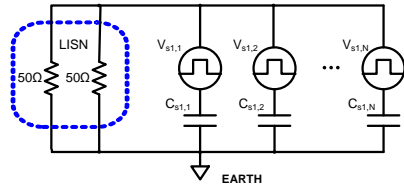


Fig. 6. CM EMI modeling of N -stage interleaved Two-Boost-Circuit BPFC.

Fig. 7 is the simulations of DM and CM EMI comparison between a 2-stage interleaved and a non-interleaved Two-Boost-Circuit BPFC, when the switching frequency f_s is improperly selected at 75kHz. Their 2nd harmonics (150kHz) are the first harmonics which locate inside the EN55013 standard, and they almost have the same values. Because that 150kHz equals to the $k \times N$, when k is 1. Therefore, the same as Eq. (3) has proved, the cutoff frequency of EMI filter in this 2-stage IBPFC should be the same as the non-interleaved BPFC.

It should be noticed that in the simulations in Fig. 7, the model of EMI receiver is not considered. Furthermore, the real EMI performances typically depend strongly on the circuit layout, semiconductor characteristics, gate drivers, operating currents, voltages, temperature and parasitic elements. The actual waveforms above 3MHz are very difficult to predict. Therefore, in this simulation, only the frequency noises below 3MHz are taken into consideration.

B. Efficiency, Power Density and System Complexity Analysis

At light load operating condition, comparing to the non-interleaved BPFC, the main disadvantages of IBPFC is that it increases the number of magnetic components and system complexity. By adding one interleaved stage, not only two extra Boost inductors will be needed but also more gate drives with $1/(N+1)$ times less phase shift are required. Facing the multi-objective requirements in power electronics today, the compromise of power density, efficiency and system complexity must be taken into consideration together.

Since the system's volume is mainly dominated by magnetic components, assuming equal inductances, the energy storage comparison of Boost inductors between N -stage IBPFC and non-interleaved BPFC appears as below [3]:

$$\frac{E_{int,N}}{E_{non}} = \frac{0.5L_{int}(\frac{I}{N})^2 N}{0.5L_{non}I^2} = \frac{1}{N} \quad (4)$$

Eq. (4) shows that: although the number of boost inductors of N -stage IBPFC is $2N$ times higher than those of non-interleaved BPFC, the energy storage on each interleaved inductor is N^2 times lower, which will do benefits on inductor volume reduction.

A multi-objective Boost inductor optimization procedure is

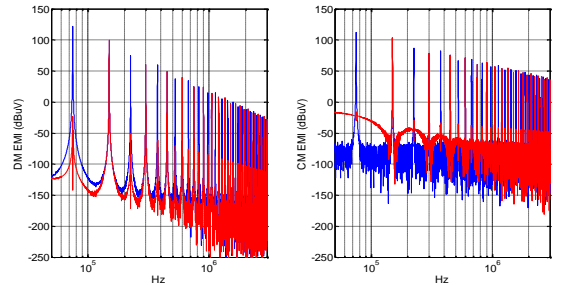


Fig. 7. DM (left) and CM (right) EMI comparison of 2-stage interleaved (red) and non-interleaved (blue) Two-Boost-Circuit BPFC with improper switching frequency.

illuminated in the flowchart in Fig. 8. It takes both the volume, efficiency and EMI reduction of the N -stage IBPFC into consideration. In the optimization, the switching frequency is limited to a fixed region from 50kHz to 70kHz. The start point of this procedure is the specifications definition, which including all the fixed critical parameters in the main circuit. For example: input and output voltages, output peak power, output capacitors, inner parameters of the semiconductors and so on. Next, the important initial starting values of the PFC variables are set. Such as: minimal CCM Boost inductance L_{min} , starting minimal output power $P_{o,min}$, parameters of cores and windings from manufactures. After finishing defining all the specifications and initial values, the mathematical BPFC model will calculate the useful RMS and average currents flowing through all the components in the circuit, finally semiconductor losses and inductor losses can be predicted.

There are three inner optimization loops in the procedure. Inner optimization loop 1 seeks the characteristics of semiconductor losses versus Boost inductance and output power, which will give a most suitable region of Boost inductance at certain power level. Inner optimization loop 2 gets a compromise of volume and efficiency of the Boost inductor. And inner optimization loop 3 is used to analyze EMI reduction. The optimal design can be realized by running these three optimization loops together.

From the optimization, Fig. 9 gives the comparison of minimal volume of high efficient Boost inductors in the interleaved and non-interleaved Two-Boost-Circuit BPFC, when the interleaved stage N varying from 2 to 8 at 3.5kW and 85Vac input. It should be noticed, in this optimization, Kool Mu E cores from Magnetics® were chosen because of their high saturation level, low core losses and cheap price. And, comparing with the traditional round winding, copper foils were selected to reduce the ac winding losses. Moreover, the thickness of the winding were optimized in order to further increase the inductor's efficiency.

From Fig. 9, it can be concluded:

1. With the number of interleaved stages increasing, the single Boost inductor's volume reduces significantly.
2. Due to the number of inductors increasing, except the 3-stage IBPFC, the total inductors' volumes of the IBPFCs are always higher than the non-interleaved BPFC with the same inductance.
3. 3-stage and 4-stage IBPFC has lower total inductor volume among all the IBPFCs. The first one has smaller system volume, and the second one has better EMI.
4. Comparing to 3 or 4 stages IBPFC, the 2-stage IBPFC has slightly higher volume and EMI, but lower cost and less control complexity.

III. BOOST INDUCTOR OPTIMIZATION OF A 2-STAGE IBPFC

A. Optimize Semiconductor Losses in Wide Output Range

According to what has been discussed in Section II Part B, only the 2-stage IBPFC is analyzed in this Section. Because of

the audio application, the IBPFC works in a wide output power range from less than 100W up to 3.5kW, in order to have a relatively flat and high efficiency, it is important that the inductance reduction caused by DC bias will not increase the semiconductor losses a lot. Implement the basic mathematic model of BPFC in reference [13], Fig. 10 shows the relationship of Boost inductance versus semiconductor losses ratio as a function of output power at 85Vac input. From Fig. 10, it is obviously that an inductance about 0.2mH at 300W is a good selection to gain lower semiconductor losses in a wide output power range.

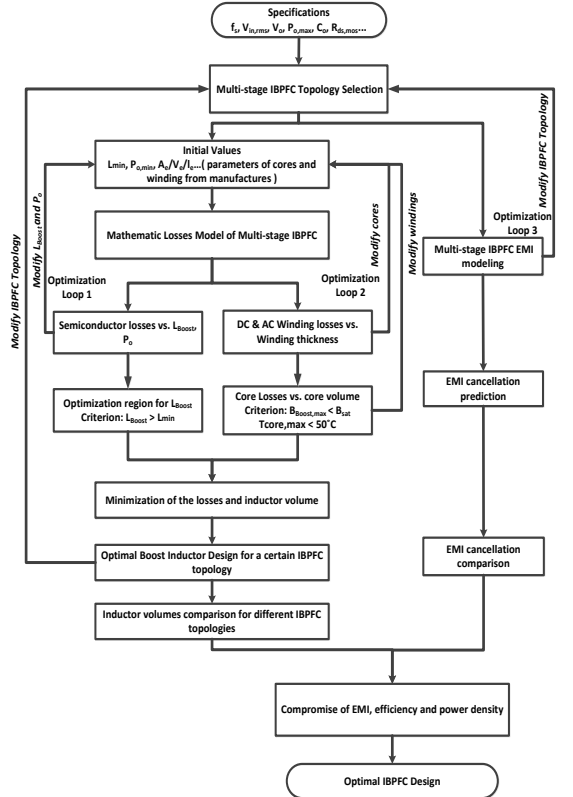


Fig. 8. Flow chart of the optimization procedure of Boost inductor for trading off efficiency and power density.

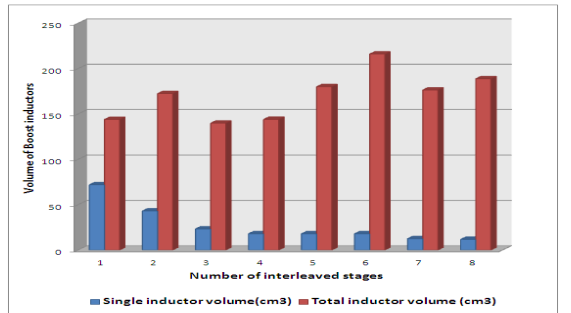


Fig. 9. Minimal single (blue) and total (red) inductor's volume comparison of

interleaved and non-interleaved Two-Boost-Circuit BPFCs.

B. Optimize Boost Inductors - Efficiency vs. Volume

To optimize Boost Inductors based on its efficiency and volume, we start from winding losses prediction. It is well known, winding losses include DC losses and AC losses [14]. To further reduce the winding losses, copper foils were used here. Using the same derivation method in paper [13], Fig. 11 gives the winding losses versus the thickness of copper foil and Boost inductance at 3.5kW output and 85Vac input. It shows that: firstly, in high power applications, the winding losses are dominated by DC losses due to when the thickness of cooper foil reduces, the total winding losses increase rapidly; secondly, for this work, the most useful thickness of the copper foil ranges from 0.15mm to 0.2mm. And thicker copper foil is not very necessary, due to it occupies more window areas in the core but cannot reduce the winding losses very much.

By using the relatively low core-loss Kool Mu cores as an example, Fig. 12 shows the total inductor losses vs. Boost inductance for all the qualified Kool Mu E cores from Magnetics®, when the thickness of copper foil h is 0.15mm. In the legend on the top right corner, the cores were ranked by their sizes, the topper the smaller.

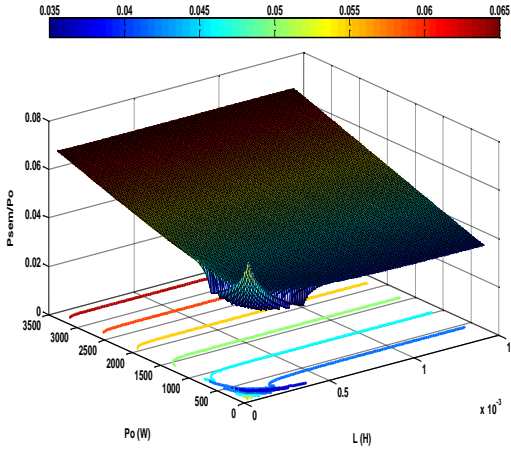


Fig. 10. Semiconductor losses ratio vs. output power and Boost inductance of 2-stage IBPFC.

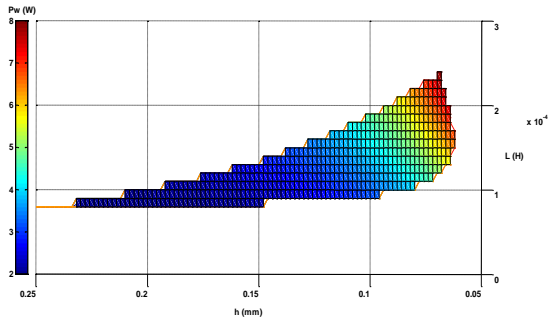


Fig. 11. Winding losses vs. copper foil's thickness and Boost inductance of proposed 2-stage IBPFC.

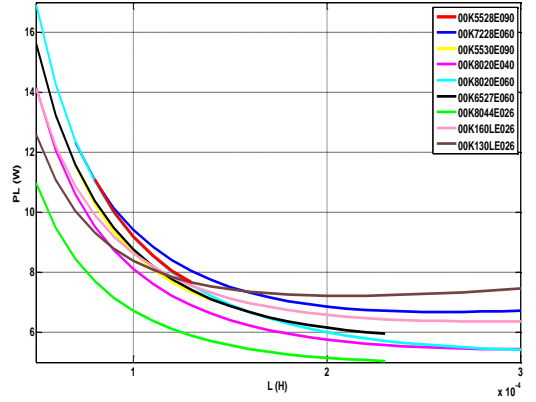


Fig. 12. Inductor losses vs. Boost inductance of proposed 2-stage IBPFC.

TABLE I. OPTIMIZED PARAMETERS OF BOOST INDUCTOR WITH HIGH EFFICIENCY AND POWER DENSITY FOR 2-STAGE IBPFC

Core No.	Winding h (mm)	P_C/P_L at 3.5kW	$\Delta T (^{\circ}C)$	L at 300W (mH)
5528E090	0.15	62.32%	60	0.22

Considering both of the efficiency and power density, the optimized parameters of Boost inductor for the 2-stage Two-Boost-Circuit IBPFC are listed in Table I. Where, P_C is core losses and P_L means total inductor losses.

IV. UNITS FREQUENCY DITHERING AND EMI SUPPRESSION

It is well known that frequency dithering belongs to carrier-frequency modulation (CFM) technique, which can be classified as periodic CFM (PCFM) and random CFM (RCFM) [15-17]. In this section, some important characteristics of frequency dithering regarding to EMI suppression are discussed.

A. Reductions of noise harmonics under cosine frequency dithering function

In this part, the research focuses on PCFM. That means the switching frequency dithers with a small amplitude variation around a central frequency. Considering a standard PWM pulse signal $G(t)$ with a duty ratio D and switching frequency f_s . Assuming $G(t)$ has a high level A and a low level 0 , implementing the Fourier series, $G(t)$ can be expressed as:

$$G(t) = \sum_{n=-\infty}^{+\infty} C_n e^{j\theta_n} \quad (5)$$

Where, C_n and θ_n are the n th series coefficients, which contain the magnitude and phase information of the n th harmonic. And C_n and θ_n can be calculated by:

$$C_n = \frac{1}{T_s} \int_{-\frac{T_s}{2}}^{\frac{T_s}{2}} G(t) e^{-j2\pi f_s n t} dt = \frac{A_j}{2\pi n} (e^{-j2\pi n D} - 1) \quad (6)$$

$$\theta_n(t) = 2\pi f_s t \quad (7)$$

When the switching frequency is modulated by a co-sinusoidal function with a dithering amplitude Δf_s and a dithering rate f_m , the instantaneous frequency and angular rotation of the dithering PWM signal are:

$$f_{ds}(t) = f_s + \Delta f_s \cos(2\pi f_m t) \quad (8)$$

$$\theta_{ds}(t) = 2\pi \int_0^t f_{ds}(t) dt = 2\pi f_s t + \gamma \sin(2\pi f_m t) \quad (9)$$

Where, γ is the dithering factor. It symbolizes the ratio of dithering amplitude and dithering rate. And it is defined as:

$$\gamma = \frac{\Delta f_s}{f_m} \quad (10)$$

Similarly as before, by applying the Fourier series, the dithering PWM signal can be expressed as:

$$G_d(t) = \sum_{n=-\infty}^{+\infty} C_n e^{j\theta_{ds,n}} = \sum_{n=-\infty}^{+\infty} C_n e^{j[\theta_n + \gamma \sin(2\pi f_m t)]} \quad (11)$$

With the derivation results from [18], Eq. (11) can be rewritten into:

$$\begin{aligned} G_d(t) &= \sum_{n=-\infty}^{+\infty} C_n \left\{ \sum_{i=0}^{+\infty} J_i(n\gamma) \left[e^{j(\theta_n + \theta_{m,i})} + (-1)^i e^{j(\theta_n - \theta_{m,i})} \right] \right\} \\ &= \sum_{n=-\infty}^{+\infty} C_n e^{j\theta_n} \left\{ \sum_{i=0}^{+\infty} J_i(n\gamma) \left[e^{j\theta_{m,i}} + (-1)^i e^{j(-\theta_{m,i})} \right] \right\} \end{aligned} \quad (12)$$

Where $\theta_{m,i}$ is the phase angular induced by frequency dithering and can be written as:

$$\theta_{m,i}(t) = 2\pi i f_m t \quad (13)$$

And $J_i(\cdot)$ is the i th order Bessel function:

$$J_i(n\gamma) = \left(\frac{n\gamma}{2} \right)^i \sum_{j=0}^{+\infty} \frac{(-1)^j \cdot \left(\frac{n\gamma}{2} \right)^{2j}}{j!(j+i)!} \quad (14)$$

From Eq. (12) one can see, the harmonics reduction at multiples of central switching frequency f_s can be predicted by setting i equals to 0. And $J_0(\cdot)$ can be written as:

$$J_0(n\gamma) = \sum_{j=0}^{+\infty} \frac{(-1)^j \cdot \left(\frac{n\gamma}{2} \right)^{2j}}{(j!)^2} \quad (15)$$

Therefore, the absolute value of $J_0(\cdot)$ in Eq. (15) shows: comparing to the standard PWM in Eq. (5), the harmonics reductions at multiples of central switching frequency of dithering PWM in Eq. (12). It is easy to see, the harmonics' reduction factor $|J_0(\cdot)|$ is a function of dithering factor γ and the harmonic's order n . The reductions' trends of the key harmonics versus the dithering factor γ are given in Fig. 13, when n changes from 1 to 4.

From Fig. 13, one can conclude that:

1. Dithering PWM has lower amplitudes at multiples of central switching frequency compared to standard PWM.
2. With the same dithering factor, the reductions vary from harmonic to harmonic.
3. When the dither factor increases, each harmonic has its maximum reduction point.

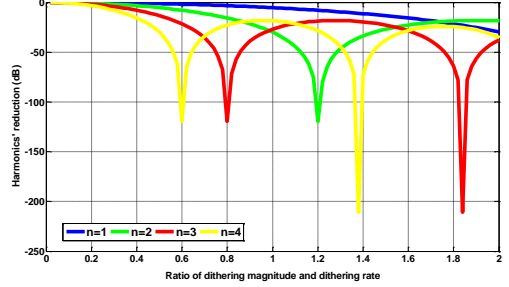


Fig. 13. Harmonics' reduction vs. dithering factor γ when harmonics' order n changes from 1 to 4

B. Limitations of frequency dithering

According to reference [14] has proved, the power spectrum of dithering PWM signal in Eq. (12) in positive frequency range can be expressed as:

$$\begin{aligned} S_d(f, \gamma) &= S(f, \gamma) + \Delta S(f, \gamma) = 2 \left| \sum_{n=1}^{\infty} C_n \left[J_0(n\gamma) \cdot \delta(f - nf_s) \right] \right|^2 + \\ &2 \left| \sum_{n=1}^{\infty} C_n \left\{ \sum_{i=1}^{\infty} J_i(n\gamma) \cdot \left[\delta(f - nf_s - if_m) + (-1)^i \delta(f - nf_s + if_m) \right] \right\} \right|^2 \end{aligned} \quad (16)$$

Where $S(f, \gamma)$ is the original power spectrum of standard PWM signal and $\Delta S(f, \gamma)$ is the spread spectrum caused by frequency dithering.

a) The limitations of central harmonics reductions

Through Fig. 13 and Eq. (16), it is not difficult to find out that in the dithering PWM, the central harmonics' reductions are limited by γ . Furthermore, in a fixed γ frequency dithering system, it is more reasonable to expect large harmonics' reductions only happening at certain frequencies not in the whole frequency range.

b) Spectrums overlapping and redistribution

According to paper [19] and Eq. (12), the dithering will also lead upper and lower sidebands at multiples of central switching frequency f_s and the bandwidth of the n th harmonic can be approximately calculated by:

$$B_n = 2(n\gamma + 1) \cdot f_m = 2(n\Delta f_s + f_m) \quad (17)$$

Fig. 14 shows the harmonics' spectrum comparison of a standard PWM and a dithering PWM [19]. Assuming the sum of the right and left bandwidths of the n th and $(n+1)$ th harmonics is:

$$B_{sum} = \frac{1}{2}(B_n + B_{n+1}) = (2n+1)\Delta f_s + 2f_m \quad (18)$$

Therefore, when B_{sum} is higher than f_s , these two sidebands will overlap each other. The same as what has shown in Fig. 14, the harmonics' power in the overlapping area of dithering PWM will be higher than standard PWM. This means, the smaller the f_s is, the larger the overlapping areas could be and the more power from the $(n+1)$ th harmonic and its lower sidebands will be pushed into the higher sidebands of n th harmonic. This is why normally when measuring the EMI from a frequency dithering system, comparing to the non-dithering system, the dithering system usually pushes the EMI from the high frequency domain into the low frequency domain.

V. EMI FILTER DESIGN CONSIDERATIONS

According to what has been mentioned in Section IV, the limitations of frequency dithering technique will definitely harm its EMI performance and impact the EMI filter design. Considering the harmonics spectrums of standard PWM and dithering PWM in Fig. 15, the filter's attenuation character is given in the red line. If the cutoff frequency of the filter at minus 20dB/dec frequency band is f_{ζ} for standard PWM, the filter's attenuation at multiple of switching frequency nf_s is:

$$\alpha_n = -20\zeta \lg \frac{nf_s}{f_{\zeta}} - A_{\zeta} \quad (19)$$

Where ζ is related to filter's type, it is a function of filter's order and structure, and A_{ζ} is the filter's attenuation at f_{ζ} .

Therefore, after filtering, the harmonics' amplitude at nf_s is:

$$X_n = 20\lg|C_n \cdot J_0(n\gamma)| + \alpha_n \quad (20)$$

Similarly, in the frequency dithering PWM, the filter's attenuations around multiple of switching frequency nf_s can be calculated as:

$$\beta_{n,k} = -20\zeta \lg \frac{nf_s + f_m \cdot k}{f_{\zeta}} - A_{\zeta} \quad (21)$$

Where k symbolizes the spread spectrum caused by frequency dithering. According to Eqs. (12) and (16), each spread spectrum has a frequency interval of f_m . By utilizing Eq. (17), the parameter k varies from $-\lfloor n\gamma + 1 \rfloor$ to $\lfloor n\gamma + 1 \rfloor$. In where, ' $\lfloor x \rfloor$ ' is the floor function, which returns the smallest integer not larger than x .

Therefore, after filtering, the harmonics amplitude around nf_s becomes:

$$Y_{n,k} = 20\lg|C_n \cdot J_{Z+k}(n\gamma)| + \beta_{n,k} \quad (22)$$

Where Z equals to $\lfloor n\gamma + 1 \rfloor$.

Unlike the constant frequency system, due to the EMI receiver has the impact on the final EMI measurement results of a frequency dithering system through its inner resolution bandwidth (RBW) filter [20]. In order to predict the EMI performance of a frequency dithering system correctly, the

model of EMI receiver cannot be neglected. According to what has been proved in reference [21], it should be precise enough to predict the measured EMI result at each frequency by only considering the harmonics located inside the 9kHz inner band pass filter of the EMI receiver.

Set X equals to the maximum value of k which satisfies that:

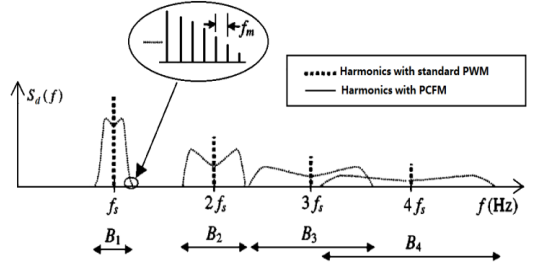


Fig. 14. Harmonics' spectrum comparison [19]

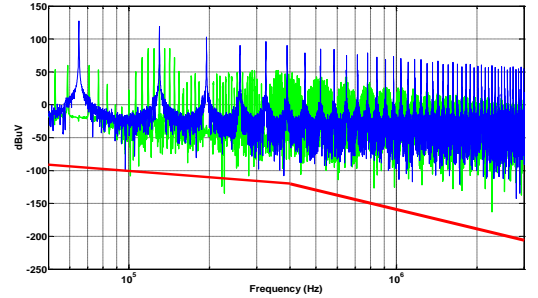


Fig. 15: Harmonics' spectrum comparison, dithering PWM (green) and standard PWM (blue), the red line is the filter's attenuation characteristics.

$$\frac{9kHz}{X \cdot f_m kHz} \geq 1 \quad (23)$$

The measured peak and average harmonics' amplitudes of dithering PWM displayed on the EMI receiver at nf_s can be predicted as below:

$$\hat{Y}_{n,Pk} = \{Y_{n,k}\}_{\max}, (k \leq |X|) \quad (24)$$

$$\tilde{Y}_{n,Av} = \frac{1}{2X} \sum_{k=-X}^X Y_{n,k} \quad (25)$$

Where, Pk. means peak value and Av. means average value. Compare Eqs. (20), (24) and (25), after filtering significant harmonics' reduction from dithering PWM may exhibit if $\tilde{Y}_{n,Av}$ far below X_n .

VI. EXPERIMENTAL VERIFICATIONS

After carefully design the 65kHz 2-stage IBPFC, the key components' information is provided in Table II. Comparison of the system's efficiency, which were measured by digital power meter PPA5530 from N4L[®], at different line voltages are drawn in Fig. 16. The predicted system's key components losses

distributions at the same operating situation are given in Fig. 17 based on the multi-objective procedure. Compare the results between measurements and calculations, the differences are below 1%. Figs. 18 and 19 give the measured input voltage and current waveforms of the proposed 2-stage IBPFC at 3.5kW in 110Vac and 230Vac input.

According to the special focus of the audio application, Fig. 20 gives the EMI measurement of the 2-stage IBPFC and a traditional BPFC at one eighth of full power without filters. In order to make a fair comparison, all the components and testing equipments selected for the 2 topologies are the same.

TABLE II. KEY COMPONENTS USED IN THE 2-STAGE IBPFC PROTOTYPE

Device	Part No.	No. of devices
Fast Diode	STPSC1206	4
Return Diode	STTH6004W	2
MOSFET	IPW60R045CP	4
Inductor	5528E090 core	4

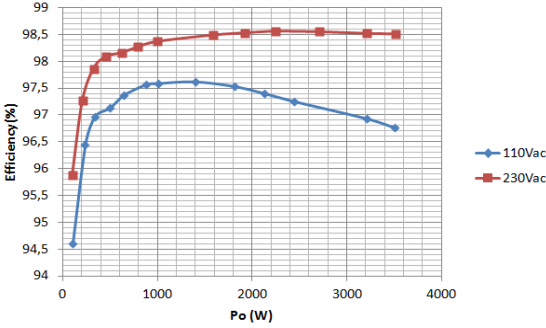


Fig. 16. Efficiency comparison of 2-stage IBPFC at different input voltages.

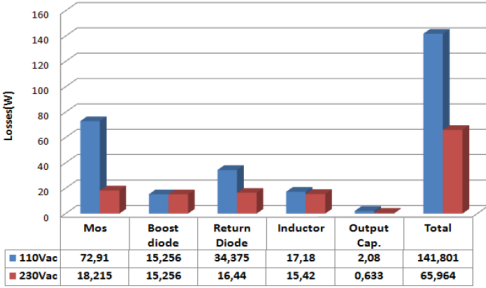


Fig. 17. Key components losses distributions of the 2-stage IBPFC in different input voltages at 3.5kW.

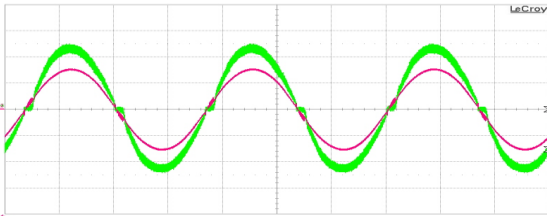


Fig. 18. Input voltage (red 100V/div) and current (green 20A/div) waveforms from 2-stage IBPFC at 3.5kW and 110Vac, PF=99.5%.

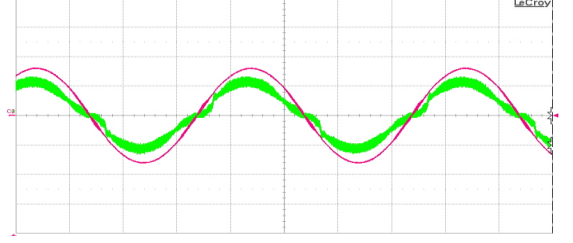
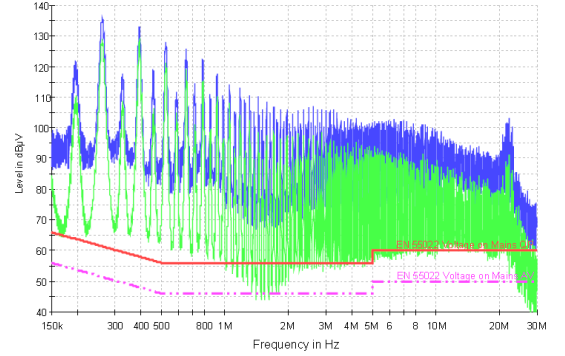
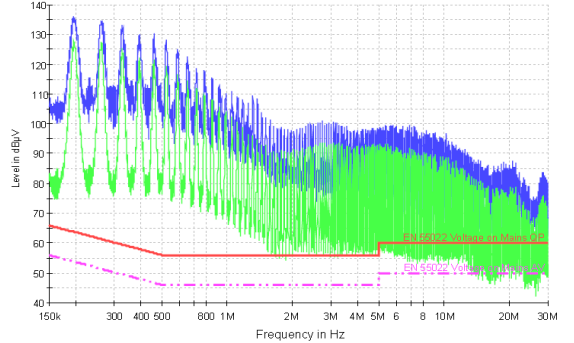


Fig. 19. Input voltage (red 200V/div) and current (green 20A/div) waveforms from 2-stage IBPFC at 3.5kW and 230Vac, PF=99.2%.



(a) Proposed 2-stage IBPFC



(b) Traditional non-interleaved BPFC

Fig. 20. EMI comparison of the 2-stage IBPFC and non-interleaved BPFC at 1/8 of full power and 110Vac input (Pk. value in blue, Av. value in green).

Fig. 20 shows that in the 2-stage IBPFC, the odd harmonics can be reduced due to phase shift.

According to the EN55013 standard, the highest harmonic's amplitude of the proposed IBPFC, which needs to be attenuated, locates at 260kHz (the 4th order harmonic). As what shows in Fig. 13, for further increasing the attenuation at 260kHz, a dithering amplitude Δf_s of 7.55kHz and dithering rate f_m of 6.1kHz are selected. This leads a dithering factor γ at 1.24, and gives a 33.15dB reduction at the 4th harmonic.

Fig. 21 shows the EMI measurements of the proposed 2-stage IBPFC with optimal frequency dithering. Additionally, in Fig. 22, there is the detailed amplitudes' comparison of 4 highest harmonics in Fig. 20 (a) and Fig. 21.

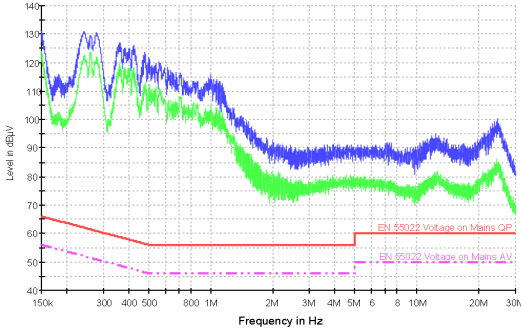


Fig. 21: Conducted EMI of the proposed frequency dithering IBPFC at 110Vac input and 1/8 of full power and no filter (Pk. value in blue, Av. value in green).

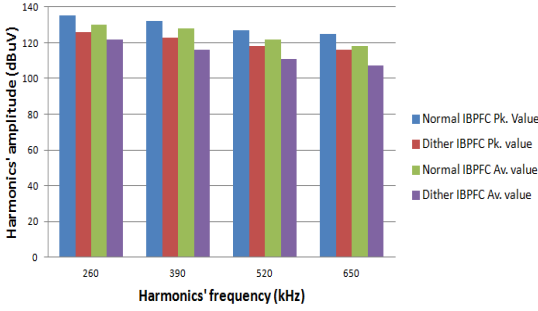


Fig. 22: Detailed EMI comparison of 4 highest harmonics in Figs. 20 (a) and 21.

TABLE III. EMI COMPARISON OF CRITICAL HARMONICS

Harmonics' frequency (kHz)		260		390		520		650	
EMI detector		Pk.	Av.	Pk.	Av.	Pk.	Av.	Pk.	Av.
Dither IBPFC (dBuV)	P.	125	124	121	116	115	107	112	109
	M.	126	122	123	116	118	111	116	107
Prediction error (dBuV)		-1	2	-2	0	-3	-4	-4	2

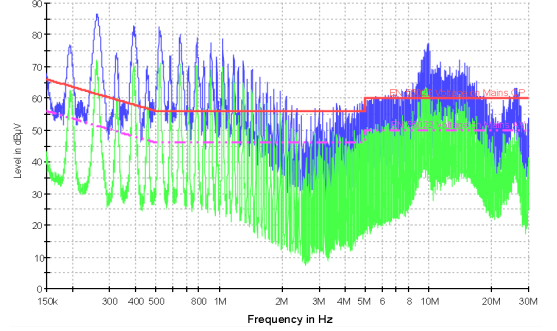
By implementing the derived mathematical models in Sections IV and V, Table III gives the harmonics' amplitudes comparison in Fig. 22 between experiments and theoretical predictions of the proposed frequency dithering IBPFC. Where, P. means predicted values and M. means measured values.

From Table III, it can be proved that using the mathematical method mentioned in Sections IV and V, the EMI performances of the frequency dithering IBPFC can be predicted approximately.

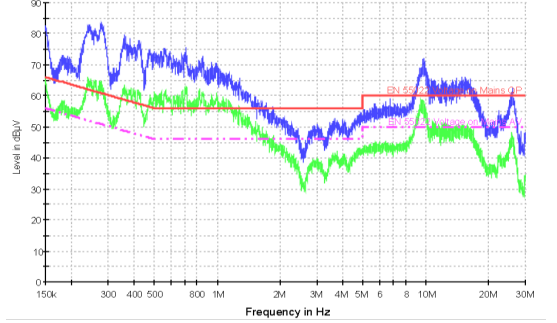
Fig. 23 shows the EMI measurement of the 2-stage IBPFC and the proposed frequency dithering IBPFC with the same filter at one eighth of full power. Figs. 21 and 23 together prove that the EMI generated by frequency dithering PWM is lower and easier to attenuate by EMI filter than normal IBPFC. And by combining of interleaved and frequency dithering, better EMI reduction can be achieved.

Fig. 24 gives the input current harmonics comparison of the 2-stage IBPFC and the proposed frequency dithering IBPFC at

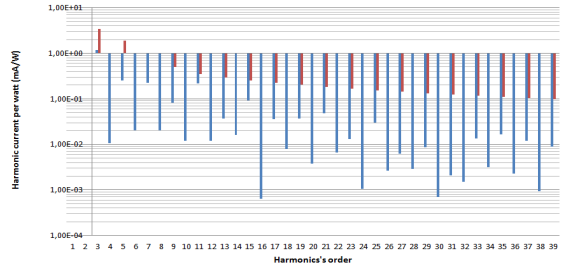
one eighth of full power. It shows that frequency dithering doesn't increase the input current harmonics very much.



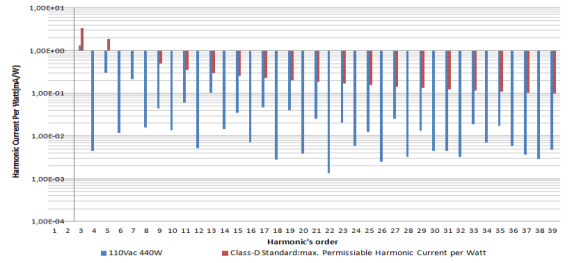
(a) Standard IBPFC, Pk. value in blue, Av. value in green



(b) Proposed frequency dithering IBPFC, Pk. value in blue, Av. value in green
Fig. 23: Conducted EMI comparison of standard IBPFC and proposed frequency dithering IBPFC at 110Vac and 1/8 peak power with the same filter.



(a) Standard IBPFC



(b) Proposed frequency dithering IBPFC

Fig. 24: Input current harmonics comparison of standard IBPFC and proposed frequency dithering IBPFC at 110Vac and 1/8 peak power.

VII. CONCLUSION AND FUTURE WORKS

In this paper, a systematic research on analysis and optimal design of a high efficiency IBPFC for class-D amplifiers is proposed. The multi-objective optimization procedure is implemented to meet the compromise of system efficiency, power density, EMI reduction and complexity. Moreover, the insights into the advantages and limitations of EMI suppression using frequency dithering are presented. The experiments prove the theoretical analysis and simulations.

According to the discussion in Section V, in the future, it will be a meaningful exploration to develop an optimized design of EMI filter under frequency dithering condition to achieve maximum EMI reduction and lowest filter' volume together. This will be a very useful combination of research and industrial application.

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APPENDIX B

C++ Code Fragment

B.1 Common Header

./code/PFCSim/com.h

```
#define SQRT2 1.4142
#define PI 3.1415927

#define frequency 50 //AC line frequency
#define sample_fre 65000 //switching frequency of converter
#define half_cycle_click (sample_fre/(frequency*2)) //total
    sample times in a half duty cycle.

#define G1(fi) (sinh(2*fi)+sin(2*fi))/(cosh(2*fi)-cos(2*fi))
#define G2(fi) (sinh(fi)*cos(fi)+cosh(fi)*sin(fi))/(cosh(2*fi)-cos
    (2*fi))
```

B.2 Header for Magnetic Core

./code/PFCSim/MagCore.h

```
/*
defined for Cores
*/
#include "com.h"
```



```

#include <String>
using namespace std;

class MagCore
{
public:
    MagCore(double Le, double Ve, double Ae, double Al, double Per)
        ;
    double getVe() const;
    double GetLoopN(double L);
    double GetLoopN(double L, double Iin); //calculate the number of
        loop it should have when inductance is given
    double CalcL_from_N_I(double N, double Iin);
    double Get_Kvol(); //get the volume of core
    double Get_H(double N, double ipeak); //calculate Magnetizing
        Force H
    double Get_K_a(); //get coefficient K_a for calculating core
        loss
    double Get_KBav(double N);

    //use "=0" to defined it as pure virtual function, so it doesn'
        t have function body, otherwise I have to write it in .cpp
        file
    virtual double Get_K_b()=0; //get coefficient K_b for
        calculating core loss
    virtual double Get_SurfaceArea()=0; //the unit of return value
        is depend on the dimension of core, such as A, B, C, M and
        so on
    virtual double Get_ff(double N, double dwidth)=0; //calculate
        fill factor
    virtual double Get_Krdc(double N, double dwidth)=0;
    virtual double Get_Fr(double N, double h, double fre)=0;
    virtual double Get_fi(double h, double fre)=0;
    void SetAl(double Al);
    void SetPartNumber(std::basic_string<char> & strname);
    std::basic_string<char>& GetPartNumber();

    //set room temperature to 20 degree
    static const int dRoomTemper=20;

private:
    double _Le; //length of magnetic path of core
    double _Ve; //volume of core
    double _Al; //nominal inductance of core
    double _Ae; //cross section of core

    double _permeability;
protected:
    std::basic_string<char> spartnumber;
};

//derived class for E core
class MagECore: public MagCore

```



```

double Get_Fr(double N, double h, double fre);

struct _wire_table
{
    int isize;
    double rpm; //resistance per meter
    double heavyBuild;
};
typedef struct _wire_table WTABLE;
private:
    double dA; //A, outer radius
    double dB; //B, inner radius
    double dC; //C, thickness of core
    double dSa; //surface area is indicated in the datasheet.
    double dLw; //Lwinding, the length of the winding, unit: mm

    static const int iwt=1;
    static const WTABLE mWTable[iwt];
    //the unit of return value is resistance/meter
    double get_r_p_m(int iwiresize);
    double get_hb(int iwiresize);
};

```

B.3 Function for Magnetic Core

./code/PFCSim/MagCore.cpp

```

#include "com.h"
#include "MagCore.h"

MagCore::MagCore(double Le, double Ve, double Ae, double Al, double
    Per)
{
    _Le = Le;
    _Ve = Ve;
    _Ae = Ae;
    _Al = Al;

    _permeability = Per;
}

double MagCore::getVe() const
{
    return _Ve;
}

void MagCore::SetAl(double Al)
{
    _Al = Al;
}

```

```

void MagCore::SetPartNumber(std::basic_string<char> &strname)
{
    spartnumber = strname;
}

std::basic_string<char>& MagCore::GetPartNumber()
{
    return spartnumber;
}

double MagCore::Get_K_a()
{
    int per = (int)(_permeability);
    double ret;

    switch(per)
    {
        case 26:
        case 40:
            ret = 1.6;
            break;
        case 60:
        case 90:
            ret = 1.46;
            break;
        default:
            ret = 1.46;
            break;
    }

    return ret;
}

double MagCore::GetLoopN(double L)
{
    return sqrt(L*1.0e9/_A1*(1-0.08));
}

double MagCore::GetLoopN(double L, double Iin)
{
    double N, ni, k=0;
    int per = (int)(_permeability);
    double p[5];

    N = sqrt(L*1.0e9/_A1*(1-0.08));
    ni = N*Iin/(2*_Le/10);
    cout<<"ni:"<<ni<<" ,_N:"<<N<<" ,_Le"<<_Le<<"\n";
    switch(per)
    {
        case 90:
            //y = -1E-09x4 + 2E-07x3 + 6E-05x2 - 0.015x + 1.0235
            p[4] = 2e-10;
            p[3] = -2e-7;
            p[2] = 1e-4;
            p[1] = -0.0159;

```

```

        p[0] = 1.0272;
        break;
    case 60:
        //y = -6E-10x4 + 4E-07x3 - 3E-05x2 - 0.006x + 1.0089
        p[4] = -7e-12;
        p[3] = -2e-8;
        p[2] = 3e-5;
        p[1] = -0.0091;
        p[0] = 1.0344;
        break;
    case 40:
        //y = -3E-09x4 + 8E-07x3 - 8E-05x2 - 0.0018x + 1.0025
        p[4] = 7e-12;
        p[3] = -2e-8;
        p[2] = 1e-5;
        p[1] = -0.0057;
        p[0] = 1.032;
        break;
    case 26:
        //y = -5e-11x4 + 5e-8x3 - 1e-5x2 - 0.0014 + 1.0021
        p[4] = -3e-12;
        p[3] = 5e-9;
        p[2] = 3e-7;
        p[1] = -0.0028;
        p[0] = 1.0225;
        break;
    default:
        return -1;
        break;
}

for(int i=0; i<5; i++)
{
    k += p[i]*pow(ni, i);
}

double ret = N/sqrt(k);
return ret;
}

double MagCore::CalcL_from_N_I(double N, double Iin)
{
    double ni = N*Iin/(2*_Le/10);
    int per = (int)(_permeability);
    double p[5], k=0;

    switch(per)
    {
    case 90:
        //y = -1E-09x4 + 2E-07x3 + 6E-05x2 - 0.015x + 1.0235
        p[4] = -1e-9;
        p[3] = 2e-7;
        p[2] = 6e-5;
        p[1] = -0.015;
        p[0] = 1.0235;

```

```

        break;
    case 60:
        //y = -6E-10x4 + 4E-07x3 - 3E-05x2 - 0.006x + 1.0089
        p[4] = -6e-10;
        p[3] = 4e-7;
        p[2] = -3e-5;
        p[1] = -0.006;
        p[0] = 1.0089;
        break;
    case 40:
        //y = -3E-09x4 + 8E-07x3 - 8E-05x2 - 0.0018x + 1.0025
        p[4] = -3e-9;
        p[3] = 8e-7;
        p[2] = -8e-5;
        p[1] = -0.0018;
        p[0] = 1.0025;
        break;
    case 26:
        //y = -5e-11x4 + 5e-8x3 - 1e-5x2 - 0.0014 + 1.0021
        p[4] = -5e-11;
        p[3] = 5e-8;
        p[2] = -1e-5;
        p[1] = -0.0014;
        p[0] = 1.0021;
        break;
    default:
        return -1;
        break;
}

for(int i=0; i<5; i++)
{
    k += p[i]*pow(ni, i);
}

return k*_A1*N*N/(1.0e9*(1-0.08));
}

double MagCore::Get_KBav(double N)
{
    return 1.0/N/2/(_Ae/100);
}

double MagCore::Get_Kloss()
{
    return 1.0*_Ve/1000;
}

double MagCore::Get_H(double N, double ipeak)
{
    return N*ipeak/2/_Le*4*M_PI;
}

double MagECore::Get_K_b()
{

```

```

        return 2;
    }

    double MagECore::Get_Kl(double N)
    {
        return 2*(dF+dC)*N;
    }

    double MagECore::Get_Am(double h)
    {
        return h*2*(dD-1);
    }

    double MagECore::Get_Krdc(double N, double h)
    {
        return 1.724e-6*10*Get_Kl(N)/Get_Am(h);
    }

    double MagECore::Get_ff(double N, double h)
    {
        return N*(h+0.1)/dM;
    }

    MagECore::MagECore(char *pstr,
                        double A,
                        double B,
                        double C,
                        double D,
                        double F,
                        double L,
                        double M,
                        double Ve,
                        double Ae,
                        double Le,
                        double Al,
                        double Per):MagCore(Le, Ve, Ae, Al, Per)
    {
        spartnumber = std::basic_string<char>(pstr);

        dA = A;
        dB = B;
        dC = C;
        dD = D;
        dF = F;
        dL = L;
        dM = M;
    }

    double MagECore::Get_SurfaceArea()
    {
        return 2*dA*dC+2*2*dB*dC+2*(2*dB*dA-2*2*dD*dM);
    }

    double MagECore::Get_fi(double h, double fre)
    {

```

```

    double KDelta;

    KDelta = 7.5/sqrt(fre);
    return h/10/KDelta;
}

double MagECore::Get_Fr(double N, double h, double fre)
{
    double fi;

    fi = Get_fi(h, fre);
    return fi*(G1(fi)+2.0*(N*N-1)/3*(G1(fi)-2*G2(fi)));
}

//initialize the const structure array in .cpp file
//don't add "static" qualifier, it is only used during class
// declaration
// wire size, resistance per meter, radius of winding(unit,
// mm)
const MagToroidCore::WTABLE MagToroidCore::mWTable[]={
    {19, 0.0264, 0.98},
};

double MagToroidCore::Get_K_b()
{
    return 2.25;
}

MagToroidCore::MagToroidCore(char *pstr,
                             double A,
                             double B,
                             double C,
                             double Ve,
                             double Ae,
                             double Le,
                             double Al,
                             double Per):MagCore(Le, Ve, Ae, Al,
                             Per)
{
    spartnumber = std::basic_string<char>(pstr);

    dA = A;
    dB = B;
    dC = C;

    /*
    area of side: pi*(A/2)^2-pi*(B/2)^2
    area of inner cross section: C*(pi*B)
    area of outer cross section: C*(pi*A)
    */
    dSa = M.PI*((dA*dA-dB*dB)/2 + dC*(dA+dB));
    /*
    length of one turn of winding
    */
    dLw = (dC+(dA-dB)/2)*2;

```



```

}

double MagToroidCore::Get_ff(double N, double h)
{
    /*
    Waw: area of cross section of windings
    */
    double Waw;

    Waw = pow(h/2, 2)*M_PI;
    return N*Waw/M_PI/pow(dB/2, 2);
}

double MagToroidCore::Get_SurfaceArea()
{
    return dSa;
}

double MagToroidCore::Get_fi(double h, double fre)
{
    double KDelta;

    KDelta = 7.5/sqrt(fre);
    //as to Toroid core, thickness of winding is higher than copper
    foil
    return h/10/KDelta*sqrt(0.8*M_PI/4);
}

double MagToroidCore::Get_Fr(double N, double h, double fre)
{
    double fi;
    double N0;

    fi = Get_fi(h, fre);
    N0 = h*N/(M_PI*dB);
    return fi*(G1(fi)+2.0*(N0*N0-1)/3*(G1(fi)-2*G2(fi)));
}

double MagToroidCore::Get_Krdc(double N, double h)
{
    double rpm = get_r_p_m(h);

    return N*dLw*1.0e-3*rpm;
}

double MagToroidCore::get_r_p_m(int iwiresize)
{
    for(int i=0;i<iwt;i++)
    {
        if(mWTable[i].isize == iwiresize)
            return mWTable[i].rpm;
    }

    return 0;
}

```

```
double MagToroidCore::get_hb(int iwiresize)
{
    for(int i=0;i<iwt;i++)
    {
        if(mWTable[i].isize == iwiresize)
            return mWTable[i].heavyBuild;
    }

    return 0;
}
```

B.4 Loop 1

./code/PFCSim/loop1.cpp

```
/*
Loop 1: Boost inductance optimization
*/
int main_entry_loss_p1()
{
#define PO_MIN 100
#define N_PO 137
#define STEP_PO 25
#define L_MIN 50e-6
#define N_L 140
#define STEP_L 10e-6
    mwArray Vloss(N_PO, N_L, mxDOUBLE_CLASS);
    mwArray Vl(1, N_L, mxDOUBLE_CLASS);
    mwArray Vp(1, N_PO, mxDOUBLE_CLASS);
    mwArray para("g");
    double *pp,*pl,*ploss, dloss;
    int i, j;

    pp = new double[N_PO];
    pl = new double[N_L];
    ploss = new double[N_L*N_PO];
    memset(ploss, 0, sizeof(double)*N_L*N_PO);
    for(i=0; i<N_PO; i++)
        *(pp+i) = PO_MIN+i*STEP_PO;
    for(i=0; i<N_L; i++)
        *(pl+i) = L_MIN+i*STEP_L;
    for(i=0; i<N_PO; i++)
    {
        Po = PO_MIN+STEP_PO*i;
        Io = Po/Vo;

        for(j=0; j<N_L; j++)
        {
            L = *(pl+j);
            Ln = L*Io/(Vo*Ts);

            dloss = calc_loss();
```

```

        *(ploss+i+j*N_PO) = Psemi/Po;
    }
}

Vl.SetData(pl, N_L);
Vp.SetData(pp, N_PO);
Vloss.SetData(ploss, N_L*N_PO);
draw3d(Vl, Vp, Vloss, para);
delete [] pp;
delete [] pl;
delete [] ploss;

return 0;
}

```

B.5 Loop 2

./code/PFCSim/loop2.cpp

```

/*
Loop 2: Optimization of Inductor losses vs. its volume
*/
int main_entry_p_h_lex(char *strcore)
{
#define STEP_h 0.002 //step of winding thickness h, unit: mm
#define STEP_L 10e-6 //step of inductor L, unit: H
#define L_MIN 50e-6 //minimum value of inductor L, unit: H
#define H_MIN 0.05 //minimum value of winding thickness h, unit: mm
#define N_h 126 //number of available value of h which ranges from
H_MIN to 0.3mm
#define N_L 156 //number of available value of inductor L
double h=H_MIN;
double dloss, N, H;
double ff, temp;
int i, j;
try{
    MagECore &core = find_core(strcore);

    k_a = core.Get_K_a(); //get a parameter k_a to calculate
core loss
    k_b = core.Get_K_b(); //get a parameter k_b to calculate
core loss
    std::ofstream ost(core.GetPartNumber().c_str());
    for(i=0; i<N_h; i++)
    {
        h = H_MIN+i*STEP_h;
        for(j=0; j<N_L; j++)
        {
            L = L_MIN+j*STEP_L;
            //normalized value of inductor L, Ts is period of
switching frequency fs
            Ln = L*Io/(Vo*Ts);

```

```

//find out the number of windings needed with given
//inductor and given current assuming efficiency
//is 90%.
N = core.GetLoopN(L, Po/0.9/Vin_rms);
//The AC winding losses increase by Fr factor due
//to the proximity effect
Fr = core.Get_Fr(N, h, sample_fre);
//calculate a factor used for calculating DeltaB,
//formula: 1/(N*2*Ae)
K_Bav = core.Get_KBav(N);
K_Vol = core.Get_Kvol(); //get the volume of core
ff = core.Get_ff(N, h); //calculate fill factor.
if (ff > 0.65)
{
    //increasing inductor value without changing
    //winding thickness would make ff
    //more larger, need to break
    cout<<"break_due_to_oversize_of_fill_factor:_"  

    <<ff<<"\n";
    break;
}

H = core.Get_H(N, getIl_peak()); //calculate
//Magnetizing Force with turns N and peak current
if (H>150)
{
    cout<<"break_due_to_saturated,_H:_"<<H<<"\n";
    break;
}
//calculate dc resistance of copper foil
K_rdc = core.Get_Krdc(N, h);
//calculate total power losses of the converter
//using the losses model of the converter
dloss = calc_loss();
//calculate temperature of core with the total
//inductor losses and its surface area.
temp = pow((Loss_l*1000)/(core.Get_SurfaceArea()
/100), 0.833)+core.dRoomTemper;
if (temp>dtemper_limit)
{
    cout<<"continue_because_temperature_is_too_high
:_"<<temp<<"\n";
    continue;
}
ost<<h<<"_"<<L<<"_"<<dloss<<"\n";
}
}
ost.flush();
}
catch(exception &error)
{
    cout<<error.what()<<"stop_calculation\n";
    return -1;
}

```

```

    cout<<"over!\n";
    return 0;
}

```

B.6 Loop 3

./code/PFCSim/loop3.cpp

```

/*
Loop 3: EMI reduction vs. number of interleaved stages
*/
//generate transient input voltage
inline double gVin(double t)
{
    return Vin*sin(PI*t/Ti);
}

//generate transient input current
inline double gIin(double t)
{
    return Iin*sin(PI*t/Ti);
}

//generate on time for current period
inline double gTon(double V)
{
    return (1-V/Vo)*Ts;
}

#define C_DMOS1(d, i, v) \
{ \
    d = sqrt(2*(1-v/Vo)*(i/Io)*Ln/(v/Vo)); \
} \

#define C_DD1(d, i, v) \
{ \
    d = sqrt(2*v/Vo*i/Io*Ln/(1-v/Vo)); \
} \

//calculate transient current of one MOSFET under DM mode
double calc_it_dm(double t, double tb)
{
    double _v=gVin(t);
    double d;

    if(t-tb<=Ton)
    {
        //when MOSFET is on
        vsig_t.push_back(0); //save transient voltage of one MOSFET
        C_DMOS1(d, gIin(t), _v);
        return _v/L*d*Ts;
    }
    else if(t-tb<=Toff)

```

```

{
    //when MOSFET is off and the current of MOSFET is larger than 0
    vsig_t.push_back(390); //save transient voltage of one
        MOSFET
    C_DD1(d, gIin(t), _v);
    return (Vo-_v)/L*d*Ts;
}
else
{
    //when MOSFET is off
    vsig_t.push_back(390);
    return 0;
}
}

//calculate transient current of one MOSFET under CM mode
double calc_it_cm(double t, double tb)
{
    double _v=gVin(t);

    if(t-tb<=Ton)
    {
        //when MOSFET is on
        vsig_t.push_back(390); //save transient voltage of one
            MOSFET
        return _v/L*(t-tb);
    }
    else
    {
        //when MOSFET is off
        vsig_t.push_back(0); //save transient voltage of one MOSFET
        return (Vo-_v)/L*(Ts-(t-tb));
    }
}

//calculate transient current and voltage for EMI simulation
//sample 1000 points in one period Ts
double calc_it_vt()
{
    long i;
    double Vit, Iit, t;
    double Dmos1, Dmos2;
    double Dd1, Dd2;
    double D11;

    update_para();
    vdeltaI.clear();
    vdelta_t.clear();
    vt.clear();
    vsig_t.clear();
    vsig.clear();

    for(i=0; i<half_cycle_click; i++)
    {

```

```

t = i*Ts;
Vit = gVin(t);
Ton = gTon(Vit);
Vit = gVin(t+Ton/2); // calculate the voltage in the middle
                        point
Iit = gLin(t+Ton/2);
Dmos1 = sqrt(2*(1-Vit/Vo)*(Iit/Io)*Ln/(Vit/Vo));
Dmos2 = Ton/Ts;
Dd1 = sqrt(2*Vit/Vo*Iit/Io*Ln/(1-Vit/Vo));
Dd2 = 1-Dmos2;
Dl1 = Dmos1+Dd1;
Toff = Dd1*Ts;

for(int j=0; j<1000; j++)
{
    double it, tt;
    tt = i*Ts+j*Ts/1000;
    vt.push_back(tt);

    if(allcase1>0 || (allcase2<=0&&(tt<=Tin || tt>=(Ti-Tin)
        )))
        it = calc_it_dm(tt, t);
    else
        it = calc_it_cm(tt, t);
    vdelta_t.push_back(it);
}
}

return 0;
}

```

B.7 Model of losses

./code/PFCSim/calc_loss.cpp

```

/*
Multi-stage IBPFC Losses Model
*/
#define RSENSE 18 // current sense resistor
#define RESR 7.6e-2 //the ESR of the output capacitor

const double RDS = 0.045; //MOSFET chip type:IPW60R045CP
const double Vd = 1.7; //forward voltage of Boost Diode STPSC1206
//const double Vd_dl = 0.83; //forward voltage of Return Diode
//STTH6004W
const double Vd_dl = 1.1; //forward voltage of Return Diode
//STTH6006W

double Po = 3500.0;
double T_ON = 0.00000005; //turn on delay plus rise time unit: s
double T_OFF = 0.00000011; //turn off delay plus fall time unit: s
double Vo = 390; //ouput voltage
double Io = Po/Vo; //output current

```

```

double Ti = 1.0/(frequency*2.0); //full duty cycle:50Hz, half duty
    cycle:100Hz
double Ts = 1.0/sample_fre; //one period, sample rate:50KHz
double L = 100.0e-6; //Boost Inductor, unit: H
double Ln = L*Io/(Vo*Ts); //nomalized Boost Inductor
double Vin_rms = 220; //RMS value of input voltage
double Vin; //peak value of input voltage
double Iin; //transient input current
double Tin;
int allcase1 = 0;
int allcase2 = 0;
double mIdelta[half_cycle_click];
//loss of MOSFET, Boost diode, Return Diode, Boost Inductor, Output
    Capacitor, Current Transformer and Resistors
double Loss_mos=0, Loss_d=0, Loss_dl=0, Loss_l=0, Loss_co=0,
    Loss_tf=0;
double Pc; //core losses
double Pw; //winding losses
double Pwac; //AC winding losses
double Pwdc; //DC winding losses
double Pcon_mos; //conduction losses of MOSFET
double Psw_mos; //switching losses of MOSFET

void update_para()
{
    //Io = Po/Vo;
    //Ln = L*Io/Vo/Ts;

    allcase1 = 0;
    allcase2 = 0;

    Vin = Vin_rms*SQRT2;
    Iin = Po*SQRT2/Vin_rms/nstage; //RMS current of two MOS in 1 PFC
        cell
    Tin = Vo/Vin-4*Ln/pow(Vin/Vo, 3);
    if(Tin>1.0)
        allcase1 = 1;
    else if(Tin<0.0)
        allcase2 = 1;
    else
        Tin = asin(Tin)/PI*Ti;
}

double It_mos[half_cycle_click]; //RMS current of MOSFET in each
    switching cycle
double It_dav[half_cycle_click]; //average current of Boost Diode in
    each switching cycle
double It_l[half_cycle_click]; //transient current of Boost Inductor
double It_dlav[half_cycle_click]; //average current of Return Diode
    in each switching cycle

double Imos_std=0, Imos_nstd=0;
double Il_std=0, Il_nstd=0;
double Idlav=0;
double Idav=0;

```



```

//calculate transient state variables for all components of the
//circuit under DM mode
#define DMCALC \
{
    Idelta = Vit*Dmos1*Ts/(L*2);\
    It_mos[i] = Idelta*2*sqrt(Dmos1/3);\
    It_dav[i] = Idelta*Dd1;\
    It_l[i] = Idelta*2*sqrt((Dd1+Dmos1)/3);\
    It_dlav[i] = Idelta0*(Dd1+Dmos1);\
    DeltaBav += Vit*Dmos1*Ts*K_Bav/half_cycle_click;\
}\

//calculate transient state variables for all components of the
//circuit under CM mode
#define CMCALC \
{
    Idelta = Vit*Ton/(L*2);\
    It_mos[i] = sqrt((pow(Iit,2)+pow(Idelta,2)/12)*Dmos2);\
    It_dav[i] = Iit*Dd2;\
    It_l[i] = sqrt((pow(Iit,2)+pow(Idelta,2)/12));\
    It_dlav[i] = Iit*2;\
    DeltaBav += Vit*Dmos2*Ts*K_Bav/half_cycle_click;\
}\

double calc_loss()
{
    long i;
    double Vit,Iit,t, Idelta, DeltaBav=0;
    double Pcon,Psw, Ptot;
    double Dmos1,Dmos2;
    double Dd1,Dd2;

    update_para();
    vt.clear();
    vdelta_t.clear();
    vdeltaI.clear();
    vd.clear();
    for(i=0;i<half_cycle_click;i++)
    {
        t = i*Ts;
        Vit = gVin(t);
        Ton = gTon(Vit);
        Vit = gVin(t+Ton/2); //calculate the voltage in the middle
                             point
        Iit = gIin(t+Ton/2);
        Dmos1 = sqrt(2*(1-Vit/Vo)*(Iit/Io)*Ln/(Vit/Vo));
        Dmos2 = Ton/Ts;
        Dd1 = sqrt(2*Vit/Vo*Iit/Io*Ln/(1-Vit/Vo));
        Dd2 = 1-Dmos2;

        vt.push_back(t+Ton/2);
    }
}

```

```

    if (allcase1 > 0)
    {
        DM_CALC;
        vd.push_back(Dmos1);
    }
    else if (allcase2 > 0)
    {
        CM_CALC;
        vd.push_back(Dmos2);
    }
    else if (t <= Tin || t >= (Ti - Tin))
    {
        DM_CALC;
        vd.push_back(Dmos1);
    }
    else
    {
        CM_CALC;
        vd.push_back(Dmos2);
    }
    //Idelta is harmonic wave on single stage PFC
    vdelta.t.push_back(Idelta);
}

Imos_std = 0;
Imos_nstd = 0;
Il_std = 0;
Il_nstd = 0;
Idlav = 0;
Idav = 0;
for(i=0; i < half_cycle_click; i++)
{
    Imos_std += pow(It_mos[i]/Io, 2)/half_cycle_click;
    Imos_nstd += pow(It_mos[i], 2)/half_cycle_click;
    Il_std += pow(It_l[i]/Io, 2)/half_cycle_click;
    Il_nstd += pow(It_l[i], 2)/half_cycle_click;
    Idlav += It_dlav[i]/half_cycle_click;
    Idav += It_dav[i]/half_cycle_click;
}

//calculate normalized current for MOS
Imos_std = sqrt(Imos_std);
//calculate non-normalized current for MOS
Imos_nstd = sqrt(Imos_nstd);
//calculate normalized current for inductor
Il_std = sqrt(Il_std);
//calculate non-normalized current for inductor
Il_nstd = sqrt(Il_nstd);

//calculate the loss for MOS
Pcon = pow(Imos_nstd, 2)*RDS;
Pcon_mos = Pcon;
Psw = Vo*Imos_nstd*(T_ON+T_OFF)*sample_fre/2;
Loss_mos = (Pcon+Psw)*2;

```

```

//calculate the loss for Boost Diode D
Pcon = Idav*Vd;
Loss_d = Pcon*2;

//calculate the loss for return Diode DL
Pcon = Idlav*Vd_dl;
Loss_dl = Pcon;

//calculate inductor winding losses
Pwdc = pow(Il_nstd , 2)*K_rdc;
Pwac = pow(calc_rms_value(vdelta_t) , 2)*K_rdc*Fr;
Pw = Pwdc+Pwac;
//calculate core losses
Pc = K_loss*pow(sample_fre/1000.0 , K_a)*pow(DeltaBav*1.0e5 , K_b
);
//convert unit of losses from mW to W
Pc = Pc/1000;
//total inductor losses
Loss_l = (Pw+Pc);

//calculate losses of output capacitor Co
double Pco,Ico;
addsig(vdelta_t , vdeltaI , nstage);//synthesize ripple current
of each single stage
Ico = calc_rms_value(vdeltaI);//the rms high frequency current
of Co
Ico = sqrt(pow(Ico , 2)+pow(Po/(0.9*Vo*SQRT2) , 2));//total
current of Co
Pco = pow(Ico , 2)*RESR/4;//Losses in each Co
Loss_co = 2*Pco;//There are 2 Co at the output side

//calculate RTFSENSE&Rsense losses
double Ptfmos , Prsense;
Prsense = pow(Imos_rms/200 , 2)*RSENSE*nstage;
Loss_tf = Prsense;

Psemi = Loss_mos+Loss_d+Loss_dl;//semiconductor loss
Ptot = Loss_mos+Loss_d+Loss_dl+Loss_l*nstage+Loss_co+Loss_tf;//
system loss

return Ptot;
}

```


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