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*Published in:*
I E E E Transactions on Power Electronics

*Link to article, DOI:*
10.1109/TPEL.2011.2159515

*Publication date:*
2012

# Analysis and Design of a Bidirectional Isolated DC-DC Converter for Fuel Cells and Super-Capacitors Hybrid System

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***Abstract*— Electrical power system in future uninterruptible power supply (UPS) or electrical vehicle (EV) may employ hybrid energy sources, such as fuel cells and super-capacitors. It will be necessary to efficiently draw the energy from these two sources as well as recharge the energy storage elements by the DC bus. In this paper, a bidirectional isolated DC-DC converter controlled by phase-shift and duty cycle for the fuel cell hybrid energy system is analyzed and designed. The proposed topology minimizes the number of switches and their associated gate driver components by using two high frequency transformers which combine a half-bridge circuit and a full-bridge circuit together on the primary side. The voltage doubler circuit is employed on the secondary side. The current-fed input can limit the input current ripple that is favorable for fuel cells. The parasitic capacitance of the switches is used for zero voltage switching (ZVS). Moreover, a phase-shift and duty cycle modulation method is utilized to control the bidirectional power flow flexibly and it also makes the converter operate under a quasi-optimal condition over a wide input voltage range. This paper describes the operation principle of the proposed converter, the ZVS conditions and the quasi-optimal design in depth. The design guidelines and considerations about the transformers and other key components are given. Finally, a 1-kW 30~50-V-input 400-V-output laboratory prototype operating at 100 kHz switching frequency is built and tested to verify the effectiveness of the presented converter.**

***Index Terms*—Bidirectional dc-dc converter, current-fed, fuel cell, phase-shit, super-capacitor**

## I. Introduction

THE HYBRID system based on fuel cells (FCs) and super-capacitors (SCs) as an environmentally renewable energy system has been applied in many fields, such as hybrid electric vehicle (HEV), uninterruptible power supply (UPS) and so on [1]-[4]. As an example, a block diagram of extended-run time battery-less double-conversion UPS system powered by FCs and SCs is illustrated in Fig. 1. Comparing to diesel generators and batteries, fuel cells are electrochemical devices which convert the chemical potential of the hydrogen into electric power directly with consequent high conversion efficiency, so it has the possibility to obtain the extended runtime range with the combustible feed from the outside. But one of the main weak points of the fuel cell is its slow dynamics because of the limited speed of hydrogen delivery system and the chemical reaction in the membranes with a slow time constant [5]. Hence, during the warming-up stage or load transient, super-capacitors [6], [7] are utilized as the auxiliary power source for smoothing the output power. In addition, the fuel cell output voltage is varied widely, almost 2:1, depending on the load condition, and the terminal voltage of the super-capacitor bank is also variable during charging and discharging periods. Thus, it is very important for the conversion system to be capable of harvesting power from theses two different power sources efficiently in widely input voltage range and load conditions.

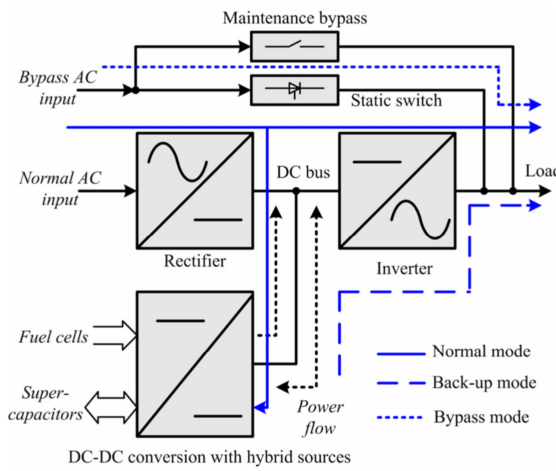

Fig. 1. Block diagram of a dual-conversion UPS system based on fuel cell and super-capacitor.

In recent years, many configurations of a hybrid DC power conversion system relating to FCs and SCs have been proposed. Connecting FCs and SCs by two individual DC/DC converters separately to a mutual DC voltage bus is the most typical configuration [8], [9], which offers many advantages, especially, the faster and more stable system response. However, it increases the system cost and power losses. A multiple DC voltage bus, which connects FCs and SCs to different cascade voltage buses through converters, is also a

Manuscript received December 9, 2011; revised February 13, 2011 and April 13, 2011; accepted May 29, 2011.
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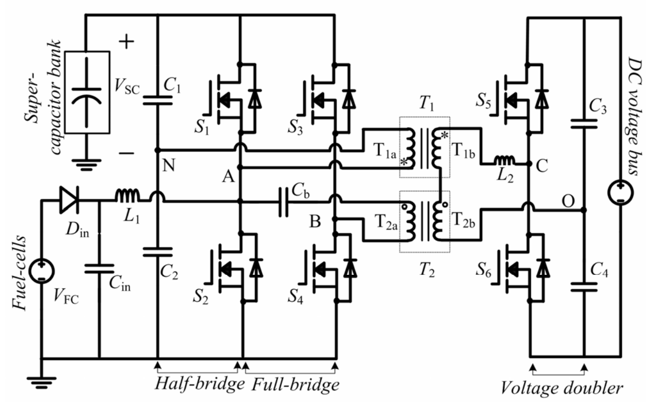



Fig. 2. The proposed hybrid bidirectional DC-DC converter topology.

widely used configuration [10], [11], but the disadvantages are the high power losses and the low reliability. Moreover FCs and the SCs cannot keep the bus voltage constant except if they are oversized. A simplest configuration is to parallel FCs and SCs directly as one power source but their output currents can not be controlled independently. In addition, a multi-port configuration was introduced [12], [13]. For the applications where the galvanic isolation is required, an isolated multi-port converter family was investigated in [14]. Based on the traditional half-bridge topology, a novel four-port converter with bidirectional ability was presented in [15] and [16]. A multi-port current-fed DC/DC converter based on the flux additivity was proposed in [17]. The boost type input port can limit the current ripple and this characteristic is helpful to increase the lifetime of fuel cells, but the diode connected in series with each MOSFETs makes reversible power flow impossible. To overcome this drawback, two current–fed dual input bidirectional converters were proposed and investigated in [18] and [19]. The solutions based on the dual-active-bridge (DAB) converter using magnetic coupling transformer were presented in [20]-[23], where the bidirectional power can be regulated by phase-shift control scheme. Converters using resonant tank or interleaved transformer windings were reported in [24] and [25], respectively. However, the control strategy for the multi-port type is not easy to implement [25].

Based on the boost-half-bridge (BHB) circuit [26], [27] and the hybrid full-bridge structure [28], a novel hybrid bidirectional DC-DC converter was derived and presented in [29]. In this paper, characteristics of the proposed converter in [29] will be analyzed in depth. As shown in Fig. 2, a fuel cell bank as the main input power source is connected to the BHB circuit which can limit the input current ripple; a super-capacitor bank as the auxiliary power source can deliver power to the load through the full-bridge circuit. The proposed converter can draw power from these two different DC sources individually and simultaneously. Moreover, using the phase-shift plus duty cycle control scheme [30], the bidirectional power flow can be regulated flexibly and the AC current root mean square (RMS) value can be reduced over a wide input voltage range. This paper is organized as follows: Section I introduces the research background and the contribution of this work; Section II gives the operation principles and the theoretical calculations; Section III presents the quasi-optimal design method. To verify the validity of the theoretical analysis and the design approach, experimental results from the laboratory prototype are presented in Section V. Finally, the conclusion is given in Section VI.

## II. Operation Principles of the Hybrid DC Converter

As shown in Fig. 2, a BHB structure locates on the primary side of the transformer $T_1$ and it associates with the switches $S_1$ and $S_2$ operating at 50% duty cycle. The super-capacitor bank is connected to the variable low voltage (LV) DC bus across the dividing capacitors, $C_1$ and $C_2$. Bidirectional operation can be realized between the super-capacitor bank and the high voltage (HV) DC bus. Switches $S_3$ and $S_4$ are controlled by the duty cycle to reduce the current stress and AC RMS value when input voltage $V_{FC}$ or $V_{SC}$ are variable over a wide range. The transformers $T_1$ and $T_2$ with independent primary windings as well as series-connected secondary windings are employed to realize galvanic isolation and boost a low input voltage to the high voltage DC bus. A DC blocking capacitor $C_b$ is added in series with the primary winding of $T_2$ to avoid transformer saturation caused by asymmetrical operation in full-bridge circuit. The voltage doubler circuit utilized on the secondary side is to increase voltage conversion ratio further. The inductor $L_2$ on the secondary side is utilized as a power delivering interface element between the LV side and the HV side. According to the direction of power flow, the proposed converter has three operation modes which can be defined as: boost mode, super-capacitor power mode and super-capacitor recharge mode. In the boost mode, the power is delivered from the fuel cells and super-capacitors to the DC voltage bus. In the super-capacitor power mode, only the super-capacitors are connected to provide the required load power. When the DC bus charges the super-capacitors, the power flow direction is reversed which means the energy is transferred from the HV side to the LV side, and thereby the converter is operated under the super-capacitor recharge mode.

### A. Boost Mode

In the boost mode, the timing diagram and typical waveforms are shown in Fig. 3, where $n_1$ and $n_2$ are the turn ratios of the transformers. The current flowing in each power switch on the primary side is presented, but the voltage and current resonant slopes during the switching transitions are not shown here for simplicity. To analyze the operation principles clearly, the following assumptions are given: (1) All the switches are ideal with anti-parallel body diodes and parasitic capacitors; (2) The inductance $L_1$ is large enough to be treated as a current source; (3) The output voltage is controlled well as a constant; (4) The leakage inductance of the transformers, parasitic inductance and extra inductance can be lumped together as $L_2$ on the secondary side.

The half switching cycle can be divided into eight intervals and the corresponding equivalent circuits are shown in Fig. 4.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication.

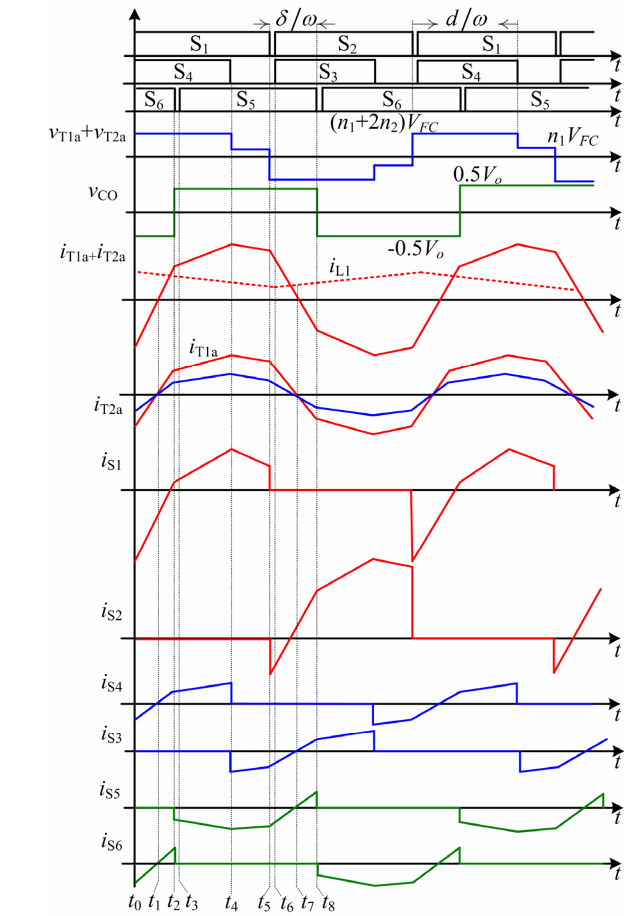
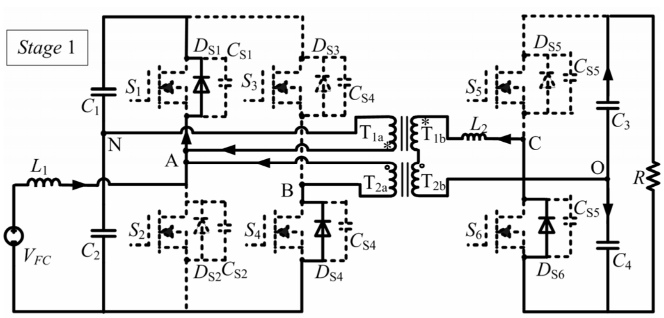
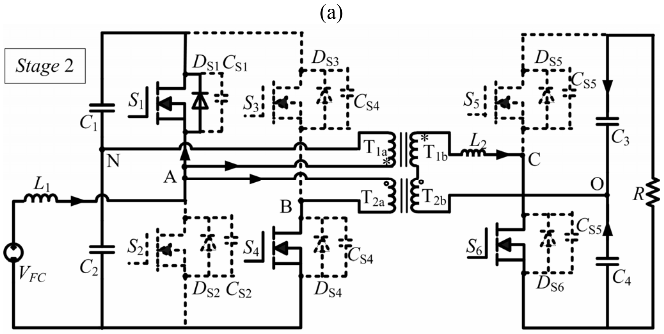




Fig. 3. Timing diagram and typical waveforms in the boost mode.

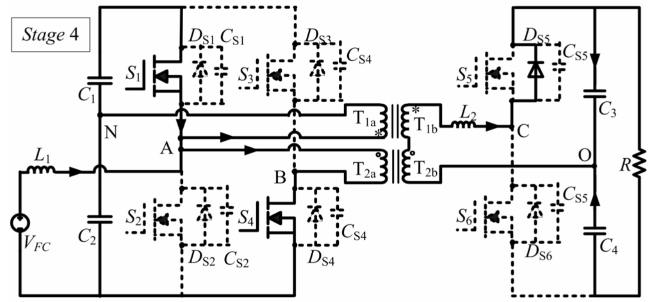



(a)

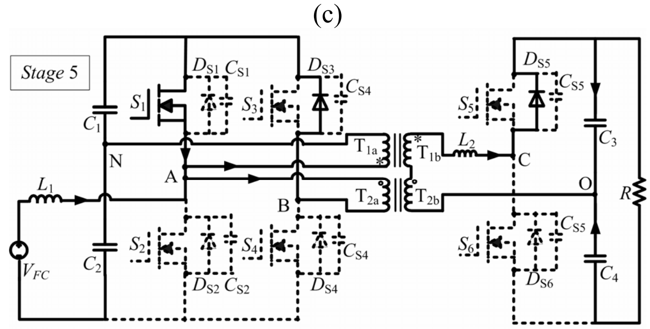



(b)

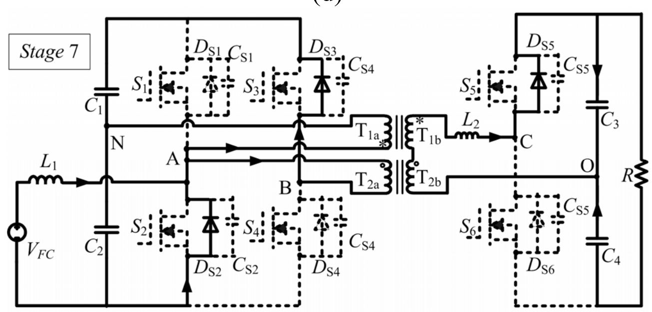
1) *Stage* 1 ($t_0$-$t_1$): It can be seen that, at any time, the voltage across $L_2$ is always $V_{T1b}$+$V_{T2b}$-$V_{CO}$, but $V_{T1b}$, $V_{T2b}$ and $V_{CO}$ have different values in different operating intervals. In ($t_0$-$t_1$), $S_1$, $S_4$ and $S_6$ are gated, so $V_{T1b}$=$n_1V_{FC}$, $V_{T2b}$=$2n_2V_{FC}$ and $V_{CO}$=-$V_o$/2, and thereby $i_{L2}$ will increase linearly. Because $i_{T1a}$+$i_{T2a}$



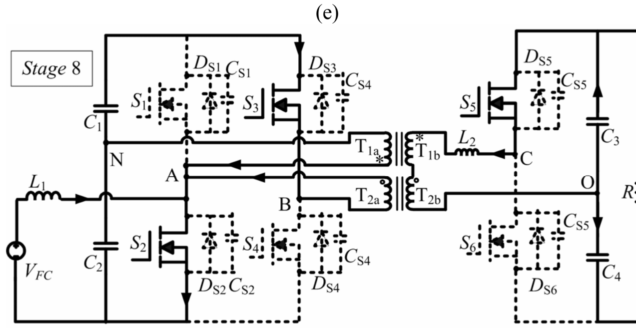

(c)




(d)




(e)




(f)

Fig. 4. Equivalent circuits in each operating stage: (a) stage 1, (b) stage 2, (c) stage 4, (d) stage 5, (e) stage 7, and (f) stage 8.

are negative and $I_{L1}$ is positive, the current flows through $D_{S1}$, the body-diode of switch $S_1$. The current paths during this interval are shown in Fig. 4 (a);

2) *Stage* 2 ($t_1$-$t_2$): From $t_1$, the value of $i_{T1a}$+$i_{T2a}$ starts to be positive, and thus $S_4$ conducts to carry the current, but $S_1$ may conduct until the value of $I_{L1}$ is smaller than that of $i_{T1a}$+$i_{T2a}$. The equivalent circuit is shown in Fig. 4 (b);

3) *Stage* 3 ($t_2$-$t_3$): At $t_2$, $S_6$ is turned off. The inductor $L_2$ begins to resonate with the stray capacitors $C_{S5}$ and $C_{S6}$. When the voltage across $C_{S5}$ reduces to zero, the body-diode of $S_5$ starts to conduct, so the voltage $V_{CO}$ equals $V_o$/2;

4) *Stage* 4 ($t_3$-$t_4$): At $t_3$, $S_5$ is turned on under ZVS. The current paths are illustrated in Fig. 4 (c);

5) *Stage* 5 ($t_4$-$t_5$): At $t_4$, $S_4$ is turned off. The inductor $L_2$ begins to resonate with the stray capacitors $C_{S3}$ and $C_{S4}$. When the voltage across $S_3$ reduces to zero, $D_{S3}$ is therefore forward biased. The voltage across the primary winding of $T_2$ is clamped to zero, i.e. $V_{T2b}$=0. Hence, $V_{L2}$ equals $V_{T1b}$-$V_{CO}$ and the current paths are shown in Fig. 4 (d);

6) *Stage* 6 ($t_5$-$t_6$): At $t_5$, $S_1$ is turned off. The inductor $L_2$ begins to resonate with the stray capacitors of the switches, $C_{S1}$ and $C_{S2}$. $C_{S1}$ is charged from approximately 0 V, while $C_{S2}$ is discharged from $2V_{FC}$. The rate of change on voltage depends on the magnitude $i_{T1a}$+$i_{T2a}$-$I_{L1}$. At $t_5$, $V_{CS2}$ attempts to overshoot the negative rail and then $D_{S2}$ is forward biased. After that, $S_2$ can be turned on under ZVS.

7) *Stage* 7 ($t_6$-$t_7$): During this interval, $V_{T1b}$=-$n_1V_{FC}$, $V_{T2b}$=-$2n_2V_{FC}$ and $V_{CO}$=$V_o$/2, so the primary current decays. Until $I_{L1}$ is bigger than $i_{T1a}$+$i_{T2a}$, the current starts to flow through the switch $S_2$, and thus the equivalent circuit is shown in Fig. 4 (e).

8) *Stage* 8 ($t_7$-$t_8$): From $t_7$, both $i_{T1a}$ and $i_{T2a}$ are to be negative, which makes $S_3$ and $S_5$ conduct. The equivalent circuit is shown in Fig. 4 (f). After $t_8$, the second half cycle starts.

The power delivered by this converter can be calculated, referring to the typical waveforms shown in Appendix, as follows:

$$P_o = \begin{cases} \dfrac{V_L V_H\left(2\pi\delta - 4\delta^2 + 2\delta d + \pi d - d^2\right)}{2\pi\omega L_2} & (0 \le |\delta| \le d) \\ \dfrac{V_L V_H\left(2\pi\delta - 2\delta^2 - 2|\delta| d + \pi d + d^2\right)}{2\pi\omega L_2} & (d \le |\delta| \le 0.5\pi) \end{cases} \quad (1)$$

where $\delta$ is the phase-shift angle; $\omega$ is the switching angular frequency; $V_L$=$n_1V_{FC}$ and $V_H$=$V_O$/2, respectively; the duty cycle $d$ is defined as:

$$d = 2\pi \cdot \frac{T_{on\,S3}}{T_s} = 2\pi \cdot \frac{T_{on\,S4}}{T_s} \quad (2)$$

When $d$=$\pi$, $v_{T1b}$+$v_{T2b}$ will be the waveform with only two voltage levels, and then (1) will be

$$P_o = \frac{2 \cdot V_L V_H}{\pi\omega L_2} \cdot \delta(\pi - \delta) \quad (3)$$

When $\delta$=0, the output power is calculated by

$$P_o = \frac{V_L V_H}{2\pi\omega L_2} \cdot d(\pi - d) \quad (4)$$

In order to limit the reactive power in the converter, the phase-shift angle normally is smaller than $\pi$/4; hence the first sub-equation in (1) is more practical to analyze the average power. Based on that, the output power, which is respect to the base $V_LV_H/2\pi\omega L_2$, is plotted in Fig. 5. It can be seen that when the duty cycle control is utilized together with the phase-shift control, at same input and output voltages, the average power delivered is increased, because the duty cycle

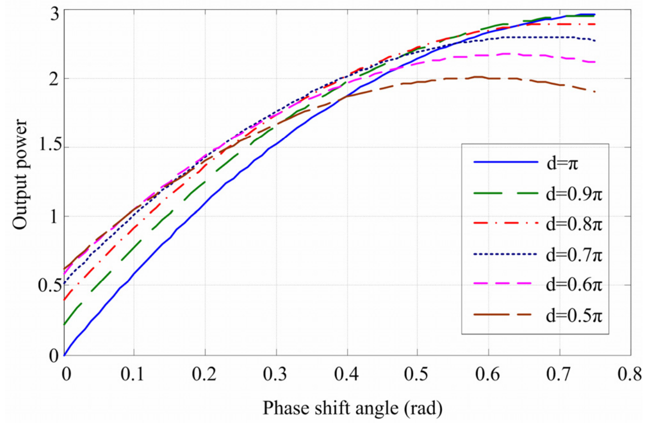


Fig. 5. The relationship between the output power (p.u.) and phase-shift angle/duty cycle.

control can limit the required reactive power. But with the duty cycle reducing, the output power increasing is not significant. When the phase-shift angle is larger than 0.6, the delivered average power is decreased, because in fact the duty cycle control reduces the average voltage across the secondary windings.

A close study reveals that because of the BHB configuration the average current stress of $S_2$ is much higher than that of $S_1$, whereas the current stresses of $S_3$ and $S_4$ are kept same. Referring to the definition in Fig. 3, the ON-time conducting current of each main device is given by

$$\begin{aligned} i_{S1\_ON}(t) &= i_{T1a}(t) + i_{T2a}(t) - i_{L1}(t) \\ i_{S2\_ON}(t) &= i_{L1}(t) - i_{T1a}(t) - i_{T2a}(t) \\ i_{S3\_ON}(t) &= i_{T2a}(t) \\ i_{S4\_ON}(t) &= -i_{T2a}(t) \end{aligned} \quad (5)$$

From (5), obviously, $S_2$ carries more current than $S_1$, so that devices with different current ratings can be chosen for $S_1$ and $S_2$. The peak current values of the primary side switches are

$$\begin{cases} I_{S1,peak} = \dfrac{P_o}{\eta V_{FC}} + (n_1 + n_2) \cdot I_{peak} \\ I_{S2,peak} = \dfrac{P_o}{\eta V_{FC}} + (n_1 + n_2) \cdot I_{peak} \\ I_{S3,peak} = I_{S4,peak} = n_2 \cdot I_{peak} \end{cases} \quad (6)$$

where $\eta$ is the efficiency of the converter and $I_{peak}$=max($I_1$, $I_2$, $I_3$), and $I_1$, $I_2$ and $I_3$ are calculated:

$$\begin{cases} I_1 = i_{L2}(t_2) = \dfrac{\pi V_H + (4\delta - d - \pi)V_L}{2\omega L_2} \\ I_2 = i_{L2}(t_4) = \dfrac{(\pi + 2\delta - 2d)V_H + (3d - \pi)V_L}{2\omega L_2} \\ I_3 = i_{L2}(t_5) = \dfrac{(2\delta - \pi)V_H + (\pi + d)V_L}{2\omega L_2} \end{cases} \quad (7)$$

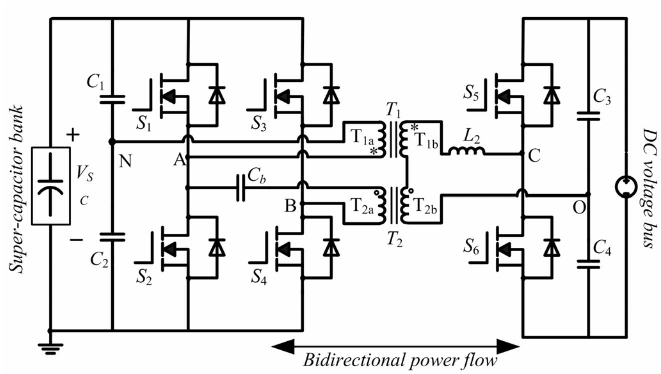



Fig. 6. The proposed converter in the super-capacitor power mode and the super-capacitor recharge mode.

The ZVS condition can be deduced on the precondition that the anti-parallel diode of switch must conduct before the switch is triggered. Then, the soft-switching conditions for switches $S_1$ and $S_2$, switches $S_3$ and $S_4$, and switches $S_5$ and $S_6$ are related to the magnitude of $i_{T1a}+ i_{T2a}-i_{L1}$, $i_{T2a}$ and $i_{L2}$, respectively, i.e. the main devices are turned off with a positive current flowing and then the current diverts to the opposite diode which allows the in-coming MOSFET to be switched on under zero voltage. Thus, in order to achieve zero-voltage-switching (ZVS) turn-on, the currents must obey:

$$\begin{cases} i_{T1a}(t_0)+i_{T2a}(t_0)-I_{L1}<0; & (for\ S_1) \\ i_{T2a}(t_0)<0; & (for\ S_4) \\ i_{L2}(t_2)>0; & (for\ S_5) \\ i_{T1a}(t_5)+i_{T2a}(t_5)-I_{L1}>0; & (for\ S_2) \\ i_{T2a}(t_5)>0; & (for\ S_3) \\ i_{L2}(t_8)<0; & (for\ S_6) \end{cases} \quad (8)$$

Hence, substituting (7) into (8), ZVS constraints with respect to circuit parameters and control variables are deduced as

$$\begin{cases} V_o > \dfrac{2n_1(n_1+n_2)(\pi+d)V_{FC}+4I_{L1}L_2\omega}{(\pi-2\delta)(n_1+n_2)} & (for\ S_1) \\ V_o < \dfrac{2n_1(n_1+n_2)(\pi+d)V_{FC}-4I_{L1}L_2\omega}{(\pi-2\delta)(n_1+n_2)} & (for\ S_2) \\ \dfrac{V_o}{V_{FC}} < 2n_1\left(\dfrac{\pi+d}{\pi-2\delta}\right) & (for\ S_3, S_4) \\ \dfrac{V_o}{V_{FC}} > 2n_1\left(\dfrac{\pi+d-4\delta}{\pi}\right) & (for\ S_5, S_6) \end{cases} \quad (9)$$

### B. Super-capacitor Power Mode

For a short period of utility power failure in UPS system which can be handled by super-capacitors or during the fuel cell warming-up stage, the converter will be operated under the super-capacitor power mode and the power flows from the super-capacitor bank to the DC voltage bus as shown in Fig. 6. The timing diagram and typical waveforms in this mode are illustrated in Fig. 7. It can be seen that the typical waveforms are similar with those in the boost mode, but because there is no $i_{L1}$, the current stresses of $S_1$ and $S_2$ are completely same. The peak current can be expressed by

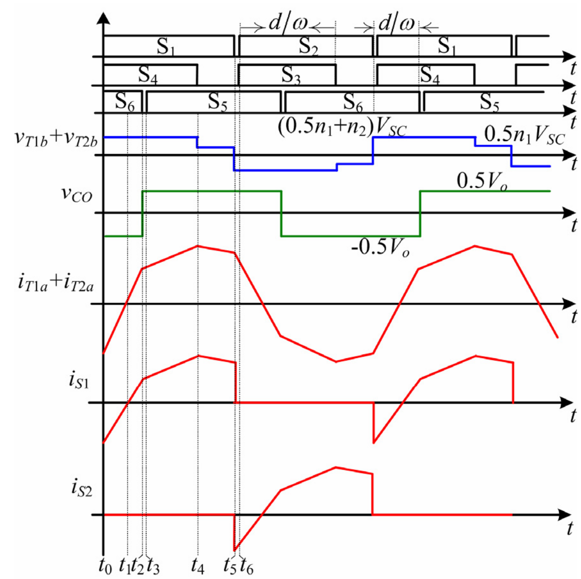



Fig. 7. Timing diagram and typical waveforms under the super-capacitor power mode.

$$I_{S1,peak}=I_{S2,peak}=(n_1+n_2)\cdot I_2 \quad (10)$$

With the same method used in the boost mode, to achieve ZVS turn-on, the currents must obey:

$$\begin{cases} i_{T1a}(t_0)+i_{T2a}(t_0)<0; & (for\ S_1) \\ i_{T2a}(t_0)<0; & (for\ S_4) \\ i_{L2}(t_2)>0; & (for\ S_5) \\ i_{T1a}(t_5)+i_{T2a}(t_5)>0; & (for\ S_2) \\ i_{T2a}(t_5)>0; & (for\ S_3) \\ i_{L2}(t_8)<0; & (for\ S_6) \end{cases} \quad (11)$$

Comparing to (8), the ZVS constraints for $S_1$ and $S_2$ are different in this mode and thereby the ZVS condition can be expressed as

$$\begin{cases} \dfrac{V_o}{V_{FC}} < 2n_1\left(\dfrac{\pi+d}{\pi-2\delta}\right) & (for\ S_1 \sim S_4) \\ \dfrac{V_o}{V_{FC}} > 2n_1\left(\dfrac{\pi+d-4\delta}{\pi}\right) & (for\ S_5, S_6) \end{cases} \quad (12)$$

### C. Super-capacitor Recharge Mode

As shown in Fig. 6, in the super-capacitor recharge mode, the super-capacitor will be charged by the high voltage DC bus which means that the power flows from the HV side to the LV side. The timing diagram and typical waveforms are

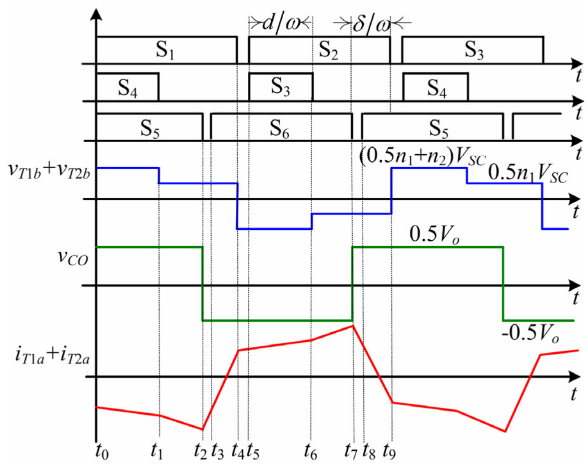



Fig. 8. Timing diagram and typical waveforms under the super-capacitor recharge mode.

illustrated in Fig. 8, where the gate drive signal of $S_5$ is leading to that of $S_1$ due to the reversed power-flow direction.

## III. Quasi-Optimal Design Method

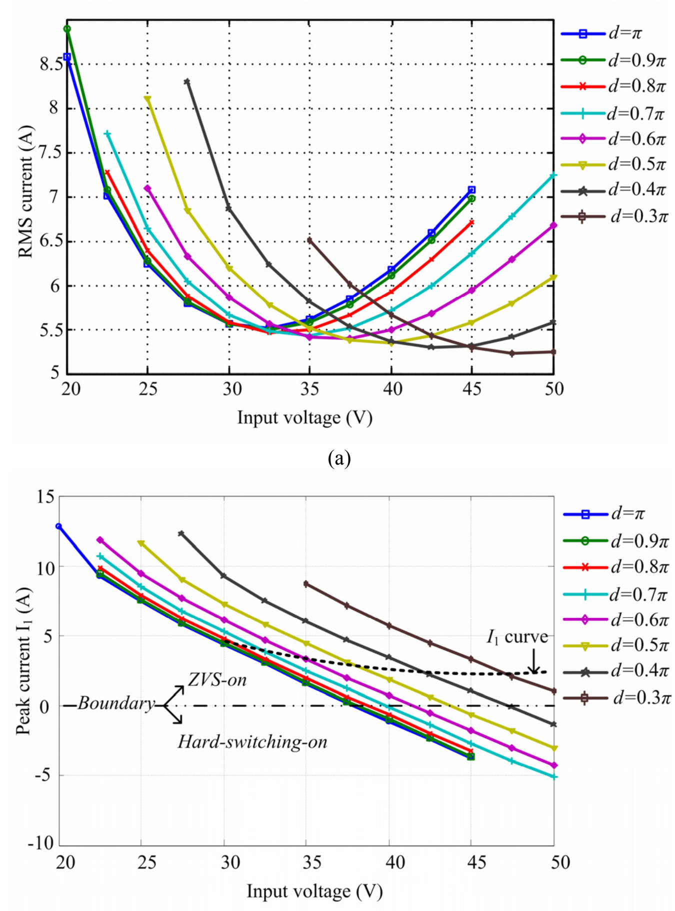
To increase the conversion efficiency, generally based on the precise mathematic model of the power loss of each component and the converter switching times, the phase-shift angle and the duty cycle can be calculated to control the converter and make the total power losses minimal [31]. But this method has two critical limitations in practice: 1) performance will suffer when the loss models employed in the circuit and the switching times are not available or not precise; 2) the controller with the needed phase-shift angle and duty cycle depending on the variable input voltage and output power is complex to design. Hence, a quasi-optimal design is proposed here which includes two design criteria as

- Minimize the RMS value of $i_{L2}$ by the phase-shift and duty cycle control to reduce the conduction losses;
- Keep the ZVS operation for high voltage side switches to reduce the switching losses.

The RMS current flowing through the secondary inductor is calculated by:

$$I_{L2,RMS} = \frac{\sqrt{3}}{3}\cdot\sqrt{\frac{(\pi-\delta)I_2^2+\left[(\pi-d)I_3+(d-\delta)I_1\right]I_2+(\pi+\delta-d)I_3^2-I_1I_3\delta+I_1^2 d}{\pi}} \tag{13}$$

From (13), the secondary side RMS current is plotted in Fig. 9 (a) according to phase-shift angles and duty cycles under the condition where the output power is 1 $k$W; the output voltage is 400 V; the interface inductance is 40 $u$H and the switching frequency is 100 $k$Hz. When the input voltage or the duty cycle varies, the phase-shift angle may be recalculated by (1) to get the required output power or DC bus voltage. It can be seen that based on the input voltage and the phase-shift angle from (1), adjusting the duty cycle value can reduce the current RMS value effectively. Furthermore, using duty cycle control can extend the soft-switching range for the high voltage side switches, $S_5$ and $S_6$, as shown in Fig. 9 (b).




(a)

(b)

Fig. 9. Typical current values with phase-shift plus duty-cycle control under the boost mode: (a) secondary RMS current values, and (b) peak current values of $i_{L2}$ at time $t_2$.

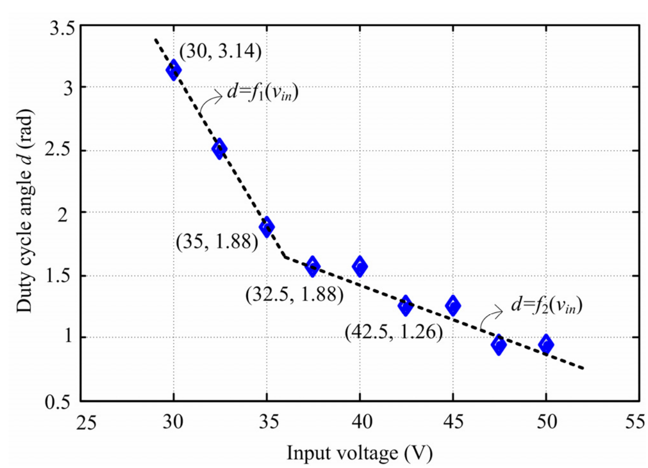



Fig. 10. Relationship between the duty cycle and variable input voltage.

The $I_1$ curve (dashed line) is the approximate track which is followed by current $I_1$ and there is a margin between the $I_1$ curve and boundary curve, which is related to the energy stored in the $L_2$ for achieving completely resonance during the dead-time of switch commutation. From Fig. 9 (a), an approximate relationship between input voltage and duty cycle can be derived as illustrated in Fig. 10, where the piecewise curve consisting of $f_1(v_{in})$ and $f_2$ $(v_{in})$ is plotted. Based on the values indicated, $d_1=f_1(v_{in})=10.676-0.251v_{in}$ ($30 \le v_{in}<35.8$) and $d_2=f_2(v_{in})=3.925-0.063v_{in}$ ($35.8 \le v_{in} \le 50$) are obtained. In practice in order to monitor the output state of fuel cell for the over-voltage protection purpose, normally, the input voltage sensing is necessary, so that the duty cycle can be decided by $f_1(v_{in})$ or $f_2(v_{in})$ without adding system complexity and it is easy to be completed by both analog and digital circuits. As stated in Section II, the average output power can be controlled by two independent control variables: $\delta$ and $d$. The analysis conducted here revealed that there is a value $d_{optimal}$ that can minimize the AC RMS current and extend the ZVS range to achieve quasi-optimal operation. Hence, variable $\delta$ is used to control the required power that transferred by the converter and variable $d$ is chosen to increase the efficiency. The algorithm to decide $\delta$ and $d$ is implemented by the following steps:

1) Find the value $d_{optimal}$ that minimizes RMS current by equating the first derivative of (13) to zero with respect to $d$ for the input voltage $V_{FC}$ or $V_{SC}$, the output voltage $V_o$ and the required output power $P_o$.

2) Determine $\delta$, using (1). If $\delta<0$ or can not find real root, set $\delta=0$, and recalculate $d$ by (4).

3) Test the value of $I_1$. If $I_1<0$, reduce $d$ and then go back to step 2 to recalculate $\delta$.

4) Using calculated $\delta$ and $d$, generate the driving signals for the power switches.

5) If one of the values of $V_{FC}$, $V_{SC}$, $V_o$ or $P_o$ changes, then go back to step 1.

In this paper, according to the variable input voltage and the required output power, the quasi-optimal designed $\delta$ and $d$ can be calculated off-line. During the hardware test, the on-line look-up table is used in the digital signal processor to control the converter effectively.

## IV. Hardware Design and Test

The converter works with a variable input voltage 30~50 V and a constant output voltage 400 V. The duty cycles of $S_1$ and $S_2$ are kept at 50%, so the voltage across $C_1$ and $C_2$ is double of the input voltage $V_{FC}$. The bidirectional power flow can be controlled by the phase-shift angle $\delta$ which is between $S_1$ and $S_5$, and the duty cycle of $S_3$ and $S_4$. It is worth noting that although the amplitude of the voltage on $T_1$ is half of that on $T_2$ due to $T_1$ associates with half-bridge structure, the same power can be delivered by each transformer since the turns ratios of $T_1$ and $T_2$ have been chosen with the relationship: $n_1=2n_2$, in this paper.

*Transformer Design*

For the low input voltage converter, the conduction losses are dominating in the total power losses. Hence, it is important to reduce the transformer winding losses. Winding losses in transformers increase dramatically with the high switching frequency due to eddy and proximity current effects [32].

Based on Dowell's assumptions and the general field solutions for the distribution of current density in a single

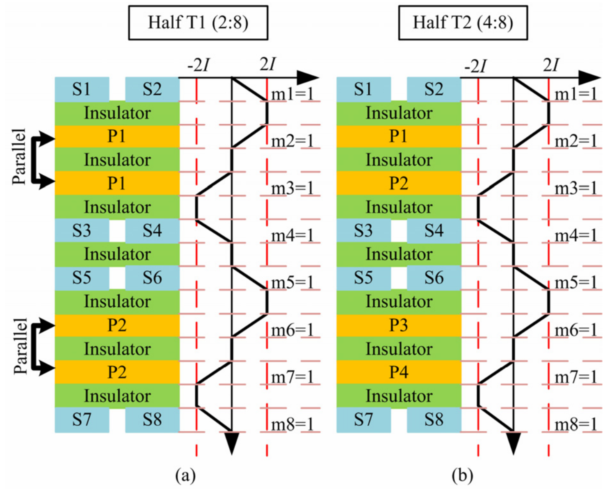



Fig. 11. Winding arrangements: (a) winding arrangement and MMF distribution for half $T_1$, and (b) winding arrangement and MMF distribution for half $T_2$.

layer of an infinitely foil conductor, the expression for AC resistance of the $m^{th}$ layer was derived in [32] and [33] as:

$$\frac{R_{ac,m}}{R_{dc,m}} = \frac{\xi}{2}\left[\frac{\sinh\xi+\sin\xi}{\cosh\xi-\cos\xi} + (2m-1)^2\cdot\frac{\sinh\xi-\sin\xi}{\cosh\xi+\cos\xi}\right] \tag{14}$$

where $m$ is defined as a ratio:

$$m = \frac{F(h)}{F(h)-F(0)} \tag{15}$$

where $F(0)$ and $F(h)$ are magnetomotive forces (MMF) at the limits of a layer, shown in Fig. 11 where $P_m$ ($m$=1~4) and $S_n$ ($n$=1~8) indicate the primary and secondary windings, respectively.

The first term in (14) is to describe the skin effect and the second term represents the proximity effect factor. The proximity effect loss in a multilayer winding may strongly dominate over the skin effect loss depending on the value of $m$ which is related to the winding arrangement. Interleaving transformer windings can reduce the proximity loss significantly when the primary and secondary currents are in phase. When the numbers of primary turns for $T_1$ and $T_2$ are 4 and 8 respectively, Fig. 11 shows the winding arrangements and MMF distributions along the vertical direction for both half of $T_1$ and $T_2$. The value of $m$ in each layer equals 1 according to (15) which contributes to lower AC resistances. Not only AC resistances can be reduced, but also leakage inductances can be significantly decreased by interleaving windings [33]. It is noted that because of fewer intersections between the primary and the secondary, inter-winding capacitance in this interleaving structure is smaller than the fully interleaving without sacrificing any other behaviors, neither leakage inductance nor AC resistance, thereby contributing to relative lower electromagnetic interference (EMI) noises.

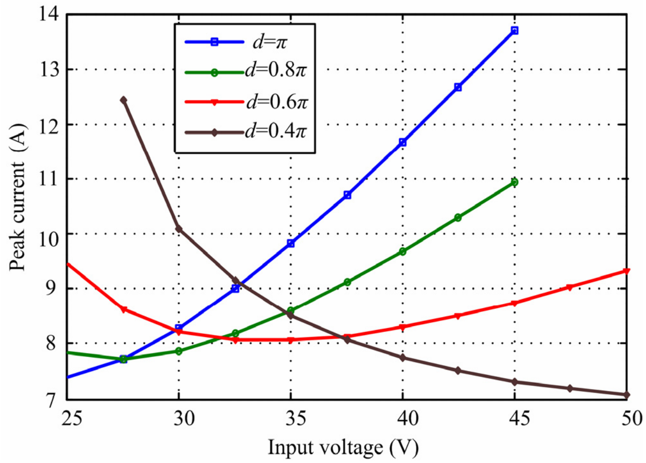


Fig. 12. Peak current of the secondary side under different input voltages.

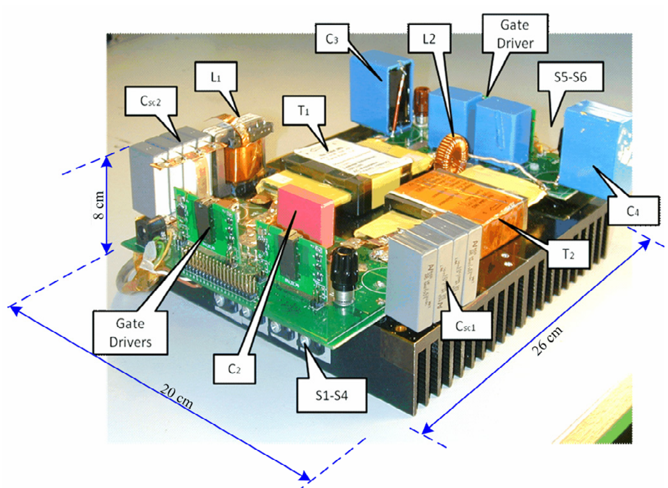


Fig. 13. The prototype of the proposed converter.

*Input Inductor*

The BHB structure with the storage inductor, $L_1$, in series with fuel cells, inherently can reduce the input current ripple. Compared to buck-derived topologies having large discontinuous input currents, the proposed converter with boost-type input port requires only very small additional input capacitance, $C_{in}$, as input filter. According to the required ripple current $\Delta I_{L1}$ of input current $I_{L1}$, the input inductance can be calculated by:

$$L_1 = \frac{V_{FC} \cdot \Delta t}{\Delta I_{L1}} = \frac{\pi V_{FC}}{\omega \cdot \Delta I_{L1}} \qquad (16)$$

where $\Delta t$ is the ON-time of switch $S_2$ during each switching cycle.

Moreover, all the individual magnetic components, two transformers and one inductor, can be integrated into one planar E-I-E core to increases the power density further [34].

*Power Switches*

Based on the analyzed results in Section II, it can be concluded that at the full load, the peak current is $I_2$ on the secondary side. The different values of $I_2$ under the phase-shift and duty cycle control can be plotted in Fig. 12 and thus using duty-cycle control one can avoid over-sized power devices. On the low voltage side, the peak current flowing through the switches can be calculated by (6) and the peak voltage across the switches on the primary side is

$$V_{peak} = 2V_{FC} \qquad (17)$$

On the high voltage side, the peak voltage for all the switches equals the output voltage, and the peak current of the voltage doubler is four times smaller than that of $S_3$ or $S_4$ on the low voltage side.

TABLE I
PARAMETERS AND COMPONENTS

| | |
|---|---|
| Input voltage $V_{FC}$, $V_{SC}$ | 30-50 VDC, 50-100VDC |
| Output voltage | 400 VDC |
| Output power | 1 *k*W |
| Switches $S_1$~$S_4$ | IRFP4568PBF (150 V/154 A) |
| Switches $S_5$, $S_6$ | SIHG20N50C (500V/20A) |
| Transformer core | Ferrite N87, EI 64 |
| Transformer turns, $T_1$<br>$T_2$ | 4:16<br>8:16 |
| Input inductor $L_1$ | 20 $\mu$H Kool M$\mu$ |
| Auxiliary inductor $L_2$ | 40 $\mu$H, Ferrite core |
| Capacitors $C_1$ and $C_2$ | 22 $\mu$F/63 V, 4 paralleled |
| Output capacitors $C_3$ and $C_4$ | 15 $\mu$F+8.6 $\mu$F each |
| DC blocking capacitor $C_b$ | 10 $\mu$F |
| Switching frequency | 100 *k*Hz |

The key parameters and components of the designed prototype are listed in Table I and photograph of the laboratory prototype is shown in Fig. 13.

In the test, a low voltage and high current DC power supply (EA-PS 9060-48: 0~60 V/0~48 A) as the primary input power source is used to simulate the fuel cell. 24 super-capacitors (BCAP0350, 2.5 V/350 F) in series connection are taken as the power storage unit connected on the low voltage DC bus.

Fig.14 ~ Fig.16 show the measured waveforms from the prototype working under the phase-shift plus duty cycle modulation in the condition where $V_{FC}$=30 V and input power is 750W. It can be seen that the measured results match well with the theoretical analysis shown in Fig. 3. When $d$=$\pi$, Fig.14 represents the waveforms of the voltages on the secondary side (Ch1: $v_{T1b}+v_{T2b}$ and Ch2: $v_{CO}$) and the currents flowing in $L_2$ and $L_1$ (Ch3: $i_{L2}$ and Ch2: $i_{L1}$) respectively. Since $v_{T1b}+v_{T2b} \approx v_{CO}$, the waveform of $i_{L2}$ is flat, which agrees with the calculated results in (7). Fig.15 shows the measured waveforms when $d$=0.65$\pi$. Comparing to Fig. 14, $v_{T1b}+v_{T2b}$ has multiple voltage levels because of the duty cycle control, while the waveform of $i_{L1}$ is same. Fig.16 shows the plots of the primary voltages (Ch1: $v_{AN}$ and Ch2: $v_{AB}$) and currents (Ch3: $i_{T1a}$ and Ch4: $i_{T2a}$) of $T_1$ and $T_2$, when $d$=0.65 $\pi$. It is clear that the $v_{AB}$ has a three-level voltage waveform.

In Fig. 17, the gate drive signals and the drain-source voltages of switches $S_2$, $S_4$ and $S_6$ are presented, respectively. These waveforms demonstrate that the voltage across switches has decreased to zero before the gate drive signal is given, which verify the turn-on ZVS operation.

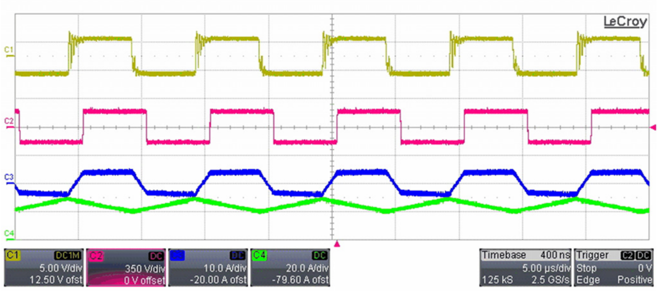


Fig. 14. Experimental waveforms in $V_{FC}$=30 VDC (input power 750 W) and $d$=$\pi$. $v_{T1b}$+$v_{T2b}$ [Ch1: 250 V/div], $v_{CO}$ [Ch2: 350 V/div], $i_{L2}$ [Ch3: 10 A/div] and $i_{L1}$ [Ch4: 20 A/div]. Time base: 5 *u*s/div.

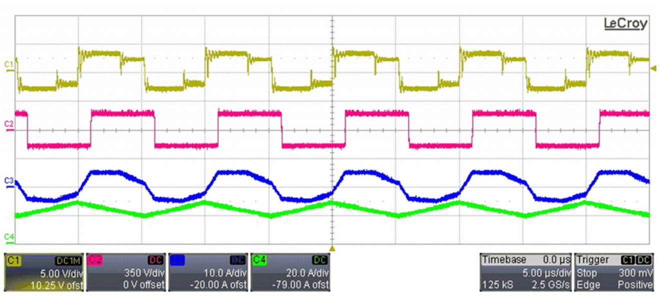


Fig. 15. Experimental waveforms in $V_{FC}$=30 VDC (input power 750 W) and $d$=0.65 $\pi$. $v_{T1b}$+$v_{T2b}$ [Ch1: 250 V/div], $v_{CO}$ [Ch2: 350 V/div], $i_{L2}$ [Ch3: 10 A/div] and $i_{L1}$ [Ch4: 20 A/div]. Time base: 5 *u*s/div.

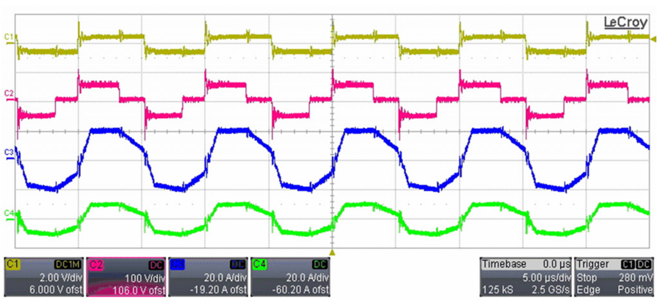
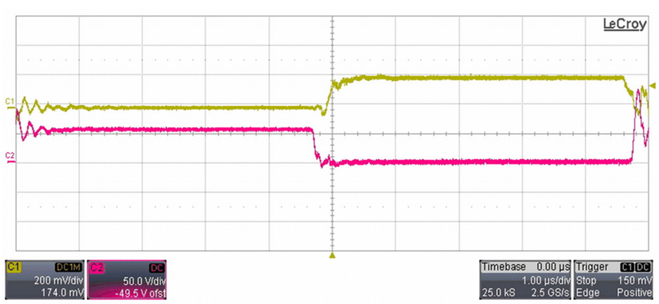
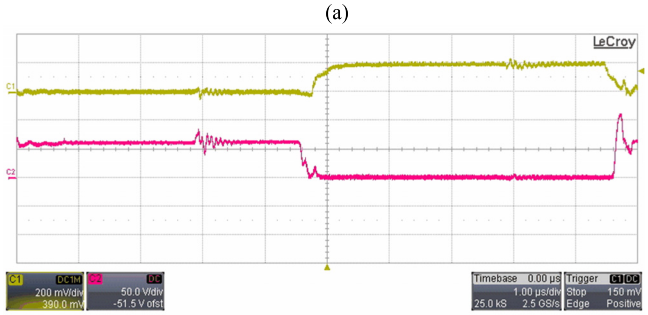


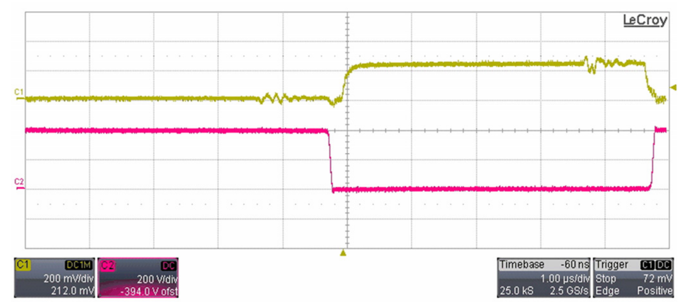
Fig. 16. Experimental waveforms in $V_{FC}$=30 VDC (input power 750 W) and $d$=0.65 $\pi$ condition. $v_{AN}$ [Ch1: 100 V/div], $v_{AB}$ [Ch2: 100 V/div], $i_{T1a}$ [Ch3: 20 A/div] and $i_{T2a}$ [Ch4: 20 A/div]. Time base: 5 *us*/div.



(a)



(b)



(c)

Fig. 17. Drain-source voltage $v_{ds}$ and gate drive signal $v_{gs}$ of the switches in $V_{FC}$=30 VDC and input power 750 W. (a) $S_2$: $v_{gs2}$ [Ch1: 10 V/div] and $v_{ds2}$ [Ch2: 50 V/div]. (b) $S_4$: $v_{gs4}$ [Ch1: 10 V/div] and $v_{ds4}$ [Ch2: 50 V/div]. (c) $S_6$: $v_{gs6}$ [Ch1: 10 V/div] and $v_{ds6}$ [Ch2: 200 V/div]. Time base: 1 *u*s/div.

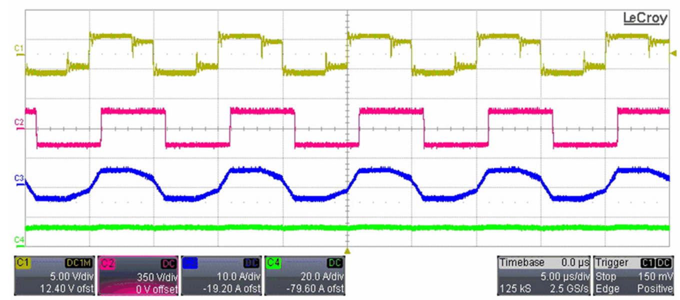


Fig. 18. Experimental waveforms in the super-capacitor power mode with the condition $V_{SC}$= 60 V, input power 750 W. $v_{T1b}$+$v_{T2b}$ [Ch1: 250 V/div], $v_{CO}$ [Ch2: 350 V/div], $i_{L2}$ [Ch3: 10 A/div] and $i_{SC}$ [Ch4: 20 A/div]. Time base: 5 *u*s/div.

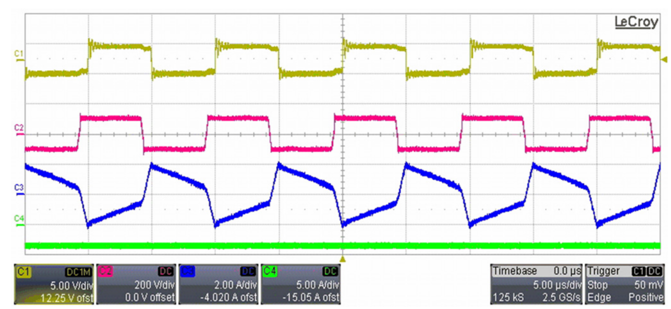


Fig. 19. Experimental waveforms when $d$= $\pi$ in the super-capacitor recharge mode with the condition $V_o$= 200 V, output power 100 W. $v_{T1b}$+$v_{T2b}$ [Ch1: 250 V/div], $v_{CO}$ [Ch2: 200 V/div], $i_{L2}$ [Ch3: 2 A/div] and $i_{SC}$ [Ch4: 5 A/div]. Time base: 5 *u*s/div.

In Fig. 18 the experimental results under the super-capacitor power mode are given. Compared to the waveforms shown in Fig. 15, the only difference is that input current $i_{L1}$ is replaced by $i_{SC}$, which is the output current of super-capacitor bank, because load is powered by the super-capacitors in this mode. In the super-capacitor recharge mode with 200 V output voltage, Fig. 19 and Fig. 20 show the experimental waveforms under the cases: $d$=$\pi$ and $d$≠$\pi$, respectively. The waveform of $v_{CO}$ is leading to that of $v_{T1b}$+$v_{T2b}$, which means that the phase-shift angle is negative in this case and $i_{SC}$ reverses to charge the super-capacitors. The similar quasi-optimal design method based on the phase-shift control and the duty cycle control can also be derived in this mode.

Fig. 21 shows the efficiency curves of the converter operating under the boost mode with the designed quasi-

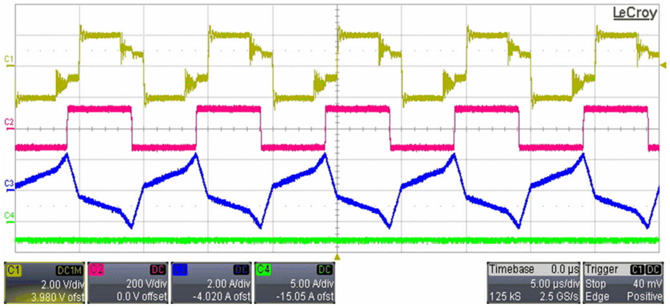


Fig. 20. Experimental waveforms when $d \neq \pi$ in the super-capacitor recharge mode with the condition $V_o$= 200 V, output power 100 W. $v_{T1b}+v_{T2b}$ [Ch1: 100V/div], $v_{CO}$ [Ch2: 200 V/div], $i_{L2}$ [Ch3: 2 A/div] and $i_{sc}$ [Ch4: 5A/div]. Time base: 5 *us*/div.

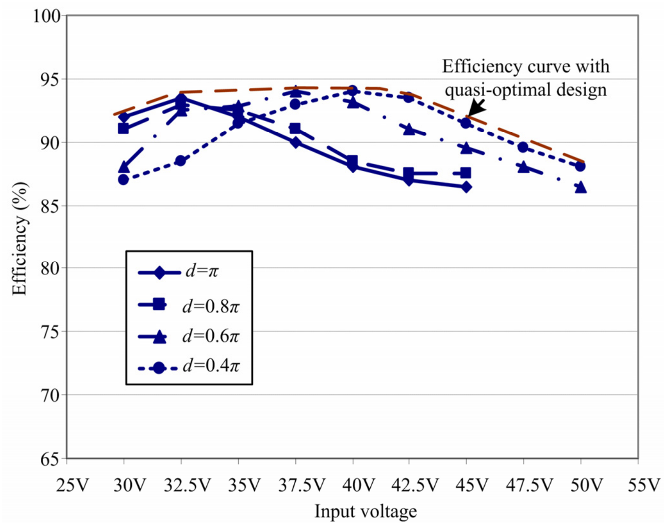



Fig. 21. The efficiency curves.

optimal phase-shift plus duty cycle control when output power is 900 W. By the quasi-optimal design method the converter efficiency is increased in the entire input voltage range as the enveloping line of the efficiency curves shown in Fig. 21, because using the duty cycle control one can find the maximal efficiency point with respect to the variable input voltage.

## V. Conclusion

A novel hybrid bidirectional DC-DC converter consisting of a current-fed input port and a voltage-fed input port was proposed and studied. Using the steady-state analysis, the relationship between the voltage gains of the proposed converter was presented to analyze the power flows. The simple quasi-optimal design method was investigated to reduce the current AC RMS current and extend the ZVS range. Experiments showed good agreement with theoretical analysis and calculation. Additionally, the experimental results reveal that the duty cycle control can effectively eliminate the reactive power and increase the efficiency when input voltage is varied over a wide range. So we can conclude that the proposed converter is a promising candidate circuit for the fuel cell and super-capacitor applications. Due to the limitation of present experiments, energy management strategies to control system power and achieve high overall efficiency of the proposed hybrid system will be studied in the future.

## Appendix

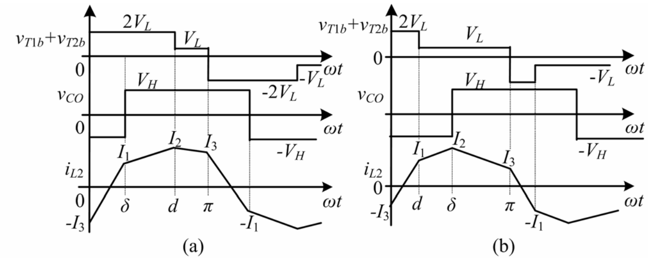



Fig. 22. The prototype of the proposed converter.

In the boost mode, in order to calculate the key values and parameters of the proposed converter, the simplified typical operating waveforms are plotted in Fig. 22.

When $0 \le \delta \le d$, referring to the waveforms shown in Fig. 22 (a), the piecewise curve of transient current $i_{L2}$ can be expressed by the formula in each interval as:

$$i_{L2}(\omega t)=\begin{cases} \dfrac{-I_3\cdot\delta+(I_1+I_3)\cdot\omega t}{\delta} & (0\le\omega t<\delta) \\ \dfrac{I_1\cdot d-I_2\cdot\delta+(I_2-I_1)\cdot\omega t}{d-\delta} & (\delta\le\omega t<d) \\ \dfrac{-I_2\cdot\pi+I_3\cdot d+(I_2-I_3)\cdot\omega t}{-\pi+d} & (d\le\omega t\le\pi) \end{cases} \tag{18}$$

where $I_1=i_{L2}(\delta)$, $I_2=i_{L2}(d)$ and $I_3=i_{L2}(\pi)$.

Using Faraday's law and voltage-second balance on the interface inductor $L_2$, we can obtain the relationships between the current values and circuit parameters as:

$$\begin{aligned} I_1+I_3&=\frac{(2V_L+V_H)}{\omega L}\cdot\delta \\ I_2-I_1&=\frac{(2V_L-V_H)}{\omega L}\cdot(d-\delta) \\ I_2-I_3&=\frac{(V_H-V_L)}{\omega L}\cdot(\pi-d) \end{aligned} \tag{19}$$

Hence, $I_1$, $I_2$ and $I_3$ can be calculated by (19) and the results are presented in (7). If any loss of the converter is ignored, the output power can be obtained form (20). According to (18), the current RMS value of $i_{L2}$ is calculated by (21).

When $0 \le d \le \delta$, as shown in Fig. 22 (b), transient current $i_{L2}$ can be expressed as:

$$i_{L2}(\omega t)=\begin{cases} \dfrac{-I_3\cdot d+(I_1+I_3)\cdot\omega t}{d} & (0\le\omega t<d) \\ \dfrac{I_1\cdot\delta-I_2\cdot d+(I_2-I_1)\cdot\omega t}{\delta-d} & (d\le\omega t<\delta) \\ \dfrac{I_2\cdot\pi-I_3\cdot\delta+(I_3-I_2)\cdot\omega t}{\pi-\delta} & (d\le\omega t\le\pi) \end{cases} \tag{22}$$

where $I_1=i_{L2}(d)$, $I_2=i_{L2}(\delta)$ and $I_3=i_{L2}(\pi)$.

According to (18) the current RMS value of $i_{L2}$ is calculated by (21). Similar to (19), using Faraday's law and voltage-second balance on the interface inductor $L_2$, $I_1$, $I_2$ and $I_3$ can be can be calculated by

$$\begin{aligned} I_1 &= \frac{(\pi+2d-2\delta)V_H+(3d-\pi)V_L}{2\omega L_2} \\ I_2 &= \frac{\pi V_H+(2\delta+d-\pi)V_L}{2\omega L_2} \\ I_3 &= \frac{(2\delta-\pi)V_H+(d+\pi)V_L}{2\omega L_2} \end{aligned} \tag{23}$$

Hence, the average output power in this case can be obtained from (24). With similar waveform analysis method, and calculation procedure, all the values in the super-capacitor power mode and the recharge mode, such as output power, current peak value, RMS value etc. can be obtained as well.

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$$\begin{aligned} P_O &= \frac{\int_0^{\pi}\left(v_{T1b+T2b}(\omega t)\cdot i_{L2}(\omega t)\right)\cdot d\omega t}{\pi} = \frac{1}{2\pi}\cdot\left((I_1-I_3)\cdot(\delta-0)\cdot 2V_L+(I_1+I_2)\cdot(d-\delta)\cdot 2V_L+(I_2+I_3)\cdot(\pi-d)\cdot V_L\right) \\ &= \frac{V_LV_H\left(2\pi\delta-4\delta^2+2\delta d+\pi d-d^2\right)}{2\pi\omega L_2} \end{aligned} \tag{20}$$

$$\begin{aligned} I_{L2RMS} &= \sqrt{\frac{1}{\pi}\cdot\left[\int_0^{\delta}\left(\frac{(I_1+I_3)\cdot\omega t-I_3\delta}{\delta}\right)^2\cdot d(\omega t)+\int_{\delta}^{d}\left(\frac{(I_2-I_1)\cdot\omega t-I_2\delta+I_1 d}{d-\delta}\right)^2\cdot d(\omega t)+\int_d^{\pi}\left(\frac{(I_2-I_3)\cdot\omega t-I_2\pi+I_3 d}{d-\pi}\right)^2\cdot d(\omega t)\right]} \\ &= \frac{\sqrt{3}}{3}\cdot\sqrt{\frac{(\pi-\delta)I_2^2+\left[(\pi-d)I_3+(d-\delta)I_1\right]I_2+(\pi+\delta-d)I_3^2-I_1I_3\delta+I_1^2 d}{\pi}} \end{aligned} \tag{21}$$

$$\begin{aligned} P_O &= \frac{\int_0^{\pi}\left(v_{T1b+T2b}(\omega t)\cdot i_{L2}(\omega t)\right)\cdot d\omega t}{\pi} = \frac{1}{2\pi}\cdot\left((I_1-I_3)\cdot(d-0)\cdot 2V_L+(I_1+I_2)\cdot(\delta-d)\cdot V_L+(I_2+I_3)\cdot(\pi-\delta)\cdot V_L\right) \\ &= \frac{V_LV_H\left(2\pi\delta-2\delta^2-2\delta d+\pi d+d^2\right)}{2\pi\omega L_2} \end{aligned} \tag{24}$$

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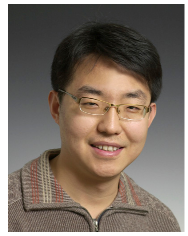

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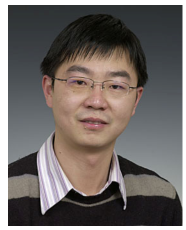

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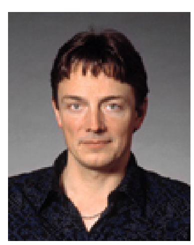

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