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Experimental investigation and digital compensation of DGD for 112 Gb/s PDM-QPSK clock recovery

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Abstract: For asynchronous sampled systems such as Polarization Division Multiplexed Quadrature Phase Shift Keying, (PDM-QPSK), phase and frequency of the sampling clock is typically not synchronized to the data symbols. Therefore, timing adjustment, so called clock recovery and interpolation, must be performed in digital domain prior to signal demodulation in order to avoid cycle slips. For the first time, the impact of first order PMD, (DGD), is experimentally investigated and quantified for 112 Gb/s PDM-QPSK signal. We experimentally show that the combined effect of polarization mixing and first order PMD can significantly affect the performance of the timing error detector gain, even for moderate values leading to system outage. We propose and experimentally demonstrate a novel digital adaptive timing error detector is robust to polarization mixing and DGD. The proposed timing error detector algorithm combines the Gardner timing error detector algorithm with an adaptive structure based on gradient method.

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1. Introduction

Advanced modulation formats have recently attracted large attention due to their ability to provide high capacity and spectrally efficient communication systems. Especially, 112 Gb/s systems employing PDM-QPSK are seen as a promising candidate for the next generation of high-capacity transmission systems. For detection of 112 Gb/s PDM-QPSK signals either asynchronous or synchronous sampling can be employed at the receiver. Typically, for 112 Gb/s PDM-QPSK systems, asynchronous sampling has been employed [1–4]. For the asynchronous sampled systems, the sampling is not synchronized to the incoming signal, i.e. sampling clock is independent of the symbol timing. Even though it would be possible to build extremely accurate oscillators, there would always exist a small difference in frequency between the free-running sampling clock and data symbols. This frequency difference must be therefore corrected in the digital domain in order to avoid cycle slips, as it is done for digital modems for wireline communication [5–8]. Therefore, for asynchronous sampled system such as PDM-QPSK it is imperative that the sampled signal must be adjusted/re-sampled/interpolated by digital methods in order to obtain the correct signal values, i.e. the same signal values that would occur if the sampling had been synchronized to the symbols. This process of signal timing adjustment is commonly referred as *clock-recovery and interpolation*. Therefore, for 112 Gb/s PDM-QPSK systems clock recovery and interpolation is done before linear equalization, including chromatic and polarization mode dispersion compensation, carrier phase recovery and decoding as demonstrated in references [1–4]. The output of the clock recovery module would therefore have correct sample values and thereby an integer number of samples per symbol, typically 1 or 2.

Recent works on 112 Gb/s CP-QPSK systems have reported on fully digital clock recovery and interpolation, see [1–4] and references therein. However, most of the techniques implemented for 112 Gb/s CP-QPSK systems are borrowed from RF communication systems [6]. The crucial part for the digital clock recovery and interpolation is the timing error detector which outputs an amount of timing error, with respect to if the sampling has been synchronized to the symbols, that is present in the signal. Typically, for 112 Gb/s CP-QPSK, the system is sampled at twice the symbol rate (~ 2 samples/symbol), and this limitation imposes some restrictions on the versatility of timing error detector schemes that can be implemented. It has been shown that the combined effects of polarization rotation and DGD can significantly affect the performance of the timing error detector gain of the clock recovery leading to system outage [9–13]. Even though the mentioned problem is very relevant, for the design of digital coherent receivers, solutions to this particular problem have been sparse [12,13]. Additionally, most of the work done on this topic have relayed on numerical simulations [9–13].

In this paper, the impact of DGD in the presence of polarization rotation on the digital clock recovery is experimentally investigated and quantified for polarization multiplexed 112 Gb/s QPSK system. In general, the experimental work confirms the investigations based on numerical simulations. Compared to the numerical simulations results, the experimental findings are more pessimistic as they indicate that even for relatively moderate values of DGD the clock recovery may fail, pointing out the importance of compensating the DGD. Additionally, we present and experimentally demonstrate a novel adaptive timing error detector algorithm whose performance is independent of polarization rotation angle and DGD. Compared to the solution presented in [13], our approach is simpler because only a single adaption loop is needed; i.e. only a single update algorithm is used to restore timing detector gain.

2. Experimental set-up

The outline of the experimental set-up for the investigation of the impact of the DGD and its compensation, for 112 Gb/s PDM-QPSK system is shown in Fig. 1. The DSP block contains only the clock recovery module as it is the main focus of the paper, see Fig. 2. As QPSK modulation format in combination with polarization multiplexing is used, we have 4 bits/symbol, and therefore the input binary data stream is parallelized into four binary data streams (2 bits/symbol for QPSK plus two polarizations). The parallelized data streams are then used to drive two nested Mach-Zehnder Modulators (MZM) for QPSK modulation, each for one polarization, i.e. x and y. The nested MZM are modulated by 28 Gb/s data streams. Using a polarization beam splitter (PBS), the -x and -y polarization components are combined to form a polarization multiplexed data signal and launched into the transmission span. The optical 112 Gb/s PDM-QPSK data signal is then applied to a DGD emulator for which the mean value of the DGD can be specified. We vary the DGD from 0 to 38.20 ps. Throughout the entire experiment, an OSNR of 20 dB is kept constant. In order to detect and demodulate the PDM-QPSK signal, a polarization-diversity coherent receiver, in combination with digital signal processing, is used, see Fig. 1. At the receiver, following a PBS, the two orthogonal polarizations are mixed with the local oscillator laser in two 90 degree optical hybrids, detected with four pairs of balanced photodiodes and then sampled at 80 Gs/s. The sampled signal is then sent to digital signal processing containing the clock recovery.

The sampled data, $V_{xi}(n)$, $V_{xq}(n)$, $V_{yi}(n)$ and $V_{yq}(n)$, where n is an integer, are then sent to the DSP block which only contains the clock recover module in this particular case, see Fig. 2(a) In this paper, for simplicity, we only consider the x-polarization clock recovery and interpolation module. However, the results obtained for the x-polarization module are also applicable to the y-polarization. Following Fig. 2(a), the signal samples from the analogue-to-digital converter (ADC), $V_{xi}(n)$ and $V_{xq}(n)$, are applied to the interpolator, which then computes the correct data signal samples using an appropriate control signal. The feedback loop controlling the interpolator consists of the Gardner timing error detector, a loop filter and a numerically controlled oscillator (NCO). The Gardner timing error detector is used to produce the error signal $y(n)$ for the control of the loop and its output is written as [9]:

$$y(n) = V_{xi}(n-2)\{V_{xi}(n-3) - V_{xi}(n-1)\} + V_{xq}(n-2)\{V_{xi}(n-3) - V_{xi}(n-1)\} \quad (1)$$

The timing error detector is one of most crucial part of the clock recovery and its performance can be characterized by the timing error detector gain, K_d . The K_d can be computed by evaluating the magnitude of the DC component present at the output of the timing error detector [7]:

$$K_d = \frac{1}{N_{seq}} \sum_{n=-N_{seq}/2}^{N_{seq}/2} y(n) \quad (2)$$

where N_{seq} is the length of sequence over which the averaging is performed. As already mentioned, it has been shown in [9–13] that the standard configuration for the clock recovery will fail due to the combined effect of polarization mixing and DGD. In this paper, we therefore propose a new scheme in which we employ an adaptive timing error detector which performs polarization separation prior to timing error detection and thereby mitigates the impact of polarization mixing and DGD. This configuration is shown in Fig. 2(b) and will be explained in more details in section 3.2.

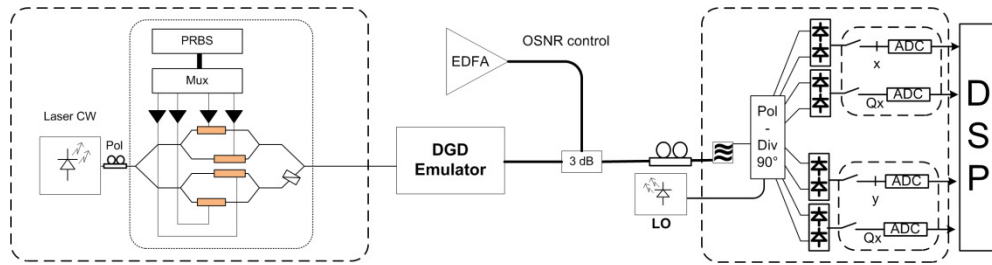


Fig. 1. General outline of the experimental set-up for 112 Gb/s PDM-QPSK system.

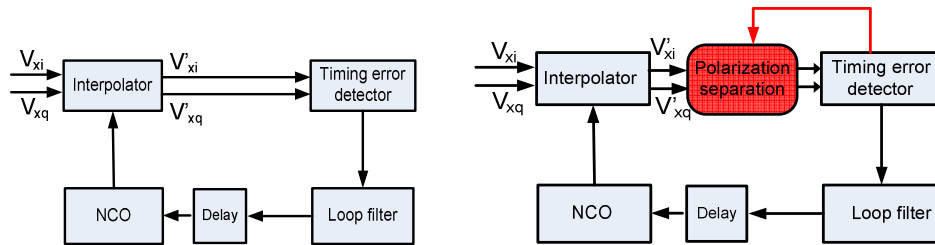


Fig. 2. (a) Clock recovery and the interpolation module. (b) Clock recovery and interpolation module employing an adaptive timing error detector.

3. Results

3.1 Performance of Gardner timing error detector

In Fig. 3 the normalized timing error detector gain, K_d , is plotted as a function of polarization rotation angle, α , for a DGD of 50% of the symbol rate, T_{sym} , for the obtained experimental data. It is observed in Fig. 3 that as the polarization rotation angle α approaches 45° , the timing error detector gain drops by the several orders of magnitude, and this means that the clock recovery loop will not be able to obtain a lock. This is in accordance with the simulation results presented in [9–11]. In general, the timing error detector gain will drop every $45^\circ + p90^\circ$, where p is an integer. The next value for which the timing error detector gain approaches zero is 135° , as shown in Fig. 3. According to Fig. 3, the normalized timing error detector gain is unaffected for $\alpha = 0$ and 90° , because for those two cases the $-x$ and $-y$ signal polarization components will not mix.

In order to quantify the impact of the DGD on the performance of the timing error detector, and thereby the clock recovery module, a histogram has been constructed in Fig. 4. The histogram depicts the number of failures for the experimentally obtained data as the DGD has been varied from 0 until 107% of T_{sym} . In order to construct the histogram, we had access to 200 traces in total. The failure is defined as the occurrence when the normalized K_d has dropped more than 15 dB when the polarization rotation angle is in the range from 0 to 90° . The reason why we defined a 15 dB as the limit is because as shown in [9], if the timing error detector gain is dropped more than 15 dB the clock recovery will not be able to satisfy the jitter tolerance curve. As expected the largest number of failures occurs when the DGD is in the range from 40 to 50% of T_{sym} . Additionally, Fig. 4 shows that even though for relatively moderate values of the specified DGD, a certain number of failures will occur.

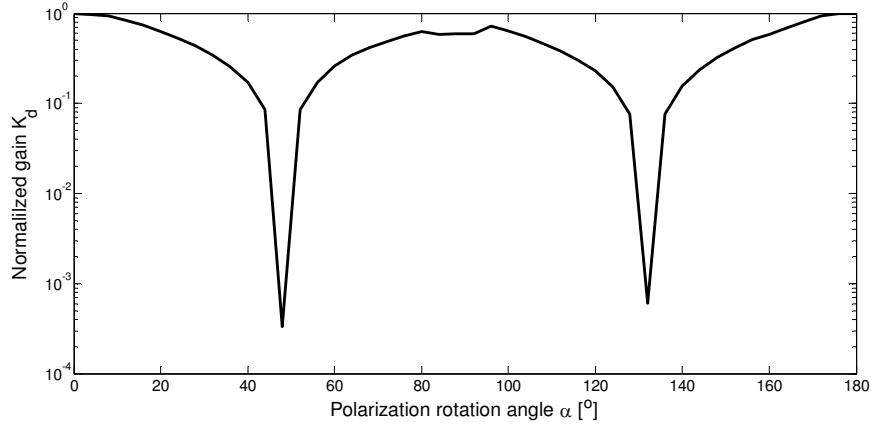


Fig. 3. Normalized timing error detector gain, K_d , as a function of polarization rotation angle for the DGD of $0.5T_{\text{sym}}$.

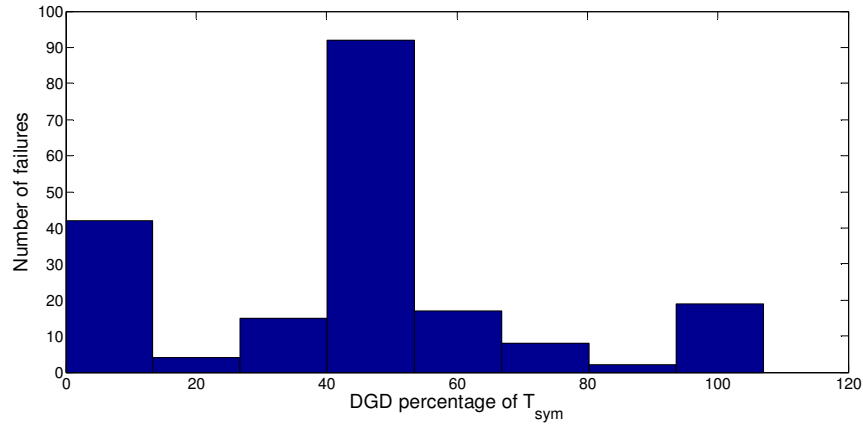


Fig. 4. Histogram depicting the number of failures as the DGD is varied from 0 to 107% of T_{sym} . 3.2 Adaptive timing error detector

In general, the Gardner timing error detector algorithm works fine as long as the input to the timing error detector does not contain contribution from both horizontal and vertical optical data signal components. The idea would therefore be to re-use the Gardner timing error detector algorithm, however, with some adaptive modification so that it is ensured that it is only the data associated with a single polarization component of the optical signal enters the Gardner timing error detector, as it will be shown shortly. The effect of polarization mixing is a linear effect, and the sampled signal components of the optical field, $V_{xi}(n)$, $V_{xq}(n)$, V_{yi} and $V_{yq}(n)$, where n is an integer, can be expressed as:

$$V_{xi}(n) = a(n)\cos(\alpha) - b(n)\sin(\alpha) \quad (3)$$

$$V_{yi}(n) = a(n)\sin(\alpha) + b(n)\cos(\alpha) \quad (4)$$

$$V_{xq}(n) = c(n)\cos(\alpha) - d(n)\sin(\alpha) \quad (5)$$

$$V_{yq}(n) = c(n)\sin(\alpha) + d(n)\cos(\alpha) \quad (6)$$

where

$$a(n) = x_{h,i}(n) \cos(\varphi(n)) - x_{h,q}(n) \sin(\varphi(n)) \quad (7)$$

$$b(n) = x_{v,i}(n - \Delta T_{DGD}) \cos(\varphi(n)) - x_{v,q}(n - \Delta T_{DGD}) \sin(\varphi(n)) \quad (8)$$

$$c(n) = x_{h,i}(n) \sin(\varphi(n)) + x_{h,q}(n) \cos(\varphi(n)) \quad (9)$$

$$d(n) = x_{v,i}(n - \Delta T_{DGD}) \sin(\varphi(n)) + x_{v,q}(n - \Delta T_{DGD}) \cos(\varphi(n)) \quad (10)$$

where $\{x_{h,i}(n), x_{h,q}(n)\}$ and $\{x_{v,i}(n), x_{v,q}(n)\}$ are data streams associated with the horizontal and vertical optical data signal component, respectively. ΔT_{DGD} is the differential group delay of the vertical optical signal component with respect to the horizontal optical data signal component. $\varphi(n)$ takes into account the total phase and frequency difference between the transmitter and LO laser. However, if the polarization mixing angle α is known the data signal components can be recovered as follows:

$$V_{xi}^{rec}(n) = V_{xi}(n) \cos(\alpha) + V_{yi}(n) \sin(\alpha) = a(n) \quad (11)$$

$$V_{xq}^{rec}(n) = V_{xq}(n) \cos(\alpha) + V_{yq}(n) \sin(\alpha) = c(n) \quad (12)$$

$$V_{yi}^{rec}(n) = -V_{xi}(n) \sin(\alpha) + V_{yi}(n) \cos(\alpha) = b(n) \quad (13)$$

$$V_{yq}^{rec}(n) = -V_{xq}(n) \sin(\alpha) + V_{yq}(n) \cos(\alpha) = d(n) \quad (14)$$

Now, if Eqs. (11)-(14) could be implemented as a part of the Gardner timing error detector, the input signal to the timing error detector V_{xi}^{rec} , V_{yi}^{rec} , V_{xq}^{rec} and V_{yq}^{rec} would not contain signal components from the other polarization, and thereby the Gardner timing error detector will not be affected by the polarization mixing and the DGD. A novel adaptive timing error timing detector structure which uses Eq. (11) in combination with the Gardner timing error detector is shown in Fig. 4. For the particular case shown in Fig. 4, the adaptive timing error detector works on signal components V_{xi} and V_{yi} and applies Eq. (11) in order to make sure that data stream only associated with a single optical data signal polarization component enters the Gardner timing error detector. The similar structure can be employed to work on signal components V_{xq} and V_{yq} . However, in order to demonstrate the working principle of the scheme we concentrate on V_{xi} and V_{yi} signal components only.

The working principle behind the structure shown in Fig. 4 is as follow. We use the gain of the Gardner timing error detector K_d defined in Eq. (2), as an error/control signal for the an adaptive timing error detector scheme in Fig. 4, since K_d is a good indicator of the amount of polarization mixing and the DGD present in the detected signals V_{xi} and V_{yi} , as illustrated in Fig. 2(a). In general, we need to look for a value of α which would maximize the timing error detector gain K_d . We can therefore define the following optimization function:

$$J = \arg \max_{\alpha \in \{0, \pi\}} \{K_d(\alpha)\} \quad (15)$$

Now, if α_{est} is denoted as the estimate of the angle α using the gradient algorithm we can adaptively estimate α_{est} as [7]:

$$\alpha_{est}(n+1) = \alpha_{est}(n) - \frac{1}{2} \mu \frac{dK_d}{d\alpha} \quad (16)$$

where μ is a step-size parameter. Moreover, to guarantee that the scheme reported in Fig. 4 converges, it must be ensured that the error signal, K_d , has minima/maxima. Using Eq. (1), (2), (3), (4), (11) and (16) it can be shown that:

$$\frac{dK_d}{d\alpha_{est}} = \left\{ \frac{1}{N_{seq}} \sum_{n=N_{seq}/2}^{N_{seq}/2} a(n-2) \{a(n-3) - a(n-1)\} - b(n-2) \{b(n-3) - b(n-1)\} \right\} \times \sin(2(\alpha - \alpha_{est})) \quad (17)$$

Equation (17) demonstrates that, provided the existence of minima/maxima in the error signal K_d the adaptive timing error detector scheme will converge, i.e: $dK_d/d\alpha_{est} \rightarrow 0$ as $\alpha_{est} \rightarrow \alpha$. In order to evaluate the error/control signal for the adaptive timing error detector, the feedback loop in Fig. 4, is open after the module where K_d is computed. In Fig. 5(a), the normalized Gardner timing error detector gain K_d is plotted as a function of α_{est} . For Fig. 5(a), the polarization mixing angle α is set to 45° and the DGD is $0.5T_{sym}$. It is observed in Fig. 5(a), that K_d contains maxima/minima and therefore can be used as the error/control signal for the structure in Fig. 4. Additionally, for $\alpha_{est} = \pi/4 + p\pi$, where $p \in \mathbb{Z}$, the timing error detector gain can be fully recovered, i.e $K_d = \pm 1$. Therefore, we can use the gradient algorithm in Eq. (15) in order to “lock” at the minima/maxima of the error signal curve shown in Fig. 5(a). In general, it can be stated that the operation of the proposed adaptive timing error detector structure in Fig. 4, based on the gradient algorithm, resembles the operation of the first-order phase-locked loop if the filter $W(z)$ is omitted.

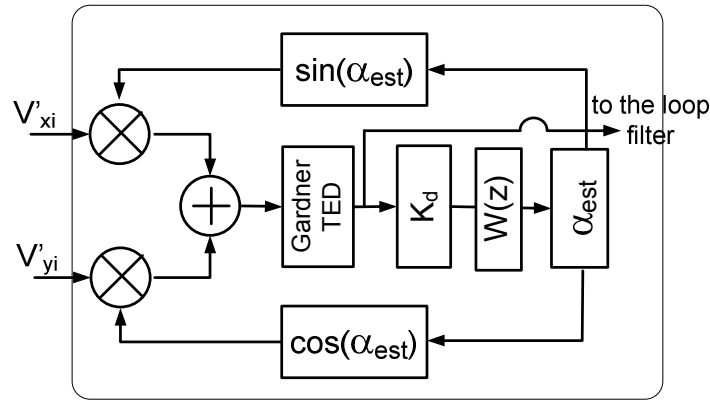


Fig. 4. An adaptive timing error detector scheme. $W(z)$ is a digital loop filter.

Next, the operation of the adaptive timing error detector scheme is first demonstrated using numerical simulations. Parameters for the numerical simulation are the same as for the experimental set up described in section 2. The main idea is that, after applying the adaptive timing error detector scheme, the output of the Gardner timing error detector gain should not be affected by α and the DGD, i.e. K_d should remain unchanged as the angle α takes different values in the presence of the DGD. In Fig. 5(b), the normalized Gardner timing error detector gain K_d is plotted as a function of a number of iterations after applying the adaptive timing error detector structure in Fig. 4 for the selected value of α . The angle α is varied from 22.5° to 90° and the DGD is fixed at $0.5T_{sym}$. It can be observed in Fig. 5(b), that the scheme converges and the normalized timing error detector gain K_d approaches 1 irrespective of the considered value of α . This means that the output of the Gardner timing error detector can now be used to control the rest of the clock recovery and interpolation loop shown in Fig. 2.

The value of K_d and α_{est} is evaluated per block of data signal samples and in Fig. 5(b) and the block length is set to 4096 samples. Therefore, each iteration in Fig. 5(b) corresponds to 2^{12} (4096) samples. It is observed in Fig. 5(b) that the normalized timing error detector gain can be fully recovered from approximately 0 to 1 for $\alpha = 45^\circ$, while for $\alpha = 90^\circ$ the K_d remains unchanged as expected. One of the important parameters of the adaptive timing error detector structure in Fig. 4, is the length of the sequence N_{seq} over which the Gardner timing error detector gain is evaluated since the gain of the Gardner timing error detector is used to

control the adaptive structure. In Fig. 6, we have therefore plotted the normalized Gardner timing error detector gain K_d for the selected values of N_{seq} . It is observed in Fig. 6, that for $N_{\text{seq}} = 2^9$, the adaptive structure exhibits small oscillations during the lock in process.

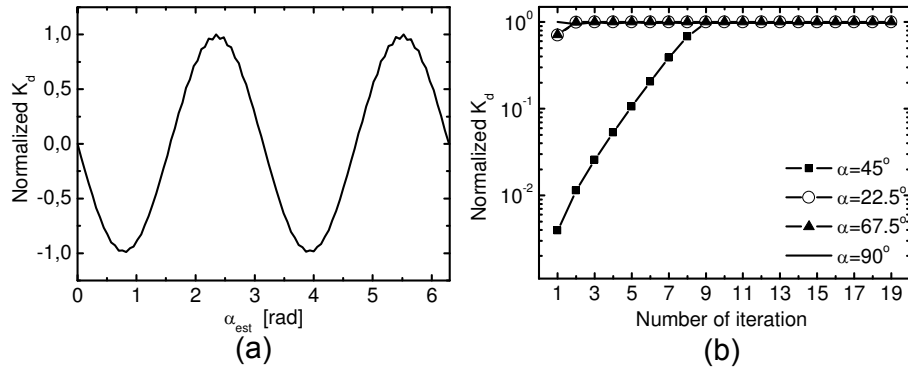


Fig. 5. (a) Normalized Gardner timing error detector gain K_d as a function of α for the open loop configuration of. (b) *Simulation data*: Normalized Gardner timing error detector gain, K_d , as a function of number of iterations for α ranging from 22.5° to 90° after applying the adaptive structure in Fig. 4.

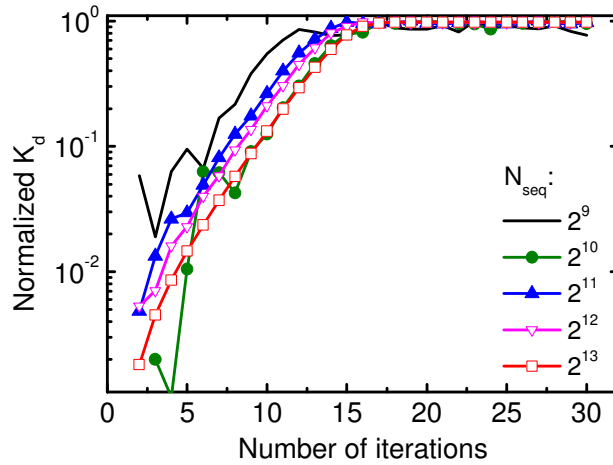


Fig. 6. Normalized Gardner timing error detector gain K_d as a function of number of iterations for the selected values of the length of the sequence N_{seq} .

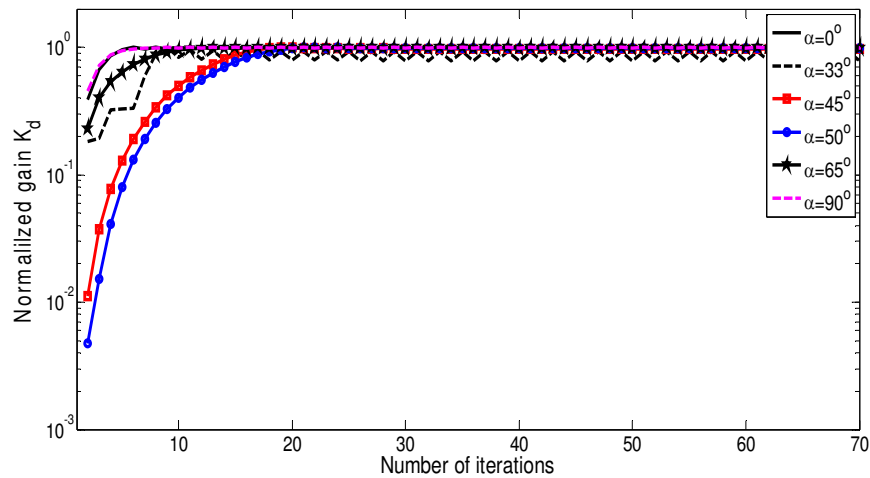


Fig. 7. *Experimental data*: Normalized Gardner timing error detector gain, K_d , as a function of number of iterations for polarization rotation angle ranging from 0 to 90° after applying the adaptive structure in Fig. 4. The DGD is 50% of T_{sym}

Finally, in Fig. 7, the normalized Gardner timing error detector gain K_d is plotted as a function of a number of iterations after applying the adaptive timing error detector structure in Fig. 4 for the selected value of polarization rotation angle of the experimental data. The polarization angle is varied from 0 to 90° and the DGD is fixed at 50% of T_{sym} , which is the worst case. It can be observed in Fig. 7, that the scheme converges and the normalized timing error detector gain K_d approaches 1 irrespective of the considered value of polarization rotation angle. There is also a qualitatively good agreement with Fig. 5(b) which is obtained using the data from numerical simulations. It is worth mentioning that using the experimental data number of iterations used to obtain the convergence is increased. In general, the presented scheme for the adaptive timing error detector can be used for any type of timing error detector and thereby easily expanded to 16-QAM.

4. Conclusion

Experimental investigations of the impact of the DGD on the timing error detector for 112 Gb/s PDM-QPSK system have been presented. We have shown that even for the moderate values of DGD a timing error detector gain can be significantly decreased leading to the failure of the clock recovery and thus making the compensation of DGD imperative. A novel adaptive timing error detector scheme has therefore been proposed and successful experimental demonstration has been confirmed. We have shown that after applying the adaptive timing error detector structure, the output of the Gardner timing error detector remains unchanged irrespective of the polarization mixing angle and the DGD.

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