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# Modeling and Control of a Dual-Input Isolated Full-Bridge Boost Converter

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*Abstract*— **In this paper, a steady-state model, a large-signal (LS) model and an ac small-signal (SS) model for a recently proposed dual-input transformer-isolated boost converter are derived respectively by the switching flow-graph (SFG) nonlinear modeling technique. Based upon the converter's model, the controllers are then designed regarding to power stage parameters and system dynamic requirements. The entire system energy management has been designed as well with the consideration on static and dynamic characteristics of the two different input energy sources. A prototype has been fabricated and tested. The measured experimental results match the simulation results fairly well on both input source dynamic and step load transient responses.**

## I. INTRODUCTION

In order to utilize more than one renewable energy sources in a hybrid power conversion system, multi-port or multi-input converters have been proposed and received more and more attentions in recent years for the applications, such as hybrid vehicles, photovoltaic (PV)-wind power systems and uninterruptible power supplies (UPS) [1]-[4]. Generally, the multi-port converters can save the amount of inductors, transformers and/or capacitors as compared to the ones obtained by simply paralleling the outs of the converters [5]-[8]. In addition, with these topologies, it is possible to achieve flexible utilization for the energy sources with intermittent properties such as PV panels. As an example, a transformer-isolated dual-input dc-dc converter is presented in Fig. 1. In order to overcome the major obstacles, e.g. high input current and high voltage conversion ratio, in a fuel cell-supercapacitor hybrid power system, a new dual-input transformer-isolated full-bridge boost converter has been proposed by the authors in [9]. When both of the energy sources are supplied to the proposed converter, they will deliver power to the load simultaneously without disturbing each other's operation, and when only one of the input sources is connected, the converter will operated as does a normal isolated boost converter. Furthermore, in a hybrid renewable energy system, the effective dynamics control and power management are required to attenuate the effects caused by characteristics of energy sources and to achieve the required system performance. Hence, the focus of this paper is on the modeling and control design of the proposed dual-input isolated boost converter. Before the controller design, modeling converter must be implemented effectively. A switching flow-graph (SFG) modeling technique has been proposed and developed for PWM converters [10]-[12]. Comparing with other modeling methods, such as state space averaging and averaged switch modeling, the SFG is a powerful analysis tool to derive steady-state, LS and SS models as well as to describe various relationships between

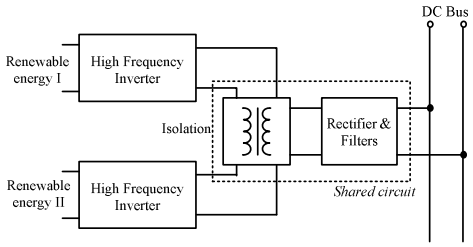



Figure 1. A block diagram of a two-input transformer-isolated converter.

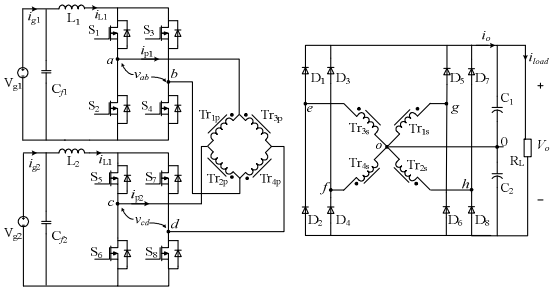


Figure 2. The proposed dual-input isolated full-bridge boost converter.

different circuit variables with minimum mathematical manipulations. By employing SFG, the model of the proposed converter is derived and the transfer functions are calculated. With the consideration on the dynamics of input power sources, a closed-loop digital control system with power management function has been designed and simulated. Finally, a prototype has been built and tested, and experimental results are presented to verify the effectiveness of the controller under input source dynamics and step load transients.

## II. MODELING THE PROPOSED DC-DC CONVERTER

### A. Swithing Flow-Graph Modeling Technique

With the SFG modeling method, basically, the switch functions of the power converter can be expressed by switch branches $k$ and $\overline{k}$. The gains of those switch branch are time dependent. Assuming that the small-ripple condition is satisfied, the equivalent output signal of the switching branch $k_i$ is equal to its average value over a switching cycle. Supposing the input signal and output signal of the $k_i$ are $x(t)$ and $y(t)$, the following equation is derived in (1), where $T_s$ is the switching period, and duty cycles $d_1+d_2+\ldots+d_n=1$.

$$y(t)=\frac{1}{T_s}\int_{t_{i-1}}^{t}x(t)dt=x(t)\frac{t_i-t_{i-1}}{T_s}=x(t)d_i(t),i=1,2,\ldots n \quad (1)$$

Adding small-signal perturbations at the steady state operating points, $X$, $Y$ and $D$, and at same time neglecting

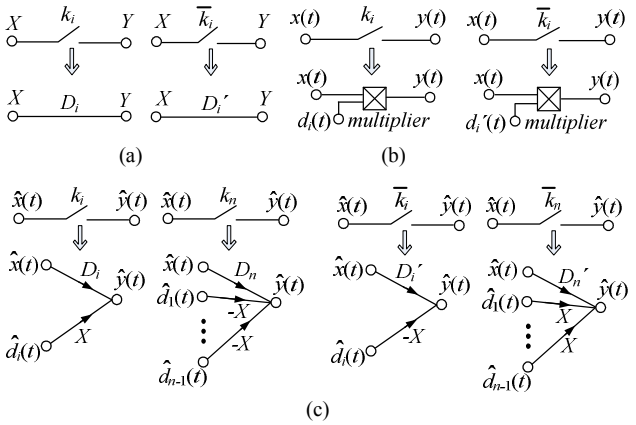



Figure 3. (a) The steady-state models of $k_i$; (b) The large models of $k_i$; (c) The small-signal models of $k_i$ and $k_n$.

the second-order perturbation terms yield the small-signal model for branch $k_i$ as described

$$\begin{aligned} y(t) = x(t)d_i(t) = Y + \hat{y}(t) = \left[X + \hat{x}(t)\right]\cdot\left[D_i + \hat{d}_i(t)\right] \\ \Rightarrow \hat{y}(t) = X\cdot\hat{d}_i(t) + D_i\cdot\hat{x}(t). \end{aligned} \tag{2}$$

Interchanging $d(t)$ with its complement $d'(t)$ leads to

$$\hat{y}(t) = -X\cdot\hat{d}_i(t) + D_i'\cdot\hat{x}(t). \tag{3}$$

Therefore, the steady-state, large-signal and small-signal models of the $k_i$ and $\overline{k}_i$ branches in the SFG can be derived and depicted in Fig. 3. Because the switching branches are the only nonlinear components in a SFG, a unified steady-state, large-signal and small-signal model can be obtained for a converter by replacing the switching branches with their models.

### *B. Obtaining the Model of the Dual-Input Boost Converter*

According to the operation principle analyzed in [9], under the continuous conduction mode (CCM), the timing diagrams and basic operating waveforms of the proposed dual-input isolated boost converter are plotted in Fig. 4, where $S_{L1}$ and $S_{L1}$ are the effective switching actions across the inductors $L_1$ and $L_2$, respectively. The effective inductor period $T_L$ and duty cycle $D_L$ [13], [14], are defined as follows:

$$T_L = T_s/2. \tag{4}$$

$$D_{Li} = 2D_i - 1 \ \ (i = 1 \ or \ 2). \tag{5}$$

There are three operating states in one inductor cycle. During $t_1<t<t_2$, on the primary side of transformers, switches $S_2$ and $S_3$ are in their Off-state, and $S_1$, $S_4$ and $S_5$~$S_8$ are in their On-state, so $L_1$ is discharged and $L_2$ is charged, respectively; while, during $t_3<t<t_4$, switches $S_6$ and $S_7$ are in Off-state, and $S_5$, $S_8$ and $S_1$~$S_4$ are in On-state, and thereby $L_1$ is charged and $L_2$ is discharged. During $t_2<t<t_3$ and $t_4<t<t_5$, both of $L_1$ and $L_2$ are charged at same time due to all the switches in their On-state on the primary side. When $d_{L1}+d_{L2}>1$, the two duty cycles are independent, so if these two duty cycles are controlled properly, the output voltage of the converter can be regulated with respect to two different input voltages. Therefore, the three sub-circuits of the proposed converter with *LC* input filter and their corresponding flow graphs $G_1$, $G_2$ and $G_3$, are obtained and depicted in Figs. 5, 6 and 7, where $R_{Lf1}$ and $R_{Lf2}$ are the parasitic resistance of input filter inductors; $R_{L1}$ and $R_{L2}$ are the parasitic resistances of boost inductor; $C_o$=0.5$C_1$=0.5$C_2$; $R_L$ is the load resistance; $n$ is turns ratio of the transformer and $n$=$N_S$:$N_P$; the reflected output voltage, output capacitance and load resistance on primary side are $V_o/n$, $n^2C_o$ and $R_L/n^2$, and denoted as $V_o'$, $C'$ and $R'$, respectively. These three flow graphs share all the nodes and part of the branches. By overlaying these flow graphs, it is observed that some branches exist in all flow graphs, while others exist only in one of them. Branches that exist in $G_1$, but not in $G_2$ and $G_3$ are replaced by $\overline{k}_1$ branches; branches that exist in $G_2$, but not in $G_1$ and $G_3$ are replaced by $\overline{k}_2$ branches. It is noted that all branches in $G_3$ are included in $G_1$ or $G_2$, so there will be no $\overline{k}_3$ branches existing. Therefore, branches $\overline{k}_1$ and $\overline{k}_2$ are decoupled due to the freedom given by $G_3$, and hereby $G$, $G_2$ and $G_3$ are combined into a switching flow graph $G$ as shown in Fig. 8. By repplacing the switching branches Fig. 8 with their models presented in Fig. 3, the steady-state and the large-signal model for the dual-input boost converter are derived as given in Fig. 9 and Fig. 10, respectively. The dc open-loop gains can be directly read from the steady-state model,

$$\frac{V_o}{V_{g1}} = n\cdot\frac{1}{1-D_{L1}}. \tag{6}$$

$$\frac{V_o}{V_{g2}} = n\cdot\frac{1}{1-D_{L2}}. \tag{7}$$

$$I_o = \frac{1-D_{L1}}{n}\cdot I_{L1} + \frac{1-D_{L2}}{n}\cdot I_{L2}. \tag{8}$$

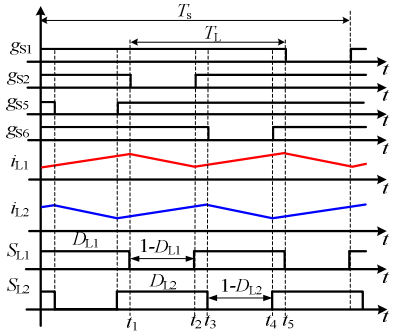



Figure 4. Timing diagrams and basic waveforms of proposed converter.

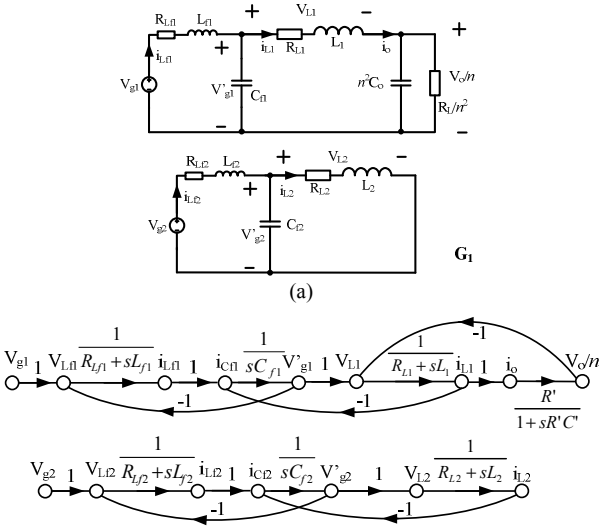



Figure 5. (a) The equivelant circuits during $t_1<t<t_2$, (b) the corresponsing flow graphs.

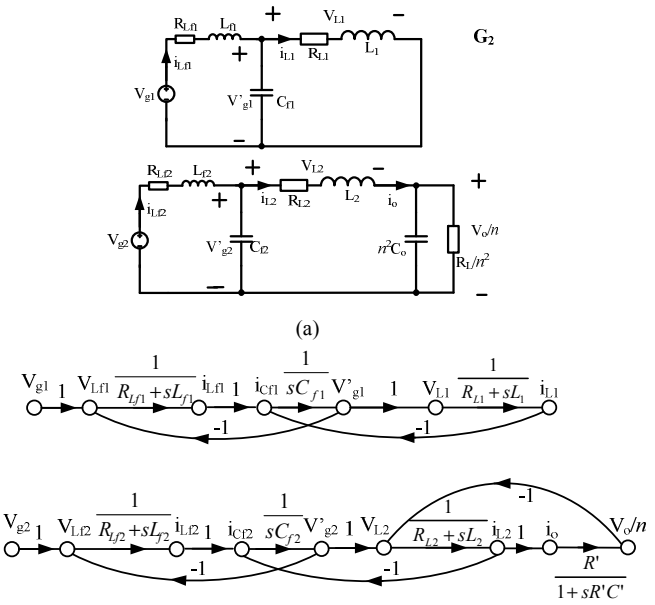



Figure 6. (a) The equivelant circuits during $t_3<t<t_4$, (b) the corresponsing flow graphs.

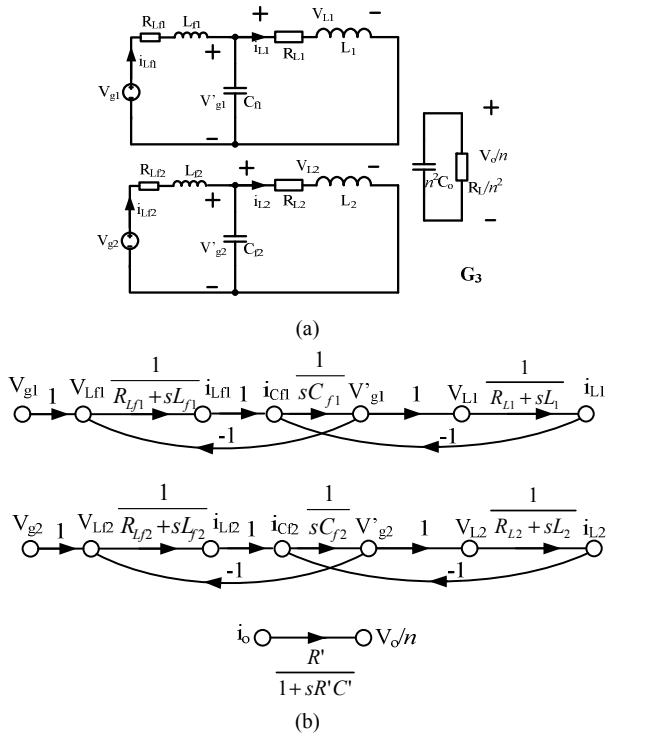



Figure 7. (a) The equivelant circuits during $t_2<t<t_3$ and $t_4<t<t_5$, (b) the corresponsing flow graphs.

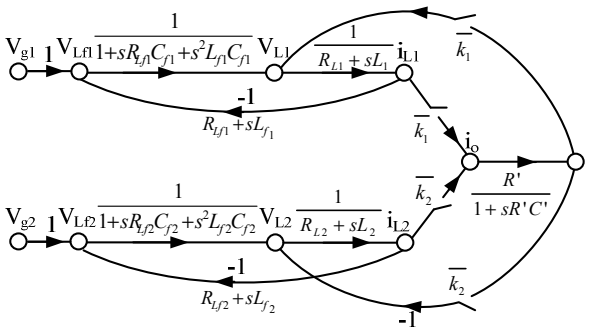


Figure 8. The switching flow graph.

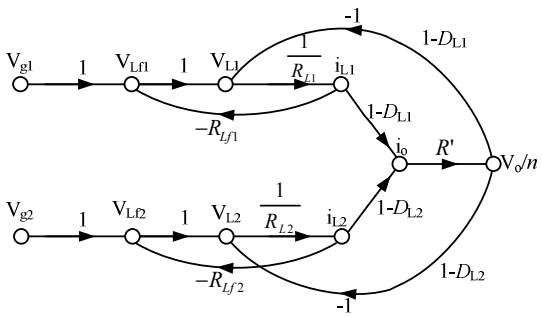


Figure 9. The steady-state model.

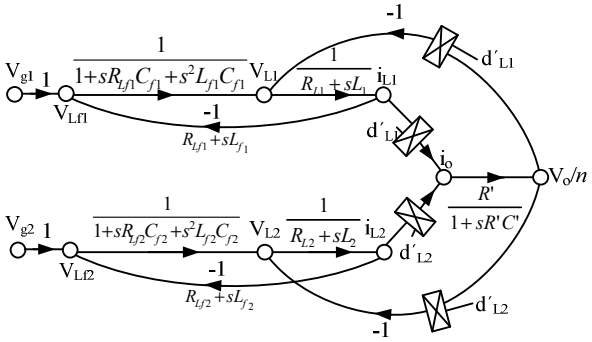


Figure 10. The large-signal (LS) model.

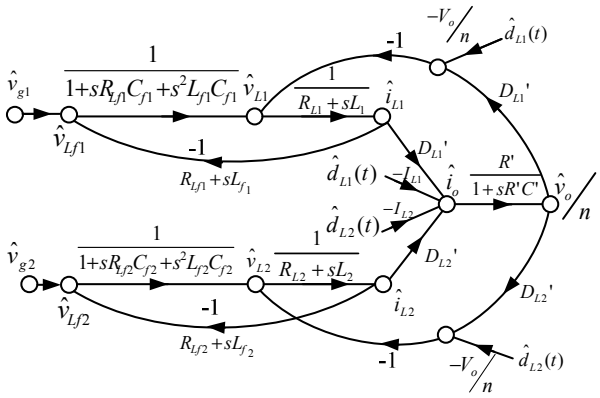


Figure 11. The small-signal (SS) model.

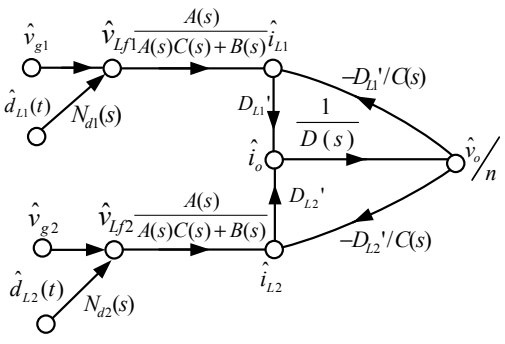


Figure 12. The simplified and reshaped small-signal (SS) model.

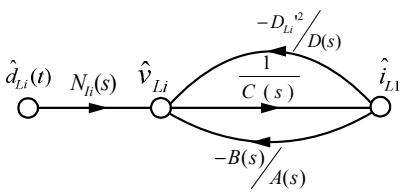
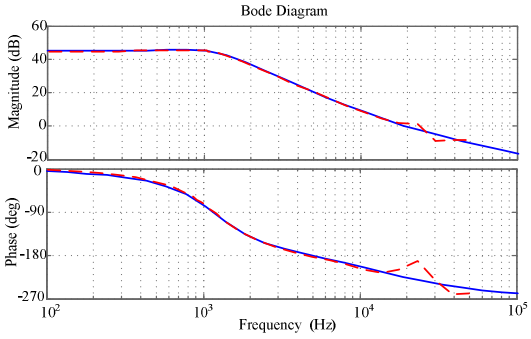
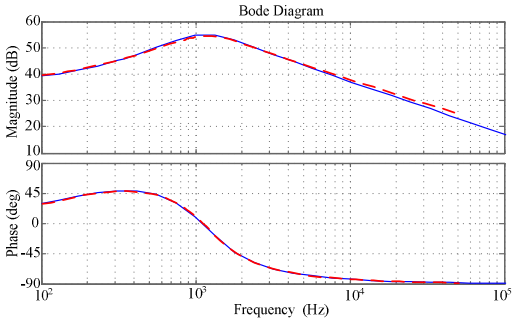


Figure 13. Reshaped flow graph for control-to-inductor current transfer funciton.




(a)




(b)

Figure 14. Bode diagrams of open-loop gain: (a) control-to-output, (b) control-to-inductor current.

From the SFG depicted in Fig. 8 and the small-signal models of the switching branches shown in Fig. 3 (c), the small-signal model of the converter is derived in Fig. 11. From the SS model, the relations between different state variables, such as the two input voltages to the output voltage or current, two control variables, $d_1$ and $d_2$, to the inductor currents, can be demonstrated clearly. Moreover, the SS model can easily give the transfer functions from one arbitrary state variable to another arbitrary state variable, such as input-to-output gain, the control-to-output gain, the input and output impedances etc.

### C. Open-Loop Transfer Functions

Move all the control branches to one node and reshape the SFG, and thereby a simplified flow-graph can be depicted in Fig. 12. As for the proposed dual-input boost converter with input filter and considering the two parasitic resistances, the input-to-output transfer function and the control-to-output transfer function can be obtained from Fig. 12, as:

$$G_{vg}(s) = \frac{\hat{v}_o(s)}{\hat{v}_g(s)} = \frac{1}{N_i(s)} \tag{9}$$

$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{N_{di}(s)}{N_i(s)} \tag{10}$$

where

$$N_i(s) = \frac{A(s)C(s)D(s)}{D_{Li}^{'}} + \frac{B(s)D(s)}{D_{Li}^{'}} + D_{Li}^{'}A(s)$$

$$N_{di}(s) = [V_o^{'} - \frac{I_{Li}}{D_{Li}^{'}} \cdot C(s)] \cdot A(s)$$

$$A(s) = \left(1 + sR_{Lfi}C_{fi} + s^2L_{fi}C_{fi}\right)$$

$$B(s) = \left(R_{Lfi} + sL_{fi}\right)$$

$$C(s) = (R_{Li} + sL_i)$$

$$D(s) = {}^{1}/_{R'} + sC'$$

$$i = 1,2$$

Move all the control branches to one node through the forward path, and then the control-to-inductor current transfer function can be demonstrated in a reshaped SFG shown in Fig. 13.

$$G_{id}(s) = \frac{\hat{\imath}_L(s)}{\hat{d}(s)} = \frac{A(s)D(s)N_{Ii}(s)}{D_{Li}^{'}} \cdot \frac{1}{N_i(s)} \tag{11}$$

where

$$N_{Ii}(s) = V_o^{'} + D_{Li}^{'}\frac{I_{Li}}{D(s)}$$

Suppose that we are given the following values: $V_g$=50V, $V_o$=400V, $L_{fi}$=0, $R_{Lfi}$=10$m\Omega$ (can be seen as the equivalent series resistance of power supplies) and $R_L$=160Ω, and thereby Bode diagrams of the open loop transfer functions of the converter can be plotted in Fig. 14. In order to verify the derived theoretical results, the converter circuit with completely same parameters is also simulated by PLECS, and the dashed lines of Fig. 14 show the simulation results based upon an AC sweep analysis. It can be seen that the calculation results and the circuit simulation results are matched very well.

## III. Designing the Closed-Loop Controllers

The above derived converter model has been used for controller design and simulation. In the steady state, the duty cycle of two input bridges is only given by (6) and (7). However, if each power source for the input-stage circuit has to supply specified power, $I_{L1}$ can be set differently from $I_{L2}$ based on the on different load conditions. Here, we assume that two different types of power sources are used as inputs, and one has higher energy density, such as battery (BAT) and fuel cells (FCs), and other one presents higher power density, such as super-capacitor (SC) bank. The SC bank delivers the difference between the current required by the load and the current supplied by BAT or FCs system in order to satisfy both efficiency and load dynamic specifications. So the respective current control target can be achieved by the action of feedback controller during the transient period. Current loop with PI type regulator is chosen for $V_{g1}$ which has the high energy density to directly control source current. The current reference is calculated with voltage of $V_{g1}$ and the required load power. The power stage of $V_{g2}$ is devoted to dc output voltage control, and thus the dual loop control configuration [15], [16], e.g. inner current loop and outer voltage loop, is employed, as shown in Fig. 15. According to the different dynamics of the power sources, the different control loop bandwidths can be determined as: the bandwidth of power control loop of $V_{g1}$ should be much lower than that of voltage control loop. As shown in Fig. 15, control system contains the voltage loop regulator, $H_v$(s), current-loop regulator, $H_i$(s), power regulator $H_p$(s), sampling delay, and the control-to-output transfer functions. In this case, the PWM period and ADC sampling period are equal. The ADC conversion is triggered at middle of the switching period and the end of ADC conversion triggers the execution of controller block, so the time delay is $T_s$/2 [17]. Considering the first-order Pade approximation, a rational, continuous time transfer function can be expressed as:

$$e^{-s\frac{T_S}{2}} \cong \frac{1-s\frac{T_S}{4}}{1+s\frac{T_S}{4}} \tag{12}$$

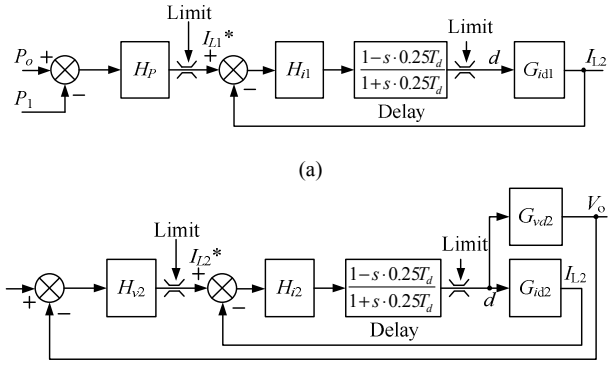



Figure 15. Control configuration (a) current loop control for $V_{g1}$, (b) dual loop control for $V_{g2}$

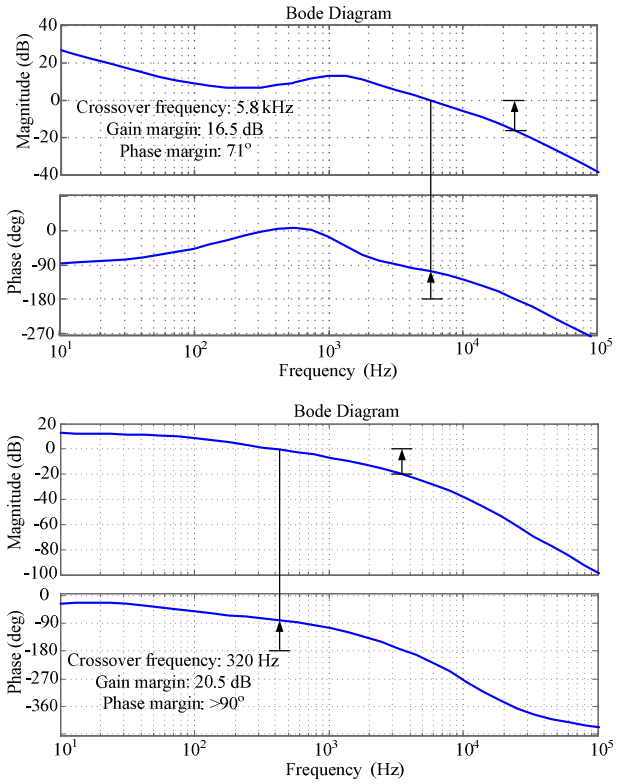



Figure 16. Bode plots of loop gain: (a) current loop gian, (b) voltage loop gian.

The loop gains for inner current $T_i$ and outer voltage loop $T_v$ can be expressed as

$$T_i(s) = H_i(s)G_{id}(s)\frac{1 - s \cdot 0.25T_d}{1 + s \cdot 0.25T_d} \tag{13}$$

$$T_v(s) = H_i(s)H_v(s)G_{vd}(s)\frac{1 - s \cdot 0.25T_d}{(1 + T_i(s)(1 + s \cdot 0.25T_d))} \tag{14}$$

where $T_{sm}$ is analogue-to-digital (ADC) sampling period .

A one-zero two-pole PI compensator is employed for both current-loop and voltage-loop here.

$$H(s) = K\frac{\frac{s}{\omega_z} + 1}{s(\frac{s}{\omega_p} + 1)} \tag{15}$$

The gain is selected for the appropriate cross-over frequency. The pole at the origin is used to eliminate the steady-state error. The pole at $\omega_p$ is placed at a high frequency to reduce the effect caused by parasitic resistance of the converter. The zero can be placed at the frequency below the resonant frequency of power stage to damp the overshoot. To ensure sufficient stability margin, the real zero and pole of the compensators are determined to make the loop have a gain margin and a phase margin more than 10 dB and 60°, respectively. Insertion of (10) and (11) into (13) and (14) with the input voltage of 50V and the output power of 2$k$W, obtains the parameters of the compensators which can be read from (16).

$$H_i(s) = 18 \cdot \frac{1 + 0.00043s}{s \cdot (1 + 0.0000073s)}$$
$$H_v(s) = 39.25 \cdot \frac{1 + 0.045}{s \cdot (1 + 0.000055s)} \tag{16}$$

Fig. 16 shows the Bode plots of current loop and voltage loop gain. The plots indicate that the current loop gain has a crossover frequency as high as 5.8 $k$Hz, with a phase margin of 71°. To avoid interaction between the sub-systems, a low control bandwidth is used for voltage loop. The resulting outer voltage loop has a crossover frequency of 320 Hz and a phase margin of larger than 90°. It is worth noting that the inherent dynamics of the input energy sources must be considered when one chooses the proper voltage loop bandwidth. Hereby, the bandwidth of power management loop in Fig. 15 (a) can be chosen as 30~40 Hz. The control requirements are satisfied.

After the regulator parameters are determined, convert those compensators from continuous time domain to discrete time domain and then they can be implemented in digital signal processer (DSP) to control the converter.

## IV. Experiment

In order to verify the theoretical analysis, a laboratory prototype of the proposed dual-input isolated full-bridge dc-dc converter with 4 individual transformers, shown in Fig. 17, is implemented and tested. The specifications and component details of the prototype are given in Table I. In the prototype, IRS2110 is used in the gate driver circuit together with ISO722C capacitive digital isolators for control signal protection. A TMS320F2808 eZdsp is used as the digital controller.

TABLE I. Specifications and Components of the Progotype

| | |
|---|---|
| Rated input voltage, $V_1$ and $V_2$ | 30-60 VDC |
| Rated output voltage, $V_o$ | 400 VDC |
| Rated output power, $P_o$ | 2 $k$W |
| Switching frequency, $f_s$ | 50 $k$Hz |
| Boost inductors, $L_1$ and $L_2$ | 22 $\mu$H, N87 core, copper foil winding<br>Parasitic resistance, 150 $m\Omega$@100$k$Hz |
| Input filter, $C_{f1}$ and $C_{f2}$ | 10 $\mu$F/250V Film Cap: 2 in parallel |
| Output filter, $C_1$ and $C_2$ | 6.8 $\mu$F/250V Film Cap: 4 in parallel |
| MOSFETs, $S_1$-$S_8$ | IRFP4568, 150V/171A |
| Diodes, $D_1$-$D_8$ | HFA15TB60, 600V/15A |

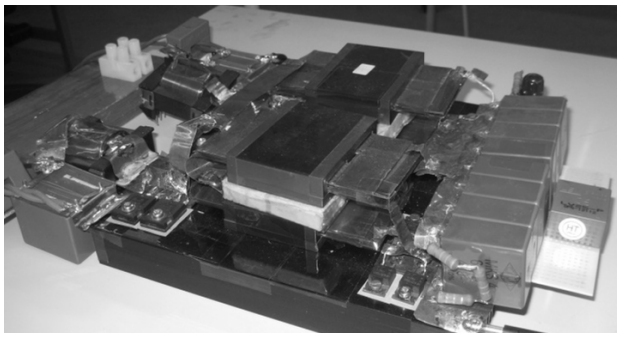


Figure 17. The photograph of the laboratory prototype.

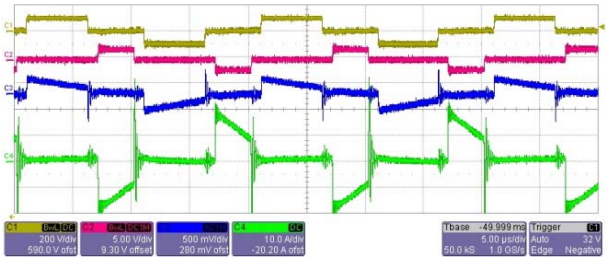


Figure 18. Experimental waveforms of the trasformer primary side voltages and currents, Ch1: $v_{ab}$ [200 V/div], Ch2: $v_{ab}$ [250 V/div], Ch3: $i_{p1}$ [10 A/div], Ch4: $i_{p2}$ [10 A/div]. (Time base: 5 $\mu$S/div)

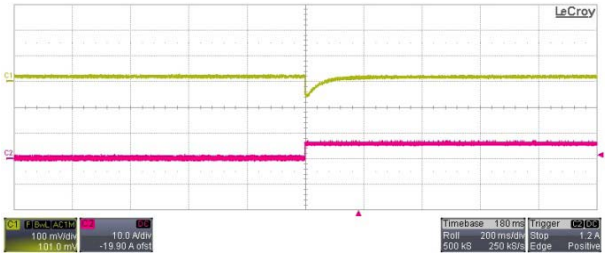


Figure 19. Experimental waveforms of the step load, Ch1: ouput volage $v_o$ [AC coupling, 50 V/div], Ch2: load current $i_o$ [10 A/div]. (Time base: 200 $m$S/div)

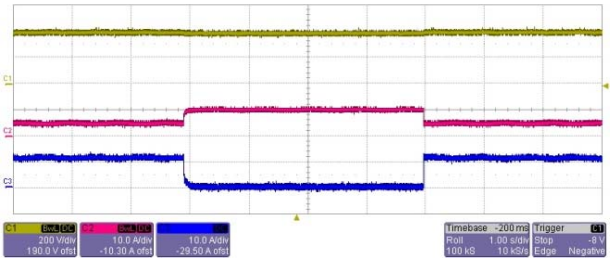


Figure 20. Transient response with respect to the input current disturbances under conditions: $V_{g1}$=50V, $V_{g2}$=30V. Ch1: ouput volage $v_o$ [200 V/div], Ch2: $i_{g1}$ [10 A/div], Ch3: $i_{g1}$ [10 A/div]. (Time base: 1s/div)

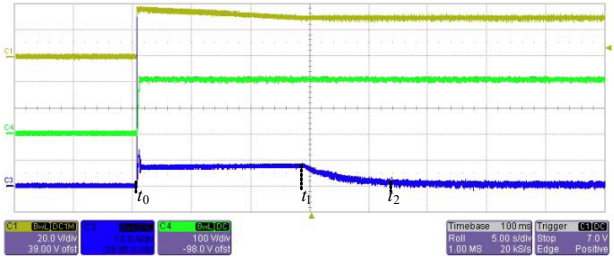
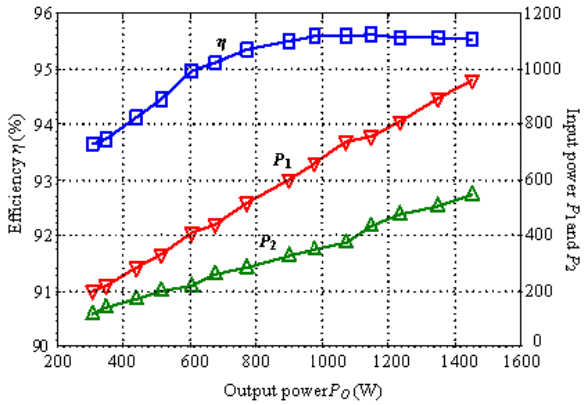
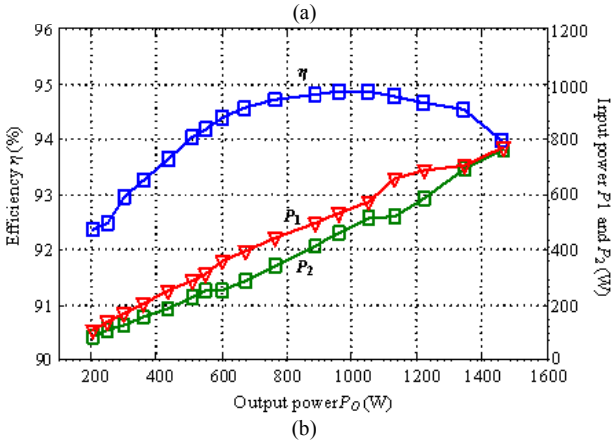



Figure 21. Transient response, Ch1: $v_{g2}$ [20 V/div], Ch3: $i_{g2}$ [10 A/div], Ch4: ouput volage $v_o$ [100 V/div]. (Time base: 5s/div)

Fig. 18 shows the experimental waveforms of the voltages $v_{ab}$ and $v_{cd}$ as well as the currents $i_{p1}$ and $i_{p2}$ on the primary side of transformers, as denoted in Fig. 2 under the dual-input mode with input voltages of 50 V and 30 V.




(a)




(b)

Figure 22. The measureed efficiency curves, (a) $V_1$=50V, $V_2$=30V and $P_1 \neq P_2$; and (b) $V_1$=$V_2$=30 V and $P_1 \approx P_2$.

Fig. 19 shows experimental results of load step with both input voltages of 40V and output voltage of 380V. The voltage drop is about 30 V or 7.9 % of the bus voltage during 90% load step (from 0.18 $k$W to 1.8 $k$W). The transient period is about 100 $m$s.

To verify the aforementioned power management strategy, Fig. 20 shows the output voltage response to transients of the two input currents, $i_{g1}$ and $i_{g2}$, with a constant output power. It can be seen that the converter can draw the power from the two input sources simultaneously or separately, and with the designed control strategy, it can be controlled and switched between the two operating modes flexibly. A small super-capacitor bank (60V/14.6F) is used as input source $V_{g2}$ and then the experimental waveforms can be obtained and present in Fig. 21. At $t_0$, the converter starts and $i_{refl}$ is 0, which is to simulate the warm-up stage of the primary power source $V_{g1}$, so converter operates under single-input mode. The required load power is provided by super-capacitor bank and output voltage keeps constant; after $t_1$, $i_{refl}$ is given according to voltage of $V_{g1}$ and the required output power, and thereby $i_{g2}$ starts to reduce until it reaches zero at $t_2$.

Under the dual-input mode, the efficiency of this dual-input power conversion system can be defined as:

$$\eta = \frac{P_o}{P_1 + P_2} \times 100\%$$

In order to measure the efficiency of the converter precisely, two EA-PS 9060-48 dc power supplies, high power rheostat, HP33401A multimeters and non-inductive

current shunts are used. Without including the gate driver losses, the measured efficiencies are plotted in Fig. 22. Fig. 22 (a) shows the efficiency curve with input voltages of 30V and 50V, and different input powers, while Fig. 18(a) presents the efficiency curve when both of the input voltages are 30V and two input power are approximately same. The maximum efficiency is measured as 95.7%.

## V. CONCLUSION

This paper analyzes and derives the model of the dual input isolated full-bridge boost converter by the SFG modeling technique. The small-signal SFG can generate analytical transfer functions easily, which can be used in practice effectively for various applications. A DSP-based digital controller for a 2 *k*W converter is presented in this paper. A dual-loop average current mode control method is employed to achieve the fast transient response. Simulation and experiment results verify the validity of the modeling and controller design for the proposed dual input boost converter.

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