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# Experimental Investigation of Digital Compensation of DGD for 112 Gb/s PDM-QPSK Clock Recovery

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**Abstract:** For the first time, the impact of DGD on clock recovery for 112Gb/s PDM-QPSK is experimentally investigated and quantified. We propose and experimentally demonstrate novel digital adaptive timing error detector which is robust to DGD

**OCIS codes:** (060.1660) Coherent communications; (060.2330) Fibre optics communication

## 1. Introduction

Coherent detection supported by digital signal processing is considered to be a key enabling technology to support spectrally efficient modulation formats. An essential part of the digital signal processing demodulation algorithms is a digital clock recovery module [1-5]. It has been shown that that the combined effects of polarization rotation and differential group delay (DGD) can significantly affect the performance of the timing error detector gain of the clock recovery leading to system outage [2-5]. Even though the mentioned problem is very relevant for the design of digital coherent receivers reported solutions to this particular problem have been sparse [4-5]. Additionally, most of the work reported so far on this topic have relied on numerical simulations [2-5].

In this paper, the impact of DGD in the presence of polarization rotation on the performance of digital clock recovery is experimentally investigated and quantified for polarization multiplexed 112 Gb/s QPSK system. In general, our experimental work confirms the investigations based on numerical simulations. Compared to the numerical simulations results, the experimental findings are more pessimistic as they indicate that even for relatively moderate values of DGD digital clock recovery may fail, pointing out the importance of compensating for DGD. Additionally, we present and experimentally demonstrate a novel adaptive timing error detector algorithm whose performance is independent of the value of polarization rotation angle and DGD. Compared to the solution presented in [5], our approach is simpler because only a single adaptation loop is needed; i.e. only a single update algorithm is used to properly restore timing detector gain.

## 2. Experimental set-up

The outline of the experimental set-up for the investigation of the impact of the DGD and its compensation, for 112 Gb/s PDM-QPSK system is shown in Fig. 1. The DSP block contains only the clock recovery module as it is the main focus of this paper, see Fig. 1(b).

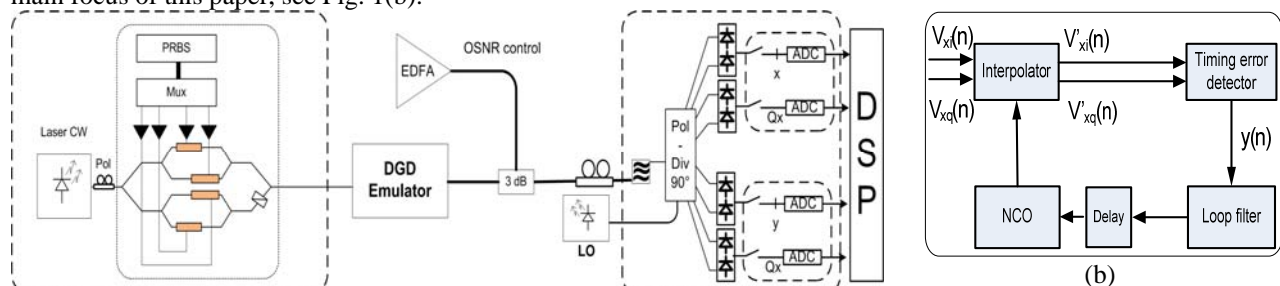


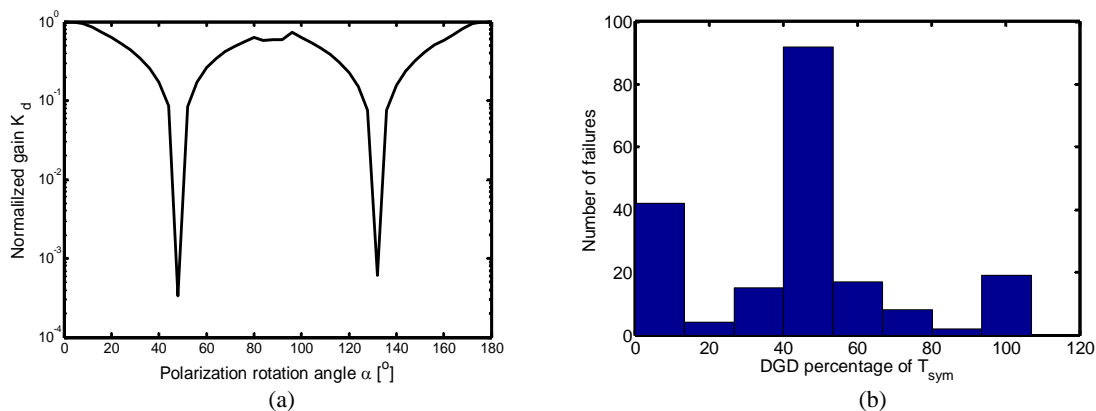
Fig 1. (a) General outline of the experimental set-up for 112 Gb/s PDM-QPSK system, (b) Clock recovery and interpolation module

At the transmitter, the electrical input binary data stream is parallelized into four binary tributaries which are used to drive two nested Mach-Zehnder Modulators (MZM) for QPSK modulation, each for one polarization, i.e. x and y. The nested MZMs are modulated by 28 Gb/s data streams. Using a polarization beam splitter (PBS), the -x and -y polarization components are combined to form a polarization multiplexed data signal. The optical 112 Gb/s PDM-QPSK data signal is then applied to a DGD emulator for which the mean value of the DGD can be specified. We vary the DGD from 0 to 38.20 ps. Throughout the whole experiment, an OSNR of 20 dB is kept constant. In order to detect the 112 Gb/s PDM-QPSK signal, a polarization-diversity coherent receiver is used; see Fig. 1(a). At the receiver, the two orthogonal polarizations are mixed with the local oscillator laser in two 90° optical hybrids,

detected with four pairs of balanced photodiodes and then sampled at 80 GS/s. The sampled data,  $V_{xi}(n)$ ,  $V_{xq}(n)$ ,  $V_{yi}(n)$  and  $V_{yq}(n)$ , are then sent to the DSP block which only contains the clock recover module in this particular case. In this paper, for simplicity, we only consider the x-polarization clock recovery and interpolation module. However, the results obtained for the x-polarization module are also applicable to the y-polarization. Following Fig. 1(b), the signal samples from the analogue-to-digital converter (ADC),  $V_{xi}(n)$  and  $V_{xq}(n)$ , are applied to the interpolator, which then computes the correct data signal samples using an appropriate control signal. The feedback loop controlling the interpolator consists of the Gardner timing error detector, a loop filter and a numerically controlled oscillator (NCO). The Gardner timing error detector is used to produce the error signal for the control of the loop. The timing error detector is one of most crucial part of the clock recovery and its performance can be characterized by the timing error detector gain,  $K_d$ . The  $K_d$  can be computed by applying the signals  $V_{xi}$  and  $V_{xq}$  to the timing error detector module and computing the magnitude of the DC component present at the output.

### 3. Results

In Fig. 2(a), the normalized timing error detector gain,  $K_d$ , is plotted as a function of polarization rotation angle,  $\alpha$ , for a DGD of 50% of the symbol rate,  $T_{sym}$ , for the obtained experimental data.



**Fig. 2:** (a) Normalized timing error detector gain,  $K_d$ , as a function of polarization rotation angle for the DGD of  $0.5T_{sym}$ . (b) Histogram depicting the number of failures as the DGD is varied from 0 to 107% of  $T_{sym}$

It is observed in Fig. 2(a), that as the polarization rotation angle  $\alpha$  approaches  $45^\circ$ , the timing error detector gain drops by the several orders of magnitude, and this means that the clock recovery loop will not be able to obtain a lock. This is in accordance with the simulation results presented in [2-3]. In general, the timing error detector gain will drop every  $45^\circ + p90^\circ$ , where  $p$  is an integer. The next value for which the timing error detector gain approaches zero is  $135^\circ$ , as shown in Fig. 2(a). According to Fig. 2(a), the normalized timing error detector gain is unaffected for  $\alpha=0$  and  $90^\circ$ , because for those two cases the -x and -y signal polarization components will not mix.

In order to quantify the impact of the DGD on the performance of the timing error detector, and thereby the clock recovery module, a histogram has been constructed in Fig. 2(b). The histogram depicts the number of failures for the experimentally obtained data as the DGD has been varied from 0 until 107% of  $T_{sym}$ . In order to construct the histogram, we had access to 200 traces in total. The failure is defined as the occurrence when the normalized  $K_d$  has dropped more than 15 dB when the polarization rotation angle is in the range from 0 to  $90^\circ$ . The reason why we defined a 15 dB as the limit is because as shown in [2], if the timing error detector gain is dropped more than 15 dB, the clock recovery will not be able to satisfy the jitter tolerance curve. As expected, the largest number of failures occurs when the DGD is in the range from 40 to 50% of  $T_{sym}$ . Additionally, Fig. 2(b) shows that even though for relatively moderate values of the specified DGD, a certain number of failures will occur.

In general, the Gardner timing error detector algorithm works fine as long as the input to the timing error detector does not contain contribution from both horizontal (-x) and vertical (-y) optical data signal components. In order to mitigate the effects of DGD, the idea would therefore be to re-use the Gardner timing error detector algorithm, however, with some adaptive modification, so that it is only the data associated with a single polarization component of the optical signal that enters the Gardner timing error detector. Therefore, if the rotation angle  $\alpha$  is known then we could use it to revert the polarization rotation digitally and assure that only data associated with a single polarization enters the Gardner timing error. A novel adaptive timing error timing detector structure which estimates rotation angle and performs digital polarization rotation, in combination with the Gardner timing error detector, is shown in

Fig. 3(a). We use (sign) gradient algorithm to estimate the polarization angle  $\alpha$ . An important part of the structure is a digital low-pass filter  $W(z)$  which is used to stabilize the loop and provide sufficient loop bandwidth. For the particular case shown in Fig. 3(a), the adaptive timing error detector works on signal components  $V_{xi}$  and  $V_{yi}$ . The similar structure can be employed to work on signal components  $V_{xq}$  and  $V_{yq}$ . However, in order to demonstrate the working principle of the scheme we concentrate on  $V_{xi}$  and  $V_{yi}$  signal components only.

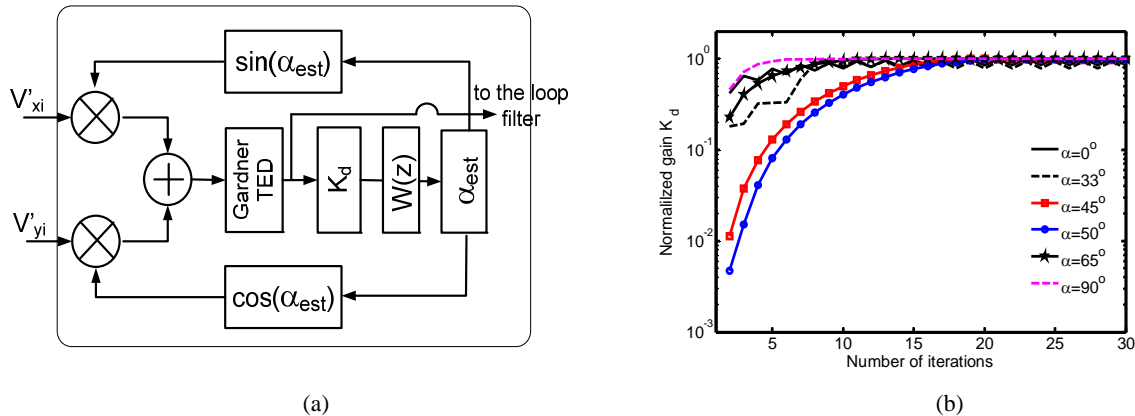


Fig. 3. (a) A novel adaptive timing error detector scheme. (b) Normalized Gardner timing error detector gain,  $K_d$ , as a function of number of iterations for polarization rotation angle ranging from 0 to  $90^\circ$  after applying the adaptive structure in Fig.4. The DGD is 50% of  $T_{sym}$

In Fig. 3(b), the normalized Gardner timing error detector gain  $K_d$  is plotted as a function of a number of iterations after applying the novel adaptive timing error detector structure for the selected values of polarization rotation angle of the experimental data. The polarization angle is varied from 0 to  $90^\circ$  and the DGD is fixed at 50% of  $T_{sym}$ , which is the worst case. It can be observed in Fig. 3(b), that the scheme converges and the normalized timing error detector gain  $K_d$  approaches 1 irrespective of the considered value of polarization rotation angle. This means that the output of the Gardner timing error detector can now be used to control the rest of the clock recovery and interpolation loop shown in Fig. 2(b). The speed of convergence is relatively fast as only app. 16 or less, iterations are needed. The presented scheme can be used for any type of timing error detector and thereby easily expanded to 16-QAM.

#### 4. Conclusion

Experimental investigations of the impact of the DGD on the timing error detector for 112 Gb/s PDM-QPSK system have been presented. We have shown that even for the moderate values of DGD a timing error detector gain can be significantly decreased leading to the failure of the clock recovery. A novel adaptive timing error detector scheme has therefore been proposed and successful experimental demonstration has been confirmed. We have shown that after applying the adaptive timing error detector structure, the output of the Gardner timing error detector remains unchanged irrespective of the polarization rotation angle and the DGD.

#### 5. Acknowledgement

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