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Comparison of Current Balancing Configurations for Primary Parallel Isolated Boost Converter

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***Abstract*— Different current balancing configurations have been investigated for Primary Parallel Isolated Boost Converter (PPIBC). It has been shown that parallel branch current balancing is possible with several configurations of coupled/uncoupled inductors. Analytical expressions for branch currents have been derived for different cases of gate signal mismatch causing current imbalance. It has been observed that turn-on and turn-off delays in parallel power stages of the PPIBC have different effects in the branch currents deviating from ideal. It has also been observed that in some configurations inductance differences due to core tolerances play an important role in current imbalance. Analytical and simulation results have shown that another side effect of the gate signal delay and inductor value difference is additional voltage stress over the switches during the mismatch times. Advantages of each configuration in terms of effective current balancing, efficiency and manufacturing simplicity have been highlighted. Simulations with ideal components for each case have been carried out to confirm the analytical derivations. Experimental results have also been included to show the performances of different configurations where component non-idealities like transformer leakage inductances also become effective.**

I. INTRODUCTION

Primary Parallel Isolated Boost Converter (PPIBC) is a high efficient topology for high input current, step up applications [1]. The effectiveness of the topology is coming from the unique parallel power stage structure in the input side where the voltage is low and the current is high. The primary side switches of each parallel power stage operate synchronously with the corresponding switches in the other parallel power stages. However due to propagation delays and rise-fall time differences of the ICs as well as component tolerances in the gate drive circuitry like gate resistances result in switching delays. These delays not only cause the branch current values to deviate but also switch voltage over-stress conditions to occur which may increase the switching losses.

Although various configurations have been claimed in the patent [2], only one of them, current balancing transformer (CBT), has been implemented so far for proof of concept. Recently integrated magnetic solutions have been proposed for this topology [3] and [4]. Deviations from ideal current waveforms in parallel branches have been reported in [5]. Similar effects can be observed if two separate inductors (TSI) or partially coupled inductors (PCI) are used. In this paper these configurations have been analytically investigated. Expressions have been derived for branch current deviations which then compared to ideal circuit simulation as well as experimental results.

II. PRIMARY PARALLEL ISOLATED BOOST CONVERTER

Fig.1 shows PPIBC topology suitable for handling high input currents for fuel cell applications. The current is forced to be equal in both primary windings by the series secondary connection of the two transformers. Primary switches share the same control signals with the same phase switching sequence which allows a simple control. Output rectification unit as well as input and output filters are common to both primary stages.

The input inductor in Fig. 1 serves as an energy storage element for both primary power stages. As long as switches S1, S2, S3, S4 and S5, S6, S7, S8 work in the same pattern (Fig. 2a), the inductor current will be shared equally by the two full bridges. In case of a mismatch in switching, the CBT (effectively an inverse coupled inductor) in series with the input inductor shows high impedance in the differential path which limits the rate of change of the differential current (Fig. 2b).

III. CURRENT BALANCING CONFIGURATIONS

In order to simplify the analysis, the converter in Fig. 1 has been reduced to the circuit in Fig. 3a. This circuit will be used through out the paper except the coupled/uncoupled inductor combinations will replace the single inductor.

A. Single inductor:

Figs. 3b-e show possible configurations of the switches both in normal and extra operation modes. Here a switch being on is equal to all four switches being on (inductor charging state). Similarly a switch being off in Fig. 3a corresponds to two diagonal switches being on in Fig. 1 (discharging state).

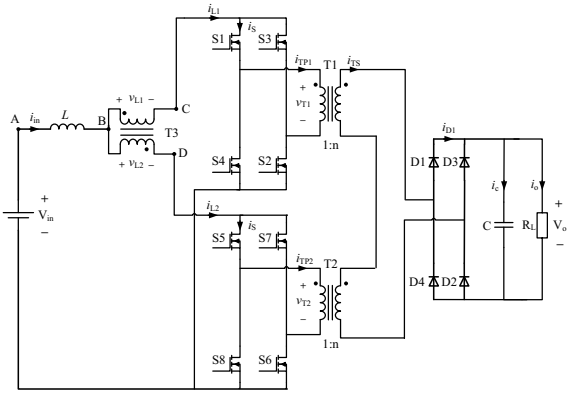


Fig. 1. PPIBC with coupled inductors for current balancing

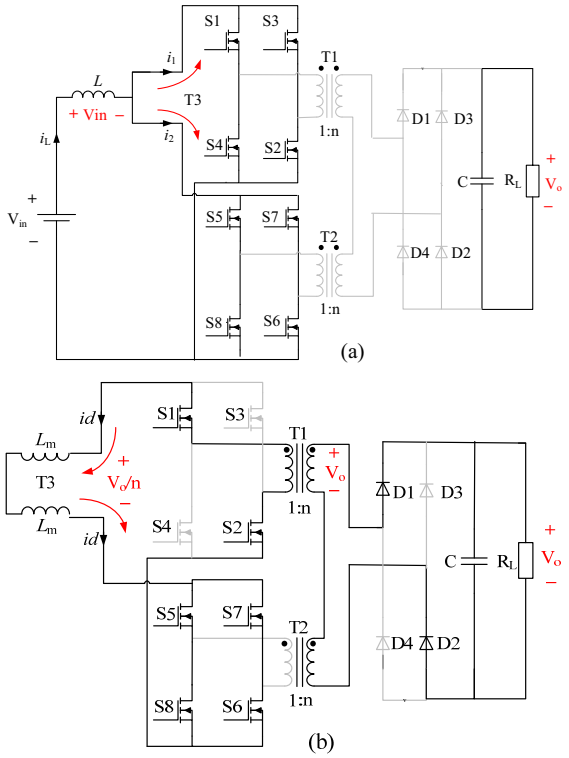
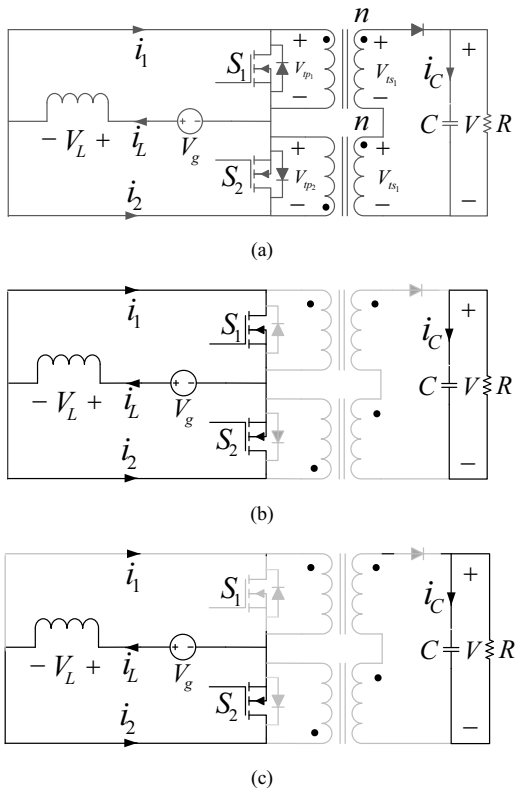


Fig. 2. (a) Forward current path in both branches during boosting (b) differential current path during gate signal mismatch

As can be observed from the branch current waveforms in Fig. 4, significant deviations occur from ideal situation at the times of turn off and turn on delays. All the input current is directed to the branch where the switch is on.



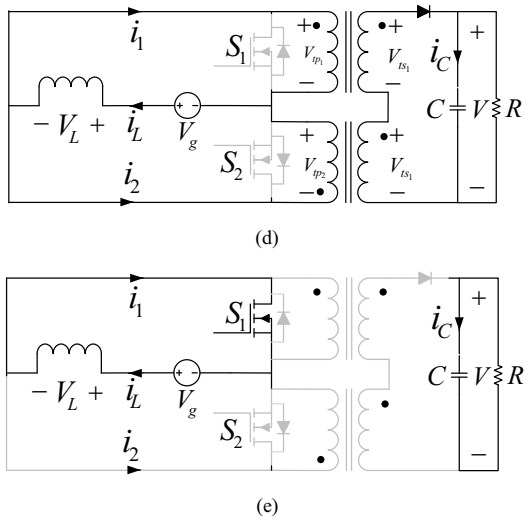


Fig. 3. (a) Simplified PPIBC with a single inductor (b) charging period (c) turn off delay in S_2 (d) discharging period (e) turn on delay in S_2 (inactive lines and components have been drawn light grey)

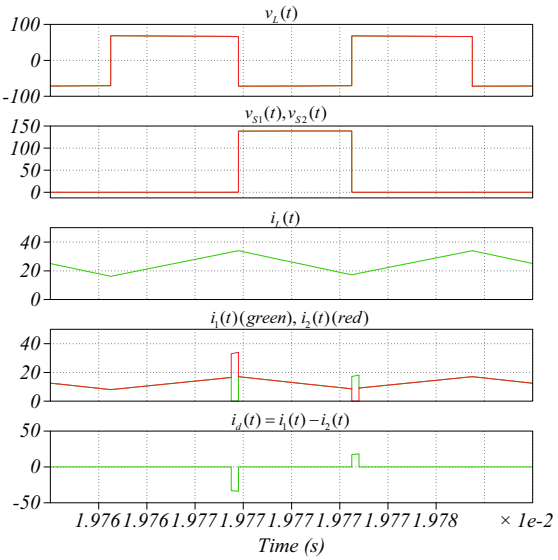


Fig. 4. Simulated waveforms of single inductor case

Relative switching delays also changes the steady state operating point of the converter by changing the effective duty cycle. Assuming that there is both a turn off and turn on delay in S_2, following expressions can be obtained:

$$(D+d_{off})(V_g)+(D'-d_{off})(V_g-V/(2n))=0 \quad (1)$$

$$V=\frac{2n}{D'-d_{off}}V_g \quad (2)$$

$$(D+d_{off})(-V/R)+(D'-d_{off})(I_L/(2n)-V/R)=0 \quad (3)$$

$$I_L=\frac{2n}{D'+d_{off}}\frac{V}{R} \quad (4)$$

Average branch current expressions can be derived from here:

$$I_1=I_L/2+K$$
$$I_2=I_L/2-K \quad (5)$$

where,

$$K = d_{on}[I_L - (D + d_{off} - d_{on})V_g/(2 f_{SW} L)]/2 - d_{off}[I_L + (D)V_g/(2 f_{SW} L)]/2 \quad (6)$$

In these equations, d_{on} and d_{off} represent the turn on and turn off delay, respectively. Similar situation occurs if two direct coupled inductors are used instead of a single inductor as seen in Fig. 5. This configuration has the same waveforms as in Fig. 4. Consequently both configurations have poor current balancing features.

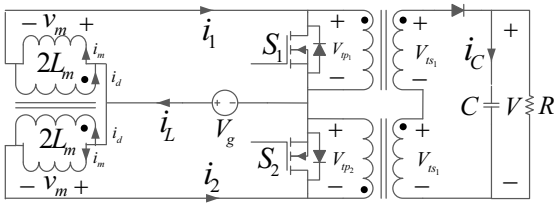
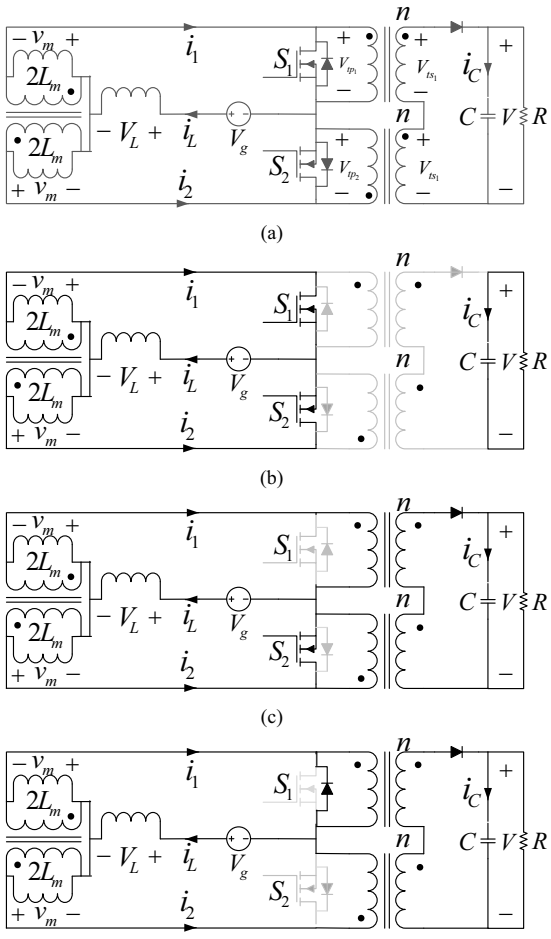


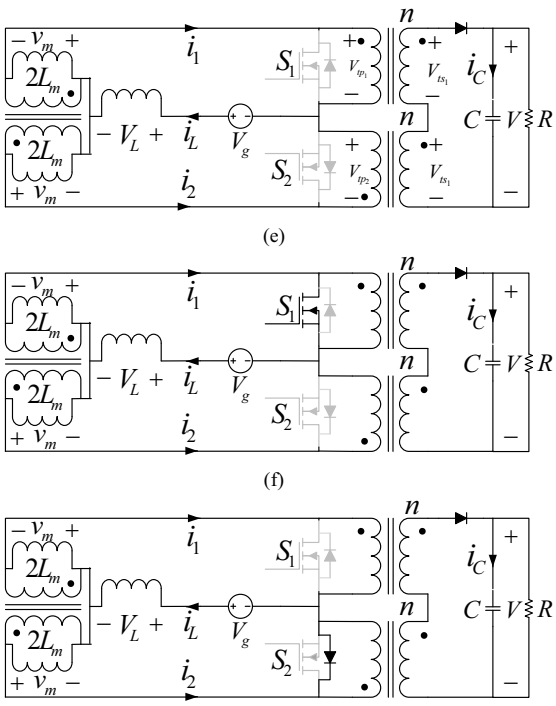
Fig. 5. Simplified PPIBC with two direct coupled inductors

B. Current balancing transformer (CBT):

A single inductor can be connected to two inverse coupled inductors acting as a CBT as shown in Fig. 6a. Figs. 6b-g show the possible operation modes. Fig. 7 shows the corresponding simulation results where switch S_2 has both a turn-off and turn-on delay.



(a) (b) (c) (d)



(e) (f) (g)

Fig. 6. (a) Simplified PPIBC with a CBT (b) charging period (c) turn off delay in S_2 (d) recovery period (e) discharging period (f) turn on delay in S_2 (g) second recovery period (body diode forced to be on)

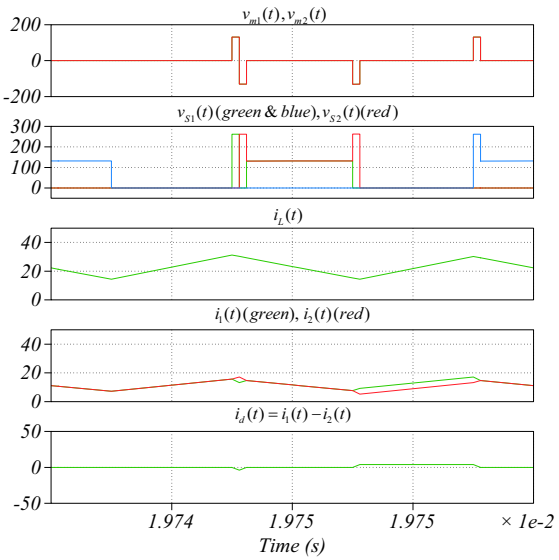


Fig. 7. Simulated waveforms of the converter with CBT

As can be observed from the branch currents after the charging period when the turn off delay occurs, i_2 (red) continues to rise where i_1 starts discharging. Following the turn-off delay period, recovery period starts where body diode of the non-delayed switch S_1 conducts the current difference between i_1 and i_2 until both currents are the same. After that the discharging period starts. Governing equations of the output voltage for this case can be obtained as follows:

$$D(V_g) + D'(V_g - V/(2n)) = 0 \quad (7)$$

$$V = \frac{2n}{D'} V_g \tag{8}$$

The average value of the inductor current can be derived using output capacitor charge balance as:

$$D(-V/R) + (D' - 2d_{off})(i_L(t)/(2n) - V/R) + (d_{off})[(< i_1(t) >_{d_{off}-S} + < i_2(t) >_{d_{off}-D})/n - 2V/R] = 0 \tag{9}$$

which can be reduced to:

$$V/R = D' I_L/(2n) + (d_{off})(< i_m(t) >_{d_{off}-S} - < i_m(t) >_{d_{off}-D})/n \tag{10}$$

In Eq. (10) $d_{off\text{-}S}$ represents the turn off delay of the switch and $d_{off\text{-}D}$ represents the recovery period. Also i_m represents the magnetizing current of the CBT which is effectively the difference current between the two branches. Turn-off delay and the corresponding recovery time are the same because the same amount of voltage drop occurs across the magnetizing inductance of the CBT during both periods. This results in the inductor current as:

$$V/R = D' I_L/(2n) \tag{11}$$

Using Eqs. (8)-(11), average branch current expressions can be derived as:

$$I_1 = I_L/2 + K$$
$$I_2 = I_L/2 - K \tag{12}$$

where,

$$K = < i_m(t) >_T = (D) < i_m(t) >_D + d_{off} < i_m(t) >_{d_{off}-S} + d_{off} < i_m(t) >_{d_{off}-D} + (D' - 2d_{off}) < i_m(t) >_{D'-2d_{off}} \tag{13}$$

Since,

$$< i_m(t) >_{d_{off}-S} = < i_m(t) >_{d_{off}-D} = -d_{off} V/(8n f_{SW} L_m) = -d_{off} V_g/(4D' f_{SW} L_m) \tag{14}$$

and,

$$< i_m(t) >_D = < i_m(t) >_{D'-2d_{off}} = 0 \tag{15}$$

The current difference can be written as in Eq. (16),

$$K = -d_{off}^2 V_g/(2D' f_{SW} L_m) \tag{16}$$

Effect of the turn-on delay is different from that of the turn-off delay. It can be observed from Fig. 7 that at the end of the discharging period a difference between i_1 and i_2 occurs due to the turn-on delay of S_2. This results in a longer time where the two branch currents have an offset. Turn-on delay changes the steady state operating point of the converter as in Eq. (17) and Eq. (18).

$$V = \frac{2n}{D' + d_{on}} V_g \tag{17}$$

$$V/R = (D' + d_{on}) I_L/(2n) \tag{18}$$

Similar to the turn-off case the difference current expression can be obtained as in Eq. (19).

$$K = D\, d_{on} V_g/(2 f_{SW} L_m (D' + d_{on})) \tag{19}$$

C. Two separate inductors (TSI)

Instead of the CBT method, each branch can have its own energy storage inductor separately as in Fig. 8. These inductors also act as impedances between the two full bridges limiting the rate of change of the difference current.

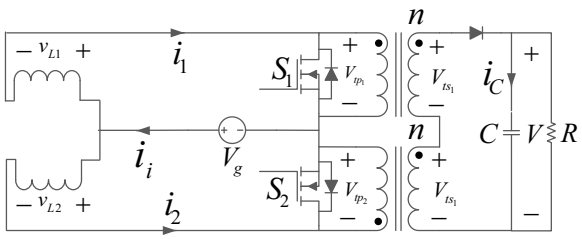


Fig. 8. Simplified PPIBC with a CBT

Normal and extra operation modes of the TSI configuration are the same as Fig. 6b-g. Similar to CBT case turn-off and turn-on delays have different current balancing effects where turn-on delay in switch S_2 produces an offset during the following charging period. Fig. 9 shows the related simulation results where maximum switch stress values appear to be the same as CBT which is two times the nominal voltage reflected through the transformer.

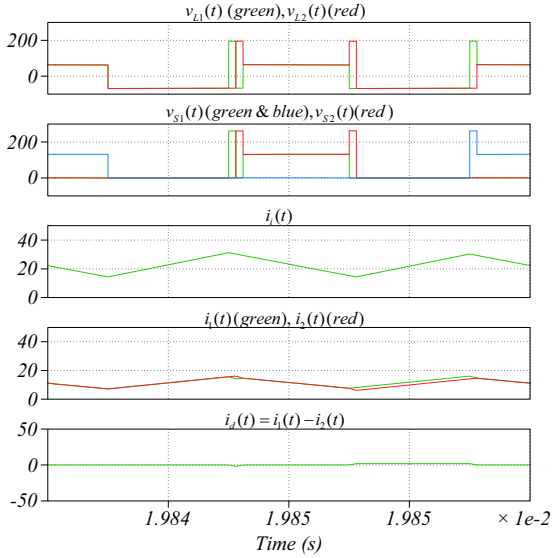


Fig. 9 Simulated waveforms of the converter with TSI

The average current difference between the two branches in TSI case can be derived as in CBT case. Based on Eq. (12) K can be obtain for turn-off and turn-on delays respectively as,

$$K = -d_{off}^2 V_g/(2D' f_{SW} L) \tag{20}$$

$$K = D\, d_{on} V_g/(2 f_{SW} L (D' + d_{on})) \tag{21}$$

D. *Partially coupled inductors (PCI)*

Similar to the previous two methods PCI provides impedance between the two full bridges to limit the rate of change of the difference current (i_d). PCI is composed of two direct coupled inductors with a low coupling factor. Fig. 10 shows simplified PPIBC with PCI acting as a current balancing mechanism. $2L_m$ represents the mutual inductance and 2Lm-2L represents the self (leakage) inductance of the coupled inductor. Possible switching configurations are the same as Fig. 6b-g. Fig. 11 shows the simulated waveforms which are similar to the previous two cases. Voltage drops over the mutual inductances can be observed to be different during the extra operation modes.

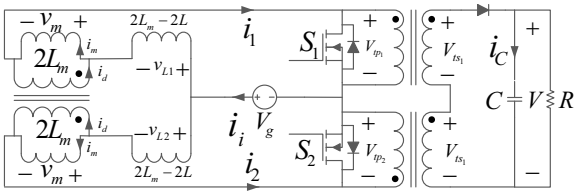


Fig. 10 Simulated waveforms of the converter with TSI

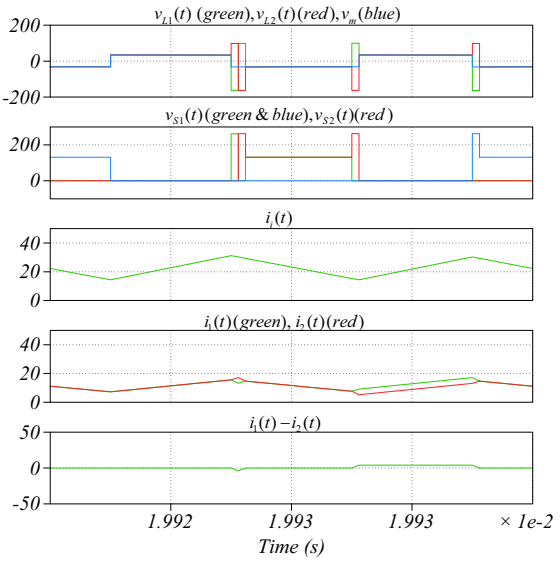


Fig. 11 Simulated waveforms of the converter with PCI

Similar to CBT and TSI case, average difference currents can be obtained analytically for the PCI case. Considering the switching positions in Figs. 6b-g applied to the simplified circuit in Fig. 10, following equations can be derived for a turn-off delayed switch S_2 operation:

$$(D)(L_m/L)(V_g) + (D')(L_m/L)(V_g - V/(2n)) = 0 \quad (22)$$

$$V = \frac{2n}{D'} V_g \quad (23)$$

The output current expression can be obtained as:

$$D(-V/R) + (D' - 2d_{off})(i_L(t)/(2n) - V/R) + (d_{off})[(< i_1(t) >_{d_{off-S}} + < i_2(t) >_{d_{off-D}})/n - 2V/R] = 0 \quad (24)$$

$$V/R = D' I_L/(2n) + (d_{off})(< i_d(t) >_{d_{off-S}} - < i_d(t) >_{d_{off-D}})/n \quad (25)$$

$$V/R = D' I_L/(2n) \quad (26)$$

From here it can be seen that turn-off delay in a switch does not affect the steady state operating point of the converter in PCI case similar to CBT and TSI cases. The average value of the difference current i_d can be calculated as the addition of average i_d values over charging, turn-off delay, recovery (body diode conduction) and discharging periods.

$$K = < i_d(t) >_T = (D) < i_d(t) >_D + d_{off} < i_d(t) >_{d_{off-S}} + d_{off} < i_d(t) >_{d_{off-D}} + (D' - 2d_{off}) < i_d(t) >_{D'-2d_{off}} \quad (27)$$

Since,

$$< i_d(t) >_D = < i_d(t) >_{D'-2d_{off}} = 0 \quad (28)$$

and the remaining periods can be calculated as:

$$< i_d(t) >_{d_{off-S}} = < i_{L1}(t) >_{d_{off-S}} - < i_m(t) >_{d_{off-S}} = \frac{d_{off}}{2f_{sw}}\left(\frac{1}{2L-2L_m}\right)\left(\frac{L-L_m}{L}V_g - \frac{2L-L_m}{2L}\frac{V}{n}\right) - \frac{d_{off}}{2f_{sw}}\left(\frac{1}{2L_m}\right)\left(\frac{L_m}{L}V_g - \frac{L_m}{2L}\frac{V}{n}\right) = -\frac{d_{off}}{8f_{sw}(L-L_m)}\frac{V}{n} = -d_{off}V_g/(4D' f_{SW}(L-L_m)) \quad (29)$$

As mentioned before turn-off delay ($d_{off\text{-}S}$) and recovery period ($d_{off\text{-}D}$) are equal. Based on Eqs. (12,28) and Eq. (29),

$$K = -d_{off}^2 V_g/(2D' f_{SW}(L-L_m)) \quad (30)$$

Again similar to CBT and TSI cases, turn-on delay affects the voltage and current conversion ratios given as in Eqs. (17,18). Turn-on delay average current expression is,

$$K = < i_d(t) >_T = d_{on} < i_d(t) >_{d_{on-S}} + (D - d_{on}) < i_d(t) >_{D-d_{on}} + d_{on} < i_d(t) >_{d_{on-D}} + (D' - d_{on}) < i_d(t) >_{D'-d_{on}} \quad (31)$$

Each component in Eq. (31) can be derived as:

$$< i_d(t) >_{d_{on-S}} = < i_{L1}(t) >_{d_{off-S}} - < i_m(t) >_{d_{off-S}} = \frac{d_{on}}{2f_{sw}}\left(\frac{1}{2L-2L_m}\right)\left(\frac{L-L_m}{L}V_g + \frac{L_m}{2L}\frac{V}{n}\right) - \frac{d_{on}}{2f_{sw}}\left(\frac{1}{2L_m}\right)\left(\frac{L_m}{L}V_g - \frac{L_m}{2L}\frac{V}{n}\right) = \left(\frac{d_{on}}{8f_{sw}(L-L_m)}\frac{V}{n}\right) = d_{on}V_g/(4f_{SW}(D' + d_{on})(L-L_m)) \quad (32)$$

and,

$$< i_d(t) >_{D-d_{on}} = 2 < i_d(t) >_{d_{on-S}} \quad (33)$$

$$< i_d(t) >_{d_{on-D}} = < i_d(t) >_{d_{on-S}} \quad (34)$$

$$< i_d(t) >_{D'-d_{on}} = 0 \quad (35)$$

Using Eqs. (32-35), average difference current for the turn-on delay can be found as,

$$K = D\, d_{on} V_g/(2 f_{SW}(D' + d_{on})(L-L_m)) \quad (36)$$

IV. Experimental Results

Figs. 12-14 show results from different configurations of current balancing for PPIBC. Switching delays in the tested converter occur due to tolerances of the used components. So, compared to the results in the previous sections, experimental waveforms are the results of not only turn-on and turn-off delays in multiple switches but also component value tolerances like inductances. In Fig. 12, single inductor case waveforms can be seen where turn-off delays cause current spikes and turn-on delays cause offsets between the branch currents.

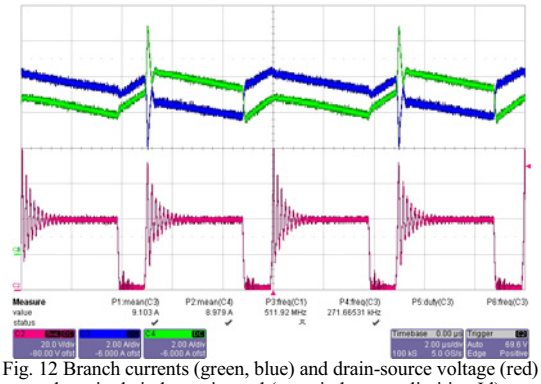


Fig. 12 Branch currents (green, blue) and drain-source voltage (red) when single inductor is used (stray inductance limiting Id)

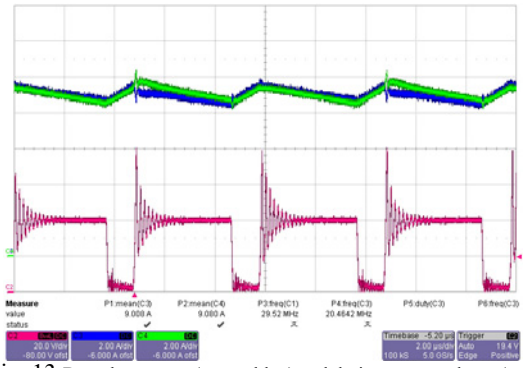


Fig. 13 Branch currents (green, blue) and drain-source voltage (red) when two separate inductors are used

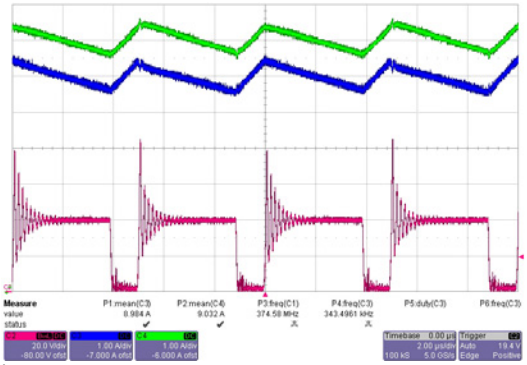


Fig. 14 Branch currents (green, blue) and drain-source voltage (red) when current balancing transformer is used

Fig 13 shows the waveforms for TSI configuration. It can be observed that the tolerance of the two inductors cause slightly different slopes for the two inductor currents. Fig 14 gives the CBT waveforms where branch current waveforms have been given an offset in the scope. Compared to Fig. 12, TSI and CBT configurations seem to suppress the effects of extra operation modes due to switch delays.

V. CONCLUSIONS

In this paper analytical expressions have been derived for single inductor, current balancing transformer (CBT), two separate inductors (TSI) and partially coupled inductors (PCI) for primary parallel isolated boost converter (PPIBC). It has been shown that compared to single inductor; other configurations achieve suppression of current spikes, occurring due to low impedance between the two full bridges in the former case. However an average difference still exists between the branch currents whose value depends on the turn-on/turn-off delay times, switching frequency, input voltage, and the inductance value between the full bridges. There are advantages and disadvantages of each configuration. For example PCI configuration can be implemented as a single component using two E-type powder core halves and winding the two windings around the two side legs. However manufacturing of this component will be expensive since of-the-shelf coil formers are generally designed for center leg windings. TSI configuration achieves current balancing and energy storage at the same time but it has a disadvantage of inductance value tolerance which may easily result in current imbalance. CBT configuration works well for current balancing but it requires two separate components.

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A Novel Topology for Producing Power Level Sinusoidal Output

H. B. Ertan, *Member, IEEE*, and E. Doğru

***Abstract*—Conventional inverter output has PWM output. This pulsed output waveform reduces insulation life time, contributes to quick degradation of the bearings and also is often source of acoustic noise. Furthermore, losses of PWM inverter-driven motors increase. In this paper a novel topology is proposed which is capable of generating a sinusoidal waveform, with low harmonic distortion. If the proposed method is used for driving motors, motor efficiency increases due to reduced losses and lifetime of the motor may be extended. The paper describes the topology used for generating power-level sinus output and how it works. The proposed converter is implemented and tested with resistive and inductive loads. The converter is shown to have the desired properties and the efficiency is shown to be above 95%. The tests on the converter while switching the load on and off illustrate that the converter output voltage is not affected at all from load switching.**

***Index Terms*—AC Machines, Energy efficiency, Inverters, Motor drives, Power conversion, Pulse width modulated converters.**

I. Introduction

MODERN industrial applications often employ variable speed drives. In this way the processes are better controlled and efficiency of the drive is improved. Most motors employed in these applications are 3-phase motors requiring sinusoidal 3-phase voltage supply. Once, the frequency level reaches to a value beyond which the desired output voltage magnitude is not achievable, flux weakening is employed. As it is well known the magnitude of the applied voltage is controlled along with the frequency to keep the magnetic circuit operating condition near design values. Present technology employs inverters for this purpose. Power stage of an inverter is usually composed of a rectifier, rectifying the supply voltage to obtain a DC bus. (Fig.1). This is often followed by a filter stage to smooth the DC bus voltage. The last stage, i.e. the inverter, is a bridge circuit with controlled semiconductors. Modern inverters employ some kind of pulse width modulation (PWM) technique which assures that the resulting pulsed output has a fundamental component at the desired frequency and magnitude.

It must be noted here that the uninterruptable power supplies use the same approach to produce an ac output. The pulsed output of an inverter causes various problems.

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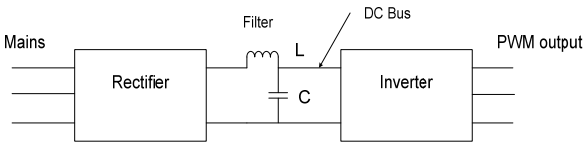

Fig. 1 Block diagram of a conventional inverter

In the first place the high frequency pulsed waveform causes current to flow through the stray capacitances (via insulation) of the motor. This high frequency current limits the life of the insulation [1] and also may cause early bearing failure [2]. A further consequence is that; the losses of the motor increase, due to the high frequency harmonics that exist in the applied voltage waveform. This issue is extensively studied in the literature. It is reported that depending on the type of modulation used, the core losses may increase up to 100% [3], [4].

One solution to this problem is to employ a filter at the output of the inverter, which increases the cost and increases the size of the drive [4]. Alternatively derating of the motor is an option. In this case however, some of the advantages gained from speed control are lost. The motor operates at a lower power factor than possible. Furthermore, the motor is possibly forced to operate at a lower efficiency.

When the motor is driven by PWM voltage source the acoustic noise emitted from the motor also increases. In many applications this constitutes an important problem [5].

Therefore, it is highly desirable to drive an ac motor with a purely sinusoidal waveform to reduce its losses and increase efficiency, and remedy the problems mentioned.

In this paper a new topology is proposed, which can deliver sinusoidal, variable-voltage, variable–frequency output. Single-phase version of the proposed topology is studied here. However, three-phase version can be easily formed by employing three such devices, with the appropriate phase shift in their output voltage.

II. Essence of The Proposal

The presentation here concentrates on illustrating the approach used to obtain a sinusoidal output with harmonic distortion less than required by the related standards. Here the European Norm EN 50160 (Voltage Characteristics in Public Distribution Systems) is taken as reference.

The general block diagram of the proposed topology is shown in Fig. 2. In the arrangement presented, the input side of the converter is a diode bridge as in most commercial UPS or inverters. The DC bus obtained in this manner may be

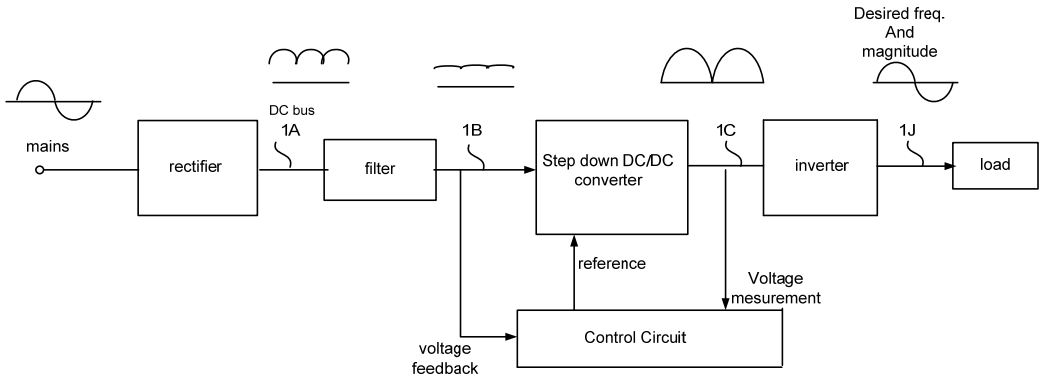

Fig. 2. Block diagram of the sinusoidal waveform generator

filtered to obtain a smoother DC bus. This is followed by a step-down DC/DC converter. This converter is controlled by a microprocessor based controller which assures that the step-down converter follows a reference input which is at the desired shape and frequency. Feedback is provided from the output of the buck converter to the controller. The controller assures that the output has the desired magnitude. Under this control strategy, the output of the converter is rectified form of the desired waveform. Now, to obtain the alternating voltage output one needs to invert the rectified waveform at the zero crossings of every other half cycle.

Note that the inverter at the output is operating at a low frequency, i.e. at the frequency of the desired output. Therefore the transistors used for this stage are not fast devices and their cost is low.

In this paper the design of the converter stages will not be discussed. The emphasis will be on the presentation of the basic idea and the control strategy used to obtain the desired performance.

III. Operation Of The Controller

The control software for the whole converter is embedded in a TMS320 based development kit (DSPACE DS 1104). Necessary feedback signals from the circuit are received by the DSP via AD conversion.

In the heart of this proposal is the conventional buck converter shown in Fig. 3. This circuit is normally used to obtain a regulated DC output, at a value smaller than the DC voltage available on the input side. The capacitor C in the circuit is charged when IGBT 1 is turned on. The output voltage rises in this mode of operation. IGBT 1 is turned off, when the output voltage exceeds the reference value, as much as V.

In that case the energy stored on the inductor L and the load circulates over the capacitor and the free-wheeling diode. The capacitor C discharges and the output voltage drops. This mode of operation goes on until the output voltage drops below the reference value set for the buck converter output, as much as much as V.

With this mode of operation output of a conventional buck converter is a DC value with a high frequency ripple of

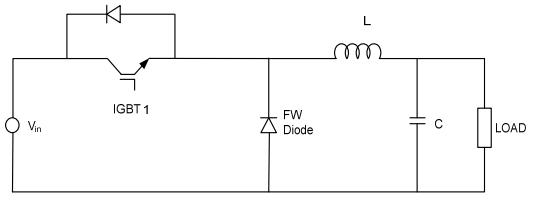

Fig. 3 The step-down dc-dc converter circuit

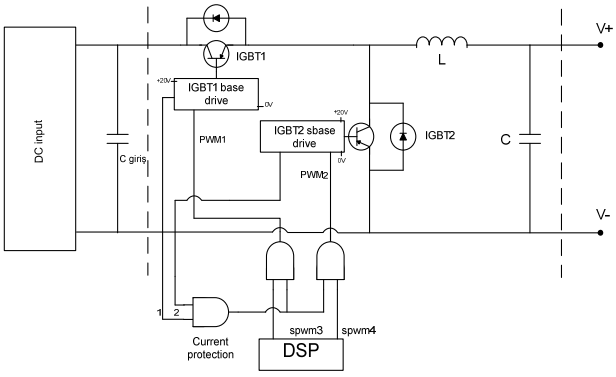

Fig. 4 The modified step down (buck) dc-dc converter circuit

magnitude 2 V. Note that in this kind of application slow decay of the output voltage is desirable, as it becomes possible to have the desired voltage ripple level at a smaller switching frequency.

The analysis of this circuit is easy to find in many power electronics books [7]. The expression for the output voltage of the converter is as in (1).

$$D \times V_{in} = V_{out} \quad (1)$$

In this expression D is

$$D = t_{on}/T \quad (2)$$

where, t_{on} represents the duration in which IGBT 1 is in conduction and T is the sum of on and off durations of IGBT 1. The switching frequency of the buck converter is 1/T.The idea proposed here, is based on the recognition of the fact that

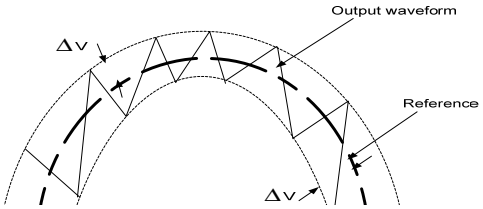

Fig. 5 Modified Buck converter reference and the actual output voltage within the hysteresis band.

the switching frequency of the converter is much higher than the power level frequency required in most applications.

Therefore, it is thought that the converter could follow a slow changing reference signal. Note that the converter can follow any reference shape provided that if frequency is low enough. It is clear that higher the switching frequency as compared to the output frequency better is the fidelity with which the desired signal is produced.

In the application here the study concentrates on generating a sinusoidal output. Initial simulations with a sinusoidal reference indicated that the output of the conventional buck circuit is not capable of following the sinus reference, while the voltage at the output is decreasing (where the output function has negative derivative). For that reason the free wheeling diode in the conventional buck circuit is replaced by an IGBT (IGBT 2 in Fig. 4).

Simulation studies were carried out using PSIM software. This investigation indicated that this arrangement works satisfactorily with the designed controller. Following this verification, the hardware is implemented and the proposed waveform generator topology is tested.

IV. The Experimental Set Up

The control software for the whole converter is embedded in a TMS320 based development kit (DSPACE DS 1104). Necessary feedback signals from the circuit are received by the DSP via AD conversion. Control software cycle is set to 50μs. Due to the discrete nature of the control; the following strategy is applied to assure that the output of the converter follows the reference. At the beginning of each control cycle the output voltage is sampled. For the particular period of time the reference voltage value is read. An error signal is calculated. This value is used to obtain a desired value for the output voltage via a PI control block. Knowing the input voltage of the buck converter a duty cycle is calculated. This information is fed to the PWM generator of the DSP which produces the gate signals for IGBT 1 and IGBT 2.

During the experiments the input voltage of the buck converter is set to 360 V so that 220V rms voltage can be obtained at 50 Hz.

Due to space limitation other details of the control algorithm, such as soft starting, controlling the waveform near zero crossings, etc. are not given here.

The experiments are performed on both resistive and inductive loads with a view to determine the output voltage harmonic distortion and efficiency of the converter. For efficiency measurements on the mains side of the converter (see Fig. 2) a power meter capable of measuring real power despite the distorted input current is used. On the load side, since both the voltage and current are sinusoidal, a power meter capable of measurements in the 25 Hz-80 Hz range is used.

Further experiments are performed to find out whether the proposed converter can handle switching the load “in” and “out”. The experiments are repeated at various frequencies. In the following section, some of the measurement results at 50 Hz output frequency are presented.

V. The Experimental Results

Fig. 6 and 7 display the output voltage of the converter at steady state conditions, while it is supplying an 800 W resistive load. In Fig. 7, the load is set to 365 VA and the power factor of the load is 0.78. These figures illustrate that the output voltage and current waveforms of the converter look very smooth.

In Fig. 6 output voltage and current are in phase as the load is resistive. In Fig. 7, the output voltage has some distortion around the zero crossings. This is because of the algorithm used for generating the rectified sinus waveform. There is certainly room for improving the waveform further.

Many experiments are performed on the proposed converter topology, with resistive and inductive loads at various frequencies. The results presented here represent what is observed quite well. Other issues that need attention are the total harmonic distortion of the voltage waveform and the overall efficiency of the converter. Table1. shows that the total harmonic distortion of the output voltage waveform for

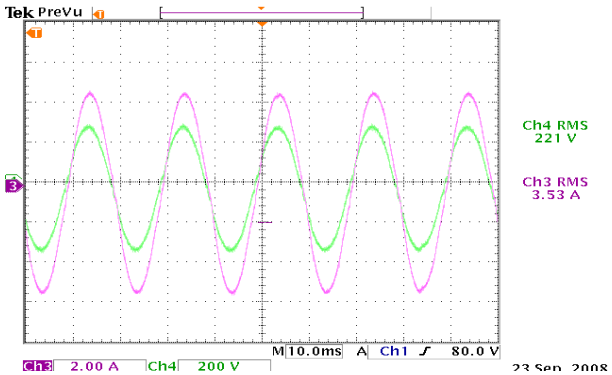

Fig. 6 Steady-state converter output voltage and current (larger magnitude sinus). 800 W resistive load.

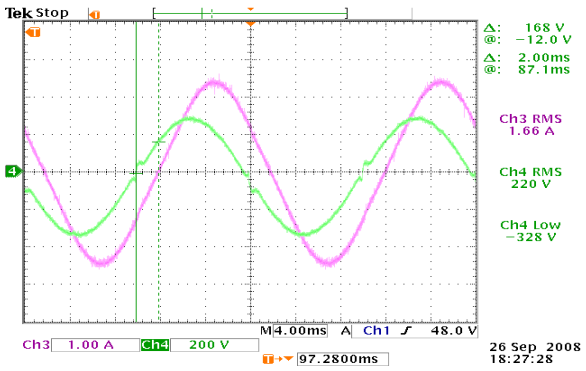

Fig. 7 Steady state inductive load experiment: 50 Hz, power factor: 0.78, 365VA output power. (current is the larger magnitude waveform)

TABLE I
PERFORMANCE OF THE CONVERTER SUPPLYING RESISTIVE LOAD

Load (W)	V_{ref} (V)	f (Hz)	V output (V)	I_{output} (mA)	THD (%)	P out (W)	V_{in} (V)	I_{in} (mA)	P input (W)	Efficiency (%)
800	220	50	221	3530	2.63	780.1	346	2320	802.0	97.2
800	220	25	221	3680	2.16	813.3	343	2490	854.1	95.2

resistive load operation at 50 Hz and 25 Hz. The measured THD is in less than 3% and is within standards. The efficiency of the converter is also very good and is more than 95%.

The performance of the converter is also investigated while inductive and resistive loads are suddenly switched on and off. Fig. 8 displays the behavior of the converter when 800 W resistive load is suddenly connected to the converter output. Fig 9 illustrates the voltage and current waveforms when 800 W resistive load is suddenly removed. It can be observed that the converter performs well and switching the load does not cause and transients on the output voltage.

VI. CONCLUSIONS

This paper introduces a novel topology which produces a smooth sinusoidal waveform (or any desired waveform) with low total harmonic distortion (within standards). There is no need for employing a filter at the output of the converter to obtain this result.

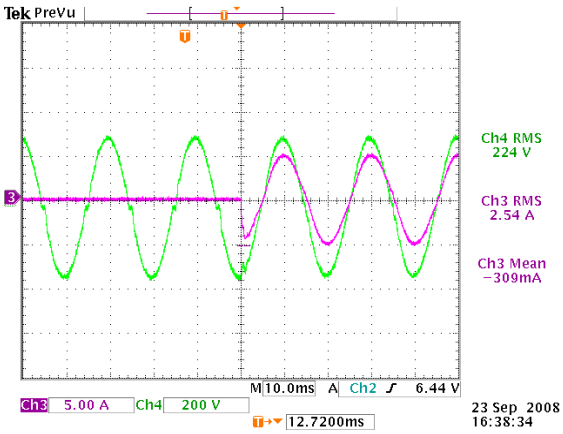

Fig. 8 Resistive load is switched on. Voltage and current waveforms (50 Hz, 800 W. current waveform has smaller magnitude).

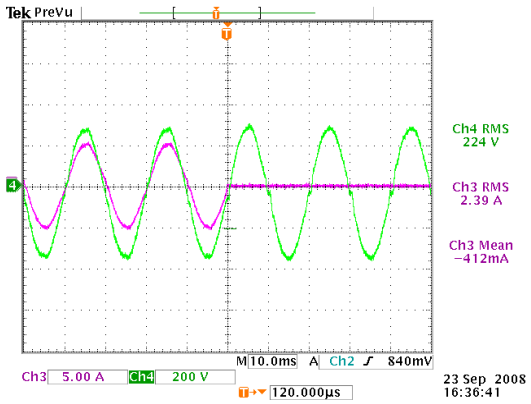

Fig. 9. Resistive load is switched off. Voltage and current waveforms (50 Hz, 800 W. current waveform has smaller magnitude)

Tests on the proposed converter show that; when operating with resistive load, the THD of the output voltage is around 2.5%. It is also observed that the efficiency of the converter is more than 97% at 50 Hz.

Experiments also display that even when the full load is suddenly switched on and off the output voltage is virtually unaffected.

Using this topology in variable frequency drive applications, motor efficiency would improve and other problems caused by pulsed waveforms would be avoided.

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Modeling and Control of Multilevel Three -Phase PWM Current Source Inverter

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Abstract: **The new three-phase 5-level current-source inverter (CSI) proposed in this paper was developed by connecting two classical current – source inverters (CSIs) in cascade. This structure lend an output current harmonics minimization and without the use of high-frequency modulation. The output current waveform of the five-level CSI is composed of intermediary current levels, which are typically obtained from inductors current sources. The operational principle of this structure was analyzed. And to reduce the output current harmonics, triangular - sinusoidal PWM control technique was used. Simulation results showed that this new three-phase 5-level CSI topology operates correctly.**

Keywords: Three-phase, Five-level current-source inverter (CSI), Topology, Harmonics current, PWM strategy.

I. INTRODUCTION

Compared to two-level inverters, multilevel inverters have enormous benefits for higher power applications, including reduced harmonics and increased power ratings because of reduced switching device voltage and current stresses. Until recently, multilevel voltage source inverters have been the dominant multilevel topology, despite the fact that current-source inverters (CSIs) have many advantages for higher power applications. These include more stable operating conditions, direct control of the output current, faster dynamic response in some circumstances, easier fault management, etc[1].

The storage elements in CSIs are inductors, which have the disadvantages of higher conduction losses and lower energy storage efficiency compared to DC-link capacitors, and thus the applications for CSIs are limited. However, some of the disadvantages of traditional inductors can now be overcome owing to the development of superconducting magnetic energy storage (SMES) technology, and hence their use is becoming more attractive, especially for very large current applications [2].

Only a few three-phase multilevel CSI topologies have been proposed [3, 4, 5]. In this paper, we propose a new three-phase 5-level current-source inverter (CSI) structure. We begin by describing operating principles of this converter. In the second part, we elaborate the knowledge and controlled model of this structure. Then the multicarrier PWM technique for multilevel source current inverter is developed. A steady dynamic modelling and representative results of circuit simulations are presented too.

II. CONVERTER MODELLING

A. Topology

The three-phase five-level current-source inverter CSI topology shown in Fig.1, which is made up by connecting two classical current – source inverters (CSIs) in cascade. Each converter consists of 6-switch (diode - transistor) S_{ki} controlled in the opening and closing.

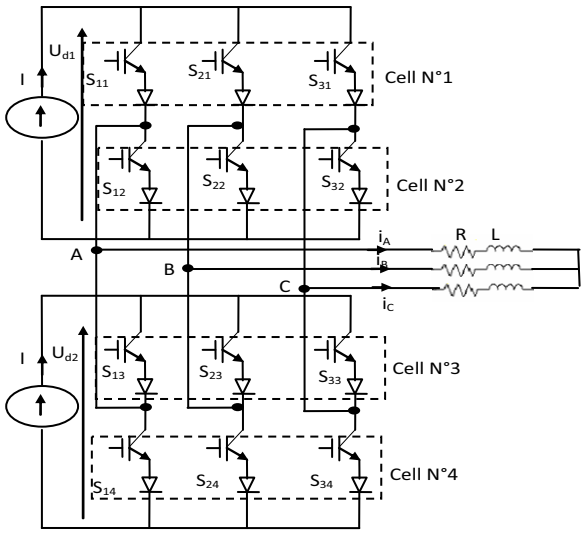

Fig.1 Structure of three phase five-level current source inverter

To generate the 5-level output current of this converter topology, the switching combination is shown in Table 1.

Table. 1 Different switching combination of three-phase 5-level CSI

Switching combinations	Output current
($S_{k1}S_{k4}$) or ($S_{k3}S_{k2}$) or ($S_{k1}S_{k2}$)or ($S_{k3}S_{k4}$)	0
(S_{k1}) or (S_{k3}) or ($S_{k1}S_{k3}S_{k4}$) or ($S_{k3}S_{k1}S_{k2}$) ($S_{k1}S_{k3}$)	I
(S_{k2}) or (S_{k4}) or ($S_{k2}S_{k3}S_{k4}$) or ($S_{k4}S_{k1}S_{k2}$)	2I
($S_{k2}S_{k4}$)	-I
	-2I

The symmetry of the three-phase five-level CSI allows its modelling by arms [5-7]. Fig.2 shows the different configuration of one arm of five-level CSI.

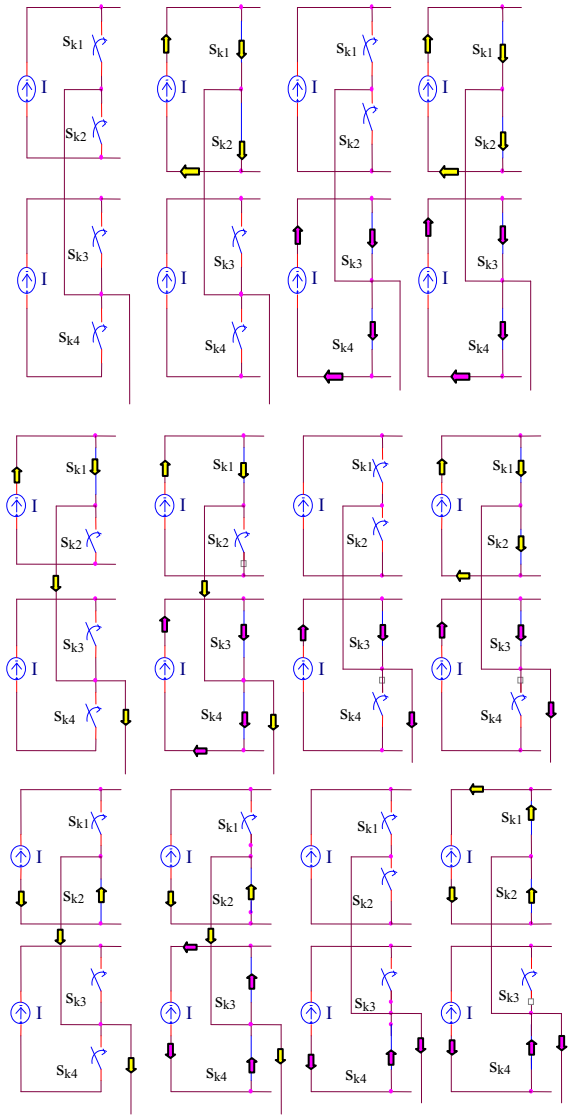

Fig.2 Different configuration of three phase five-level current source inverter

B. *Knowledge model of the converter*

Several complementary laws are possible for three-phase five-level CSI. The optimal complementary law (which gives the five levels without short or open circuit) used for this converter is presented below [6-7]:

$$S_{1i} + S_{2i} + S_{3i} = 1 \tag{1}$$

S_{ki} is the control signal of the semiconductor TD_{ki}; i indicates the number of the switches (1, 2,3 or 4) and k = (1,2 or 3) number of phase.

In order to elaborate the control model of each rectifier (Fig.1), we define for each semi-conductor S_{ki} of the converter the connection function s_{ki} as follows [6-7]:

$$S_{ki}(t) = \begin{cases} 1, & S_{ki}\ closed \\ 0, & S_{ki}\ open \end{cases} \tag{2}$$

At any given instant, only one switch in the upper half and one switch in the bottom half of the bridge conducts. So that the input voltages are never shorted, and freewheeling path for the inductor current is always provided. These conditions can be expressed as:

$$S_{ki} + S_{ki} + S_{ki} = 1 \tag{3}$$

Then, from Fig.1, the output currents are given by:

$$\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \begin{bmatrix} (S_{11} - S_{12}) + (S_{13} - S_{14}) \\ (S_{21} - S_{22}) + (S_{23} - S_{24}) \\ (S_{31} - S_{32}) + (S_{33} - S_{34}) \end{bmatrix} . I \tag{4}$$

While the input voltages U_{d1} and U_{d2} are:

$$\begin{bmatrix} U_{d1} \\ U_{d2} \end{bmatrix} = \begin{bmatrix} S_{11} - S_{12} & S_{21} - S_{22} & S_{31} - S_{32} \\ S_{13} - S_{14} & S_{23} - S_{24} & S_{33} - S_{34} \end{bmatrix} \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} \tag{5}$$

Where V_{AN}, V_{BN} and V_{CN} are the load phase voltages.

C. *Controlled Model of the converter*

At frequencies significantly below the switching frequency, operation of the circuit can be modelled by an average model. Thus, we define the generating function "X_g" of the discontinuous one "X", as the mean of "X" on a modulation period T_h supposed very small as follow [5-7]:

$$X_g = \left[\frac{1}{T_h} \int_0^{T_h} X\, dt \right] \tag{6}$$

The average model of three-phase five-level CSI, where all quantities are continuous, is given by the following equations with $\langle i_A \rangle$, $\langle i_B \rangle$ and $\langle i_C \rangle$ representing the mean value of the instantaneous ones, and S_{kig} are generating connection function of each switches s_{ki}.

$$\begin{bmatrix} \langle i_A \rangle \\ \langle i_B \rangle \\ \langle i_C \rangle \end{bmatrix} = \begin{bmatrix} S_{11g} - S_{10g} \\ S_{21g} - S_{20g} \\ S_{31g} - S_{30g} \end{bmatrix} I_{red} \tag{7}$$

$$\text{And} \begin{bmatrix} \langle U_{d1} \rangle \\ \langle U_{d2} \rangle \end{bmatrix} = \begin{bmatrix} S_{11g} - S_{12g} & S_{13g} - S_{14g} \\ S_{21g} - S_{22g} & S_{23g} - S_{24g} \\ S_{31g} - S_{32g} & S_{33g} - S_{34g} \end{bmatrix}^T \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} \quad (8)$$

The average model of the three-phase five-level CSI is used to develop new algorithms of PWM control strategy.

III. PWM CONTROL STRATEGY

Different PWM control strategies are developed for multilevel CSI. These strategies are extended from two-level carrier-based PWM techniques to multilevel inverters by making the use of several triangulo carriers and one reference signal by phase.

A. Triangulo-Sinusoidal with two Carriers

This strategy is based on the general principle given by **T.ONISHI** and **K.OKITSU** in 1983 [6, 7, 8]. This algorithm consists in comparing two unipolar triangular carriers with the currents references $i_{ref}(k)$ as its shown in Fig.3. These references signals are defined as follow:

$$i_{ref}(k) = I_m . \sin\left(2.\pi.t.f - \frac{2\pi}{3}(k-1)\right) \quad (9)$$

We defined for this strategy the magnitude modulation index *r* and the frequency ratio *m* as:

$$r = \frac{I_m}{I}, \quad m = \frac{f_h}{f} \quad (10)$$

Where f_h is the modulation frequency.

The algorithm of this strategy can be summarized as following:

- $0 \le t \prec \frac{T}{6}$: We module by S_{11}, S_{21}, S_{31}, S_{13}, S_{23} and S_{33}.

Then, we have: $S_{12} = S_{32} = 0$ & $S_{22} = 1$

$if\ i_{ref1} > U_{p1}\ then\ S_{11} = 1\ else\ S_{11} = 0$

$if\ i_{ref1} > U_{p2}\ then\ S_{13} = 1\ else\ S_{13} = 0$

$if\ i_{ref3} > U_{p2}\ then\ S_{31} = 1\ else\ S_{31} = 0$

$if\ i_{ref3} > U_{p2}\ then\ S_{33} = 1\ else\ S_{33} = 0$

$S_{21} = 1 - S_{11} - S_{31}$

$S_{23} = 1 - S_{13} - S_{33}$

- $\frac{T}{6} \le t \prec \frac{T}{3}$: We module by S_{12}, S_{22}, S_{32}, S_{14}, S_{24} and S_{34}.

Then, we have: $\begin{cases} S_{21} = S_{31} = 0 \ \& \ S_{11} = 1 \\ S_{23} = S_{33} = 0 \ \& \ S_{13} = 1 \end{cases}$

$if\ i_{ref2} > U_{p1}\ then\ S_{22} = 1\ else\ S_{22} = 0$

$if\ i_{ref2} > U_{p2}\ then\ S_{24} = 1\ else\ S_{24} = 0$

$if\ i_{ref3} > U_{p2}\ then\ S_{32} = 1\ else\ S_{32} = 0$

$if\ i_{ref3} > U_{p1}\ then\ S_{34} = 1\ else\ S_{34} = 0$

$S_{12} = 1 - S_{22} - S_{32}$

$S_{24} = 1 - S_{14} - S_{34}$

During the rest of the period T of the network, the connection functions are:

$$S_{12}(\omega t) = S_{22}(\omega t + 2\pi/3) = S_{32}(\omega t + 4\pi/3)$$
$$S_{14}(\omega t) = S_{24}(\omega t + 2\pi/3) = S_{34}(\omega t + 4\pi/3)$$

$$S_{11}(\omega t) = S_{21}(\omega t + 2\pi/3) = S_{31}(\omega t + 4\pi/3)$$
$$S_{13}(\omega t) = S_{21}(\omega t + 2\pi/3) = S_{31}(\omega t + 4\pi/3)$$

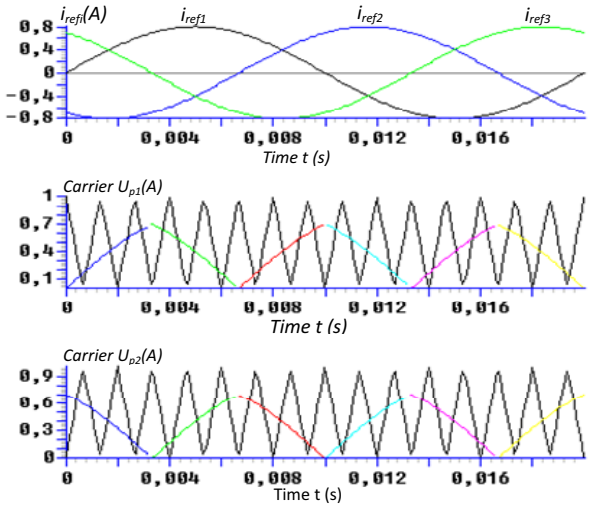

Fig.3 Control strategy signals

In order to verify the effectiveness of this strategy, some simulation tests are carried out for *m* =6, 21 and r = 0,8. In this section, we suppose that, the DC input current sources are constant and equal (*I*=15A). The output current i_A of the five-level NPC CSI is symmetrical and has sinusoidal wave form (Fig.4-*) with low harmonics. We note that the current harmonics gather by families around frequencies multiple of 2*mf (Fig.4-*). The highest amplitudes of these harmonics are of the rank $2m \pm 1$et $2m \pm 4$. The even and odd harmonics are present for m=21.

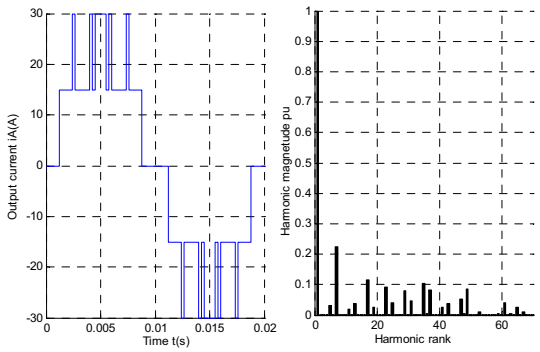

Fig.4-a Output current of five-level CSI for m=6,r=0.8

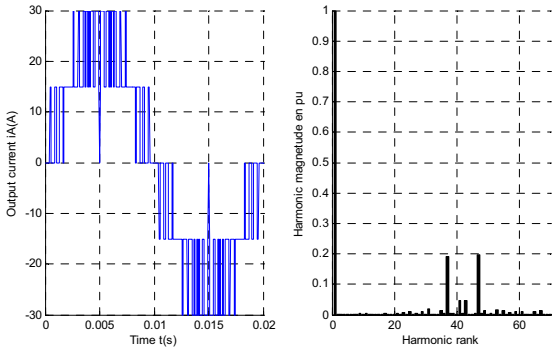

Fig.4-b Output current of five-level CSI for m=21,r=0.8

Fig.5 presents the harmonics rate. These later decreases when the amplitude modulation index r increases

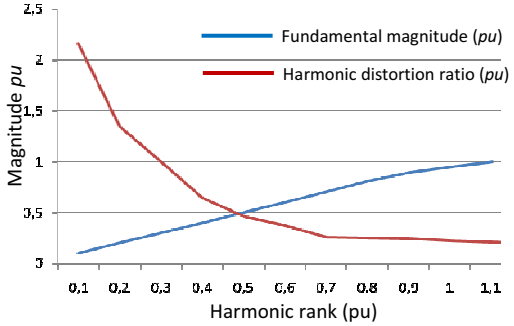

Fig.5 Harmonic rate of the line current of five level CSI

The three line currents (i_A, i_B & i_C) of five level CSI are shown in Fig.6. We note that these currents present symmetric three-phase.

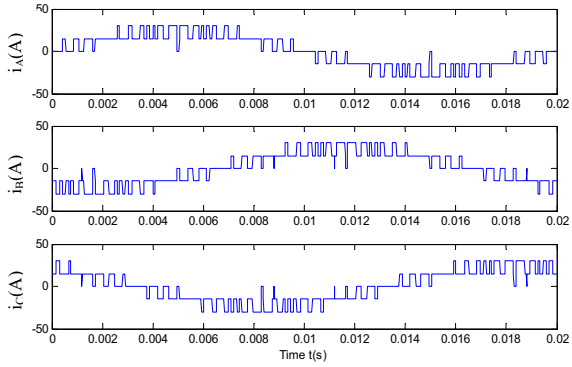

Fig.6 Output currents i_A, i_B & i_C of five level CSI

B. Algebraic PWM Strategy

Different Triangular-sinusoidal strategies could be achieved with digital mean by sampling reference signal. In this paper, we develop a new digital PWM algorithm of three-phase five level CSI dedicated for a digital realisation and obtained by using the control model developed previously[6-7]. The general flow chart of an algebraic PWM using this control model is presented in Fig.7. This strategy is characterised by modulation index m defined as a ratio between the frequency f_c of the carrier and the frequency of the reference signal ($m_c = f_c / f$), and modulation rate (r_c) is the ratio of the reference signal magnitude and that of the carrier ($r_c = I_m / I$).

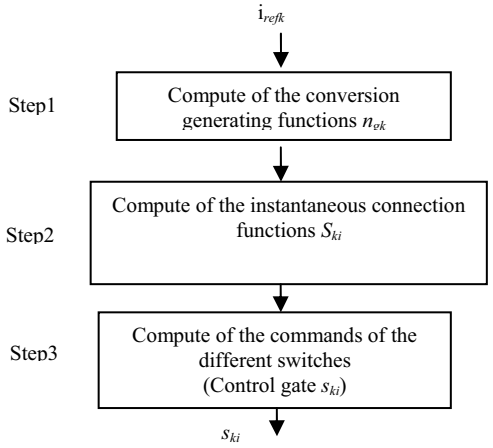

Fig. 7 The general of flow chart of an algebraic modulation using average model of the CSI

This algorithm is based on the triangular-sinusoidal strategy with two carriers [6]. The different steps of the algorithm are as follow

Step 1: Compute of the generating simple conversion functions n_{gk} :

$$ng_k = \frac{i_{refk}}{I}; \quad k = 1,2,3 \tag{11}$$

With $i_{refk} = I_{ref}\sqrt{2}\sin(\omega t - \frac{2\pi}{3}(k-1))$ and I is the DC input current.

Step 2: Compute of the connection functions S_{ki}

1- Detection of maximum of n_{gk} :

$$Y = \max(|ng_1|, |ng_2|, |ng_3|)$$

2- Compute of time of conduction

$$t_1 = |ng_1|.T_h$$

$$t_2 = |ng_2|.T_h$$

$$t_3 = |ng_3|.T_h$$

With T_h is modulation period.

3- if $Y = |ng_1|$ Then if $ng_1 \succ 0$ then :

- $S_{11} = S_{13} = 1, S_{21} = S_{31} = S_{23} = S_{33} = 0$
- $0 \prec t \le t_2 \Rightarrow \begin{cases} S_{12} = S_{32} = 0, S_{22} = 1 \\ S_{24} = S_{34} = 0, S_{14} = 1 \end{cases}$
- $t_2 \prec t \le t_2 + t_3 \Rightarrow \begin{cases} S_{22} = S_{12} = 0, S_{32} = 1 \\ S_{14} = S_{34} = 0, S_{24} = 1 \end{cases}$
- $t_2 + t_3 \prec t \le T_h \Rightarrow \begin{cases} S_{22} = S_{32} = 0, S_{12} = 1 \\ S_{14} = S_{24} = 0, S_{34} = 1 \end{cases}$

if $ng_1 \prec 0$ then :

- $S_{12} = S_{14} = 1, S_{22} = S_{32} = S_{24} = S_{34} = 0$

- $0 \prec t \le t_2 \Rightarrow \begin{cases} S_{11} = S_{31} = 0, S_{21} = 1 \\ S_{23} = S_{33} = 0, S_{13} = 1 \end{cases}$
- $t_2 \prec t \le t_2 + t_3 \Rightarrow \begin{cases} S_{11} = S_{21} = 0, S_{31} = 1 \\ S_{13} = S_{23} = 0, S_{33} = 1 \end{cases}$
- $t_2 + t_3 \prec t \le T_h \Rightarrow \begin{cases} S_{21} = S_{31} = 0, S_{11} = 1 \\ S_{23} = S_{33} = 0, S_{13} = 1 \end{cases}$

4- if $Y = |ng_2|$ Then if $ng_2 \succ 0$ then :

- $S_{21} = S_{23} = 1, S_{11} = S_{31} = S_{13} = S_{33} = 0$
- $0 \prec t \le t_1 \Rightarrow \begin{cases} S_{22} = S_{32} = 0, S_{12} = 1 \\ S_{14} = S_{34} = 0, S_{24} = 1 \end{cases}$
- $t_1 \prec t \le t_1 + t_3 \Rightarrow \begin{cases} S_{22} = S_{12} = 0, S_{32} = 1 \\ S_{24} = S_{34} = 0, S_{14} = 1 \end{cases}$
- $t_1 + t_3 \prec t \le T_h \Rightarrow \begin{cases} S_{12} = S_{23} = 0, S_{22} = 1 \\ S_{14} = S_{34} = 0, S_{24} = 1 \end{cases}$

if $ng_2 \prec 0$ then :

- $S_{22} = S_{24} = 1, S_{12} = S_{32} = S_{14} = S_{34} = 0$
- $0 \prec t \le t_1 \Rightarrow \begin{cases} S_{21} = S_{31} = 0, S_{11} = 1 \\ S_{13} = S_{33} = 0, S_{23} = 1 \end{cases}$
- $t_1 \prec t \le t_1 + t_3 \Rightarrow \begin{cases} S_{11} = S_{21} = 0, S_{31} = 1 \\ S_{23} = S_{33} = 0, S_{13} = 1 \end{cases}$
- $t_1 + t_3 \prec t \le T_h \Rightarrow \begin{cases} S_{11} = S_{31} = 0, S_{21} = 1 \\ S_{13} = S_{23} = 0, S_{33} = 1 \end{cases}$

5- if $Y = |ng_3|$ Then if $ng_3 \succ 0$ then :

- $S_{31} = S_{33} = 1, S_{11} = S_{21} = S_{13} = S_{23} = 0$
- $0 \prec t \le t_3 \Rightarrow \begin{cases} S_{22} = S_{32} = 0, S_{12} = 1 \\ S_{34} = S_{24} = 0, S_{14} = 1 \end{cases}$
- $t_1 \prec t \le t_1 + t_2 \Rightarrow \begin{cases} S_{32} = S_{12} = 0, S_{22} = 1 \\ S_{14} = S_{34} = 0, S_{24} = 1 \end{cases}$
- $t_1 + t_2 \prec t \le T_h \Rightarrow \begin{cases} S_{12} = S_{23} = 0, S_{23} = 1 \\ S_{14} = S_{34} = 0, S_{24} = 1 \end{cases}$

if $ng_3 \prec 0$ then :

- $S_{34} = S_{32} = 1, S_{12} = S_{22} = S_{24} = S_{14} = 0$
- $0 \prec t \le t_1 \Rightarrow \begin{cases} S_{21} = S_{31} = 0, S_{11} = 1 \\ S_{23} = S_{13} = 0, S_{33} = 1 \end{cases}$
- $t_1 \prec t \le t_1 + t_2 \Rightarrow \begin{cases} S_{11} = S_{31} = 0, S_{21} = 1 \\ S_{23} = S_{33} = 0, S_{13} = 1 \end{cases}$
- $t_2 + t_1 \prec t \le T_h \Rightarrow \begin{cases} S_{21} = S_{11} = 0, S_{31} = 1 \\ S_{13} = S_{33} = 0, S_{23} = 1 \end{cases}$

Step 3: Compute of the commands of the different switches (Control gate s_{ki})

$$\begin{cases} S_{ki} = 0 \Rightarrow s_{ki} = 0 \\ S_{ki} = 1 \Rightarrow s_{ki} = 1 \end{cases}$$

Fig. 8-* represent the line output current of three-phase five level CSI controlled by the proposed algebraic modulation for m =15, m =24 and r=0.8. The current harmonics gather by families centred on frequencies multiple of $m.f$, where the most important harmonics are $(m\pm1)$ and $(2.m\pm1)$ in view of their magnitude.

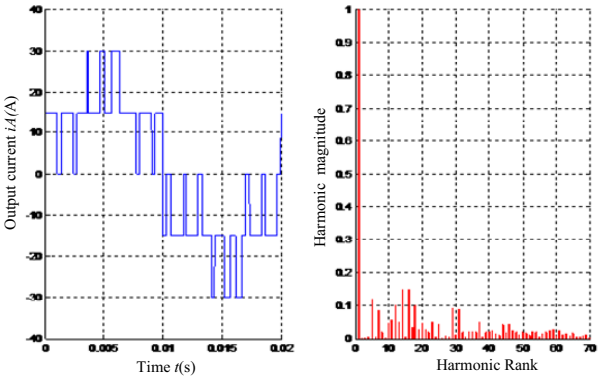

Fig.8-a Output current of five-level CSI for m=15,r=0.8

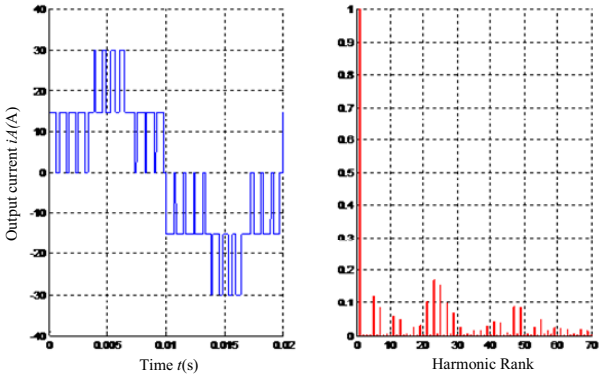

Fig.8-b Output current of five-level CSI for m=24,r=0.8

Fig.9 presents the harmonics rate. These later decreases when the amplitude modulation index r increases

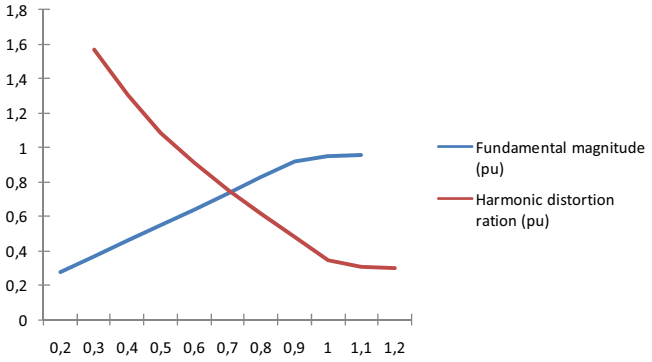

Fig.9 Harmonic rate of the line current of five level CSI

The three line currents (i_A, i_B & i_C) of five level CSI are shown in Fig.10. We note that these currents present symmetric three-phase.

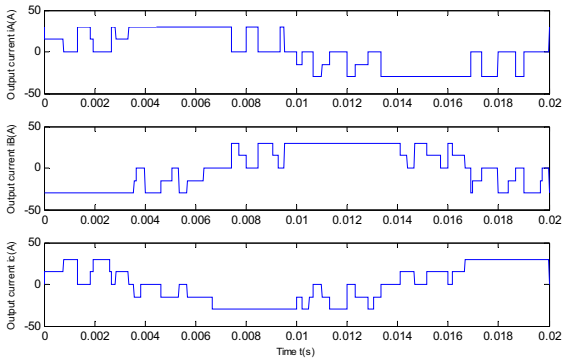

Fig.10 Three phase output currents i_A, i_B & i_C of five level CSI

IV. CONCLUSION

In this paper, a new structure of three-phase PWM current source inverter is proposed. Two PWM control strategies are developed. The triagulo-sinusoidal strategy with multi carriers gives an output current of the five-level PWM CSI with odd harmonics for odd and even frequency index modulation *m*. When the magnitude modulation index is increased the harmonics are rejected towards high rank where it is easily to filter them by the machine. The three output current i_A, i_B & i_C present symmetric three phase system.

The algebraic modulation permit to have an output current of the five-level PWM CSI with odd and even harmonics for odd and even frequency index modulation *m*. This strategy is used for implamentation.

The performances obtained are full of promise to use this converter in great power and high voltage industrial fields.

V. REFERENCE

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Operation of Three-Phase Power Factor Corrected (PFC) Rectifiers

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***Abstract*–Rectifier circuits make a large number of higher harmonics in the mains and lower the power factor (PF). To reduce this harmful effect, rectifier circuits with electronic control are introduced. This article presents two Power Factor Correction rectifier circuits: 1- and 3-phase circuits. We present here the method of controlling these rectifiers, that allows to increase the power factor of these rectifiers. In the article we present also an algorithms, that provide this controlling. The simulation results confirms effectiveness of the proposed controlling. Presented method of controlling of 1- and 3-phase rectifiers causes, that the current drawn from the main is close to sinusoid and has the same phase as feeding voltage. Computer simulations confirmed effectiveness of the presented controlling. So this circuits can be considered as the Power Factor Correction circuits.**

I. INTRODUCTION

For ideal sinusoidal course power factor $cos(\varphi)$ is ratio of active power P to apparent power S. Occurrence of higher harmonics should be considered at deformed courses. Therefore, power factor PF is expresses by formula:

$$PF = \frac{I_{(1)}}{I} \cdot \cos(\varphi) \le 1 . \tag{1}$$

Where factor $cos(\varphi)$ is related to basic harmonic while $I_{(1)}$ and I are root-mean-square values, basic harmonic and full current course respectively. To boost efficiency of electric circuit it is favorable to obtain possible high value of this factor PF. New regulation require monitoring of feed power at power higher than 200 V. Conventional rectifiers consume currents from the mains in impulse way. Maximal current value can be even 7 times higher than maximal value of substitute sinusoidal current. It courses a lot of problems. Higher harmonics of currents and voltages in the mains are formed which can be dangerous for the number of devices. It is also connected with high losses and the necessity of redimensioning of the mains. Maximal power which can be transmitted by the mains is limited and power factor can be even reduced to value 0.45. High voltage drops are connected with higher current harmonics in the mains which can cause the necessity of paying high compensation Power Factor Correction (PFC) rectifiers presented in the article have the task of bringing current consumed from the mains closer to sinusoidal current in voltage-phase. In this way resistance load is simulated. It is possible by electronic controlling of rectification process.

II. POWER FACTOR CORRECTION (PFC) 1-PHASE AC/DC RECTIFYING CIRCUIT

Fig. 1 shows 1-phase rectifier circuit which makes it possible to meet this demand.

The "Boost" rectifier operation means that obtained rectified voltage $uz = uC$ should be higher than maximal value of feed voltage *es*. The cycle of transistors T6 turn-on (*d*) and turn-off (1–*d*) equals in time cycle t_wyp_time of turning is off. In order to obtain relatively high factor PF, feed current course *i*8 should be as much close to sinusoidal as possible. It is assumed that feed voltage course $es(t)$ is shown as:

$$\begin{aligned} es(t) &= Esm \cdot \sin(\omega 0 \cdot t + faza) \\ us(t) &= \sin(\omega 0 \cdot t + faza) \end{aligned} \tag{2}$$

Where *Esm* is feed voltage maximal value, $\omega 0$ is basic harmonic pulsation, while $us(t)$ is a model voltage with maximal value equal 1. To obtain high PF factor value, feed current *i*8 flowing from the mains should be proportional to model voltage $us(t)$:

$$i8(t) = pr\_Im \cdot us(t) \tag{3}$$

Where *pr_Im* is this current maximal value. It is subject to control to guarantee obtaining of given value *uz_ref* by rectified voltage $uz = uC$. Considering instantaneous rectified voltage variation *uz_ref*, higher harmonics filtered voltage *uzf* is taken to control. Filtration is to connect rectified voltage *uz* into series circuit input *Rf*, *Lf*. Filtered voltage *uzf* is consumed

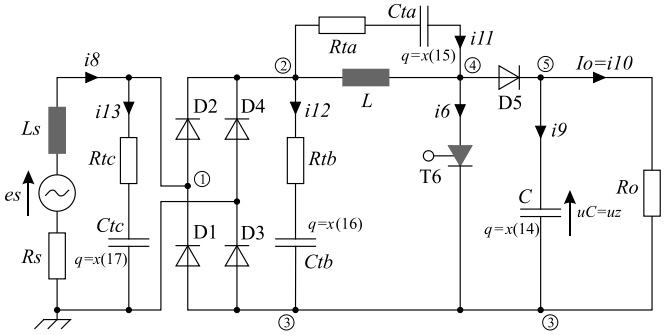

Fig.1. 1-phase AC/DC rectifier in "Boost" circuit which inductance current *L*, *prL=iL=i7*.

voltage over resistance *Rf*. Difference (*uz_ref* – *uz_f*) is fed into PI controller input (procedure `wej_st_pm()`), by determining maximum of input current *pr_Im*:

$$pr\_Im = 30 + 5 \cdot PI(uz\_ref - uz\_f) \tag{4}$$

At the whole cycle spam *t_wyp_c* relative time $d = d\_akt$ of turning transistor T6 on is determined. Towards the end of this period the next control d is determined. In order to do that (also over the mains) at the end of each period (time cycle *t_wyp_c*) as:

$$prL = pr\_Im \cdot \sin(\omega 0 \cdot (t + t\_wyp\_c) + faza) \tag{5}$$

and the mains voltage rectified by bridge circuit, also in the end-point of the next time cycle:

$$ef = Esm \cdot abs(\sin(\omega 0 \cdot (t + t\_wyp\_c) + faza)) \tag{6}$$

At the moment current flowing over inductance at the beginning of new cycle is $pr7 = x(7)$. Relative time of switching *d* translator T6 on is determined by balance on inductance current gain *L*:

$$t\_wyp\_c \cdot \left[\frac{ef}{L} \cdot d + \frac{ef - uC}{L} \cdot (1 - d) \right] = prL - pr7 \tag{7}$$

that is:

$$d = \frac{\left(\frac{prL - pr7}{t\_wyp\_c} \right) - \left(\frac{ef - uC}{L} \right)}{\frac{uC + 0{,}1}{L}}. \tag{8}$$

Rectified voltage *uC* was here boosted by 0.1 to avoid dividing by 0.

The circuit from fig. 1 under consideration was completed in order to damp oscillations on series circuits *Rta*, *Cta*, *Rtb*, *Ctb* and *Rtc*, *Ctc*. It includes $ig = 13$ branches, $iv = 5$ independent modes. Amount of unknowns is $in = 17$. State variables $x(in)$ are determined as: $x(1:5)$=diode currents; $x(6)$is transistors T6 current; $x(7) = il$; $x(8) = i8 = is$; $x(9) = iC$; $x(10) = Io$; $x(11:13) = x(15:17)$ damping capacity charges *Cta*, *Ctb*, *Ctc*.

The program that calculates circuit transient states from fig. 1 is presented below:

```
nw=5; in=17;  iv=5; x=zeros(in,1); x0=x;
d_p=0; d=d_p; id=6; us=0; Esm=230*sqrt(2);
przew=zeros(id,1); przew_p=przew; p_d=przew;
V=zeros(iv,1); Cic_st=0; faza=0.0;
C=3.3e-3;  Ro=30.0; w0=2*pi/0.02; pi23=2*pi/3;
pi43=4*pi/3;
uz_ref=500; icm=0; t_wyp_c=0.0250e-3;
czas_lm=0; czas_lw=0; czas_zm=20*t_wyp_c;
t_d1=t_wyp_c; t_d0=0; Rd=zeros(id,1); Ed=Rd;
st_d=Ed; Ud=Ed; Rdn=Rd; Udn=Ud; Edn=Ed;
us_p=sin(faza); us_prz=us_p; ig=13;
pol=zeros(ig,iv); Yv=zeros(iv,iv);
Ev=zeros(iv,1); V=Ev; Yg=zeros(ig,1); Eg=Yg;
pol(1,1)=1; pol(1,3)=-1; pol(2,2)=1; pol(2,1)=-
1; pol(3,3)=-1; pol(4,2)=1; pol(5,5)=1;
pol(5,4)=-1; pol(6,3)=1; pol(6,4)=-1;
pol(7,4)=1; pol(7,2)=-1; pol(8,1)=1;
pol(9,3)=1; pol(9,5)=-1; pol(10,3)=1;
pol(10,5)=-1;  pol(11,4)=1; pol(11,2)=-1;
pol(12,3)=1; pol(12,2)=-1; pol(13,1)=-1;
uz_f=0;pol=pol'; d_nast=0;
for ii=1:id, st_d(ii)=1; end; dp=0; d=dp;
st_d(id)=d; dp=0; d=dp; d_akt=1; ktore_n=-1;
d_akt_n=0.9; male_L=0; L=0.15e-1;  L=0.0004;
male_L=1;
R=w0*L/1000; Rs=0.00001; Ls=Rs/w0;
ik=500000; dt=1e-6; dt_m=dt*1e-5; dt_mx=dt_m;
dt0=dt_m; lm=1; lw=0;
wy=zeros(in+7,ik); twy=zeros(1,ik); t_pocz=0;
wyV=zeros(iv,ik); logo=1; t_d_nastepne_st=0.5;
for iijj=1:ik, dtx=dt; if (dt0<0.01*dtx),
dtx=dt*0.011; end;
if ((d_p==0)&(d==1)), dtx=dt*1e-5; end; if
((d_p==1)&(d==0)), dtx=dt*1e-5; end;
if (dtx<dt_m); dtx=dt_m; end; dt_obl=dtx;
d_p=d; x0=x; V0=V;
t_kon=t_pocz+dtx;  w0t=w0*t_kon; us_p=us;
us=sin(w0t+faza); st_d(id)=d;
for jj=1:id,
[Ud(jj),Ed(jj),Rd(jj),U0,p0,przew_p(jj)]=diod(x
0(jj),st_d(jj)); end; Yd=1./Rd;
uz=x0(14)/C; uC=uz; aa=dtx/C; Rta=1e3; Cta=1e-
9; dd=dtx/Cta; ee=1/(Rta+dd);
Rtb=1e3; Ctb=1e-9; ff=dtx/Ctb; gg=1/(Rtb+ff);
Rtc=1e3; Ctc=1e-9; hh=dtx/Ctc; kk=1/(Rtc+hh);
Rss=(Rs+Ls/dtx); Yss=1/Rss; Y=1/(R+L/dtx);
Yg=[Yd;Y;Yss;1/aa;1/Ro;ee;gg;kk]; Yc=diag(Yg);
Yv=pol*Yc*pol'; uC=x0(14)/C;
uCta=x0(15)/Cta; uCtb=x0(16)/Ctb;
uCtc=x0(17)/Ctc; Eg=[-Ed;0;Esm*us;-uC;0;-uCta;
-uCtb;-uCtc]; Eg(7)=Eg(7)+(L/dtx)*x0(7);
Eg(8)=Eg(8)+(Ls/dtx)*x0(8);
Ig_=Yg.*Eg; Iv=pol*Ig_; V=Yv\Iv; Eg_=Eg-pol'*V;
Ig__=Yg.*Eg_; x(1:ig)=Ig__;
Io=x(10); IC=x(9); ICa=x(11); ICb=x(12);
ICc=x(13); x(14)=x0(14)+IC*dtx;
x(15)=x0(15)+ICa*dtx; x(16)=x0(16)+ICb*dtx;
x(17)=x0(17)+ICc*dtx; uC=x(14)/C;
uCta=x(15)/Cta; uCtb=x(16)/Ctb; uCtc=x(17)/Ctc;
uz=uC; lo=1;  dt0=dtx; los=1;
if (los==1), for jj=1:id,
[Udn(jj),Edn(jj),Rdn(jj),U0,p0,przew_n(jj)]=dio
d(x(jj),st_d(jj));
lo1=(przew_n(jj)==przew_p(jj)); if (~lo1),
dty=dtx*abs((x0(jj)-p0)/(x0(ii)-x(jj)));
if (dty>dt), dty=dt; end; if (dty<dt0),
dt0=dty; end; dt0=dt0*1.0000001;
if (dt0<dt_m); dt0=dt_m; end; dt_mx=dt0; end;
lo=lo&lo1; end; lox=lo;
if (lo==0); dt0=dt0*1.0000001;
t_kon=t_pocz+dt0; dtx=dt0; x=x0+(x-
x0)*(dt0/dt_obl);
Io=x(10); Is=x(8); IC=x(9); ICa=x(11);
ICb=x(12); ICc=x(13); x(14)=x0(14)+IC*dtx;
x(15)=x0(15)+ICa*dtx; x(16)=x0(16)+ICb*dtx;
x(17)=x0(17)+ICc*dtx; uC=x(14)/C;
```

```
uCta=x(15)/Cta; uCtb=x(16)/Ctb; uCtc=x(17)/Ctc;
uz=uC;V=V0+(V-V0)*(dt0/dt_obl);end; end; uz=uC;
IL=x(7); twy(iijj)=t_kon; wy(1:in,iijj)=x;
czas=t_kon; poz=mod(czas,t_wyp_c)/t_wyp_c;
poz=poz-0.5;
Rf=1000; Lf=0.06*Rf; uz_fp=uz_f; prf=uz_f/Rf;
dprf=(uz-uz_fp)/Lf;
uz_f=uz_f+Rf*dprf*dtx;
[err,Cic_st]=wej_st_pm(uz_ref,uz_f,Cic_st,dt0);
pr_Im=30.0+err*5;
us_n=sin(w0t+faza+w0*t_wyp_c);
ef=abs(Esm*us_n); prL=abs(pr_Im*us_n);
pr7=x(7);
d_akt_n=((prL-pr7)/t_wyp_c-(ef-uz)/L)/((uz+1e-
1)/L);
ktore_p=ktore_n; ktore_n=fix(t_kon/t_wyp_c);
czas_st=t_kon-(t_wyp_c*ktore_n);
if (ktore_n~=ktore_p),
if (d_akt_n>0.95), d_akt_n=0.95; elseif
(d_akt_n<0.05), d_akt_n=0.05; end;
t_wla=(t_wyp_c*d_akt_n); end; if
(czas_st<t_wla), d_akt=1; else d_akt=0; end;
d=d_akt; t_pocz=t_kon;
wy(1+in:7+in,iijj)=[d;dt0;uz_f;err;pr_Im;us;uC]
; wyV(:,iijj)=V; i1000=1000;
ijkl=fix(iijj/i1000); if ((ijkl*i1000)==iijj),
[iijj/ik, dtx, lo, t_kon, x(7), x(8), Io, uz,
d, uz_f, err, pr_Im, Is], end;
end;
```

The obtained runs includes fig. 2.

The program that calculates transient states makes use of secret Euler method for the purpose. It is to apply nodal potential method. Independent nodal potentials for time which is the end of time step under consideration are calculated. Conduction and blockage state of diodes is tested at the beginning of time step. Check comes whether it is the same at the end of interval. If it is different then the time step is reduced to such value so that a diode (or transistor) conduction at the end of time step will be at the limit point between conduction and blockage. It should be noticed that inductance conductivity comes to Δt/L while capacity conductivity comes to C/Δt, where Δt is integration step. It turned out that circuit did not show vibration and the role of damping circuits was rather small.

III. Controlling of "Vienna" 3-phase PFC rectifier

The "Vienna" 3-phase rectifier was shown in fig. 3. It generates two rectified voltages *uz*1 , *uz*2 which have common node N. Despite possible different loads of these voltages *uz*1, *uz*2 by resistance *R*1, *R*2, their values should be equal. It requires the proper controlling of switching transistors T7, T14, T21 on. Controlling is also essential is case when determined output voltages *uz1_ref* and *uz2_ref* are higher than power conducting voltage.

Current that flow from the mains should be in the phase of proper phase voltages in the mains. In this way the circuit corrects power factor (Power Factors Correction). The circuit contains $nw = 12$ independent nodes, and $ig = 32$ branches whose numbers are marked in fig. 3. The quantity of unknowns x comes to $in = 32$. Branch currents and capacitor-accumulated charges make them. Except for capacitors C1, C2, on which useful rectified voltage *uz*1, *uz*2 is accumulated, series circuits were introduced like R147, C147 in order to avoid overvoltages and making operations easier for diodes and transistors. While switching over, the introduced current-circuit *i*29 plays a less role about it. Its aim is reducing the node voltage variation N. If power current it is of positive direction, then it would seem obvious, that it should boot charge *q* of capacitor C1. The assumed voltage *uz1_ref* on this output is, however, higher than maximal line-to-line power voltage.

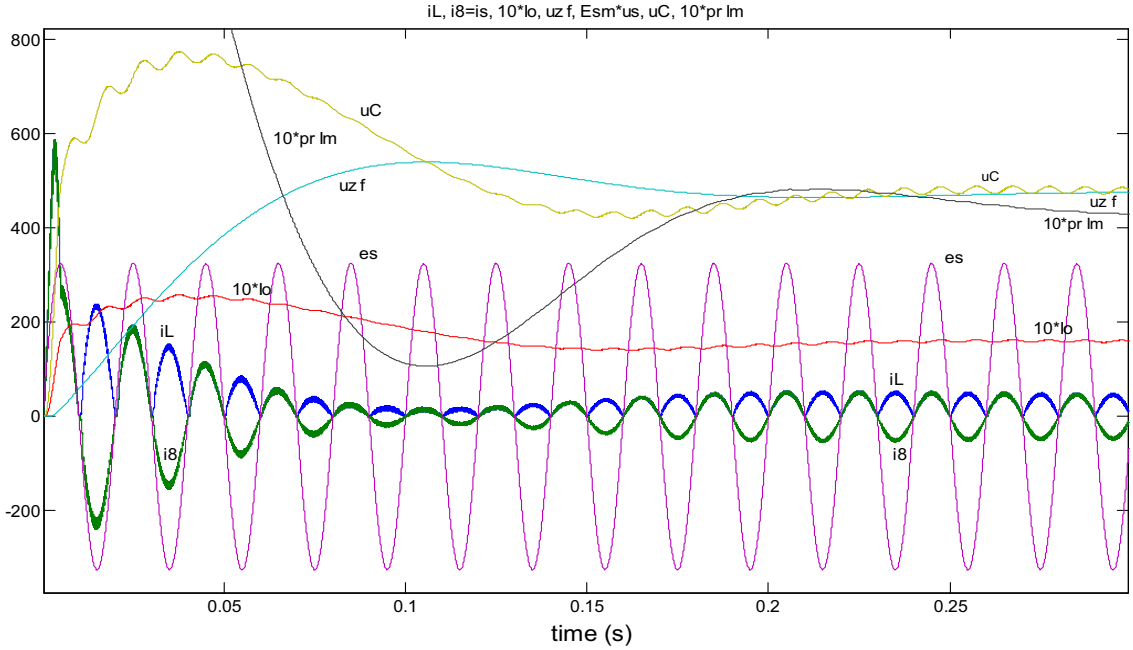

Fig.2. Feed voltage courses *es*, current *iL* flowing over inductance *L*, the current consumed from the mains *i*8, load current *Io*(*10), voltage across load *uC*, voltage filtered across load *uz_f* and controlling maximal value of current consumed from the mains *pr_Im* (*10) system from fig 1.

Therefore, transistors T7 should be turned on in cycles and the circuit should operate in the "Boost" system. After transistor T7 has been switched on by diodes and transistor D1, T7, D4, current *i*1 as current *iN* flows to capacitor C2 and boots voltage *uz*2. Therefore, the applied control system of turning transistors on at positive phase voltage value (then phase current should be positive also), turning transistors on adjusts to voltage value *uz*2. While at negative phase voltage value the way of turning transistors on is dependent on voltage quantity *uz*1. The way of controlling of "Vienna" 3-phase rectifier system is shown in fig. 4.

For each of 3 phases voltages $us = es/Esm$ is calculated, which has maximal value equals 1. Depending in this voltage sign *us* error (*uz1_ref* – *uz*1) or (*uz2_ref* – *uz2*) is used for controlling. This signal is passed over regulator PI (`wej_st()`), and next multiplied by voltage us. In this way phase current standard is obtained, which should flow from the mains and which is in power phase voltage-phase. It is compared with measured power current *im*, and hysteresis regulator (with hysteresis h) gives an initial signal to turn transistor dp on.

Transistor turn-on and off time cycle equals *t_wyp_c* was assumed. Transistor turn-on time *t_wyp_1* and its turn-off time (*t_wyp_c* – *t_wyp_1*) make up this cycles. The factor *wsp* determines a limiting relative transistors turn-on time within the cycle *t_wyp_c*. This factor is determinate according to theory of "Boost" system operations. Which is to guarantee the voltage *uz_ref* (=*uz_ref*1 or =*uz_ref*2 depending on the sign *us*), at present voltage *uz*(=*uz*1 or =*uz*2). The voltage *uz2_ref* is higher than maximal delta voltage value. Filling factor *wsp* is of auxiliary character, supporting hysteresis regulator and is calculated by the formula:

$$wsp0 = \frac{uz\_ref - 250}{uz\_ref} \quad ; \quad wsp\_ = \frac{uz\_ref - 250}{uz} \qquad (9)$$

$$wsp = wsp0 + 1.5 \cdot (wsp\_ - wsp0)$$

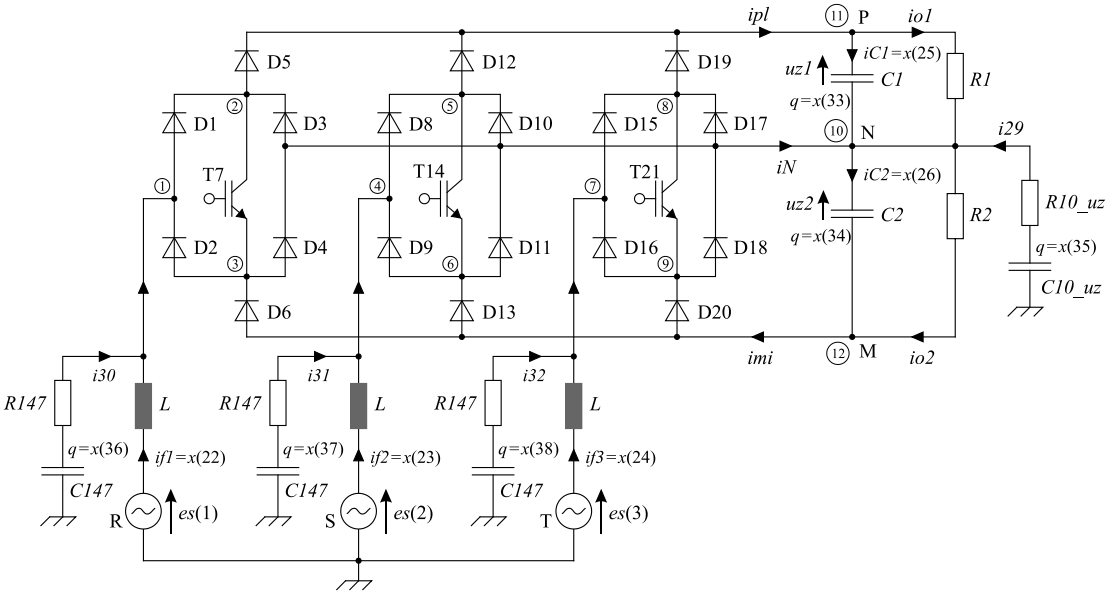

Fig.3. "Vienna" controllable 3-phase rectifier, generating two voltages DC, *uz*1, *uz*2, at equal value.

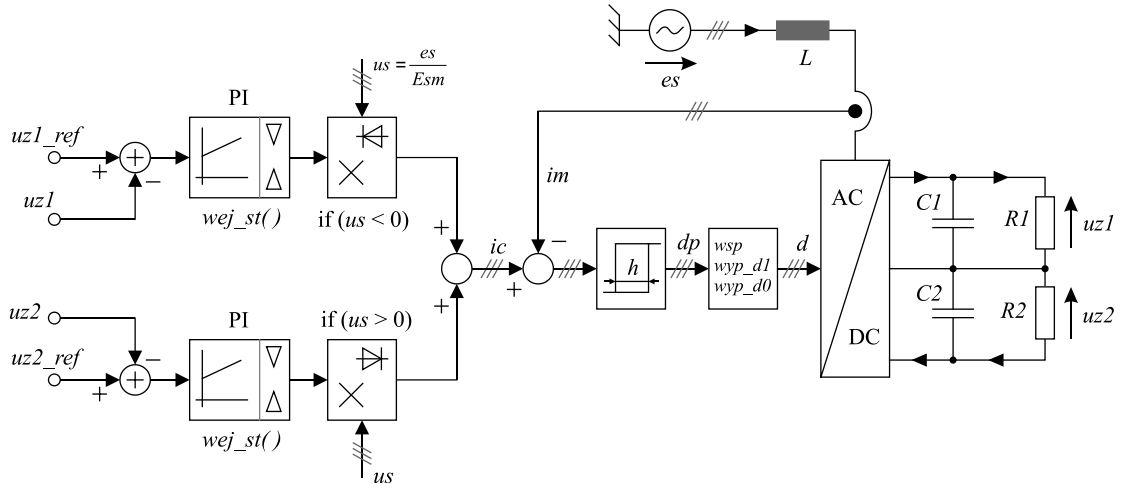

Fig.4. Controlling of turning transistors on T1, T7, T14 the system from fig. 3.

This formula corresponds to the way of "Boost" circuit operation but is of empirical character. The magnitude *uz*0 = 250 is assumed as effective supply voltage value. The program takes care that obtained transistor dp turn-on signal, obtained by hysteresis regulator should fulfil these time dependences determined by factor *wsp*. Transistor *d* turn-on signal equal 9 to signal *dp* as long as this turn-on time *wyp_d1* is lower than *t_wyp_1*. When turn-on time *dp* is higher than *t_wyp_1*, then value 0 is assumed for transistor *d* turn on indicator, until the end of cycle time *t_wyp_c*. It also should be noticed that for negative voltages *us*, its denial is assumed for signal *dp*.

The following program realizes the presented dependences:

```
nw=12; in=38; ifa=3;  x=zeros(in,1);
d_p=zeros(ifa,1); d=d_p; id=ifa*7;
us=zeros(ifa,1); Esm=230*sqrt(2);
przew=zeros(id,1); przew_p=przew; p_d=przew;
V=zeros(12,1); C1=1e-3; C2=1e-3; R1=35; R2=65;
w0=2*pi/0.02; pi23=2*pi/3; pi43=4*pi/3;
uz1_ref=400; uz2_ref=400; icm=0; Cicm=0;
icp=0; Cicp=0; wyp_d1=zeros(3,1);
wyp_d0=zeros(3,1); t_wyp_c=1.e-4;
t_wyp_1=(3/8)*t_wyp_c;
Rd=zeros(id,1); Ed=Rd; st_d=Ed; Ud=Ed; Rdn=Rd;
Udn=Ud; Edn=Ed;
iv=9+3; ig=32; pol=zeros(ig,iv);
Yv=zeros(iv,iv); Ev=zeros(iv,1); V=Ev;
Yg=zeros(ig,1); Eg=Yg;
pol(1,2)=1; pol(1,1)=-1; pol(2,1)=1; pol(2,3)=-
1; pol(3,2)=1; pol(3,10)=-1;
pol(4,10)=1; pol(4,3)=-1; pol(5,11)=1;
pol(5,2)=-1; pol(6,3)=1; pol(6,12)=-1;
pol(7,3)=1; pol(7,2)=-1;
pol(1+7,2+3)=1; pol(1+7,1+3)=-1;
pol(2+7,1+3)=1; pol(2+7,3+3)=-1;
pol(3+7,2+3)=1; pol(3+7,10)=-1;
pol(4+7,10)=1; pol(4+7,3+3)=-1; pol(5+7,11)=1;
pol(5+7,2+3)=-1; pol(6+7,3+3)=1; pol(6+7,12)=-
1;
pol(7+7,3+3)=1; pol(7+7,2+3)=-1;
pol(1+14,2+6)=1; pol(1+14,1+6)=-1;
pol(2+14,1+6)=1; pol(2+14,3+6)=-1;
pol(3+14,2+6)=1; pol(3+14,10)=-1;
pol(4+14,10)=1; pol(4+14,3+6)=-1;
pol(5+14,11)=1; pol(5+14,2+6)=-1;
pol(6+14,3+6)=1; pol(6+14,12)=-1;
pol(7+14,3+6)=1; pol(7+14,2+6)=-1; pol(22,1)=1;
pol(23,1+3)=1; pol(24,1+6)=1;
pol(25,10)=1; pol(25,11)=-1; pol(26,12)=1;
pol(26,10)=-1; pol(27,10)=1; pol(27,11)=-1;
pol(28,12)=1; pol(28,10)=-1; pol(29,10)=1;
pol(30,1)=1; pol(31,1+3)=1; pol(32,1+6)=1;
pol=pol';
for ii=1:id, st_d(ii)=1; end; for ii=1:ifa,
st_d(ii*7)=d(ii); end; dp=zeros(3,1); d=dp;
Ls=4*0.01e0;  Ls=0.015e0; Rs=w0*Ls/1000;
ik=6*300000; dt=1e-6; dt_m=dt*1e-3; dt_mx=dt_m;
dt0=dt_m;
wy=zeros(in+7,ik); twy=zeros(1,ik); t_pocz=0;
wyV=zeros(12,ik); logo=1;
for iijj=1:ik, dtx=dt; if (dt0<0.01*dtx),
dtx=dt*0.011; end;
if
((d_p(1)==0)&(d_p(2)==0)&(d_p(3)==0))&((d(1)==1
)&(d(2)==1)&(d(3)==1)),
dtx=dt*1e-5; end;
if
((d_p(1)==1)&(d_p(2)==1)&(d_p(3)==1))&((d(1)==0
)|(d(2)==0)|(d(3)==0)),
dtx=dt*1e-5; end;  if (dtx<dt_m); dtx=dt_m;
end;
d_p=d; dt_obl=dtx; x0=x; V0=V;
t_kon=t_pocz+dtx;  w0t=w0*t_kon;
us(1)=sin(w0t);  us(2)=sin(w0t-pi23);
us(3)=sin(w0t-pi43);
for ii=1:ifa, st_d(ii*7)=d(ii); end; %
transistor controlling
for jj=1:id,
[Ud(jj),Ed(jj),Rd(jj),U0,p0,przew_p(jj)]=diod(x
0(jj),st_d(jj)); end; Yd=1./Rd; uz1=x0(33)/C1;
uz2=x0(34)/C2; aa=dtx/C1; bb=dtx/C2;
R10_uz=1e3; C10_uz=1e-11; cc=dtx/C10_uz;
R147=1e1; C147=1e-7; dd=dtx/C147;
ee=1/(R147+dd);
Rss=(Rs+Ls/dtx); Ys=1/Rss;
Yg=[Yd;Ys;Ys;Ys;1/aa;1/bb;1/R1;1/R2;1/(R10_uz+c
c);ee;ee;ee]; Yc=diag(Yg); Yv=pol*Yc*pol';
u10_uz=x0(35)/C10_uz; uC147_1=x0(36)/C147;
uC147_4=x0(37)/C147; uC147_7=x0(38)/C147; Eg=[-
Ed;Esm*us(1);Esm*us(2);Esm*us(3);-uz1;-uz2;0;0;
-u10_uz;-uC147_1;-uC147_4;-uC147_7];
Eg(22:24)=Eg(22:24)+(Ls/dtx)*x0(22:24);
Ig_=Yg.*Eg; Iv=pol*Ig_; V=Yv\Iv; Eg=Eg-pol'*V;
Ig_=Yg.*Eg; x(1:ig)=Ig_;
io1=x(27); io2=x(28); VN=V(10); Vp=V(11);
Vm=V(12); iC1=(x(25)+x0(25))/2;
iC2=(x(26)+x0(26))/2; i29=(x(29)+x0(29))/2;
i30=(x(30)+x0(30))/2; i31=(x(31)+x0(31))/2;
i32=(x(32)+x0(32))/2;iC1=x(25); iC2=x(26);
i29=x(29); i30=x(30); i31=x(31); i32=x(32;
ipl=x(5)+x(5+7)+x(5+14);
imi=x(6)+x(6+7)+x(6+14); iN=ipl-imi;
x(33)=x0(33)+iC1*dtx; x(34)=x0(34)+iC2*dtx;
x(35)=x0(35)+i29*dtx; uz1=x(33)/C1;
uz2=x(34)/C2; u10_uz=x(35)/C10_uz;
x(36)=x(36)+i30*dtx; x(37)=x(37)+i31*dtx;
x(38)=x(38)+i32*dtx; uC147_1=x(36)/C147;
uC147_4=x(37)/C147; uC147_7=x(38)/C147;
lo=1;  dt0=dtx; for jj=1:id,
[Udn(jj),Edn(jj),Rdn(jj),U0,p0,przew_n(jj)]=dio
d(x(jj),st_d(jj));
lo1=(przew_n(jj)==przew_p(jj)); if (~lo1),
dty=dtx*abs((x0(jj)-p0)/(x0(ii)x(jj)));
if (dty>dt), dty=dt; end; if (dty<dt0),
dt0=dty; end; dt0=dt0*1.0000001;            if
(dt0<dt_m); dt0=dt_m; end; dt_mx=dt0; end;
lo=lo&lo1; end; lox=lo; if (lo==0);
dt0=dt0*1.0000001; t_kon=t_pocz+dt0; dtx=dt0;
x=x0+(x-x0)*(dt0/dt_obl); iC1=x(25); iC2=x(26);
i29=x(29); i30=x(30); i31=x(31); i32=x(32);
x(33)=x0(33)+iC1*dtx; x(34)=x0(34)+iC2*dtx;
x(35)=x0(35)+i29*dtx; uz1=x(33)/C1;
uz2=x(34)/C2; u10_uz=x(35)/C10_uz;
x(36)=x(36)+i30*dtx; x(37)=x(37)+i31*dtx;
x(38)=x(38)+i32*dtx; uC147_1=x(36)/C147;
uC147_4=x(37)/C147; uC147_7=x(38)/C147;
```

```
V=V0+(V-V0)*(dt0/dt_obl);  uz1=x(33)/C1;
uz2=x(34)/C2; end;
twy(iijj)=t_kon; wy(1:in,iijj)=x;
[icm,Cicm]=wej_st(uz1_ref,uz1,Cicm,dt0);
[icp,Cicp]=wej_st(uz2_ref,uz2,Cicp,dt0);
for ii=1:ifa, usi=us(ii); lo=(usi>=0); if (lo),
ic=icp*usi; else ic=icm*usi; end;
uz_ref=(uz1_ref+uz2_ref)/2; uz0=250;
wsp0=(uz_ref-uz0)/uz_ref;
wsp=wsp0; uz=(uz1+uz2)/2; if (lo),
uz_ref=uz2_ref; uz=uz2; else  uz_ref=uz1_ref;
uz=uz1; end; if (uz>250),
wsp_=wsp0*(uz_ref/uz); wsp=wsp+1.5*(wsp_-wsp);
end; if (wsp>0.92), wsp=0.92; end;
t_wyp_1=wsp*t_wyp_c; h=0.5; % histereza
im=x(21+ii); if  (im>(ic+h)), dp(ii)=0; elseif
(im<(ic-h)), dp(ii)=1; end;
if (lo), d(ii)=dp(ii); else d(ii)=mod(dp(ii)-
1,2); end;
if (d(ii)==1), wyp_d1(ii)=wyp_d1(ii)+dt0; end;
if (d(ii)==0), wyp_d0(ii)=wyp_d0(ii)+dt0; end;
if ((wyp_d1(ii)+wyp_d0(ii))*(1-
wsp)>wyp_d0(ii)),
if (wyp_d1(ii)>t_wyp_1), d(ii)=0; end; if
((wyp_d1(ii)+wyp_d0(ii))>t_wyp_c),
wyp_d1(ii)=0; wyp_d0(ii)=0; end; end; end;
t_pocz=t_kon; wy(1+in:7+in,iijj)=[d;dt0;us(1);
us(2);us(3)]; wyV(:,iijj)=V;
i1000=1000; ijkl=fix(iijj/i1000); if
((ijkl*i1000)==iijj), [iijj/ik, dtx, lox,
t_kon, uz1, uz2,d'], end;
if (iijj==fix(2.0*ik/3)), R2=R1; t_zm_R=t_kon;
end;
if (iijj==fix(2.5*ik/3)), uz1_ref=500;
uz2_ref=500; t_zm_u=t_kon; end;
end; [t_zm_R, t_zm_u],
```

The figures 5,6,7 show the obtained simulation results.

With calculations loading resistance $R1$=35 Ω, $R2$=65 Ω were assumed. For time $ti = 0.1925$ s comes equalization of loading $R2 = R1 = 35$ Ω. Given rectified voltage values $uz1\_ref = uz2\_ref = 500$ V. In fig. 6, you can see a good stabilization of rectified voltages at their some error in relation to given voltages. In fig. 5 you can see that phase angle of power currents coincides with phase angle of proper power phase voltages. Also the course of currents consumed from the mains resemble sinusoidal ones.

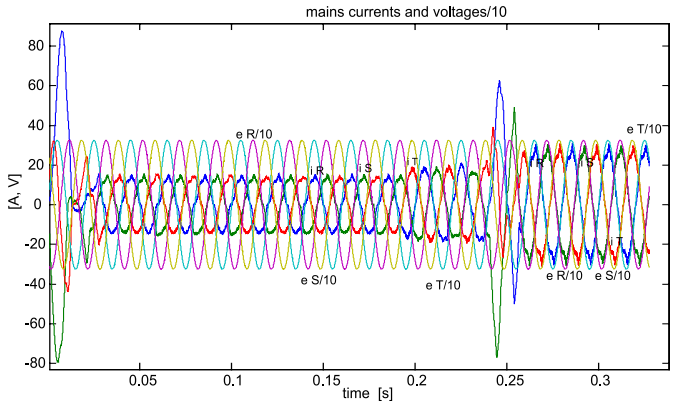

Fig. 5. Currents consumed from the mains and power phase voltages (/10) in time function of the circuit from fig. 3.

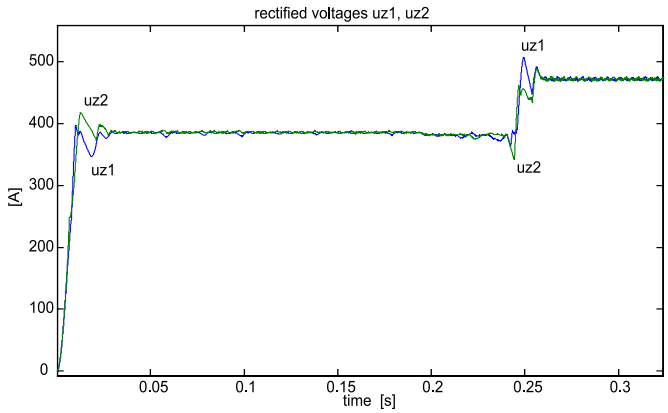

Fig.6. Course of rectified voltages *uz*1 and *uz*2 in time function of the circuit from fig. 3.

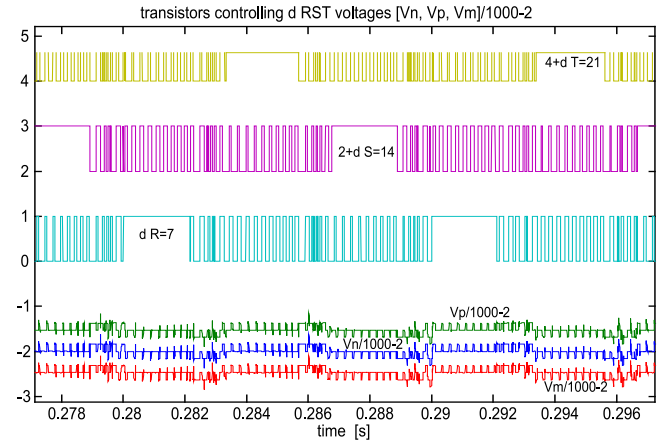

Fig.7. Course of controls d of transistor T7 transistor T14 (after adding 2) and transistor T21 (after adding 4) and potentials of modes 11(Vp), 10(Vn) and 12(Vm) (after dividing by 1000 and subtracting 2) of the circuit from fig. 3.

IV. Conclusions

The presented way of controlling of 1- and 3-phase rectifiers causes that current consumed from the mains is of shape resembles sinusoid and is in feed voltage-phase. Computer simulations proved effectiveness of the presented control. Therefore these circuits can be rated among Power Factor Correction group.

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Novel Bridgeless Power Factor Correction with Interleaved Boost Stages in Continuous Current Mode

(Topic: Power Electronics)

ABSTRACT

The operation and trade-off of Bridgeless Power Factor Correction (BPFC) with interleaved Boost stages are investigated. By using interleaved technology, an overall reduction of the sizes of Boost inductance and EMI filter are achieved without reducing system efficiency. Furthermore, the optimization design procedure of Boost inductor is given to improve system efficiency.

I INTRODUCTION

Bridgeless Power Factor Correction (BPFC) is a popular technique to achieve both unity power factor and high efficiency nowadays. Since this kind of PFC topologies have fewer semiconductors in the current flowing path comparing with conventional PFCs, higher efficiency can be reached. [1] gives a systematic comparison among five most popular BPFCs and a normal Boost PFC, the Two Boost Bridgeless PFC over performs all the other topologies by having reduced EMI without increasing semiconductor losses too much. Therefore, now the Two Boost BPFC is the new favorite of many PFC designers.

The main goal of this paper is to investigate the operation and design trade-offs of the Two Boost BPFC based on interleaved cells operating in continuous inductor current mode (CCM). It is shown that the application of interleaved Two Boost BPFC results in a dramatic overall size reduction of the boost inductors and differential mode (DM) EMI filter comparing with the traditional Two Boost BPFC with the same EMI requirement, without penalty of reducing the system efficiency. Furthermore, comparing the interleaved with non-interleaved Two Boost BPFC in the same Boost inductance, the pervious one has higher efficiency. Simulation and analysis results taken from a 350W interleaved BPFC are given. Experimental results from the hardware prototype will be shown in the final paper.

II SCHEMETIC AND OPERATING PRINCIPLES

Fig. 1 shows the schematic of the interleaved Two Boost BLPFC. The characteristic waveforms of the circuit are in Fig. 2. In the positive half line period, Boost inductor L_1, L_2, MOSs S_1, S_2 and Boost diodes D_1, D_2 work interleaved with D_5 returning current to V_{ac}. In the negative half line period, the converter works symmetrically. This topology can be expected to have higher efficiency than both Boost PFC and non-interleaved Two Boost BPFC, because: firstly, it doesn't need the freewheeling diodes rectifier and has one less semiconductor in current path than Boost PFC [1]; secondly, it uses multiple interleaved switching cells, which will significantly reduce the semiconductor and inductor losses than the non-interleaved one with the same inductance energy storage, due to the lower input current ripples.

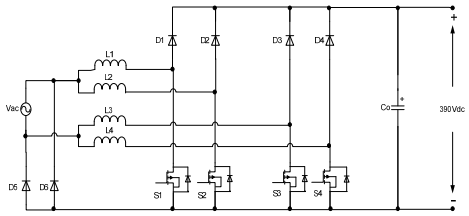

Figure 1: Interleaved Two Boost Bridgeless PFC

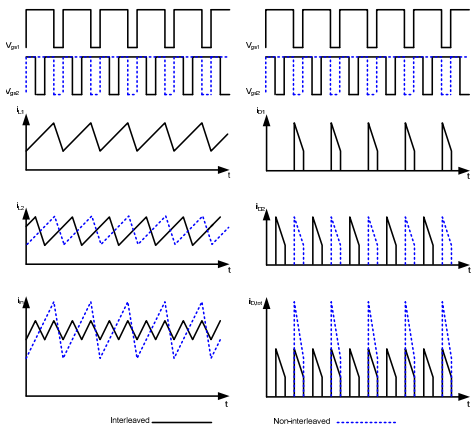

Figure 2: Switch states, inductor current and Boost diode current waveforms

III OPTIMIZATION DESIGN PROCEDURES OF BOOST INDUCTOR

Magnetic component is often the most important part of a power converter, and its performances mainly dominate the reliability and efficiency of a system. In Fig. 3, a flow chart of the developed procedure for optimizing the design variables of the Boost inductor for PFC systems is shown. Using this simple and effective method, a compromise

design between the size and losses of the inductor can be reached.

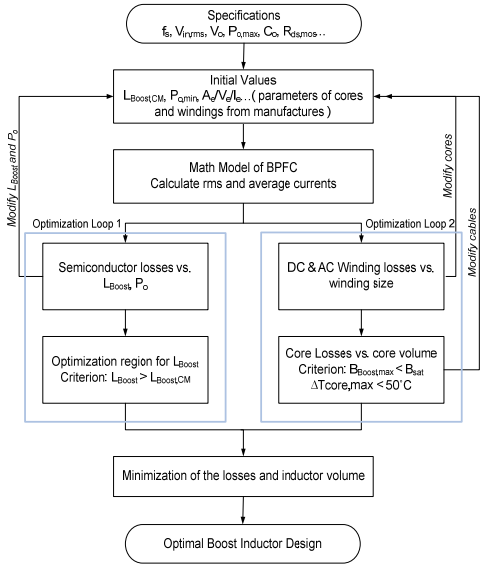

Figure 3: Flow chart of the optimization procedure of Boost inductor for trading off efficiency and power density

IV PERFORMANCES COMPARASION

In order to compare the system efficiency in the interleaved and non-interleaved Two Boost BPFC converters, it will be interesting to know the different currents of them. Paper [2] and [3] gave the detailed method for calculating various current in semiconductors of PFC converters.

When output is 350W, according to the system parameters as below:

$V_{in,rms} = 220V \quad L_1 = L_2 = L_3 = L_4 = 1.25mH$

$V_o = 390V \quad I_o = 0.9A \quad f_s = 65kHz \quad f_{line} = 50Hz$

Table I gives the inductances' volumes, the MOS, Boost diode, return diode, inductor RMS currents and the RMS high-frequency (HF) line currents for the two stages interleaved Two Boost BPFC, non-interleaved Two Boost BPFC with equal energy storage and non-interleaved Two Boost BPFC with equal HF RMS current. In order to clear the calculation, except the inductances' volumes, **all the parameters have been normalized** which is the same as what had been done in reference [3]. To get a fair comparison, **I assume that there are 2 MOSs and 2 Boost diodes paralleled in each Boost cell of non-interleaved BPFCs**.

From Table I, it is obvious to find out that:

1. With the same energy storage inductor, the HF RMS line current of the non-interleaved BPFC is 3.84 times greater than that of the interleaved BPFC, which means that: the EMI filter of non-interleaved BPFC must provide 11.69dB higher attenuation at switching frequency than interleaved BPFC. This will increase the size of the EMI filter.
2. With equal HF RMS line current, the inductance of the non-interleaved BPFC is 1.98 times greater than what in interleaved BPFC. If the size of inductor has been optimized, this means one can not enlarge the inductance by increasing the turns, higher inductance will certainly lead a higher inductor volume. Using the procedure in section III, the result shows that the optimized size of each inductor in non-interleaved BPFC with equal HF current is almost 1.6 times larger than the interleaved BPFC.
3. With equal HF RMS line current, the MOSs conduction losses of the interleaved BPFC is only 1.04 times larger than the non-interleaved PFC. Furthermore, the losses differences of other semiconductors are very small as well. That means interleaving stages will not increase the conduction losses in semiconductors.

Table I. Boost inductances' volumes, normalized inductances and RMS currents in different BPFC topologies

PFC topologies	Interleaved BPFC (Case1)	Non-interleaved with equal energy storage (Case 2)	Non-interleaved with equal HF RMS current (Case 3)
Boost inductance	0.187	0.094	0.370
MOS current	0.514	0.525	0.504
Boost Diode current	0.738	0.742	0.730
Return Diode current	1.774	1.817	1.774
Inductor current	0.899	1.818	1.774
HF line current	0.270	1.037	0.270
Inductances' volume	6.66cm^3	21.3cm^3	10.5cm^3

It would also be nice to point out that: although paper [4] has presented that the more interleaved stages, the larger range of duty ratios experiencing near-total input current ripple cancellation and the more operating points yielding to complete cancellation; unless it is really necessary for it, by increasing the number of stages, we will quickly enlarge the size of the whole system, then the limited reduction of magnetic and filter volumes may go away. On the other hand, increasing interleaved stages will be accompanied with increasing circuit complexity and cost, and reducing system reliability as well.

V SIMULATION RESULTS

According to the system parameters shown in section IV, simulate the BPFCs without input filters at 350W and 220V input. Fig. 4 gives the line voltage and current of the interleaved BPFC. Fig.5 shows the input current ripple of both interleaved BPFC and non-interleaved BPFC with equal energy storage in one line period.

After carefully choosing the components, Fig. 6 shows the system efficiency comparison of three BPFCs in Table I, when input voltage is changing from 85V to 265V. Where, MOSs are SPW47N60C3 from Infineon; Boost diodes are implemented with IDT04S60C SiC diode from Infineon; and diodes 1N5406 from Multicomp are used as the return diodes. The Magnetics cores for the Boost inductors *L* are 77894A7HT19 (volume: 6.66cm^3) in interleaved BPFC in case 1, 77439A7 (volume: 21.3cm^3) in non-interleaved BPFC in case 2 and 77083-A7 (volume: 10.5cm^3) for non-interleaved BPFC in case 3. A magnet wire (AWG#19) was used for winding. It should be noted that: although the BPFC in case 2 has lower inductance, it helps nothing to reduce the core size. The reason is: large current ripples increase core losses and temperature rising significantly. Finally, the high voltage aluminum capacitor (270μF, 400VDC) is used for bulk capacitor.

In Fig. 6, it can be seen that the interleaved Two Boost BPFC has higher efficiency comparing with the non-interleaved equal energy storage one because of its lower current ripple. And comparing with the non-interleaved equal HF current BPFC, the interleaved one almost has the same efficiency. And with the voltage increasing, the efficiency difference becomes smaller due to the current reduction.

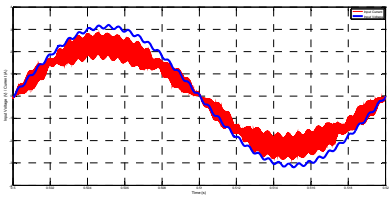

Figure 4: Input voltage (blue 100V/div), input current (red 1A/div) of the interleaved BPFC

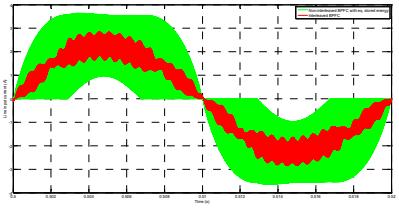

Figure 5: Input current ripple of interleaved BPFC (red), non-interleaved BPFC equals energy storage (green)

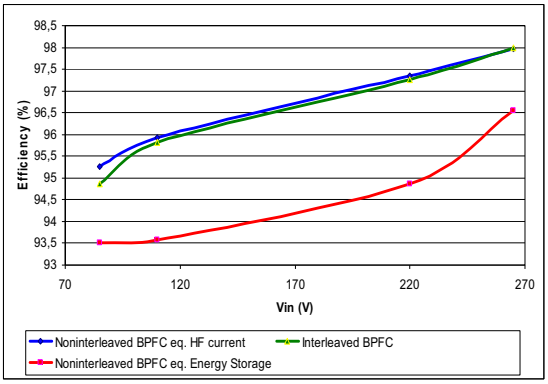

Figure 6: Efficiency comparison for three BPFCs in Table I

VI CONCLUSIONS

Interleaving BLPFC is a useful novel topology, which can increase system efficiency and power density by reducing the size of Boost inductors and EMI filter. With the properly designing of the magnetic components in the interleaved BPFC converter, a trade off between efficiency and power density can be achieved.

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Modeling of non-ideal Improved Switched Inductor (SL) Z-source Inverter

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Abstract- **Recently switching inductor Z-source inverter topology has been proposed to increase the boost factor. But the problem of stress on switch and capacitor is still remaining; hence an improved switched capacitor has been proposed to decrease the capacitor voltage stress. To design the control for this topology the transfer function is used. This paper presents the small signal analysis of the new topology; where, the state space averaging method is employed to achieve the transfer functions.**

Keywords: *state space averaging method, small signal model, switched inductors Z-source inverter.*

I. INTRODUCTION

Since Z-source inverters has proposed in 2002 as a novel topology to achieve the buck and boost functions, to decrease the current impact and to reduce the grid current harmonics [1]. On the other side, this topology has allowed to overcome the problem of the short circuit between the upper and lower switches of the same leg. Compared with the traditional inverter (VSI), two capacitors and two inductors was added to form an 'X' shape in the input side of the inverter as it is shown in Fig. 1.

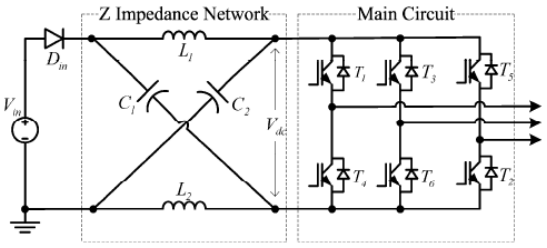


Fig. 1. Classical Z-Source inverter.

The boost factor B of the voltage across the DC- Link bus is expressed as follows [1]:

$$B = \frac{V_{dc}}{V_{in}} = \frac{1}{1-\frac{2T_0}{T}} = \frac{1}{1-2D} \qquad (1)$$

Where: T_0 is the interval of the shoot-through zero state during a switching cycle T. D is the duty ratio which is equal to T_0/T. This topology presented a major drawback of a large capacitor voltage stress; therefore, this topology was improved to overcome this main problem [2]. Indeed, the improved topology had exactly the same components as the previous topology, whereas, the network impedance is moved to be placed after the inverter as shown in Fig. 2

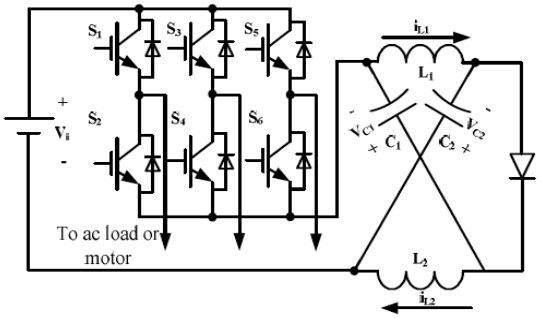


Fig.2 Improved Z-source Inverter

Recently, the Z-source topology has been greatly explored from various aspects [3-10], where a new topology was proposed in [11] to increase the boost factor by using an additional inductors and diodes as shown in Fig. 3. The following expression can be deduced:

$$V_{dc} = \frac{1+D}{1-3D} = B \cdot V_{in} \qquad (2)$$

Hence, the boost factor can be expressed as follows:

$$B = \frac{1+D}{1-3D} = \frac{1+\frac{T_0}{T}}{1-\frac{3T_0}{T}} \qquad (3)$$

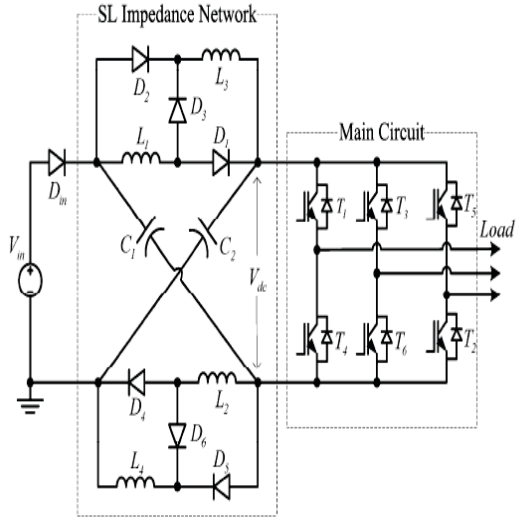


Fig. 3. Topology of proposed SL Z-source inverter

This topology is improved once more in the present work, where the main aim is to avoid the problem which was faced in the first topology by the minimization of the voltage capacitor stress, this idea is based on moving the SL Z-source to be placed after the inverter Fig 4. As it is shown clearly this new topology is different from that presented in Fig. 2.

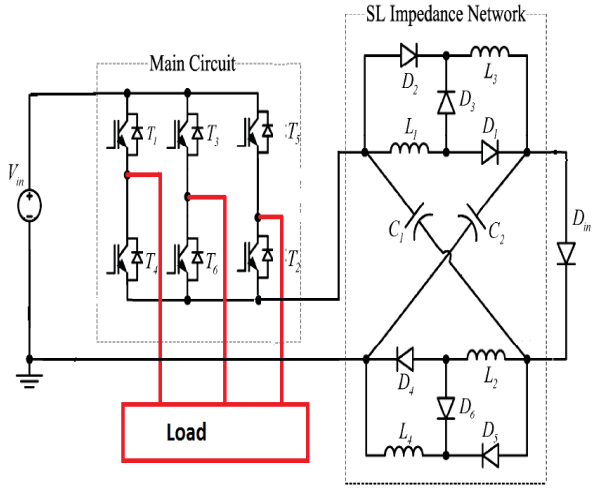


Fig. 4 Improved SL Z-source

II. STATE SPACE AVERAGING OF IMPROVED SL Z-SOURCE INVERTER

On the other hand, the small signal model of the non ideal improved SL Z-source inverter is investigated to obtain the transfer function, where the equivalent circuit of the improved SL Z-source presented in Fig 5 is used under the following assumptions:

1- Improved SL Z-source operates in continuous conduction mode CCM.

2- $L_1 = L_2 = L_3 = L_4 = L$; $C_1 = C_2 = C$

$r_{L1} = r_{L2} = r_{L3} = r_{L4} = r_L$; $r_{C1} = r_{C2} = r_C$.

3- Because of the Symmetry of the inductors and the capacitors the following relations can be deduced :

$V_{01} = V_{02} = V_0$, $V_{L1} = V_{L2} = V_{L3} = V_{L4} = V_L$

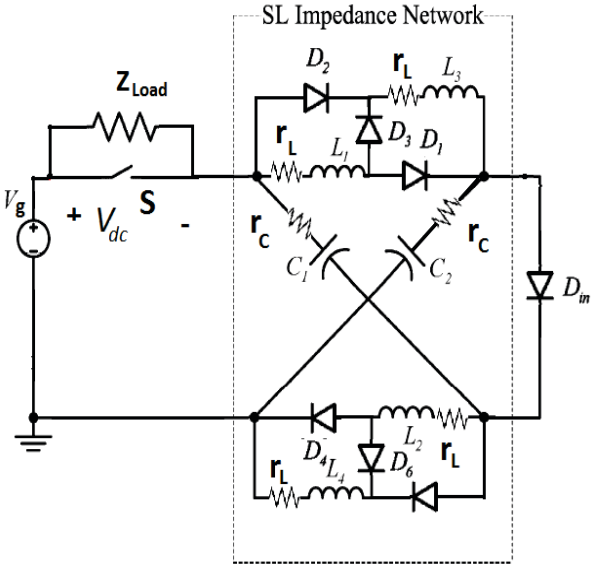


Fig. 5 Non ideal equivalent improved SL Z-source

A- *Shoot-through state*

The shoot-through actions of the top and bottom arms of the main circuit, and its equivalent circuit are shown in Fig. 6(a). When the switch S is on, the different states of the diodes D_{in} , D_1 , D_2 , D_3 , D_4 , D_5 and D_6 are presented in Tab. I, it is obvious that when the two diodes D_1 and D_2 are turned on the inductors L_1 and L_3 are charged, and the diode D_3 is turned off. On the other side when the two diodes D_4 and D_5 are turned on the inductors L_2 and L_4 are charged, and the diode D6 is turned off, In this case the diode D_{in} remains turned off.
The state equation of shoot-through mode can be written in the space form:

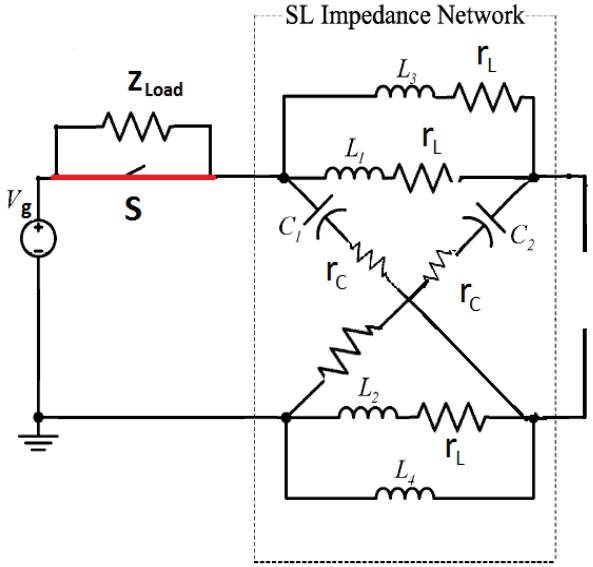
$$\dot{x} = A_1.x + B_1.u \qquad (4)$$

$$\begin{bmatrix} L\frac{di_{L1}}{dt} \\ L\frac{di_{L2}}{dt} \\ C\frac{dv_{C1}}{dt} \\ C\frac{dv_{C2}}{dt} \end{bmatrix} = \begin{bmatrix} (2r_C \quad r_L) & 0 & 0 & 1 \\ 0 & (2r_C \quad r_L) & 1 & 0 \\ 0 & 2 & 0 & 0 \\ 2 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix} + \begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \end{bmatrix} V_g \qquad (5)$$

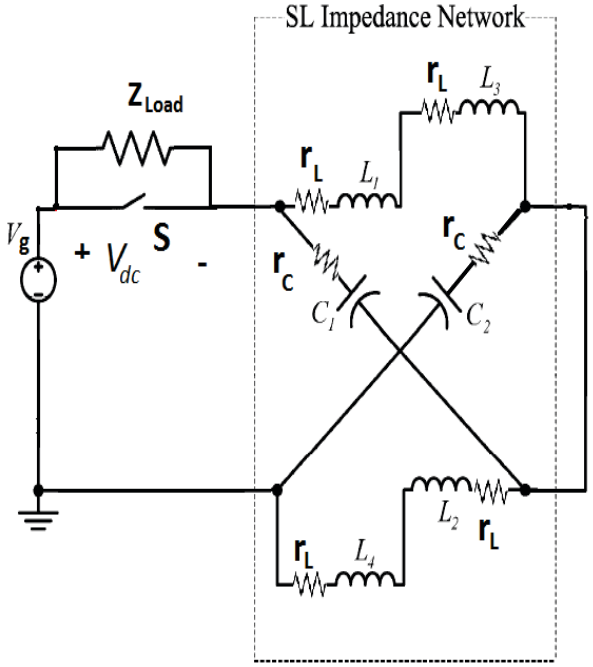
Where:

$$A_1 = \begin{bmatrix} (2r_C - r_L) & 0 & 0 & 1 \\ 0 & (2r_C - r_L) & 1 & 0 \\ 0 & -2 & 0 & 0 \\ -2 & 0 & 0 & 0 \end{bmatrix}, x = \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} V_g \\ V_g \\ 0 \\ 0 \end{bmatrix}, \dot{x} = \begin{bmatrix} L\frac{di_{L1}}{dt} \\ L\frac{di_{L2}}{dt} \\ C\frac{dv_{C1}}{dt} \\ C\frac{dv_{C2}}{dt} \end{bmatrix}$$



(a) Shoot-Through State



(a) Non-shoot-through state

Fig. 6 Equivalent circuit of improved SL Z-source inverter.
(a) Shoot-through state. (b) Non-shoot-through state.

B- NON-SHOOT-THROUGH STATE

Equivalent circuit of this mode is shown in Fig. 6(b). When the switch S is off, the different states of the diodes D_{in} , D_1 , D_2 , D_3 , D_4 , D_5 and D_6 are presented in Tab. I. As the two diodes D_1 and D_2 are turned off and D_3 is turned on, this makes the two inductors L_1 and L_3 to be connected in series. On the other side when the two diodes D_4 and D_5 are turned off and the diode D_6 is turned on the two inductors L_2 and L_4 are connected in series, In this case the diode D_{in} remains turned on.

TABLE 1
THE DIFFERENT STATES OF THE DIODES FUNCTION OF S STATE.

S	D_{in}	D_1	D_2	D_3	D_4	D_5	D_6
on	off	on	on	off	on	on	off
off	on	off	off	on	off	off	on

The state equation of non shoot-through mode can be written in the space form:

$$\dot{x} = A_2.x + B_2.u \quad (6)$$

$$\begin{bmatrix} L\frac{di_{L1}}{dt} \\ L\frac{di_{L2}}{dt} \\ C\frac{dv_{C1}}{dt} \\ C\frac{dv_{C2}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{(r_C+2r_L)}{2} & 0 & 0 & -\frac{1}{2} \\ 0 & -\frac{(r_C+2r_L)}{2} & -\frac{1}{2} & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix} + \begin{bmatrix} \frac{I_o(r_C)}{2} \\ \frac{I_o(r_C)}{2} \\ I_o \\ I_o \end{bmatrix} \quad (7)$$

Where:

$$A_2 = \begin{bmatrix} -\frac{(r_C+2r_L)}{2} & 0 & 0 & -\frac{1}{2} \\ 0 & -\frac{(r_C+2r_L)}{2} & -\frac{1}{2} & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix}$$

$$B_2 = \begin{bmatrix} \frac{I_o(r_C)}{2} \\ \frac{I_o(r_C)}{2} \\ I_o \\ I_o \end{bmatrix}$$

An average model for improved SL Z-source can be written as:

$$\begin{bmatrix} L\frac{di_{L1}}{dt} \\ L\frac{di_{L2}}{dt} \\ C\frac{dv_{C1}}{dt} \\ C\frac{dv_{C2}}{dt} \end{bmatrix} = A \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{C2} \end{bmatrix} + \begin{bmatrix} DV_g + 0.5DI_o(r_C) \\ DV_g + 0.5DI_o(r_C) \\ DI_o \\ DI_o \end{bmatrix} \quad (8)$$

Where

$$A = \begin{bmatrix} \frac{(5D-1)r_C - 2r_L}{2} & 0 & 0 & \frac{(3D-1)}{2} \\ 0 & \frac{(5D-1)r_C - 2r_L}{2} & \frac{(3D-1)}{2} & 0 \\ D' & -2D & 0 & 0 \\ -2D & D' & 0 & 0 \end{bmatrix}$$

The DC state equation is:

$$\begin{bmatrix} \frac{(5D-1)r_C - 2r_L}{2} & 0 & 0 & \frac{(3D-1)}{2} \\ 0 & \frac{(5D-1)r_C - 2r_L}{2} & \frac{(3D-1)}{2} & 0 \\ D' & -2D & 0 & 0 \\ -2D & D' & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C1} \\ V_{C2} \end{bmatrix} + \begin{bmatrix} DV_g + 0.5D'I_o(r_C) \\ DV_g + 0.5D'I_o(r_C) \\ D'I_o \\ D'I_o \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (9)$$

Where

$I_{L1}, I_{L2}, V_{C1}, V_{C2}, V_g$ are DC steady state values. Due to the similarty , simplification was done by applying the following simplications : $I_{L1} = I_{L2} = I_L$ and $V_{C1} = V_{C2} = V_C$

The AC state equation becomes

$$\begin{bmatrix} L\frac{d\hat{i}_{L1}}{dt} \\ L\frac{d\hat{i}_{L2}}{dt} \\ C\frac{d\hat{v}_{C1}}{dt} \\ C\frac{d\hat{v}_{C2}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{(5D-1)r_C - 2r_L}{2} & 0 & 0 & \frac{(3D-1)}{2} \\ 0 & \frac{(5D-1)r_C - 2r_L}{2} & \frac{(1+D)}{2} & 0 \\ D' & -2D & 0 & 0 \\ -2D & D' & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{v}_{C1} \\ \hat{v}_{C2} \end{bmatrix} + \begin{bmatrix} (2.5r_C - r_L)I_{L1} + 1.5V_{C2} + V_g - 0.5I_o r_C \\ (2.5r_C - r_L)I_{L1} + 1.5V_{C2} + V_g - 0.5I_o r_C \\ I_o - 3I_L \\ I_o - 3I_L \end{bmatrix} \hat{d}(s) \quad (10)$$

From (9) and (10) the Laplace transformation is used to obtain the following expressions:

$$i_{L1}(s) = \frac{(3D-1)v_{C2}(s) + K_1 d(s)}{(2sL - (5D-1)r_C + 2r_L)} \quad (11)$$

$$i_{L2}(s) = \frac{(3D-1)v_{C1}(s) + K_1 d(s)}{(2sL - (5D-1)r_C + 2r_L)} \quad (12)$$

Where:

$$K_1 = \left((5r_C - 2r_L)I_{L1} + 3V_{C2} + 2V_g - I_o r_C\right)$$

$$v_{C1}(s) = \frac{1}{Cs}\left(D'i_{L1}(s) - 2Di_{L2}(s) + (I_o - 3I_L)d(s)\right) \quad (13)$$

$$v_{C2}(s) = \frac{1}{Cs}\left(-2D'i_{L1}(s) + D'i_{L2}(s) + (I_o - 3I_L)d(s)\right) \quad (14)$$

It is supposed that the two capacitors have the same voltage due to their similarity, hence:

$$v_C(s) = v_{C1}(s) = v_{C2}(s)$$

From (11)-(14) the voltage $v_C(s)$ satisfies the following expression:

$$\frac{v_C(s)}{d(s)} = \frac{sb_1 + b_0}{a_2 s^2 + a_1 s + a_0} \quad (15)$$

Where:

$$b_1 = \left(2L(I_o - 3I_L)\right)$$
$$b_0 = \left(K_1(1-3D)\right) + \left(I_o - 3I_L\right)\left((1-5D)r_C + 2r_L\right)$$
$$a_2 = 2CL\,;\; a_1 = \left(2r_L - (5D-1)r_C\right)\,;\; a_0 = (1-3D)^2$$

It is possible to present the RHP of (15) by noting that during voltage boost I_L is large than I_o which makes the first term in the numerator of (15) negative.

TABLE 2

Z- SOURCE INVERTER PARAMETER

Parameter	Value
V_g	36V
I_{Load}	10A
C	0.8mF
L	1mH
r_C	0.03Ω
r_L	0.05Ω
D	0.3

From (9), the following expressions can be deduced:

$$I_L = \frac{D'}{1-3D} I_o \quad (16)$$

$$\left((5D-1)r_C - 2r_L\right)I_L + (3D-1)V_C + 2DV_g + D' I_o r_C = 0 \quad (17)$$

From (16) and (17) and taking into account the values presented in Tab. 2, the values of I_L and V_C can be calculated:

$$I_L = 70\ A\ ,\ V_C = 217.25\ V$$

Figure 7 presents the bode diagram of the inverter according parameters presented in Tab. 2 and based on (15).

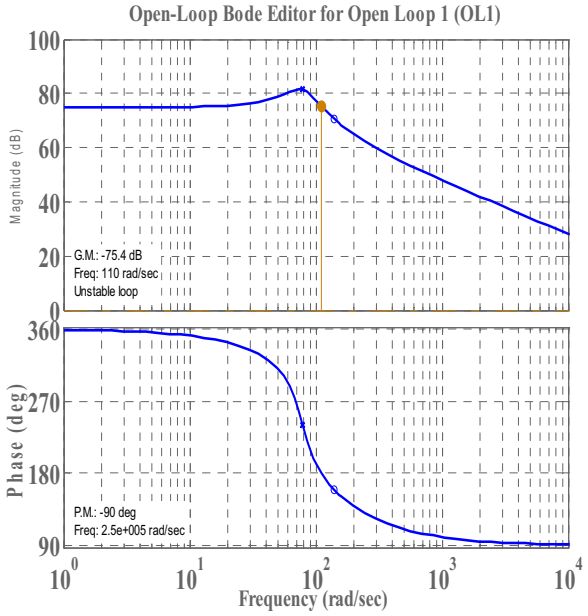


Fig. 7 Bode plot of transfer function

As it is shown in Fig. 8 when the capacitance value in X-shape network varies from $0.2\ mF$ to $1\ mF$ the poles are shifted toward the real axis and the system settling time is increased while the right hand zero is kept constant .
From (15) the quality factor is presented as follows:

$$Q = \frac{\left(\sqrt{2LC}\right)^{1.5}}{(1-3D)(5D-1)r_C} \quad (18)$$

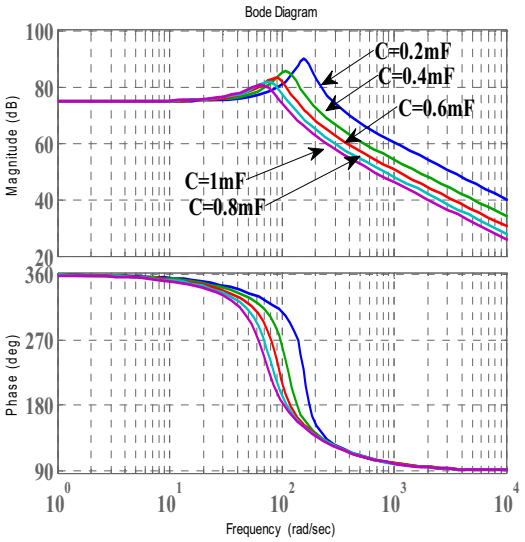


Fig. 8. Bode plot of transfer functionwith different capacitances

It is obvious in Fig. 9 that the Q factor increases with the increase of the inductance value from $0.5\ mH$ to $5\ mH$, whereas the capacitance is kept constant (C = 0.8mF).

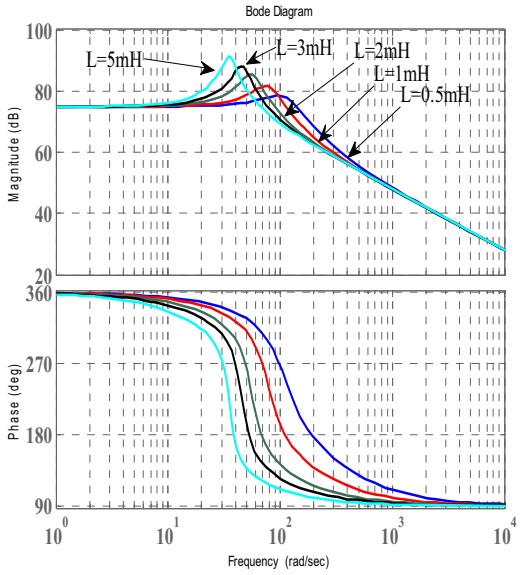


Fig. 9. Bode plot of transfer functionwith different inductors

III. CONCLUSION

In this paper, a complete AC small signal analysis model of an improved SL Z- source inverter is presented. The state space averaging method is applied taking into account the parasitic elements of the capacitors and the inductors, where the transfer function and the small signal model are derived. The right hand plane zero (RHP)of bode diagram obtained from the transfer function cannot be placed away by adjusting the parameters in the proposed topology, on the other hand the value of the RHP can be reduced by choosing a small inductance. The main perspective of the present work is the use of the closed loop case to improve the responses of the system.

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