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BOOTSTRAPPED LOW-VOLTAGE ANALOG SWITCHES

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ABSTRACT

Novel low-voltage constant-impedance analog switch circuits are proposed. The switch element is a single MOSFET, and constant-impedance operation is obtained using simple circuits to adjust the gate and bulk voltages relative to the switched signal. Low-voltage (1-volt) operation is made feasible by employing a feedback loop. The gate oxide will not be subject to voltages exceeding the supply voltage difference.

Realistic switches have been simulated with HSPICE. The simulations show that the switch circuits operate very well, even when the supply voltage approaches the technology's threshold voltage.

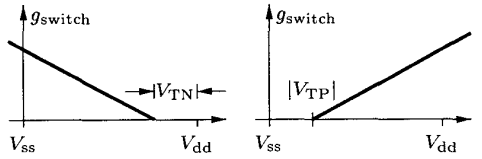
1. INTRODUCTION

Technology constraints and battery-powered operation require that low-voltage analog circuits be designed. Whereas low-voltage operation is associated with many advantages for digital circuits, it generally complicates the design of analog circuits. When the supply voltage is lowered, not only does it become increasingly difficult to maintain the same (high) level of SNDR performance, but even the functionality of the circuit may be hard to preserve.

High-performance analog circuits are usually implemented as discrete-time circuits, often as switched-capacitor (SC) circuits. The design of analog switches which conduct reliably in the rail-to-rail range is the main difficulty in the design of low-voltage SC circuits. Switched-opamp and other dedicated low-voltage SC circuit techniques that avoid the need for rail-to-rail switching have been proposed [1, 2]. Although such techniques are useful and commercially utilized, it should be understood that they represent a tradeoff with respect to speed, power consumption, and design flexibility. This paper describes simple circuits that implement the rail-to-rail switching function, thereby facilitating the implementation of general low-voltage SC circuits.

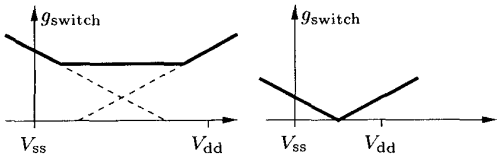
2. MOSFET-BASED ANALOG SWITCHES

A MOSFET in itself can be used as an analog switch. The drain and source terminals are the two switch terminals, and the gate and bulk[1] terminals are used to control the conductivity of the channel between the two switch terminals. Unfortunately, the MOSFET switch's conductivity depends not on the absolute potential of the control terminals, but on their potentials relative to the conductive channel's potential. Despite of this property, MOSFET switches are, for simplicity, often controlled by CMOS-logic clock signals having fixed potentials in the on and off states. The conductance of such a MOSFET switch is strongly signal-dependent (Fig. 1). An NMOS and a PMOS switch can be used in parallel to form a transmission-gate switch having a region where the conductance is approximately signal-independent. However, when the supply voltage is lower than the sum of the two transistors' threshold voltages (absolute values), this region not only vanishes, but is replaced by a region (in the middle of the supply-voltage range) where the switch does not conduct reliably (Fig. 2).



(a) NMOS (b) PMOS

Figure 1: On-state conductance of the single-MOSFET switch vs. the potential of the switched signal. The switches are controlled by CMOS-logic signals.



(a) 3-V supply voltage (b) 1.5-V supply voltage

Figure 2: On-state conductance of the transmission-gate switch.

2.1. Low-Voltage Operation

If the supply voltage is low (say, 1.2 volts) and low-threshold-voltage MOSFETs (which are subject to leakage problems) are not available, rail-to-rail switching operation requires that control signals exceeding the supply-voltage range be generated. Clock-signal doublers have been proposed [3], but in a single-well technology they can be used only for MOSFETs of one type[2]; hence

[1] Occasionally, the bulk terminal is called the *back-gate* terminal. For single-well technologies, the bulk may be the substrate, in which case it cannot be controlled separately for each MOSFET.

[2] In a P-well technology, doubled clock signals can be generated only for NMOS switches. The problem is related to the forward-biasing of PN

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the switch conductance will be strongly signal-dependent. Another disadvantage is that the gate oxide will be subject to voltages of up to twice the supply-voltage difference, which may cause hot-electron effects and possibly permanent breakdown of the gate oxide.

3. BOOTSTRAPPED SWITCH

To obtain constant-conductance operation the gate-to-channel voltage should preferably be held constant during the on state. This can be obtained using a bootstrap technique (Fig. 3). The technique is discussed in Section 11.3 in [4], but a circuit realization is unfortunately not provided.

In the off state $\overline{\Phi}$ the bootstrap capacitor C_b is charged to the supply-voltage difference, and ideally it will act as a floating battery in the on state Φ. The NMOS switch N0 will be non-conducting in the off state because sw3 connects the gate terminal to the low supply potential V_{ss}. In the on state, the switches sw1 and sw2 connect the fully-charged bootstrap capacitor C_b between N0's gate and source terminals. Assuming that the stray capacitance loading of C_b is small, N0's overdrive will be nearly constant and the switch's on-state conductance will be approximately (neglecting the body effect and the stray load of C_b)

$$g_{\text{switch}} = \mu C_{\text{ox}} \frac{W}{L}(V_{\text{dd}} - V_{\text{ss}} - V_{\text{TN}}) \qquad (1)$$

Hence, if $V_{\text{dd}} - V_{\text{ss}} > V_{\text{TN}}$, the bootstrapped switch will conduct in the entire supply-voltage range, and its conductance will be nearly signal-independent. Clearly, the difficulty lies in the implementation of the internal switches, particularly (but not exclusively) sw1 which must also be able to conduct in the rail-to-rail range.

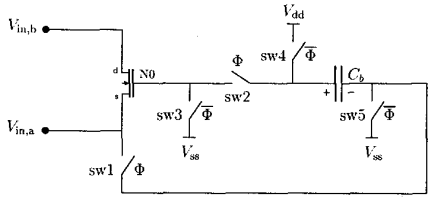

Figure 3: Bootstrapped switch: fundamental principle.

3.1. Simple Implementation

Fig. 4 shows a simple implementation of the bootstrapped switch, where sw1 is implemented as a bootstrapped NMOS switch N1. The main difference between N1 and N0 is that N1's source terminal is connected to V_{ss} in the off state, whereas the switch terminals, $V_{\text{in,a}}$ and $V_{\text{in,b}}$ are floating[3].

Switches sw3 and sw5 implement trivial switching functions, hence they are implemented as simple NMOS switches N3 and N5. At first sight, the design of sw4 may also appear to be trivial, but this is not the case. Unfortunately, sw4 cannot be implemented as a simple PMOS switch controlled by CMOS logic because it would leak during Φ when the bootstrap capacitor provides a potential that exceeds V_{dd}[4]. Instead, sw4 may be implemented as an NMOS switch N4, which is controlled by a level-shifted clock signal having levels V_{dd} and $2V_{\text{dd}}$ (assuming $V_{\text{ss}} = 0$). The level shifter is based on the widely-used Nakagome charge pump [5].

As illustrated, sw2 can be implemented as a simple PMOS switch P2. Because P2's channel potential will exceed V_{dd} in the on state Φ, it is necessary to bias its bulk terminal to a voltage which is at least as high as that provided by the bootstrap capacitor. A simple option is to connect the bulk terminal to the source terminal (as shown), but it may be better to connect it to $2V_{\text{dd}}$ which can be generated using the level shifter and a few extra transistors (traditional voltage doubler, not shown)[5]. The biased-well PMOS implementation of sw2 is a considerable drawback for the circuit because it implies that N0 cannot be implemented in a separate well (using a single-well technology); consequently, N0 cannot be compensated for the body effect. Unfortunately, sw2 cannot be designed as an NMOS switch because that would require that large clock signals be generated.

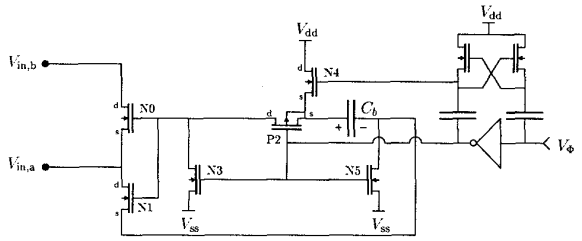

Figure 4: Bootstrapped switch: simple implementation.

3.2. Improved Implementation

Fig. 5 shows an improved implementation of the switch. N1b is a simple NMOS switch which should be included if the supply voltage is only slightly higher than the PMOS threshold voltage. N1b prevents switch malfunction which may occur if clock feedthrough is allowed to reduce the channel potential of P2 to a level where it does not turn on, in which case N1 (and hence N0) will not turn on neither.

A more serious problem of the simple implementation (Fig. 4) is that the gate oxide of N3 and P2 is subject to voltages that exceed the supply voltage difference. This may become inadvisable in the foreseeable future. N3 is easily protected by including the cascode device NMOS N3b. The gate oxide of P2 is more difficult to protect because the high stress occurs when it conducts. The problem is solved by operating P2 with a constant overdrive. N2 is a bootstrapped switch that connects C_b between the gate and source terminals of P2, whereby P2 also becomes bootstrapped. The two interconnected bootstrap loops do not lock automatically, which is why the small capacitor C_2 is needed to initiate the switch's on

junctions connected to the substrate.

[3]The stray load of $V_{\text{in,a}}$ is greater than that of $V_{\text{in,b}}$, hence $V_{\text{in,a}}$ should be considered as the driving (input) switch terminal. The operation of many low-voltage SC circuits is such that $V_{\text{in,a}}$ is connected to V_{ss} (in the off state) by a separate switch. In that case, sw1 can be implemented as a conductor (metal layer).

[4]In that case, the main switch element's gate potential would not be able to exceed $V_{\text{dd}} + |V_{\text{TP}}|$

[5]The advantage is that the bootstrap capacitor will not have to drive the capacitive load constituted by the well in which P2 is implemented. Hence, C_b can be smaller and/or the switch's conductance will be less signal-dependent.

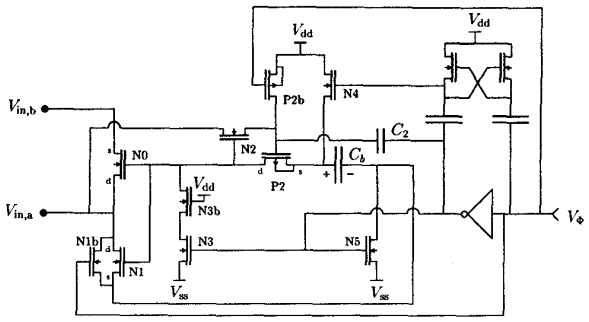

Figure 5: Bootstrapped switch.

state Φ. P2 is turned off (and C_2 is precharged) by the simple PMOS switch P2b.

A similar switch has been developed and published in parallel to this work [6]. The only differences are that it lacks N1b (which was unnecessary because the supply voltage was fairly high, 1.5 V) and that it fails to effectively protect the gate oxide of P2.

4. BODY EFFECT COMPENSATION

At very low supply voltages, and in other critical situations, the MOSFET switch's body effect may represent an intolerable nonlinearity. As discussed above, it is the PMOS implementation of sw2 which prevents the bootstrapped switch (Fig. 3) from being compensated for the body effect when implemented in a single-well technology. An alternative bootstrap topology, which is not subject to this problem, is shown in Fig. 6.

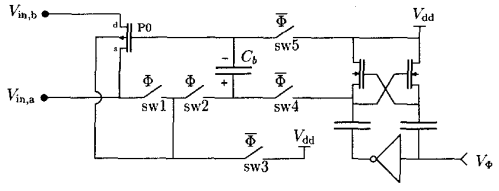

Figure 6: Body-effect-compensated bootstrapped switch.

The fundamental difference is that the bootstrap capacitor is connected directly to the gate terminal of P0. sw5 turns off P0 in the off state, and that requires C_b to be charged between V_{dd} and $2V_{dd}$. The high potential $2V_{dd}$ is generated by the charge pump. In the on state, sw1 and sw2 close the bootstrap loop. Notice that P0 is compensated for the body effect by connecting the bulk terminal to $V_{in,a}$ in the on state. sw2 and sw3 can, in principle, be a short and an open circuit respectively, but they should be real switches to avoid loading the charge pump by the well in which P0 is implemented.

4.1. Implementation

Fig. 7 shows an implementation of the switch. Here, sw4 is implemented as a PMOS P4, which operates as a rectifier for the alternating voltage provided by the charge pump. sw3 and sw5 are implemented as the simple PMOS switches P3 and P5a. The gate oxide of P5a is protected by the cascode device PMOS P5b.

sw1 can, for example, be implemented as a PMOS device controlled by the same gate signal as P0 (not shown). sw2 is the only switch that may be difficult to design because it is exposed to the high potential from the charge pump. If the gate oxide is robust, sw2 can be implemented as an NMOS N2 with its gate terminal connected to "Node A" in the charge pump (not used in the the shown implementation). Alternatively, if the gate oxide is sensitive and the supply voltage is fairly high[6], sw2 may be designed as a transmission-gate-type switch[7]. The shown implementation of sw1 and sw2 illustrates an option for use in the most complicated situation where the gate oxide is fragile and the supply voltage is only slightly higher than the threshold voltage.

In this case, sw2 can be an NMOS N2* controlled by a gate signal which is V_{dd} in the off state and $V_{in,a}$+V_{dd} in the on state. This signal is generated by the bootstrapped switch shown in Fig. 5, where it is available at the source terminal of P2. If this switch (Fig. 5) is implemented anyway, sw1 can be implemented simply as a bootstrapped switch N1* controlled by the signal provided at the drain terminal of P2.

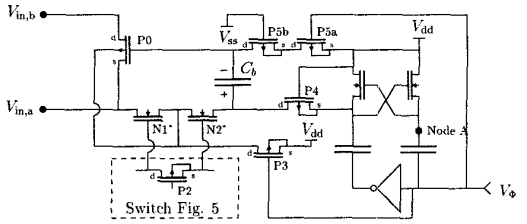

Figure 7: Low-voltage low-stress (gate oxide) implementation.

5. SIMULATION RESULTS

The switches shown in Figs. 5 and 7 have been simulated with HSPICE using BSIM3v3 transistor models for a 0.6μm technology, in which the threshold voltages were approximately 0.8 V and -0.85 V for NMOS and PMOS transistors, respectively. All transistors were minimum-length, and N0 and P0 were respectively 10 μm and 30 μm wide. Except for N1, N1*, and N2* which were 3 μm wide, all internal NMOS transistors were 1 μm wide, and all internal PMOS transistors were 3 μm wide. All capacitors were 1 pF, except C_2 which was only 0.1 pF. The switches were generally simple to design, and very little optimization was performed for these simulations.

The generation of the non-overlapping clock signals is, however, a design aspect which can make a great difference in the performance[8]. The inverter shown in Figs. 5 and 7 was used to drive

[6]This situation is quite likely to occur because this type of switch is generally useful for circuits that sample continuous-time voltage signals. These circuits need not necessarily be subject to a supply voltages that are so low that transmission-gate switches are useless.

[7]Where the NMOS's gate is connected to V_{dd} and the PMOS is controlled by a doubled clock signal (V_{ss} and $2V_{dd}$).

[8]The use of non-overlapping clock phases is necessary to prevent the 1 pF capacitors from being partially discharged in the transition between the two states Φ and $\overline{\Phi}$. This is advisable even for the charge pump.

an SR latch with delayed outputs[9], and *all* internal switches were driven by the thereby generated non-overlapping clock phases Φ and $\overline{\Phi}$ (each clock phase was generated both as an inverted and as an noninverted voltage signal).

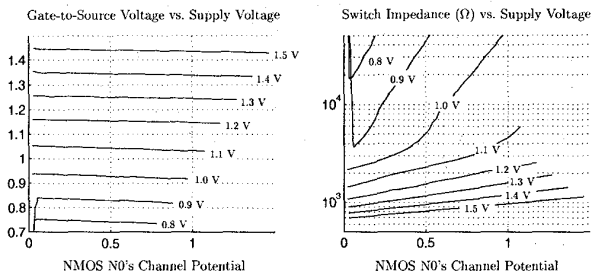

Figure 8: Simulated performance of the bootstrapped switch shown in Fig. 5.

Fig. 8 summarizes the performance of the bootstrapped switch shown in Fig. 5, which was simulated for supply voltages in the range from 0.8 V to 1.5 V. The gate-to-source voltage is fairly signal-independent and only about 50 mV less than the supply voltage[10]. This illustrates that C_b indeed operates as a floating battery. The slight droop is caused by the stray-capacitance loading of C_b, which is dominated by the well in which P2 is implemented (this can be avoided, as discussed above). This droop accounts for some of the switch's impedance's signal dependence, but it is the body effect which is the dominating factor. The switch's operation is reliable for supply voltages greater than 1.1 V, for which the impedance is less than 6 kΩ and the maximum operating speed about 3 MHz (40 MHz was obtained for 1.5 V supply voltage, although the transistor sizing was somewhat arbitrary).

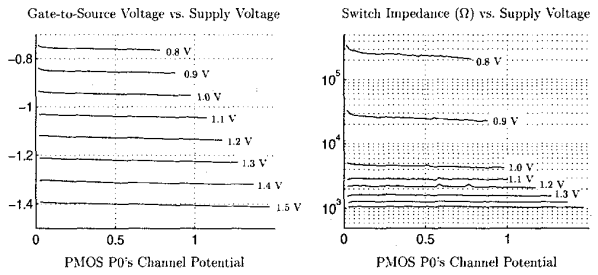

Figure 9: Simulated performance of the body-effect-compensated bootstrapped switch shown in Fig. 7.

Fig. 9 summarizes the performance of the body-effect-compensated bootstrapped switch shown in Fig. 7. The gate-to-source voltage is almost signal-independent; the droop is smaller than that observed in Fig 8 because the capacitive load of C_b is smaller.

[9]Two cross-coupled NAND gates were used, each driving an inverter string; this configuration is often used in SC circuits to generate non-overlapping clock phases.

[10]The offset (50 mV) represents a charge portion equivalent to the inversion charge accumulated in the conductive channel during the on state. This charge flows to the gate of N0 to charge the gate-to-channel "capacitor."

The switch's impedance is very well-behaved; the slight droop in impedance is caused by the corresponding droop in the gate-to-source voltage. The switch's operation is reliable for supply voltages as low as 0.9–1.0 V, for which the switch impedance is in the order of 10 kΩ.

If large (low-impedance) switches are designed without increasing C_b proportionally, the gate-to-source voltage may have a considerable droop. The switch, however, can still be designed such that the impedance will be nearly signal-independent. By connecting a small NMOS device, say N6, in parallel with P0, and by connecting N6's gate terminal to the gate terminal of N1* in Fig. 7, a bootstrapped "transmission-gate" switch with an appropriate "mix" of the impedance curves in Figs. 8 and 9 can be designed.

6. CONCLUSION

Bootstrapping techniques are suitable for the linearization of MOSFET switches. It was demonstrated that bootstrapped switches with a reliable linear switching operation can be implemented in a standard CMOS technology, even when the supply voltage is as low as 1 volt. Using these switches, low-voltage SC circuits can be implemented in any usual topology.

The best performance is obtained if the switching MOSFET is compensated for the body effect. This is feasible also in single-well technologies, using a new bootstrap topology (Fig. 6) where the bootstrap capacitor is connected directly to the gate of the switching MOSFET. The switch circuits can be designed such that the gate oxide is not subject to voltages exceeding the supply voltage difference. This requires the use of several transistors, but the total chip area required is modest.

The switch's remarkable linearity makes it a prime candidate for use in circuits that sample continuous-time signals (low voltage or not). A patent is pending on the described circuits.

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