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ON DYNAMIC RANGE LIMITATIONS OF CMOS CURRENT CONVEYORS

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ABSTRACT

This paper is concerned with the dynamic range of continuous time CMOS current mode circuits. As a representative current mode device a class AB current conveyor is examined. First, the voltage input range of the high impedance Y input is investigated. Next, the current input range of the low impedance X input is investigated. It is compared to the thermal noise in the X to Z signal path in order to evaluate the dynamic range, and the dependencies of the dynamic range on the supply voltage and the transistor lay-out is derived, both for the situation where the conveyor is used over a narrow frequency band and for the situation where the conveyor is used over the full bandwidth achievable. Finally, the optimisation of the current input range is related to the distortion characteristics and it is pointed out that to a first order approximation the distortion is independent of the current range.

1. INTRODUCTION

Current mode signal processing has been advocated as a candidate for low voltage, high speed signal processing for several reasons [1]. One reason is that in true current mode signal processing the nodes are kept at a low impedance level which minimizes the influence of parasitic capacitances, leading to good high frequency performance. Another is the dynamic current range achievable even with low supply voltages. In bipolar technology it is obvious that large currents can be achieved in spite of low supply voltages because of the exponential relation between the collector current and the base-emitter voltage of a bipolar transistor. For MOS, the basic device equation is not quite as favourable with respect to the dynamic current range.

In this paper we will present an analytical investigation of the theoretical limits to the dynamic range in a CMOS current mode system. As a representative building block for current mode systems we have selected a CCII+ current conveyor [2] and we have examined the dynamic range of a class AB CMOS current conveyor implementation. The maximum output range is related to other important properties such as noise, bandwidth and distortion. Emphasis will be on the current mode input and output of the conveyor since we are mostly interested in characterizing the device with respect to current mode signal processing. However, for completeness a short description of the voltage follower stage will be given. For the purpose of the analysis we have selected the well-known basic class AB implementation of a CCII+ conveyor shown in fig. 1. This configuration forms the basis for many other implementations of CMOS current conveyors and the analysis given here is with few modifications relevant also for improved

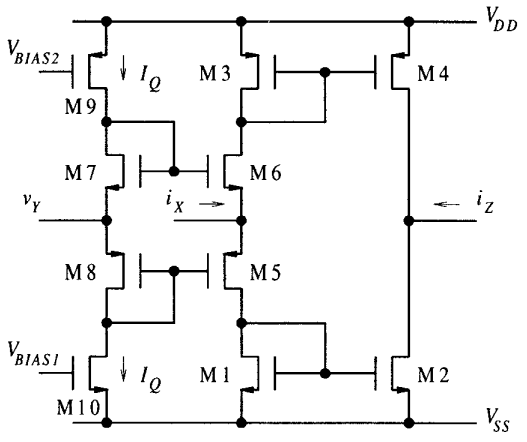

Figure 1. Class AB CMOS current conveyor

configurations such as configurations utilizing cascode transistors [3]. We assume that the conveyor has been designed such that $\beta = \mu C_{ox}\frac{W}{L}$ matches for relevant N-channel and P-channel transistors (e.g. M1 and M3), and we assume $V_{TN} = -V_{TP} = V_T$. Also, $V_{DD} = -V_{SS}$.

2. VOLTAGE INPUT RANGE

The voltage input range is determined by the Y to X voltage follower which is essentially just a complementary source follower. For maximum voltage range the output current sensing mirrors (M1-M2 and M3-M4) should be designed such that there is room for their input gate-source voltages and the drain-souce voltages of M5 and M6 within the supply voltage limits. To a first order approximation this is achieved if $\beta_1 = \beta_3 \geq \beta_6 = \beta_5$. Since the maximum gate voltage of M6-M7 is $V_{DD} - V_{satq}$ where $V_{satq} = \sqrt{2I_Q/\beta}$ is the saturation voltage of M9, the maximum input voltage is $V_{DD} - V_{satq} - V_{GS7} = V_{DD} - V_T - 2V_{satq}$ where we have assumed the same saturation voltage at the bias current level I_Q in M9 and M7. Similarly, we find a minimum input voltage of $V_{SS} + V_T + 2V_{satq}$.

With an X input current $i_X \neq 0$ the voltage range of the voltage follower is reduced because there must be room for the gate-source voltage of M5 or M6 within the supply voltage limits. Thus, the

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maximum Y input voltage is

$$V_{Y,max} = V_{DD} - |V_{GS5}| + V_T + V_{satq}$$
$$= V_{DD} - V_{satq}(\sqrt{\frac{I_{X,max}}{I_Q}} - 1) \quad (1)$$

assuming that $I_{X,max} \gg I_Q$.

A similar equation applies for $V_{Y,min}$.

Thus, in order to achieve a large Y-X voltage range one should select large supply voltages and large values of β for the transistor, i.e. wide transistors.

A significant improvement of the Y to X voltage range can be achieved by using a voltage follower based on a rail to rail CMOS opamp configured as a unity gain amplifier with output current mirroring for the X to Z signal path.

We also note a constraint on the minimum useful supply voltage: V_{DD} must be large enough to leave room for a gate-source voltage plus a saturation voltage, i.e.

$$V_{DD} \geq V_T + 2V_{satq} \quad (2)$$

or

$$\beta_{min} = 8I_Q/(V_{DD} - V_T)^2 \quad (3)$$

The minimum value of β characterizes the transistor geometries which will utilize all of the available voltage for the gate-source voltage. This leaves no room for signal swings, so in practice a value of β significantly larger than the minimum value must be used. When β is increased, the gate-source voltage and the saturation voltage decreases which allows room for signal swing. It should be mentioned that if β is increased very much the gate-source voltage approaches the threshold voltage and at some point the transistors may go into weak inversion. The following analysis applies only to the situation where the transistors remain in strong inversion and where a standard Shichman-Hodges transistor model [4] can be used.

In the analysis above we have neglected the bulk effect on the source follower transistors M5-M8. The bulk effect increases the effective value of V_T for these transistors, further limiting the voltage swing. Also, we have assumed single transistors. In practice, cascodes will often be used in configurations such as the one shown in fig. 1. In this case the saturation voltages are increased. With optimum biasing the saturation voltage of a low voltage cascode is twice the saturation voltage of a single MOS transistor [5] and the minimum value of β is four times the value given by (3).

3. CURRENT INPUT RANGE

The current input range is determined by the complementary current mirror M1-M2, M3-M4. The input range depends on the voltage at the Y input. The maximum input current into M1 or M3 is limited by the gate voltage available. Assuming for instance $i_X > 0$ and $v_Y = 0$ the gate-source voltage available for M1 is $|V_{SS}| - V_{satq}$ and the maximum input current is limited by

$$I_{D1} = \frac{\beta}{2}(|V_{SS}| - V_{satq} - V_T)^2 \quad (4)$$

With a design for minimum supply voltage, i.e. I_Q, V_{DD} and β related by (3) we find

$$I_{D1} = \frac{\beta}{8}(V_{DD} - V_T)^2 \quad (5)$$

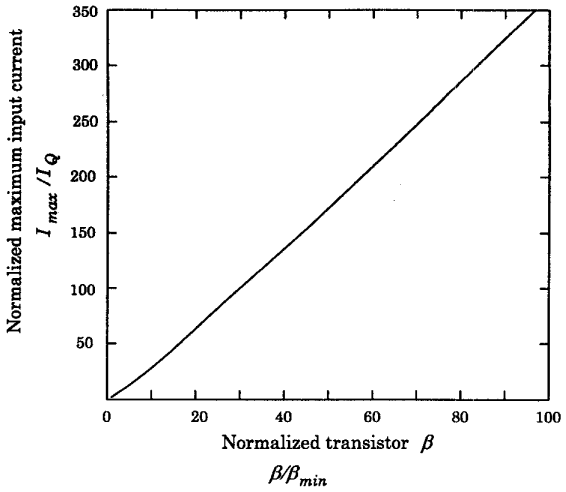

Figure 2. Current input range versus transistor size

This is in fact equal to I_Q so for this design there is no room for an input current when all transistors are required to operate in saturation. In order to obtain a design which can operate in class B it is necessary to increase β above the minimum value given by (3). A larger value of β will decrease the saturation voltage to

$$V_{satq} = \frac{V_{DD} - V_T}{2}\sqrt{\frac{\beta_{min}}{\beta}} \quad (6)$$

and this leaves room for more signal voltage swing at the gate of the mirror transistors. Class B operation is achieved for $|I_X| > 4I_Q$ [6] and in this situation (4) can be rewritten into

$$\frac{I_{X,max}}{I_Q} = 4\frac{\beta}{\beta_{min}}\left(1 - \frac{1}{2}\sqrt{\frac{\beta_{min}}{\beta}}\right)^2 \quad (7)$$

This relation is depicted graphically in fig. 2.

With $v_Y \neq 0$ the gate voltage available for the mirror transistors M1 and M3 is increased for one of the mirrors and decreased for the other. However, the increase in available gate voltage is note very useful because it is accompanied by a shift of the X input voltage due to the voltage follower from Y to X. This makes it impossible to create the gate-source voltage required by M5 or M6 because the X input cannot be taken above or below the positive and negative supply rail, respectively. Hence, in practice a voltage at the Y input would limit the current input and output range to a useful range of

$$|i_X| < \frac{\beta}{2}(V_{DD} - V_{satq} - V_T - |V_y|)^2 \quad (8)$$

Obviously, in order to obtain a large current range one should select large supply voltages and large values of β for the transistors, i.e. wide transistors, just as was the case for the voltage input range.

For the current buffer it is not easy to envisage configurations which can extend the current range because, essentially, the current must come from a MOS transistor which has a limited gate voltage available.

4. NOISE LEVEL

In order to evaluate the current range it can be compared to the noise current present at the output of the conveyor.

The output noise current comes from M1, M2, M3 and M4 whereas M5 and M6 do not contribute to the noise. Thus, the output noise power (thermal noise) is given by

$$\overline{di_{eq}^2} = 4 \times \frac{8kT}{3} g_m df = \frac{32kT}{3} \beta V_{satq} df$$
$$= \frac{16}{3} kT \sqrt{\beta \beta_{min}} (V_{DD} - V_T) df \quad (9)$$

We might relate this to the available signal output power given by $I_{max}^2/2$ to calculate a signal to noise ratio. This yields (after some calculations)

$$SNR = \frac{3}{16} \frac{I_Q (V_{DD} - V_T)}{kT \cdot df} (\frac{\beta}{\beta_{min}})^{3/2} (1 - \frac{1}{2} \sqrt{\frac{\beta_{min}}{\beta}})^4 \quad (10)$$

Apparently, the SNR depends strongly on β and also on the supply voltage and quiescent current. A theoretical worst case situation is $\beta = \beta_{min}$ which results in

$$SNR_{wc} = \frac{3}{256} \frac{I_Q (V_{DD} - V_T)}{kT \cdot df} \quad (11)$$

As an illustrative numeric example we may assume $I_Q = 1\mu A$ and $V_{DD} - V_T = 1V$. For a bandwidth $df = 1kHz$ this yields a signal to noise ratio of about $95dB$. Fig. 3 shows the improvement in signal to noise ratio which can be obtained by increasing β.

It might be interesting to compare this noise performance to the noise performance of a voltage mode system. Let us for simplicity assume that a voltage mode system has a full swing range of $\pm V_{DD}$ and that the noise is dominated by the equivalent gate noise voltage from two input transistors (a differential pair). This would yield a signal to noise ratio given by

$$SNR_v = \frac{(2V_{DD})^2/2}{16/3 \cdot kT/g_m \cdot df} = \frac{3}{16} \frac{I_Q V_{DD}}{kT \cdot df} \times \frac{4V_{DD}}{V_{sat}} \quad (12)$$

where I_Q and V_{sat} are the quiescent current and saturation voltage of the noise contributing transistors. Comparing (12) with (10) we see that in voltage mode $4V_{DD}/V_{sat}$ takes over the $\beta-$dependence found in the current mode situation. Apparently, there is no inherent, fundamental advantage to be obtained from neither voltage mode, nor current mode, and in both cases a good signal to noise ratio is obtained by using a large supply voltage, a large supply current and wide transistor to keep β high and V_{sat} low.

5. BANDWIDTH CONSIDERATIONS

In addition to the noise considerations, the X to Z buffer may be optimized for speed. An essential parameter to consider with respect to speed optimization is $f_T = g_m/(2\pi C_g)$ for the mirror transistors since the maximum limit to the pole of the mirrors is $f_T/2$. The P-channel mirror will be the limiting mirror in the complementary current mirror. For this we find

$$f_T/2 = \frac{3}{8\pi} \frac{\mu}{L^2} \sqrt{\frac{2I_Q}{\beta}} = \frac{f_{T,max}}{2} \sqrt{\frac{\beta_{min}}{\beta}} \quad (13)$$

where

$$\frac{f_{T,max}}{2} = \frac{3}{8\pi} \frac{\mu}{L^2} \sqrt{\frac{2I_Q}{\beta_{min}}} = \frac{3}{16\pi} \frac{\mu}{L^2} (V_{DD} - V_T) \quad (14)$$

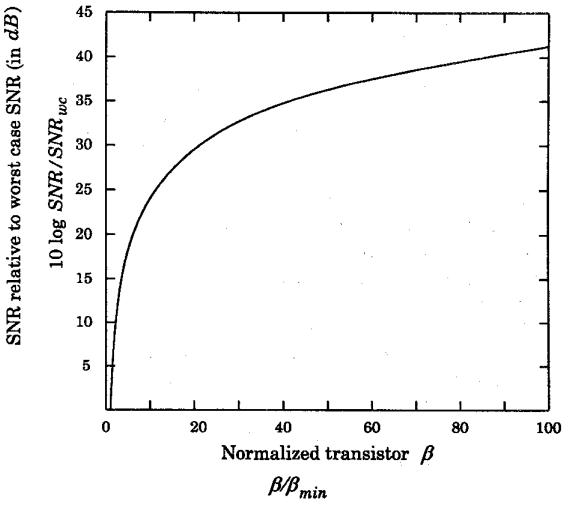

Figure 3. Signal to noise ratio versus transistor size

Obviously, a high frequency is obtained by using short transistors, a small value of β and a large supply voltage.

Often in practice, the input capacitance to the mirror is dominated by the parasitic drain capacitances C_D of M3 and M6 rather than the gate capacitances. In this case we find a frequency limit given by

$$f_D = \frac{g_m}{2\pi C_D} = \frac{\sqrt{2\beta I_Q}}{2\pi C_D} \quad (15)$$

The parasitic capacitance C_D depends on the lay-out style. If C_D is independent of β, a large bias current is an advantage and β can also be selected to be large. Often, however, C_D can be considered proportional to the transistor channel width W in which case (15) can be rewritten into

$$f_D = f_{D,max} \sqrt{\frac{W_{min}}{W}} = f_{D,max} \sqrt{\frac{\beta_{min}}{\beta}} \quad (16)$$

where

$$f_{D,max} = \frac{\sqrt{2\beta_{min} I_Q}}{2\pi C_{D,min}} \quad (17)$$

i.e. the same lay-out dependence as found when C_g is limiting the frequency response.

In the expressions above the transistor channel length L has been assumed fixed, i.e. the design parameter for modifying β is the channel width W.

It might be instructive to consider the signal to noise ratio achieved over the full bandwidth of the current buffer.

From (10) and (13) we get

$$SNR = \frac{\pi I_Q L^2}{kT\mu} (\frac{\beta}{\beta_{min}})^2 (1 - \frac{1}{2} \sqrt{\frac{\beta_{min}}{\beta}})^4 \quad (18)$$

For a quiescent current of $1\mu A$ and a channel length of $1\mu m$ this leads to a signal to noise ratio of about $34dB$ for a design with $\beta = \beta_{min}$. The signal to noise ratio increases with increasing β as shown in fig. 4.

We see that there is a trade off between noise performance and bandwidth. In order to improve noise performance, β should be selected large whereas the highest possible bandwidth limitation is

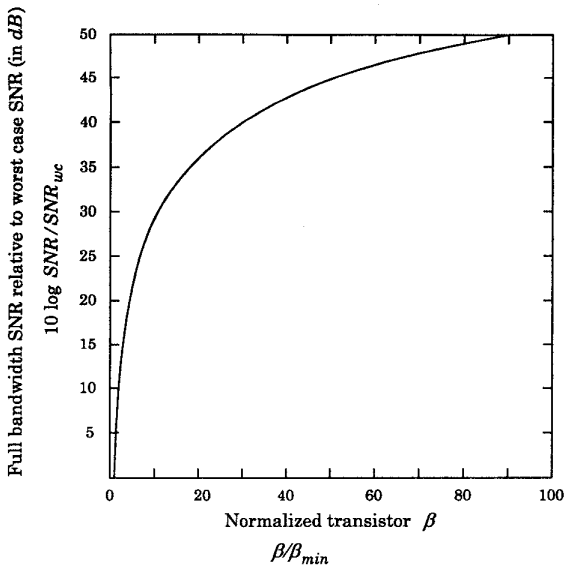

Figure 4. Full bandwidth signal to noise ratio versus transistor size

obtained from a small value of β. It is also noteworthy that a large supply voltage and a large quiescent current is advantageous both for bandwidth and for noise performance.Obviously, the signal to noise ratio over the full bandwidth is not impressive, so normally some other form of bandwidth limitation than the inherent high frequency limit must be imposed in order to obtain a reasonable signal to noise ratio.

6. DISTORTION

There are several sources of distortion in the current buffer stage of the conveyor [7]. The most important one is electrical mismatch due to different operating conditions for the input and output transistors in the current mirrors. This can be eliminated by proper cascoding techniques and if suitable low voltage cascode types are used it will not severely affect the maximum output range of neither the voltage buffer nor the current buffer. Even with the electrical mismatch eliminated, some distortion remains due to statistical mismatch of the current mirror transistors. It has been shown recently [6] that the mismatch induced distortion can be estimated from

$$THD = \sqrt{(0.26\frac{\Delta\beta}{\beta})^2 + (0.09\frac{\Delta V_T}{V_{satq}})^2} \qquad (19)$$

For the distortion to be minimized it is obviously necessary to select large geometries in order to minimize $\Delta\beta$ and ΔV_T. For a conveyor designed for low voltage operation the saturation voltage will normally have to be selected so small that the second term in (19) will be dominant. In this case (19) simplifies to

$$THD \simeq 0.09\frac{\Delta V_T}{V_{satq}} = 0.18\frac{\Delta V_T}{V_{DD} - V_T}\sqrt{\frac{\beta}{\beta_{min}}} \qquad (20)$$

Now, ΔV_T can often be considered to be inversely proportional to the transistor area [8], so with a constant channel length L and the channel width W as the variable design parameter, ΔV_T is inversely proportional to $\sqrt{W}$ while $\sqrt{\beta/\beta_{min}}$ is proportional to $\sqrt{W}$. This implies that to a first order approximation the total harmonic distortion is independent of the channel width, and the channel width may be designed to give the desired output current range and signal to noise ratio. For large values of the gate area ΔV_T tends to saturate [9] and in this situation the distortion will increase if the channel width is increased to obtain a larger output current range.

7. CONCLUSION

We have examined the maximum current range achievable for conventional class AB CMOS current conveyor implementations and we have discussed the optimisation of the current conveyor with respect to dynamic range over a frequency range. In the discussion we have included trade offs between noise, dynamic range, bandwidth, and distortion. It is found that the supply voltage and the transistor β are crucial parameters in all of the optimisations. A higher supply voltage leads to better performance in all respects. It is also found that there are conflicting requirements between noise optimisation and bandwidth optimisation because the noise optimisation calls for a small value of saturation voltage (wide transistors) whereas a good high frequency performance is achieved with a large saturation voltage. Concerning distortion, the optimisation for dynamic range and noise will only have second order effects on the distortion introduced by device mismatch.

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