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A 3RD ORDER LOW POWER SI ΣΔ-A/D CONVERTER FOR VOICE-BAND APPLICATIONS

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ABSTRACT

This paper presents a 3rd order switched current-ΣΔ-modulator. The ΣΔ-modulator operates at a sampling rate of $f_s = 600kHz$ and the signal band is $f_b = 5.5kHz$, i.e., an oversampling factor of $R = 54.5$ is used. Multiple input signals are used to reduce the internal signal swings which results in reduced power consumption. The shaping of the noise from the 2nd and 3rd integrator is used to allow the noise power from these integrators to be increased to further save power. The total power consumption is approximately $2.5mW$ with a supply voltage of $V_{DD} = 3.3V$. The maximum *SNR* is approximately 74.5dB.

1. INTRODUCTION

Over the last years ΣΔ-modulators have gained increasing popularity as they have the potential for high accuracy data conversion with modest analog requirements. The reason for the popularity originates in the fact that the quantization noise is moved from the signal band $[-f_b; +f_b]$ to high frequencies (Noise Shaping). This allows for very coarse quantization, e.g., 1-bit using a simple comparator.

In this paper a 3rd order ΣΔ-analog-to-digital (A/D) modulator for voice band applications is presented. The design of the ΣΔ-modulator is optimized with respect to minimum power consumption. In section 2 the basic theory for ΣΔ-modulators is reviewed. The section presents the most important parameters that describe the ΣΔ-modulator and discusses how the internal signal swings in the ΣΔ-modulator can be reduced to minimize power consumption. In section 3 the SI-circuits that are used to implement the integrators are presented. Section 4 reports the measurement results.

2. SYSTEM DESIGN

In figure 1 a block diagram of the 3rd order ΣΔ-modulator used in this design is shown. The signals are shown as currents as the ΣΔ-modulator is to be implemented using switched current (SI) techniques.

The quantizer in figure 1 can be modeled by replacing the comparator with a amplification factor, K_n, and a white noise source, n_q, that represents the quantization noise [2], [3]. It is a widespread misunderstanding to assume that the gain K_n equals one because if it was so then the modulator would not be invariant to scaling of k_3. In fact, it is not necessary to assume anything about the gain K_n in order to design the modulator filter, i.e., determination of the coefficients b_1, b_2 and b_3.

The ΣΔ-modulator coefficients b_1, b_2 and b_3 are determined by designing the *NTF*(z), [1] and [2], as a 3rd order highpass Butterworth filter.

If a signal is forced into the ΣΔ-modulator one will observe that it becomes unstable if the amplitude of the signal is greater than a certain value called the maximum stable input amplitude *MSA* [2]. In [4] the authors showed that the cut-off frequency f_n for the *NTF*(z) has a very strong influence on the *MSA* whereas the influence on the *SNR* is very weak. When the ratio between f_n and f_s decreases then the *MSA* increases and the signal-to-quantization-noise-ratio is approximately constant over a wide range of cut-off frequencies, f_n. In ΣΔ-A/D modulators it is desirable to get as much signal power into the modulator as long as the quantization noise is well below the analog noise floor as the overall *SNR* then increases.

If the ΣΔ-modulator is designed to have only one input ($a_2 = 0$ and $k_1 = k_2 = k_3 = 1$) the internal signal swings in the integrators are very different. By forcing a sinusoidal signal with an amplitude of *MSA* into the ΣΔ-modulator the peak signal swing in INT1, INT2 and INT3 is approximately $5I, 16I$ and $24I$ respectively (assuming that the integrators are ideal). The internal signal swings can be adjusted to have the same peak value as the swing in the first integrator by adjusting the scaling factors k_1, k_2 and k_3. This scaling results in a constant k_3 in front of the quantizer which can be removed as a positive constant in front of a comparator does not affect the output of the comparator. This will therefore not affect the modulator filter.

The internal signal swings can be reduced further by introducing a second input, i.e., $a_2 \neq 0$. This input is added between INT1 and INT2. It was found that $a_2 = b_2$ results in an optimal reduction of the internal signal swings in the integrators by a factor of approximately 3. After introducing the second input the internal signal swings are approximately $1.7I$ for all three integrators. The reduction in the internal signal swings will substantially reduce the power consumption of the modulator, because it allows for lower bias currents in the switched current integrators. The extra input a_2 results in a peak in the signal transfer function *STF*(z), [1] and [2], at high frequencies ($\approx f_n$), that results in a slight increase of the *STF*(z) in the signal band. At the frequency f_b the *STF*(z) is 0.1dB larger than at DC.

In figure 1 the analog noise sources n_1, n_2 and n_3 represent the noise from the integrators and D/A converter in the feedback loops. The noise at the output of the modulator is the sum of n_1 unfiltered, n_2 1st order highpass filtered, n_3 2nd order highpass filtered and, finally, n_q 3rd order highpass filtered, *NTF*(z). As the noise sources n_2 and n_3 are highpass filtered INT2 and INT3 can be allowed to generate more noise than INT1 without affecting the overall *SNR* at

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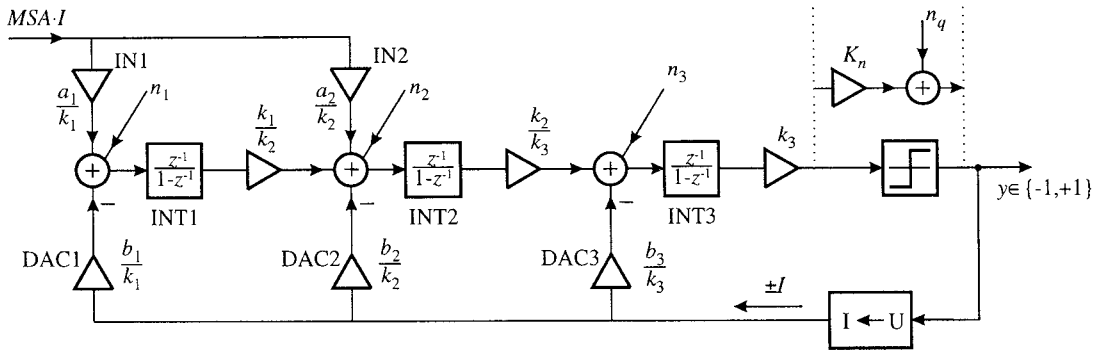

Figure 1. Block diagram of the 3rd order ΣΔ-modulator.

the output. In this design this technique was used to lower the internal signal swings and thereby the quiescent current in INT2 and INT3 by a factor of 2 and 4 respectively. This results in the same *SNR* but reduces the power consumption by a factor of $\frac{1+1+1}{1+0.5+0.25} = 1.71$.

Because the noise from INT2 and INT3 is shaped, the noise at the output of the modulator is dominated by the noise from the input section, i.e., INT1, DAC1 and IN1. By increasing the *MSA* we increase the signal power at the input of the modulator which allows a noisier input section for a given *SNR*. We utilize this to lower the power consumption. A very high *MSA* will result in a reduction of the *SNR* because the modulator begins to perform poor coding of the input signal which result in increased quantization noise at the output. As a compromise we chose $MSA = 0.69I$ which equals to $f_n = 0.15f_s$ for a $NTF(z)$ designed as a 3rd order Butterworth highpass filter [4]. For $f_n = 0.15f_s$ the following coefficients are found (see figure 1): $a_1 = b_2 = 1$, $a_2 = b_2 = 5.66$, $b_3 = 13.6$ and due to the scaling $k_1 = 1$, $k_2 = 17.4$ and $k_3 = 64.0$.

3. IMPLEMENTATION

The SI-integrator used in this design is shown in figure 2. The SI-integrator is a cascode type but also a folded cascode type was considered. However, the folded cascode SI-integrator introduced extra noise due to the extra current sources needed and therefore this solution would consume more power for a given *SNR* and thus it was rejected.

The integrator in figure 2 has a very low input impedance as the transistors $M_{2,1}$ and $M_{2,2}$ act as current conveyors which reduce the input impedance (compared to the input impedance of a single transistor) by a factor of $L_G = (1+\frac{g_{m2}}{g_{o2}})$ where g_{m2} and g_{o2} are the transconductance and output admittance for the M_2's. The input impedance of this circuit is therefore in the order $\frac{g_{o2}}{g_{ms}g_{m2}}$ which can be as low as 1Ω at low frequencies. This eases the interfacing to the circuit, in fact, the input devices IN1 and IN2 in figure 1 are just resistors that convert the input voltage to a current. This is indicated in figure 2.

The transfer function for the integrator is:

$$\frac{i_{out}(z)}{i_{in}(z)} = K\frac{z^{-1}}{1-z^{-1}} \qquad (1)$$

It is important that the integrator has very little loss as any loss results in a finite DC-gain which gives rise to an increase in the quantization noise at low frequencies. The loss in the SI-integrator is caused by finite output resistance and the gate-drain overlap capacitances for $M_{s,1}$ and $M_{s,2}$ but the transistors $M_{2,1}$ and $M_{2,2}$ reduce these error with

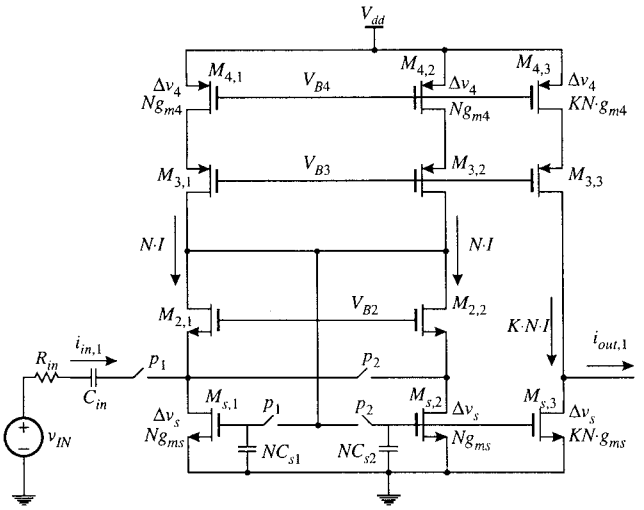

Figure 2. SI-Integrator.

the same gain factor L_G as mentioned before. The loss in the SI-Integrator used in this design is less than 0.1%. The scaling factor K in figure 2 is controlled by the length and the width of MOS-transistors.

It is well known that one of the main problems using SI-circuits is the nonlinear settling behavior [1]. When high signal currents compared to the quiescent current are processed, the nonlinear settling behavior degrades the performance of the SI-integrator drastically. Hence, it also decreases the performance of the ΣΔ-modulator. It is, however, not possible to evaluate this problem using SPICE as the simulation time would be enormous. It was therefore necessary to evaluate this problem by other means. A 'C++'-program that modeled the SI-integrator as a nonlinear component was written. The program models the SI-integrator as build from two current copiers (CCOP) (see, [1]). A CCOP is basically a operational transconductance amplifier (OTA) and some switches. The OTA is in the program described as a component with a nonlinear relationship between the input voltage and the output current. For each sample the program solves the nonlinear settling problem using the 2nd order Runge-Kutta algorithm. The program was verified by comparing its results with simulations using PSPICE, performed on relatively simple building blocks.

Simulations performed on the entire ΣΔ-modulator showed that the internal signal swings were increased from approximately $1.7I$ to $2.4I$, when the integrators were made

nonlinear using a square law relationship (to model the behavior of MOS transistors) for the OTA's in the CCOP's. Furthermore, the nonlinear settling causes a DC-component at the output of the modulator which causes nonharmonics in the signal band for small input amplitudes. To reduce the effect of this a quiescent current of $3I$, i.e., $N = 3$ was chosen.

4. MEASUREMENT RESULTS

The $\Sigma\Delta$-modulator is measured using a LabVIEW setup. The 1-bit output of the $\Sigma\Delta$-modulator is captured using a high speed digital data acquisition board located in a PC that also runs the LabVIEW software. The LabVIEW analysis software assume that two levels of the 1-bit output from the $\Sigma\Delta$-modulator is in the set $\{-1, +1\}$.

All measurements are based on FFT-analysis of 16384 output samples captured from the $\Sigma\Delta$-modulator. Averaging is used to reduce the varians of the measured spectra.

All of the measurements of the $\Sigma\Delta$-modulator are performed with a supply voltage of $V_{DD} = 3.3V$, and the bias current in the first integrator is $NI = 96.0\mu A$ ($I = 32.0\mu A$). The signal bandwidth is $0Hz - 5.5kHz$ and the sampling rate is $f_s = 600kHz$.

First the relationship between the 1-bit output is determined and the input voltage. This is done by applying a sinusoid with a frequency of $3kHz$ and an amplitude of $0.1V_{peak}$ to the input of the $\Sigma\Delta$-modulator. Using FFT-analysis the amplitude of the sinusoid at the output of the modulator is 0.0242 RMS corresponding to -32.3dB.

The expected amplitude is calculated from:

$$\begin{aligned} G &= \frac{V_{in,peak}}{\sqrt{2}} \frac{1}{R_{in}} \frac{1}{I} = \frac{0.1V_{peak}}{\sqrt{2}\, 89.1k\Omega \cdot 32.0\mu A} \\ &= 0.0247 \text{ RMS} \sim -32.1\text{dB} \end{aligned} \quad (2)$$

where $R_{in} = 89.1k\Omega$ is the resistor at the input of the modulator shown in figure 2. The results above show good agreement between the measured gain and the expected gain, they only differ with 0.2dB.

In figure 3(a) the output spectrum of the $\Sigma\Delta$-modulator is shown for no input signal applied.

A $\Sigma\Delta$-modulator with zero input has a large tone at $\frac{f_s}{2}$. When a small DC component is present at the input of the modulator the tone at $\frac{f_s}{2}$ splits into two tones located at $(1 \pm DC)\frac{f_s}{2}$ [2]. This effect is seen in figure 3(a). The small DC component at the input of the modulator also causes nonharmonic tones to appear in the signal band, as seen in 3(b). These tones are are correlated with tone at $\frac{f_s}{2}$. This effect was also observed in the simulation using the 'C++'-program. If the DC component is removed then the tones in the signal band disappears.

In [1] it is shown that the noise power in SI circuit increases by a factor of two when the storage capacitance, C_{s1} and C_{s2} in figure 2, is halved. The chip is designed so that the storage capacitance can be halved and hence the above effect can be tested. With zero input current the noise power in the frequency range $1600Hz$ to $2800Hz$ is measured to -93.4dB. With the storage capacitance halved the noise power was measured to -90.0dB, i.e., a difference of 3.4dB which indicates that effect of halving the storage capacitance is as described in [1]. In both cases the noise power was estimated by averaging 32 spectra.

In figure 4 the output spectrum of the modulator is shown, with a $3kHz$-sinusoid and an amplitude of $1V_{peak}$

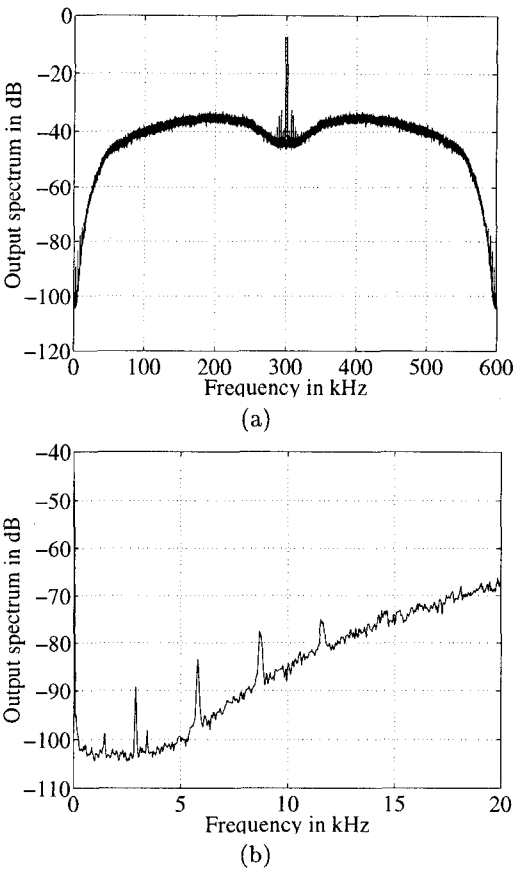

Figure 3. (a) Output spectrum with zero input $0Hz - 600kHz$ and (b) output spectrum with zero input $0Hz - 20kHz$. 16 averages.

(6dB below *MSA*) applied to the input. In figure 4(a) a lot of tones are observed around $\frac{f_s}{2}$. This can be explained by the fact that the modulator will see the input sinusoid as slowly varying DC because of the high oversampling ratio. Previously it was stated that a small DC component splits the tones at $\frac{f_s}{2}$ into two tones. As the input is varying in time the tones at $\frac{f_s}{2}$ are effectively FM-modulated with the input signal. This was also verified by simulations.

In figure 4(b) the input sinusoid is clearly visible in the output spectrum. A small 2nd order harmonic is also present due to the large amplitude of the input sinusoid. No nonharmonic tones are visible at low frequencies in contrast to figure 3(b). This is partly because the modulator is busy coding the input sinusoid and partly because the order of $\Sigma\Delta$-modulator is higher than 2 which makes it more chaotic and thus diffusing the tones.

In figure 5(a) the *SNR* as a function of the input signals is shown. The measurements are based on averages of 16 spectra for each input amplitude to lower the varians of the measured *SNR*. The harmonic distortion in figure 5(b) is measured the same way. The peak *SNR* is approximately 74.5dB. Considering the low power consumption of this $\Sigma\Delta$-modulator, which is $2.5mW$, this *SNR* is, to the knowledge of the authors, significantly higher than previously reported $\Sigma\Delta$-modulator implemented using switched-current technique.

The maximum *SNR* is measured for a RMS value of the input amplitude of -6.17dB. The $\Sigma\Delta$-modulator was design to have a *MSA* of $0.69I$. The RMS value of a sinusoid with

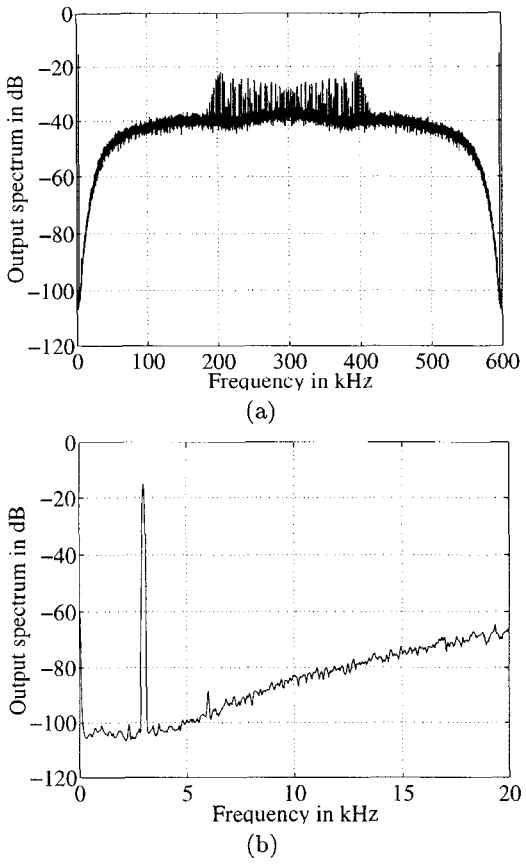

Figure 4. (a) Output spectrum ($0Hz - 600kHz$, 16 averages) with sinusoid at the input and (b) output spectrum ($0Hz - 20kHz$, 16 averages) with sinusoid at the input.

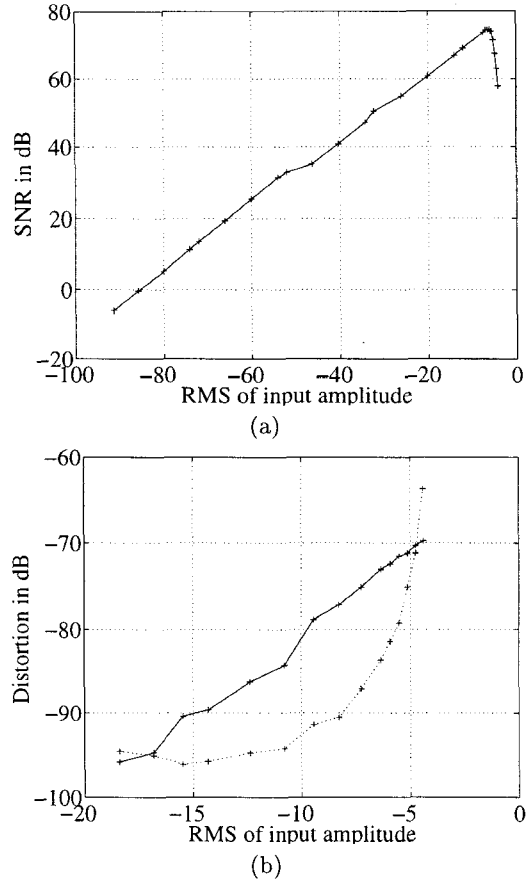

Figure 5. (a) Signal-to-noise ratio and (b) Harmonic distortion relative to input signal, solid line: 2nd harmonic and dotted line: 3rd harmonic.

an amplitude of MSA is, RMS= $20\log\left(\frac{0.69}{\sqrt{2}}\right) = -6.23$dB. Hence, the measured and expected MSA correspond very well.

For input amplitudes exceeding MSA, the harmonic distortion increases significantly as shown in figure 5(b), but the modulator does not become unstable. This is seen by the fact that the modulator does not generate a sustained oscillation at the output when the input signal is removed, but enters a stable idle state. This property results from the clamping of large internal signals in the class A switched-current integrators. For high order modulators (3rd order and higher), it is of outmost importance to scale the $\Sigma\Delta$-modulator so that the internal signals are clamped, when an input signal is present with an amplitude of MSA. This will in most situations ensure reliable and stable operation of the modulator.

5. CONCLUSION

In this paper a 3rd order switched current-$\Sigma\Delta$-modulator is presented. Design aspects at the system level are presented together with detailed measurements. By feeding the $\Sigma\Delta$-modulator with multiple input signals and by allowing for increased noise in the integrators as they approach the comparator, the internal signal swings are kept at a minimum. This effectively results in low current consumption and hence low power consumption. At a supply voltage of $V_{DD} = 3.3V$, the power consumption of the $\Sigma\Delta$-modulator is $2.5mW$ when it operates at a sampling frequency of $600kHz$. With this low power consumption the signal-to-noise-ratio is as high as $SNR = 74.5$dB. Due to internal clamping in the integrators and proper scaling, the stability properties of the $\Sigma\Delta$-modulator are excellent.

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