Nano-cantilevers flully integrated with CMOS for Ultrasensitive mass detection

Forsén, Esko Sebastian; Boisen, Anja

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Nano-cantilevers fully integrated with CMOS for ultrasensitive mass detection

Esko Forsén[1]

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[1]Department of Micro and Nanotechnology, Technical University of Denmark, Building 344, 2800 Kgs. Lyngby, Denmark

Supervisor:

Professor Anja Boisen
Department of Micro and Nanotechnology
Technical University of Denmark

Thesis Defence:

Wednesday December 14th 2005, 1 p.m. building 341, auditorium 22
Technical University of Denmark.

Evaluation Committee:

Professor Pietro Andreani
Ørsted, Center for Physical Electronics
Technical University of Denmark.

Dr. Javier Tamayo
Institute of Microelectronics of Madrid, Spain.

Professor Michael Roukes
Kavli Nanoscience Institute
California Institute of Technology, USA.

Preface

This thesis has been written as a part of the requirements for obtaining the Ph.D. degree at the Technical University of Denmark (DTU). The Ph.D. project has been carried out at the Department of Micro and Nanotechnology at DTU in the period from July 2002 to September 2005.

This Ph.D. project has been financed by a DTU Ph.D. grant. The work has been conducted within the Nanomass project within the BioProbe group under the supervision of:

Professor, Dr. Anja Boisen

I would like to thank all the persons involved in the *Nanomass*-project at CNM and UAB in Spain for their inspirative enthusiasm. I would especially like to thank Assoc. Prof. F. Pérez-Murano for all his kinds help during my visits at UAB and CNM and his patience in learning me SFM nanolithography. Assis. Prof. G. Abadal for sharing his vast experience and for his help with characterization of devices. Prof. N. Barniol, J. Verd, J. Teva, X. Borrisé, and M. Villaroya for their effort in answering every possible question regarding CMOS and other.

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I feel that the spirit in the group is one of its kind, which is also reflected in the productivity. This spirit has been nourished by the leadership of Prof. A. Boisen, to whom I owe special thanks. First, for supervising me during my Ph.D., making me grow as a scientist by always supporting me to make my own decisions. Second, for her help during the last stage of the Ph.D., proof reading the thesis and giving valuable feedback.

I would like to take the opportunity to thank: My mother for all her support, and who managed to convince me to learn the multiplication table by heart when I started school. My father who always nourished my curiosity, showing me books on atom physics as a child.

The greatest of thanks goes to my family, Annika and Emmy. To Emmy, who was born as I was in the middle of writing this thesis, and made my perception of the world turn upside down. To Annika, who helped me during the hard times and celebrated the good. Without your love, support and encouragement this would never have been possible.

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Abstract

This Ph.D. thesis deals with the development of mass sensitive silicon cantilever systems integrated with complementary metal oxide semiconductor (CMOS). The principle is based on the change in resonance frequency as mass adsorb onto the cantilever, which is measured using the signal amplification circuitry of the CMOS.

The cantilever is made to oscillate by using electrostatic actuation, and the resonance frequency is measured by capacitive readout as the cantilever oscillates in close proximity to a parallel electrode. The capacitive detection method necessitates CMOS integration due to the need to minimize the parasitic capacitance contribution, which otherwise would screen the resonance signal. The CMOS integration is achieved by adopting a post-process scheme on standard CMOS.

By reducing the dimensions of the cantilever to the nanometer regime, and consequently increasing the resonance frequency, an increased mass sensitivity is achieved. Hence, in order to define nanoresonators the use of lithography techniques such as electron beam lithography, scanning force microscopy based nanolithography, and direct write laser lithography have been evaluated. Resonator structures comprising of cantilevers having widths of 400 nm, a thickness of 600 nm, and a length of 20 µm, having a resonance frequency of the order of 1.5 MHz have successfully been fabricated onto pre-processed standard CMOS. The developed post-process is directly transferable onto state-of-the-art CMOS.

The devices have been characterized in ambient air and vacuum conditions and the mass sensitivity has been determined by adding point masses onto the cantilever. The resulting mass sensitivity is of the order of attogram (10^{-21} kg), which is the same order of magnitude as a single medium size biomolecule such as heme.

Possible applications are found within the field of biosensors, in detection of hazardous or non-hazardous agents such as explosives, nerve gas, gas system diagnostics. Another possible application is characterization and calibration of advanced lithography systems such as atom- or molecular beam lithography systems.

Dansk Resumé

Denne afhandling behandler udviklingern af massesensorer baseret på silicium bjælker (eng: cantilever), som er integreret med komplementerende metal-oxid-halvledere (eng: CMOS). Ændringen i silicium bjælkens resonansfrekvens forårsaget af masse adsorption detekteres af CMOS-forstærkeren.

Ved at påtrykkeen vekselspænding mellem cantileveren og en parallel elektrode, initieres cantileverens vibration. Da cantileveren vibrerer, når den er i nærheden af en elektrode-overflade, bliver der skabt en vekslende kapacitet mellem dem, som bliver detekteret af de integrerede kredse. CMOS integration er nødvendig, da dette signal er meget svagt og ville drukne i støjen skabt af ydre kapacitets-kilder. CMOS integrationen af cantilever strukturen er sket gennem mikro- og nanofabrikation efter fremstilling af de integrerede kredse.

Ved at reducere størrelsen på cantileverne til nanometer-dimensioner, og derigennem øge resonansfrekvensen, opnås en øget masseflsomhed. Dermed er litografi-teknikker som elektronstrålelitografi, atomkraftsmikroskopi-baseret nanolitografi samt direkte laserlitografi undersøgt for struktureringen af nanocantilevere på standart CMOS. Cantilevere med en bredde på 400 nm, en tykkelse på 600 nm og en længde på 20 µm, som har en resonans-frekvens i størrelsesordenen 1.5 MHz er fremstillet på standart CMOS. Den udviklede fabrikationsteknik kan endog anvendes på mere avanceret CMOS teknologier.

Fremstillede strukturer er karakteriseret i luft samt vacuum og masseføls omheden er undersøgt ved at placere punktmasser på cantileveren. Derved er en massef ølsomhed i størrelsesorden af et attogram (10^{-21} kg) blevet bestemt. Dette er i samme størrelsesorden som en enkelt middelstort biomolekyle.

Mulige anvendelsesområder findes indenfor biosensorindustrien, indenfor gas detektion af farlige emner som eksempelvis sprænstofer og nerve-gasser, samt diagnosticering af gassystemer. Et yderligere anvendelsesområde er karakteriseringen og kalibreringen af avancerede atom- og molekylestråle-litografisystemer.

Svensk Resumé

Denna avhandling behandlar utvecklingen av mass-sensorer baserade på kiselresonatorer vilka är integrerade med komplementerande metalloxid-halvledare (eng: CMOS). Förändringen i kiselresonatorns resonansfrekvens orsakad av massadsorption detekteras av CMOS-förstärkaren.

Genom att applicera en växelspänning mellan resonatorn och en parallell elektrod initieras vibrationen av resonatorn. Eftersom resonatorn vibrerar nära en electrod skapas en alternerande kapacitans mellan dem, vilken detekteras av de integrerade CMOS-kretsarna. CMOS-integration är en nödvändighet eftersom den kapacitiva signalen är mycket svag och annars skulle döljas i bruset skapat av externa kapacitanskällor. CMOS-integrationen av resonatorstrukturen har skett genom mikro- och nanofabrikation efter framställningen av de integrerade CMOS-kretsarna.

Genom att reducera storleken av resonatorn till dimensioner i nanometerstorlek, och därigenom höja resonansfrekvensen, erhålls en ökad masskänslighet. Därmed har lithografi-tekniker som elektronstråle-lithografi, atomkraftsmikroskopi baserad nanolithografi samt direkt laser-lithografi undersökts för stuktureringen av nanoresonatorer på CMOS. Resonatorer med en bredd av 400 nm, en tjocklek av 600 nm och en längd av 20 µm, som har en resonansfrekvens i storleksordningen 1.5 MHz har tillverkats på standard CMOS. Den utvecklade fabrikationstekniken kan även tillämpas på mer avancerade CMOS-teknologier.

Tillverkade strukturer har karakteriserats i luft och i vakuum och masskänsligheten har undersökt genom att placera punktmassor på resonatorn. Härigenom har en masskänslighet bestämts i storleksordningen av attogram (10^{-21} kg). Detta är i samma storleksordning som en enda medelstor biomolekyl, t.ex. hemin.

Möjliga användningsområden finns inom biosensorindustrin, inom gasdetektion av farliga ämnen som t.ex. sprängmedel och nervgaser, inom diagnostisering av gassystem. Ytterligare ett tillämpningsområde finns inom karakteriseringen och kalibreringen av avancerade atom- och molekylärstråle-lithografisystem.

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Chapter 1

Introduction

A sensor is a system which senses a specific force, compound or physical phase change and renders an analyzable data output. A sensor can be exemplified as consisting of three major parts, Fig. 1.1(a), a sensing layer, a transducer and an actuator. An example of an optimized chemical sensor used by everyone, all the time, is the nose. The sensation of smell is nothing but small quantities of chemicals which are sensed by the olfactory membrane inside the nose, as illustrated in Fig. 1.1(b). The olfactory membrane is the biological recognition element, the nerve cells are the transducers of the response of the olfactory membrane and finally our brain is the actuator which transforms the nerve signal into a sensation of smell. Today we have the possibility to mimic nature and develop artificial noses [1] based on cantilever sensor arrays capable of multiple component detection.

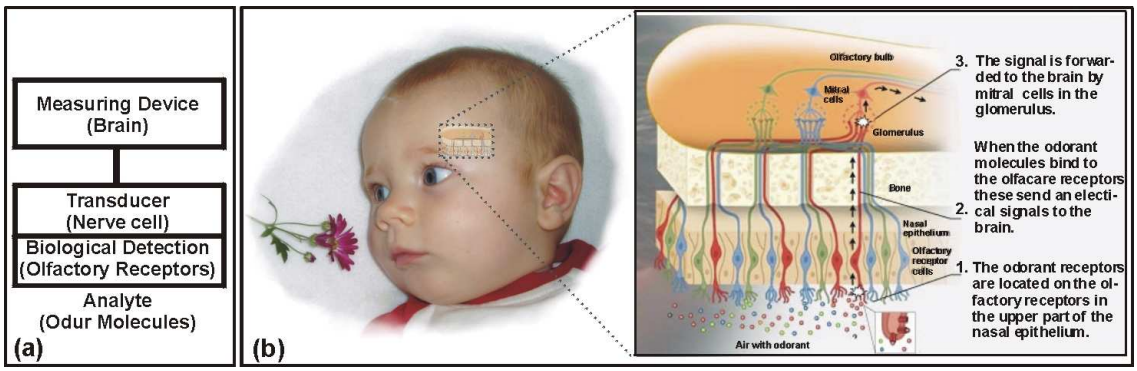

Figure 1.1: *Schematic representation of the parts of a sensor (a) and the analogy with the human nose (b).*

In order to have biosensors which meet the needs from industry, e.g. the pharmaceutical industry, a few demands need to be fulfilled. The sensor must achieve high sensitivity, it needs to be fast, preferably have some degree of parallelization, and perhaps most importantly it should be cheap. Cantilever sensors fulfill all these demands.

1.1 Cantilever Based Sensing

Micromachined cantilevers have been used for force sensing since the 1980's as a result of the development of scanning probe microscopy (SPM) techniques initiated by the invention of scanning tunnelling microscopy in 1982 by Binning *et al.* [2]. Scanning force microscopy (SFM) [3] is a technique based on the detection of force due to tip-sample interaction as a micrometer sized cantilever having a sharp tip at the apex, is scanned over a surface as illustrated in Fig. 1.2.

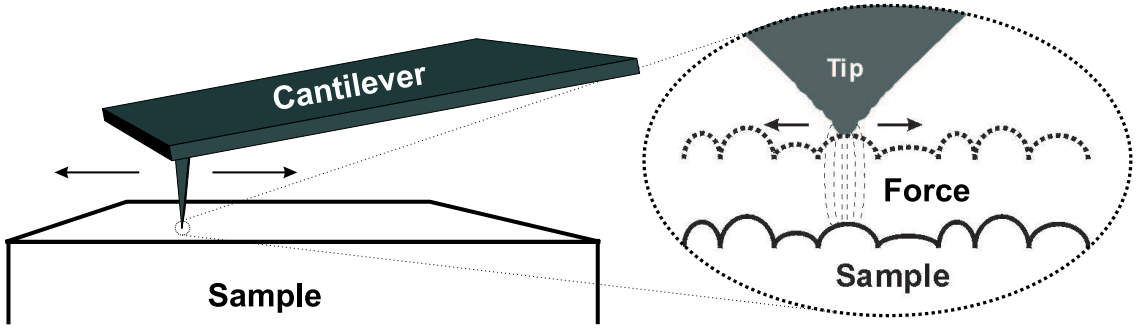

Figure 1.2: *Illustration of the principle of SFM. The forces interaction between a sharp tip and the surface can be used for high sensitivity surface metrology.*

The force acting on the tip bends the cantilever which acts as a force transducer. Since then the use of micromachined cantilevers have not only been restricted to force sensing, but also for biosensor applications. In 1995 Ratieri *et al.* [4] measured surface stress changes of an SFM cantilever caused by the adsorption of molecules onto one side of the cantilever. Today cantilevers are used for sensing of DNA, proteins, antigen-antibody reactions, and gases. [5][6][7][8][9]

The major benefits of using cantilever sensors are:

- High sensitivity
- Real time measurements in situ
- Label free detection
- Possible to Miniaturize
- High trough-put fabrication
- Possible to fabricate and measure on arrays of cantilevers

Furthermore, due to the development of batch process fabrication technologies for the silicon (Si) integrated circuitry (IC) business, micromachining of Si cantilevers has become a low-cost task.

Some specific disadvantages using cantilevers as sensors include:

- Mechanism of surface stress change not fully understood.
- Sensitive to everything (e.g. unspecific binding of molecules, changes in temperature, pressure, viscosity, or turbulence)
- Detection in liquid limits the methods for actuation/readout.

Cantilever sensing can be divided into two categories, as illustrated in Fig. 1.3:

- Static cantilever measurements; associated with the detection of a static deflection of the cantilever.
- Dynamic cantilever measurements; associated with the detection of a resonance frequency change as a result of changed mass and surface stress of the cantilever system.

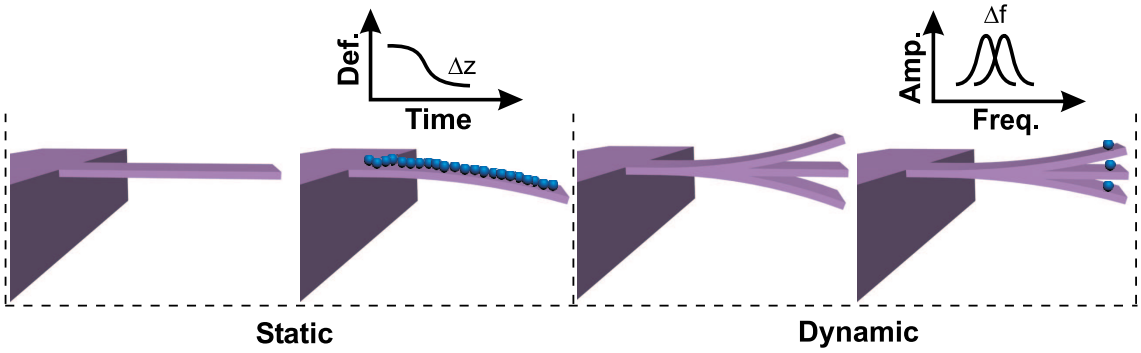

Figure 1.3: *Schematic representation of static and dynamic cantilever sensing.*

1.1.1 Static System

Static cantilever systems are based on the detection of static cantilever deflection. Such systems can be used for biosensing where a molecule/cantilever reaction causes cantilever surface stress changes. Another possibility is to use bimetallic cantilever systems for temperature sensing, monitoring the deflection of the bimetallic cantilever due to temperature changes. The artificial nose system developed by Baller *et al.* [1] was used for high sensitivity detection of various alcohols by coating the cantilever with a thin polymer layer, and Fritz *et al.* [5] used a similar cantilever array for monitoring DNA hybridization. Wu *et al.* [6] describes a method to use similar microcantilever arrays for the detection of prostate cancer specific antigens in human serum.

A benefit of using static cantilever measurements compared to dynamic cantilever measurements is that it offers a degree of simplicity since no actuation method needs to be considered. The disadvantages is that generally careful calibrations are needed and also the presence of an on-chip reference system is crucial in order to reduce the effects of unspecific events.

Static Readout

The readout is traditionally achieved by means of optical detection [10], as in common SFM systems, for which a laser beam is reflected on one side of the cantilever and the position of the reflected beam is monitored using position sensitive photo detectors. Other optical detection techniques are based on diffraction or interferometric detection. [11][12]

Another detection technique is piezoresistive readout [13][14]. When most materials are strained the strain induces changes of the electrical resistivity of the material. However, for a piezo-resistive material this effect is much larger compared to other materials. Single crystalline Si (s-Si) is piezoresistive, and combined with excellent mechanical properties it is often used as structural material for cantilever sensors. The change in resistance due to changes of surface stress is often detected by adopting a Wheatstone bridge configuration. Some benefits of piezoresistive read-out are that they are unaffected by optical artifacts which might arise as one is measuring in a liquid medium, there is no need for bulky optical equipment, or for laser alignment, and the read-out electronics can be integrated on a single chip platform.

1.1.2 Dynamic System

Dynamic cantilever measurements are based on measuring the resonance frequency of a cantilever, and the change in resonance frequency as matter adsorb onto the cantilever. The resonance frequency change is due to the change in mass as well as the change in surface stress of the cantilever. The merits compared to static cantilever measurements is that dynamic cantilever measurements give both absolute information regarding the mass of the adsorbed compound as well as the surface stress without the need of careful calibration. Ono *et al.* [15] describe the detection of hydrogen storage in carbon nanotubes deposited on a microcantilever. Thundat *et al.* has demonstrated the use of polymer coated microresonators for vapour detection with picogram sensitivity [16] as well as radiation dosimetry [17]. Ilic *et al.* [18] demonstrated the possibility to measure the mass of single viruses having a average mass of the order of a few femtograms.

Dynamic measurements are not well suited for measurements in a liquid medium due to the liquid damping. Compared to static systems the actuation of the cantilever needs to be considered. In the following sections some main actuation and read-out methods will be described, Fig 1.4.

Dynamic Actuation

The actuation of micrometer sized objects into mechanical resonance is a non-trivial task. The most common actuation method adopted from SFM applications is by piezoelectrical means [7][20][21]. Piezoelectrical materials induce electric charge as they are mechanically strained. Consequently, imposing a sinusoidal bias perturbation on a piezoelectrical material induces a sinusoidal mechanical response. In SFM

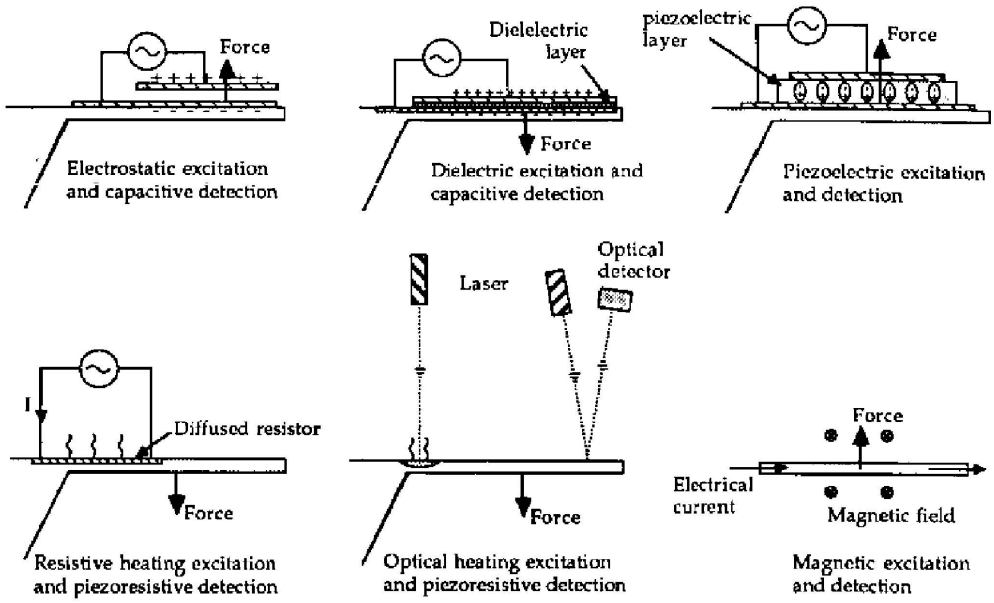

Figure 1.4: *Schematic representation of various dynamic cantilever actuation and read-out principles [19].*

applications the cantilever is mounted on a piezoelectric plate and when a sinusoidal bias is applied the piezoelectric plate starts to vibrate. By sweeping the frequency of the bias it may initiate a mechanical resonance mode of the cantilever. The benefits of piezoelectric actuation are, low power consumption, and miniaturizability on a single chip. A disadvantage is that common piezoelectric materials, e.g. zinc oxide (ZnO) or lead zirconate titanate ($Pb(Zr,Ti)O_3$), are not compatible with IC processing.

Thermal actuation can be achieved by optical heating by focusing a periodically activated laser beam on the cantilever. The irradiation generates heat stress which can actuate the cantilever into resonance. Lavrik *et al.* [22] used the technique for the detection of the chemisorption of 11- mercaptoundecanoic acid on the surface of gold-coated microcantilvers with a sensitivity of the order of femtogram. Another approach using thermal actuation is by adding an additional heating resistor on the bottom of a composite cantilever. When the composite cantilever is heated, by running a current through the resistor, the difference in heat expansion of the composite materials will give rise to a bending moment (bi-morph effect). Hagleitner *et al.* [23] have reported on actuation frequencies of 380 kHz using CMOS integrated cantilevers based on piezoresistive readout achieving detection of toluene at the single ppm level. A disadvantage of using thermal actuation is related to the fast cooling time constant needed for the composite materials to ensure excitation at higher frequencies. Furthermore, the heat generation might affect the properties as a chemical sensor since

heat can modify or destroy the compound which is to be measured.

Magnetic actuation can be achieved by adding a magnetic material on the cantilever and applying an external sinusoidal magnetic field creating a sinusoidal bending force acting on the cantilever. Another approach is by applying an sinusoidal current to a cantilever having an incorporated conductor, and at the same time applying a constant external magnetic field. This generates Lorentz forces which initiate a mechanical vibration. The benefits of magnetic actuation is low power consumption (if the magnetic field is strong enough). The disadvantage consist of increased fabrication complexity since a permanent magnet must be incorporated on the sensor.

Electrostatic actuation is achieved by placing the cantilever close to a fixed parallel plate driver electrode. As an sinusoidal bias is applied to the driver electrode the electrostatic interaction between the driver and the cantilever induces a sinusoidal force (attractive/repulsive) acting on the suspended cantilever, which initiates a mechanical vibration. The distance between the cantilever and the driver should be of the order of a µm in order to reduce the actuation voltage needed. The technique has been used by Blanc *et al.* [24] for dynamic mode SFM. The technique is suitable for detection in gas environment, especially in vacuum due to the reduced damping between cantilever and driver. The disadvantages are that this system can not be operated in a liquid due to Faradic currents.

Dynamic Read-Out

Another challenge is the read-out of the tiny vibrations, of tiny cantilevers, at high frequencies. As for static read-out the most common dynamic read-out method is still to use optical detection as in SFM. Such systems use a position sensitive photodetector to detect the reflected laser beam from the apex of the cantilever. This is a sensitive method but due to the finite size of the laser beam the cantilever needs to have a width of at least a few micrometers. Another optical detection technique which enables resonance measurement on nanometer sized structures is laser doppler vibrometry [25]. Laser doppler vibrometry is based on measuring the doppler shift of the reflected laser beam from the cantilever. Kim *et al.* [26] has used the technique on 100 nm wide, 2 µm long and 300 nm thick Si resonators measuring resonance frequencies of 91 MHz. The common weakness of optical read-out techniques is the difficulties arising when measuring in liquids, mainly due to optical adsorption and diffraction phenomena. Furthermore, they need lasers, photo detectors or more advanced optics, and preferably long beam pathways which results in a bulky measurement system with reduced possibility for miniaturization on a single chip platform.

Piezoresistive read-out is another common read-out technique since the most common cantilever materials, single crystalline silicon and poly crystalline silicon both are piezoresistive materials (at appropriate doping levels). The change in resonance frequency is measured as a change in the resistivity of the incorporated piezoresistors. The method enables integration on a single chip and Lange *et al.* [27] has demonstrated

measurement of gas-phase concentrations of n-octane and toluene in the single-ppm range. However, the method limits the miniaturization of the cantilever to the µm-regime since piezoresistor wiring needs to be fitted on to the cantilever.

The reverse process to the magnetic actuation principle can be used for detection. The vibration of a cantilever with a incorporated conductor, in a constant magnetic field, generates an induced sinusoidal voltage which is measured. [28]

Capacitive read-out is achieved by placing the cantilever in close proximity to a fixed parallel plate electrode. As the cantilever vibrates a sinusoidal capacitance is generated between the cantilever and the electrode, which is a measure of the cantilever resonance. The method has been used for SFM applications [24][29]. Capacitive read-out is highly suitable for miniaturization on a single chip platform, and is ideal for gas phase operation. However, careful design of the cantilever/electrode system needs to be conducted in order to reduce the air damping between the cantilever and electrode structure. The distance between the cantilever and electrode must be small, of the order of a few µm or below, and preferably the thickness/width-ratio should be large giving a large surface area towards the driver electrode in order to have a measurable capacitance signal. As the cantilever area facing the driver electrode is reduced the capacitance is also reduced. A small capacitance signal necessitates some kind of integrated electronics in order to reduce the noise level caused by the parasitic capacitance contribution from wiring and external electronics, which could entirely screen the capacitance signal originating from the vibration of the cantilever.

1.2 CMOS integrated cantilever sensor systems

CMOS integration has been an attractive route for cantilever sensing due to the possibility to add on "smart" features such as frequency tracking and Q-factor enhancement [8][30][31]. Pioneering work has been achieved by Baltes *et al.* [8][23][32] who in 1989 highlighted a new approach based on system-on-chip (SoC) integrating MEMS with CMOS. The realization of CMOS integrated cantilever sensor systems can be divided into three fabrication approaches: pre-processing, intermittent processing, and post-processing.

1.2.1 CMOS Pre-processing

Sensor fabrication by CMOS pre-processing is achieved by first making the cantilever/transducer structures and then afterwards initiating the CMOS fabrication. This allows a wide range of materials and processes to be used for the making of the cantilever/transducer since high temperature (T>400°C) processing may be used. This approach has been used by e.g. Sandia National Laboratories [33] in their MM/CMOS process in which the poly-silicon resonator structure is placed in a shallow trench, the wafer is planarized, and the poly-silicon structures are buried and sealed inside the trench, Fig. 1.5. The planarized wafers are then used as start-

ing material for the conventional CMOS processing. After the CMOS processes the CMOS is passivated and the trench area is reopened, and the microstructures are released. A weakness of the pre-processing approach is that the method necessitates that the IC foundry will accept pre-processed wafers. This is seldom the case since IC foundries are very cautious not to introduce any contaminations to their fabrication environment, which would reduce their yield.

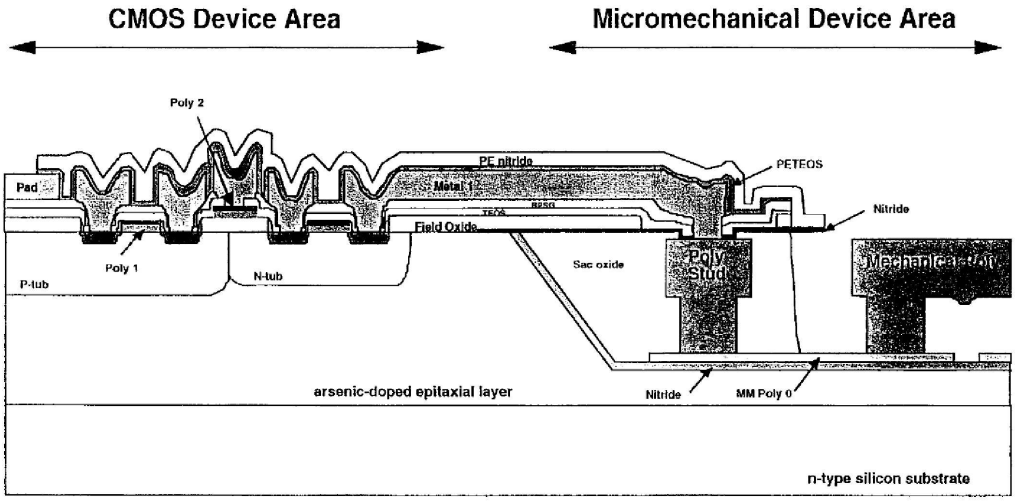

Figure 1.5: *Cross sectional illustration of the Sandia National Laboratory MM/CMOS process (CMOS pre-process) [33] showing the MEMS gas sensor structure embedded in the CMOS.*

1.2.2 CMOS Intermittent processing

In intermittent CMOS processing the degree of influence on the CMOS due to the device fabrication depends on in which step the structuring of the mechanical device is introduced. By fabricating the mechanical device after the most sensitive CMOS processes, such as the formation of the gate oxide, a reduced impact of the CMOS functionality compared to the pre-processing approach can be achieved. However, the reduced functionality impact comes at the expense of a reduced thermal process window, since the diffusion of dopants needs to be prevented. Some examples of projects which have been using this approach are the BiMEMS accelerometers by Analog Devices [34] (Fig. 1.6), and BiCMOS pressure sensors by Siemens [35].

1.2.3 CMOS Post-processing

In CMOS post-processing the mechanical device is made after the completion of the CMOS process. The CMOS process is not altered and hence the CMOS designers have a large freedom in designing the CMOS, which however comes at the expense of the freedom of the MEMS/NEMS-designer. Since most companies/research facilities

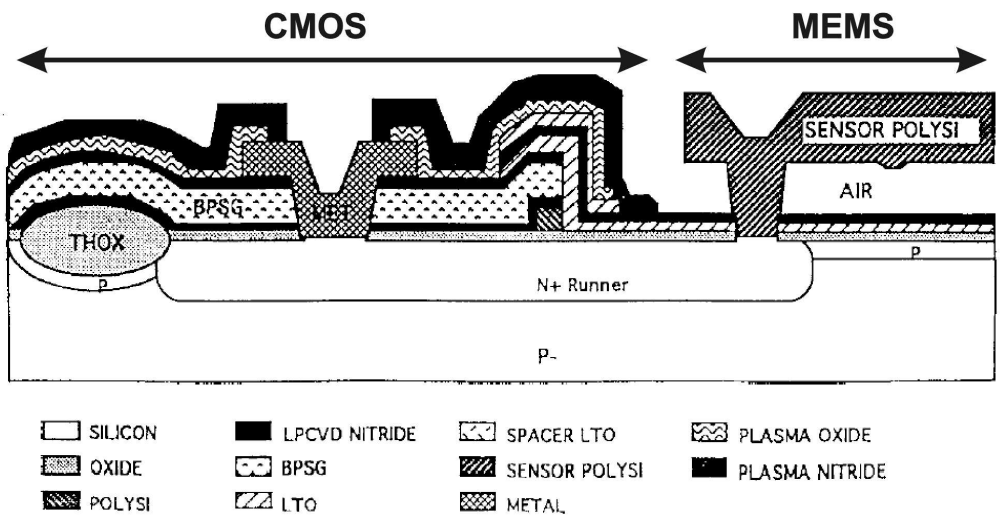

Figure 1.6: *Cross sectional illustration of the BiMEMS capacitive accelerometer system by Analog Devices [34].*

do not have their own IC foundry the post-process approach becomes an attractive path since they can buy standard CMOS at a lower cost and conduct the final micromachining themselves. No time or money is spent on CMOS process optimization as for the pre- and intermittent CMOS integration approaches. The disadvantage is that the thermal process window is now even more limited compared to the intermittent approach (T<400°C) and growth of materials such as poly-Si is not feasible. There are several examples of sensors based on CMOS post-processing, e.g. accelerometers [36], pressure [37], and radiation sensors [38].

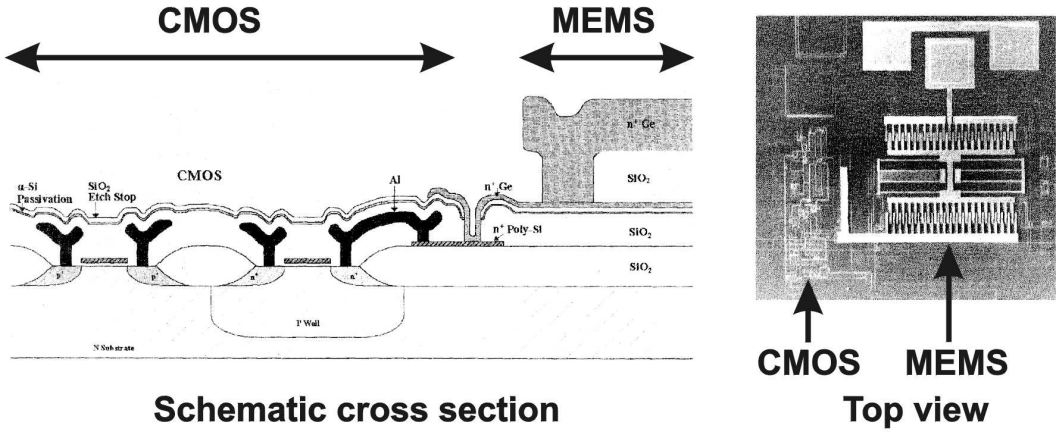

Figure 1.7: *Cross sectional illustration of the UC Berkeley Modular Integration of CMOS and polycrystalline germanium microstructures [39]. Poly-Ge comb-drive microresonators integrated with trans-resistance CMOS amplifiers were realized by adopting conventional low pressure chemical vapor deposition followed by rapid thermal annealing.*

1.2.4 Hybrid integration

In most cases, the CMOS integration problems for SoC approaches have been solved by making a compromise on the global performance and by trying to make the different fabrication technologies compatible. Even if some have achieved product status, it remains a challenge to merge MEMS/NEMS devices on CMOS at a reasonable cost and high performance. System-in-package (SiP) is a different approach which circumvents problems related to CMOS integration. SiP's include e.g. flip-chip techniques [40] [41] (Fig. 1.8) and multi-chip modules [42]. The common idea for these approaches is that the CMOS circuitry and the MEMS/NEMS device are made on separate chips/dies which are combined by a final bonding-step to a common substrate. This gives ultimate freedom and flexibility for the MEMS- and CMOS-designer since standard processes, components, as well as standard packaging can be used. Furthermore, such techniques have a cost advantage at low production volumes. However, when it comes to the noise performance, CMOS integration still has the advantage of better performance improvement capabilities .

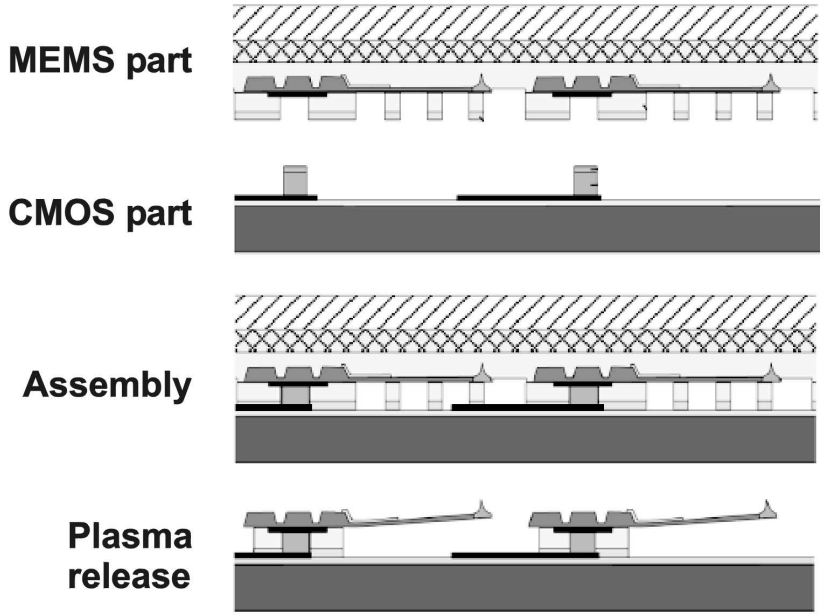

Figure 1.8: *Process flowchart showing a cross section of the basic cantilever-transfer processing steps used by IBM in their cantilever based data storage project (Millipede) [41].*

1.3 Thesis Outline

The aim of my Ph.D. has been to develop nanoresonators for ultra sensitive mass detection purposes integrated with standard CMOS using a post-process integration approach, as outlined within the *Nanomass II* project described in chapter 2.

The development of dynamic cantilever systems at the department was initiated in

year 2000 by the EU FP4 *Nanomass I* project initiated by G. Abadal, Z. Davis, A. Boisen, N. Barniol and F. Perez-Murano. The second phase was initiated in 2002 though the EU FP5 *Nanomass II* project in which I started my Ph.D. From the *Nanomass I* project it was found that no appreciable out-put signal was measurable for plain poly-Si cantilevers based on electrostatic actuation and capacitive readout, hence CMOS integration was needed.

My objective has been to design and fabricate silicon nanoresonators onto pre-processed CMOS chips. In particular, I have developed the technology platform to combine standard CMOS technology with post-process nanofabrication of NEMS. This includes nanocantilever fabrication using lithography techniques such as:

- SFM nanolithography (SFL).
- Direct write laser lithography techniques (DWL).
- Electron beam lithography (EBL).
- Combination of the above technologies.

The different nanolithography processes have been compared in order to evaluate the advantages of these techniques in terms of CMOS compatibility, yield, and minimum resolution.

In this thesis my effort has been to give a clear view of the project. I will describe its main theoretical and technological constituents, and I will show the characterization as well as mass measurements on finalized devices.

1.3.1 Chapters Outline

Chapter 2: The chapter contains a brief description of the *Nanomass II* project including areas of responsibility and work-packages.

Chapter 3: The theory of cantilever resonators is presented as well as a brief discussion regarding the major noise sources.

Chapter 4: The design of the CMOS is discussed and a small signal model is presented. The fabrication of standard CMOS and SOI-CMOS is described.

Chapter 5: The lithography techniques used within the project are presented.

Chapter 6: The process of integration of cantilevers onto CMOS is described.

Chapter 7: This chapter contains the characterization of the fabricated devices.

Chapter 8: Discussion.

Chapter 2

The Nanomass Project

The objective of the *Nanomass II* project has been the development of technologies for the combination of CMOS circuit fabrication with nanotechnology processes. Nanofabrication is applied for the realization of mechanical mass sensors based on resonant silicon cantilevers integrated monolithically with CMOS signal conditioning circuits. The excitation and detection of the cantilever displacement is performed through the integrated CMOS circuitry. The monolithic integration approach utilizes one of the poly-silicon layers of the standard CMOS as the structural layer for the NEMS, which is defined by novel nanofabrication methods such as electron beam lithography (EBL), scanning force microscopy based nanolithography (SFL), and direct write laser lithography (DWL).

Mass detection is based on monitoring the resonant frequency shift of the cantilever when nano/micrometer-sized particles or molecules are deposited on the cantilever. The cantilever is excited electrostatically by means of a fixed electrode separated by a μm gap to the parallel cantilever. A change in the cantilever resonance frequency is detected as a capacitance change. Electrostatic transduction in the nanometer-size regime requires the minimization of the parasitic capacitance. This is due to that the magnitude of the capacitive current generated by the oscillation is proportional to the coupling capacitance (order of 10^{-16} F) between the cantilever and the driver electrode. Consequently, the readout circuitry has to be integrated with the NEMS device "on-chip" in order to eliminate the parasitic capacitance introduced by the external bonding pads and wires, which otherwise would screen the resonance signal. The goal of the project has been the development of a ultrasensitive system-on-chip based mass sensor, based on a nanoelectromechanical device and integrated read-out circuitry.

2.1 Work-Packages

The *Nanomass II* consortium group and the expertise of each group are as follows:

- **Autonomous University of Barcelona** (Spain): CMOS circuit design. Electrical characterization. Sensor modelling.

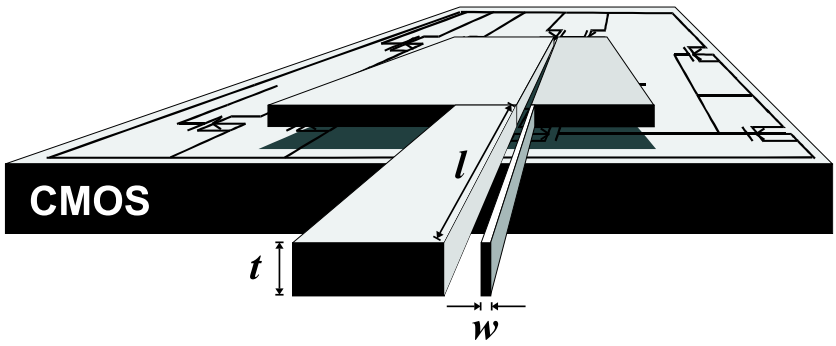

Figure 2.1: *Schematic illustration of the SoC principle of the Nanomass II project.*

- **Department of Micro and Nanotechnology of the Technical University of Denmark**: Si-processing, general surface micromachining. MEMS/ NEMS fabrication by laser and SFM nanolithography. Systems characterization. Biosensors.
- **The National Microelectronics Center** (Spain): CMOS circuit fabrication and microsystems in general.
- **Lund University** (Sweden): Nanolithography techniques such as Electron beam lithography and Nanoimprint lithography.

The work packages (WP) and the mayor responsibility of the work packages are:

- **WP1**: Fabrication of sensors based on poly-Si cantilevers based on post-process CMOS surface micromachining. (UAB/CNM/MIC)
- **WP2**: Fabrication of sensors using SOI technology. The standard CMOS circuitry is fabricated using a silicon on insulator (SOI) wafer. This process requires challenging pre-processing of the SOI, after which the CMOS is fabricated. Finally, the cantilever is fabricated by post-processing similar to WP1. (UAB/CNM)
- **WP3**: Fabrication of metal cantilevers by electroplating. The WP was halted during the first year.
- **WP4**: Fabrication of nano-cantilevers using electron beam lithography. Evaluation of the CMOS compatibility using EBL in the post-process, followed by fabrication of cantilevers with a width of 500 nm and below. (LU/MIC)
- **WP5**: Fabrication of nano-cantilevers using nanoimprint lithography. Evaluate NIL for large scale nanofabrication of NEMS devices with CMOS. (LU)
- **WP6**: Evaluation of applications. (All)

- **WP7**: Functional evaluation. Characterization of the performance of the sensor in both air and vacuum. (MIC/UAB)
- **WP8**: Dissemination and implementation. Evaluation of possible industrial applications. (UAB)

Chapter 3

Theory

In this chapter the formalism for the mechanical theory of cantilevers will be presented. The focus is on deriving the analytical expressions related to the resonance frequency, quality factor and noise, needed for the appropriate design of cantilever sensors.

For a more detailed theoretical description the reader is suggested to use one of the several text books which covers the topic, e.g. "*Scanning Force Microscopy*" by Sarid [43], "*Vibrational Problems In Engineering*" by Timoshenko *et al.* [44], or "*Theory Of Vibration With Applications*" by Thomson *et al.* [45].

3.1 Cantilever Theory

In order to design a cantilever sensor system properly a profound knowledge of the properties of the system is needed. Here I will first derive the expression for the spring constant and then derive the expression for the resonances frequency of a rectangular cantilever clamped at one end, as schematically shown in Fig. 3.1.

Spring Constant

The lateral deflection of a cantilever as in Fig. 3.1. having a length l, a thickness t, and a width w, is a function of the bending moment M, the Young's modulus E, and the moment of inertia of a rectangular beam $I = \frac{tw^3}{12}$ according to:

$$\frac{d^2x(y)}{dy^2} = \frac{M}{EI} \tag{3.1-1}$$

The bending moment produced by the force acting at any given point a along the length of the cantilever is given by:

$$M = F(y - a) \tag{3.1-2}$$

Insertion of Eq. 3.1-2 in Eq. 3.1-1. considering a cantilever clamped at one end and integrating twice results in the following expression:

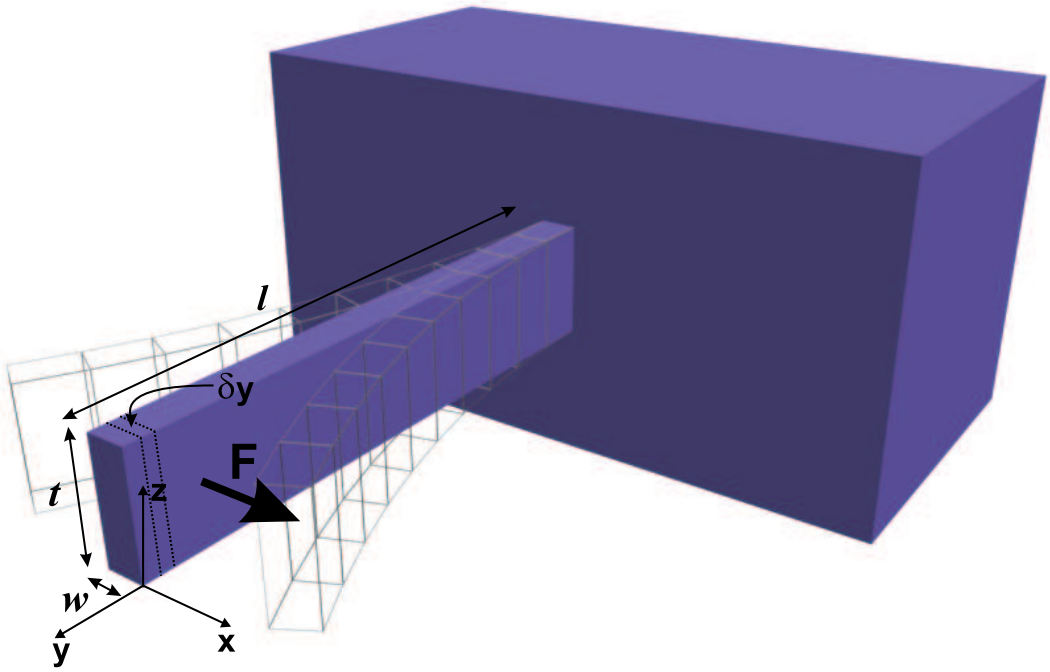

Figure 3.1: *Schematic illustration of cantilever system having a length l, a thickness t and a width w.*

$$x(y) = \frac{Fy^2}{6EI}(y - 3a) \tag{3.1-3}$$

and setting $y = a = l$ renders:

$$x(l) = -\frac{l^3}{3EI}F \tag{3.1-4}$$

The definition of the spring constant k is given by Hooke's law which contains the force F acting on the cantilever and the deflection $x(l)$ of the cantilever:

$$k = \left|\frac{F}{x(l)}\right| \tag{3.1-5}$$

by insertion of Eq. 3.1-4. into Eq. 3.1-5. one gets the expression for the spring constant of a cantilever according to:

$$k = \frac{3EI}{l^3} \tag{3.1-6}$$

Euler-Bernoulli Beam Theory

By defining the shear force V as:

$$V = \frac{\delta M}{\delta y} \tag{3.1-7}$$

and deriving the equation of motion for a cantilever element, with a length δy, by a shear force dV gives us:

$$dV = -\delta m\, \ddot{x} = -\rho \Gamma \delta y \frac{\delta^2 x}{\delta t^2} \tag{3.1-8}$$

in which $\Gamma = wt$ is the cross section, and ρ is the mass density. After combining Eq. 3.1-8. with Eq. 3.1-1. and assuming EI as a constant one gets:

$$\begin{aligned} \frac{\delta^2}{\delta y^2}\left(EI\frac{\delta^2 x}{\delta y^2}\right) &= -\rho\Gamma\frac{\delta^2 x}{\delta t^2} \Rightarrow \\ \frac{\delta^4 x}{\delta y^4} + \frac{\rho\Gamma}{EI}\frac{\delta^2 x}{\delta t^2} &= 0 \end{aligned} \tag{3.1-9}$$

which is the one-dimensional Euler-Bernoulli beam equation of a homogeneous cantilever beam. The general solutions to Eq. 3.1-9. under transverse vibration are given by:

$$x(y,t) = x(y)\cos\left(\omega_n t - \chi\right) \tag{3.1-10}$$

in which n is the order of the mode and χ is an arbitrary phase constant. By defining the parameter κ in the form:

$$\kappa_n^4 = \omega_n^2 \frac{\rho\Gamma}{EI} \tag{3.1-11}$$

Eq. 3.1-9. is reduced to:

$$\frac{\delta^4 x}{\delta y^4} - \kappa_n^4 x = 0 \tag{3.1-12}$$

which has the solution:

$$x(y) = A\cosh\kappa_n y + B\sinh\kappa_n y + C\cos\kappa_n y + D\sin\kappa_n y \tag{3.1-13}$$

By substituting the necessary boundary conditions into the general solution, Eq. 3.1-13., one solves the fourth order differential equation for a cantilever beam clamped at one end:

$$\text{At } y = 0 \quad \left\{ \begin{array}{ll} x & = 0 \\ \frac{dx}{dy} & = 0 \end{array} \right\} \quad \begin{array}{l} \therefore A = -C \\ \therefore B = -D \end{array}$$

$$\text{At } y = l \quad \left\{ \begin{array}{lll} M = 0 & \text{or} & \frac{d^2x}{dy^2} = 0 \\ V = 0 & \text{or} & \frac{d^3x}{dy^3} = 0 \end{array} \right\} \quad \therefore \cosh \kappa l \cos \kappa l + 1 = 0$$

The last equation is solved by a number of values for κl which corresponds to each resonance mode. The values for the first three modes are displayed in Tab. 3.1.:

mode (n)	$\kappa_n l$
Fundamental	1.875
First Higher	4.694
Second Higher	7.855

Table 3.1: Constants for the first three modes of a resonating cantilever.

Since the mass of a cantilever is distributed along the length of the cantilever the effective mass m_{eff} needs to be used when the expression for the resonance frequency is derived. The effective mass is given by:

$$m_{eff} = \frac{3}{(\kappa_n l)^4} m = r_n m \qquad \therefore r_0 \cong 0.2427 \tag{3.1-14}$$

The expression of the undamped resonance frequency of a rectangular cantilever has the form:

$$f_n = \frac{1}{2\pi} \sqrt{\frac{k}{r_n m}} = \frac{(\kappa_n l)^2}{2\pi\sqrt{12}} \frac{w}{l^2} \sqrt{\frac{E}{\rho}} \tag{3.1-15}$$

and the resonance frequency for the fundamental mode is reduced to:

$$f_0 \cong 0.1615 \frac{w}{l^2} \sqrt{\frac{E}{\rho}} \tag{3.1-16}$$

It is worth noting that the expression for the resonance frequency is independent of the thickness of the cantilever. Hence, it is viable to fabricate thick cantilevers for capacitive detection purposes without degrading the sensitivity, due to a reduced resonance frequency.

An additional mass Δm, uniformly distributed on the cantilever, results in a changed fundamental resonance frequency $f_{\Delta m}$ according to:

$$\begin{aligned} f_{\Delta m} &= \frac{1}{2\pi}\sqrt{\frac{k}{r_0(m+\Delta m)}} \Rightarrow \\ m+\Delta m &= \frac{k}{4\pi^2 r_0 f_{\Delta m}^2} \end{aligned} \tag{3.1-17}$$

by revising Eq. 3.1-17. using the plain mass of the cantilever one gets:

$$\Delta m = -\frac{k}{4\pi^2 r_0}\left(\frac{1}{f_0^2} - \frac{1}{f_{\Delta m}^2}\right) \tag{3.1-18}$$

or

$$f_{\Delta m} = \frac{f_0}{\sqrt{1+\frac{\Delta m}{m}}} \tag{3.1-19}$$

By using a first-order Taylor series expansion 3.1-19 is rewritten as:

$$\begin{aligned} f_{\Delta m} &\approx f_0\left(1-\frac{1}{2}\frac{\Delta m}{m}\right) \overset{f_{\Delta m}=f_0-\Delta f}{\Longrightarrow} \\ \frac{\Delta m}{\Delta f} &\approx 2\frac{m}{f_0} \end{aligned} \tag{3.1-20}$$

The calculated resonance frequency and the corresponding mass sensitivity for micro/nanoresonators are displayed in Tab. 3.2.

Width	Length	f_0	$\frac{\Delta m}{\Delta f}$
10.0 µm	355.7 µm	0.11 MHz	$1.5{\cdot}10^{-16}$ kg/Hz
1.0 µm	35.6 µm	1.12 MHz	$1.5{\cdot}10^{-19}$ kg/Hz
0.1 µm	3.6 µm	11.20 MHz	$1.5{\cdot}10^{-22}$ kg/Hz

Table 3.2: Comparison of resonance frequency for Si cantilevers having different dimensions but the same spring constant $k = 1$ N/m and thickness $t = 1$ µm. The Young's modulus is $E = 180$ GPa and the mass density is $\rho = 2.33 \cdot 10^3$ kg/m^3.

Hence, by reducing the cantilever dimensions to the nanoscale the theoretical mass resolution of resonator sensors increases dramatically.

3.2 The Quality Factor

The quality factor Q is a dimensionless parameter to model the energy loss of a mechanical system. The most common definition of the quality factor is shown in Eq.

3.2-1.

$$Q = 2\pi \frac{W_0}{\Delta W} = \frac{f_n}{\Delta f_{3dB}} \tag{3.2-1}$$

in which W_0 is the energy stored, ΔW is the energy lost per cycle, and Δf_{3dB} is the frequency bandwidth at the 3dB amplitude drop. The definition essentially does not put any restriction to the type of system.

The quality factor can also be derived from the Euler-Bernoulli beam equation [46] in the form:

$$Q = \frac{2\pi f_n \rho \Gamma}{\xi} \tag{3.2-2}$$

in which ξ is the damping coefficient per unit length and unit velocity. Hence, the quality factor is expected to increase linearly with an increase in resonance frequency, which is another reason for the down scaling of cantilevers.

For resonant systems, a high quality factor helps to increase the sensitivity of the resonant sensors and reduces the phase noise of the oscillators. There are several dissipation mechanisms that contribute to the damping ΔW for a MEMS/NEMS device. These can be divided into intrinsic, due to the physical structure of the MEMS/NEMS device, and extrinsic, due to viscous and turbulent flow of the surrounding media. The inverse of the total quality factor can be written as the inverse sum of all contributions, intrinsic and extrinsic:

$$\frac{1}{Q_{tot}} = \sum \frac{1}{Q_{int}} + \sum \frac{1}{Q_{ext}} \tag{3.2-3}$$

3.2.1 Intrinsic

Acoustic damping: Depending on the motion of the mechanical device, it can be slide film damping (viscous drag-laterally moving devices) or squeeze film damping (out of plane devices). In most of the cases acoustic damping is a combination of squeeze and slide film damping.

Material damping: This type of losses occur due to internal damping of solid materials. The main subclasses are thermoelastic damping, phonon-phonon interaction and defect caused dissipation.

Anchor losses: Resonant mechanical systems radiate some of the vibration energy through the support points (anchors), lowering the quality factor.

External load losses: One additional concern is the external system that interfaces to the resonators. The quality factor in the presence of an external loading (e.g. a feedback circuit to sustain oscillations) is called loaded quality factor.

3.2.2 Extrinsic

Molecular damping: The damping is caused by individual collisions of gas molecules with the resonator surface.

Viscous damping: This type of losses are caused by pressure independent viscous friction.

Turbulent damping: Close to atmospheric pressure the turbulent damping becomes proportional to the Reynolds number, i.e. proportional to the pressure.

3.3 Noise

Before the fabrication of nanoresonator systems an important issue needs to be addressed. If one succeeds in overcoming the challenges in fabricating the NEMS device, will one be able to utilize its full potential in terms of increased sensitivity, or will the sensitivity be screened by noise? The resulting question that needs to be answered is: what is the minimum frequency shift $\delta\omega_0$ that realistically can be resolved in a real measurement situation, and what is the corresponding ultimate mass sensitivity?

The general answer, as given by Cleland and Roukes [47], is obtained by integrating the weighted spectral density of the frequency fluctuation $S_\omega(\omega)$:

$$\delta\omega_0^2 \approx \int_{\omega_0-\pi\Delta\omega}^{\omega_0+\pi\Delta\omega} S_\omega(\omega)d\omega \tag{3.3-1}$$

The precise functional form of $S_\omega(\omega)$ depends on the physical noise processes that are operative. There are also extrinsic noise sources which are read-out specific and the noise due to electrostatic excitation. These are shortly discussed in section 3.4.

The major physical noise processes which need to be considered for a resonator gas sensor operating at room temperature are thermomechanical fluctuations as well as adsorption-desorption processes.

3.3.1 Thermomechanical Fluctuations

The thermomechanical frequency stability of a resonator having a resonance frequency ω_0 depends on the magnitude of influence from the thermally driven random motion of the resonator. The mean square thermal displacement $\langle x_{th}^2\rangle$ at a temperature T of a resonator having an effective mass m_{eff} satisfies the expression:

$$\frac{1}{2}k\langle x_{th}^2\rangle = \frac{1}{2}m_{eff}\omega_0^2\langle x_{th}^2\rangle = \frac{1}{2}k_BT \tag{3.3-2}$$

in which k is the spring constant and k_B is the Boltzmann's constant. The effective spectral density can be estimated by [47]:

$$S_{th}(\omega) \approx \frac{\omega_0^5}{Q^3}\frac{k_B T}{E_c}\frac{1}{(\omega^2-\omega_0^2)^2+\omega^2 f_0^2/Q^2} \tag{3.3-3}$$

in which $E_c = m_{eff}\omega_0^2\langle x_c^2\rangle$ is the maximum drive energy in the direction of resonance for the externally driven system, with a mean square driving amplitude $\langle x_c^2\rangle$.

The frequency fluctuation is given by integrating Eq. 3.3-1 using $S_{th}(\omega)$ from Eq. 3.3-3 over the measurement bandwidth Δb. In the case for $Q \gg 1$ and $2\pi\Delta b Q \ll \omega_0$ one arrives at the common expression:

$$\delta\omega_0 \approx \sqrt{\frac{k_B T}{E_c}\frac{\omega_0 \Delta b}{Q}} \tag{3.3-4}$$

From this it becomes obvious that an improved Q-factor renders an improved frequency resolution. Hence it is viable to design nanoresonators with high resonance frequency and high Q.

The corresponding minimum mass sensitivity δM_{th} is given by inserting Eq. 3.3-4 into Eq. 3.1-20 after which one gets:

$$\delta M_{th} \approx 2m_{eff}\sqrt{\frac{k_B T}{E_c}}\sqrt{\frac{\Delta b}{Q\ 2\pi f_0}} \tag{3.3-5}$$

The calculated mass sensitivity for various cantilever dimensions at realistic measurement conditions is displayed in Tab. 3.3.

Width	Length	f_0	$\frac{\Delta m}{\Delta f}$	δM_{th}
10.0 µm	355.7 µm	0.11 MHz	$1.5{\cdot}10^{-16}$ kg/Hz	$1.28{\cdot}10^{-16}$ kg
1.0 µm	35.6 µm	1.12 MHz	$1.5{\cdot}10^{-19}$ kg/Hz	$4.05{\cdot}10^{-19}$ kg
0.1 µm	3.6 µm	11.20 MHz	$1.5{\cdot}10^{-22}$ kg/Hz	$1.28{\cdot}10^{-21}$ kg

Table 3.3: Mass sensitivity limited by thermally driven frequency fluctuations for the Si resonators found in Tab. 3.2. For this example the measurement bandwidth is set to $\Delta b = 1$ kHz, the temperature is $T = 300$ K, the mean square vibrational amplitude $\langle x_c^2\rangle = 100$ nm, and as the resonators are driven in ambient air the corresponding $Q = 100$ is set quite low.

Hence for resonance based mass sensors it is beneficial to use nanoscaled resonators, justifying a small m_{eff}, a high resonance frequency, and a high Q, and to use a small measuring bandwidth. Furthermore, it should be possible to achieve high mass sensitivity at room temperature at ambient air conditions.

3.3.2 Adsorption-Desorption Processes

The random adsorption-desorption of gas molecules onto the resonator from the measurement medium is another noise source causing frequency fluctuations. The adsorption can be modelled by a flux-dependant adsorption rate r_a, in which the flux F_a is given by the Hertz-Knudsen formula according to:

$$F_a = \frac{p}{\sqrt{2\pi m_m k_B T}} \tag{3.3-6}$$

in which p is the pressure of the gas of the measurement medium, m_m is the mass of the gas molecule, and T is the temperature. The adsorption rate can be described as:

$$r_a = F_a \cdot s \cdot a^2 \tag{3.3-7}$$

in which s is the sticking coefficient ($0 < s < 1$) and a is the lattice constant of the cantilever compound. Here I believe that Cleland and Roukes [47] and Ekinci *et al.* [48] might make an error by not incorporating the a^2 term. This term is added since the flux should be in terms of flux per surface adsorption site, which is assumed to be one per a^2. F_a is in units of Hz/m^2 and s is dimensionless. This gives that for instance Fig. 5. in the article by Ekinci *et al.* [48] seems wrong.

The thermally activated desorption rate r_d is given by:

$$r_d = \exp\left(-\frac{E_b}{k_B T}\right) \cdot v_d \tag{3.3-8}$$

in which E_b is the binding energy and v_d is the desorption coefficient, which is of the order of the vibrational frequency of diatomic molecules, $v_d \sim 10^{13}$ Hz.

The resulting spectral density of the frequency fluctuations is given by [47]:

$$S_{a-d}(\omega) = \frac{2\pi\omega_0^2 N_a \sigma_{occ}^2 \tau_{cor}}{1 + (\omega - \omega_0)^2 \tau_{cor}^2} \left(\frac{m_m}{m_{eff}}\right)^2 \tag{3.3-9}$$

in which N_a is the number of sites available for adsorption, the variance in the site occupation probability is given by $\sigma_{occ}^2 = \frac{r_a r_d}{(r_a + r_d)^2}$, and the correlation time of an adsorption-desorption cycle is given by $\tau_{cor} = \frac{1}{(r_a + r_d)}$.

By inserting the expression for $S_{a-d}(\omega)$ in Eq. 3.3-1 and integrating one obtains an estimate of the frequency fluctuations due to adsorption-desorption processes according to:

$$\delta\omega_0 = \frac{m_m \omega_0}{2\pi m_{eff}} \sqrt{\sigma_{occ}^2 N_a \arctan(2\pi\tau_{cor}\Delta b)} \tag{3.3-10}$$

which yields a mass sensitivity according to:

$$\delta M_{a-d} \approx \frac{m_m}{2\pi} \sqrt{\frac{r_a r_d}{(r_a + r_d)^2} N_a \arctan\left(\frac{2\pi\Delta b}{r_a + r_d}\right)} \tag{3.3-11}$$

An estimate of the impact of N_2 gas adsorption and desorption (s=0.1) on the ultimate mass sensitivity of resonators at room temperature ($K = 300$) and at various pressures are displayed in Fig. 3.2 (1u=$1.66 \cdot 10^{-27}$ kg).

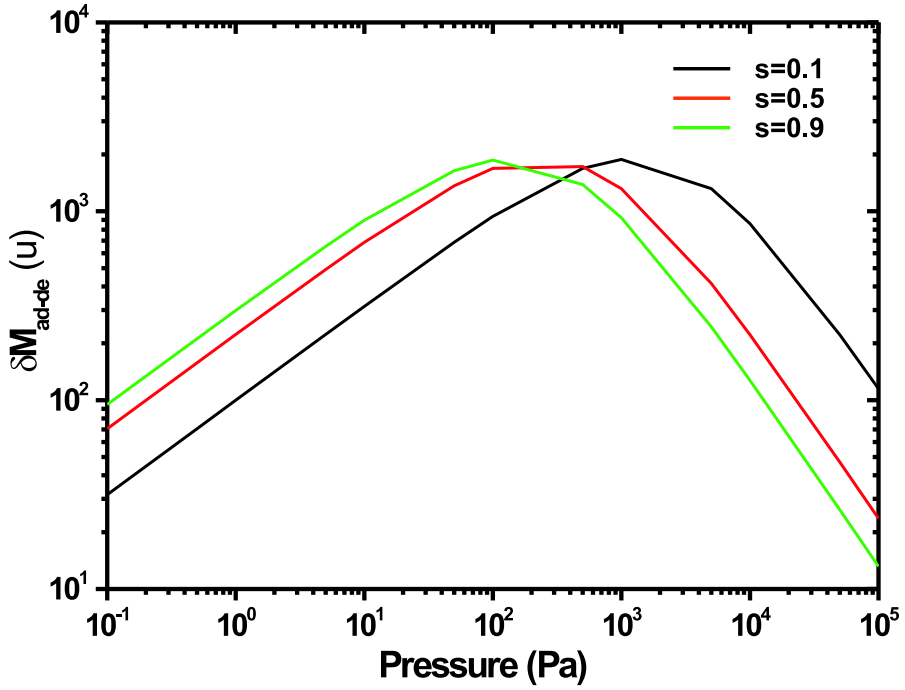

Figure 3.2: *Graph showing the calculated minimum detectable mass due to adsorption-desorption noise processes as function of pressure for a Si resonator having the dimensions:* $l = 20$ *µm,* $t = 0.6$ *µm,* $w = 0.5$ *µm, and* $f_0 = 1.77$ *MHz.*

The mass sensitivity was calculated for three sets of molecular sticking coefficients for Si resonators having the dimensions ($l = 20$ µm, $t = 0.6$ µm, $w = 0.5$ µm, $f_0 = 1.77$ MHz) similar to the cantilevers realized within this project. The measurement bandwidth is set to $\Delta b = 100$ Hz, the number of binding cites are estimated to be of the same order as the number of Si atoms on the surface $N_a \sim 4 \cdot 10^8$, and the desorption coefficient is $v_d = 4 \cdot 10^{-13}$ Hz. As expected, for very low pressure situations the minimum detectable mass is reduced since the desorption rate dominates, which is also the case for high pressure situations where the adsorption rate dominates. The noise due to adsorption-desorption processes reaches a peak when there is a balance in the adsorption rate and the desorption rate, which is reached at mbar pressure. The corresponding minimum detectable mass as a function of the measurement bandwidth at a pressure of $1.3 \cdot 10^2$ Pa (1 Torr) is shown in Fig. 3.3.

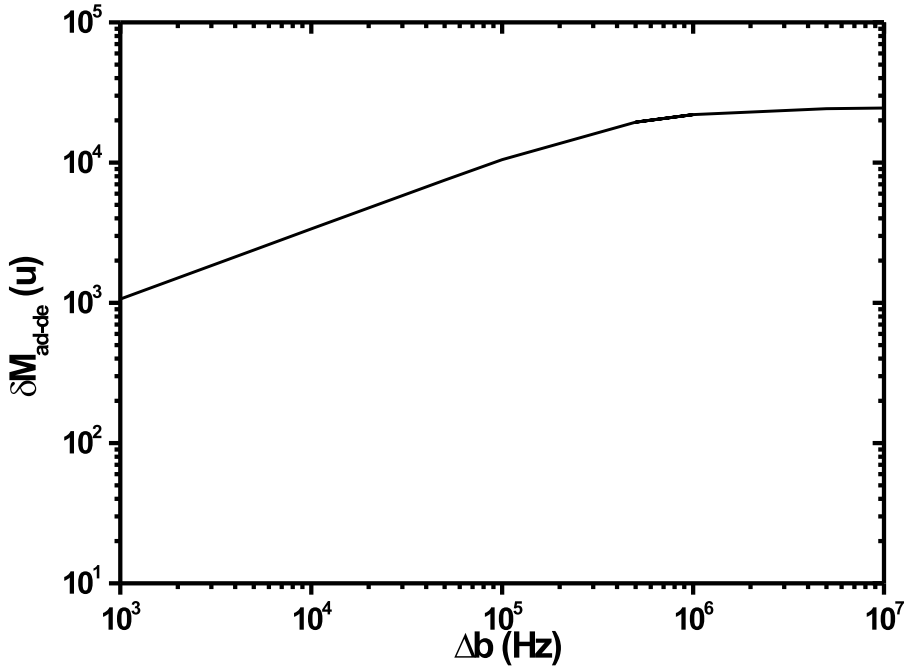

Figure 3.3: *Graph showing the calculated minimum detectable mass due to adsorption-desorption noise processes as a function of the measurement bandwidth at a pressure of* $1.3 \cdot 10^2$ *Pa.*

3.4 Spring Softening

Due to the chosen electrostatic actuation approach the issue of electrostatic perturbation arises. The perturbation due to the applied electric field exerts an electrostatic force on the resonator which effectively changes the spring constant of the resonator.

The total potential energy U stored in a resonator system as in Fig. 2.1. is a combination of the potential energy stored in the deflected cantilever and the energy stored in the parallel plate driving electrode capacitor C according to:

$$U = \frac{1}{2}k_{eff}\langle x^2\rangle = \frac{1}{2}k\langle x^2\rangle - \frac{1}{2}C\langle V_{net}^2\rangle \tag{3.4-1}$$

in which k_{eff} is the effective spring constant, k is the unperturbed spring constant, and $\langle V_{net}^2\rangle$ is the mean square applied net voltage. By taking the second derivative of Eq. 3.4-1. an expression for k_{eff} is deduced:

$$k_{eff} = k - \frac{1}{2}\langle V_{net}^2\rangle\frac{\delta^2 C}{\delta x^2} \approx k - \langle V_{net}^2\rangle\frac{\epsilon\Gamma_c}{d-x} \tag{3.4-2}$$

in which ϵ is the dielectric constant, Γ_c is the area of the capacitor and d is the initial separation between the cantilever and the driver electrode.

The effective resonance frequency due to electrostatic perturbation f_e is given by:

$$f_e = f_0\sqrt{1 - \frac{\zeta}{k}\langle V_{net}^2\rangle} \tag{3.4-3}$$

in which $\zeta = \frac{\epsilon\Gamma_c}{(d-x)^3}$.

V_{net}^2 is given by:

$$\begin{aligned} V_{net}^2 &= (V_{DC} + V_{AC})^2 \\ &= V_{DC}^2 + 2V_{DC}V_{AC} + V_{AC}^2 \\ &= V_{DC}^2 + 2V_{DC}V_{ac}\sin(\omega t) + V_{ac}^2\sin^2(\omega t) \\ &= V_{DC}^2 + 2V_{DC}V_{ac}\sin(\omega t) + \frac{1}{2}V_{ac}^2 + \frac{1}{2}V_{ac}^2\sin^2(\omega t) \;\Rightarrow \\ \langle V_{net}^2\rangle &= V_{DC}^2 + \frac{1}{2}V_{ac}^2 \end{aligned} \tag{3.4-4}$$

by which an expression for the effective resonance frequency can be rewritten as:

$$f_e \approx f_0 - \frac{f_0\zeta}{2k}(V_{DC}^2 + \frac{1}{2}V_{ac}^2) \tag{3.4-5}$$

As seen the resonance frequency scales with the square of the applied voltage, and an example of frequency tuning is described by Yao *et al.* [49] in which the possibility to tune the center resonance frequency position of MEMS resonators is achieved by adjusting the applied DC voltage.

Furthermore, it is apparent that the frequency stability is a function of the voltage. By differentiating Eq. 3.4-3 with respect to δV one can deduce the frequency fluctuations due to voltage fluctuations according to:

$$\delta f = \frac{f_0}{k}\zeta V\delta V \tag{3.4-6}$$

Hence, in order to minimize the electrical noise the restrictions are set by the voltage suppliers and the measuring instruments, meaning that the AC and DC voltage suppliers should have stable characteristics with minimal amount of voltage fluctuations.

3.5 Summary

In this chapter the theoretical formalism for cantilever resonators has been introduced. The main findings are that from a theoretical point of view it is desirable to decrease the dimensions of resonators in order to achieve ultrahigh mass sensitivity. The resonance frequency f_0 is independent of the thickness of the cantilever and could

therefore be made μm thick, which is a necessity for the capacitive readout method chosen in this project.

Physical noise has briefly been discussed, and the ultimate mass sensitivity limit has been deduced based on thermomechanical frequency fluctuations as well as molecular adsorption-desorption generated frequency fluctuations. For a cantilever having similar dimensions as for the one fabricated within the project an ultimate mass sensitivity of $\delta M_{th} \sim 10^{-21}$ kg should be possible at ambient air conditions, at room temperature, and at moderate quality factors. In order to obtain higher mass sensitivity, measurements should be conducted at low temperature, the driving amplitude should be high (close to the linear limit), and f_0 should be high as this also is expected to yield a high quality factor. The quality factor is expected to increase linearly with an increase of resonance frequency. The noise contribution due to adsorption-desorption processes are negligible compared to the contribution from thermomechanical fluctuations.

Chapter 4

CMOS Design

In this chapter the details of electrostatic actuation and readout using CMOS is introduced. The knowledge of parameters such as the displacement current induced by the resonance of a cantilever in close proximity to a fixed parallel plate electrode is vital in order to design the CMOS and the NEMS structure properly. The major work covered within this chapter has been performed by Gabriel Abadal, Jaume Verd, Jordi Teva, Maria Villaroya and Xavier Borrisé at the Dep. of Electronical Engineering at UAB [30][50][51].

4.1 Sensor Principle

The transduction of the cantilever resonator designed within the *Nanomass II* project is achieved by electrostatic actuation and capacitive readout, as schematically illustrated in Fig. 4.1.

An AC voltage V_{AC} is applied to a fixed driver electrode, which is separated by a gap g to the parallel cantilever. This results in an electrostatic force that drives the cantilever oscillation. The capacitive readout approach consists of detecting the capacitance current. The current is induced by the change of the capacitance between the cantilever and the driver electrode as a consequence of the change of their spacing as the cantilever oscillates. In order to be able to detect the capacitance current, an additional DC voltage V_{DC} needs to be applied.

Since the induced capacitance by the cantilever is as small as $C_p \sim 0.1$ fF the parasitic capacitance must be reduced in order not to screen the capacitance induced by the cantilever. As a consequence the use of standard external amplifiers is not feasible. Hence, integrated amplification and signal conditioning electronics must be integrated together with the NEMS system, which is achieved by CMOS integration. The capacitive current induced by the oscillation of the cantilever is converted to a voltage V_g using a capacitor (the build in parasitic capacitance) and the resulting voltage is measured and amplified using a voltage buffer amplifier rendering a voltage output V_{out}. This approach introduces less noise compared to resistive amplification

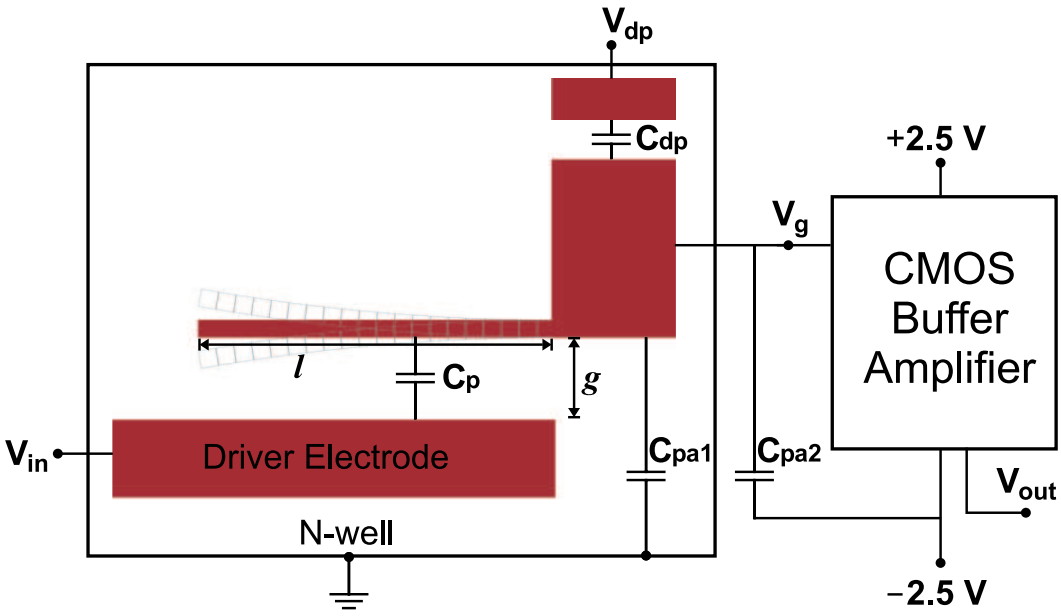

Figure 4.1: *Schematic illustration of the electrostatic actuation of the resonator and the capacitive resonance frequency read-out system.*

since the capacitor does not introduce current noise from the input source.

4.2 Snap-In Voltage

The deflection of a cantilever as a consequence of the influence by electrostatic force can be expressed by a non-linear differential equation according to [52]:

$$El\frac{\delta^4 x(y)}{\delta y^4} - \frac{\epsilon w V^2}{2[g - x(y)]^2} \tag{4.2-1}$$

in which $x(y)$ is the cantilever deflection, ϵ is the permittivity and V is the voltage difference between the cantilever and the driver electrode. There is no analytical solution to this non-linear differential equation. However, an approximate solution can be derived by approximating a linear bending shape of the cantilever under the influence from a uniform electrostatic force along the length of the cantilever. The deflection of the cantilever apex as a function of the voltage can be found by balancing the electrostatic pull-in force and the restoring elastic force according to:

$$\frac{\delta E_e}{\delta x} = \frac{\delta E_{pi}}{\delta x} \tag{4.2-2}$$

in which the elastic deformation energy is given by $E_e = \frac{48}{30}\frac{E}{l^2}x^2$ and the electrostatic pull-in energy is $E_{pi} = \frac{1}{2}C(x)V^2$. The system becomes instable (collapses) if the pull-in force increases faster than the restoring force with increasing x, and instability is reached if:

$$\frac{\delta^2 E_e}{\delta x^2} = \frac{\delta^2 E_{pi}}{\delta x^2} \tag{4.2-3}$$

By using a capacitance $C(x)$ between the cantilever and the driving electrode:

$$C(x) = \frac{\epsilon t l}{x} \ln\left|\frac{g}{g-x}\right| \tag{4.2-4}$$

Eq. 4.2-3. renders the expression for the snap-in voltage V_{si} and snap-in distance x_{si} according to [52][53]:

$$V_{si} = \sqrt{0.28\frac{Eg^3w^3}{\epsilon l^4}} \tag{4.2-5}$$

$$x_{si} = 0.44g \tag{4.2-6}$$

Figure 4.2. shows the calculated snap-in voltage for four sets of cantilever dimensions as a function of cantilever length.

4.3 Small Signal Model

An electrical model of the sensor system is required to achieve the appropriate CMOS circuit design. For this purpose, a simple electromechanical model, developed by G. Abadal *et al.* [30], has been used to model the system in the linear regime. This model makes it possible to derive the electrical requirements for the CMOS circuitry, e.g. displacement current levels at the resonance frequency and V_{AC} and V_{DC} voltages for excitation and readout.

The linear small-signal electromechanical model is based on passive elements and is schematically shown in Fig. 4.3.

The static capacitance C_0 of the cantilever-driver system increases when a V_{DC} is applied and the new capacitance C_p is given by:

$$C_p = (1+\kappa)C_0 = (1+\kappa)\frac{\varepsilon_0 l t}{g} \tag{4.3-1}$$

in which ε_0 is the vacuum dielectric constant. The so-called electromechanical coupling parameter κ is given by:

$$\kappa = \frac{1}{2}\frac{\varepsilon_0 l t}{k g^3}V_{DC}^2 \tag{4.3-2}$$

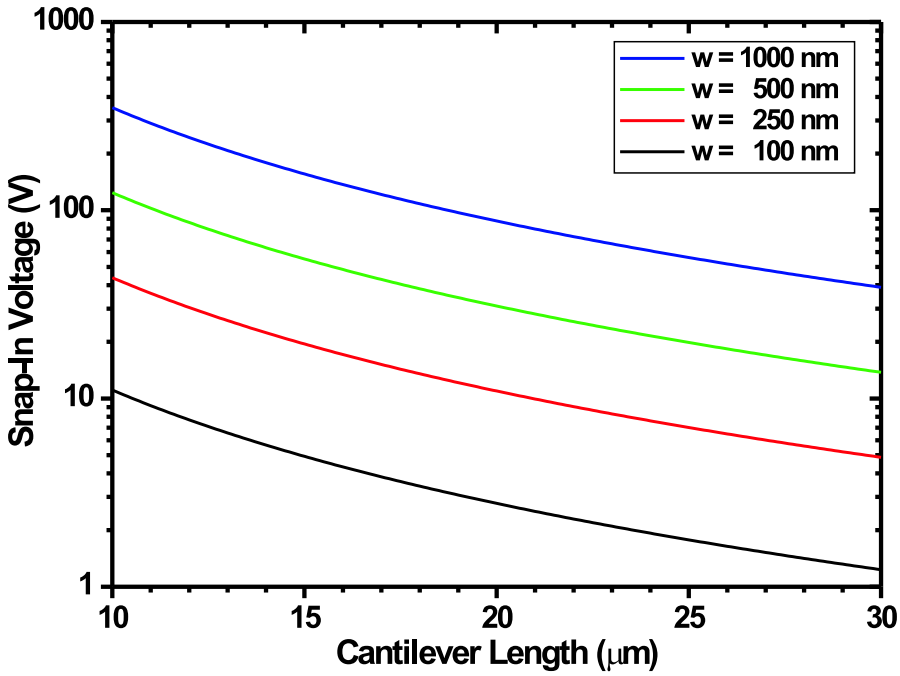

Figure 4.2: *Graph of the calculated snap-in voltage V_{si} for various cantilever widths and lengths. The gap g is 1 μm, the Young's modulus is 180 GPa.*

The R_s L_s C_s series, as in Fig. 4.3., describe the current component induced by the applied V_{DC} according to [30]:

$$C_s = 1.789\kappa C_0 \tag{4.3-3}$$

$$L_s = \frac{1}{2\pi C_s f_0} \tag{4.3-4}$$

$$R_s = \frac{1}{Q}\sqrt{\frac{L_s}{C_s}} \tag{4.3-5}$$

Also an additional parasitic capacitance connected in parallel C_{pa} is also included in the model. The parasitic capacitance is associated with the connection lines between the cantilever and the circuit as well as the input capacitance of the amplifier.

Using these equations the capacitance and the expected current can be estimated for a resonator having the following dimensions: $l = 40$ μm, $t = 1$ μm, $w = 1$ μm, with a gap of $g = 1$ μm. The resulting capacitance is calculated to be $C_p = 0.236$ fF, and the current at the resonance frequency is calculated to be $I_{C\{f_0\}} = 25.7$ nA, when applying a $V_{DC} = 21.3$ V and an $V_{ACpp} = 2.4$ V.

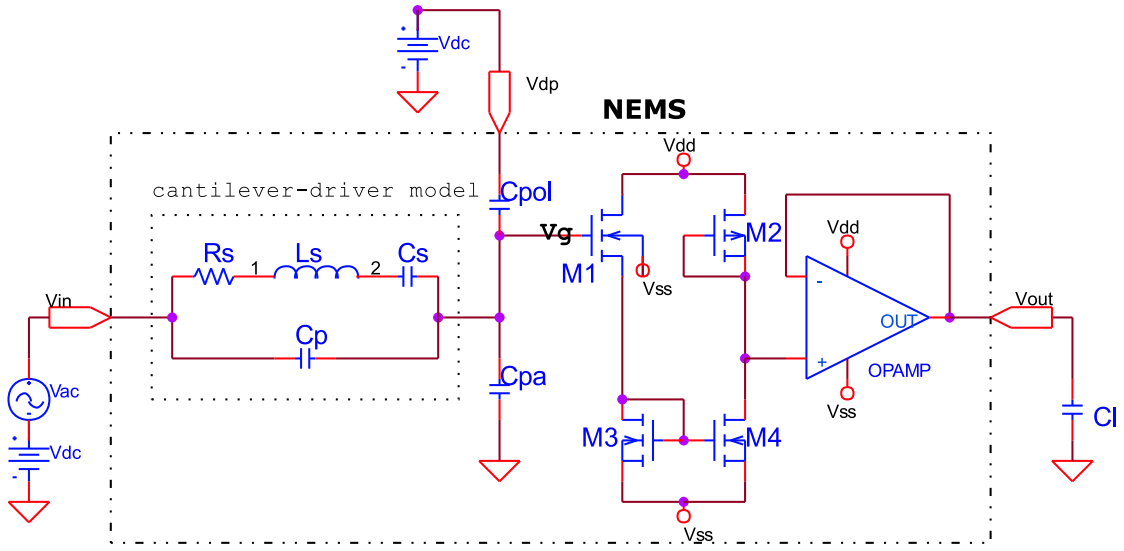

Figure 4.3: *Schematic illustration of the buffer amplifier circuit and passive elements of the small-signal electromechanical model.*

The purpose of the readout circuitry is to detect and amplify the capacitive current I_C generated at the cantilever-driver interface. The capacitive current is given by:

$$\begin{aligned} I_C(t) &= \frac{\delta}{\delta t}(CV) \\ &= (C_p + c)\frac{\delta V_{AC}}{\delta t} + (V_{AC} + V_{DC})\frac{\delta c}{\delta t} \\ &\approx C_p\frac{\delta V_{AC}}{\delta t} + V_{DC}\frac{\delta c}{\delta t} \\ &= I_p + I_d \end{aligned} \tag{4.3-6}$$

in which c is a time variable that reflects the capacitance variations due to the movement of the cantilever, I_p represents the parasitic current since it does not depend on the movement of the cantilever and is generated due to the AC voltage that it is applied for excitation of the cantilever. The displacement current I_d reflects the oscillation of the cantilever since it depends on the variations of the driver-cantilever capacitance.

Assuming that the apex of the cantilever oscillates, due to the electrostatic excitation using an AC voltage with a frequency ω, with a harmonic movement $x(l,t)$ given by:

$$x(l,t) = x(t) = A_{eff}\sin(\omega t) \tag{4.3-7}$$

in which $A_{eff} = 0.39A$ is the effective oscillation amplitude. The analytical expression

for the cantilever-driver capacitance $C(t)$ and its time derivative is derived according to:

$$C(t) = C_p + c = \frac{\varepsilon_0 lt}{[g - x(t)]} \tag{4.3-8}$$

$$\frac{\delta C(t)}{\delta t} = \frac{\delta C(t)}{\delta x}\frac{\delta x}{\delta t} = \frac{\varepsilon_0 lt}{[g - x(t)]^2} A_{eff}\omega \cos(\omega t) \tag{4.3-9}$$

From the last expressions, one can determine the regime for which the displacement current is the dominating term. The amplitude of the displacement current and parasitic current versus the ratio $\frac{V_{DC}}{V_{AC}}$ is showed in Fig. 4.4. An oscillation amplitude of the cantilever tip $A = 675$ nm is assumed and the gap between the cantilever and the driver electrode is approximately 1 μm. From Fig. 4.4. it is seen that as long as snap-in is avoided and linearity is preserved large V_{DC} should be applied.

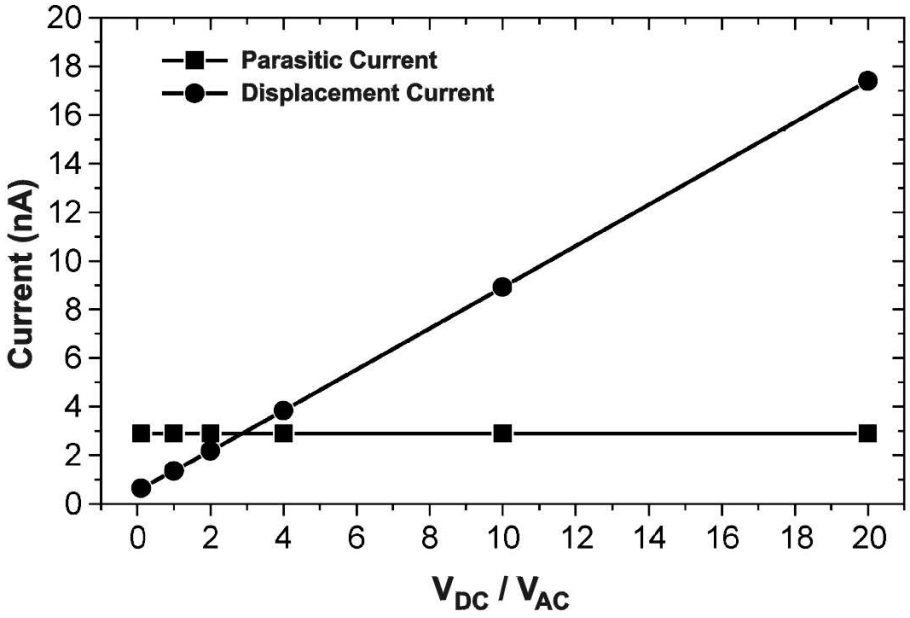

Figure 4.4: *Graph showing the displacement current I_d and the parasitic current I_{pa} as a function of the ratio $\frac{V_{DC}}{V_{AC}}$. As the ratio increases I_d dominates, hence as large DC voltages should be used as long as the system still is in the linear regime and V_{DC} is well below the snap-in threshold.*

An approximate analytical expression for the magnitude of the capacitive voltage V_g is given by:

$$V(C) = V_{in} - V_g = V_{AC} + V_{DC} - V_g = (V_{AC} + V_{DC})\frac{C_{pa}}{C_p + C_{pa}} \Rightarrow$$

$$V_g = \frac{I_C}{\omega C_{pa}} \cong \frac{C_p}{C_p + C_{pa}} V_{AC} + 0.39\frac{C_p}{C_p + C_{pa}}\frac{V_{DC}}{g} A = V_p + V_d \tag{4.3-10}$$

in which ω is the frequency of the AC voltage, V_p is the parasitic voltage term due to the applied AC voltage, V_d is the displacement voltage which is proportional to the DC voltage and the oscillation amplitude. Equation 4.3-10. takes into account that the excitation signal $V_{in} = V_{AC} + V_{DC}$ does not only drop on the cantilever-driver capacitor but also on the parasitic capacitor $C_{pa} = \sum_i C_{pa\{i\}}$, since it is based on a capacitor voltage divider scheme. Furthermore, it is clear that V_g is inversely proportional to C_{pa}. Hence, reducing C_{pa} renders an increased sensitivity.

4.4 Readout Circuitry

The readout circuit, as schematically outlined in Fig. 4.3., is based on a CMOS voltage buffer amplifier biased as a voltage follower. Since V_g is floating (not externally biased) it needs to be polarized in order to reach the optimal range of the amplifier. This was an important finding from *Nanomass I* in which polarization of V_g was not included, which had the consequence that the V_g in most cases was far away from the optimal regime making it impossible to obtain resonance measurement using the capacitive read-out method. The optimal regime for the NMOS circuit is $V_g \sim 0$ V as shown in Fig.4.5.

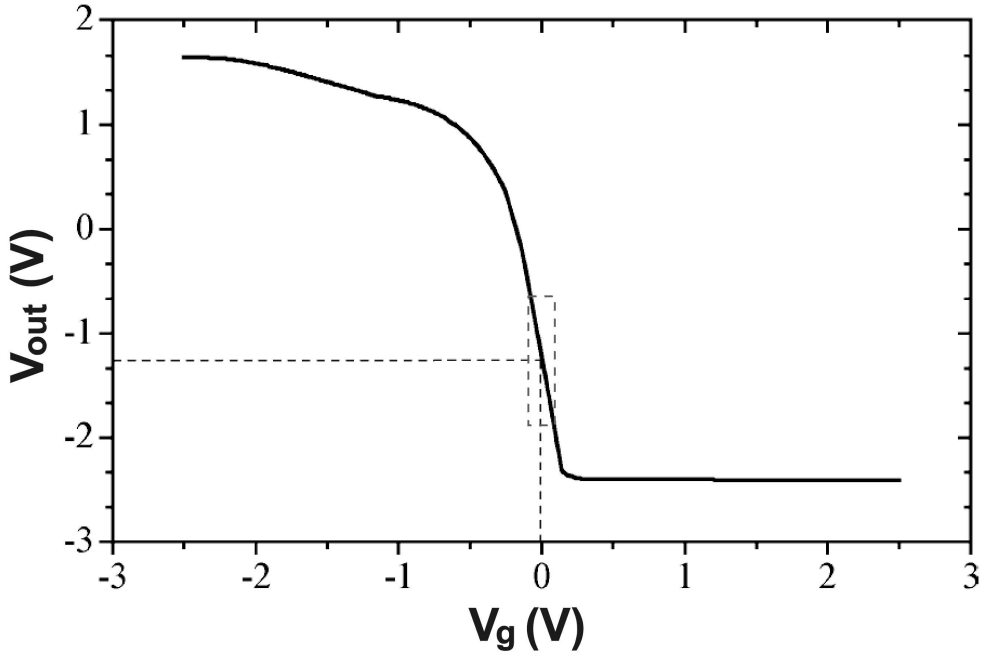

Figure 4.5: *Graph of the optimal operation regime for V_g for NMOS circuits.*

In order to obtain the optimal regime a polarization capacitance in the form of an interdigitated electrode configuration (so called comb-capacitor, as seen in Fig. 4.6.) is fabricated during the cantilever post-process fabrication sequence.

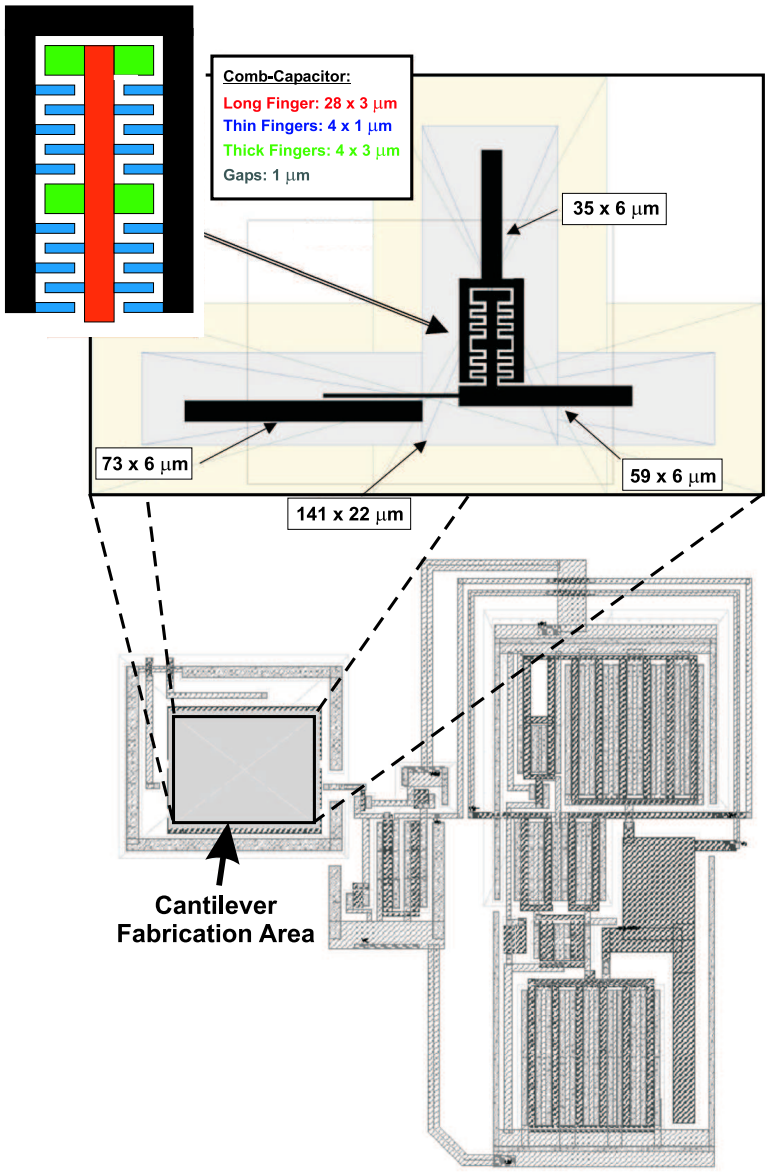

Figure 4.6: *Schematic illustration of the cantilever design and the CMOS circuitry. The comb-capacitor is used to polarize V_g to the optimal range of the amplifier.*

The circuit characteristics is presented in Tab. 4.1.

4.5 Electrical Noise

A simple estimate of the transducer out-put V_{out} close to the resonance peak can be expressed as the ratio between the maximum voltage at the resonance V_{max} and the frequency bandwidth Δf from which the frequency fluctuation δf_{SNR} due to the signal-noise-ratio (SNR) of the read-out circuitry can be derived, according to:

Parameter	Buffer Amp. Run 1995	Buffer Amp. Run 2000
Bandwidth, -3dB (MHz)	1.7	1.9
Gain (V_{DC})	6.2	6.7

Table 4.1: CMOS amplifier specifications for two CMOS runs.

$$\frac{\delta V_{out}}{\delta f} \approx \frac{V_{max}}{\Delta f_{\mathrm{SNR}}} = \frac{QV_{max}}{f_0} \Rightarrow$$
$$\delta f_{\mathrm{SNR}} \approx \frac{f_0 \delta V_{out}}{QV_{max}} \approx \frac{f_0}{Q}\frac{1}{\mathrm{SNR}} \tag{4.5-1}$$

By inserting an estimate of the SNR≈84 dB ($V_{max} \sim 130$ mV, $\delta V_{out} \sim 250$ nV/$\sqrt{\mathrm{Hz}}$ and $\Delta b = 1$ kHz) one gets an estimate of the noise generated by the readout circuit for a cantilever having the dimensions $l = 20$ µm, $t = 600$ nm, $w = 500$ nm, and operating in ambient air $Q_{air} \approx 100$, according to:

$$f_{\mathrm{SNR}} \approx 0.9 \text{ Hz} \tag{4.5-2}$$

This yields a lower mass detection limit of the order of $\delta M_{\mathrm{SNR}} \sim 10 \cdot 10^{-21}$ kg (10 ag), calculated using Eq. 3.1-20.

4.6 Fabrication of Standard CMOS

The standard CMOS that is used for defining the mass sensor system is the CMOS25 technology available at the the CMOS foundry at *Centro Nacional de Microelectronica* (CNM) in Barcelona. The CMOS25 technology is an 8 mask 2.5 µm twin-well 2 poly-1 or 2 metal-CMOS technology. The resonator is defined using the first poly-silicon layer (poly0). Beneath the poly0 is a 1 µm thick thermally grown field SiO_2 which is used as a sacrificial layer in the fabrication of the resonator device. The poly0 layer is used as the bottom plate for analog capacitors in the standard CNM CMOS process, and it is possible to slightly modify the process parameter in fabricating the poly0 layer without changing the transistor characteristics. Therefore the thickness of the structural poly0 layer is increased from 350 nm to 600 nm in order to achieve a larger aspect ratio more suitable for the capacitive detection approach, as well as improving the mechanical properties of the poly0. The deposition temperature is reduced to 580°C instead of the CNM standard 630°C and doped using $POCl_3$ at a temperature of 950°C instead of the CNM standard 900°C.

The resulting poly0 has a sheet resistance of 13.8 Ω/sq and the surface roughness is

7 nm [54]. The poly0 is oxidized during the formation of the gate oxide and then covered by a the second poly-silicon layer (poly1) in order to protect it during the rest of the CMOS processing. Finally, when the whole CMOS has been fabricated a hole is opened in the passivation layer, consisting of 400 nm thick LPCVD oxide and nitride, of the CMOS and reactive ion etching (RIE) is used to remove the poly1 layer exposing the poly0. This final process defines the *nanoarea*, which is the area in which the nanofabrication of the resonator structure is to be conducted.

The CMOS fabrication is achieved in the following steps, as shown in the schematic illustration in Fig. 4.7.

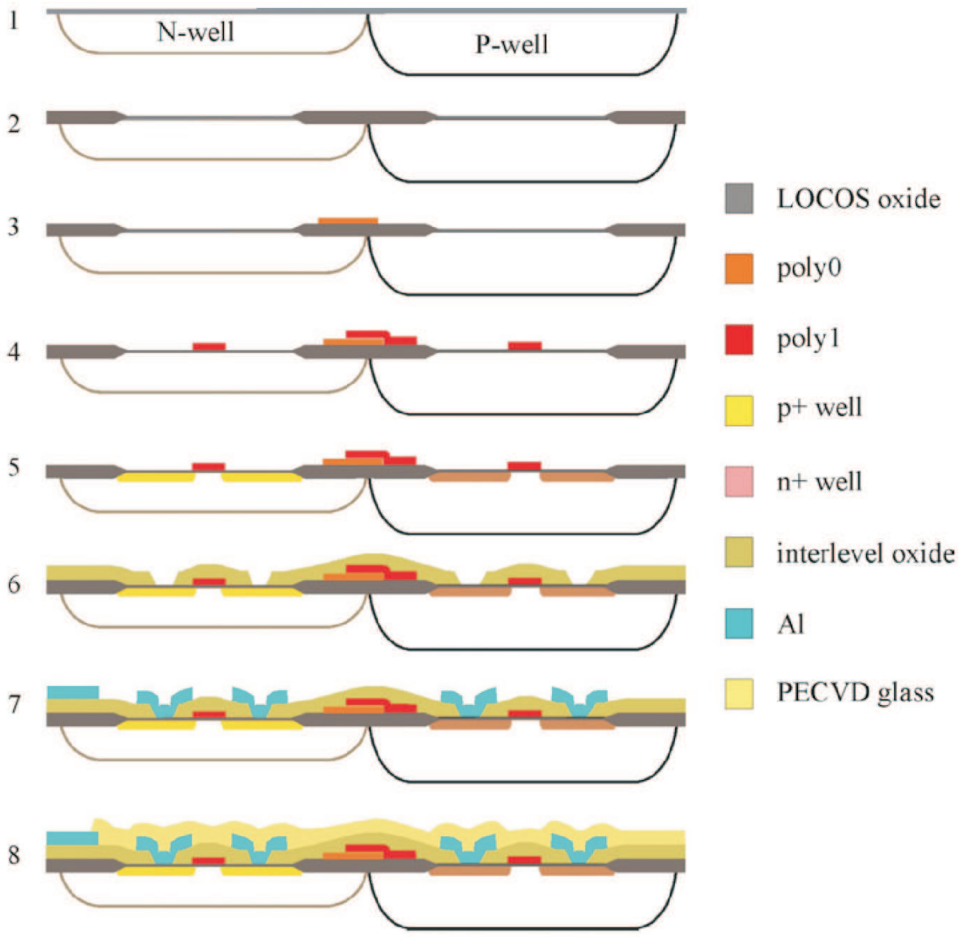

Figure 4.7: *Schematic description of the CNM CMOS25 process sequence. First, the twin wells are defined (1). Then, the thick LOCOS oxide is deposited (2). After that, the first poly0 layer is deposited and defined (3). Then the gate oxide is grown and the top poly1 layer is deposited and defined (4). The source and drain are now defined (5) and the interlevel BPSG oxide is then deposited and defined. Finally, the metal wires and bonding pads are defined (7) and the chips is passivated with a 700 nm thick PECVD glass (8).*

4.7 SOI-CMOS

A SOI-CMOS is fabricated by using bonded and etched-back silicon on insulator (BESOI) wafers with 1.3 µm thick single crystalline Si (s-Si) and 1 µm thick buried SiO_2. SOI-CMOS is desirable in order to further improve the mechanical properties of the resonator. Single crystalline silicon has a higher Young's modulus compared to the poly-Si of the standard CMOS. Furthermore, the s-Si layer is readily twice as thick as the poly0 layer, which further would improve the capacitive detection approach. Another benefit is that the s-Si is not as rough as the poly-Si. A low surface roughness is a necessity if one considers to perform SFM nanolithography, which is virtually impossible to perform on a poly-Si surface having a surface roughness of 7 nm or greater, as will be discussed in Chapter 5.3.

Chapter 5

Lithography

Lithography is a fundamental tool by which modern way of life has evolved over the past decades based on the increasing amount of advanced consumer electronics. In the context of physics lithography stands for surface patterning and surface structuring. The development of micrometer resolution photo lithography achieving high throughput and high yield has been an important part of the development of the Si-semiconductor integrated circuitry (IC) business, pre-dominantly in the branch of microprocessors.

In order to fabricate Si resonators in the CMOS a metal/metaloxide-mask needs to be defined using lithography in the so called nanoarea of the pre-processed CMOS. The metal/metaloxide mask is then used as an etch mask for anisotropic reactive ion etching (RIE) of the underlying Si layer of the CMOS which transfers the metal mask pattern to the structural poly-Si layer.

In the following chapter conventional photo lithography as well as advanced nanolithography techniques which have been used for the cantilever fabrication onto preprocessed CMOS are presented. The process steps in defining the RIE etch mask using direct write laser lithography (DWL), electron beam lithography (EBL), scanning force microscopy (SFM) based nanolithography, and combination of these techniques are presented.

5.1 Photo Lithography

Photo lithography stands for a group of lithography techniques that use light, visible or ultra violet (UV), to expose a light sensitive polymer film (resist) in order to create a pattern. The main photo lithography techniques are contact-, proximity-, and projection lithography, enabling sub-micrometer resolution. They are parallel techniques and enable high throughput on a wafer scale. As illustrated in Fig. 5.1.
the main difference between the photo lithography techniques is that contact- and proximity lithography are 1:1 exposure techniques whereas projection lithography usually gives 4 or 5 times feature size reduction and hence needs to be "stepped"

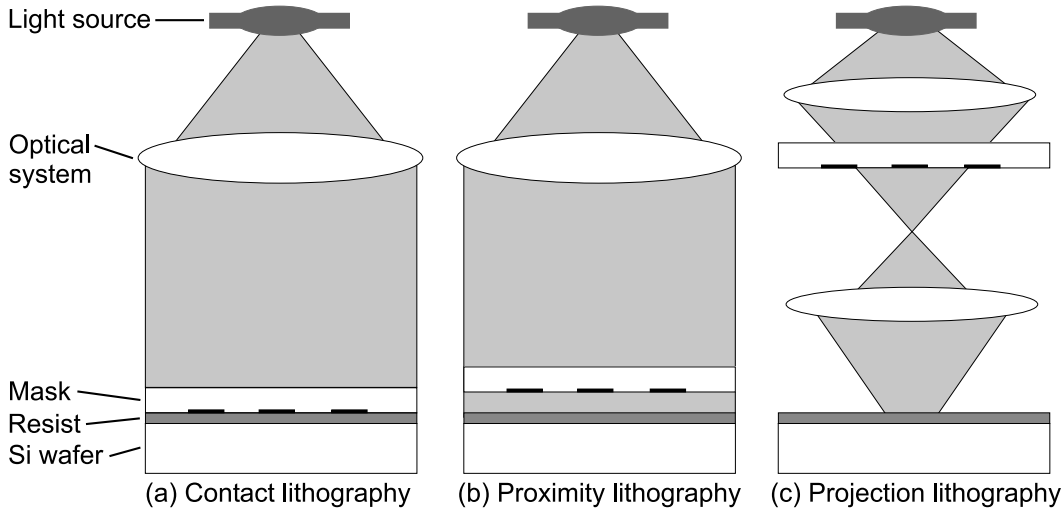

Figure 5.1: *Schematic illustration of contact-, proximity-, and projection lithography*

several times to cover the whole wafer. Projection lithography is the main lithography techniques used in Si-IC fabrication since the technique is more reliable as opposed to contact lithography. This is due to that the mask is not in contact with the wafer and hence it is not as sensitive to topographical variations in the resist or in the wafer, and consequently the mask does not have to be cleaned after each lithography process, opposed to contact mask lithography.

In order to differentiate areas that should and should not be exposed to light a mask having the desired pattern must be made. The mask typically consists of a glass wafer, which is transparent to UV-light, and which has a non-transparent pattern, typically consisting of a 0.5 μm thick Cr layer. Before light exposure the sample wafer is coated with the appropriate photo sensitive polymer (resist) by dispensing the resist on the wafer followed by spinning the wafer in order to achieve a homogenous resist thickness. By controlling the spin rotation speed and time the resist thickness can be controlled with a precision of some tenths of nanometers. The process parameters consists of the resist composition, resist film thickness and pre/post-bake time.

Contact lithography is achieved by clamping the predefined mask and the resist coated wafer in semi-contact with each other. In proximity lithography the mask and the wafer are separated by a distance g so that no part of the mask/wafer are in contact. Thereafter the UV-light is radiated on the backside of the mask, as illustrated in Fig. 5.1.(a) and (b). In projection lithography the mask and wafer are not in contact and opposed to proximity lithography the projection of the mask is focused down on the wafer using extra optics, as illustrated in Fig. 5.1.(c).

The light that reaches the resist results in a chemical change in the material. The chemical modification of the exposed resist areas results in a change of molecular weight compared to the non-exposed areas. Hence, a liquid chemical solvent is used

to rinse away the resist areas having the lowest molecular weight, which are the most soluble.
The resolution limit for contact- (r_c), proximity- (r_p), and projection lithography (r_s) are given by the Rayleigh criteria of diffraction [55]:

$$r_c = \sqrt{\alpha_c \lambda \cdot (g_c + \frac{1}{2})d} \quad (5.1\text{-}1)$$

$$r_p = \sqrt{\alpha_p \lambda \cdot g_p} \quad (5.1\text{-}2)$$

$$r_s = \alpha_s \frac{\lambda}{\mathrm{NA}} \quad (5.1\text{-}3)$$

where α is an empirical constants assigned to each individual lithography system, λ is the wavelength of the incident light, g is the separation between the mask and the resist surface, d is the thickness of the resist and NA is the numerical aperture of the optical system.

In order to achieve the highest possible resolution the wave length of the light should be short, the gap between the mask and the wafer should be small and the resist film should be thin. For projection lithography the numerical aperture should be high.

An estimate of the resolution for the described techniques can be made by assuming a KrF excimer laser light source with a wavelength $\lambda = 248$ nm and typical values for α ($\alpha_c \sim 1.6$, $\alpha_p \sim 1.6$, $\alpha_s \sim 0.75$) and g ($g_c \sim 2$ µm, $g_p \sim 25$ µm) and $d \sim 2$ µm and NA ~ 0.6 which gives:

$$\begin{aligned} r_c &\sim 630 \text{ nm} \\ r_p &\sim 890 \text{ nm} \\ r_s &\sim 310 \text{ nm} \end{aligned}$$

By pushing the technology using short wavelength light sources, such as ArF excimer lasers ($\lambda = 193$ nm), innovative resist materials, and advanced optics, IC circuits with features below 100 nm can readily be achieved [56].

5.2 Laser Lithography

Direct write laser lithography (DWL) represents various maskless lithography techniques based on serial laser beam-induced surface modification. Laser micromachining of Si by deposition and doping or etching have been thoroughly investigated for over 20 years [57][58][59]. Over the years several different types of novel DWL techniques have emerged that enable surface patterning with sub-micrometer resolution, e.g. etching of Si [60][61], thermal oxidation of thin Al- and Si-films [62][63][64], chemical vapor deposition of Si, Au, Co or Al_2O_3 [57][65][66][67] and ablation of

polymers [68][69][70][71][72]. Applications of DWL techniques can be found within rapid prototyping of MEMS devices as well as within photo lithography and x-ray lithography-mask fabrication [73].

The DWL techniques developed during the *Nanomass II* project enable sub-micrometer linewidth lithography over cm^2 areas. Most importantly, the techniques are compatible with post-processing on CMOS. The techniques enable very high flexibility in terms of pattern definition since new patterns can be implemented immediately without the need of a pre-designed mask, as opposed to photo lithography. The laser spot power can been varied between 10 mW to 300 mW and the dwell time can be varied from 0.5 ms to 50 ms, which enables fast prototyping of MEMS devices.

5.2.1 Instrumentation

The direct write laser lithography set-up at MIC consists of a continuous-wave argon ion laser, beam-conditioning optics and a motorized sample stage, as displayed in Fig. 5.2. The argon ion laser is tuned at λ= 488 nm and has a maximum operational power of 5W.

Using the beam conditioning optics the laser beam can be focused onto the sample to a nominal spot size of approximately 600 nm. The beam is fixed and patterns are generated by the motion of the motorized sample stage, which is controlled by a computer connected to the control unit of the stage. The x-y sample stage is set so that the minimum distance between consecutive lines/spots is 500 nm. Alignment of the laser beam onto the sample is achieved by using a CCD camera. This gives an alignment precision of a few µm. Patterns are generated as the laser beam is turned on and off synchronized with the motion of the stage.

5.2.2 Laser Induced Thermal Oxidation of Al

Direct write laser lithography based on thermal oxidation (DWL-TO) of thin Al films has been used for rapid prototyping of MEMS devices on Si and SiO_2 substrates [62][64][74].

First, a thin insulating oxide layer is grown on the Si-sample in order to achieve thermal insulation, after which a 6-10 nm thin Al film is deposited. As the laser beam irradiates the Al film with a sufficient laser power the Al is thermally oxidized and an Al_2O_3/SiO_2 alloy is believed to be formed [62]. A pattern can be formed by utilizing the difference in etch rates between the native Al film and the thermally oxidized Al as the sample is placed in phosphoric acid (H_3PO_4). After etching of the non-oxidized Al the remaining Al_2O_3/SiO_2 alloy can be used as an etch mask for further surface micromachining steps.

A mayor benefit of laser lithography techniques is that one can utilize the gaussian

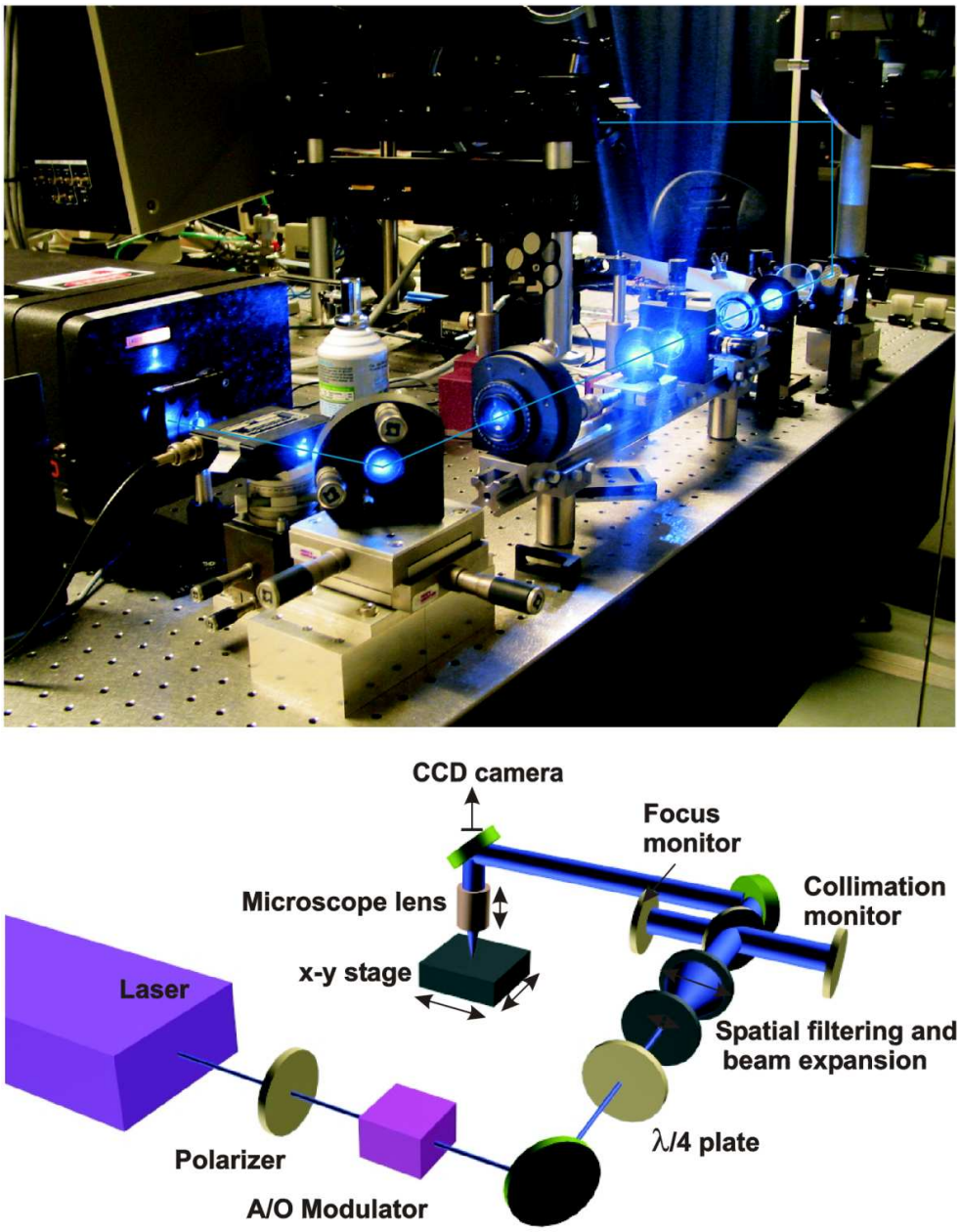

Figure 5.2: *(top) Photograph of the main optics section of the DWL system. (bottom) Schematic representation of the DWL system. The DWL set-up consists of a argon ion laser (continuous-wave, λ=488 nm), an acousto-optic modulator for beam switching, beam-conditioning optics including a λ/4-plate and a microscope objective attached to a z-axis-stage enabling controlled laser beam focusing. The sample is placed on a computer controlled x-y-axis-stage.*

intensity distribution of the beam in order to allow patterning below the conventional optical resolution limit.

Process Flow

Thermal oxidization of thin Al films is a CMOS compatible lithography technique which has been used for defining resonators on standard CMOS. The process steps involved in making Al_2O_3 mask are schematically displayed in Fig. 5.3.

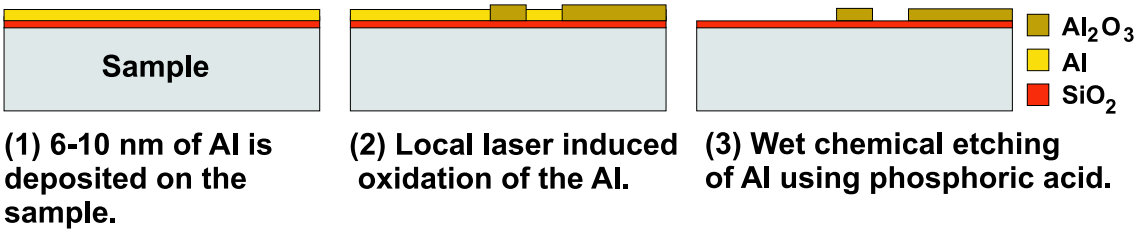

Figure 5.3: *Schematic illustration of the process flow of Direct Write Laser lithography based on oxidation of thin Al films.*

An Al film is deposited on the pre-processed CMOS chip using thermal evaporation, Fig. 5.3(a), at a rate of 5 Å/s. The grain size is typically 3-5 nm, which is of the same order of magnitude as the surface roughness of the poly0 of the CMOS. The CMOS chip is ideally immediately used for lithography since the build up of the native Al oxide will reduce the difference in etch rates when exposed to H_3PO_4. Alternatively, if lithography is not possible the CMOS chip is stored in a N_2-box, effectively reducing the native oxide formation.

The laser lithography process is as follows: After thermal deposition of Al on several CMOS chips, Fig. 5.3(b), one of them is used as a test chip on which a laser power test is performed in order to determine which is the optimal laser power for the specific Al film thickness and quality. The CMOS chip is mounted on the sample stage by simply placing a small water droplet on the stage after which the CMOS chip is placed on top of the drop. The surface tension keeps the chip fixed onto the stage, and it takes a quite large force in order to overcome the pull-down force when removing the chip. Before the lithography step the laser system has been warmed up for a half an hour in order to reduce laser power fluctuations. The performance of the laser system is verified by monitoring the out-put power as a function of the applied current that is applied to the laser. The power table is made in order to deduce the equivalent amount of power corresponding to the applied current. The nanoareas of the test chip are irradiated using a wide range of laser power ranging from 10 mW to 100 mW in steps of 10 mW, Fig. 5.3(c). The power and writing speed is set in the LabView® software, which controls the laser input current, the motion of the sample stage, and the switching of the A/O-modulator. After the laser induced oxidization the non-oxidized Al is wet etched using H_3PO_4, Fig. 5.3(d).

For the end result the wet etching time is crucial, but the time is also difficult to absolutely determine. If the etching time is too short there will remain Al in the nanoarea which will acts as an etch mask for the anisotropic RIE. This means that

there will be no pattern transfer to the poly0. If the chip is etched for too long time the Al_2O_3 will also be etched which results in an inadequate RIE etch mask. The etching time depends strongly on the amount of native Al oxide which has been formed since the time of Al deposition. Generally, the etching time for 6-10 nm of Al that has been deposited within 12 h is approximately 1 minute and 30s. After wet etching the test CMOS chip is inspected optically and the optimal laser power is determined and used on the rest of the CMOS chips which were deposited with Al in the same batch. This procedure is repeated for all batches of chips since even a small variation of Al film thickness and quality results in a different optimal laser power needed to ensure reproducible lithography with linewidths below 700 nm.

Results

Examples of cantilever etch masks as defined by laser induced local oxidization are shown in Fig. 5.4.

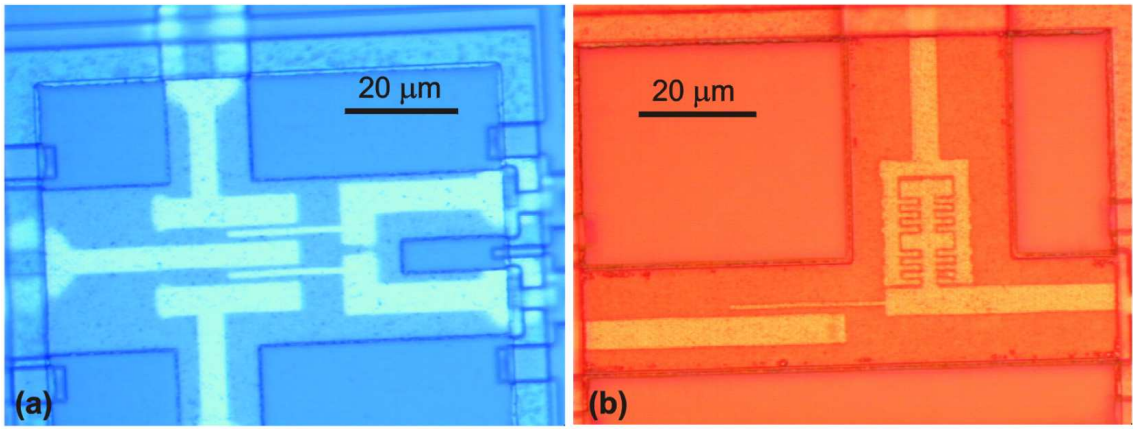

Figure 5.4: *Optical image of Al_2O_3 cantilever mask patters defined on CMOS by lased induced local oxidation followed by wet etching of the non-oxidized Al. (a) 2-cantilever array and (b) single cantilever with comb-capacitor.*

The power was 52 mW and the writing speed was 0.1 mm/s. Below this power there was no oxide which withstood the wet etching step. Above this power the minimum linewidth rapidly increased. Only by increasing the power by 10 mW renders a linewidth increase by as much as 40%. The most important parameter is the thickness of the Al film. If the the Al film is too thin the grain size of the deposited Al becomes an issue due to the possibilities of pin-holes in the metal mask which can limit further processing. On the other hand if the metal film is too thick the minimum resolution will be reduced since a higher power will be needed in order to fully oxidize through the Al film thickness.

Examples of fully processed cantilevers defined by laser induced local oxidization are shown in Fig. 5.5.

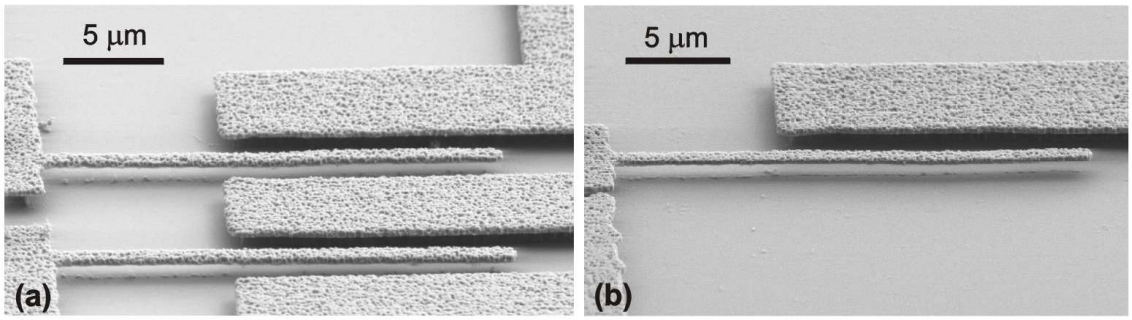

Figure 5.5: *SEM images of fully processed cantilevers defined by DWL-TO on CMOS. (a) 2-cantilever array system and (b) a single cantilever system with comb-capacitor. The length of the cantilevers are 25 µm and the width is 880 nm. The surface roughness is quite large due to that the Al_2O_3 mask is of the same thickness as the surface roughness of the poly0 layer, resulting in insufficient RIE masking.*

As seen from these images the silicon surface is quite rough. This is due to the combination of having an Al film thickness which is of the same order of magnitude as the inert surface roughness of the underlying poly0 (8 nm and 7 nm respectively). This inevitably results in pin-holes in the metal mask which reduces the capability to withstand the RIE process. This highlights the mayor limitation of the technique. Thin metal masking may result in large amounts of pin-holes in the structural layer, if the surface roughness of the structural layer is of the same order of magnitude or larger compared to the Al-film thickness. The later case drastically reduces the yield of operational devices.

5.2.3 Laser Lithography by Ablation of Polymers

As a consequence of reduced yield when using laser induced local oxidation on the poly0 of the standard CMOS another direct write laser lithography technique has been developed. The technique is based on laser induced thermal ablation of polymers (DWL-TA) followed by a lift-off process. The important benefit of the ablation technique compared to the oxidization technique is that by using combining ablation of a polymer a lift-off process can be used which enables fabrication of thicker metal masks drastically reducing the amount of pin-holes.

The principle of operation is simple: By coating a sample with a thin resist film a pattern can be defined by locally irradiating the resist using the laser. The irradiation causes intense heat and the polymer is ablated. A cross-sectional SEM image, Fig. 5.6 shows a laser exposed resist bi-layer consisting of PMMA (poly[methyl methacrylate]) on top of a layer of LOR (poly[methyl glutarimide]). The ablation of the resist bi-layer results in a gaussian like profile of the resist, which is due to the gaussian intensity distribution of the cross section of the laser beam.

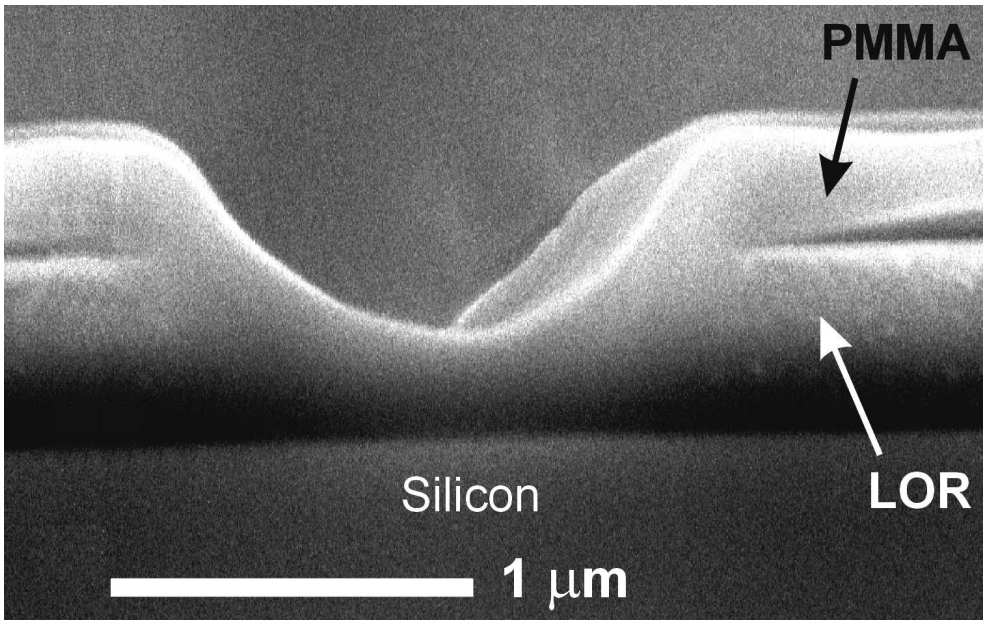

Figure 5.6: *SEM image of a cross-section of a PMMA/LOR bilayer on Si after laser ablation. The resist bilayer consist of 300 nm PMMA and 700 nm LOR.*

Process Flow

The process flow is schematically illustrated in Fig. 5.7.

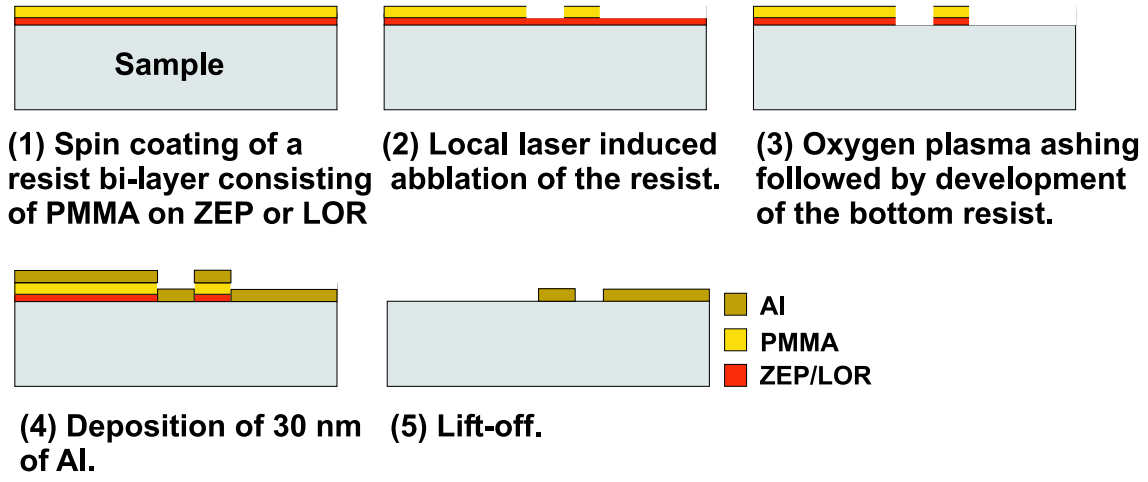

Figure 5.7: *Schematic illustration of the process flow of Direct Write Laser lithography based on ablation of thin polymer films.*

The CMOS chips are spin-coated with an approximately 200 nm thick resist (as measured by ellipsometry on plain Si samples) Fig. 5.7(a). Three different resist compositions have been used:

- AZ5214E
- PMMA950(1:1)/LOR
- PMMA950(1:1)/ZEP520A7

The resist bi-layers were investigated in an effort to evaluate the possibility to combine laser lithography with electron beam lithography (EBL) and nanoimprint lithography (NIL) for which these resist bi-layer compositions often are preferred. As a consequence of spin-coating 200 nm thin resist on CMOS chips, they will have slightly different resist thicknesses due to the limited step-coverage of thin resist on a highly topographical CMOS surface. The nanoarea lies 1.7 µm lower than the surface of the CMOS. Hence, the laser power test needs to be performed individually on each CMOS chip.

The resist parameters are given by:

- AZ5214E: The CMOS chip is spin-coated with AZ5214E and hard baked on a hot-plate at 120°C for 2 minutes. An resist thickness of 200 nm is used for the patterning.
- PMMA/LOR: The CMOS chip is spin-coated with LOR and hard baked on a hot-plate at 220°C for 20 minutes. Next, the CMOS chips are spin-coated with PMMA and baked at 180°C for 10 minutes. An bi-layer thickness composition of 120:80 nm is used for the patterning.
- PMMA/ZEP: The CMOS chip is spin-coated with ZEP and baked on a hot-plate at 180°C for 15 minutes. Next, the CMOS chips are spin-coated with PMMA and baked at 180°C for 10 minutes. An bi-layer thickness composition of 70:130 nm is used for the patterning.

The resist coated CMOS chip is placed on the sample stage, as described previously. For each chip a set of power tests are performed. A merit of using ablation is that it is possible to monitor the result immediately. Hence, a very few sets of laser powers generally need to be evaluated before the optimal regime is deduced. A typical laser power in the range of 30-80 mW at a writing speed of 0.01 mm/s has been used for the patterning on CMOS. After the laser ablation, Fig. 5.7(b), the sample is treated with oxygen plasma (99 sccm O_2 : 20 sccm N_2, 30 W, 80 mTorr for 20 s) using a reactive ion etcher, in order to remove possible PMMA residues within the patterned structure, which would hinder the development of the bottom resist layer, Fig. 5.7(c).

In order to fully transfer the laser written pattern to the structural Si layer the bottom resist layer is dissolved with dedicated solvents, Fig. 5.7(d). The LOR is dissolved in diluted MF 319 developer. MF 319 is mixed with deionized water to a 1:40 solution in order to give a desired dissolution rate of the order of tenths of nm per minute. The ZEP is dissolved in O-xylene for 5 minutes. A slow dissolution process enhances

control of the necessary undercut profile and prevents over development, in which case the PMMA layer might collapse or break apart. The LOR and the ZEP are dissolved isotropically, hence creating a lower boundary on the minimum distance between lines. This is an inherent property of the wet-etch process and a distance of at least 1.5 times the vertical resist thickness is needed between structures. This limits the minimum line separation to 300 nm, for the resist compositions which have been used for cantilever fabrication.

Metal deposition is carried out by thermal evaporation of Al or Cr, Fig. 5.7(e). The lift-off process is carried out in two steps. First, a warm acetone bath is used to expand and dissolve the PMMA, Fig. 5.7(f). This will create cracks in the metal layer on top of the PMMA and start an initial lift-off. The LOR and ZEP are unaffected by the acetone and will thus prevent metal flakes from adhering to the silicon substrate. Subsequently, warm Remover PG (*MicroChem*) dissolves the LOR or ZEP layer and remove the remaining metal, Fig. 5.7(g).

Results

The developed direct write laser lithography technique has enabled the realization of etch masks in 30-40 nm thick Al and Cr with minimum line widths of 500 nm, using a power of 80 mW and a writing speed of 0.01 mm/s, as shown in Fig. 5.8.

Due to varied topography of the CMOS, and most importantly since the nanoarea lies 1.7 μm within the CMOS surface, there is inevitably mayor resist thickness variations within the nanoarea. Hence, it has been a mayor challenge to reproduce linewidths below 600 nm on CMOS chips. An Example of a fully processed cantilever defined by laser induced local oxidization is shown in Fig. 5.9.

As expected there are no pin-holes in the resonator structure due to the increased etch mask thickness. However, the yield is low due to the slow writing speed needed and the fact the every CMOS chip needs thorough laser power testing. These issues together with the difficulties achieving linewidths below 600 nm does not make DWL-LA the preferred lithography technique for the development of nanoresonators within the *Nanomass II* project. However, as will be presented in the next section the technique has successfully been used as a flexible complement to both EBL and SFM based nanolithography for seamless etch mask definition and NEMS prototyping.

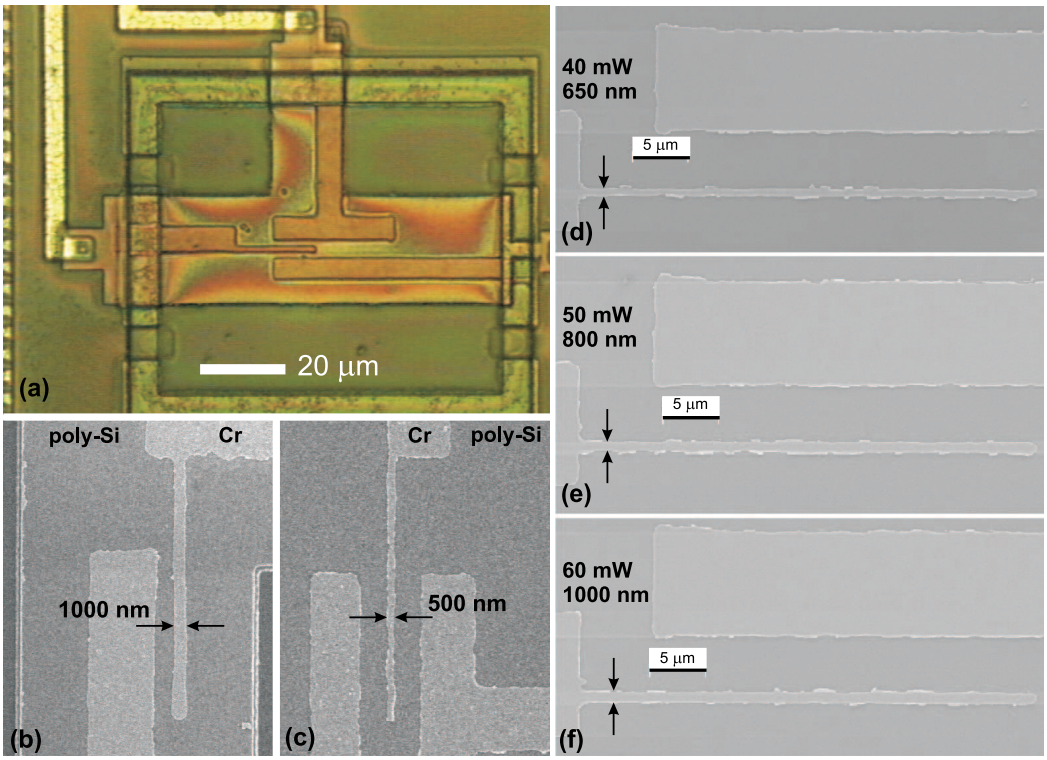

Figure 5.8: *Images of Al cantilever mask patters defined by DWL-TA on CMOS. (a) Optical image after laser ablation in PMMA/ZEP. (b)-(c) Cr pattern defined on standard CMOS using laser ablation. (d)-(f) The linewidth can be controlled by controlling the laser power at a constant writing speed of 0.5 mm/s. A power increase of 10 mW results in a linewidth increase by approximately 200 nm.*

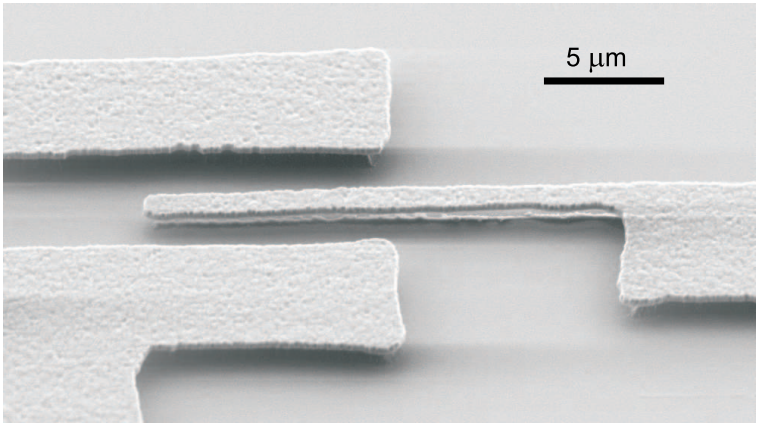

Figure 5.9: *SEM image of a fully processed poly-Si cantilever defined by DWL-TO on CMOS. The cantilever width is 900 nm, the length is 20 µm, and the thickness of the poly0 is approximately 400 nm, which is below the desired thickness.*

5.3 Scanning Probe Lithography

Lithography techniques based on local surface modification using a micrometer sized cantilever having a sharp tip at the apex have emerged since the development of scanning probe microscopy (SPM) techniques. The development of SPM was initiated by the innovation of scanning tunnelling microscopy (STM) by G. Binning *et al.* in 1982 [2]. STM has been a mayor breakthrough in surface science and enables surface metrology on conductive surfaces with atomic resolution. Scanning force microscopy (SFM) was developed shortly afterwards enabling surface metrology also on non-conductive surfaces. The first article discussing SFM was published by G. Binning *et al.* in 1986 [3], which also was the same year as G. Binning and H. Rohrer received the nobel prize in physics for their previous work on STM.

Over the last 15 years several SPM based lithography techniques have emerged. These lithography techniques are based on physical surface modification by mechanical scratching [75], electron exposure of a resist [76][77], electrochemical oxidation of Al, Ti or Si [78][77][79][80] and deposition of organic or inorganic compounds [81][82][83].

Scanning probe lithography by means of local anodization of thin Al films has been investigated for NEMS prototyping within this project. The technique is a slight modification of conventional non-contact mode SFM, and is illustrated in Fig. 5.10.

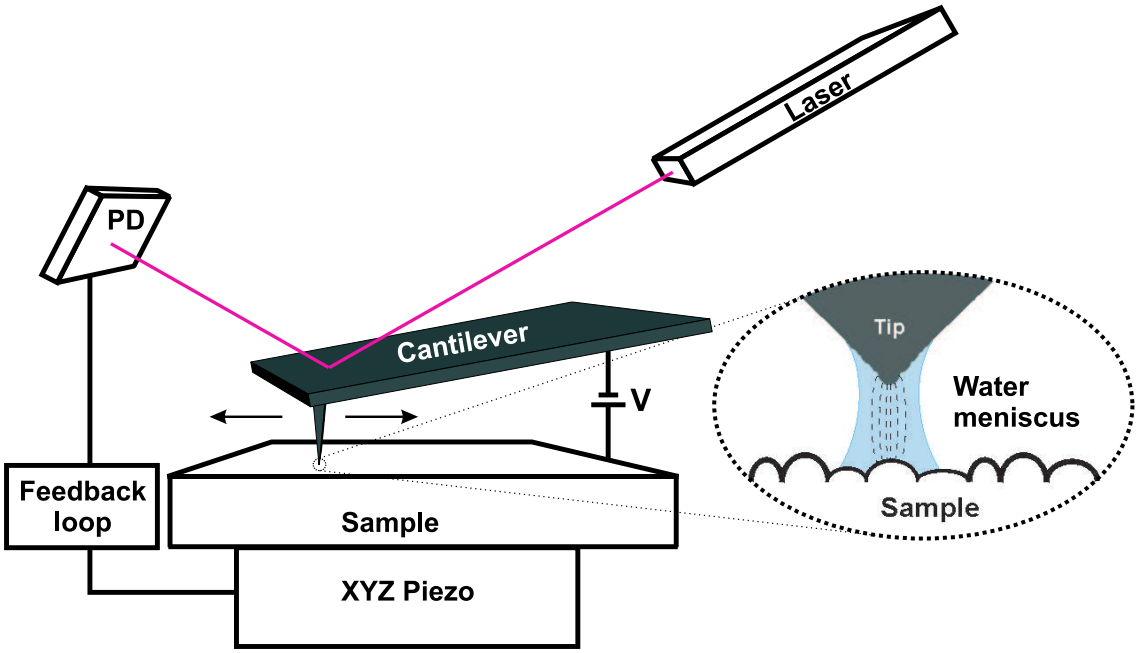

Figure 5.10: *Schematic illustration of SFM nanolithography based on local oxidation. A negative potential is applied between the conductive tip resulting in local oxidization of the sample surface.*

In order to enable lithography the cantilever needs to be conductive. As a voltage is applied between the tip and the sample the sample surface is oxidized if a voltage is applied which is greater than the threshold voltage V_{th} of oxidization. The oxidization is achieved in the presence of water on the sample which supplies to necessary oxidization reagents as the water is hydrolyzed by the applied bias. The OH^--groups in the hydrolyzed meniscus are accelerated by the potential difference between the tip and the sample into the thin Al-film which is locally oxidized. The oxide growth is determined by the diffusion time and the magnitude of the applied voltage. The oxidization process is ultimately self-limited, as the oxide thickness increases the diffusion barrier increases eventually stoping the oxidization.

The threshold voltage is needed in order to create the necessary water meniscus between the tip and the surface at a finite separation. As shown by Schenk *et al.* in Fig. 5.11. [84] a water meniscus is formed as a sharp tip is brought into contact with a surface having a thin water film.

Furthermore, the width of the water meniscus can be controlled by adjusting the tip-sample distance. This means that the lithography line width can be adjusted by controlling the tip-sample separation which changes the meniscus width and hence the oxidization cross section area. The formation of the water meniscus can be monitored by analyzing the cantilever oscillation amplitude after applying a voltage pulse $V \geq V_{th}$ to the cantilever synchronized with turning off the feed-back loop. After meniscus formation the oscillation amplitude is reduced compared to when the feed-back loop was turned on. This is due to the pull-down force exerted by the water meniscus on the cantilever. Lithography with minimum linewidths down to a few nanometers has been reported [85]. Another benefit of using non-contact SFM lithography is lack of tip-wear compared to contact SFM lithography which drastically would reduce the resolution and the reproducibility.

5.3.1 Process

I performed the SFM nanolithogarphy under the guidance of F. Pérez-Murano at CNM. The lithography system is an Digital Instruments Dimensions 3100. The sample is coated with a 6-10 nm thin Al film which is to be oxidized. The plane of the surface chosen for lithography is recorded using the SFM. The recorded plane is used to achieve a controlled tip-sample separation as the feed-back loop is turned off during lithography. A voltage equals to or greater than the threshold voltage is applied to create the water meniscus necessary in order to oxidize the Al.

The lithography parameters are the humidity, oxidization voltage, and the writing speed. Typically one needs to test the parameter space for each sample due to possible variations in the amount of native Al oxide of the Al, humidity variations, and the condition of the tip. Typical lithography parameters at ambient air conditions are voltages in the range from 20-35 V and writing speeds in the range of 1-5 μm/s. The great benefit of SFM nanolithography is that the lithography result can be mon-

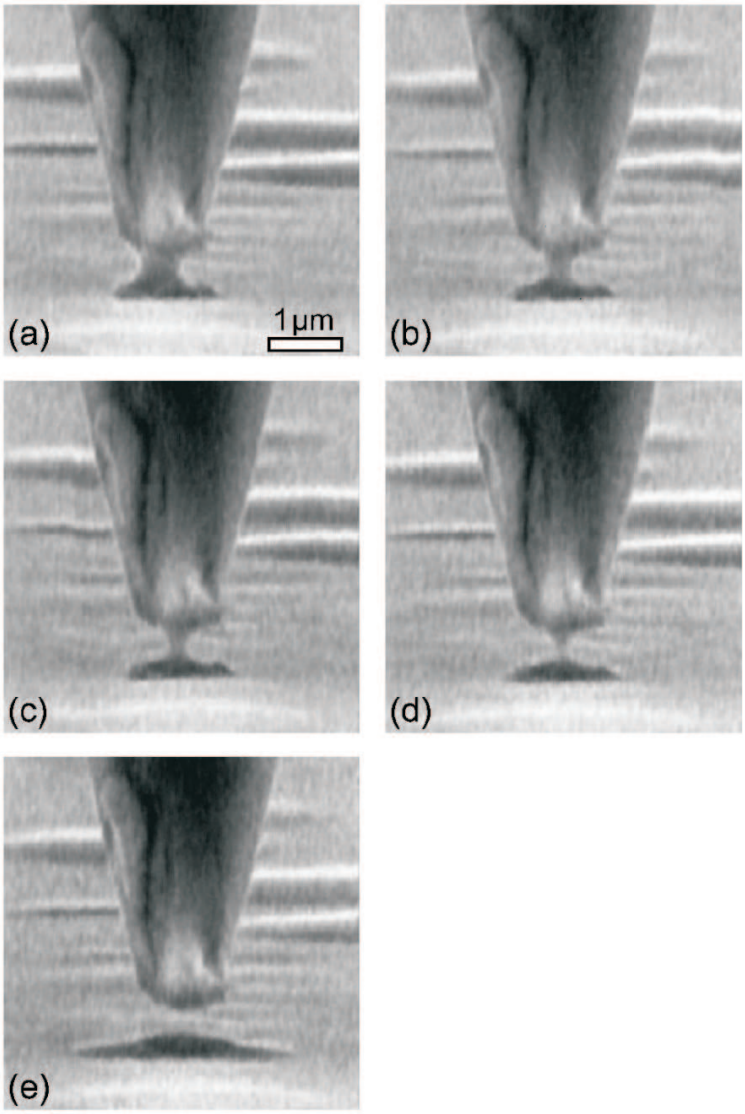

Figure 5.11: *Time-resolved sequence of SEM images recorded with an ESEM-E3. The water meniscus between the tungsten tip and the Pt/C-coated mica is clearly visible (a)-(d). Due to locally decreasing relative humidity the meniscus becomes gradually smaller until it snaps off. The sequence was recorded at a pressure of 1.2 kPa within 11 s and each image was acquired within about 2 s.[84]*

itored instantly after the oxidization process using the SFM nanolithography system. Hence, one gets direct feed-back on wether one have been using the optimal process parameters.

The rest of the processing is identical as for direct write laser lithography based on oxidization of Al. The SFM defined pattern is revealed by selective wet etching using H_3PO_4.

Results

As mentioned the minimum linewidth can be controlled by increasing or decreasing the tip-sample separation. Figure 5.12 illustrates this phenomena. As the tip-sample separation is increased the linewidth also decreases as a consequence of the reduced channel width for the oxidizing OH^--groups. An oxide linewidth of approximately 20 nm is achieved using a voltage of 25V and a writing speed of 1 µm/s.

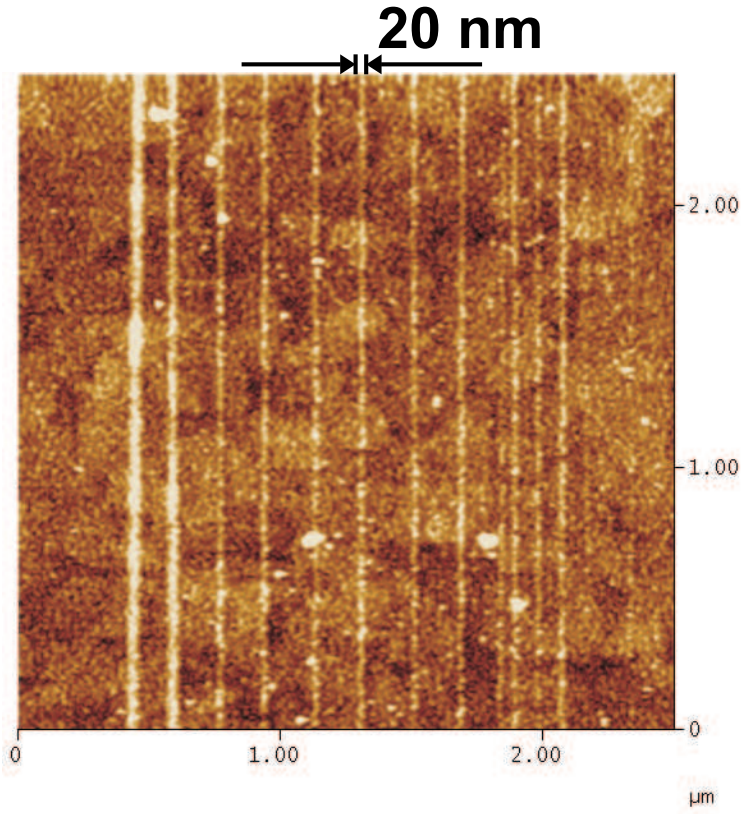

Figure 5.12: *SFM image taken directly after SFM nanolithography of an 6 nm thick Al film on a SOI-substrate. The minimum linewidth is approximately 20 nm.*

Examples of oxide patterns defined on 6 nm Al on SOI are shown in Fig. 5.13. Fig. 5.13(c)-(d) illustrates the reason why it is possible to monitor the oxidization result after lithography. The reason it the volume expansion as the Al is oxidized forming Al_2O_3. After oxidization a 6 nm high step has been formed due to this volume expansion, which is well enough to be detected by SFM. The linewidth of the cantilever structure was measured to 150 nm as seen in Fig. 5.13(e)-(f).

As a consequence of the direct visualization of the lithography result without detaching the SFM cantilever from the surface introduces a level of flexibility which is unperceived by any other lithography technique available. It is shown to be possible to "repair" delicate structures with nanometer precision, as illustrated in Fig. 5.14.

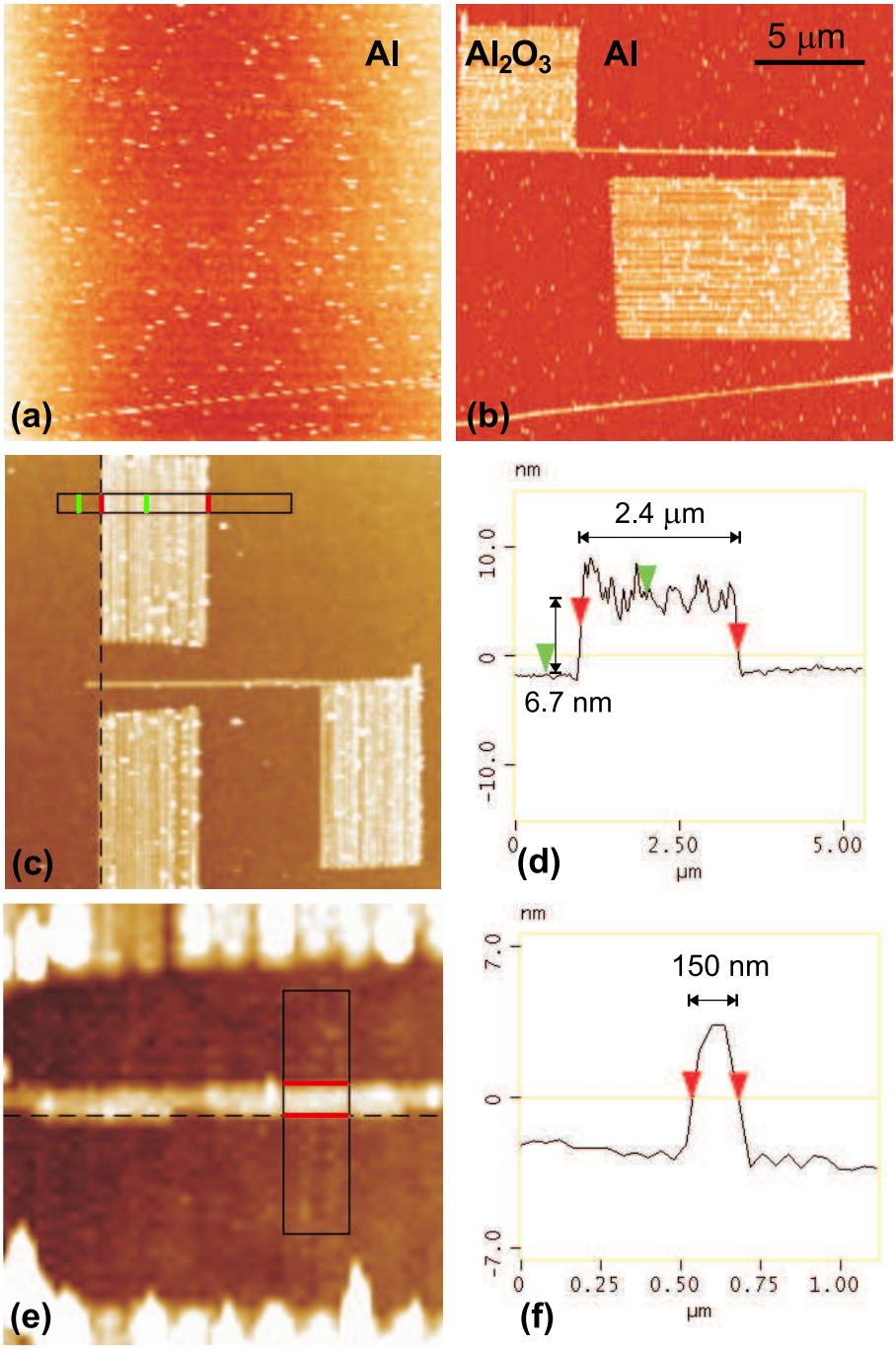

Figure 5.13: *SFM images of resonator patterns defined in 6 nm Al on SOI using SFM nanolithography. (a) Al/SOI surface before oxidization, the line at the bottom of the image is a scratch. (b) The cantilever pattern after lithography using 28 V and 4 µm/s. (c) Another cantilever structure, (d) the corresponding oxide step height is measured to be 6.7 nm. (e) A zoom in on the cantilever, (f) the cantilever oxide pattern is measured to have a linewidth of 150 nm.*

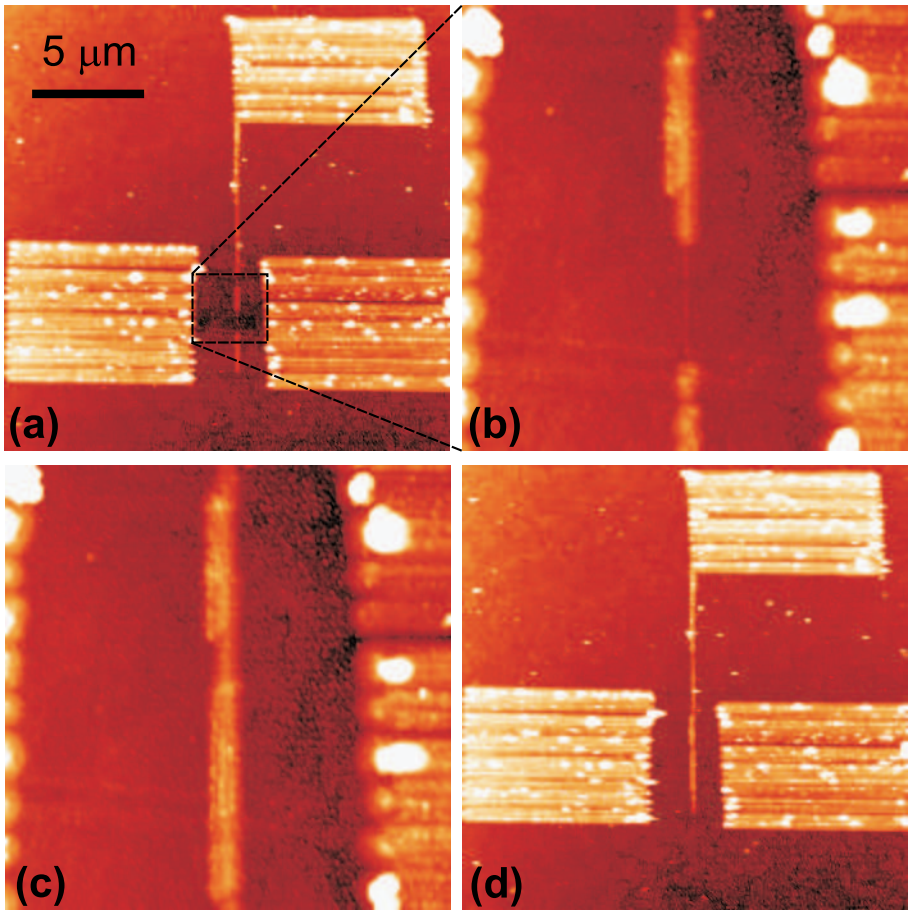

Figure 5.14: *SFM images after unsuccessful pattern definition. (a) The cantilever oxide pattern is inhomogeneous with areas which have not been fully oxidized. (b) Zoom in on the bottom part of the cantilever before and (c) after repairing the structure with nanometer precision. (d) The cantilever pattern after pattern repair.*

The technique has also been used for patterning on standard CMOS. This has been shown to be extremely cumbersome due to the surface roughness of the poly0 layer. The surface roughness necessitates that the cantilever in practise is operated in contact mode lithography which inevitably results in linewidth degeneration. Another problem as a consequence of patterning in contact mode using high voltages (50-60 V) was the phenomena of dielectric breakdown. The dielectric breakdown destroys the Al surface in the nanoarea completely, making it useless for further processing. This is shown by the change of color in the nanoarea as viewed by the CCD of the SFM. Furthermore, it is not possible to directly visualize the lithography result since the surface roughness of the poly0 is of the same order of magnitude or greater than the Al layer. Hence, the oxide volume expansion is not enough to give a clear topographical contrast. The only way to observe the result is optically which is not capable to render detailed information. Figure 5.15 shows an oxidized pattern on standard

CMOS and one can barely distinguish the cantilever and it is impossible to absolutely determine feature sizes.

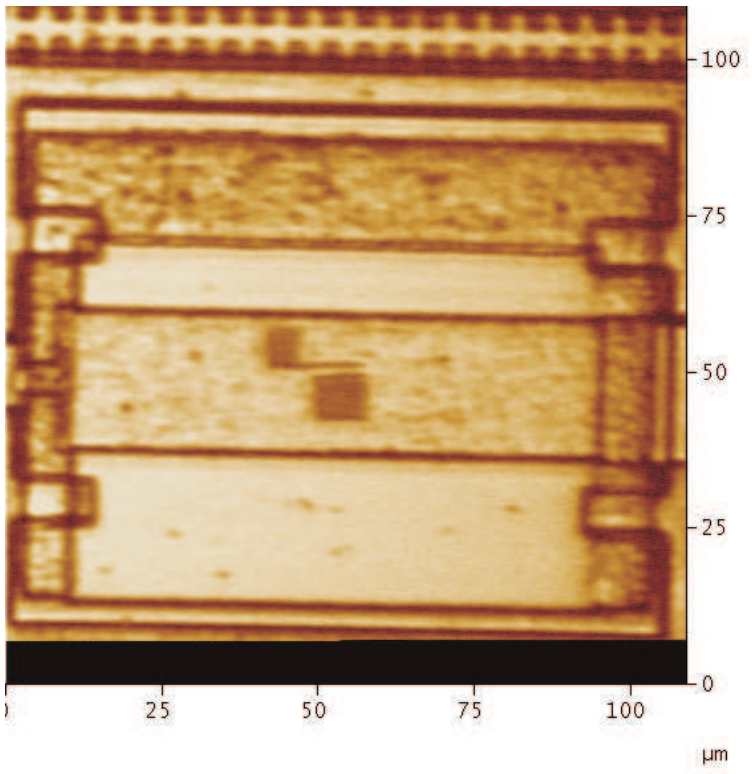

Figure 5.15: *Optical image of a cantilever structure defined on standard CMOS as obtained with the CCD of the SFM system.*

The possibility to directly monitor the oxidization result after lithography and the possibility to define patterns with linewidths below 10 nm makes SFM a powerful tool for NEMS prototyping. However this necessitates a flat (roughness<2nm) and clean surface. The maximum scan size which is feasible for reproducible results is 20×20 µm. If one desires to pattern larger areas the piezo needs to be retracted, the new position needs to be found, and the piezo needs to be let to stabilize as the cantilever is approached to the sample surface. All this is quite time consuming. Therefore SFM nanolithography needs to be combined with other lithography techniques in order to connect to µm-structures. Hence, SFM nanolithography at its present level is not a process technology that would be used for large scale production.

5.3.2 SFM Nanolithography Combined with Laser Lithography

In order to be able to connect NEMS devices defined by SFM nanolithography additional lithography needs to be added in order to define structures such as wires or

bonding pads.

By using direct write laser lithography based on oxidization as the complementary lithography technique seamless pattern transfer is achieved. The same Al layer is used for the two oxidation processes. After the SFM patterning the sample is ideally patterned as soon as possible using laser lithography in order to limit native oxide formation. Since the oxidization of Al on CMOS renders a color contrast, as seen in Fig. 5.15, it is possible to use the CCD of the laser system to make alignment onto a oxidized square as small as 3×3 µm. After the two oxidization processes the non-oxidized Al is etched using H_3PO_4 as previously described. Results of NEMS prototyping using a combination of SFM nanolithography and direct write laser lithography are shown in Fig. 5.16.

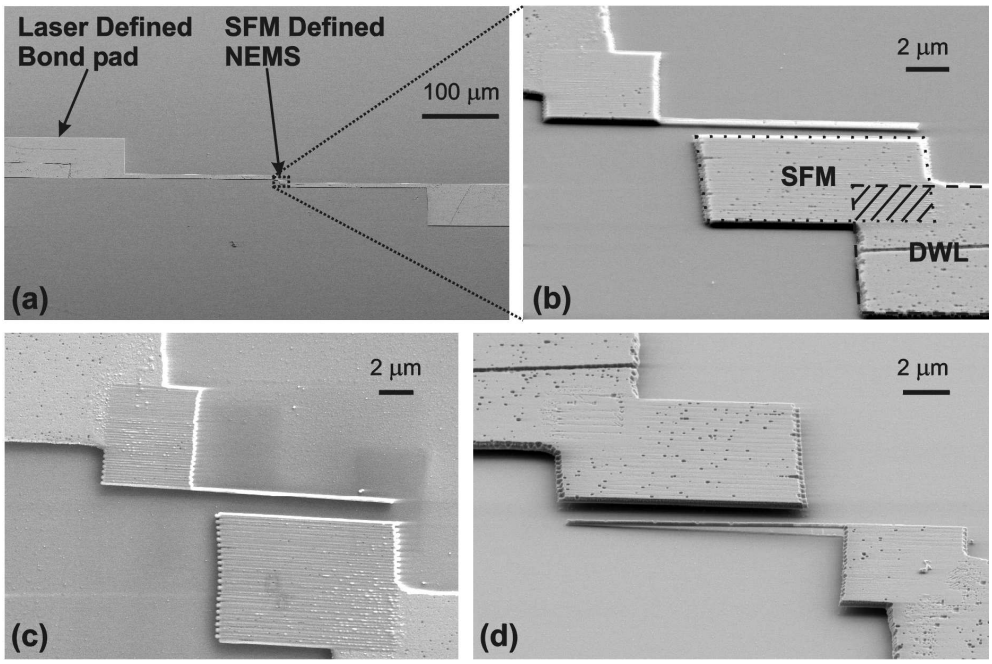

Figure 5.16: *SEM images of a NEMS resonator device defined by a combination of SFM nanolithography and direct write laser lithography. (a) Tilted view of NEMS structure defined by SFM and wire bonding pads defined by DWL. (b) Magnification of NEMS structure after anisotropic RIE. (c) Top view and (d) tilted view of a fully processed NEMS device.*

As another alternative it is also possible to use the other laser lithography technique based on ablation of a polymer followed by metal lift-off. In this case the CMOS chip is patterned by SFM and the non-oxidized Al is removed by the H_3PO_4 etching. Thereafter the chip is treated with the standard laser ablation process sequence. Examples of a structure defined on SOI-CMOS are shown in Fig. 5.17. After laser ablation and development, Fig. 5.17(a)-(b), a 30 nm thick Al film is deposited followed by lift-off, Fig. 5.17(c). The chip is thereafter treated with anisotropic RIE, Fig. 5.17(d), and finally the sacrificial oxide layer is etched using HF, Fig. 5.17(e).

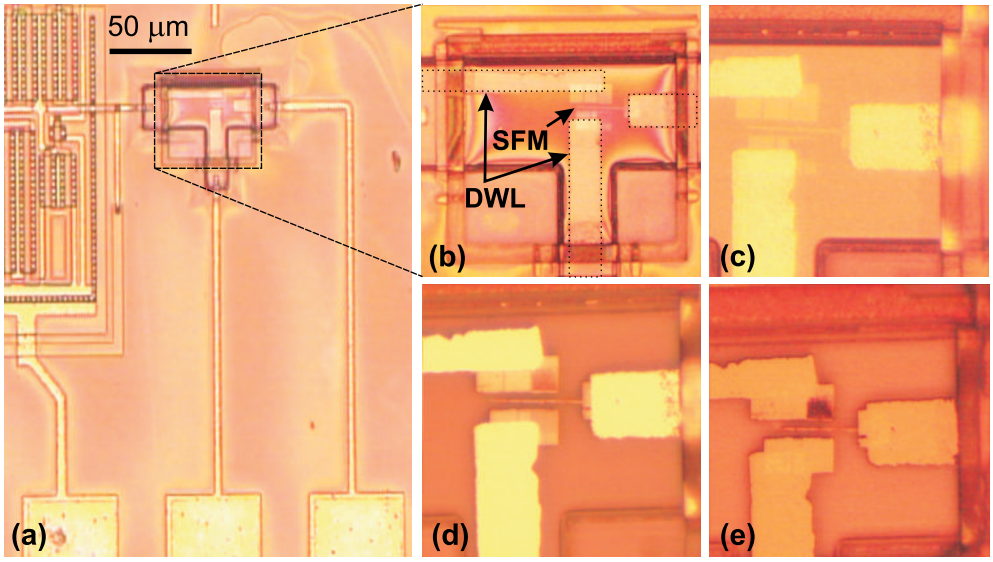

Figure 5.17: *SEM images of a NEMS resonator device defined by a combination of SFM nanolithography and direct write laser lithography on SOI-CMOS. (a)-(b) Images after the laser ablation process, followed by deposition of a 30 nm thick Al film followed by lift-off (c). The chip is thereafter treated with anisotropic RIE which transfers the etch mask pattern to the structural silicon layer (d), and finally the sacrificial oxide layer is removed by HF wet etching. The width of the cantilever is approximately 300 nm wide and the silicon thickness is approximately 1.3 µm.*

5.4 Electron Beam Lithography

Beginning with the worldwide use of SEMs in 1965, when the Cambridge Instrument Company in England marketed their Stereoscan 1 SEM, followed by the almost simultaneous release of the JSM 1 SEM by JEOL in Japan, a new type of lithography technique emerged. The possibility to use computers to move and control an electron beam over a sample surface with nanometer precision lead to the development of electron beam lithography (EBL), which has had an enormous impact on the development of IC and nanotechnology. The JSM 1 SEM had a resolution of 25 nm (at 25kV) and enabled 30,000×magnification. The year after the introduction of the JSM 1 SEM JEOL introduced their first electron beam lithography system.

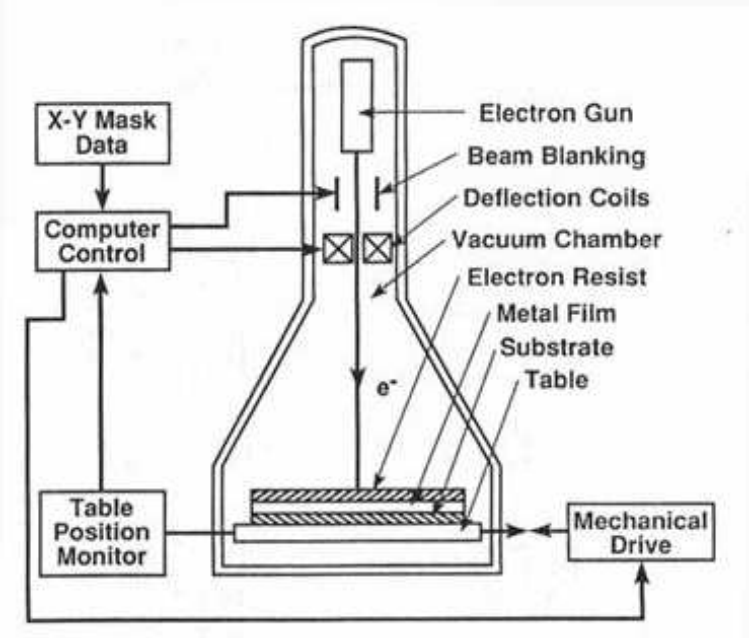

Figure 5.18: *Schematic illustration of the main constituents of an EBL and SEM system.*

The instrumentation principle of EBL and SEM systems is illustrated in Fig. 5.18. The most important parts are the electron source, which often consist of a thermal field emission emitter such as ZrO/W or LaB_6, that emits electrons when heated by an applied current. Various coils are used to produce electromagnetic fields which acts as electromagnetic lenses bending and focusing the produced electron beam. By using several electromagnetic fields acting along the beam path, the electrons are accelerated to the desired energy and can be focused to a specific point on the sample.

EBL is a serial lithography technique based on local electron exposure of a electron sensitive polymer film (resist). As the electron beam is scanned over the resist the electrons interact with the polymer resulting in a chemical change similar to photo lithography. The exposed resist is either cross-polymerized or the polymer chains are

broken (depending on the type of resist). After exposure the areas of the resist that has the lowest molecular weight can be rinsed away in dedicated solvents. Similar to photo lithography a pattern is exposed in the resist which thereafter is developed, revealing the defined structure.

EBL is the most common way of producing nanometer structures and is also used for production of high quality photo- and x-ray lithography masks. The resolution of an EBL system is resist and system dependant, but resist patterning down to some tenths of nanometers is routinely achieved. The resolution is mainly governed by the energy of the electrons, the beam current, the beam size/profile and the sensitivity of the resist.

5.4.1 EBL Process

Electron beam lithography has mainly been performed at Lund University by S. G. Nilsson [86] on standard CMOS, and preliminary processing has been performed on SOI-CMOS at MIC. The system at Lund University is a modified JEOL JSM 6400 SEM with a LaB_6 cathode. The system at MIC is a JEOL JBX-9300FS with a ZrO/W emitter. This JBX-system is able to define patterns on 12"-wafers with a stitching error of 10 nm.

Figure 5.19 illustrates the different processing steps as outlined below.

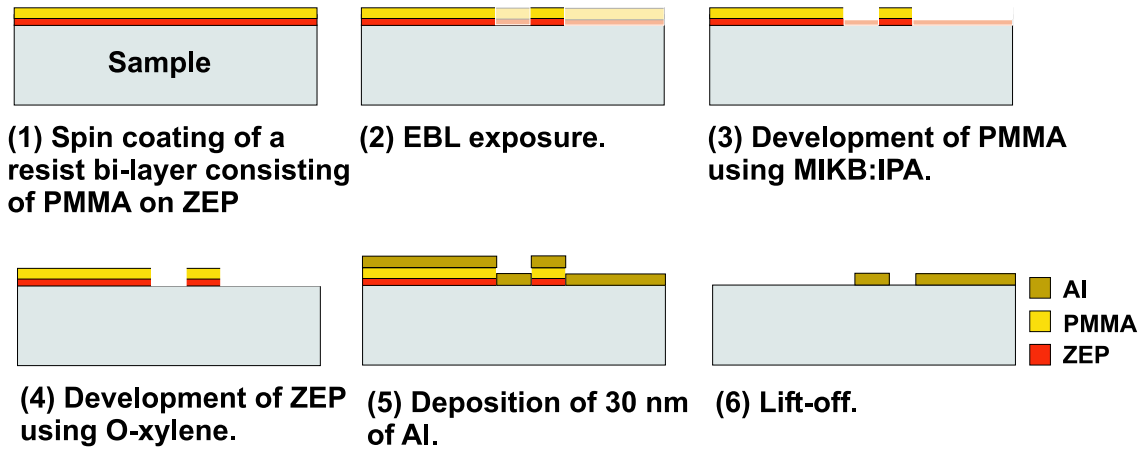

Figure 5.19: *Schematic illustration of the Electron Beam Lithography process used.*

A positive resist bi-layer system is deposited on the CMOS chips by spin coating. First, the CMOS chip is spin-coated with ZEP at a spin speed of 6000 rpm for 30 s after which the chip is baked on a hot-plate at 180°C for 15 minutes. Next, the CMOS chip is spin-coated with PMMA at a speed of 3000 rpm at 30 s after which the chip is baked at 180 °C for 10 minutes. A bi-layer composition of approximately 70 nm PMMA on top of a 130 nm thick ZEP layer is achieved, Fig. 5.19(1). The bottom layer consists of

approximately 170 nm of ZEP-520A7 and the top layer consists of approximately 70 nm of PMMA 950 A4. Following the EBL exposure, Fig. 5.19(2), the resists are first developed in a mixture of methylisobutylketone/isopropanol (MIBK:IPA; 1:3) for 60 s followed by rinsing in IPA for 30 s, Fig. 5.19(3). This step develops the top PMMA layer without affecting the underlying ZEP layer. Thereafter the ZEP is developed in O-xylene for 5 min with a final rinse in IPA for 30 s, Fig. 5.19(4). Then a 30 nm thick Al layer is thermally evaporated, Fig. 5.19(5), and lifted off, using warm acetone followed by PG Remover, Fig. 5.19(6).

Results

Examples of EBL defined cantilever mask structures using an acceleration voltage of 35 kV are shown in Fig. 5.20. As shown the mask is very well defined and and is an ideal RIE etch mask.

However, the use of the standard acceleration voltage of 35 kV severely damages the functionality of the CMOS circuitry. In order to circumvent CMOS damage the acceleration energy has been reduced to 3 kV which has shown to be well within the allowed irradiation energy range.

Low energy EBL exposure can be a method to achieve high resolution without CMOS irradiation damage. Examples of low energy EBL defined structures are shown in Fig. 5.21.

As schematically illustrated in Fig. 5.22 there is an approximately 1.7 μm step between the poly-Si layer and the protection layer for the circuitry. Spin coating with thin resist inevitably produces a thicker bi-layer at the edges of the structuring area. This complicates low energy EBL since the exposure dose needs to be much increased at these edges, but without overexposing the delicate CMOS circuitry which are in close vicinity. Even by locally increasing the dose by one order of magnitude, compared to the dose in the center of the nanoarea, does not improve the exposure quality sufficiently at the edges.

It is clearly seen that the low energy electron beam lithography allows pattern definition with as high quality as the case with high energy electron beam.

5.4.2 EBL Combined With DWL-TA

In order to solve the problem with insufficient exposure using low energy EBL a combination of low energy EBL exposure with laser ablation has successfully been implemented. First, low energy EBL (3 kV, in order to minimize irradiation damage) has been used for exposure on the resist bi-layer on CMOS. Second, DWL has been used for writing holes or "anchor points" using the identical resist bi-layer. The EBL defined structure are hence connected to the rest of the CMOS circuitry, using the laser method described in Chapter 5.2.3. After making the holes in the resist, the

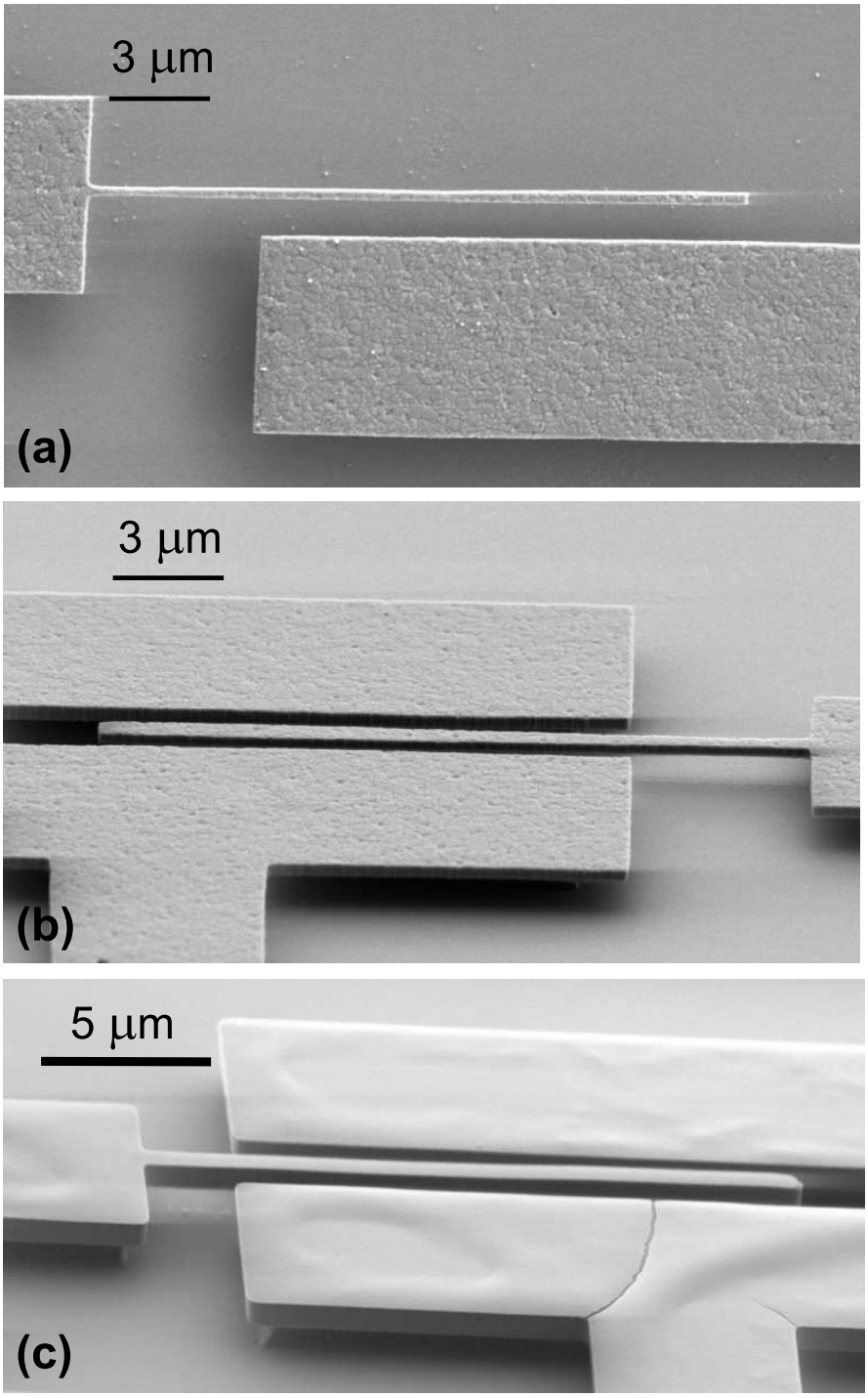

Figure 5.20: *SEM images of NEMS resonators defined by EBL (35 kV) on standard CMOS (a)-(b). (a) Top view of a 400 nm wide cantilever. (b) Tilted view of a 600 nm wide cantilever. Due to proximity effects the width is greater at the apex compared to the anchor point. (c) Shows a resonator structure defined on SOI-CMOS. The cantilever has a width of 600 nm, a thickness of 1.3 µm and a length of 20 µm.*

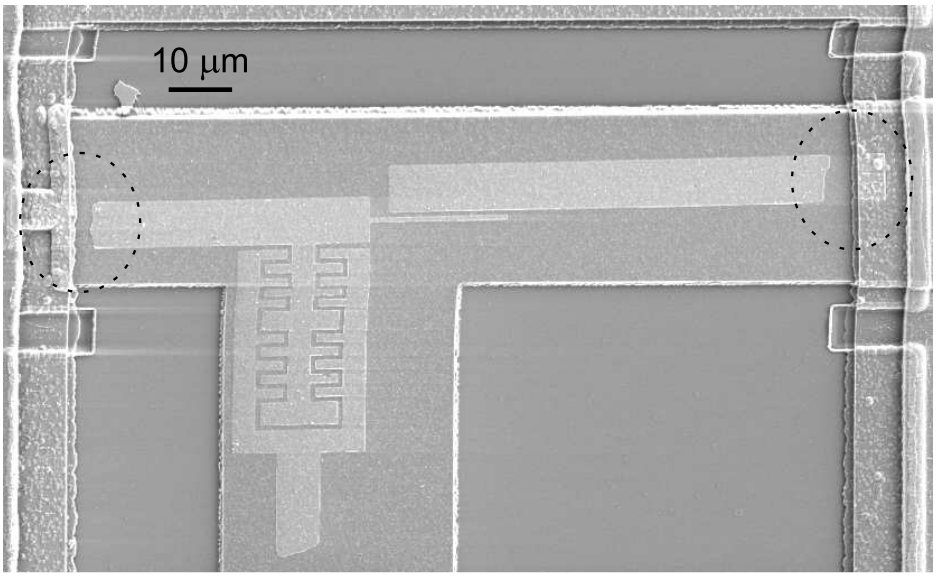

Figure 5.21: *SEM images of NEMS resonators defined by 3 kV EBL followed by 30 nm Al lift-off on standard CMOS. The pattern definition is comparable to 35 kV EBL, and cantilever width is 880 nm. However, due to insufficient exposure dose at the edges of the nanoarea, where the resist is as thickest, the mask does not connect to the CMOS circuitry and can hence not be used for processing.*

CMOS chip has been developed according to standard EBL processing scheme as previously described and metal lift-off has been achieved. As shown in Fig. 5.23 the edge uniformity and the lateral positioning control is excellent between the EBL and the laser defined areas.

Hence, on highly topographical samples such as CMOS chips, delicate EBL patterning can be achieved using low energy EBL combined with laser ablation. This method rendered the resonator devices which have been used for the performance characterization described in Chapter 7.

5.5 Summary

The lithography techniques which have been evaluated and used for the fabrication of resonator devices onto CMOS has been presented. These different techniques have all their merits and at a certain stage of the project it was difficult to identify a single preferred technique. Laser lithography has proven possible to fabricate devices in the 500 nm linewidth regime both using oxidization of Al thin films as well as by ablation of thin resist films. The yield and most importantly the reproducibility is an issue. The amount of native oxide on the Al, quality of Al deposition, surface roughness of

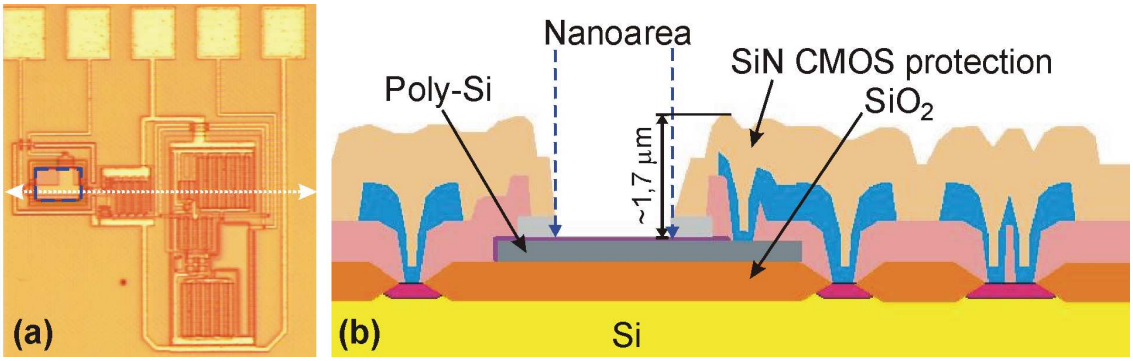

Figure 5.22: *Schematic illustration of the cross section of the nanoarea of the CMOS (a) and the 1.7 µm step from the bottom of the nanoarea to the surface of the CMOS (b). As a consequence low energy EBL is not capable to fully expose the resist at the edges of the nanoarea where the resist film is much ticker compared to the middle of the nanoarea, for which the exposure dose has been optimized.*

the poly0, as well as the varying thermal insulation of the oxide between individual CMOS chips are a true challenge to overcome. In the case of laser ablation the main problem is related to the uniformity of the resist spin-coating on a CMOS chip having a profile with multiple steps. These techniques have however been an important aid for the realization of devices using SFM nanolithography and low energy EBL.

SFM nanolithography has proven a powerful tool for situations when linewidth is the most important issue and throughput is set aside. But the implementation of SFM nanolithography on samples having a large surface roughness is not optimal and it is not possible to use the full potential of the technique. At present the throughput is low but there is potential for improvement using cantilever arrays similar to the idea behind the IBM millipede project.

Low energy EBL has been the technique which has met the requirements of reproducible fabrication of resonators with linewidths below 500 nm. The encountered problem regarding the pattern definition at the edges of the nanoarea have been circumvented by a combination of lithography techniques.

The fundamental properties of the lithography techniques are summarized in table 5.5.

Lithography Technique	Type	Resolution Limit	Typical Metal Thickness	Patterning Time	Advantage	Disadvantage
CPL	Parallel	500 nm	30-50 nm	5 min	High Throughput and Reproducibility	Flat sample surface needed.
EBL	Serial	10 nm	30-50 nm	3.5 h	Resolution and Reproducibility.	CMOS irradiation damage.
SFM	Serial	10 nm	6-8 nm	7 h	Resolution.	Low throughput and necessitates a small surface roughness.
DWL-TO	Serial	500 nm	6-8 nm	1 h	Flexibility	Necessitates small surface roughness.
DWL-TA	Serial	500 nm	30-50 nm	1.5 h	Flexibility	Flat sample surface needed.

Table 5.1: Summary of different lithography techniques for definition of MEMS/NEMS on CMOS. The resolution should be interpreted as the minimum line width obtained in the metal mask layer. The patterning time has been approximated for structuring 20 100×100 µm areas including pre-handling time.

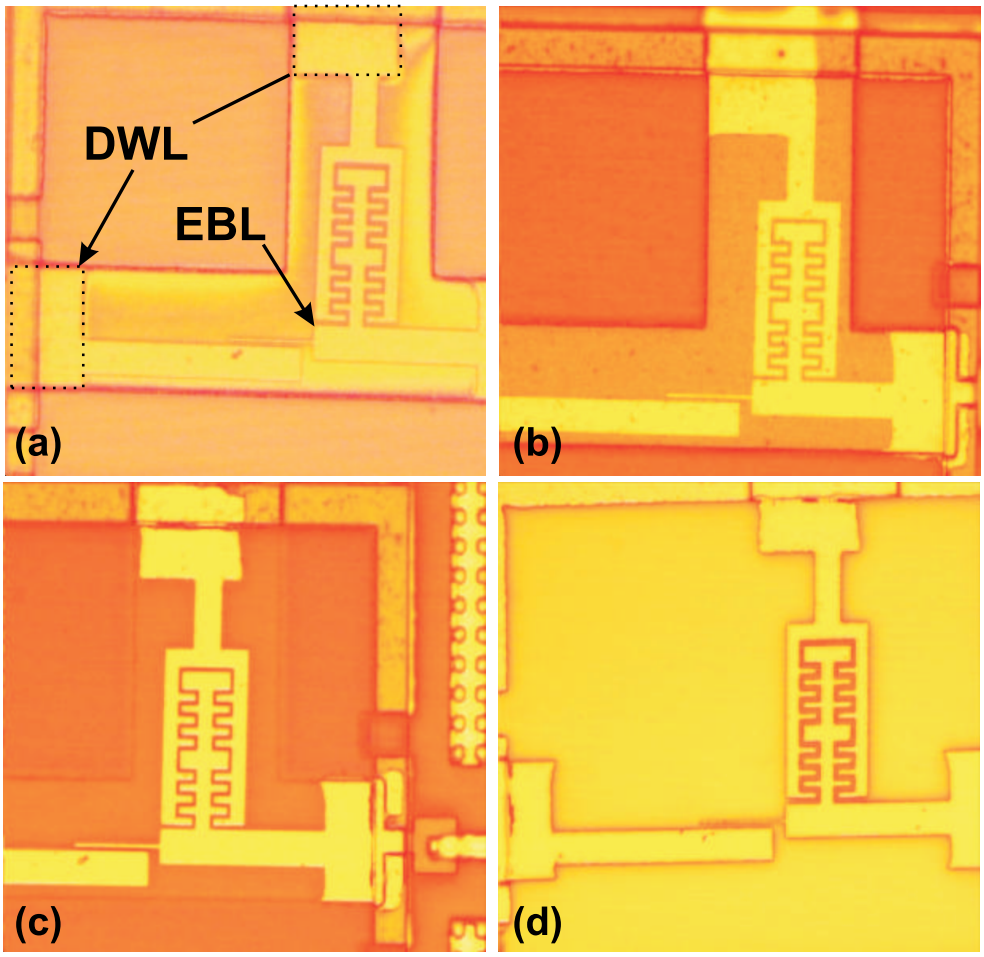

Figure 5.23: *Optical images of cantilevers defined by EBL combined with DWL-TA. The laser ablation is performed after the EBL exposure, but before the development of the resists. (a) After EBL and DWL. (b) After 30 nm Cr lift-off. (c) After anisotropic RIE. (d) After final release. (e) SEM image of a fully processed NEMS structure as defined by EBL combined with DWL.*

Chapter 6

CMOS Post-Processing

The goal to develop ultra sensitive nano/micro-mechanical mass sensors based on electrostatic actuation and capacitive readout necessitates that the electronics for signal conditioning and amplification should be as close as possible to the mechanical devise. This is in order to minimize the external noise contribution from the parasitic capacitance. If one would use standard off-ship electronics and wire bonding the parasitic capacitance would totally screen the capacitance signal of the resonance measurement of the system. CMOS integration is a way to reduce the contribution of the parasitic capacitance since the integrated current amplification circuits can be placed within 50 µm of the mechanical device.

Within the *Nanomass II* project both standard poly-Si CMOS as well as CMOS having integrated silicon-on-insulator (SOI) islands have been evaluated. The monolithic integration of resonators with CMOS is a non-trivial task, and during the project several compatibility issues during fabrication have been encountered. The technological obstacles and the way to circumvent them are discussed in the following chapter. A condensed process sequence can also be found in Appendix 16.

6.1 The Post-Process

The fabrication of the resonators is based on CMOS compatible surface micromachining steps, such as reactive ion etching (RIE) and wet chemical etching. As shown in the process flow chart in Fig. 6.1 the first task is to define an etch mask by lithography, Fig. 6.1(b), consisting of Al, Al_2O_3 or Cr. This part is described in Chapter 5.
After the lithography process the defined metal pattern is used as an etch mask for anisotropic RIE using an SF_6:O_2-plasma, Fig. 6.1(c). After the RIE process of the CMOS chip a protection mask is applied in order to protect the CMOS circuitry from the hydrofluoric acid (HF) wet etch which would etch the Al wires of the circuitry. The protection mask is achieved by standard contact mask photolithography using 2.5 µm thick AZ5214E photo resist which has been baked at 120°C for 1 min, Fig. 6.1(d). Before spin-coating the CMOS chip has been treated with a HMDS-treatment which consists of a gas phase silanization process in order to improve the adhesion of the

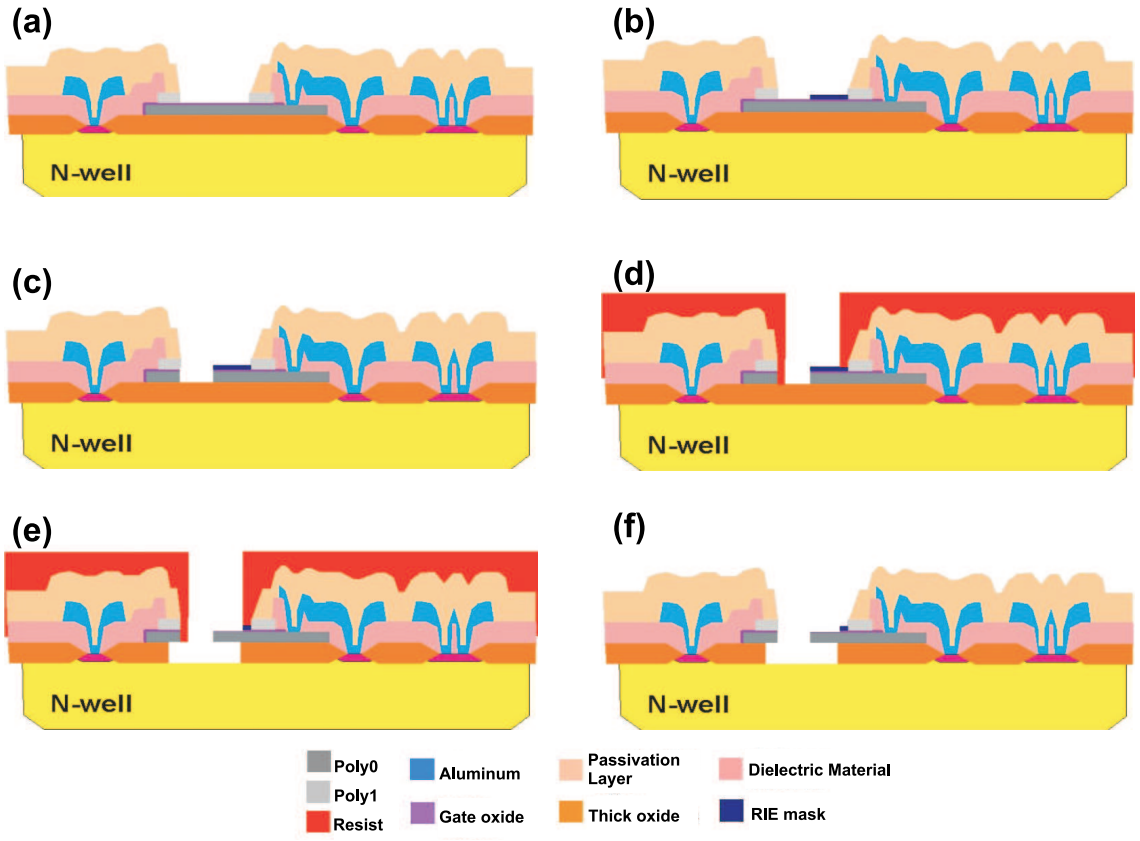

Figure 6.1: *Schematic illustration of post-process steps. (a) CMOS with defined nanoarea. (b) Metal masking by lithography, followed by anisotropic RIE (c). A protective resist film is spin-coated, followed by photo lithography (d). The cantilever is released by an isotropic wet etch of the SiO_2 using BHF (e) followed by a dry plasma release (f).*

resist. After exposure and development the only area which is exposed to the HF-acid is the nanoarea of the CMOS. The Al/Al_2O_3 etch mask has also been removed since it is etched by the developer. Hence, it is critical that the resist coverage is homogenous and that a good step-coverage is achieved, otherwise there is a large risk that the developer might etch the wires of the CMOS circuit. The final release of the cantilever is achieved by sacrificial wet etching of the SiO_2 layer. The SiO_2 is etched by buffered HF, Fig. 6.1(e). Thereafter the chip is rinsed thoroughly with deionized water after which the protective resist is remover in acetone. The sample is never allowed to be dried out during the etching and rinsing since capillary forces would otherwise act on the cantilever which can collapse onto the substrate surface. Stiction is avoided by coating the chip with resist while the chip is kept in a liquid. After spin-coating and soft-baking the resist is removed by a oxygen plasma in a RIE which etches the resist and releases the cantilever, Fig. 6.1(f).

6.2 Reactive Ion Etching

Reactive ion etching (RIE) is based on the combination of the chemical activity of the gaseous species generated in a plasma and the physical effect caused by ion bombardment on the material which is to be etched. This makes RIE a highly versatile micromachining technique since the variety of available process parameters to be optimized, such as the mask material, etch material, chamber operation pressure, gas mixtures, and acceleration voltage. Figure 6.2. illustrates the basic RIE system.

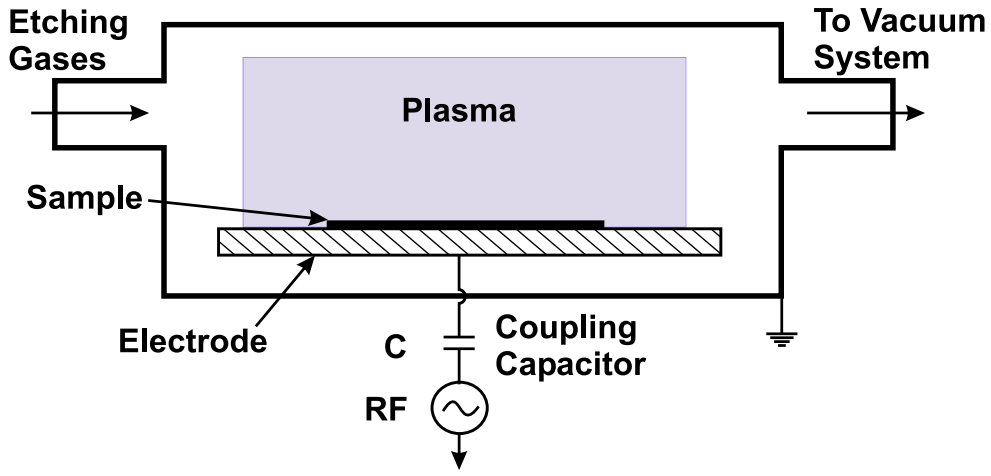

Figure 6.2: *Illustration of a basic RIE system. The sample to be etched is placed on a RF powered electrode.*

Anisotropy is achieved by optimizing the process parameters so that the sidewall of the etched structure is coated by an etch inhibiting film. The sidewalls of an etched structure is not exposed to the ion bombardment, which results in that gaseous species will remain on the sidewalls hence inhibiting the surface reactions causing the etching. The bottom of the etched structure is continually bombarded with ions which prevent molecules to remain on the bottom of the structure.

For the anisotropic RIE of the poly-Si of the standard CMOS an gas mixture consisting of 30 sccm O_2 and 10 sccm SF_6 using a RF power of 35 W at 80 mTorr gives an undercut of roughly $\frac{1}{7}$ of the etch depth. By an etch rate of the order of 125 nm/min the standard CMOS is etched for 7 min. The extended time is to ensure complete etching through the layer since there can be poly0 thickness variations by as much as $\pm$200 nm. SEM images of resonator devices after anisotropic RIE on SOI are shown in Fig. 6.3.

In order to further improve the anisotropic RIE of poly-Si CHF_3 could be added to the gas mixture. This might be needed for the successful pattern transfer using mask with minimum linewidth which are below one fifth of the thickness of the Si layer to be etched.

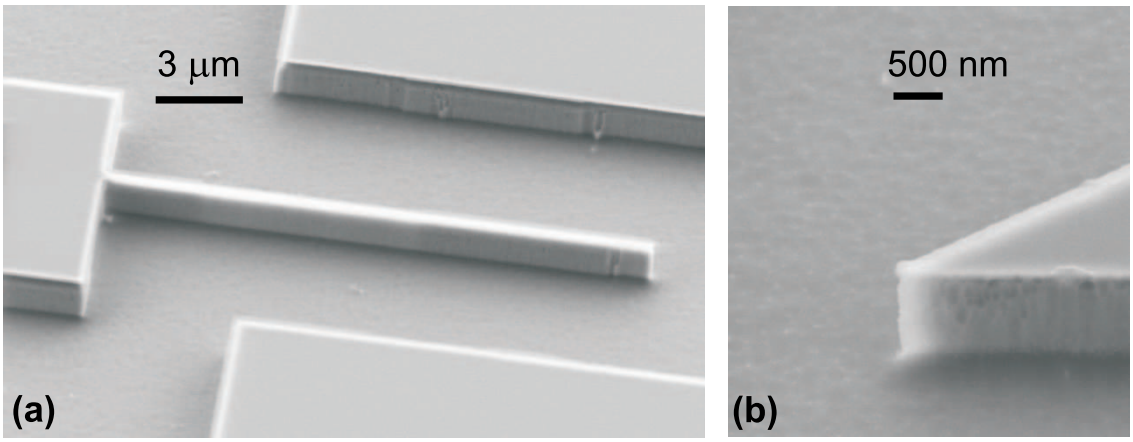

Figure 6.3: *SEM images of resonator structures after anisotropic RIE. (a) The width of the cantilever is 400 nm and the thickness of the silicon of the SOI is 1.3 µm. (b) Magnification of a section of another device which displays the vertical sidewall after anisotropic RIE.*

6.3 Stiction

In fabrication of MEMS and NEMS devices by surface micromachining often rely on wet etching of a sacrificial layer in the final release of the mechanical structure. As the structural dimensions decrease the surface/volume ratio increases and as a consequence the physics at surfaces become increasingly important. Specifically, avoiding stiction of suspended micro- or nanostructures becomes an important processing issue [52].

The fabricated resonator within this project are typically separated from nearby surfaces by distances of the order of a µm or less. Hence, there is a large risk of stiction caused by capillary forces originating from the dehydration of meniscuses formed between suspended structures and these surfaces after complementary rinsing following the wet etching steps [87]. In order to avoid stiction caused by capillary forces techniques such as vapor phase HF- etching [88] and critical point drying [89] have been developed which avoids meniscus formation. However, these techniques are generally complicated processes, and within the frame of this project vapor phase HF-etching is not applicable due to possible damage of the CMOS. Instead, two other techniques have been evaluated. These are freeze drying and an oxygen plasma based dry release using a resit as an intermittent sacrificial layer.

6.3.1 Freeze Drying

Freeze drying is a method in which the liquid meniscus formation is circumvented by having a direct transition from solid to gas phase of the final solvent in the sacrificial SiO_2 wet etching process. The condensed process can be found in Appendix 17.

After the sacrificial wet etching of the SiO_2 layer using hydrofluoric acid (HF) the chip is is thoroughly rinsed in de-ionized water for 5 minutes. Thereafter the resist layer protecting the CMOS circuitry from the BHF is dissolved using acetone. After rinsing the chip in propanol the chip is immersed in liquid tert-butanol (TB). The TB has been heated on a hot-plate at 50°C in order assure that the TB has been liquified, the freezing temperature of TB is 25°C. The chip, covered with liquid TB, is placed on a ceramic cooling plate inside a small vacuum chamber immediately freezing the TB to solid form. The TB slowly evaporates as the chamber is evacuated. After leaving the chip in vacuum for 12 h the TB has evaporated completely and the suspended structures have been released.

By using the freeze-drying method stiction caused by meniscus dehydration is circumvented. However, the technique has a disadvantage. One of the problems with the freeze drying technique is the risk of contamination. Figure 6.4 shows an example of a cantilever structure with large amount of contaminants on the surface after freeze drying. This is highly undesirable for the production of any sensor system and becomes a critical issue when the contaminating particles and the dimensions of the mechanical sensor system are of the same size range. The contaminations are possibly caused by chemicals having a lower freezing temperature than the TB, e.g. water, and the TB needs to be used as fresh as possible in order to limit contaminations.

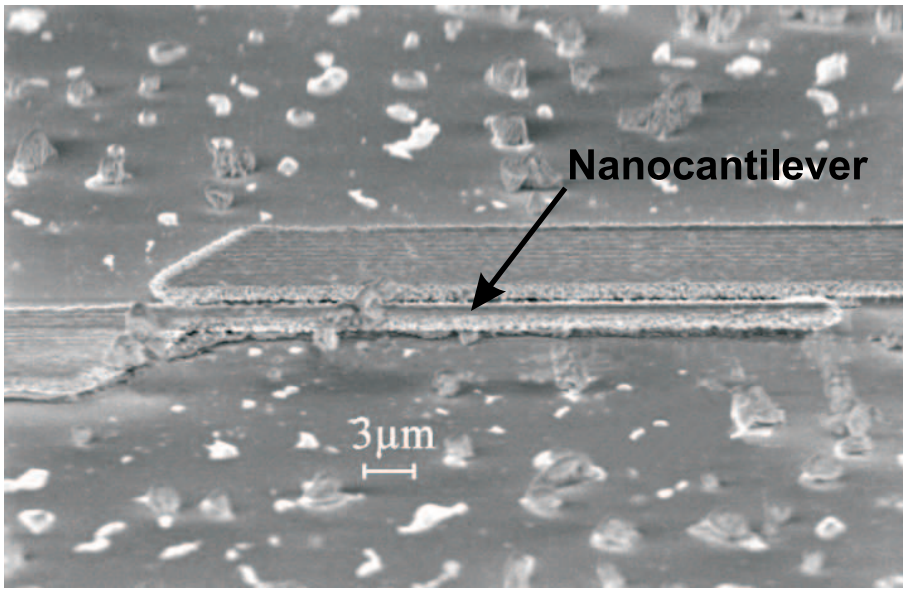

Figure 6.4: *SEM image of contaminations after the Tert-Butanol release.*

6.3.2 Dry Plasma Release

Due to the contamination issues concerning the freeze drying technique a dry release process using an intermittent sacrificial layer has been investigated [87] as suggested

by Orpana *et al.* [90]. The process is based on plasma etching of an sacrificial resist which acts as a support for the suspended NEMS device. The condensed process sequence is listed in Appendix 18.

After that the cantilever has been released from the substrate by an isotropic wet etch of the sacrificial SiO_2 layer, using hydrofluoric acid (HF), it is thoroughly rinsed in de-ionized water and the protective resist layer is dissolved using acetone. The sample is not allowed to dry at any point during the rinsing/coating process. Subsequently, the sample is placed in acetone, after which liquid photoresist (AZ5214E) is applied until the liquid covering the sample is concentrated resist. The AZ-resist covered sample is then spun at 3000 rpm for 30 s and subsequently soft-baked at 90°C, resulting in a 1.7 µm thick resist layer fully encapsulating the suspended cantilever, as shown in Fig. 6.5(a).

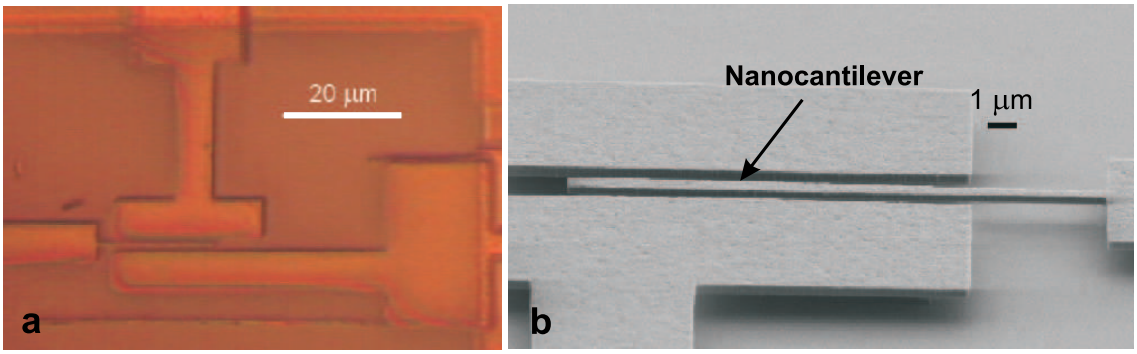

Figure 6.5: *Optical image showing a suspended cantilever structure integrated on a CMOS chip. The cantilever is fully encapsulated in resist and is not sticking. (b) SEM image showing a cantilever structure fabricated using the dry release method. The cantilever is 30 µm long with a width of roughly 450 nm as defined by 35 kV EBL. The cantilever thickness is 600 nm and the gap between the cantilever and the substrate is 1 µm.*

By inspection of the focal plane of the cantilever, compared to the parallel electrodes, using an optical microscope one can determine that the cantilever indeed is freestanding. The resist layer acts as a support for the suspended mechanical structure. Finally, the structure is released using RIE by a oxygen plasma (99:20 sccm O_2:N_2, 30 W, 80 mTorr for 15 min).

The dry release method does not damage structures of nanometer dimensions and has been implemented in the cantilever production. Furthermore, it reduces the risk of contamination which is important for the fabrication of sensor systems. Another benefit is the possibility to store and transport a fabricated device encapsulated in resist without the risk of stiction induced by electrostatic interaction or mechanical chock.

6.3.3 Anti-sticktion Layer

In addition, in order to reduce in-use stiction after the release, it is possible to expose the released device to a CHF_3 plasma. This deposits a fluorocarbon (FC) film on the device acting as an anti-stiction layer. Plasma deposited FC films have previously been used as anti-stiction layers and have shown excellent anti-stiction properties [91]. Moreover, plasma deposition has shown to produce thin FC film thicknesses of the order of a few nm [92], which is highly desirable in NEMS production. X-ray emission spectroscopy can be used for the confirmation of the existence of the FC film. X-ray emission spectra acquired with energy dispersive spectrometry (EDS) inside a scanning electron microscope (SEM) using 3 keV electrons show the expected fluorine signal at 0.68 keV and a carbon signal at 0.28 keV, Fig. 6.6. An untreated Si refer-

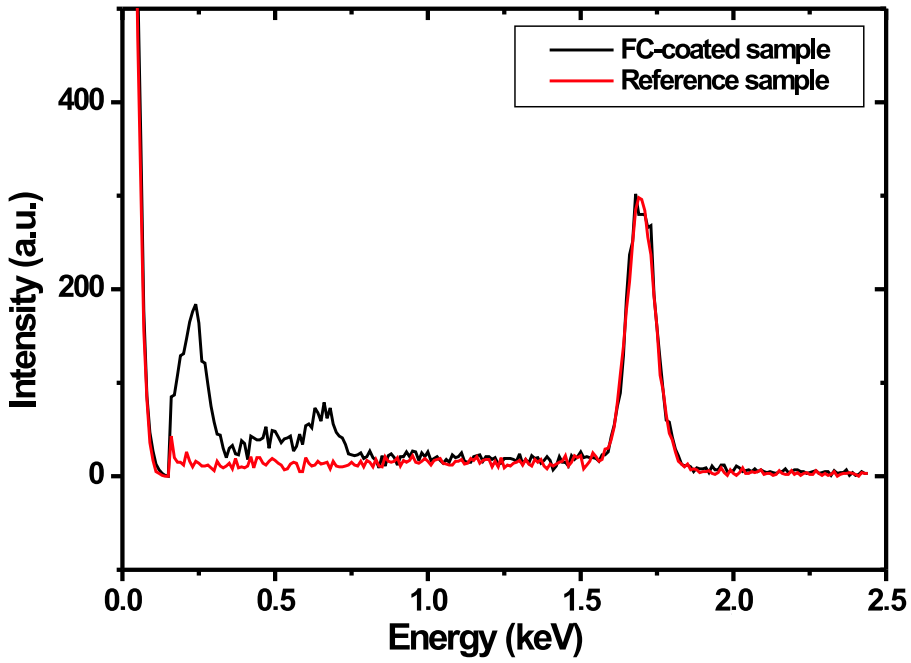

Figure 6.6: *X-ray emission spectra acquired with EDS inside a SEM, using a 3 keV electron energy. The CHF_3 plasma treated sample shows the expected fluorine signal at 0.69 keV and the carbon signal at 0.28 keV, compared to the un-coated reference sample which only shows the Si signal at 1.74 keV.*

ence sample does not display these peaks, confirming the existence of a fluorocarbon coating. Ellipsometry was not a viable way to measure the FC film thickness due to the very thin coverage. Similar FC plasma coatings have previously been examined by x-ray photoelectron spectroscopy (XPS) and revealed a film thickness of about 5 nm [92].

6.4 CMOS Compatibility

The compatibility between the CMOS performance and the used lithography techniques has been made. The characteristics such as the threshold voltage for the NMOS and PMOS transistors have been monitored before and after processing. A brief summary of result achieved by F. Campabadal at UAB is presented in this section.

6.4.1 CMOS Compatibility: DWL

After DWL processing no significant difference is observed compared with results obtained before CMOS processing. In particular the threshold voltages for NMOS and PMOS transistors, Fig. 6.7, for the measured chips show no significant difference after laser processing. Therefore it can be concluded that monolithic integration of cantilever structures with CMOS circuitry using DWL and the surface micromachining steps described in this chapter does not cause significant CMOS compatibility issues.

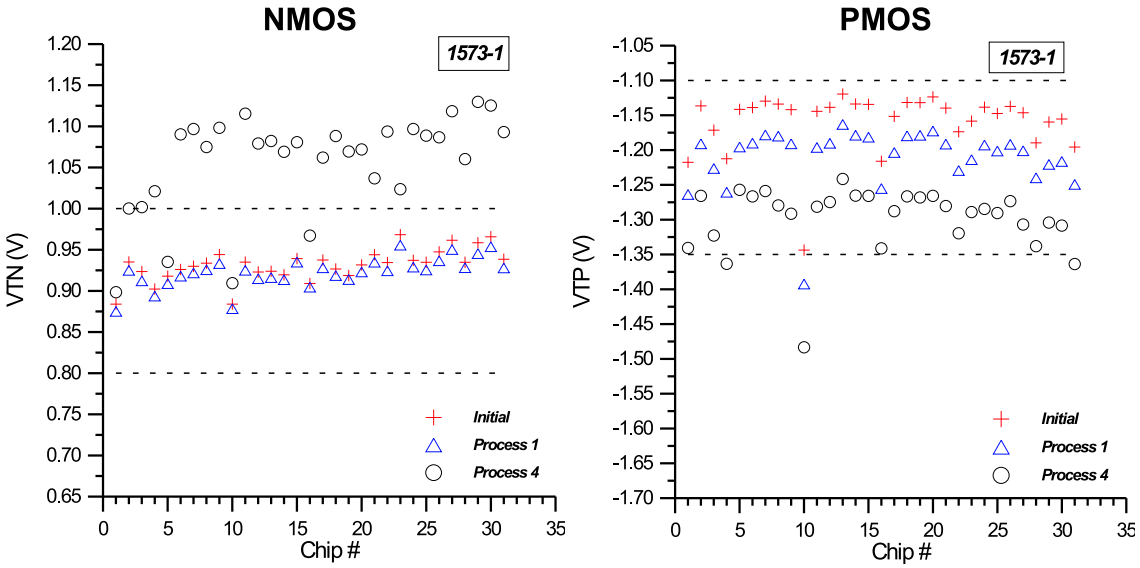

Figure 6.7: *Graph showing the threshold voltage for CMOS NMOS and PMOS transistors before and after laser processing. Process I stands for the definition of the nanoarea using RIE. Process 4 stands for the full laser lithography process including the release of the cantilever structures. The dotted lines highlight the acceptance level of the CMOS foundry, which does not mean that a slightly higher/lower value means that the circuit does not work.*

6.4.2 CMOS Compatibility: EBL

A compatibility study regarding the influence on the performance of the CMOS circuitry due to exposure to an high energy electron beam was performed. The reason for the investigation was that it was observed that the performance of the CMOS circuitry degraded after conventional EBL processing. In this study the poly0 layer

of the nanoarea of the CMOS has been exposed at Lund University using electron energies of 4 kV, 10 kV, 15 kV, and 35 kV followed by 30 nm Al lift-off. The poly0 layer is electrically connected to the gate of an NMOS transistor. Since the NMOS transistor has the four terminals available, it is possible to measure the complete electrical characteristics of the transistor.

The electrical characterization of the NMOS transistor revealed that high energy EBL indeed changes the characteristics. The results obtained for the 5 processed samples at the same conditions are summarized in Fig. 6.8.

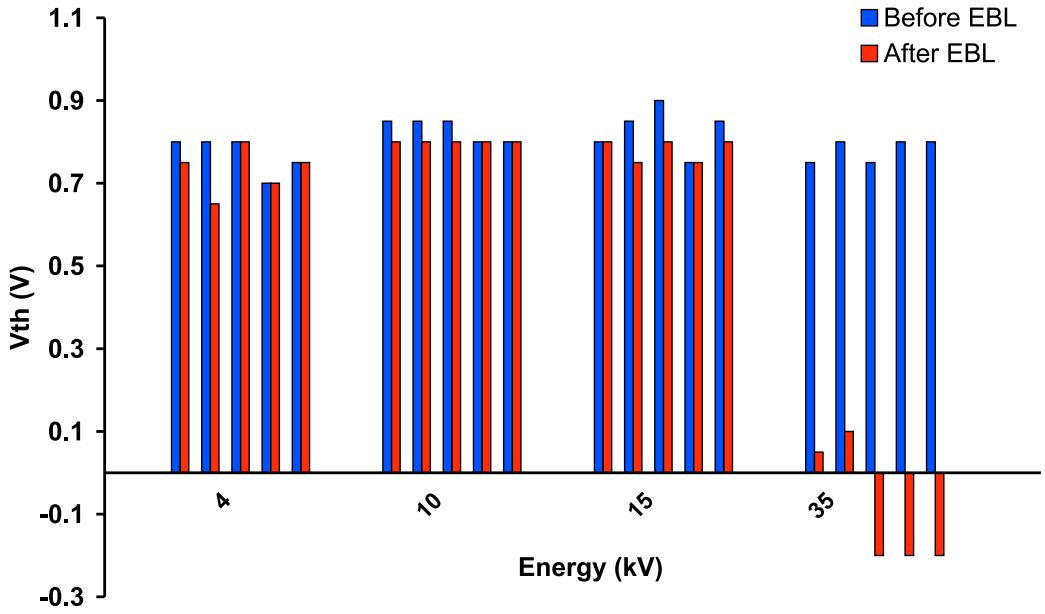

Figure 6.8: *Graph showing the threshold voltage for NMOS transistors before and after EBL processing.*

In view of these results we can conclude that EBL processing of resonator devices on CMOS leads to a degradation of the NMOS transistor characteristics when the EBL is carried out at an e-beam acceleration voltage of 35 kV. The most severe degradation corresponds to a shift of the threshold voltage to negative values of the order of 0.9 V.

When EBL is carried out at acceleration voltages lower than 15 kV, most of the differences are within the tolerances for the CMOS technology used, and would consequently not lead to a significant degradation of the performance of the CMOS circuitry.

The finding that EBL seriously effects the CMOS circuitry has also resulted in that

SEM inspection of fabricated devices has been limited, even using acceleration voltages as low as 3 kV. This is since when one performs SEM on CMOS chips inevitably the whole circuit is exposed which is not the case for EBL where only the nanoarea is exposed. As one measures the out-put signal of a plain CMOS chip without any processing the coupling between the input voltage and the out-put voltage is degraded over a time period of 30 min using an acceleration voltage of 3 kV, which is a typical SEM inspection time.

6.5 Summary

The CMOS compatible post-process has been described. The main difficulties in the post-processing of standard CMOS have been related to:

- Quality of the RIE etch mask. The mask quality has been improved by 30 nm thick metal masking using EBL and DWL-TA.
- Thickness variations of the poly0 layer, which occasionally has complicated the anisotropic RIE by over/underetching.
- Inadequate adhesion of the HF-protective resist film, which results in etching of the CMOS Al wires by the developer and the HF-acid. The adhesion has been improved by adding an adhesion promoter by HMDS-treatment.
- Process induced stiction by capillary forces. This has been circumvented by a dry release process.

Furthermore, it has been identified that high energy EBL severely degrades the performance of the CMOS circuitry. In order to circumvent irradiation damage acceleration energies below 15 kV should be used. Another option would be to try to ground the poly0 layer during EBL exposure. This has not been feasible for the EBL systems used.

Chapter 7

Device Characterization

The electrical characterization of the cantilever based mass sensor system is described in the following chapter. The resonance response has been verified both optically as well as electrically using the on-chip electronics. A custom made chamber has been assembled in order to ensure characterization in a controlled environment. CMOS chips having single cantilever devices as well as chips having arrays of 4 or 8 cantilever structures have been characterized using this chamber. Finally, the mass sensitivity in air has been investigated by placing punctual masses (latex beads, glycerine drops) onto the apex of the cantilever and measuring the resulting frequency change.

7.1 Optical Verification

Initial optical verification in air has been preformed by mounting the chip on a probe station and then monitoring the resonance of the cantilevers using the microscope of the probe station. Since the width of the cantilevers is below 1 μm the microscope renders a blurred image of the outline of the cantilever. Hence, a detailed characterization of the resonance frequency and other properties such as the Q-factor is not possible using the present optics of the probe station. However, the method is useful for determining which devices are mechanically functional and also to deduce the approximate position of the resonance frequency for later more detailed studies using the on-chip electronics.

7.2 Controlled Environment Chamber

Detailed characterization of the cantilever system is performed in a custom made chamber in which the pressure is controllable. The chamber has been assembled at MIC by R. Sandberg and W. Svendsen [93] at the Department of Micro and Nanotechnology as part of the *Nanomass II* project and is illustrated in Fig. 7.1.
The chamber is made out of stainless steel due to its small chemical reactivity. There are electrical connections inside the chamber for connecting the chip to the measurement equipment outside the chamber using KF-flanges. At present the pressure can

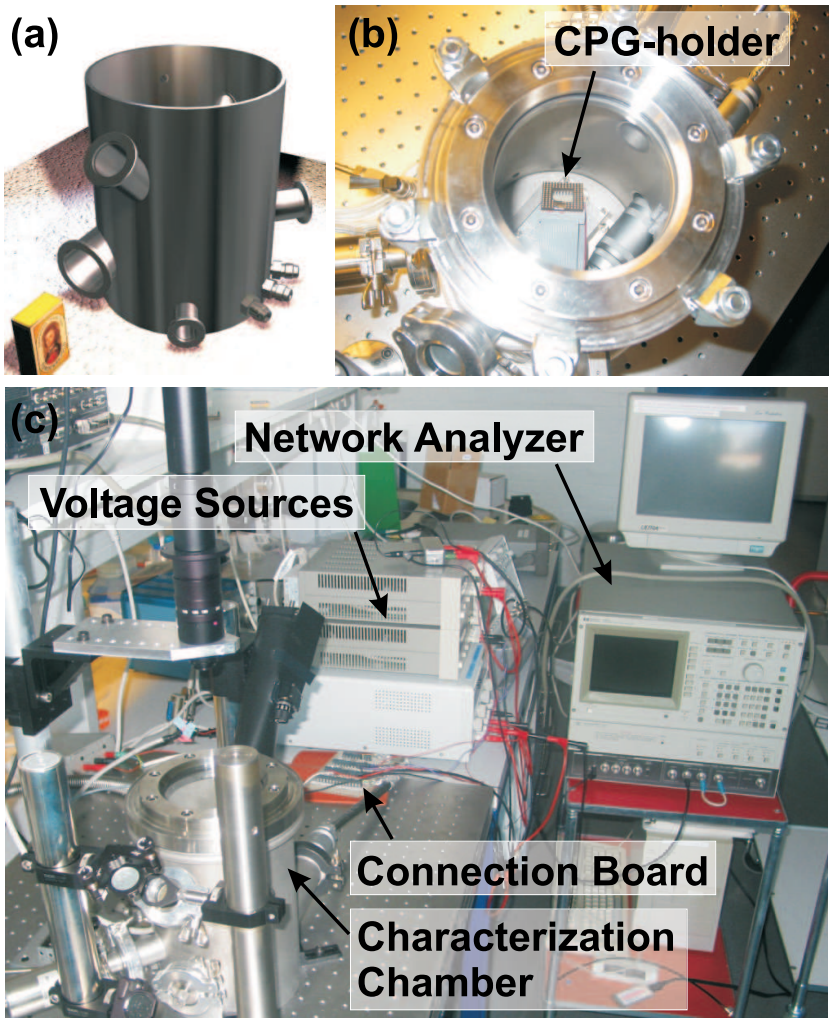

Figure 7.1: *Gas chamber illustration (a) and image from the lab (b)-(c). (b) Top view showing the connection grid for the CMOS chip mounted on a CPG inside the chamber. (c) The external measurement equipment.*

be controlled down to 10^1 Pa, and the future objective is to have the possibility to have a pressure down to 10^{-2} Pa.

7.3 Measurement Instrumentation

In order to be able to measure inside the chamber the chip is mounted on a ceramic pin-grid chip (CPG) (*CPG12006, Spectrum Semiconductor Materials*) using double sided carbon-tape, as shown in Fig. 7.2.
The electrical connections to the pin-grid chip are made by standard wire bonding between the CPG-pads and the appropriate bonding pads on the chip using a Wedge bonder. It is possible to have up to 5 devices simultaneously wire bonded on the CPG. The bonding scheme is displayed in Fig. 7.3.

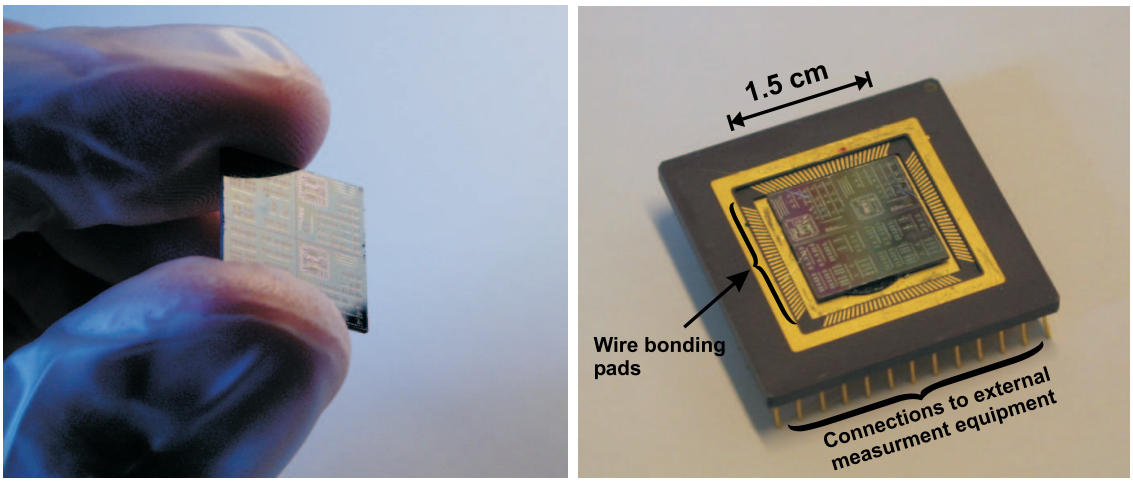

Figure 7.2: *Wedge bonded CMOS chip mounted on ceramic pin-grid chip (CPG).*

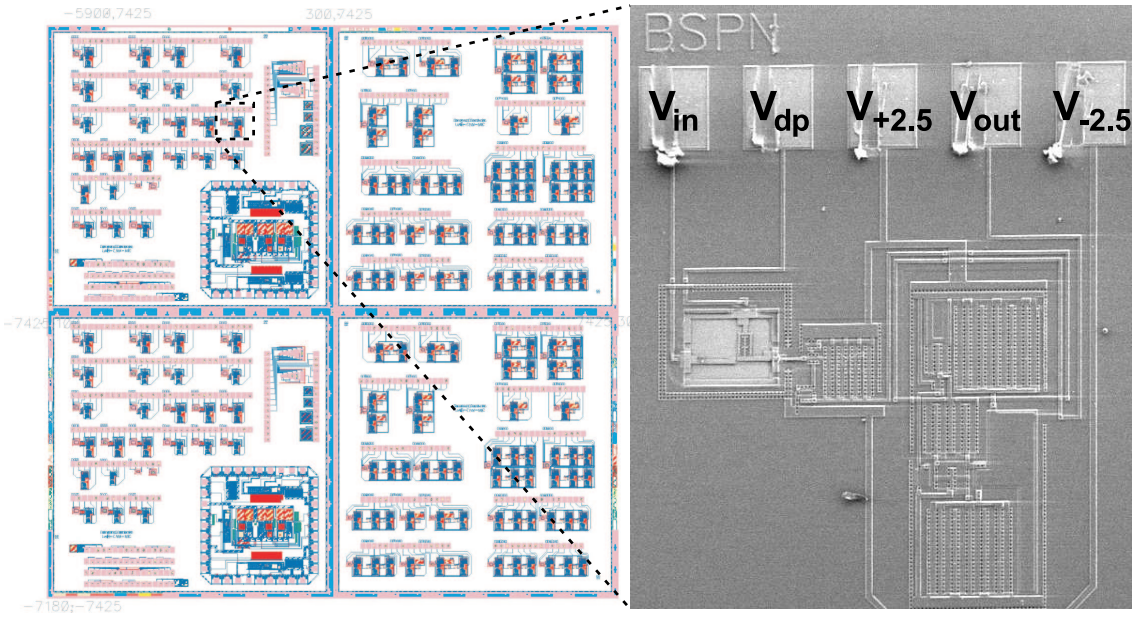

Figure 7.3: *An illustration of the CMOS chip and a SEM image of a single system with the connection scheme.*

When the chip has been mounted in the CPG-holder inside the chamber the measurement electronics are connected to the appropriate port on the connection socket outside the chamber, according to the connection scheme. The network analyzer gives an AC voltage output, which is connected in series with a DC voltage to the driver electrode. Another DC voltage source is connected to the comb-capacitor V_{dp} in order to polarize V_g to ensure optimal operation of the buffer amplifier. DC voltages of ± 2.5 V_{DC} are applied in order to polarize the buffer amplifier. The out-put of the

circuit is connected to a network analyzer (*HP4194A*) and to an oscilloscope. The oscilloscope is used for fast verification that the CMOS circuitry is working according to the design. If the circuitry is not working properly it is difficult or impossible to polarize the amplifier and this is seen by analyzing the output signal using the oscilloscope. If the circuit is damaged there is often no coupling between the applied polarization voltages and the output voltage V_{out}.

7.4 Single Cantilever CMOS Characterization

As predicted electrical measurements performed on cantilevers without integrated CMOS circuit did not show any appreciable resonance frequency signal, due to the screening effect of the parasitic capacitance introduced by the pads and external wires.

7.4.1 Resonance Frequency

The on-chip resonance frequency response of a low energy EBL defined poly-Si cantilever having a length of 20 µm, a thickness of 600 nm and a width of 420 nm is shown in Fig. 7.4. The resonance frequency was measured at a pressure of 0.4 mbar using an applied peak-to-peak AC voltage of 600 mV_{pp}, a DC voltage of 1 V_{DC}, and a polarization voltage of $V_{dp} = 8V$.

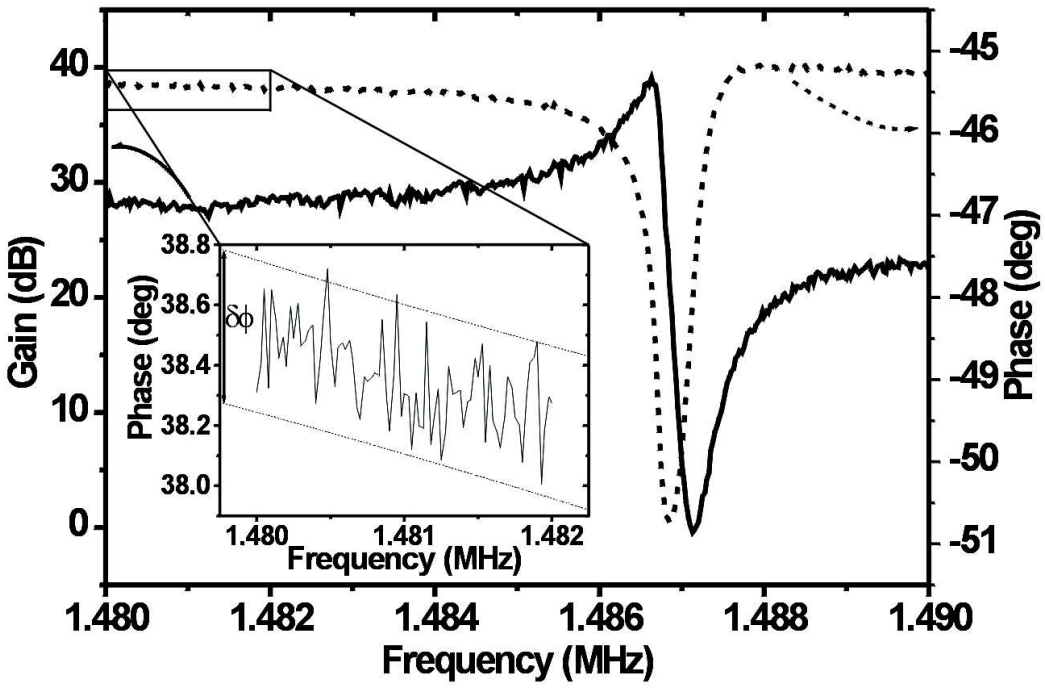

Figure 7.4: *Graph showing the resonance frequency as measured using the integrated CMOS circuitry. The resonance frequency at the pressure of 0.4 mbar, V_{pp} = 600 mV, and V_{DC} = 1 V, is found to be 1.487 MHz.*

The resonance frequency is measured to be approximately 1.487 MHz, which is relatively close to the calculated resonance frequency of $f_0 = 1.491$ MHz using a Young's modulus of $E = 180$ GPa. The resonance curve has the expected shape with a resonance and anti-resonance peak which originates from the presence of the parasitic capacitance in parallel with the cantilever-driver electrode capacitance. The anti-resonance peak, for which the impedance has a maximum, is found a few kHz above the resonance peak.

7.4.2 Spring Softening

The same device has been investigated with respect to the applied DC voltage as shown in Fig. 7.5. As the V_{DC} is increased the resonance frequency reduced. This behavior is supposed to be due to electrostatic spring softening. The reduction of the resonance frequency is caused by the increase of electrostatic force as V_{DC} is increased. The influence of the electrostatic force on the cantilever can be described as a reduction of the effective spring constant of the cantilever, as discussed in Chapter 3.4. The unperturbed resonance frequency of the system is determined by first plotting the resonance frequency as a function of the applied DC voltage squared and then finding the intersection of the linear fit with the y-axis at zero applied voltage. By this method the resonance frequency was determined to be 1.487 MHz.
The Young's modulus of the investigated poly-Si cantilever is calculated using Eq. 7.4-1:

$$E = \frac{16\pi^2 l^2 \rho r_0 f_0^2}{w^2} = 175 \pm 18 \text{ GPa} \tag{7.4-1}$$

in which l=20 μm is the length and w=425 nm is the width of the cantilever, ρ=2.33·10^3 kg/m^3 is the mass density of the poly-Si, $r_0 = 0.2427$ is a geometrical form factor for the fundamental vibration mode originating from the Euler-Bernoulli beam equation, as described in Chapter 3.1. The error is estimated by using $\Delta l = \pm 200$ nm, $\Delta\rho = \pm 1 \cdot 10^{-5}$ g/m3, $\Delta f = \pm 5$ kHz, and $\Delta w = \pm 10$ nm. The calculated Young's modulus is in consistency with measurements on similar poly-Si thin films with E=158±7 GPa [94].

7.4.3 Pressure

The chamber makes it possible to characterize the frequency response, as well as the Q-factor response, as a function of the chamber pressure. Investigation of the resonance frequency behavior at a pressure ranging from $10^1 - 10^5$ Pa was made. The response of the normalized resonance frequency ($\frac{f}{f_0}$) as a function of chamber pressure is displayed in Fig. 7.6.

As the pressure is reduced, the resonance frequency is slightly increased at a constant DC voltage of 9 V_{DC}. This is an effect due to that the effective mass of the cantilever decreases as the amount of gas molecules that moves with the cantilever is reduced

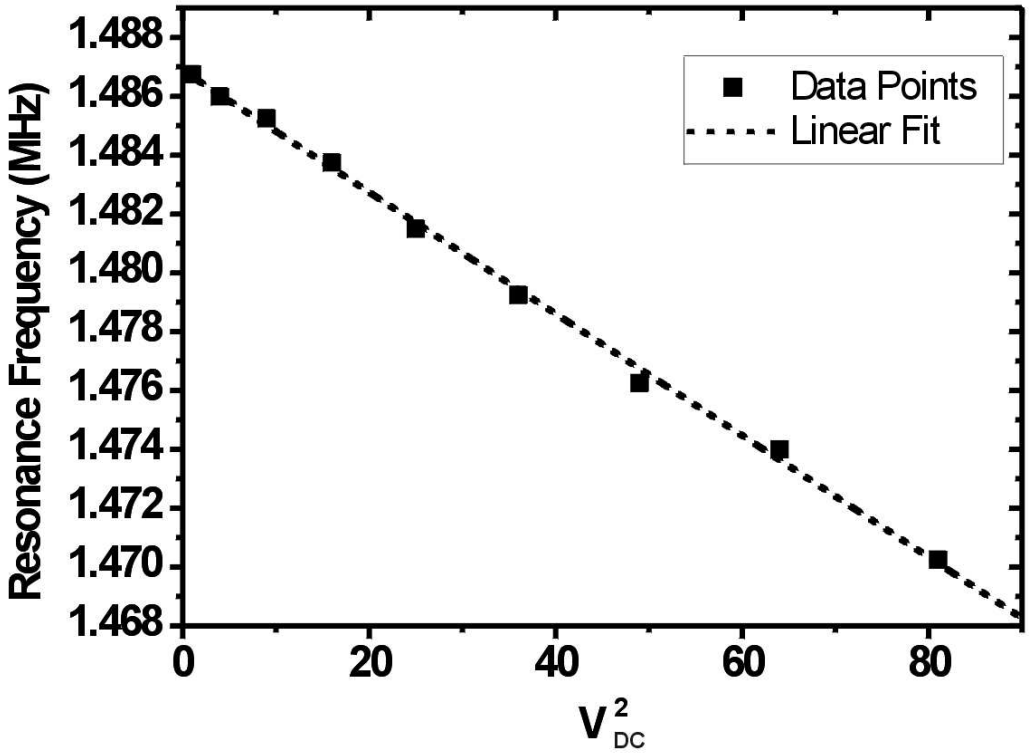

Figure 7.5: *Graph showing the resonance frequency as a function of the applied DC voltage squared. The graph display the effect of spring softening. The unperturbed resonance frequency is found from the intersection with the y-axis, and is found to be 1.487 MHz.*

as a consequence of the reduced pressure. The reason for that the $\frac{f}{f_0}$ ratio does not reach 1 is due to the electrostatic spring softening of the cantilever. An analytical expression of the resonance frequency change as function of pressure is given by J. E. Sader [95]:

$$\frac{f_{n,gas}}{f_{n,vac}} = \frac{1}{\sqrt{1 + \frac{\pi \rho_m t}{4 \rho_c w} \Gamma_r(\mathrm{Re})}} \tag{7.4-2}$$

in which $f_{n,vac}$ is the frequency of the n:th resonance mode in vacuum, $\rho_m = 1.16$ kg/m^3 is the density of the measurement medium (assuming N_2) at room temperature, t is the thickness of the cantilever, ρ_c is the mass density of the cantilever material, and w is the width. The calculated dependence is shown in Fig. 7.6 and display the similar characteristics as the measured frequency dependence. The relative change is twice as large for the measured device compared to the theoretical calculation which might be due to the increased air damping at ambient conditions due to the small separation ($g \leq 1$ µm) between the cantilever and the parallel driver electrode.

Furthermore, investigation of the Q-factor dependence as function of pressure has been made. The Q-factor was estimated by measuring the $\frac{f}{\Delta f_{3dB}}$ from the gain signal.

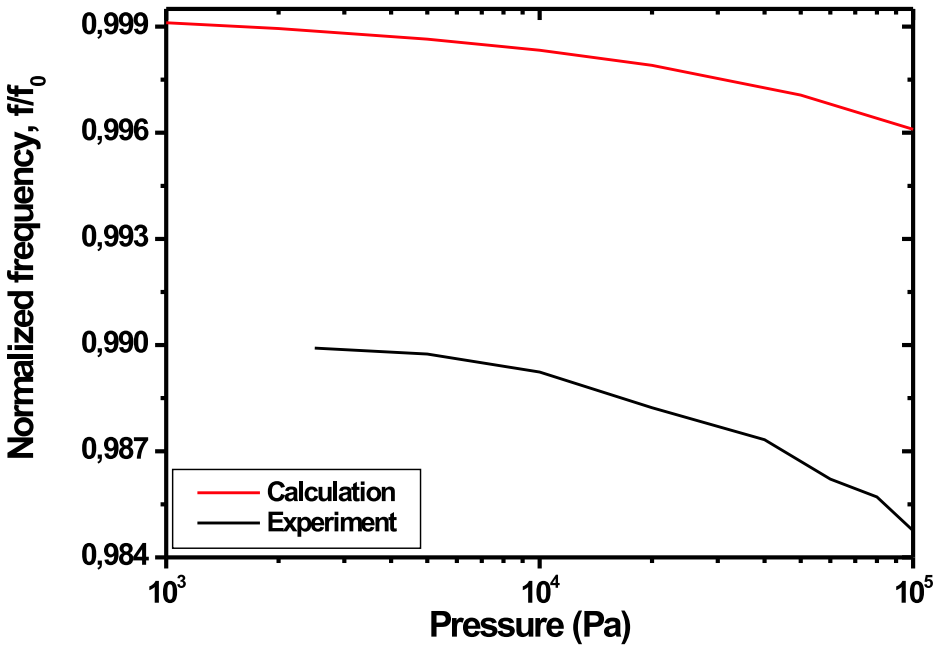

Figure 7.6: *Graph showing the normalized frequency response $\frac{f}{f_0}$ as a function of the pressure.*

The quality factor was measured in the range from $10^1 - 10^5$ Pa and display a log-log dependence as shown in Fig. 7.7.

Given the actuation voltage of 1 V_{DC} and 0.9 V_{pp} a quality factor of approximately 4500 is determined at a pressure of 0.4 mbar. The quality factor is reduced to 30 at ambient air conditions. This is comparable to visual characterization of similar sized, equivalent resonators that were not CMOS integrated. Here, a quality factor of 70 was found for air operation [74] and the value increased to approximately 20000 for operation at a pressure of 10^{-2} Pa [64]. The graph showing the Q-factor as a function of the pressure looks as expected since the pressure is in the regime where external dissipation mechanism are the dominating ones, as discussed in Chapter 3.2. In the pressure regime from $10^1 - 10^3$ Pa the dominating dissipation mechanisms are due to damping caused by individual collisions of gas molecules with the resonator surface, hence called molecular-regime. In the pressure regime $10^3 - 10^5$ Pa the dominating dissipation mechanism is due to viscous friction. The influence of the pressure on the Q-factor is reduced as the pressures comes below 10^1 Pa (below the range of Fig. 7.7) and the dominant dissipation mechanisms below this pressure are the intrinsic.

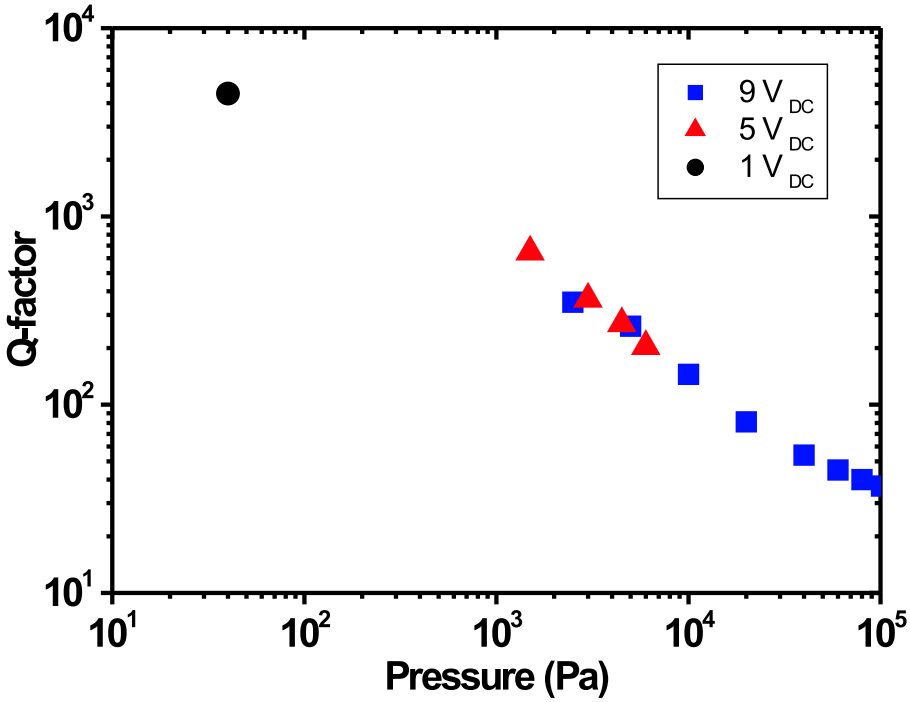

Figure 7.7: *Graph showing the Q-factor as a function of the chamber pressure.*

7.4.4 Gas Composition

In order to investigate the sensitivity towards different gas compositions measurements were performed by changing the chamber gas composition from an air mixture to nitrogen. The end result was that no appreciable change in resonance frequency was noticed, as shown in Fig. 7.8. This was expected since the energy dissipation should be approximately the same comparing nitrogen molecules with the molecules in plain air. However, It would be interesting to compare nitrogen with a heavy noble gas such as Argon or Xenon, for which one should see a reduction of resonance frequency due to the Q-factor reduction as a consequence of molecular dissipation. Such experiments are planned in the near future.

7.5 Cantilever Array CMOS Characterization

In order to investigate the possibility of using cantilever arrays a test batch of arrays with 4 and 8 microcantilevers was integrated with CMOS, as shown in Fig. 7.9. The arrays have been characterized using the same methodology as for the single cantilever chips. The cantilevers are defined in poly-Si by photo lithography. The cantilever

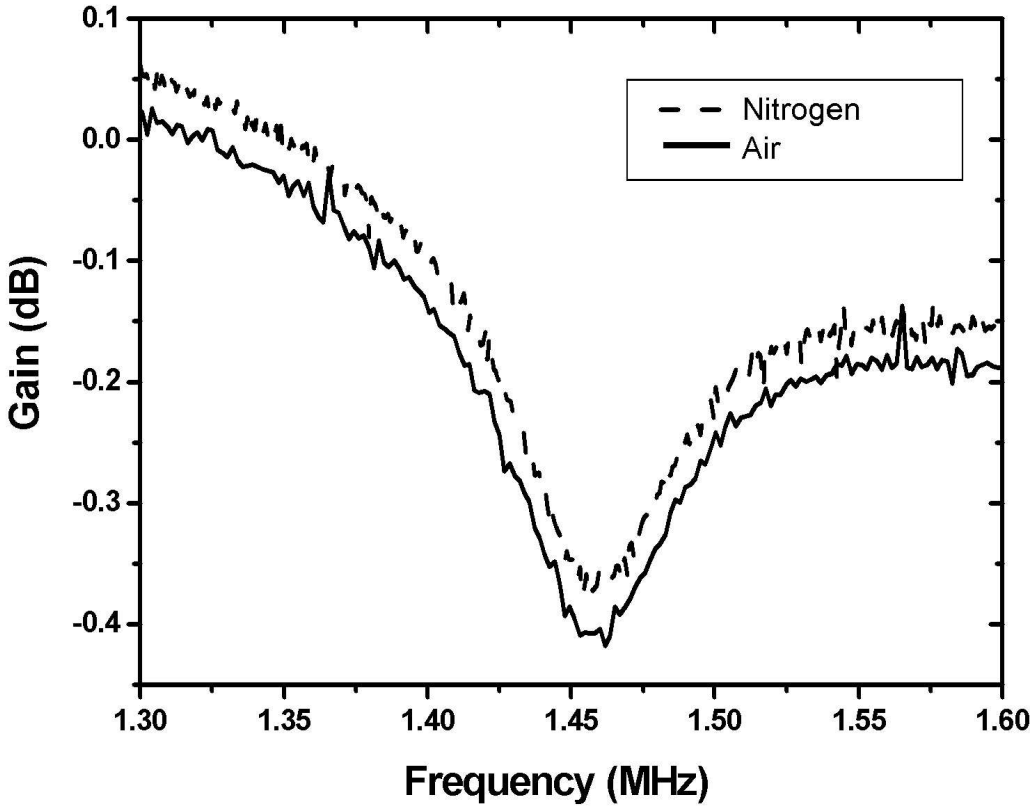

Figure 7.8: *Electrical characterization of the resonance frequency response comparing air and nitrogen at* 10^5 *Pa, using 10* V_{DC} *and 0.8* V_{pp}.

arrays have multiplexed connections between the cantilevers and the read-out circuitry to allow simultaneous measurements of multiple cantilevers. The difference in the CMOS design between the single cantilever chips and the array chips is that a digital module has been incorporated in the array chip circuitry in order to manage the cantilever multiplexing.

7.5.1 Resonance

Using an array of 4 cantilevers simultaneous dual detection of the resonance frequency in air was achieved, as shown in Fig. 7.10.

The resonance frequency is 502 kHz for cantilever nr1 and 513 kHz for cantilever nr2, using 9 V_{ACpp} and 18 V_{DC} at 10^5 Pa. The theoretical resonance frequency using a Young's modulus of 180 GPa is 682 kHz. A single cantilever of an 8-component array has a resonance frequency of approximately 440 kHz using V_{pp}=180 mV and V_{DC}=0.5 V at a pressure of 10^2 Pa, as shown in Fig. 7.11.

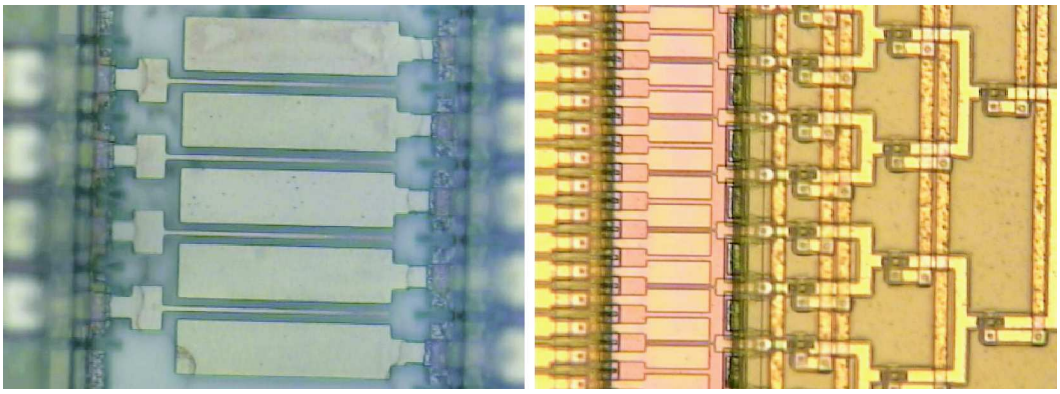

Figure 7.9: *Optical images of 4 respectively 8 cantilevers with independent electrical excitation and detection. The cantilevers in the 4-component array are approximately 50 µm long, 1.2 µm wide, and 600 nm thick.*

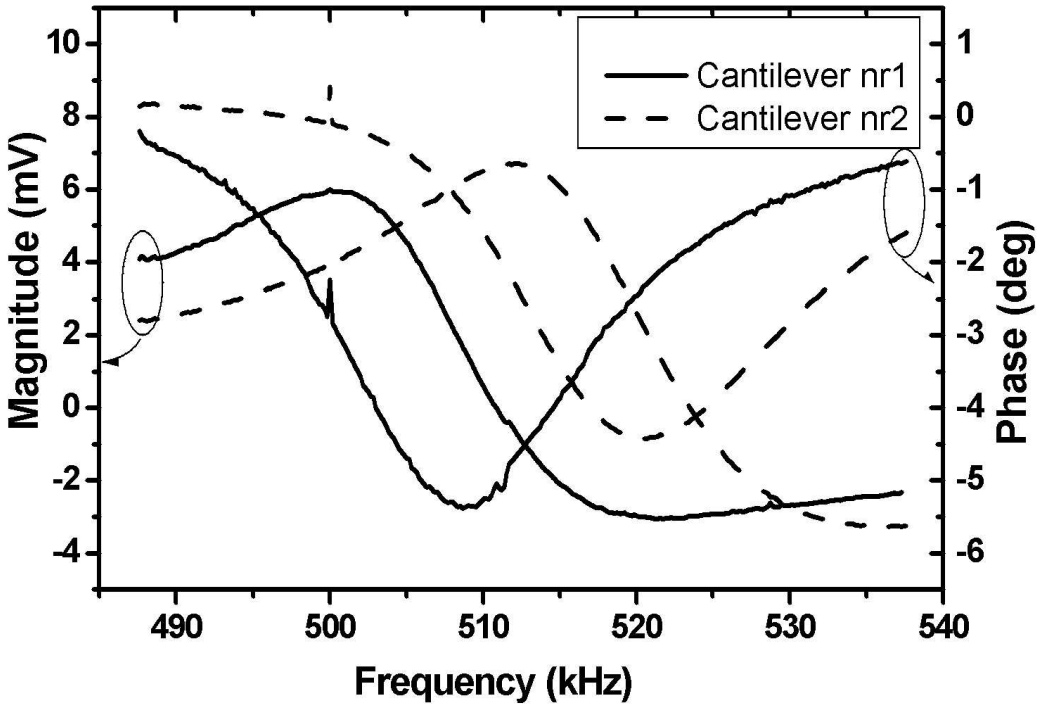

Figure 7.10: *Dual electrical characterization of 2 cantilevers out of a 4-component array in air. The resonance frequency is 501 kHz for cantilever nr1 and 512 kHz for cantilever nr2.*

7.5.2 Pressure

The Q-factor was also determined as function of the chamber pressure and is shown in Fig. 7.12. The Q-factor was estimated by measuring the $\frac{f}{\Delta f_{3dB}}$ from the gain signal. The quality factor was measured in the range from $10^2 - 10^5$ Pa and display a similar dependence as previously shown in Fig. 7.7. The Q-factor for this device

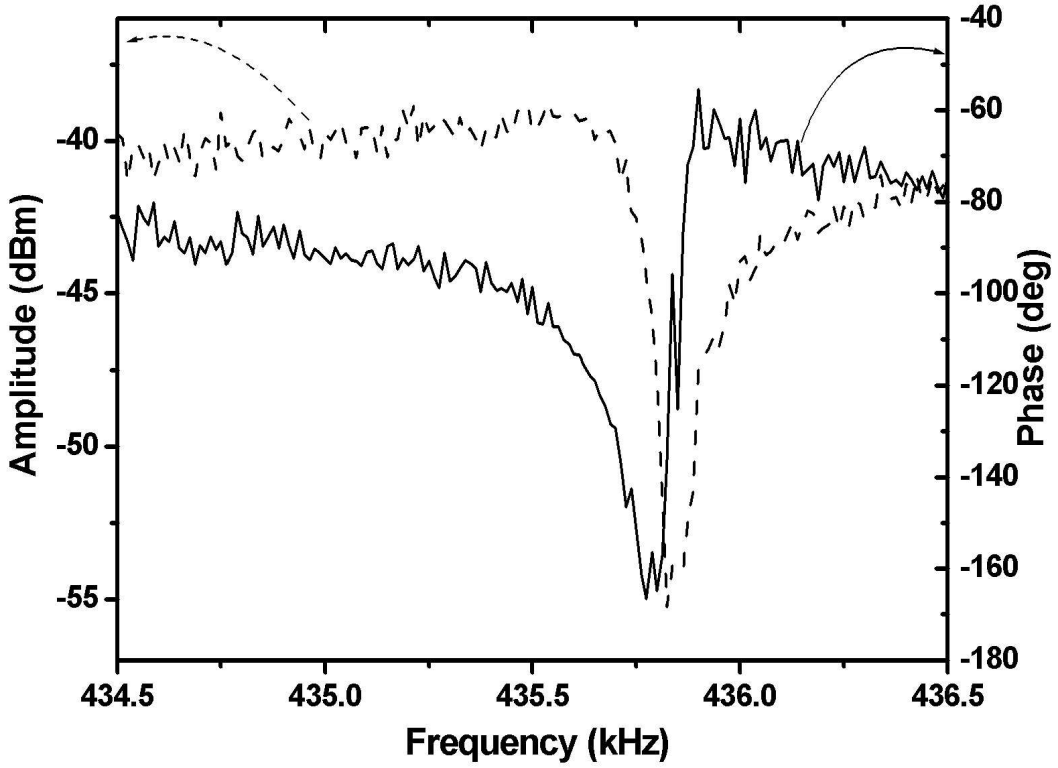

Figure 7.11: *Electrical characterization of one cantilever out of a 8-component array at a pressure of* 10^2 *Pa. The resonance frequency is approximately 440 kHz using* V_{pp}*=180 mV and* V_{DC}*=0.5 V.*

is approximately 4000 at a pressure of $1.5 \cdot 10^2$ Pa. This is in consistency with the measured Q-factor for the single cantilever system.

7.6 Mass sensitivity

In order to characterize the mass sensitivity in air of the resonator device, punctual masses are placed on poly-Si cantilevers that were approximately 20 μm long, 425 nm wide and 600 nm thick.

7.6.1 Latex Bead

This experiment was performed together with S. Dohn at the Department of Micro and Nanotechnology. In the experiment single latex beads having a diameter of 990 nm are placed selectively on the apex of the cantilever using a tungsten tip. The tungsten tip is fabricated by etching a thin tungsten wire by anodic dissolution in a KOH-solution. The final tip typically has a radius of curvature of below 1 μm. The tip is mounted on a piezo-micromanipulator having a precision better than 50 nm. A Si-slide covered with the selected latex beads is mounted on a xyz-stage enabling

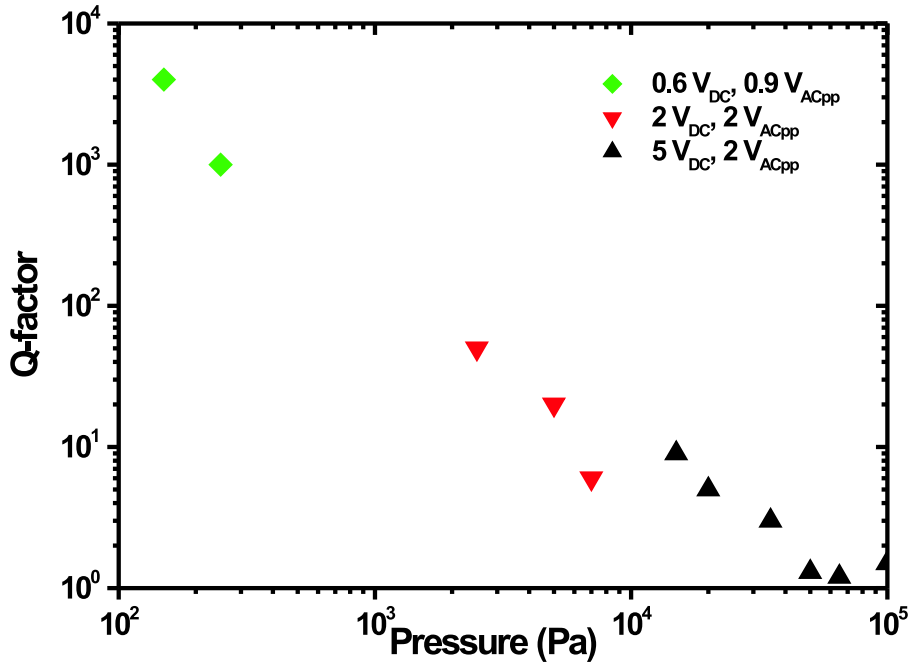

Figure 7.12: *Q-factor dependence as function of pressure for one cantilever in a 8-component array. A Q-factor of approximately 4000 is reached at a pressure of* $1.5 \cdot 10^2$ *Pa.*

positioning with a resolution of 50 nm. The positioning of the tip on the surface is monitored by a Navitar microscope which has a resolution of the order of 20 nm. The tungsten tip collects a latex bead from the Si surface as a potential difference is applied between the tip and the sample surface, after which the Si-slide is replaced by the CMOS chip having the pre-characterized nanoresonator. The tungsten tip with the latex bead is positioned over the selected cantilever and as the bias is removed the latex bead is transferred from the tungsten tip to the resonator.

The change of resonance frequency as a consequence of the deposition of a latex bead on the apex of a poly-Si cantileveris shown in Fig. 7.13.

The resonance frequency was measured using an AC voltage of 6 V_{pp} and a DC voltage of 14 V applied to the approximately 20 µm long, 425 nm wide and 600 nm thick nanoresonator. A resonant frequency of 1.470 MHz is measured at a pressure of 10^3 Pa before the deposition of the latex bead. After the deposition of the latex bead a frequency shift of 36.5 kHz is determined from the shift in amplitude. Using Eq. 7.6-1 as described in Chapter 3.1:

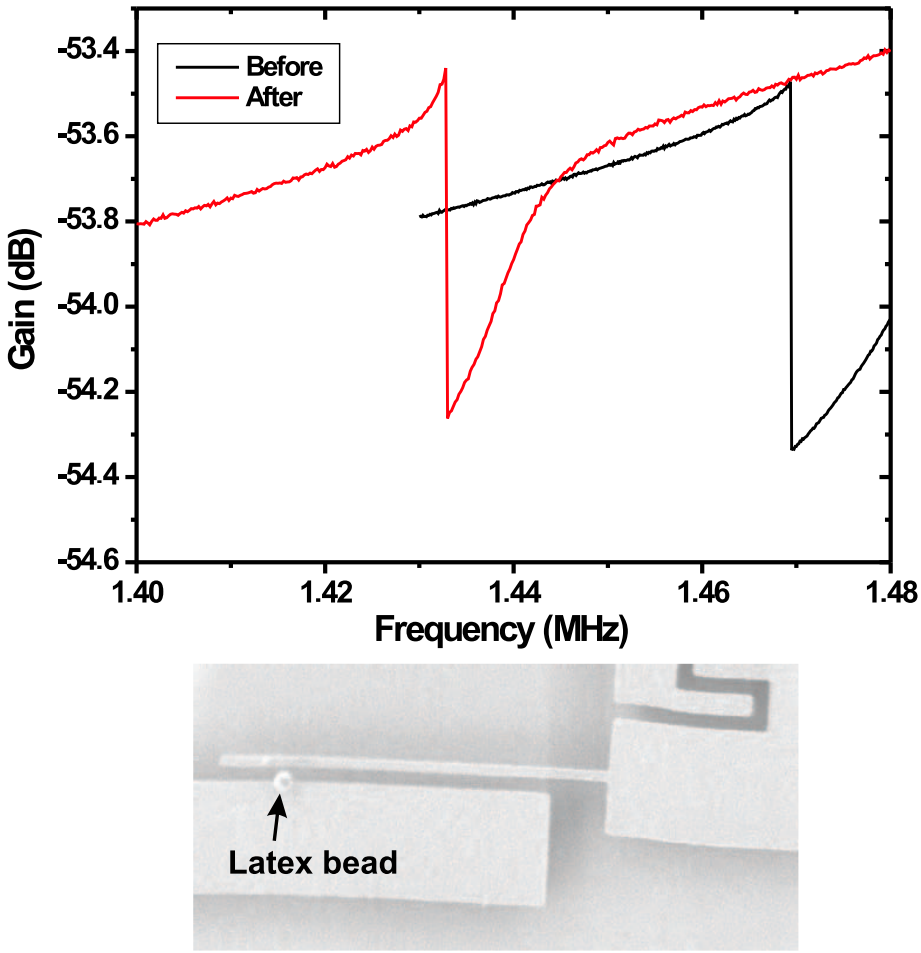

Figure 7.13: *Electrical characterization of the resonance frequency response due to the latex bead deposition at a pressure of Pa, using 10 V_{DC} and 0.8 V_{pp}.*

$$\Delta m = \frac{2m_{eff}\Delta f}{f_0} \tag{7.6-1}$$

where $m_{eff} = n_1 lwt\rho_{Si}$ is the effective mass of the cantilever for the fundamental vibration mode, calculated using a density of poly-Si ρ_{Si}= 2.33·10^6 g/m^3, and a resonance frequency f_0=1.487 MHz, an added mass of 580 fg is calculated. This is close to weight of the latex bead of 540 fg calculated using the specifications given by the manufacturer, ρ_{latex} = 1.06·10^6 g/m^3 and a bead radius r = 495 nm. Hence, the resulting mass sensitivity of the system is of the order of 14 ag/Hz.

The only problem was that as the cantilever with the latex bead was to be imaged in detail using SEM it became apparent that the bead was not positioned on the

cantilever anymore. It is difficult to draw a clear conclusion to the origin of this, but it is possible that the bead jumped to the driver due to charge accumulation as the CMOS chip was irradiated by electrons in the SEM. It was not possible to measure on the structure after the SEM irradiation.

7.6.2 Glycerine Drop

This experiment was performed by Associate Professor G. Abadal at the Department of Electronical Engineering at UAB. In the experiment single glycerine drops are placed selectively on the apex of the cantilever using a glycerine coated tungsten STM-tip. The coating is achieved simply by dipping the tungsten tip in a glycerine solution. The chip with the resonator device is placed on a probe station and the glycerine coated tungsten tip is positioned in close vicinity to the selected cantilever using µm-screws. As the glycerine coated tungsten tip is brought into contact with the cantilever apex a transfer of glycerine to the apex of the cantilever is achieved. The deposited glycerine drop has a diameter of approximately 500 nm, estimated by comparing the drop size with the known width of the cantilever. Assuming a hemispherical volume and ρ_g=1.26·10^3 kg/m^3 the mass of the glycerine drop is estimated to be $41 \cdot 10^{-18}$ kg (or 41 fg).

The resonance frequency is measured using a network analyzer. Figure 7.14 shows the on-chip read-out before and after the positioning of a single glycerine drop at the apex of the resonator. An AC voltage of 6 V_{pp} and a DC voltage of 14 V is applied to an approximately 20 µm long, 425 nm wide and 600 nm thick nanoresonator. A resonant frequency of 1.453 MHz is measured in air before the deposition of the glycerine drop. Directly after the deposition of the glycerine a frequency shift in air of 14.8 kHz is determined from the shift in phase. From the frequency shift an added mass of 57 fg is calculated using Eq. 7.6-1. For the presented system this yields a mass sensitivity of 4 ag/Hz.

7.7 Noise - Ultimate Sensitivity

As discussed in Chapter 3.3, inevitably the ultimate mass resolution is limited by the noise of the NEMS system. In order to get an estimate of the minimal detectable mass, δM, which is the mass change that results in a frequency shift that overcomes the noise floor, an investigation of the phase noise of the system needs to be conducted. The magnitude of the phase noise, caused by both intrinsic and extrinsic noise sources from the transducer and the readout circuitry is shown in Fig. 7.15.
From in Fig. 7.15 the phase noise can be determined to be on the order of 0.5 deg, at a pressure of 0.4 mbar. Since the slope of the phase signal at the frequency of the resonance peak was $\frac{\delta\phi}{\delta f} = -0.108$, the corresponding minimum frequency shift is $\delta f \approx$4.6 Hz. Hence, the minimal detectable mass is calculated as:

$$\delta M = 2m_{eff}\delta f / f_0 \approx 18 \text{ ag}. \tag{7.7-1}$$

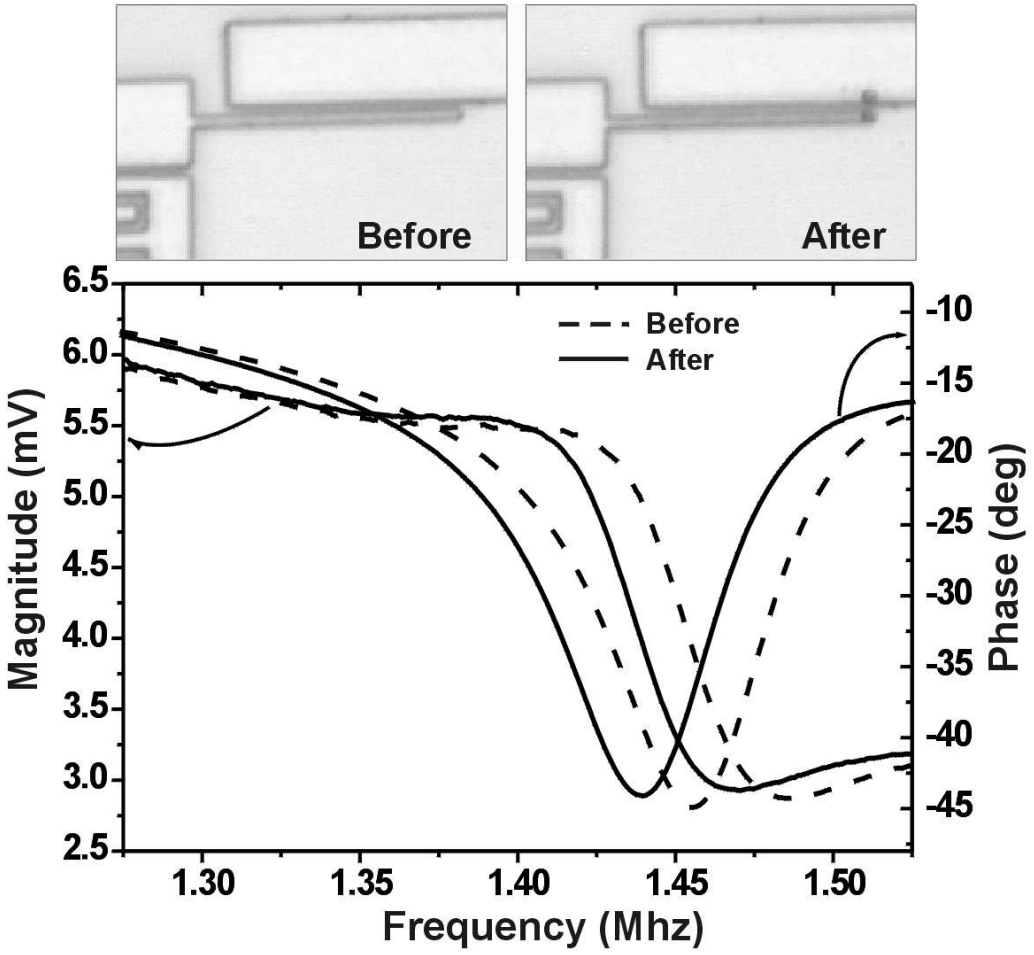

Figure 7.14: *The graph shows the resonance frequency shift after placing a glycerine drop onto the cantilever apex.*

This is in consistency with the experimental work by Ekinci *et al.* [96] regarding noise limitations for nanoresonator mass sensor systems. The phase noise is increased as one increases the pressure, due to the reduced quality factor, thermomechanical noise, and perhaps mainly due to additional drift of the circuit.

At ambient conditions, the minimum frequency shift that can be monitored is of the order of $\delta f \sim 100$ Hz, which corresponds to an ultimate mass resolution in air less than femtograms.

The ultimate resolution for a nanoresonator, equivalent with the single cantilever chip structure, only taking intrinsic thermomechanical noise into account, and excluding extrinsic noise limitations, can be approximated using Eq. 7.7-2. as discussed in Chapter 3.3.

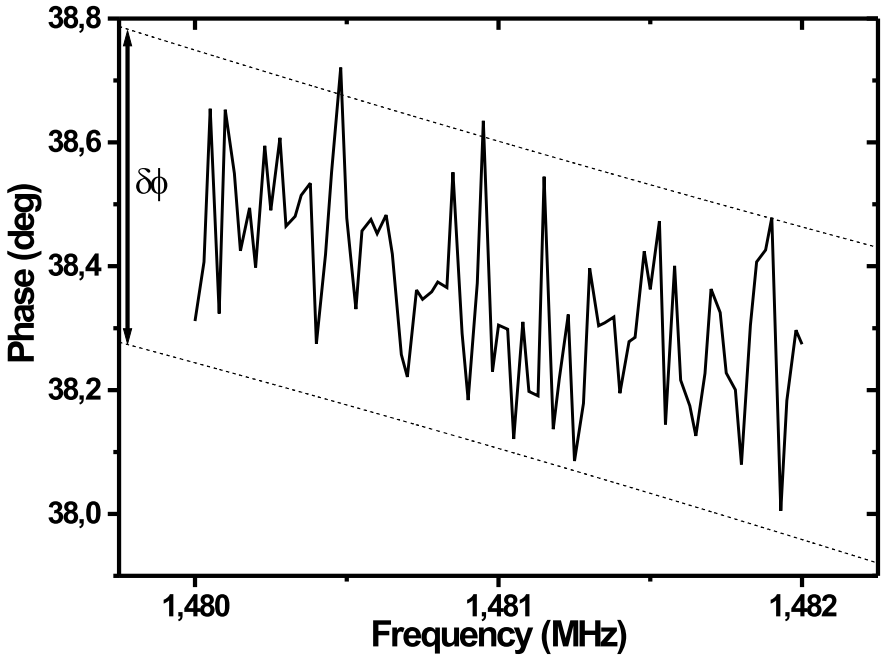

Figure 7.15: *The graph shows fluctuations of the phase of the out-put signal, $\delta\phi \sim 0.5$ deg.*

$$\delta M_{th} \approx 2m_{eff}\sqrt{\frac{k_B T}{E_c}}\sqrt{\frac{\Delta b}{Q\ 2\pi f_0}} \sim 1 \text{ ag} \tag{7.7-2}$$

where $E_T = k_B T$ is the thermal energy at room temperature, $E_c = m_{eff} 4\pi^2 f_0^2 \langle x_c^2 \rangle$ is the driving energy, $\langle x_c^2 \rangle \approx$100 nm is the approximate mean square drive amplitude in the direction of vibration still consistent with producing a linear response, and Δb=1 kHz is the measurement bandwidth.

7.8 Summary

Single cantilever systems and cantilever array systems have been characterized in a gas characterization chamber enabling controlled characterization situation. The Q-factor has been determined to be 30 during operation in ambient air conditions and as the pressure is decreased the Q-factor increases. This is due to the reduced damping by gas molecules. The Q-factor reaches a maximum of 5000 at 10^1 Pa which is at the pressure limit of the vacuum pump connected to the chamber. The Q-factor of the array system is as high as 25000 at the same pressure.

The mass sensitivity has been determined by placing latex beads having a diameter of 1 µm or glycerine drops onto the apex of the cantilever using a etched tungsten tip. The frequency shift due to glycerine adsorption is 14.8 kHz which renders a mass sensitivity of $4 \cdot 10^{-21}$ kg (4 ag).

The ultimate mass sensitivity is limited by noise. Ultimately the only limiting noise is due to intrinsic noise. The mayor source of intrinsic noise if one desires to operate in ambient air conditions is the noise generated by thermomechanical fluctuations. The ultimate sensitivity due to such noise is calculated to be of the order of a single ag (10^{-21} kg) which is of the same order of magnitude as a single medium sized biomolecule such as heme.

Chapter 8

Discussion

The objective of this thesis has been the realization of nanoresonator devices based on electrostatic actuation and capacitive readout integrated with CMOS for high sensitivity mass sensing.

The theory of dynamic cantilever sensing has been discussed and it has been shown that surpassed sensitivity could be achieved by miniaturization of the cantilever dimensions. The effect of the Q-factor and intrinsic and extrinsic noise sources have been discussed.

The principle of electrostatic actuation and capacitive detection and the main constituents of the CMOS circuitry has been presented. The CMOS consists of the CNM CMOS25 technology which is a 2.5 μm technology. The CMOS technique renders constraints on the cantilever design due to that the bandwidth is limited to 1.7 MHz. This restrict the resonance frequency of the cantilever and hence further minimization beyond the dimensions of the cantilever structures demonstrated in this thesis has not been feasible.

Since the cantilever ideally should have a width in the nanometer regime several lithography techniques have been evaluated within the framework of the *Nanomass II* project. Two laser lithography techniques enabling 500 nm linewiths have been developed. One based on local oxidization of 6-10 nm thin Al films and the other based on local laser ablation of a 200 nm polymer film followed by 30 nm Al lift-off. A more advanced nanolithography technique is SFM nanolithography which has been used for the oxidization of 6-10 nm thin Al films achieving linewidths of 20 nm. The technique allows unsurpassed flexibility in the patterning of nanometer structures since direct information on the pattern quality can be gained. The technique is not suitable for patterning on rough surfaces as is the case for standard CMOS. Hence, the throughput is very low on CMOS using the current technology level and the successful patterning of as few as 10 patterns on a CMOS chip can take a few days of processing. The preferred technology is EBL which routinely can pattern structures with a minimum linewidth down to some tenths of nanometers. The only issue has been the CMOS compatibility. It has been found that irradiation damage is drastically reduced as

the acceleration voltage is reduced to below 15 kV. Within this project as low as 4 kV EBL has been performed which has presented new processing problems. The insufficient low energy EBL exposure has been circumvented by using a combination of EBL and DWL-LA.

A process scheme for the post-process fabrication of resonator devices onto pre-processed CMOS has successfully been developed. The process circumvents process induced stiction due to capillary forces by adopting a dry plasma release.

Finally, single cantilever systems as well as cantilever array systems have been characterized in ambient air and in controlled environment using an custom made gas characterization chamber. Q-factors of the order of $10^4 - 10^5$ have been achieved at a pressure of 10^1 Pa. The effect of spring softening due to electrostatic force has been demonstrated. The mass sensitivity has been determined by placing point masses on the apex of the cantilever. Latex beads as well as glycerine drops have been used as point masses and a mass sensitivity of the order of 10^{-21} kg/Hz has been determined. This is of the order of magnitude as the mass of a single medium sized protein, such as heme. For this system an ultimate mass sensitivity δM of the order of 10^{-21} kg has been calculated based on thermomechanical noise. This is the sensitivity one could achieve if one could exclude the extrinsic noise contributions from the CMOS and the measurement equipment. The sensitivity is of the same order of magnitude as presented by other research groups [17][97], even though we measure in ambient air and at room temperature opposed to the others. Furthermore, we have used standard CMOS which leaves plenty of room for performance optimization when using state of the art CMOS foundries. Most importantly the developed fabrication methodology can be directly transferred to such state of the art CMOS, which is what would be necessary if one would commercialize such a system.

The applications of the resonator system which has been presented in this thesis are multiple. The system could be used for characterization and calibration of advanced evaporation systems, such as atom beam lithography systems, molecular beam epitaxy systems, or focused ion beam lithography systems. A collaboration has already been initiated with the objective to integrate a similar device into a nanostencil atom lithography system. A cantilever array system could be used for high sensitivity detection of bio/chemical agents such as volatile compounds, nerve gases, or explosives. Another application is with RF communication for example in the mobile phone industry. A collaboration between UAB and EPSON has been initiated for the development of new electromechanical elements for high frequency telecommunication applications, based on the knowhow gained within the *Nanomass II* project.

To sum up the above it is clear that the initial objective indeed was met. However, in order to further improve the sensitivity and possibly reduce the noise the fabrication of resonator onto SOI-CMOS is to be pursued.The extrinsic noise could be reduced by using a more advanced CMOS. Fabrication results have shown that it is possible to fabricate resonator devices in SOI-CMOS using a similar process as used for the

fabrication of resonators on standard CMOS. However, due to an CMOS design error in the first batch it has not been possible to characterize these systems.

The issue of achieving selectivity during mass sensing is still an open issue and in order to be able to use the system as a true biosensor much effort will be needed within surface functionalization and definition of a test measurement system. A possibility in defining a low throughput test system could be by placing pre-functionalized latex beads on the apex of the cantilever and sense the added mass as complementary molecules bind to the latex bead.

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Chapter 9

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‡ Joint 1^{st} author.

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Chapter 10

"Ultrasensitive mass sensor fully integrated with complementary metal-oxide-semiconductor circuitry"

Ultrasensitive mass sensor fully integrated with complementary metal-oxide-semiconductor circuitry

E. Forsen
Department of Micro and Nanotechnology, Technical University of Denmark, Kgs. Lyngby, DK-2800, Denmark

G. Abadal
Department of Electronic Engineering, Universitat Autonoma de Barcelona, 08193 Bellaterra, Spain

S. Ghatnekar-Nilsson
Solid State Physics and The Nanometer Consortium, University of Lund, 22362 Lund, Sweden

J. Teva and J. Verd
Department of Electronic Engineering, Universitat Autonoma de Barcelona, 08193 Bellaterra, Spain

R. Sandberg and W. Svendsen
Department of Micro and Nanotechnology, Technical University of Denmark, Kgs. Lyngby, DK-2800, Denmark

F. Perez-Murano, J. Esteve, E. Figueras, and F. Campabadal
National Microelectronics Centre, Universitat Autonoma de Barcelona, 08193 Bellaterra, Spain

L. Montelius
Solid State Physics and The Nanometer Consortium, University of Lund, 22362 Lund, Sweden

N. Barniol
Department of Electronic Engineering Universitat Autonoma de Barcelona, 08193 Bellaterra, Spain

A. Boisen
Department of Micro and Nanotechnology, Technical University of Denmark, Kgs. Lyngby, Dk-2800, Denmark

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Nanomechanical resonators have been monolithically integrated on preprocessed complementary metal-oxide-semiconductor (CMOS) chips. Fabricated resonator systems have been designed to have resonance frequencies up to 1.5 MHz. The systems have been characterized in ambient air and vacuum conditions and display ultrasensitive mass detection in air. A mass sensitivity of 4 ag/Hz has been determined in air by placing a single glycerine drop, having a measured weight of 57 fg, at the apex of a cantilever and subsequently measuring a frequency shift of 14.8 kHz. CMOS integration enables electrostatic excitation, capacitive detection, and amplification of the resonance signal directly on the chip. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1999838]

The advances of nanotechnology can be utilized in developing portable sensor systems for applications in biological, physical, or chemical sensing, achieving ultrasensitive detection with low analyte consumption. One approach in developing such a system is to make a nanoresonator device where a change in the mass of the resonator is detected as a change in the resonance frequency of the resonator. In order to achieve the highest possible mass sensitivity, research on fabrication, integration, and development of nanoelectromechanical resonator systems is pursued.[1–3] The most frequently used techniques for measuring the resonance frequency of a cantilever are based on optical detection.[4] The advantage is its inherent simplicity and high sensitivity. Some disadvantages are problems with alignment capability, miniaturization and portability. Resonator systems can be actuated by piezoelectric, magnetic, or thermal actuation.[5–7] Another option is to use electrostatic actuation and capacitive readout. This is achieved by connecting nano/microstructures with standard microelectronics. Previously,[8–11] we have reported on the principle of design and fabrication of cantilever resonators integrated with standard complementary metal-oxide-semiconductor (CMOS) circuitry. CMOS integration enables simple electrostatic actuation, capacitive read-out, and signal amplification. In this letter, we present the functional evaluation of CMOS integrated cantilever structures achieving attogram/Hz mass resolution in air.

The sensing principle is based on monitoring the resonance frequency change of a cantilever as a function of mass adsorption, e.g., due to the adsorption of molecules. The nanoresonator structures are excited into lateral vibration by applying an ac and dc voltage between the suspended cantilever and a fixed parallel electrode. The frequency shift upon added mass is measured on-chip by capacitive resonance frequency detection. CMOS integration reduces the parasitic capacitance contribution and is hence crucial for our choice of cantilever readout. Furthermore, CMOS integration allows for increased functionality in terms of frequency tracking and Q-factor enhancement,[12,13] and can be used as a component in a portable device.

The nanoresonators are defined by combined electron-beam lithography and direct write laser lithography on a preprocessed CMOS chip.[11] Examples of fabricated 425 nm wide, 600 nm thick, and 20 μm long polycrystalline silicon

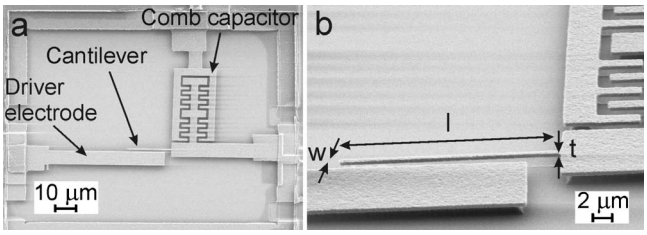

FIG. 1. SEM images of fabricated poly-Si cantilever structures on a CMOS chip. (a) Top view image of a defined cantilever structure. The cantilever is excited into lateral resonance by applying an ac and dc voltage between the driver electrode and the cantilever. The cantilever is connected to a comb capacitor in order to polarize the CMOS circuitry. (b) Tilted view image of a 20 μm long, 425 nm wide, and 600 nm thick cantilever.

(poly-Si) cantilevers, integrated on a CMOS chip, are demonstrated in Fig. 1. We have used standard CMOS technology[14] which leads to cantilever design constraints, limiting the highest detectable resonance frequency to approximately 2 MHz. The on-chip frequency response of such a cantilever, as a function of applied dc voltage (V_{dc}), is measured using a gain-phase analyzer, see Fig. 2(a). The resonance frequency is reduced when the V_{dc} is increased, due to electrostatic spring softening.[15] The unperturbed resonance frequency of the system is determined to be $f_0 = 1.487$ MHz from the intersection of the linear fit with the y axis at zero-applied voltage, Fig. 2(b). Electrical measurements performed on equivalent cantilevers without an integrated CMOS circuit did not show any appreciable resonance frequency signal, due to the screening effect of the parasitic capacitance introduced by the pads and external wires. The Young's modulus of the poly-Si cantilever is calculated using Eq. (1) to have a value of $E = 175 \pm 18$ GPa (Ref. 16)

$$E = \frac{16\pi^2 \ell^4 \rho n_1 f_0^2}{w^2}, \tag{1}$$

in which $\ell = 20$ μm is the length and $w = 425$ nm is the width of the cantilever, $\rho = 2.33 \times 10^6$ g/m^3 is the mass density of the poly-Si, $n_1 \cong 0.2427$ is a geometrical form factor for the fundamental vibration mode originating from the Euler–Bernoulli beam equation.[17] The calculated Young's modulus is consistent with measurements on similar poly-Si thin films with $E = 158 \pm 7$ GPa.[18]

Resonator structures have been characterized in a chamber in which the pressure has been controlled in the range of 1013 mbar–0.1 mbar. The quality factor as a function of the pressure displays a log-log dependence, as shown in Fig. 2(c). Given a dc+ac actuation voltage of 1 V_{dc} and 0.9 V peak-peak (V_{PP}), a quality factor of approximately 5000 is determined at a pressure of 0.4 mbar. The quality factor is reduced to 30 at ambient air conditions. This is comparable to previous visual characterization of similar sized equivalent resonators that have not been CMOS integrated. Here, a quality factor of 70 was found for air operation[14] and the value increased to 28 000 for operation at a pressure of 2 μbar.[8]

In order to characterize the mass sensitivity of the resonator device in air, punctual masses are placed on the cantilever. Single glycerine drops are placed selectively on the apex of the cantilever using a glycerine coated scanning tunneling microscope (STM) tip. The deposited glycerine drop has a diameter of approximately 500 nm, estimated by comparing the drop size with the known width of the cantilever. Assuming a hemispherical volume and $\rho = 1.26 \times 10^6$ g/m^3, the mass of the glycerine drop is estimated to be 41 fg. Figure 3 shows the on-chip readout before and after the controlled positioning of a single glycerine drop at the apex of the resonator. An ac voltage of 6 V_{pp} and a dc voltage of 14 V is applied to a 20 μm long, 425 nm wide, and 600 nm thick nanoresonator, similar to the resonator shown in Fig. 1(c). A resonant frequency of 1.453 MHz is measured before the deposition of the glycerine drop. Directly after the deposition of the glycerine, a frequency shift in air of $\Delta f = 14.8$ kHz is determined from the shift in phase. From the frequency shift, an added mass of 57 fg is calculated using Eq. (2)[19]

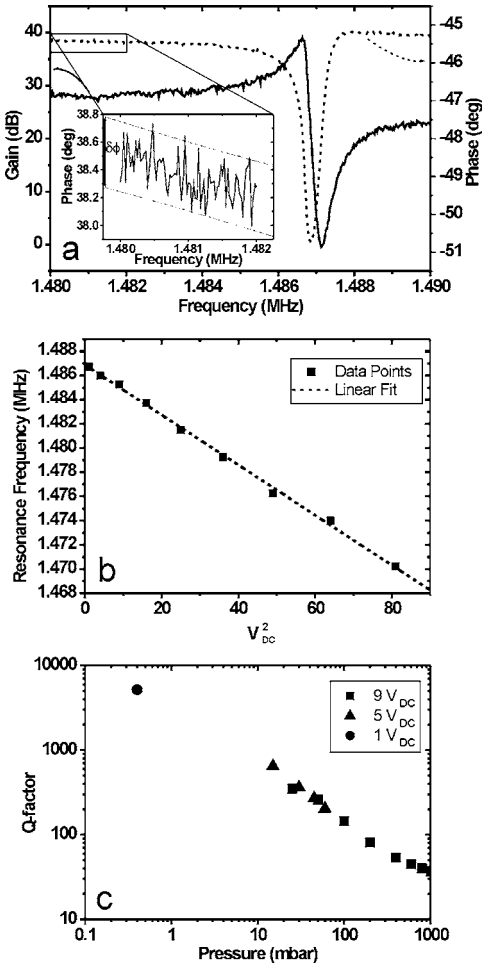

FIG. 2. (a) On-chip readout using a poly-Si cantilever with a width of 425 nm, a thickness of 600 nm and a length of 20 μm, at a pressure of 0.4 mbar. The frequency signal from the CMOS circuitry was analyzed using a gain-phase analyzer. The inset shows the fluctuation of the phase signal ($\delta\phi \approx 0.5°$). (b) The effect of electrostatic spring softening is shown. The unperturbed resonance frequency of the system is determined from the intersection of the linear fit at zero-applied dc voltage. The fundamental resonance frequency is 1.487 MHz. (c) The quality factor dependence on the pressure displays a log-log relationship. A quality factor of approximately 5000 is determined at 0.4 mbar and 1 V_{dc} and 0.9 V_{PP}.

$$\Delta m = \frac{2 m_{\text{eff}} \Delta f}{f_0}, \tag{2}$$

where $m_{\text{eff}} = n_1 \rho \ell w t$ is the effective mass of the cantilever for the fundamental vibration mode, calculated using a density of poly-Si $\rho = 2.33 \times 10^6$ g/m^3, and a resonance frequency

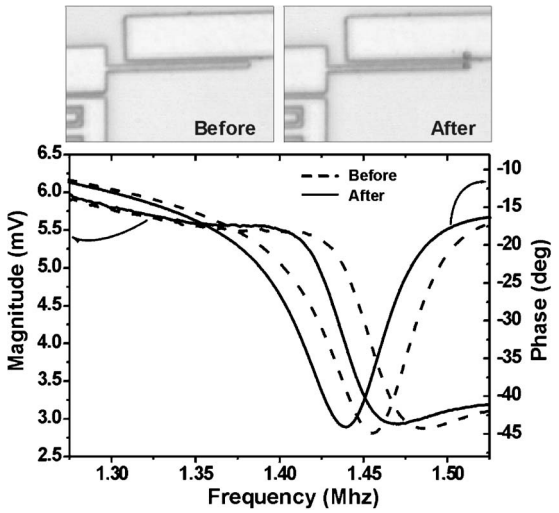

FIG. 3. The diagram shows the electrical resonance signal for a poly-Si resonator structure as measured through the CMOS. At ambient conditions, the resonance frequency was 1.453 MHz. The cantilever is 20 μm long, 425 nm wide, and 600 nm thick. The cantilever is excited into resonance by applying 14 V_{dc} and 6 V_{PP} ac. The inset shows two glycerine droplets, one at the apex of the cantilever and the other is on the parallel actuation electrode. This is due to the fact that the glycerine-coated STM-tip touched the electrode on the first approach, resulting in a glycerine drop on the electrode. After deposition of a single glycerine drop onto the cantilever, the resonance frequency was reduced by 14.8 kHz, which yields a mass sensitivity on the order of 4 ag/Hz at ambient conditions.

$f_0 = 1.487$ MHz. Hence, the calculated mass sensitivity of the system is 4 ± 1 ag/Hz.

Inevitably, the ultimate mass resolution is limited by the noise of the system. In order to get an estimate of the minimal detectable mass, δM, which is the mass change that results in a frequency shift that overcomes the noise floor, an investigation of the phase noise of the system needs to be conducted. From the inset in Fig. 2(a), the magnitude of the phase noise—caused by both intrinsic and extrinsic noise sources from the transducer and the readout circuitry—can be determined to be of the order of $\delta\phi \approx 0.5°$ at a pressure of 0.4 mbar. Since the slope of the phase signal at the frequency of the resonance peak was $\partial\phi/\partial f = -0.108$, the corresponding minimum frequency shift is $\delta f \approx 4.6$ Hz. Hence, the minimal detectable mass is calculated as $\delta M_{\text{noise}} = 2m_{\text{eff}}\delta f/f_0 \approx 18$ ag. The ultimate resolution for a nanoresonator, equivalent with the one presented in this letter, only taking intrinsic phase noise into account and excluding extrinsic noise limitations can be approximated using Eq. (3):[19]

$$\delta M_{\text{intrinsic}} = 2m_{\text{eff}}\sqrt{E_T/E_c}\sqrt{\Delta f/Q2\pi f_0} \approx 1 \text{ ag}, \tag{3}$$

where $E_T = k_B T$ is the thermal energy at room temperature, $E_c = m_{\text{eff}} 4\pi^2 f_0^2 \langle x_c^2 \rangle$ is the driving energy, $\langle x_c \rangle \approx 100$ nm is the approximate root-mean-square drive amplitude in the direction of vibration still consistent with producing a linear response, and $\Delta f = 1$ kHz is the measurement bandwidth. This is consistent with the theoretical/experimental work by Ekinci *et al.*[4,19] regarding noise limitations for nanoresonator mass sensor systems.

The phase noise is increased as one increases the pressure, mainly due to the reduced quality factor but also adsorption/desorption processes on the cantilever and additional drift of the circuit are limiting factors. At ambient conditions, the minimum frequency shift that can be monitored is of the order of $\delta f \approx 1$ kHz, which corresponds to an ultimate mass resolution in air of the order of a few femtograms.

In conclusion, the characterization of a fully integrated resonator mass sensor system in air and at low pressure conditions has been discussed. CMOS integrated cantilevers have been electrostatically excited into mechanical resonance and the resonance frequency has been detected on-chip by capacitive readout. The mass sensitivity of the system has been determined by controlled positioning of glycerine drops on a cantilever, whereby a mass sensitivity of the order of 4 ag/Hz is measured for a resonator system with a fundamental resonance frequency of 1.487 MHz. At 0.4 mbar, the quality factor is determined to be approximately 5000. The sensitivity of the system is comparable to recent results achieved with resonator structures based on external actuation and readout.[4,20] Nanoresonator devices should be functionalized in order to enable selective mass sensing. The ultimate goal is to develop nanoresonator devices as integral parts of a portable sensor system.

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Chapter 11

"Design, fabrication, and characterization of a submicrometerelectromechanical resonator with monolithically integrated CMOS readout circuitry"

Design, Fabrication, and Characterization of a Submicroelectromechanical Resonator With Monolithically Integrated CMOS Readout Circuit

Jaume Verd, *Student Member, IEEE*, G. Abadal, J. Teva, María Villarroya Gaudó, Arantxa Uranga, Xavier Borrisé, Francesca Campabadal, Jaume Esteve, Eduardo Figueras Costa, Francesc Pérez-Murano, *Member, IEEE*, Zachary J. Davis, Esko Forsén, Anja Boisen, and Nuria Barniol, *Member, IEEE*

***Abstract*—In this paper, we report on the main aspects of the design, fabrication, and performance of a microelectromechanical system constituted by a mechanical submicrometer scale resonator (cantilever) and the readout circuitry used for monitoring its oscillation through the detection of the capacitive current. The CMOS circuitry is monolithically integrated with the mechanical resonator by a technology that allows the combination of standard CMOS processes and novel nanofabrication methods. The integrated system constitutes an example of a submicroelectromechanical system to be used as a cantilever-based mass sensor with both a high sensitivity and a high spatial resolution (on the order of 10^{-18} g and 300 nm, respectively). Experimental results on the electrical characterization of the resonance curve of the cantilever through the integrated CMOS readout circuit are shown. [1318]**

***Index Terms*—Capacitive transducers, CMOS analog integrated circuits, microelectromechanical devices, nanotechnology.**

I. Introduction

EXAMPLES of microelectromechanical systems include sensors for detecting different kinds of physical or chemical properties [1]. A reduction of the dimensions of the mechanical transducer leads to a new generation of systems called nanoelectromechanical systems (NEMS) [2]–[5] that represent an improvement on sensitivity, spatial resolution, energy efficiency and response time. As an example of NEMS, we present the design of a mass sensor based on a laterally oscillating cantilever with nanometer-scale dimensions, which has both a high sensitivity and a high spatial resolution (down to the range of 10^{-18} g and 300 nm, respectively). Mass detection is based on monitoring the resonant frequency shift of the cantilever when nanometer-sized particles or molecules are deposited on the cantilever [6], [7].

The cantilever is electrostatically excited by means of a driver electrode. A change in the cantilever resonance frequency is detected as a capacitance change. Electrostatic transduction in the nanometer-size regime requires the minimization of the parasitic capacitance since the magnitude of the current to be detected is proportional to the coupling capacitance between the cantilever and the driver, which is in the order of 10^{-17} F. Consequently, the readout circuitry has to be integrated "on-chip" along with the mechanical transducer in order to eliminate the parasitic capacitance introduced by the external bonding pads and wires. CMOS circuitry for excitation and read-out of the cantilever deflection is integrated together with the cantilever by using a monolithic technology that consists of the combination of standard CMOS processes and novel nanofabrication methods.

For demonstration purposes, in the present paper we have used a CMOS technology (2.5 μm, two metal and two polysilicon layers) that allows such combination [8]. The integration of the cantilever, the excitation system and the readout circuitry on the same chip provides us with a smart sensor system (see Fig. 1) which will permit detection of the deposited mass with *in situ* added functionalities like for example automatic tracking of the resonance frequency.

Although the principle of operation of this smart sensor is very simple, its practical realization requires carefully addressing of several issues that arise from the combination of nanometer scale devices and microelectronic circuits. In this work, we present the main aspects of the sensor modeling (Section II), circuit design (Section III), and system fabrication (Section IV) that have allowed the successful electrical characterization of the first prototypes, as it is shown in Section V.

II. Sensor Principle and Modelization

The two main cantilever parameters: i) spring constant k, and ii) the fundamental resonance frequency f_o can be calculated according to the dimensions of the resonant structure and the mechanical properties of the material (Young modulus E and mass density ρ) [9]

$$k = \frac{E}{4}\frac{w^3}{l^3}t \quad (\mathrm{N/m}) \tag{1}$$

$$f_o = \frac{1}{2\pi}\sqrt{\frac{E}{\rho}}\frac{w}{l^2} \quad (\mathrm{Hz}) \tag{2}$$

where w, l, and t are, respectively, the width, length, and thickness of the lateral oscillating cantilever (see Fig. 1). Approxi-

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J. Verd, G. Abadal, J. Teva, M. Villarroya Gaudó, A. Uranga, and N. Barniol are with the Department of Enginyeria Electrònica, Universitat Autònoma de Barcelona, E-08193 Bellaterra, Spain (e-mail: Gabriel.Abadal@uab.es).

X. Borrisé, F. Campabadal, J. Esteve, E. Figueras Costa, and F. Pérez-Murano are with the Institut de Microelectrònica de Barcelona (IMB-CNM-CSIC), E-08193 Bellaterra, Spain (e-mail: Francesc.Perez@cnm.es).

Z. J. Davis, E. Forsén, and A. Boisen are with the Mikroelektronik Centret, Denmark Technical University, 2800 Lyngby, Denmark .

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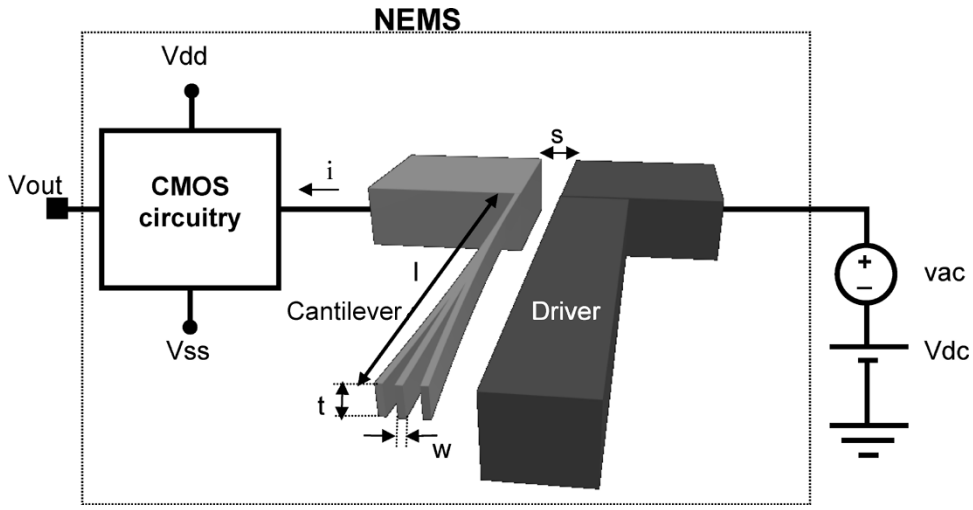

Fig. 1. Schematic drawing of the NEMS system based on a laterally vibrating cantilever (s direction) electrostatically excited and with capacitive readout. The structural layer for the cantilever is one of the polysilicon layers used in CMOS technology.

mating the cantilever tip displacement by a mass-spring model, the resonance frequency can be expressed as

$$f_o = \frac{1}{2\pi}\sqrt{\frac{k}{m_{eff}}} \quad \text{(Hz)} \tag{3}$$

where m_{eff} is the effective mass of the cantilever, $m_{\text{eff}} = 0.24\rho wlt$ (kg) [9].

The resonance frequency of the cantilever will change when a mass is deposited. The dependence of the mass change (δm) on the resonance frequency shift (δf) is expressed in (4). This equation assumes that the extra mass is added at the tip of the cantilever, producing no change in the spring constant, but only a shift in its resonance frequency [6].

$$\delta m = \frac{k}{4\pi^2}\left[\frac{1}{(f_o - \delta f)^2} - \frac{1}{f_o^2}\right] \quad \text{(kg)}. \tag{4}$$

A linear approximation of the previous equation around the resonance frequency, leads to a simpler expression for the mass sensor sensitivity

$$\frac{\delta m}{\delta f} = \frac{1}{2\pi^2}\frac{k}{f_o^3} \quad \text{(kg/Hz)}. \tag{5}$$

Using (1) and (2) and assuming a poly-Si cantilever ($E = 160$ GPa and $\rho = 2330\ \text{kg/m}^3$), (5) can be written as

$$\frac{\delta m}{\delta f} \cong 0.9 l^3 t \quad \text{(kg/Hz)} \tag{6}$$

which implies that a theoretical mass sensitivity of 34.4 ag/Hz can be obtained with a cantilever of $l = 40\ \mu\text{m}$ and $t = 600\ \text{nm}$. Note that under this approximation, the sensitivity does not depend on the width of the cantilever.

Electrostatic transduction of the cantilever is accomplished by electrical force actuation and capacitive readout (see Fig. 1). An ac voltage is applied to a driver electrode, which is placed close and parallel to the cantilever, resulting in an electrostatic force that drives the cantilever oscillation. The capacitive readout consists of detecting the electrical current, i.e., the displacement current, which is induced by the change of the capacitance between the cantilever and the driver electrode as a consequence of the change of the spacing when the cantilever oscillates. In order to detect this displacement current, an additional dc voltage must be applied (see Section III). The parasitic capacitance must be reduced as much as possible, and because of this a CMOS circuit must be integrated together with the cantilever/driver system.

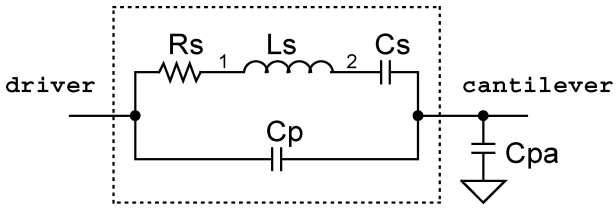

Fig. 2. Small-signal electromechanical model of the oscillating cantilever-driver system based on passive elements.

An electrical model of the sensor is required to address the CMOS circuit design. For this purpose, a simple linear electromechanical model has been used [6]. This model makes it possible to derive the electrical requirements for the CMOS circuitry, as for example capacitive current levels at the resonance frequency I_{res} and dc and ac voltages for excitation and measurements.

The linear small-signal electromechanical model based on passive elements is shown in Fig. 2. The static capacitance of the cantilever-driver system C_p increases when a dc voltage V_{dc} is applied

$$C_p = C_o(1+\kappa) \quad \text{(F)} \tag{7}$$

$$C_o = \varepsilon\frac{l\cdot t}{s} \quad \text{(F)} \tag{8}$$

where ε is the vacuum dielectric constant, s is the gap between cantilever and driver, and κ is the so-called electromechanical coupling parameter, which is calculated from

$$\kappa = \frac{\varepsilon}{2\cdot k}\frac{l\cdot t}{s^3}V_{\text{dc}}^2. \tag{9}$$

The series $R_s\ L_s\ C_s$ branch of the equivalent circuit describes the resonance behavior according to [6]

$$C_s = 1.789\cdot\kappa\cdot C_o \quad \text{(F)} \tag{10}$$

TABLE I
ELECTRICAL PARAMETERS FOR DIFFERENT NANOCANTILEVER LENGTHS, width = gap = 1 μm AND thickness = 600 nm AND ASSUMING POLYSILICON AS THE STRUCTURAL LAYER (E = 160 Gpa AND ρ = 2330 kg/m^3). AN EXPECTED QUALITY FACTOR FOR THE CANTILEVER-DRIVER SYSTEM IN AIR, Q = 50, HAS BEEN CONSIDERED FOR THE CALCULATION

Length (μm)	20	30	40	50
k (N/m)	3400	1	0.42	0.22
f_{res} (MHz)	3.55	1.58	0.89	0.58
V_{si} (V)	97	43	24	16
V_{DCopt} (V)	85	38	21	14
V_{ACopt} (V)	9.4	4.2	2.4	1.5
Cs (aF)	21.7	32.6	43.5	54.4
Cp (fF)	0.183	0.177	0.237	0.296
Ls (H)	92.4	312	740	1440
Rs (MΩ)	41.2	61.9	82.5	103
I_{res} (nA)	206	61.0	25.7	13.2

$$L_s = \frac{1}{2\pi \cdot C_s \cdot f_{\text{res}}} \quad \text{(H)} \tag{11}$$

$$R_s = \frac{1}{Q}\sqrt{\frac{L_s}{C_s}} \quad (\Omega). \tag{12}$$

In this model, the quality factor Q and C_{pa} are both empirical parameters. C_{pa} is an additional parasitic capacitance. It accounts for the parasitic capacitance associated with the connection lines between the cantilever and the circuit as well as the input capacitance of the amplifier.

In Table I, electrical parameters as a function of cantilever length are listed. $V_{\text{pull-in}}$ represents the minimum voltage that causes the cantilever to collapse onto the driver electrode. V_{dcopt} and V_{acopt} are the optimal voltages applied to the driver electrode, which are used to calculate the values of the elements in the small-signal model. These optimal voltages are calculated from a total optimal voltage, V_{opt}, which is obtained as a fraction of the pull-in voltage [6]. Under these conditions, pull-in is avoided and the linearity regime of the oscillations is ensured. An expected quality factor for the cantilever-driver system in air, $Q = 50$, has been considered for these calculations. This Q factor has been obtained from an optical characterization of the oscillation of several integrated cantilevers [7]. Values for the parameters that correspond to a 40-μm-long cantilever have been used for the design of the CMOS read-out circuits (Table I). With these dimensions, C_p is as low as 0.236 fF and the expected current at the resonance frequency (887 kHz) is 25.7 nA when applying a dc voltage of 21.3 V and an ac voltage amplitude of 2.4 V. Note the large value of the equivalent motional resistance (R_s), which causes a low value of the amplitude current at the resonance frequency, unlike other types of mechanical structures where an off-chip detection system is possible [10], [11]

III. CMOS CIRCUIT DESIGN

The purpose of the readout circuitry is to detect and amplify the capacitive current generated in the driver-cantilever interface, which is a measure of the oscillation amplitude of the cantilever. This current follows (13) where C represents the cantilever-driver capacitance composed by a static capacitance C_p plus a time variable component c that reflects the capacitance variations due to the movement of the cantilever.

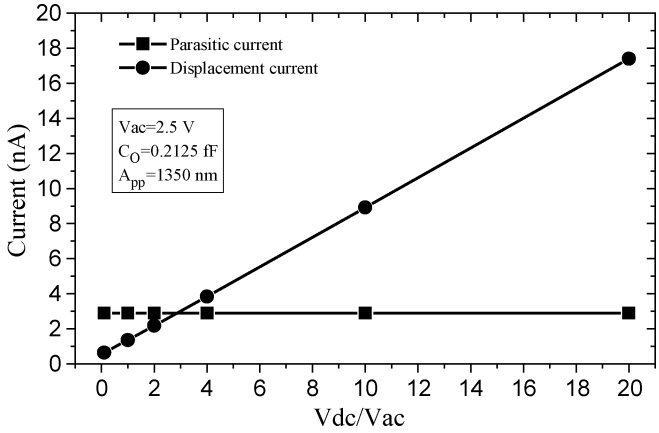

Fig. 3. Displacement and parasitic current amplitudes generated by the cantilever-driver system versus the ratio between the dc and ac applied voltages. Cantilever dimensions: l = 40 μm, s = 1 μm, w = 840 nm and t = 600 nm. The assumed oscillating amplitude (675 nm) corresponds to experimental data when the cantilever is at its resonance. The left hand portion of the figure (when Vdc<Vac) violates the assumption made for calculating the current, but it is shown here for completeness.

$$\begin{aligned} I_C(t) &= \frac{\partial}{\partial t}(C \cdot V) \\ &= (C_p + c)\frac{\partial V_{\text{ac}}}{\partial t} + (V_{\text{dc}} + V_{\text{ac}})\frac{\partial c}{\partial t} \\ &\approx C_p \frac{\partial V_{\text{ac}}}{\partial t} + V_{\text{dc}}\frac{\partial c}{\partial t} \\ &= I_p + I_d. \end{aligned} \tag{13}$$

The first term of this equation is a parasitic current (I_p) since it does not reflect the movement of the cantilever and it is generated due to the ac voltage that it is applied for excitation of the cantilever. The second term, called displacement current (I_d), reflects the oscillation of the cantilever since it depends on the variations of the driver-cantilever capacitance.

Assuming that the tip of the cantilever oscillates according to an harmonic movement $z(t)$ since it is excited electrostatically by means of an ac voltage signal at a frequency ω, we can found the analytic expressions for the cantilever-driver capacitance (14) and its time derivative (15).

$$C(t) = C_p + c = \frac{\varepsilon_o l t}{s_o - z(t)} \quad \text{with} \quad z(t) = A_{eff}\sin(\omega t) \tag{14}$$

$$\frac{\partial C}{\partial t} = \frac{\partial C}{\partial z}\frac{\partial z}{\partial t} = \frac{\varepsilon_o l t}{(s_o - z(t))^2} A_{\text{eff}}\omega\cos(\omega t). \tag{15}$$

The parameter A_{eff} is the effective displacement of the cantilever assuming parallel displacement with respect to the driver. This parameter is calculated from the real amplitude oscillation of the cantilever tip according to $A_{\text{eff}} = 0.39$ A, which takes into account that the cantilever deflection is not exactly linear [12].

From the last expressions, we can evaluate when the displacement current is dominant. Fig. 3 shows the amplitude of the displacement and parasitic currents versus $V_{\text{dc}}/V_{\text{ac}}$, when a cantilever oscillation amplitude of 675 nm is assumed (the gap between cantilever and driver is around 1 μm). The use of high

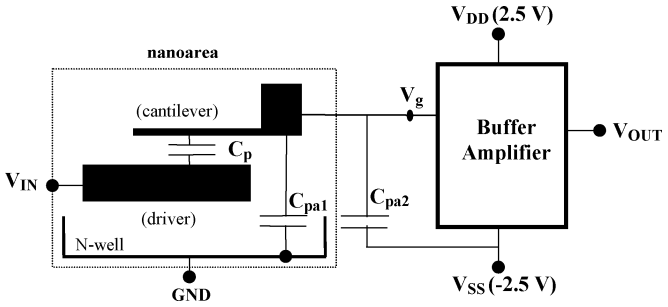

Fig. 4. Diagram of the capacitive read-out method used to detect the capacitive current generated in the driver-cantilever interface. The parasitic capacitance C_{pa} (parallel of C_{pa1} and C_{pa2}) is used as the integration capacitor.

V_{dc} values, as far as the pull-in of the cantilever is avoided, increases the displacement current and in consequence enables an easier detection.

A capacitive detection method has been chosen in order to detect the displacement current. The principle of operation is based on the integration of the capacitive current I_C by using a capacitor ($C_{pa} = C_{pa1} + C_{pa2}$) and measuring the resulting voltage (V_g in Fig. 4) by means of a voltage buffer circuit. This nonsampled technique in CMOS technology introduces less noise than resistive or transimpedance methods, since the capacitor does not introduce input-referred current noise [13].

An approximate analytical expression for the amplitude of V_g, is presented in (17), where ω is the signal frequency, A is the oscillation amplitude of the cantilever tip, and s_o is the gap distance in equilibrium. This equation takes into account that the excitation signal ($V_{in} = V_{dc} + V_{ac}$) does not only drop on the cantilever-driver capacitor but also on the parasitic capacitor, since it is based on a capacitor voltage divider scheme (16).

$$V(C) = V_{in} - V_g = V_{in}\frac{C_{pa}}{C_p + C_{pa}} \tag{16}$$

$$V_g = \frac{I_C}{\omega C_{pa}} \cong \frac{C_p}{C_p + C_{pa}}V_{ac} + 0.39\frac{C_p}{C_p + C_{pa}}\frac{V_{dc}}{s_o}A = V_p + V_d. \tag{17}$$

The parasitic term V_p is due to the applied ac voltage and the term corresponding to the cantilever displacement V_d is proportional to both the dc voltage and the oscillation amplitude. V_g does not depend on the frequency and it is inversely proportional to the value of C_{pa}. By reducing C_{pa}, the sensitivity of the detection system increases and consequently the capacitive current signal-to-noise ratio (SNR) at the V_g node improves. Due to the low level of current (few nA) at relatively high resonance frequencies (MHz) and the low value of C_p (0.2 fF), the use of integration capacitances in the fF range is compulsory. Consequently we have chosen the small intrinsic capacitance at the V_g node as the integration capacitance.

Fig. 4 shows that the parasitic capacitance (C_{pa}) can be divided in two components: C_{pa1}, constituted by the cantilever structure and substrate plus the electrical coupling to the cantilever, and C_{pa2} that represents the equivalent input capacitance of the CMOS circuit. The readout circuit design has focused on the minimization of all the parasitic capacitances as well as on getting high impedance at the sense node.

The read-out circuit design is presented in Fig. 5. It is based on a CMOS voltage amplifier biased as a source-follower (common drain configuration). The voltage at the gate node controls the current of transistor M1, this current is mirrored and amplified through transistors M3 and M4 and finally the voltage across transistor M2 (configured as active load) is measured. This approach minimizes the input capacitance of the circuit because the dominant capacitance is C_{gd} (M1) which in the saturation region is smaller than C_{gs} (M1). Finally a voltage follower has been included for driving the load capacitance C_l, that corresponds to the output pad and electrical test setup. Similar design of read-out circuit was used by Petersen *et al.* [14] for developing a micromechanical accelerometer integrated with a CMOS circuit.

Since V_g is a floating node (no dc path to any fixed voltage), it has to be polarized at the linear region of the amplifier. In this case the optimal value of V_g is around 0 V (Fig. 6). To guarantee this value, it is necessary to have a tuning circuit for biasing V_g. As aforementioned, we have to assure that the impedance at the sense node V_g is dominated by C_{pa} since the system has to operate like an integrator. On the other hand, any additional biasing element (zero-biased diode, MOS device acting as a switch, etc.) connected at the sense node may have undesired effects on the read-out system (basically an increment of the parasitic capacitance C_{pa} and also an increment of the input-referred current noise). In the present paper, the V_g biasing has been achieved by adding an extra capacitance between the gate and a dc voltage source V_{dp}, C_{pol} in Fig. 5. The value of this capacitance must be high enough to control the biasing of V_g without having to apply high voltages and low enough to not increase the parasitic capacitance (ΔC_{pa}). A good tradeoff for this capacitance is in the 1 fF range. In Fig. 7(a), an HSPICE simulation shows the effectiveness in polarizing the transistor gate and Fig. 7(b) shows the experimental results of the variation of V_{out} as a function of V_{dp} demonstrating the feasibility to polarize the amplifier with reasonable voltages. Note that experimentally it is not possible to measure the voltage at the gate of the input transistor V_g.

The polarization capacitance is defined in a postprocess to the CMOS circuit fabrication using the same nanofabrication methods as used for the cantilever fabrication. By using an interdigitized capacitor configuration, we minimize the increase of the parasitic capacitance due to the increase of the cantilever anchor dimensions.

Fig. 8(a) shows the layout of the cantilever/driver electrode system together with the additional capacitor in an interdigitized configuration (comb structure). The gray area of the layout is defined during the CMOS circuit fabrication and it results in what we call the "nanoarea," i.e., the area where the nanomechanical device will be fabricated. The final structure (black areas in Fig. 8(a) is defined as a postprocess to the CMOS circuit fabrication using nanolithography and etching processes. Fig. 8(b) illustrates the concept of the nanoarea: it shows the layout of the CMOS circuit and the square area where the nanocantilever will be fabricated.

Although the success of V_g polarization has been verified (see Fig. 7(b) and Section V), using a capacitor produces an unstable dc voltage at the sense node due to leakage currents, which in turn produces variations of the bias point. These variations have

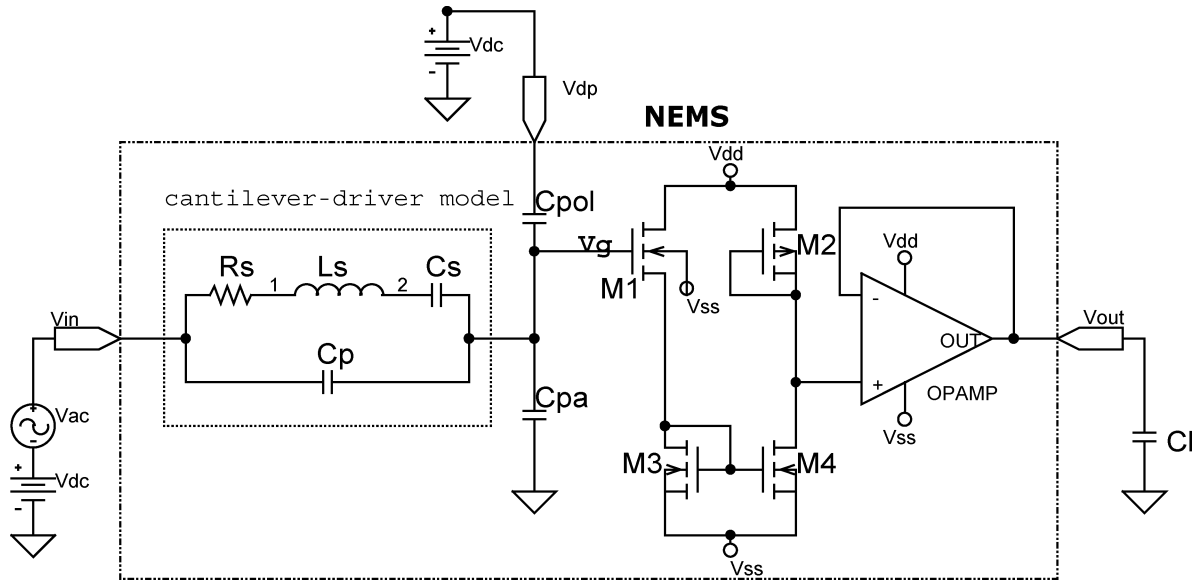

Fig. 5. Electrical scheme of the read-out circuit along with the nanotransducer electrical model. The read-out circuit is by a CMOS voltage amplifier biased as source-follower plus voltage follower for output driving.

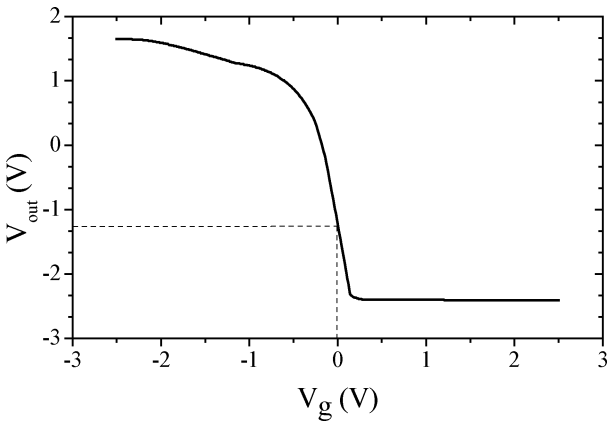

Fig. 6. Simulation of the static characteristic of the read-out CMOS circuit. The optimal dc polarization voltage (which corresponds to the maximum gain) is indicated.

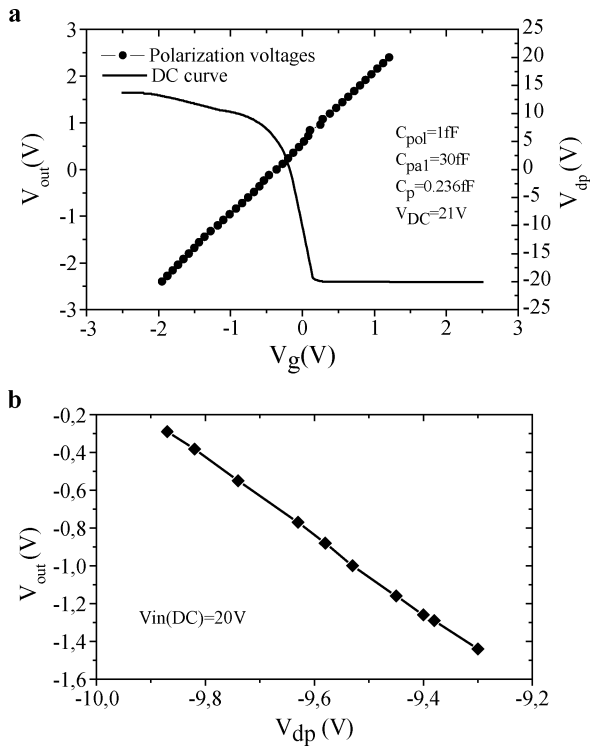

Fig. 7. (a) HSPICE simulation of the variation of the gate voltage $\mathrm{V_g}$ and output voltage $\mathrm{V_{out}}$ for different polarization voltages $\mathrm{V_{dp}}$. (b) Experimental results of the variation of the output voltage $\mathrm{V_{out}}$ of the amplifier as a function of different polarization voltages $\mathrm{V_{dp}}$.

been detected for a time scale long enough to not affect the measurement of the full frequency spectral resonance of the cantilever (see Section V). Other strategies for circuit polarization are currently being undertaken, which are based on the use of a very large resistor (zero-biased diode) in a special feedback topology that minimizes the negative effect of the junction diode capacitance on C_{pa}.

In Fig. 9, we show the frequency response of the overall system (mechanical resonator plus the read-out circuit) obtained by HSPICE postlayout electrical simulation. We can observe the resonance peak located at 887 kHz for a cantilever with a length of 40 μm (the rest of the parameters are chosen from Table I). Fig. 9(a) corresponds to the case of a parasitic capacitance $C_{pa1} = 30$ fF. The effect of increasing C_{pa} is shown in Fig. 9(b), which illustrates the necessity of keeping the parasitic capacitance as small as possible.

IV. Fabrication

The fabrication process is depicted in Fig. 10. The fabrication of the cantilever is performed as a postprocess module on prefabricated CMOS chips. The CMOS technology is a standard twin well, 2-poly, 2-metal technology [8]. The cantilever is fabricated using the first poly-silicon layer (poly0). This layer is used in the CNM standard CMOS process as the bottom plate for analog capacitors, and consequently, it is possible to slightly modify it without changing the transistors characteristics. In our case, the poly0 layer thickness was increased from 350 to 600 nm to improve mechanical properties of the cantilever; the deposition temperature was reduced to 580 °C and doped at

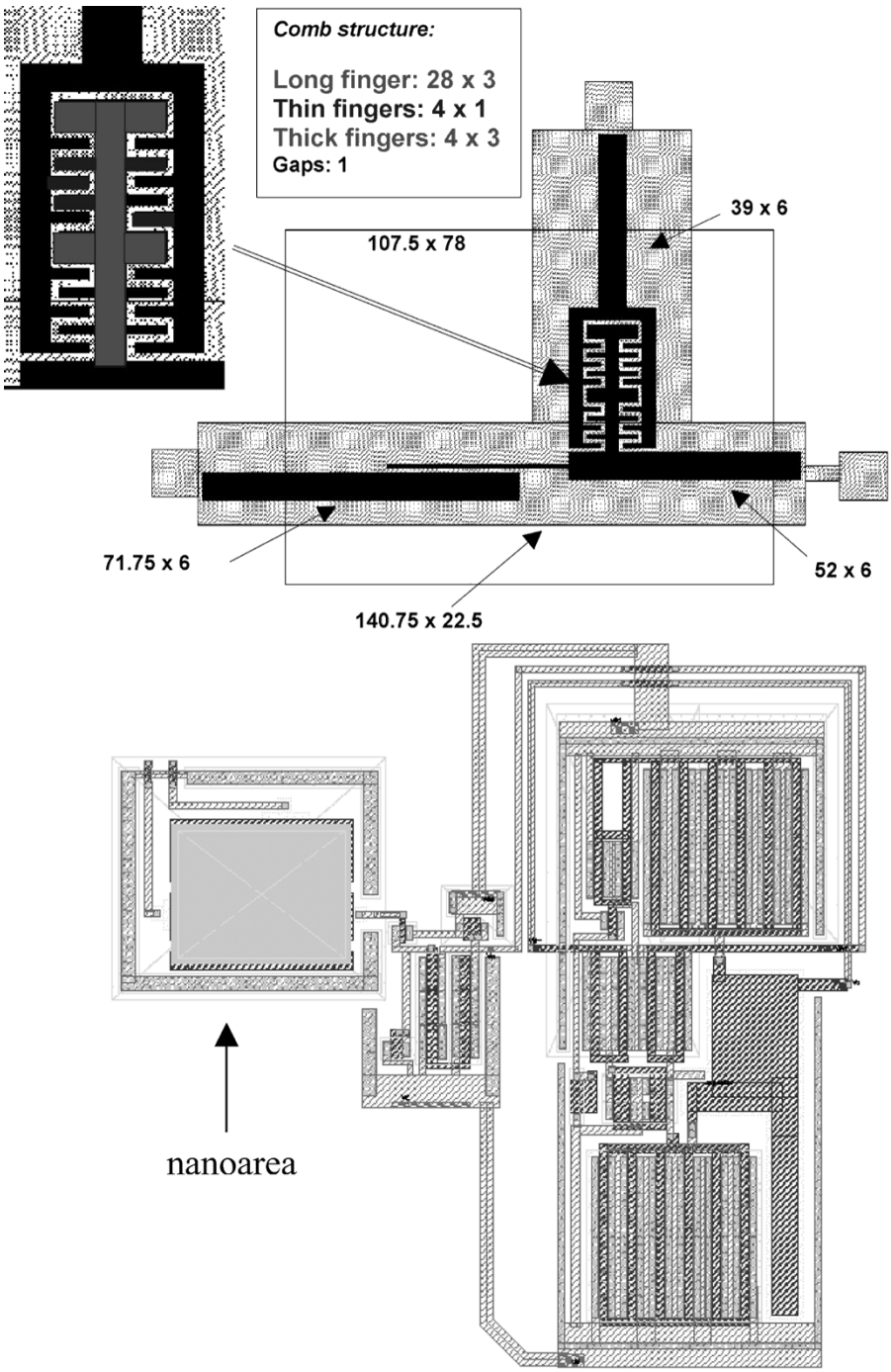

Fig. 8. (a) Schematic diagram of the mechanical structure to be fabricated with nanofabrication techniques. Cantilever, driver and comb capacitor for biasing the voltage amplifier are shown. All dimensions are in micrometers. (b) Layout of the monolithic system showing the nanoarea where the mechanical transductor will be fabricated as a post-CMOS process.

950 °C with $POCl_3$. The final layer has a sheet resistance of 13.8 Ω/sq and the surface roughness has been reduced from 15 to 7 nm [15]. This layer is oxidized during the growth of the gate oxide and covered by the second polysilicon layer (poly1) to protect it. Until the end of the CMOS fabrication, masks are designed to remove oxide and metal layers on top of the platform area.

For prototyping purposes, the postfabrication step is performed on a chip basis. The first step of the postfabrication is opening a hole in the passivation of the CMOS circuit and dry etching through the top poly1 layer [Fig. 10(a)] to define the "nanoarea." Then, the *cantilever/driver electrode/polarization capacitor* mask definition step is performed [Fig. 10(b)]. A thin aluminum layer is deposited on the entire chip and it is selectively annealed using laser lithography, which presents a linewidth resolution of around 700 nm. Next, the nonannealed Al is etched chemically leaving the annealed-Al mask [16]. After the mask definition, the pattern is transferred to the poly0 layer by dry etching [Fig. 10(c)]. Finally, the structures are released in BHF, which etches the underlying 1-μm-thick SiO2 layer [Fig. 10(d)]. Fig. 11 shows an image of one of the fabricated sensors. In this case, the width of the cantilever is

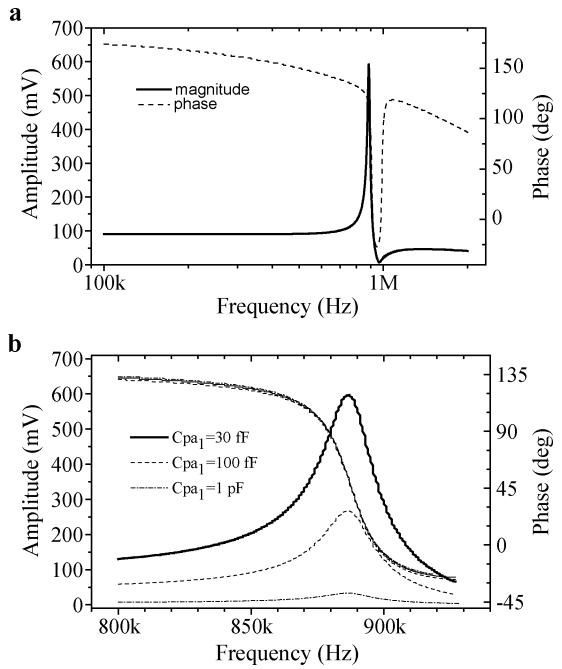

Fig. 9. (a) Simulation of the frequency response for the global system (mechanical resonator plus read-out circuit). A $C_{pa1} = 30$ fF has been assumed. (b) Hspice simulation of the frequency response (amplitude and phase) around the resonance frequency of the electromechanical system for different values of the parasitic capacitances. Note the degradation of the amplitude signal when the parasitic capacitance increases.

TABLE II
ELECTRICAL PARAMETERS FOR THE DIFFERENT FABRICATION PROCESSES OF THE VOLTAGE AMPLIFIER (AVERAGE FROM SEVERAL CHIPS FROM EACH PROCESS)

Parameter	RUN1995	RUN2000	RUN2380
BW (-3dB) MHz	1.75	1.9	2.2
Gain (DC)	6.2	6.7	6

approximately 800 nm. A similar process has been recently developed employing e-beam lithography instead of laser lithography, which can reduce the width of the cantilever down to 350 nm [17].

V. ELECTRICAL CHARACTERIZATION AND TEST

The frequency response and the static characteristic of the implemented CMOS amplifier (before the post-CMOS fabrication of the mechanical device) are depicted in Fig. 12. The frequency response of the circuit has been characterized when $V_o(\mathrm{dc}) = -1.3\,\mathrm{V}$, which corresponds to an optimal dc biasing. The resulting experimental frequency bandwidth and voltage gain are 1.75 MHz and 6.22 V, respectively. Due to some variations of the CMOS parameters, several circuits from different fabrication processes have been tested. In Table II the dispersion on these parameters is shown. From the electrical characterization the expected performance of the transducer is obtained.

The electrical magnitude of the frequency response of the nanoelectromechanical system is presented in Fig. 13(a). These two curves have been obtained by applying an ac voltage of 7 $\mathrm{V_{pp}}$ and a dc voltage of 18 and 20 V to the driver. The peak of the curves corresponds to the mechanical resonance of the cantilever as it has been corroborated by the simultaneous inspection with an optical microscope

Fig. 13(a) shows that the resonance peak is larger and shifted to a lower frequency when increasing the dc voltage. When applying a higher dc voltage the force between the driver and cantilever increases, increasing the oscillation amplitude of the cantilever and thereby the voltage output. Also, the increase in electrostatic force decreases the effective spring constant of the cantilever and thus decreases the cantilever resonance frequency. An analytical expression of the dependence of the resonance frequency on the dc voltage is [18]

$$f(V) = f_o - \left(\frac{2 f_o \varepsilon_o l^4}{E w^3 s^3}\right) V^2 \quad (\mathrm{Hz}). \tag{18}$$

Since we use both dc and ac voltage, $V^2 = V_{\mathrm{dc}}^2 + 1/2(V_{\mathrm{ac}}^2)$ in this case. Fig. 13(b) shows the experimental (dots) dependence of the resonance frequency together with the linear fit curve. From the dimensions of the cantilever and using the equations from the electromechanical model explained in Section II, we find that the theoretical value of the natural resonance frequency $(\mathrm{V_{dc}} = 0)$ is 703 kHz. This is approximately the same value as obtained from the experimental results, shown in Fig. 13(b). From these results, we obtain that the theoretical sensitivity of this cantilever is $34 \cdot 10^{-18}\,\mathrm{g/Hz}$, which is an extremely high sensitivity for punctual mass detection. In terms of distributed mass detection, the sensitivity is $12 \cdot 10^{-13}\,\mathrm{g/Hz/cm^2}$ which is comparable to quartz microbalances. By further decreasing the dimensions of the cantilever, this sensitivity can be improved.

The final resolution of the cantilever will depend on the minimum change of frequency that the system will be able to detect. Along with factors like electrical and thermomechanical noise, this is limited by the value of the Q-factor. The Q-factor of the cantilever depends strongly on the environment where the measurements are performed. In this case, the experimental results have been obtained in air. For both curves, we have obtained a $\mathrm{Q-factor} \approx 21$. This value is increased when working in vacuum, as we have already shown for discrete resonators [7], or by using feedback specific techniques, as previously proposed [6].

First, we can evaluate the minimum change of frequency due to the electrical noise for our integrated read-out circuit. A simple and rough estimation of the change of the transducer output V_{out} close to the resonance can be expressed as the ratio between the maximum voltage at the resonance and the second-order system frequency bandwidth (19). Taking into account the definition of the quality factor Q we obtain

$$\frac{\partial V_{\mathrm{out}}}{\partial f} \approx \frac{V_{\max}}{\Delta f} = \frac{Q V_{\max}}{f_o}. \tag{19}$$

From this expression, the variation of frequency as a function of the SNR of the read-out system at the resonance can be obtained

$$\delta f \approx \frac{f_o}{Q} \frac{\delta V_{\mathrm{out}}}{V_{\max}} \approx \frac{f_o}{Q} \frac{1}{\mathrm{SNR}}. \tag{20}$$

From the values of the simulated electrical noise and the bandwidth of our read-out system (250 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ and 1 kHz, respectively), the $\mathrm{SNR} \cong 84\,\mathrm{dB}$. Consequently, from (20), the

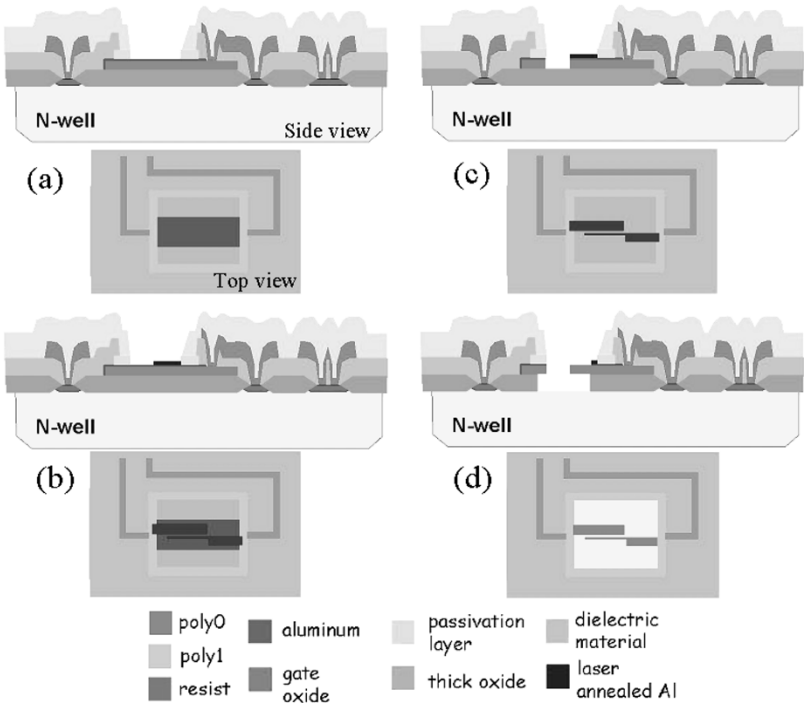

Fig. 10. Diagram of the simplified post-CMOS process to fabricate the nanomechanical device using laser litography compatible with CMOS.

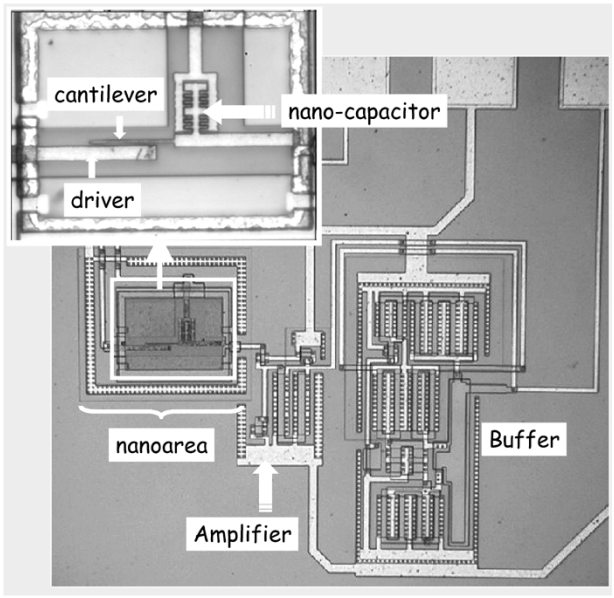

Fig. 11. Optical images of the nanomechanical resonator integrated monolithically with the CMOS voltage amplifier. The large image shows the CMOS circuit and the area where the nanomechanical device is fabricated. The inset ia a zoom image of it, where it can be better appreciated the cantilever, the driver and the integrated capacitor for proper circuit polarization. The dimensions of the cantilever are: length $l = 40\ \mu\mathrm{m}$; width $w = 840\ \mathrm{nm}$; thickness $t = 600\ \mathrm{nm}$, and gap spacing $s = 1.3\ \mu\mathrm{m}$.

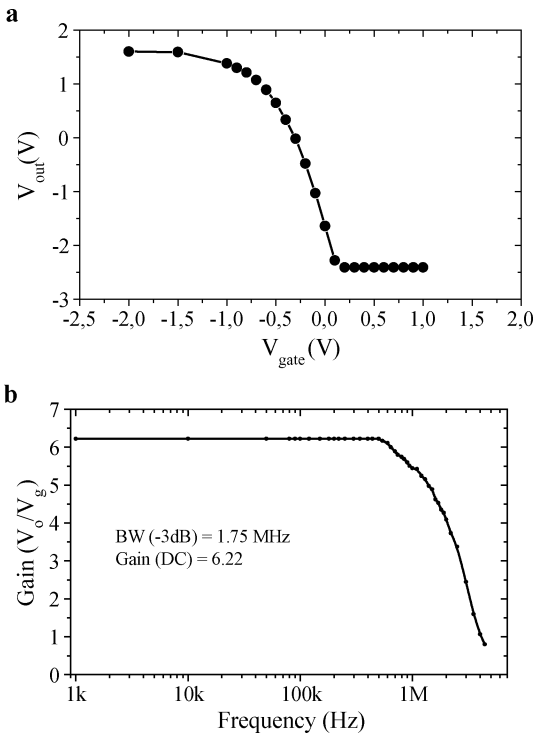

Fig. 12. Experimental electrical test results of the implemented read-out circuit. (a) Static characteristic. (b) Frequency response.

minimum measurable frequency change is $\delta f \approx 1.9$ Hz. In this case, the mass sensitivity with the integrated system will be below 65 attograms.

Second, we have evaluated the effect of $\mathrm{V_g}$ polarization which induces dc voltage instabilities at the sense node, which in turn produces variations of the bias point. We have experimentally obtained that the dc variation at the output of the circuit is in the order of 5 mV in the time framework of the experiment. Taking into account that the experimental gain of the circuit (buffer amplifier) is 4.85, the Vg variation voltage will account for 1 mV. The frequency stability evaluation can be derived from the frequency dependence with the applied voltage [Fig. 13(b) and (21)].

$$f_{\mathrm{res}}\ (\mathrm{kHz}) = 701 - 0.139V^2. \tag{21}$$

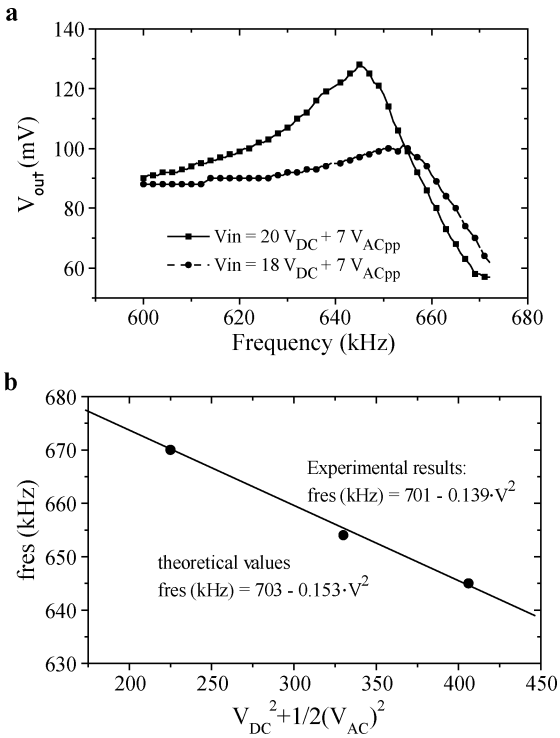

Fig. 13. (a) Electrical characterization of the global system (CMOS voltage amplifier circuit plus electromechanical transducer) corresponding to the system shown in Fig. 11 for two different dc voltages ($\mathrm{V_{dc}}$). (b) Experimental dependence of the resonance frequency the applied voltage. The points corresponds to three experimental resonance frequencies [two of them corresponding to (a)] and the straight line to the linear fit.

According to this dependence, and taking into account the dc voltage applied in this experimental data ($\mathrm{Vdc} = 18$ V), the frequency stability will be $\Delta \mathrm{f} = 5$ Hz [calculated from (22)] which is in the same range than the thermomechanical noise inherent to mechanical devices and constitutes the major source of noise in our system

$$\delta f_{\mathrm{res}}\,(\mathrm{kHz}) = 2 \cdot 0.139 \cdot V_{\mathrm{dc}} \delta V. \tag{22}$$

From the ac value of V_{out} at 600 kHz, when the cantilever is out of resonance, we can estimate the value of the total parasitic capacitance C_{pa} by assuming a simple ac capacitive voltage divider formed by C_{pa} and the static capacitance C_p (16). The value of V_g is the value of $V_{\mathrm{out}}(ac)$ $(90\ \mathrm{mV_{pp}})$ divided by the gain (G_{amp}) of the circuit at 600 kHz. This gain has been determined experimentally from the frequency response of this readout circuit and it is found to be 4.85 (at 600 kHz). Thus, we obtain a value of $V_g = 18.6\ \mathrm{mV_{pp}}$. The value of V_g cannot be tested directly because any external connection would introduce an additional parasitic capacitance. However, we know the value of C_p calculated from the dimensions obtained by the optical inspection of the fabricated cantilever, which is around 122 aF (note that for this evaluation the coupling length of the cantilever is 30 μm). With these values and knowing that $V_{\mathrm{in}}(ac)$ is 7 $\mathrm{V_{pp}}$, we obtain a value of $C_{pa} = 46$ fF. This is in good accordance with the expected value. From this result and taking into account (17), we are able to evaluate the amplitude of the cantilever movement at the resonance (≈250 nm). Finally from this amplitude and assuming a linear deflection of the cantilever,

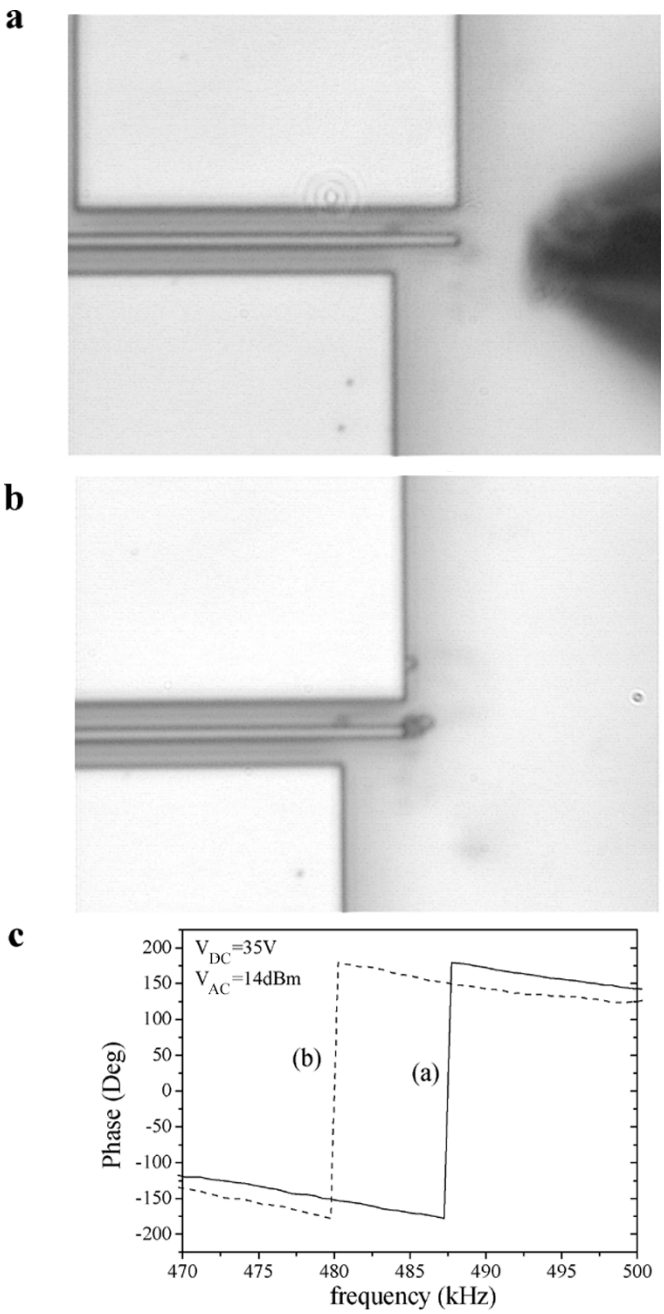

Fig. 14. Optical images of a cantilever before (a) and after (b) a cluster of 4 latex spheres (1 μm diameter) has been electrodeposited from an STM tip by applying a 50-V pulse. (c) Phase frequency response of the cantilever before (a) and after (b) the deposition of the 4 latex spheres. The 8-kHz shift on the resonance frequency corresponds to a mass of 2160 fg.

we can also evaluate the variation of the static capacitance (C_p) due to the cantilever movement $(\Delta C \approx 40\ \mathrm{aF})$. These results validate the overall circuit design and fabrication process that we have chosen to fabricate the mass sensor, and the success of the combination of a nanomechanical device and a CMOS circuit.

Testing of mass sensitivity requires dedicated experimental setup that will allow to deposit known small quantities of mass at the tip of the nanometer-scale cantilever. Here, we present preliminary measurements performed on nonintegrated devices fabricated on SOI wafers (Fig. 14). In this case, the thickness

of the SOI layer, and in consequence, the thickness of the cantilever, is $t = 5\ \mu\mathrm{m}$. Then, the cantilever is robust enough to withstand the mass deposition. On the contrary, a larger thickness is not compatible with the CMOS technology used, forcing the use of an optical characterization scheme. The cantilever is electrostatically excited to its resonance frequency, and the resulting amplitude and phase of the oscillation, with respect to the excitation signal, is measured optically. Mass detection has been tested by locally adding clusters of 1 $\mu\mathrm{m}$ diameter latex beads (549 fg/bead) [19] at the very end of the cantilever. The procedure used to deposit latex beads on the cantilever consists on the following steps: 1) A cluster of latex beads is deposited by contact at the end of a electrochemical sharpened gold wire. 2) The cluster at the end of the gold wire is approached to less than 1 um of the free end of the cantilever [Fig. 14(a)]. 3) The cluster is deposited from the gold wire to the cantilever by applying a positive voltage to the wire [Fig. 14(b)]. This method can be performed on the same set-up where the electrical characterization is performed and, as a consequence, it allows to measure the resonance frequency of the cantilever right before and right after depositing mass locally at the end of the cantilever [Fig. 14(b)]. By this procedure, we have been able to detect the mass of a cluster of 4 latex beads. The mass of this cluster, 2160 fg, is deduced from an 8-kHz shift on the frequency response [Fig. 14(c)] which has been measured on a cantilever with a mass sensitivity of 3.7 Hz/fg.

VI. Conclusion

We have presented the main aspects of the monolithic integration of a submicron mechanical resonator with a CMOS circuit for the development of a high sensitivity mass sensor. The combination of nanomechanical devices with CMOS circuits requires addressing specific issues such as the decrease of parasitic capacitance. The fabrication of the first prototypes shows the feasibility of the circuit strategy and technological approaches. The results presented here indicate an extremely high sensitivity in terms of absolute mass detection and a similar sensitivity to quartz microbalances in terms of distributed mass detection.

The sensitivity of the devices can be improved by a further reduction of the dimensions of the cantilever. For doing this, the approach presented here is general enough to continue being valid. The present limitations are imposed by the minimum size of the width of the cantilevers that can be patterned and by the maximum frequency of the circuit operation. Smaller cantilevers have already been fabricated using e-beam lithography. Increasing the frequency operation of the circuits requires the use of more advanced CMOS technology, which can be easily addressed taking into account that the structural layer of the resonators is a polysilicon layer which is usually present in all standard CMOS technologies. Further developments in course are the introduction of intelligence in the system by increasing the functionality of the CMOS circuits.

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Jaume Verd (S'04) was born in Pollença, Spain. He received the B.Eng. degrees in telecommunication engineering in 1997 and in electronics engineering in 2001 from the Universitat Politècnica de Catalunya, Spain, and the Universitat Autònoma de Barcelona, Spain, respectively. In 2003, he received the M.Sc. degree in electronics engineering from the Universitat Autònoma de Barcelona. He is currently pursuing the Ph.D. degree at the Electronics Engineering Department.

His current research focuses on CMOS integrated sensors based on micro/nanoelectromechanical systems (M/NEMS).

G. Abadal received the degree in physics in 1991 and the Ph.D. degree in electrical engineering in 1997 from the Universitat Autònoma de Barcelona, Spain.

Since 2002, he has been an Associate Professor in the Electronics Engineering Department, Universitat Autònoma de Barcelona. His research interests are in the area of SPM-based nanolithography, design, and characterization of nanoelectromechanical systems (NEMS) and compatibilization of nanotechnologies with CMOS microtechnologies.

J. Teva was born in Barcelona, Spain, in 1977. He received the B.Sc. degree in physics and in electrical engineering from the Universitat Autònoma of Barcelona in 1999 and 2002, respectively. He received the M.Sc. degree in electrical engineering. He is currently working towards the Ph.D. degree at the Universitat Autònoma of Barcelona.

Since 2001, he has been an Assistant Professor with the Electronics Engineering Department, Universitat Autònoma of Barcelona. His current research activities are the design and characterization of nanoelectromechanical systems (NEMS) for sensors and RF applications.

María Villarroya Gaudó was born in Soria, Spain, in 1977. She received the B.Sc. degree in physics from the University of Zaragoza, Spain, in 2000. In September 2002, she received the M.Sc. degree in electronics engineering from the Autonoma University of Barcelona, Spain. She is a Ph.D. student with the Department of Electronics Engineering, Autonoma University of Barcelona. Currently, she is pursuing the Ph.D. degree at the Autonoma University of Barcelona.

Her research field is nanoelectromechanical systems based on silicon technology. Her work is mainly focused in cantilever-based sensors, specifically in the compatibility of standard CMOS technology with new nanotechnology and in biological sensors working in liquid. She is also an Assistant Professor with the Department of Informatics and Systems Engineering, University of Zaragoza.

Arantxa Uranga was born in Burgos, Spain, in 1971. She received the degree in physics and electronic engineering from the Valladolid University, Spain, in 1994 and 1996, respectively, and the Ph.D. degree in electronic engineering from the Autònoma University of Barcelona, Spain, in 2001.

Since 1996, she has been with the Department of Electronic Engineering, Universitat Autònoma de Barcelona, where she is a Research Scientist. Her research interests include the design of CMOS circuits for biomedical and RF applications.

Xavier Borrisé was born in Girona, Spain, in 1971. He graduated in physics in 1994 and received the Ph.D. degree in electrical engineering in 2000, working on the design of scanning near-field optical microscope for the characterization of optoelectronic devices, and the application of the microscope to silicon-based integrated waveguide devices.

Since 2003, he has been with the National Center for Microelectronics of Spain, working in the application of nanolithographic and technology fabrication for nanothecnology, like NanoImprint, electron beam, and AFM lithography.

Francesca Campabadal was born in Sabadell, Spain, in 1959. She received the Ph.D. degree in physics in 1986 from the Universitat Autònoma de Barcelona, Spain.

In 1987, she joined the Microelectronic National Centre (CNM-CSIC), where she is working on thin oxide technology and characterization. Since 1992, her research activities have been also in the field of technologies for silicon sensors and microsystems and in the monolithic integration of mechanical sensors and CMOS circuitry.

Jaume Esteve was born in Parets del Vallés, Barcelona, Spain, in 1961. He received the Ph.D. degree in physical electronics from the University of Barcelona in 1988.

In 1990, he joined the Department of Silicon Technology and Microsystems, Microelectronic National Centre (CNM-CSIC), as a Senior Research Scientist. His areas of interest include silicon micromachining technologies and their application to integrated sensors and actuators.

Eduardo Figueras Costa was born on March 14, 1959, in Barcelona, Spain. He graduated in physics and received the Ph.D. degree in physics in 1983 and 1988, respectively, both from the "Universitat Autonoma de Barcelona."

From 1983 to 1984, he was an Assistant Professor with the Electronics Department, Universitat Autonoma de Barcelona. From 1985 to 1988, he was with the Microelectronic Laboratory of the "Université Catholique de Louvain," Belgium, wjere he worked on improvements of the isolation oxide on CMOS. In 1989 he obtained a post with the Microelectronic National Centre (CNM-CSIC) as Tenured Scientist (Científico Titular). Until 1998, he supervised all technological processes developed at CNM and was responsible of the standardization of all new fabrication processes as Clean Room Manager. Since 1999 his main activity has been focused on microsystems fabrication processes. He is currently with the Microsystems and Silicon Technologies Department dealing mainly with gas sensors and surface and bulk nano/micromachining. His interests are aimed at developing nano/micromachining resonant devices to be used as gas sensors.

Francesc Pérez-Murano (M'99) was born in Barcelona, Spain, in 1966. He received the degree in physics in 1989 and the Ph.D. degree in 1994, both from the Universitat Autónoma de Barcelona.

He has been an Associate Professor with the Electronics Engineering Department, Universitat Autònoma de Barcelona. Currently, he holds a Scientific Research position with the Centro Nacional de Microelectrónica belonging to the Spanish Research Council. He has been involved in the following research areas: microelectronics, integrated optoelectronics, nanotechnology, and scanning probe microscopy. His current research activities include the development of new methods for nanofabrication and the application of nanoelectromechanical systems to the field of physical, chemical, and biochemical sensing.

Zachary J. Davis received the M.Sc. degree in engineering within the field of applied physics and the Ph.D. degree in electrical engineering from the Technical University of Denmark (DTU) in 1999 and 2003, respectively.

He has worked with design, fabrication, and characterization of MEMS and NEMS for biochemical sensors and monolithic integration of these sensors with CMOS technology. In 2003, he joined EPSON Europe Electronics GmbH as a MEMS/NEMS engineer, coordinating a project between EPSON BRDL and CNM, both located in Barcelona, Spain, where he is developing HF/RF MEMS oscillators also monolithically integrated with CMOS technology for electronic applications.

Esko Forsén received the M.Sc. degree in physics from the University of Lund, Sweden, in June 2002. The subject of his master's degree thesis was the development of electrochemical biosensors. He received a Ph.D. degree scholarship from the Technical University of Denmark (DTU).

After graduating from the University of Lund, he joined the Department of Micro and Nanotechnology (MIC), DTU. He has been the author or coauthor of seven scientific publications. His work deals with the fabrication of nanoelectromechanical resonator systems for biosensor applications. His research interests deal with combining different aspects of nanotechnology with microelectronics for life science applications.

Anja Boisen received the M.Sc. degree in physics from Roskilde University, Denmark, in 1993. She received the Ph.D. degree in micromechanics from the Department of Micro and Nanotechnology (MIC), Technical University of Denmark (DTU), in 1997.

She has been with the MIC since 1997 as an Assistant Professor, and was appointed Associate Professor in 1999. She is currently leading a project on cantilever-based biochemical sensors.

Nuria Barniol (M'99) received the B.S. and Ph.D. degrees in physics from the Universitat Autònoma de Barcelona, Spain, in 1987 and 1992, respectively.

Currently, she is a Professor with the Electronics Engineering Department at the same university. Her research interests are on the development of new analog integrated circuit structures for sensory and high-frequency systems in MEMS/NEMS applications.

Chapter 12

"Resonators with integrated CMOS circuitry for mass sensing applications, fabricated by electron beam lithography"

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Resonators with integrated CMOS circuitry for mass sensing applications, fabricated by electron beam lithography

S Ghatnekar-Nilsson[1,5], E Forsén[2,5], G Abadal[3], J Verd[3], F Campabadal[4], F Pérez-Murano[4], J Esteve[4], N Barniol[3], A Boisen[2] and L Montelius[1]

[1] Solid State Physics/The Nanometer Consortium, Lund University, PO Box 118, S-221 00 Lund, Sweden
[2] Department of Micro and Nanotechnology (MIC), Technical University of Denmark, Kongens Lyngby, Denmark
[3] Departamento de Enginyeria Electrónica, Universitat Autónoma Barcelona, Bellaterra, Spain
[4] Centro Nacional de Microelectrónica, Campus Universitat Autónoma de Barcelona, Bellaterra, Spain

E-mail: Sara_G.Nilsson@ftf.lth.se

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Abstract
A resonator system has been fabricated directly on a pre-processed CMOS chip. The system is to be used for high sensitivity mass sensing applications in air and vacuum. The resonator system, corresponding of a cantilever and structures for electrostatic actuation and capacitive read-out, have been defined by electron beam lithography on top of a charge and radiation sensitive CMOS layer in predefined areas as a post-process step. This has been accomplished without affecting the electronic properties of the pre-processed CMOS circuits. The subsequent etching steps to fully release the cantilevers have been obtained without stiction of the cantilevers to the substrate. Cantilevers are driven at their mechanical resonance in a lateral mode, and the frequency is monitored by capacitive read-out on the chip. CMOS integration enables signal detection directly on the chip, which radically decreases the parasitic capacitances. Consequently, low-noise electrical measurements with a very high mass sensitivity are obtained. Fabricated resonator systems were characterized to have resonance frequencies of approximately 1.49 MHz, which is in good agreement with a theoretical estimation of 1.41 MHz. The theoretical mass resolution, $\partial m/\partial f$, is approximately 17 ag Hz^{-1}, using a Young modulus value of 160 GPa.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Micrometre-sized cantilever structures are widely used for sensor applications. Monitoring cantilever deflection has been used quite extensively for biosensing [1–4] where adsorbed molecules have led to a deflection induced by surface stress. A static cantilever deflection is mostly detected optically [5] and piezoresistively [6]. The fabrication of microcantilevers is known from the art of micromachining [7] and complies with batch processing. Dynamic mode cantilever sensors are based on vibrating the cantilever and detecting the cantilever resonance frequency shift due to mass changes of the cantilever, e.g. due to adsorption of molecules. For a cantilever with a rectangular cross section a simple harmonic oscillator

[5] Have equally contributed in this work.

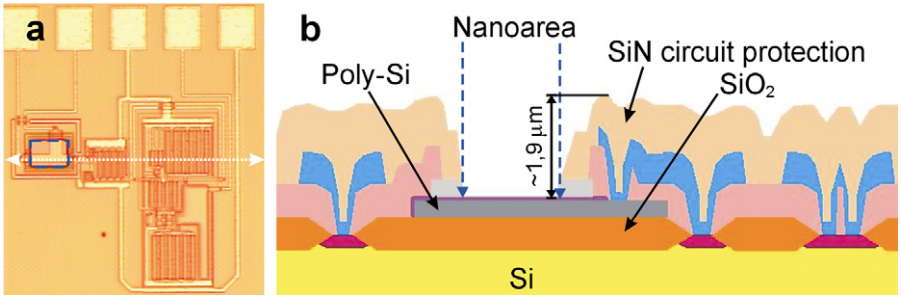

Figure 1. (a) An optical microscope image of a section of a CMOS chip. The white dotted line represents the cross section area. The dark square represents the lithography area on a CMOS chip (called the nanoarea in the text). A schematic cross section of the CMOS chip, as shown in (a), is viewed in (b). (b) Cantilevers are defined out of the 600 nm thick poly-Si layer over a 1 μm thick sacrificial SiO_2 layer. The fabrication area lies in a 1.9 μm deep trench and hence spin coating of resist leads to thickness variations in the nanoarea. Consequently, care has to be taken to establish electrical contacts over the edges.

model can be applied to describe the resonance frequency [8], from which an expression describing the mass resolution can be obtained,

$$\frac{\delta m}{\delta f} \propto \frac{k}{f_0^3}.$$

f_0 is the cantilever resonance frequency, k is the spring constant, δm is the minimum detectable mass and δf is the frequency resolution. In order to deduce an adsorbed mass, only the magnitude of the resonance frequency shift and the value of the resonance frequency need to be determined, assuming that the spring constant is not affected by the added mass. Furthermore, one can conclude that increasing the resonance frequency while keeping the spring constant fixed leads to an increase in mass sensitivity. Such systems can benefit significantly from miniaturization e.g. by simply reducing the dimensions of the cantilever to the nanometre scale. Hence, in order to achieve highest possible mass sensitivity, research on fabrication, integration and development of nanomechanical resonator systems are pursued [9–11].

We have previously reported on the principle and fabrication of a nano-electromechanical system (NEMS) based resonator sensor system [12, 13]. The resonator system consists of a cantilever and structures for electrostatic actuation and capacitive read-out. Mass measurements are performed by electrostatically driving the cantilever at its mechanical resonance. If an additional mass is loaded on the cantilever, e.g. adsorption of molecules, the resonance frequency will be reduced corresponding to the increase in mass. The resonance frequency shift is monitored by a capacitive detection technique on chip [13, 14]. The cantilevers are defined out of a poly-Si layer on pre-processed CMOS chips. The fabrication is based on electron beam lithography (EBL), followed by several etching steps. To our knowledge, this is the first time EBL has been used to define a NEMS structure on top of a pre-processed CMOS chip.

The approach to detect the signal directly on the chip is beneficial from several points of view. It makes it possible to integrate an array of cantilevers for simultaneous label free detection of different compounds on a single chip, and to increase the signal to noise ratio by performing differential detection. However, the largest advantage is the radical decrease in parasitic capacitances since large bonding pads and external wires are eliminated, which enables low-noise electrical measurements. Hence, CMOS integration allows the development of systems based on cantilevers miniaturized to dimensions of the nanometre scale. This is the major reason for defining the cantilevers with EBL since devices with dimensions less than 50 nm can easily be patterned by this technique. The result is systems with high sensitivity, low energy consumption and short response times.

However, it is far from straightforward to realize such a system. First, the electron beam lithography on top of a delicate charge and radiation sensitive CMOS layer has to be considered. Second, the normally not harmful solid–liquid–vapour forces after the release etching of the cantilever structure will become a severe threat to the survival of such structures when at the nanometre scale. Third, the nanometre sized cantilever has to function in accordance with the circuits on the chip, and be made of a material compatible with the pre-patterned CMOS circuit.

In this paper we will discuss all these considerations in detail and describe a way to solve these issues leading toward a fully functional integrated cantilever chip. In particular, we present EBL using low acceleration voltage to minimize irradiation damage on CMOS chips.

2. Experimental details

The fabrication of the mechanical cantilever is performed as a post-process module on pre-fabricated CMOS chips. The CMOS technology is a standard 2.5 μm twin-well, two-poly–two-metal-level CMOS. Cantilevers are fabricated out of the bottom poly-Si layer (defined as the nanoarea) as shown in figure 1. The poly-Si thickness is roughly 600 nm and underneath is a 1 μm thick sacrificial SiO_2 layer. In figure 2, a sequence of images at various magnifications is shown, illustrating the different processing steps as outlined below.

A double-layer positive resist system is deposited on the CMOS chips by spin coating. The bottom layer consists of approximately 170 nm of ZEP-520A7 and the top layer consists of 70–80 nm of PMMA 950 A4. A converted JSM 6400 scanning electron microscope (SEM) with a LaB_6 cathode with an ELPHY III pattern generator (*RAITH GmbH*) is used for the EBL patterning. Following the EBL exposure, the resists are first developed in a mixture of methylisobutylketone/isopropanol (MIBK:IPA; 1:3) and then in *o*-xylene with a final rinse in IPA. Then a 30 nm thick Al layer

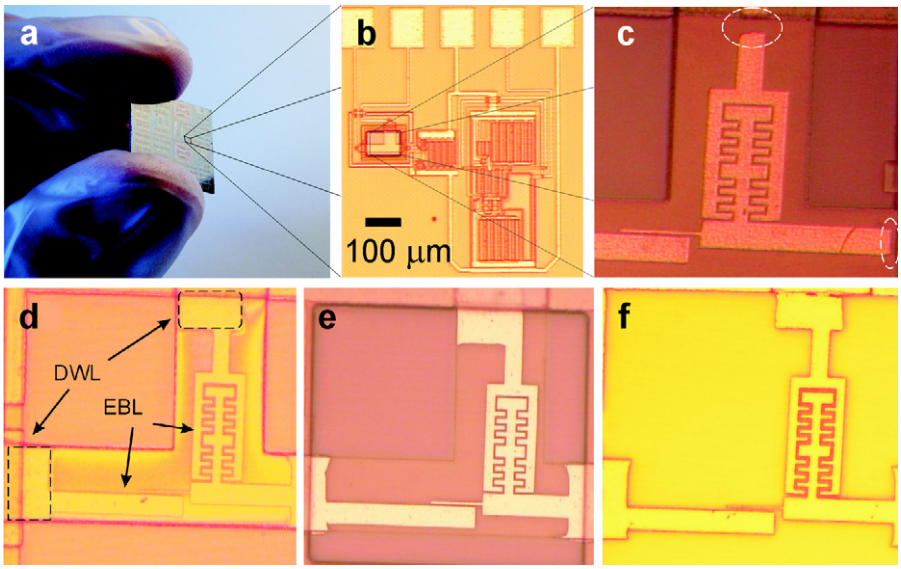

Figure 2. Optical images of combined EBL and DWL on CMOS at different magnifications and stages of the processing. (a) An optical image of the CMOS chip indicating one NEMS system. (b) This picture shows an enlargement of the NEMS system with the nanoarea and the corresponding CMOS circuits. (c) Due to the thicker resist layer at the edge of the fabrication area, 3 kV electron beam exposure is not enough to fully expose all the resist, resulting in inadequate Al mask definition at the edges of the fabrication area. (d) This image shows the result of combined EBL and DWL after the development of the resist. DWL was used for patterning of rectangular structures on to resist that was pre-exposed with EBL. (e) Result of 30 nm Cr lift-off using combined EBL and DWL. The edge uniformity between the DWL and the EBL exposed areas is excellent. (f) This picture shows the result after sacrificial wet etching of the defined cantilever. A supportive resist film is present, which later is removed in a dry fashion by oxygen plasma.

is thermally evaporated and lifted off to serve as an etching mask.

After the lift-off, anisotropic reactive ion etching (RIE) is performed in order to transfer the EBL made pattern to the structural poly-Si layer. The anisotropy is achieved with SF_6:O_2 plasma.

After structural patterning, the poly-Si structures are to be released from the substrate by an isotropic wet etch of the SiO_2 layer, using buffered hydrofluoric acid (BHF). First, the CMOS chips are spin-coated with 2.5 μm of the photo-resist AZ 5214E. The photo-resist acts as a protection mask for the CMOS circuitry against the BHF. Next, ultra-violet lithography (UVL) is used to create windows over the structural areas after which the chips are placed in BHF. Finally, the chips are thoroughly rinsed in de-ionized water followed by a dry release sequence [15].

In order to avoid stiction of processed cantilevers to the substrate or other surfaces, a dry release process is used [15]. The dry release method is based on solidification of a supportive photoresist film followed by oxygen plasma removal. During rinsing of the BHF the de-ionized water is replaced by acetone, which dissolves the resist protection mask. Stiction is prevented by gradual substitution of the acetone with standard photo-resist until the liquid covering the sample is concentrated resist. The resist covered sample is then spin-coated and soft-baked, resulting in a resist layer fully encapsulating the suspended cantilevers. Finally, the cantilevers are dry released using oxygen plasma ashing. During operation, stiction of the cantilevers may occasionally occur but they can be released using an atomic force microscope [16].

3. Results and discussion

For the electron beam lithography process, it is vital to expose the pattern in the nanoarea using the appropriate acceleration voltage and parameters such as dwell time and probe current. Initially the chips were exposed using an acceleration voltage of 35 kV. However, the circuit performance of the chips which were exposed with this high energy electron beam turned out to be significantly affected by the high energy electrons degrading the circuits even after a post-process annealing. For instance, it was demonstrated that the threshold voltages of the circuits were severely altered after exposure. The reason for this behaviour and how to prevent it is currently under investigation. In order to minimize the damage of the circuits, exposures using low energy EBL were made, and the accelerating voltage was decreased to 3 kV. Chips with circuits tested before exposure were then exposed with low energy electron beams and after the lift-off process the circuits were measured again. The tests showed that the threshold voltages of the circuits were unaffected when the chips were exposed by 3 kV electron beams. A major advantage of exposing with low energy electrons is that the electrons will lose most of their energy in the resist layer and thus not reach the underlying substrate. Consequently, the chips were patterned with EBL using an acceleration voltage of 3 kV.

As schematically illustrated in figure 1 there is an approximately 1.9 μm high step between the poly-Si layer and the protection layer for the circuitry. Spin coating with thin resist inevitably produces a thicker bi-layer at the edges of the fabrication area. This complicates low energy electron beam exposure on CMOS chips since the exposure dose needs to be increased at the edges of the nanoarea, without overexposing delicate structures, which are in close vicinity.

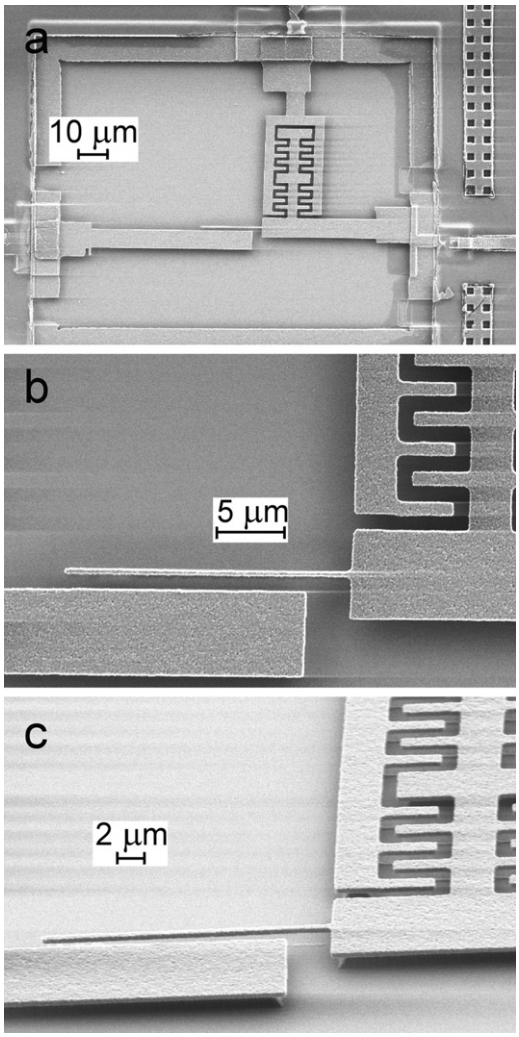

Figure 3. (a) A top view scanning electron microscope (SEM) image showing a fully processed resonator structure. The structures are patterned by 3 kV EBL. In order to pattern the structures at the edges where the resist layer is thicker DWL was used. (b) This top view SEM image shows a released cantilever. Approximate dimensions of the cantilever are: 420 nm wide, 600 nm thick and 20 μm long. It is clearly seen that low energy EBL can generate high resolution structures. (c) The tilted view SEM image shows a cantilever suspended 1 μm above the bottom substrate.

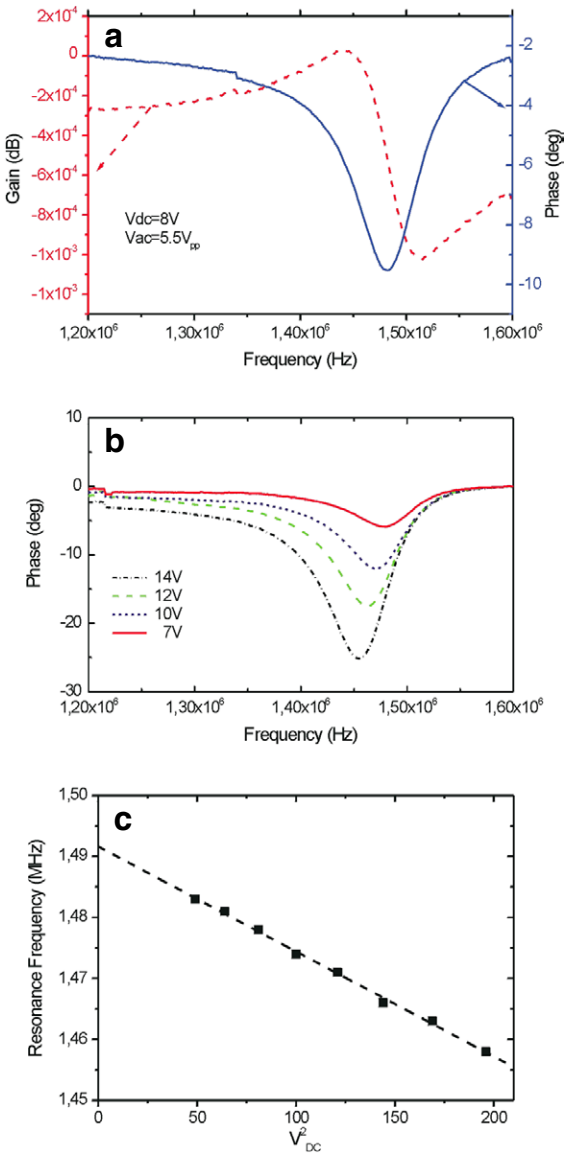

Figure 4. (a) The graph shows the on-chip voltage (gain amplitude and phase) response of a resonating cantilever having a width of 420 nm and a length of 20 μm. The cantilever is driven by 5.5 V AC peak-to-peak and 8 V DC. (b) A set of curves acquired at different DC voltages, from 14 to 7 V DC. (c) The graph shows the dependence on resonance frequency as a function of applied DC voltage. The decrease in resonance frequency when increasing the DC voltage is due to electrostatic spring softening. When extrapolating the measured frequencies to an applied voltage of 0 V DC the inherent resonance frequency of the cantilever is 1.49 MHz.

However, the different nanoareas on the CMOS chips have not exactly the same step heights. The consequence of this height difference is that the resist thickness will not be the same on all chips. Attempts have been made to locally increase the EBL exposure dose at the edges but the results have been inconclusive due to the variation in resist thickness at the edges. Further, since the circuits are sensitive to the electron beams, an increase in exposure dose might also have an effect on the circuit performance. Therefore, investigations in finding a sufficient dose high enough to pattern the edges were not pursued. Hence, when using 3 kV electron beam exposure some nanoareas have an insufficient pattern definition at the edges, as shown in figure 2(c). Unfortunately, it is not possible to detect the poor pattern definition at the edges until after the lift-off process is finished. However, this has been solved by a newly developed direct write laser lithography (DWL) technique [12] applied after the EBL exposure at areas where the pattern definition has been unsatisfactory.

DWL is a lift-off technique based on thermally assisted direct laser writing on substrates coated with a resist bi-layer. Cantilevers have been fabricated by this technique on the CMOS chips [12] but the DWL method is limited to defining lines with dimensions above 500 nm. In this work, the EBL resist bi-layer system was first exposed by EBL and was then patterned by DWL at the edges.

After the DWL patterning in the resist, the CMOS chip was developed (figure 2(d)) according to standard EBL processing,

and metal lift-off was achieved; see figure 2(e). The edge uniformity and the lateral positioning control are excellent between the DWL and the EBL written areas. An optical image of a dry released suspended EBL/DWL defined cantilever is shown in figure 2(f).

An example of a processed suspended poly-Si cantilever is shown in figure 3. The approximate dimensions of the cantilever are 420 nm wide, 600 nm thick and 20 μm long. The theoretical resonance frequency of this system is 1.41 MHz, and the theoretical mass resolution, $\partial m/\partial f$, is 17 ag Hz^{-1}, using a Young modulus value of 160 GPa.

Figure 4(a) shows the on-chip voltage (gain amplitude and phase) response of a resonating cantilever. The cantilever is driven by 5.5 V AC peak to peak to induce the oscillation. An external lock-in amplifier was used in the characterization for noise reduction. Simultaneously, a DC voltage is applied, which allows detection of the displacement current, and in this way the oscillation of the cantilever is translated into an electrical signal [13]. The DC voltage was varied between 7 up to 14 V. The set of curves acquired at different values of a DC voltage, from 14 to 7 V DC, is seen in figure 4(b). Using 14 V DC resulted in the largest resonance signal since the cantilever is pulled closer to the measurement electrode which leads to an increased capacitive current, and the resonance frequency is approximately 1.46 MHz. When using 7 V DC the resonance frequency is 1.48 MHz. The decrease in resonance frequency when increasing the DC voltage is due to electrostatic spring softening, and in figure 4(c) the dependence of resonance frequency on voltage is shown. The extrapolation of the curve to a 0 V DC voltage indicates an inherent resonance frequency of the cantilever of 1.49 MHz. Currently, experiments are performed to deduce the mass sensitivity. The results will be reported elsewhere.

4. Conclusions

We have reported on the fabrication of a resonator directly on a pre-processed CMOS chip. The cantilevers and corresponding driver systems have been defined by a combination of electron beam lithography, and direct write laser lithography, on top of a charge and radiation sensitive CMOS layer in predefined areas. The subsequent etching to fully release the cantilevers has been obtained without stiction of the cantilevers to the substrate.

The detection of the signal directly on the chip radically decreases the parasitic capacitances, which enables low noise electrical measurements with a very high sensitivity. The response of a resonating cantilever when applying different values of a DC voltage shows that the resonance frequency decreases as the voltage increase due to electrostatic spring softening of the system. When extrapolating the measured frequencies to an applied voltage of 0 V DC the inherent resonance frequency of the cantilever is 1.49 MHz. The mass sensitivity of such a system is estimated to be 17 ag Hz^{-1}.

Acknowledgment

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Chapter 13

"Fabrication of cantilever based mass sensors integrated with CMOS using direct write laser lithography on resist"

INSTITUTE OF PHYSICS PUBLISHING NANOTECHNOLOGY
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Fabrication of cantilever based mass sensors integrated with CMOS using direct write laser lithography on resist

E Forsén[1], S G Nilsson[2], P Carlberg[2], G Abadal[3], F Pérez-Murano[4], J Esteve[4], J Montserrat[4], E Figueras[4], F Campabadal[4], J Verd[3], L Montelius[2], N Barniol[3] and A Boisen[1]

[1] MIC—Department of Micro and Nanotechnology, Technical University of Denmark, Bldg 345 East, Ørsteds Plads, DK-2800 Kgs. Lyngby, Denmark
[2] Solid State Physics and The Nanometer Consortium, University of Lund, S-22362, Lund, Sweden
[3] Departamento de Enginyeria Electrònica, Universitat Autònoma Barcelona, E-08193, Bellaterra, Spain
[4] Institut de Microelectrònica Barcelona, Campus Universitat Autònoma Barcelona, E-08193, Bellaterra, Spain

E-mail: ef@mic.dtu.dk (E Forsén)

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Abstract
A CMOS compatible direct write laser lithography technique has been developed for cantilever fabrication on pre-fabricated standard CMOS. We have developed cantilever based sensors for mass measurements in vacuum and air. The cantilever is actuated into lateral vibration by electrostatic excitation and the resonant frequency is detected by capacitive readout. The device is integrated on standard CMOS circuitry. In the work a new direct write laser lithography (DWL) technique is introduced. This laser lithography technique is based on direct laser writing on substrates coated with a resist bi-layer consisting of poly(methyl methacrylate) (PMMA) on lift-off resist (LOR). Laser writing evaporates the PMMA, exposing the LOR. A resist solvent is used to transfer the pattern down to the substrate. Metal lift-off followed by reactive ion etching is used for patterning the structural poly-Si layer in the CMOS. The developed laser lithography technique is compatible with resist exposure techniques such as electron beam lithography. We demonstrate the fabrication of sub-micrometre wide suspended cantilevers as well as metal lift-off with feature line widths down to approximately 500 nm.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The demand for sensors with increased sensitivity, new improved functionality, and reduced analyte usage as well as reduced fabrication costs is driving the development of sensors from the micro- to the nano-regime. The advances of nanotechnology have enabled the development of a variety of novel electrochemical biosensors, e.g. admittance spectroscopy based sensors using nanoelectrodes [1] and electrochemical DNA sensors [2]. Also, mechanical sensors are moving into the nano-regime. Microcantilevers have been widely used for sensor applications, often based on the detection of surface stress changes as response signal. A static cantilever deflection is mostly detected optically [3]

and piezoresistively [4, 5] and the fabrication process is known from AFM cantilever fabrication. Further minimization of such static cantilever systems would encounter several obstacles. For example, the optical detection set-up would become complicated due to the alignment and focusing of the laser beam on a nanometre sized cantilever. Nanocantilevers with integrated piezoresistors would be a challenge to fabricate due to the small feature sizes. Hence, these approaches would not easily lead to any cheap and compact nanomechanical sensor device for commercialization. Furthermore, the mechanism causing surface stress changes upon molecular adsorption on the cantilever surface is still not fully understood.

However, cantilevers can also be operated in the dynamic mode where a mass change is monitored as a change in the resonant frequency of the cantilever. These systems can benefit significantly from minimization. Adsorption or deposition of a compound on a vibrating object can be detected by monitoring the resonant frequency shift due to the added mass. Quartz crystal micro-balance sensors [6] are based on this dynamic principle and can achieve nanogram mass sensitivity.

We want to achieve attogram sensitivity or beyond, using dynamic mode cantilever sensors. For a cantilever with a rectangular cross section a simple harmonic oscillator model can be applied to describe the resonant frequency according to [7],

$$f_0 = \frac{1}{2}\sqrt{\frac{k}{m^*}} \tag{1}$$

where f_0 is the cantilever resonant frequency, k is the spring constant and $m^* = nm$ is the effective mass of the cantilever, where m is the mass and n is a geometrical parameter derived from the Euler–Bernoulli beam equation [8]. Hence, an estimate of the mass resolution can be achieved by assuming that the added mass is uniformly distributed on the cantilever as well as that the spring constant is unaffected,

$$\delta m = \frac{k}{4\ ^2 n}\left(\frac{1}{f_0 - \triangle f\ ^2} - \frac{1}{f_0^2}\right) \tag{2}$$

where δm is the minimum detectable mass and $\triangle f$ is the resonant frequency shift due to the added mass. Linear approximation of the above formula leads to a simple expression for the mass resolution according to [11],

$$\frac{\delta m}{\delta f} \cong 0.211\frac{k}{f_0^3} \tag{3}$$

where δf is the frequency resolution. In order to deduce the adsorbed mass, only the magnitude of the resonant frequency shift and the value of the resonant frequency need to be determined. Furthermore, one can conclude that increasing the resonant frequency while keeping the spring constant fixed leads to increased mass sensitivity. This can be achieved by simply reducing the cantilever dimensions. Hence, in order to have the highest possible mass sensitivity, nanocantilevers need to be fabricated. Table 1 illustrates how the mass sensitivity can be improved by minimizing dimensions. The cantilever dimensions in the first row are similar to an atomic force microscope cantilever having a quite low resonant frequency. The second row corresponds to a cantilever structure similar to cantilevers presented in this work. Such a design would not be far from having attogram mass sensitivity.

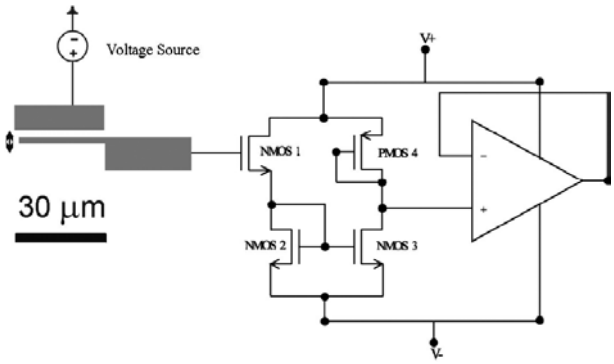

Figure 1. Schematic image of the cantilever system design and a circuit diagram. The sensor principle is based on electrostatic excitation of the cantilever into lateral vibration and capacitive read-out of the resonant frequency as a function of deposited mass. The diagram shows the current amplification and current to voltage conversion of the CMOS.

Table 1. Theoretical mass resolution as a function of cantilever dimensions. The spring constant is 1 N m^{-1}.

Width (nm)	Height μm	Length μm	f_0 (MHz)	$\frac{\delta m}{\delta f}$ g Hz^{-1}
3000	40	242	0.05	1.6×10^{-12}
700	0.7	21.2	2.08	2.3×10^{-17}
100	0.5	2.8	17.65	3.8×10^{-20}

The final row corresponds to a nanocantilever design, having in theory close to zeptogram mass sensitivity. However, the last design would not be appropriate since the resonant frequency would not be electrostatically detectable using the present CMOS design. This is because the operational frequency range is lower than the nanocantilever resonant frequency. The operational frequency range extends up to approximately 2 MHz, which corresponds to a cantilever design such as in row 2 in table 1.

Other groups [9, 10] have developed nanocantilever systems but these systems need low temperature, high magnetic fields or complicated laser Doppler shift detection. By these approaches it is thus not straightforward to realize compact systems.

In this paper the fabrication of a cantilever based mass sensor fully integrated on CMOS circuitry is presented. The finalized device is compact, the process sequence is batch process compatible, and the device could in the future be used as a component in a portable system. The principle of the system is schematically shown in figure 1. By applying an AC and a DC voltage between a suspended cantilever and a parallel electrode the cantilever can be excited into lateral vibration [11]. When the cantilever mass is changed, e.g. by adsorption of molecules, the reduced resonant frequency is measured by the capacitance change between the cantilever and the parallel plate electrode. The capacitance between the cantilever and electrode induces a very small current signal, which makes it necessary to minimize the parasitic capacitance contribution. This makes CMOS integration crucial. CMOS integration is used for signal amplification as well as conversion of the capacitive current signal into a measurable voltage output. CMOS integration can add

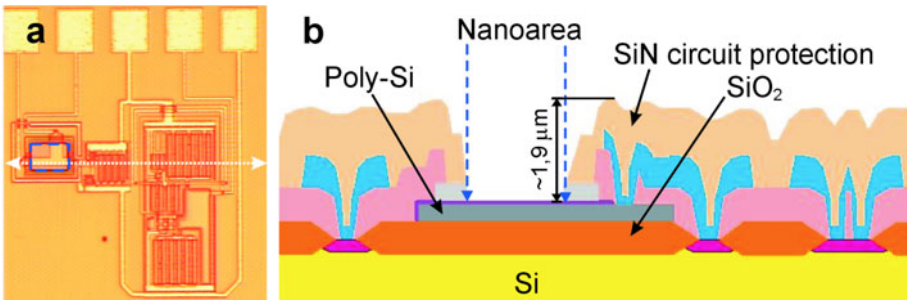

Figure 2. (a) An optical image showing a lithography area on a CMOS chip. The area for definition of the cantilever, dark dotted square, is typically 100 × 100 μm^2. (b) Schematic illustration of the different layers on the CMOS chip, white dotted line in (a). A hole has been etched down to the poly-Si layer in order to enable patterning in the so-called nanoarea. The poly-Si is approximately 600 nm thick and the SiO_2 layer is approximately 1 μm thick. The circuitry protection consists of PECVD oxide and PECVD nitride.

Table 2. CMOS lithography comparison. The resolution should be interpreted as the minimum line width obtained in the metal mask layer.

Lithography method	Resolution	Metal (nm)	Patterning time[a] (h)	CMOS compatibility
EBL	10 nm $\leqslant x$	30–50	3.5	Possible damage
AFM	10 nm $\leqslant x$	6–8	7	No damage
Laser annealing	600 nm $\leqslant x$	6–8	1	No damage
Laser ablation (DWL)	500 nm $\leqslant x$	30–50	1.5	No damage

[a] The patterning time has been approximated for structuring 20 100 × 100 μm^2 areas including pre-handling time.

functionality to the sensor, in terms of frequency tracking and Q-factor enhancement [12–14].

1.1. Overview of lithography techniques

Previously, technologies such as electron beam lithography (EBL), atomic force microscopy lithography (AFM-L), and local laser annealing of 6–8 nm thin Al layers have been evaluated for the fabrication of nanocantilevers on standard CMOS [15, 16]. Their fundamental properties are summarized in table 2. The techniques are different in terms of resolution and throughput. When performing EBL processing on CMOS typically a 30–50 nm thick metal mask is defined by lift-off. This metal layer thickness is optimal for pattern transfer to a structural poly-Si layer using anisotropic reactive ion etching (RIE). However, CMOS compatibility is an issue. Electron beam induced irradiation damage on thin gate oxides degrading the functionality of the CMOS is for example a problem [17]. This has been experienced for e-beam acceleration voltages between 10 and 35 kV [15]. It takes approximately 5 min to expose a design as schematically shown in figure 1. A CMOS chip typically contains 20 resonator structures. Writing 20 structures including 2 h of pre-handling (alignment etc) will result in a total processing time of roughly 3.5 h.

AFM-L enables very high resolution pattern generation and instant lithography result monitoring but necessitates a clean surface with a roughness below 2–3 nm. AFM-L is based on the local oxidization of 6–8 nm thick Al layers. AFM-L of a thin Al film on a poly-Si layer is very difficult due to tip wear and tip hopping. The oxidization of a design as in figure 1 takes roughly 10 min. Writing 20 structures with 10 min of system stabilization time in between, including 30 min of pre-handling, will result in a total processing time of roughly 7 h.

Laser annealing of 6–8 nm thick Al layers has previously been used proving the CMOS compatibility of laser lithography based technologies [18]. The technique enables rapid patterning (a whole chip with 20 structures takes approximately 1 h to pattern), but large numbers of pin-holes can be produced when patterning poly-Si. This is because the optimal Al thickness which can be used for oxidization is comparable to the poly-Si surface roughness. Thin metal masking results in large numbers of pin-holes and hence unsuccessful RIE pattern transfer. This drastically reduces the throughput of working devices. Hence, the desired lithography technique should allow fabrication of metal masks thicker than 20 nm to avoid pin-holes and should be fast and flexible. In this paper we present such a technique, which is introduced in the following section.

1.2. DWL on CMOS

We present a CMOS compatible direct write laser lithography (DWL) technique based on local laser writing of a resist bi-layer and subsequent metal lift-off. The technique enables fast and flexible metal masking. The technique can produce thick metal masks with sub-micrometre line widths over cm^2 areas. DWL is performed as a post-process step on pre-fabricated CMOS chips. The CMOS technology is a standard twin-well, two-poly-Si two-metal technology. The size of the lithography area is typically 100 × 100 μm^2 as shown in figure 2(a). The cantilever is fabricated out of the bottom poly-Si CMOS layer, shown in figure 2(b), which is B^{++} doped.

2. Process

An argon ion laser is used for DWL. The laser is tuned to = 488 nm. Optics allow the laser beam to be focused to an optimal spot size of approximately 500 nm [19]. A CCD camera is used for alignment of the laser beam on the sample, enabling lateral control with a precision of a few micrometres. The lithography pattern is generated by moving the substrate

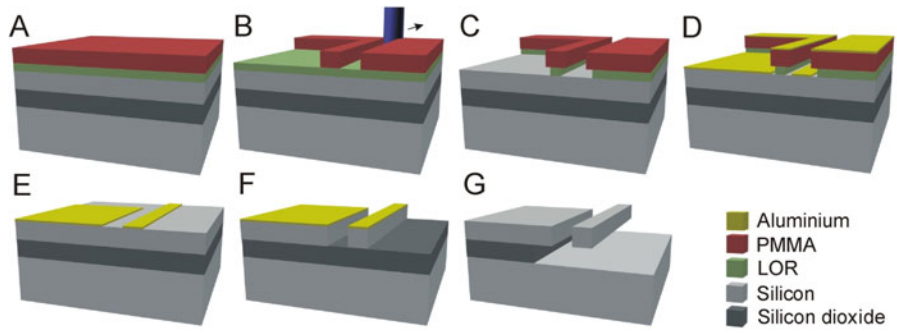

Figure 3. Schematic image describing the process steps involved in lift-off based laser lithography. (a) CMOS chips are coated with a resist bi-layer consisting of PMMA on LOR. (b) Laser lithography thermally removes PMMA and partly also LOR. (c) Oxygen ashing removes possible PMMA residues within structures followed by isotropic dissolution of LOR using MF 319, creating a desired undercut profile. (d) Thermal deposition of Al (Cr has also been used). (e) Warm acetone is used to dissolve the PMMA. Warm Remover PG is used to dissolve the LOR. (f) Pattern transfer to the Si by SF_6:O_2 reactive ion etching. (g) Isotropic etching of the SiO_2 layer using BHF followed by rinsing and spin-coating with photo-resist acting as supporting layer. Finally, the cantilever is released by an oxygen plasma etch removing the photo-resist.

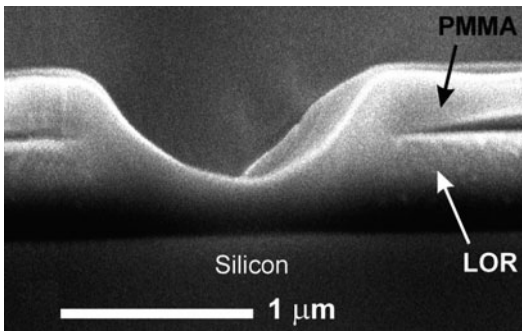

Figure 4. SEM image of a cross section of PMMA/LOR bilayer on plain Si after laser writing. A trench with a Gaussian-like profile is formed in the 300 nm thick PMMA on the 700 nm thick LOR.

on an x–y stage. The x–y stage is set so that the minimum distance between consecutive lines/spots is 500 nm.

As shown in the schematic process illustration in figure 3, the CMOS chips are coated with LOR and hard baked on a hot-plate at 220 °C for 20 min. Next, the CMOS chips are coated with PMMA and baked at 180 °C for 20 min (figure 3(a)). An optimal bi-layer thickness composition of 120/80 nm (PMMA/LOR, measured by ellipsometry) was chosen for the patterning. The laser beam is turned on and off synchronized with the motion of the stage and patterns are defined through thermal evaporation of the bi-layer (figure 3(b)). Figure 4 shows a cross-sectional image of a laser exposed bi-layer. The evaporation of the bi-layer resulted in a Gaussian profile of the resist. The important parameters are the laser power and the spot dwell time (writing speed). The laser spot power can be varied between 10 and 300 mW and the dwell time can be varied from 0.5 to 50 ms. After the exposure the CMOS chips are treated with oxygen ashing (99 sccm O_2:20 sccm N_2, 30 W, 80 mTorr for 20 s) using an *STS* reactive ion etcher, in order to remove PMMA residues, which would hinder the development of the LOR (figure 3(c)).

In order to transfer laser written patterns to the structural poly-Si layer the LOR is dissolved with diluted developer MF 319 (*Shipley*) (figure 3(d)). MF 319 is mixed with deionized water to give a desired dissolution rate of tenths of a nanometre per minute. A slow dissolution process enhances control of the necessary undercut profile and prevents over-development, in which case the PMMA layer might collapse or break apart. The LOR is dissolved isotropically, hence creating a lower boundary on the minimum distance between lines. This is an inherent property of the wet-etch process and a distance of at least 1.5 times the vertical resist thickness is needed between structures. This limits the minimum line separation to 300 nm, for the resist composition used for cantilever fabrication.

Metal deposition was carried out by thermal evaporation of aluminium or chromium (figure 3(e)). The lift-off process is carried out in two steps. First, a warm acetone bath is used to expand and dissolve the PMMA (figure 3(f)). This will create cracks in the metal layer on top of the PMMA and start an initial lift-off. The LOR is unaffected by the acetone and will thus prevent metal flakes from adhering to the silicon substrate. Subsequently, warm Remover PG (*MicroChem*) dissolves the LOR layer and remove the remaining metal (figure 3(g)). The metal mask is used as an etch mask when performing anisotropic RIE (30 sccm O_2:10 sccm SF_6, 35 W, 80 mTorr for 7 min), transferring the design to the structural poly-Si layer. The cantilevers are released from the substrate by an isotropic wet etch of the SiO_2 layer, using hydrofluoric acid (HF), followed by thoroughly rinsing in de-ionized water.

The CMOS chips are not allowed to dry at any point during the rinsing steps after the etching of the SiO_2 layer. This is due to stiction related problems caused from capillary forces acting on the suspended cantilever by the dehydration of water menisci. Stiction is circumvented by using a dry release method [20]. The CMOS chip (still covered by water) is placed in acetone, after which standard photo-resist (AZ 5214E, *Clariant*) is applied until the liquid covering the sample is concentrated resist. Next, the resist covered sample is spun at 3000 rpm for 30 s and subsequently soft-baked at 90 °C, resulting in a 1.7 μm thick resist layer fully encapsulating the suspended nanocantilever. Finally, the cantilevers are dry released using oxygen ashing (99:20 sccm O_2:N_2, 30 W, 80 mTorr for 15 min) of the photo-resist support.

3. Results and discussion

The developed DWL technique has enabled patterning with 30–40 nm thick Al and Cr metal masks on standard CMOS

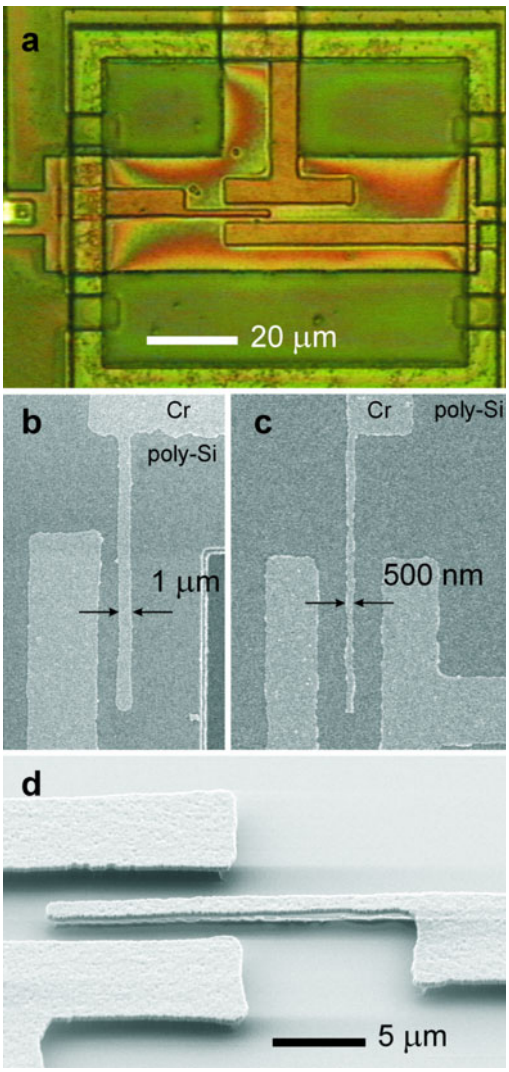

Figure 5. (a) Optical image showing a cantilever design after laser exposure of 120/80 nm thick PMMA/LOR. Laser writing, oxygen plasma ashing, and development of the LOR has opened windows through the bi-layer down to the structural poly-Si layer. (b) SEM image showing a 30 nm thick Cr mask after lift-off. The line width is approximately 1 μm. The mask was written using 55 mW at a writing speed of 0.05 mm s^{-1}. (c) SEM image showing an approximately 500 nm wide cantilever Cr mask. The mask was written using 40 mW at a writing speed of 0.05 mm s^{-1}. The line edge roughness is approximately 100 nm which is partly due to the mechanical resolution of the x–y stage. Minor rip-off is evident. (d) Tilted-view SEM image showing a suspended cantilever fabricated by DWL on CMOS. The fabricated cantilever has a width of approximately 900 nm and a length of 20 μm.

chips, as shown in figure 5. The DWL generated resist mask can clearly be seen using an optical microscope (figure 5(a)). The mechanical resolution of the x–y stage is 100 nm and explains the edge roughness but minor rip-off is also evident as seen in figure 5(c). The DWL method enables metal lift-off with minimum line widths of 500 nm. By increasing the power slightly the line width can be tuned from 500 nm up to several micrometres. By tuning the anisotropic RIE process parameters for the pattern transfer to the structural poly-Si layer the line width could be reduced further.

Figure 5(d) shows a 900 nm wide, approximately 600 nm high and 20 μm long fully suspended poly-Si cantilever fabricated by DWL on CMOS. Using a Young's modulus of 160 GPa and a density of 2330 kg m^{-3} for the poly-Si cantilever shown in figure 5(d), a calculated spring constant of 2.2 N m^{-1} is deduced. The resonant frequency is calculated to be approximately 3 MHz and hence the mass sensitivity would ideally be 1.7×10^{-17} g Hz^{-1}. Previous characterizations of similar poly-Si cantilevers without CMOS have shown quality factor values of $Q_{\text{air}} = 70$ [7] and $Q_{\text{vacuum}} = 28\,000$ [21].

DWL limits the minimal cantilever width to 500 nm, and a 600 nm high and 14.4 μm long cantilever, having a spring constant of 1 N m^{-1}, would have a resonant frequency of approximately 3.25 MHz. Hence an ideal mass sensitivity of 6×10^{-18} g Hz^{-1} could be achieved using the developed laser lithography technique. This would require re-designing the CMOS in order to increase the operational frequency range of the electrostatic read-out.

3.1. Combining DWL with EBL

Although the developed DWL technique offers several benefits for CMOS processing there could be some concern regarding the resolution. It seems as if the resolution cannot be improved to go much beyond 500 nm and it will certainly never give the same resolution as for instance EBL or AFM-L. Low energy EBL exposure can be a method to achieve high resolution without irradiation damage of the CMOS. As schematically illustrated in figure 2(b) there is an approximately 1.9 μm step between the poly-Si layer and the protection layer for the circuitry. Spin coating with thin resist inevitably produces a thicker bi-layer at the edges of the structuring area. This complicates low energy EBL since the exposure dose needs to be increased at such edges, without overexposing delicate structures which are in the close vicinity. We have been able to combine DWL with EBL exposure of a resist bi-layer consisting of a 80 nm thick PMMA layer on a 170 nm thick layer of ZEP 520 A7 (*Zeon Corp. Japan*). First, low energy EBL (3 kV, in order to minimize irradiation damage) has been used for exposure on CMOS. Second, DWL has been used for writing holes or 'anchor points', connecting the EBL defined structure to the rest of the CMOS circuitry, using the method previously described. After making the holes in the resist, the CMOS chip has been developed according to standard EBL processing [15] and metal lift-off has been achieved, as shown in figure 6. The edge uniformity and the lateral positioning control is excellent between the DWL and the EBL written areas. Hence, when needed, very delicate nanopatterning on CMOS could be achieved using low energy EBL which thereafter could be connected by DWL. This could increase the throughput and possibly reduce the fabrication costs of high definition EBL made nanodevices since a combination of DWL and EBL could reduce the total patterning time.

4. Conclusion

In conclusion, a DWL technique has been developed for lithography on pre-fabricated CMOS chips. The technique enables fast and flexible lithography using thermal evaporation of a resist bi-layer followed by metal lift-off. DWL is

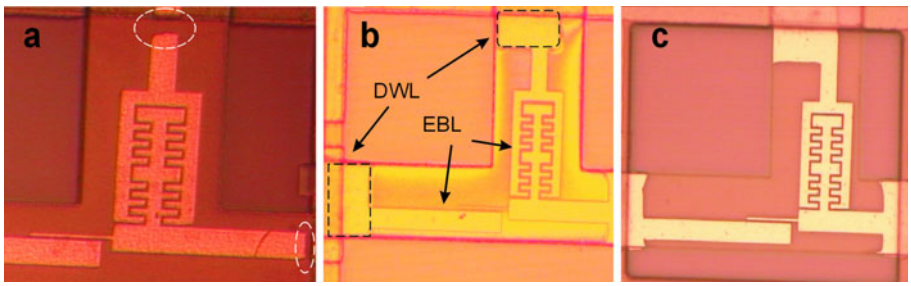

Figure 6. Results of combined DWL and EBL using a resist bi-layer on CMOS. (a) Optical image of typical results of only EBL followed by Al lift-off. Due to the thicker resist layer at the edge of the fabrication area 3 kV e-beam exposure is not enough to fully expose all the resist, resulting in inadequate RIE mask definition at the edges. (b) Optical image after development of the resist after the DWL patterning of rectangular structures onto resist that has been pre-exposed with EBL. (c) Optical image after 30 nm Cr lift-off after combined DWL and EBL. The edge uniformity and the lateral positioning between the DWL and the EBL exposed areas is excellent. The cantilever is 23 μm long and approximately 400 nm wide.

fully CMOS compatible and has been used for fabrication of nanocantilevers on CMOS. The designed system has been optimized for mass measurements and is to be used for biosensing in vacuum and air. Mask definition with line widths down to 500 nm has been shown, and by tuning the anisotropic RIE process parameters the line width could be reduced further. Successful fabrication of suspended cantilevers has been demonstrated, as well as the possibility to combine the technique with EBL exposure of resist. This latter point opens up possibilities in terms of cost reduction and pattern definition flexibility as well as the possibility of patterning radiation sensitive surfaces at low EBL energies. At present, DWL defined cantilever structures are to be characterized and a measurement set-up is being built for molecular immobilization experiments.

Acknowledgments

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Chapter 14

"Dry release of suspended nanostructures"

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Dry release of suspended nanostructures

E. Forsén [a,*], Z.J. Davis [a], M. Dong [a], S.G. Nilsson [b], L. Montelius [b], A. Boisen [a]

[a] *Department of Micro and Nanotechnology, Technical University of Denmark, Bldg. 345 east, Ørsteds Plads, DK-2800, Kgs. Lyngby, Denmark*
[b] *Solid State Physics and The Nanometer Consortium, University of Lund, Sweden*

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Abstract

A dry release method for fabrication of suspended nanostructures is presented. The technique has been combined with an anti-stiction treatment for fabrication of nanocantilever based nanoelectromechanical systems (NEMS). The process combines a dry release method, using a supporting layer of photoresist which is removed using oxygen ashing in a reactive ion etcher (RIE), with CHF_3 plasma induced deposition of an fluorocarbon (FC) film acting as an anti-stiction coating. All in a single RIE sequence. The dry release process is contamination free and batch process compatible. Furthermore, the technique enables long time storage and transportation of produced devices without the risk of stiction. By combining the dry release method with a plasma deposited anti-stiction coating both fabrication induced stiction, which is mainly caused by capillary forces originating from the dehydration of meniscuses formed between suspended structures and the substrate during processing, as well as in-use stiction, occurring during mechanical operation of the system, are avoided.

Keywords: Dry release; Anti-stiction; Suspended nanocantilever; Nanoelectromechanical system

1. Introduction

The possibility to fabricate mechanical devices in the nanometer regime enables development of novel sensor systems. Such nanoelectromechanical sensor systems are commonly fabricated using processing techniques adopted from standard surface micro machining. For instance, metal masking by lift-off techniques, reactive ion etching and wet etching of sacrificial layers has readily been adopted from microelectromechanical systems (MEMS) fabrication for the development of nanoelectromechanical systems (NEMS). However as the dimensions decrease the role of surface physics increases and as a consequence stiction of suspended nanostructures becomes a large problem.

The fabrication of suspended NEMS structures, e.g. nanocantilevers for biosensing purposes [1], are typically released by isotropic wet etching of a sacrificial SiO_2 layer beneath a structural Si layer. Fabricated structures are typically separated by distances of the order of a μm. Hence, there is a large risk of stiction caused by capillary forces originating from the dehydration of meniscuses formed

* Corresponding author.
E-mail address: ef@mic.dtu.dk (E. Forsén).

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between suspended structures and the substrate after complementary rinsing following the wet etching step [2]. Large effort has to be put into the rinsing and drying steps in order to avoid stiction. Methods such as freeze drying [3] or vapor phase hydrofluoric acid (HF) etching [4] prevent meniscus formation. However, these techniques are generally complicated processes with reproducibility issues. Even if the release method has been successful there can be a risk of the structures coming into contact with nearby surfaces during mechanical operation, hence leading to permanent "in-use" stiction due to Van der Waals or electrostatic forces [2].

Here we present a release technique used for nanostructure fabrication, which combines a dry release and an anti-stiction coating. After wet etching of the sacrificial layer the rinsing agents are substituted with standard photoresist. After coating and soft baking, the photoresist acts as a support for suspended nanostructures, as suggested by Orpana et al. [5]. Here we demonstrate that such a dry release method can be implemented in NEMS production. It is shown that the release technique does not damage structures of nanometer dimensions. Furthermore, it is contamination free which is important for the fabrication of sensor systems. Another benefit is the possibility to store and transport a fabricated device without the risk of stiction induced by electrostatic interaction or mechanical chock.

The photoresist is removed using RIE in a oxygen plasma. In addition, in order to reduce in-use stiction after dry release, structures have been treated with a CHF_3 plasma which deposits a fluorocarbon (FC) film acting as an anti-stiction layer. Plasma deposited FC films have previously been used as anti-stiction layers and have shown excellent anti-stiction properties [6]. Moreover, plasma deposition has shown to produce thin FC film thicknesses of the order of a few nm [7], which is highly desirable in NEMS production.

2. Experimental

The combined dry release and anti-stiction treatment has been used for the fabrication of nanocantilever based NEMS integrated on complementary metal oxide semiconductor (CMOS) chips [8]. Nanocantilevers have been fabricated out of the poly-Si layer of the CMOS. Beneath a 600 nm thick structural poly-Si layer lies a 1 μm thick sacrificial SiO_2 layer.

The process steps are schematically described in Fig. 1. The cantilevers are defined by anisotropic RIE of the poly-Si layer using an electron beam lithography (EBL) defined Al etch mask. The cantilevers are released from the substrate by an isotropic wet etch of the sacrificial SiO_2 layer, using HF, and thoroughly rinsed in de-ionized water. The sample is not allowed to dry at any point during the rinsing/coating process. Subsequently, the sample is placed in acetone, after which AZ 5214E photoresist (*Clariant GmbH*) is applied until the liquid covering the sample is concentrated resist. The resist covered sample is then spun at 3000 rpm for 30 s and subsequently soft-baked at 90 °C, resulting in a 1.7 μm thick resist layer fully encapsulating the suspended nanostructures, as shown in Fig. 2(a). By inspection with an optical microscope of the focal plane of the cantilever, compared to the electrodes, one can determine if the cantilever indeed is freestanding.

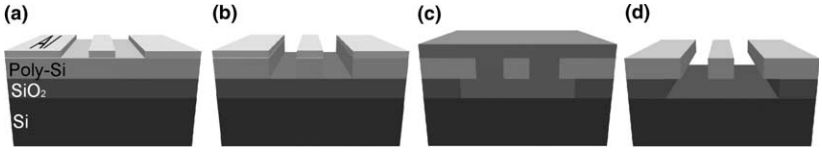

Fig. 1. Schematic description of the process steps involved in the dry release method of suspended MEMS/NEMS structures. (a) A 30 nm thick Al metal mask has been deposited on a poly-Si/SiO_2/Si substrate using EBL, (b) The Al mask is used as an etch mask for anisotropic RIE of the poly-Si, (c) BHF is used for isotropic wet etching of the SiO_2 followed by rinsing with DI-H_20, the water is replaced by acetone after which AZ 5214E photoresist is applied until the final liquid covering the sample is concentrated resist. The sample is spun and soft-baked at 90 °C. (d) The sample is treated with oxygen ashing, removing all resist after which a CHF_3 plasma is used for the deposition of an anti-stiction coating consisting of a FC film.

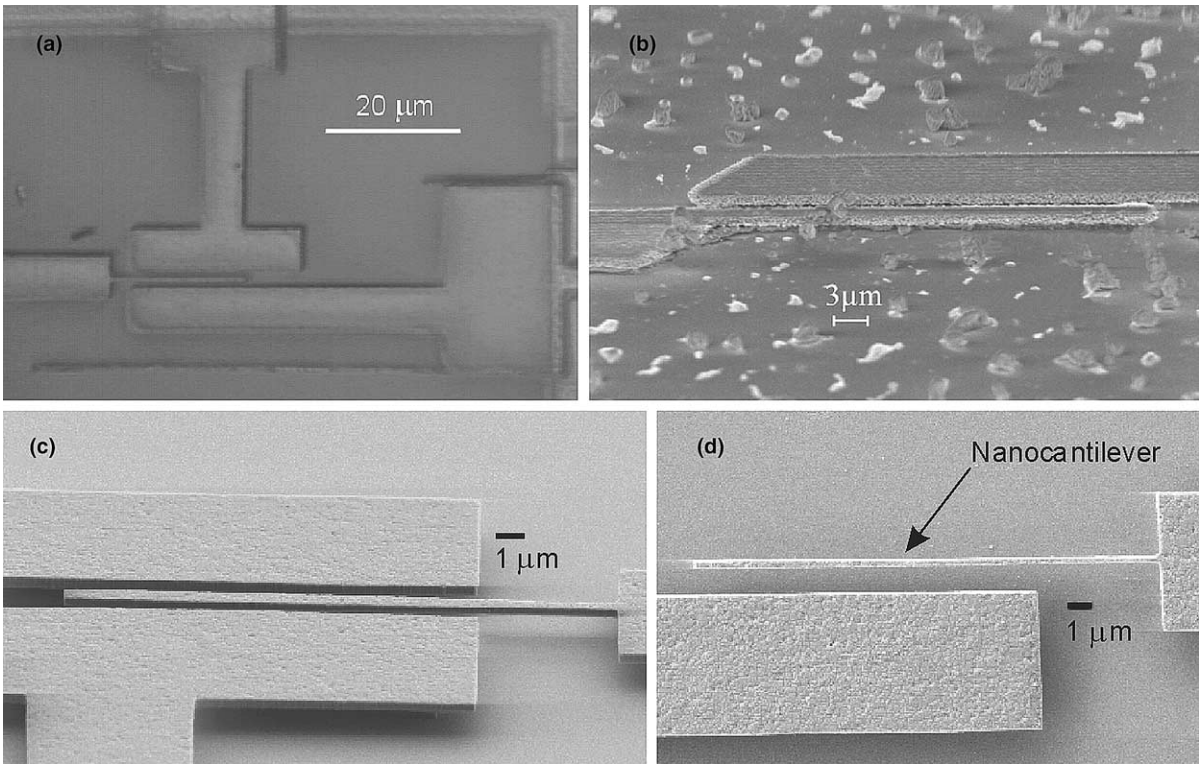

Fig. 2. (a) Optical image showing a suspended nanocantilever structure integrated on a CMOS chip. The nanocantilever is suspended between two electrode structures used for electrostatic actuation as well as capacitive read-out. The nanocantilever is fully encapsulated in resist and is not sticking, (b) SEM image of a nanocantilever structure released by freeze drying. A large amount of contamination is evident, (c)–(d) SEM images showing nanocantilever structures fabricated using the dry release method and anti-stiction coating. The cantilevers are 30 μm long with a line width of roughly 450 nm [(c) top view] and 600 nm [(d) tilted view], the line width is increased at the cantilever end-point due to EBL proximity effects. The cantilever thickness is 600 nm and the gap between the cantilever and the substrate is 1 μm.

The structures are dry released using oxygen ashing (99:20 sccm O_2:N_2, 30 W, 80 m Torr for 15 min) in a RIE. Next, a thin hydrophobic FC layer is deposited without removing the device from the RIE, using a CHF_3 plasma (40 sccm CHF_3, 30 W, 40 m Torr for 2 min), after which the structures are fully released and freestanding as shown in Fig. 2(c)–(d). The FC deposition was adopted from a CHF_3 plasma process optimized for FC passivation of Si surfaces in anisotropic RIE.

3. Results

By using the combined dry release method and anti-stiction coating the fabrication through-put has increased significantly compared to when freeze drying is used. One of the problems with the freeze drying technique is the risk of contamination. Fig. 2(b) shows an example of a cantilever structure with large amount of contaminants on the surface after freeze drying. This is highly undesirable for the production of any sensor system and becomes a critical issue when the contaminating particles and the dimensions of the mechanical sensor system are of the same size. The contaminants might be induced by contamination of the freeze drying liquid with water or other chemicals.

In contrast to freeze drying, the developed dry release and anti-stiction treatment has never displayed sign of contamination.

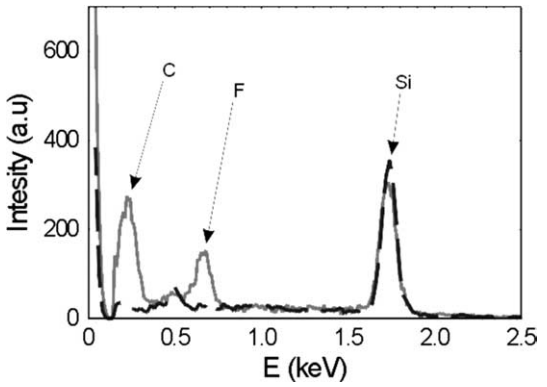

Fig. 3. X-ray emission spectra acquired with EDS inside a SEM, using a 3 keV electron energy. The CHF_3 plasma treated sample (grey solid line) shows a clear fluorine signal at 0.69 keV and the carbon signal at 0.28 keV, compared to the un-coated reference sample (black dotted line) which only shows the Si signal at 1.74 keV.

X-ray emission spectroscopy was used for the confirmation of the existence of the FC film. X-ray emission spectra acquired with energy dispersive spectrometry (EDS) inside a scanning electron microscope (SEM) using 3 keV electrons show a clear fluorine signal at 0.69 keV and a carbon signal at 0.28 keV as shown in Fig. 3. An untreated Si reference sample does not display these peaks, confirming the existence of the FC coating.

Ellipsometry was not a viable way to measure the FC film thickness due to the very thin coverage. Similar FC plasma coatings have previously been examined by X-ray photoelectron spectroscopy (XPS) and revealed a film thickness of about 5 nm [7].

4. Conclusion

In conclusion we have successfully developed a dry release method with anti-stiction treatment, having greater reproducibility than freeze drying as previously used for the fabrication of NEMS. The technique is CMOS compatible. The dry release process is robust, fast, contamination free and does not damage mechanical structures of nm dimensions. The resist layer functions as a supporting layer for suspended nanostructures, preventing adhesion due to capillary forces, electrostatic forces and mechanical chock. Nanocantilevers for biosensing have been fabricated using the dry release method in combination with CHF_3 plasma deposition of FC anti-stiction coating. Furthermore, the resist coated device can be transported and stored without concern about stiction and the structures can thereafter be released using oxygen ashing.

Acknowledgements

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Chapter 15

"Laser lithography on resist bi-layer for nanoelectromechanical systems prototyping"

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Laser lithography on resist bi-layer for nanoelectromechanical systems prototyping

E. Forsén [a,*], P. Carlberg [b], L. Montelius [b], A. Boisen [a]

[a] *Department of Micro and Nanotechnology, Technical University of Denmark, Bldg. 345 east, Ørsteds Plads, DK-2800 Kgs. Lyngby, Denmark*
[b] *Solid State Physics and The Nanometer Consortium, University of Lund, Sweden*

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Abstract

We present a laser lithography technique based on lift-off, for fast and flexible prototyping of micro and nanoelectromechanical systems (MEMS/NEMS). The technique is based on direct laser writing on substrates coated with a resist bi-layer consisting of polymethyl methacrylate (PMMA) on lift-off resist (LOR). Laser writing melts and evaporates the PMMA exposing the LOR. Oxygen ashing removes PMMA residues within the lithography pattern. A resist solvent is used to transfer the pattern down to the substrate. The LOR is dissolved isotropically while the PMMA is unaffected by the solvent, hence creating an undercut profile. After metal evaporation a two-step lift-off process prevents metal flakes from adhering to the surface. First, warm acetone dissolves the PMMA and lifts off the metal layer, then warm Remover PG removes the LOR and any remaining metal. Metal structures with line widths down to 600 nm and dots with 600 nm diameters are presented.

Keywords: Laser lithography; Nanoeletromechanical systems; Resist bi-layer; Direct write; Rapid prototyping

1. Introduction

Direct write laser lithography (DWL) is a maskless lithography technique based on localized beam-induced surface modification. Several types of sub-micrometer resolution DWL exists, e.g. annealing of thin metal films [1], etching of Si [2] and deposition [3]. There are commercial direct write systems available claiming minimum feature sizes down to 500 nm [4] using UV laser induced chemical modification of photoresists. Such systems are, however, expensive and mainly used for industrial fabrication of photolithography masks. DWL bridges the gap between nanolithography techniques such as electron beam lithography (EBL), atomic force microscopy-based lithography (AFM-L), both achieving sub 10 nm line widths, and micrometer-resolution photolithography. Here, we present a novel DWL technique using lift-off, enabling sub-micrometer resolution over cm^2 areas. The developed technique is compatible

* Corresponding author.
E-mail address: ef@mic.dtu.dk (E. Forsén).

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with post-processing on complementary metal oxide semiconductor (CMOS) chips. CMOS compatibility is important due to the possibility to fabricate nanoelectromechanical systems (NEMS) on CMOS for the development of compact/portable devices with increased functionality. NEMS are commonly fabricated using lithography techniques such as EBL [5] and AFM-L [1]. Both techniques enable tremendous resolution but are generally expensive, complicated and achieve low throughput. Furthermore, EBL has CMOS compatibility problems due to e-beam irradiation damage caused on thin gate oxides [6]. AFM-L is CMOS compatible but sensitive to surface roughness, hence the structural layer of the CMOS needs to be smooth. Otherwise, tip-wear and tip-jumping will make reproducible lithography impossible. The low throughput of AFM-L is also a hinderance. Previously, DWL based on the local annealing of thin Al films has been investigated for NEMS device fabrication [2]. However, the method was shown not to be applicable on poly-Si based CMOS due to surface roughness of the structural poly-Si layer, being of the same order as the Al film thickness needed for annealing. This lead to bad metal NEMS mask definition with large amounts of pin-holes and defects occurring during processing. CMOS post-processing using thicker metal masks would significantly increase the throughput.

A lift-off based lithography method where a thicker metal layer easily can be achieved has been developed. Substrates coated with a resist bi-layer are locally patterned by a laser beam which evaporates the bi-layer. The process steps involved are schematically displayed in Fig. 1. We use a bi-layer resist method where differences in dissolution rates makes it possible to create an evaporation-mask in the upper resist layer. The bi-layer consists of a top layer of polymethyl methacrylate (PMMA; MicroChem) and a bottom layer of LOR (MicroChem). The laser patterning is due to thermal melting and evaporation of the bi-layer, which results in a trench with a Gaussian profile, as displayed in the scanning electron microscope (SEM) image in Fig. 2. Hence, the bi-layer is necessary in order to have an undercut of the top resist layer, which is desirable for lift-off processes.

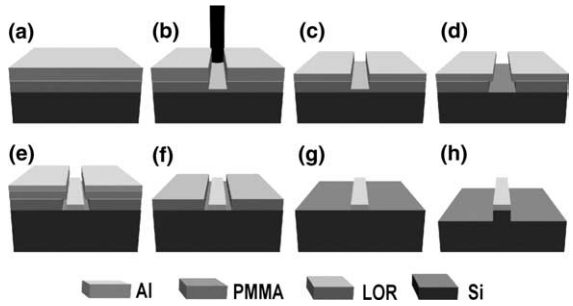

Fig. 1. Schematic image describing the process steps involved in lift-off based laser lithography. (a) Si substrates are coated with a resist bi-layer of PMMA and LOR. (b) Laser lithography, thermally removing PMMA and partly also LOR. (c) Oxygen ashing removes PMMA residues within structures. (d) Isotropic dissolution of LOR using MF 319 creates an undercut profile. (e) Thermal deposition of Al or Cr. (f) Warm Acetone is used to dissolve the PMMA. (g) Warm Remover PG is used to dissolution the LOR. (h) Pattern transfer to the Si by SF_6:O_2 reactive ion etching (this step has not always been used).

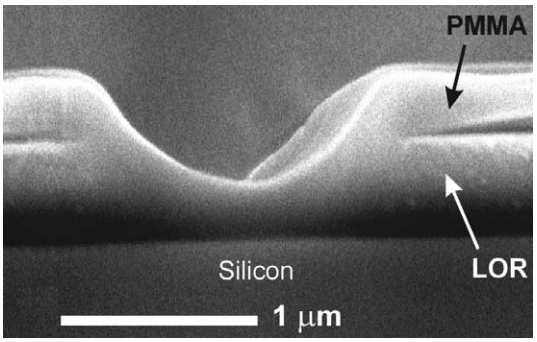

Fig. 2. SEM image of a cross-section of PMMA/LOR bilayer on Si after laser writing; 300 nm PMMA and 700 nm LOR.

The pattern line width can be controlled by varying the laser power, dwell time as well as the thickness composition of the bi-layer. Furthermore, a two-step lift-off process makes the use of ultra sonic agitation unnecessary.

2. Experimental

Structures were fabricated on standard 4-in. silicon wafers. An argon ion laser (Coherent Innova) was used for the lithography, tuned to $\lambda = 488$ nm and maximum power of 1 W. Optics, as described by Boisen, et al. [1], allow the laser

beam to be focused to an optimal spot size of 500–1000 nm. A CCD camera is used for alignment of the laser beam on the sample, enabling lateral control with a precision of a μm. The lithography pattern is generated by moving the substrate on an *x–y* stage (Newport PM 500) with a maximum scan area of 100×100 mm. The *x–y* stage is set so that the minimum distance between consecutive lines/spots is 500 nm. As shown in the schematic process Fig. 1, the silicon substrates are coated with LOR and hard baked on a hot-plate at 220 °C for 20 min. Next, the substrates are coated with PMMA and baked at 180 °C for 20 min (Fig. 1(a)). Various bi-layer thickness compositions have been investigated, ranging from 300/700 nm to 120/70 nm (PMMA/LOR), as measured by ellipsometry. The laser beam is turned on and off synchronized with the motion of the stage and patterns are defined through thermal evaporation of the bi-layer (Fig. 1(b)). Important parameters are the laser power and the spot dwell time (writing speed). The laser spot power can been varied between 10 and 300 mW and the dwell time can be varied from 0.5 to 50 ms. After exposure, samples are treated with oxygen ashing (99 sccm O_2:20 sccm N_2, 30 W, 80 mTorr for 20 s) using an *STS* reactive ion etcher, in order to remove PMMA residues, which would hinder the development of the LOR (Fig. 1(c)). In order to transfer laser written patterns to the substrate, the LOR is dissolved with diluted developer MF 319 (Shipley) (Fig. 1(d)). MF 319 is mixed with deionized water to give a desired dissolution rate of tenths of nm per minute. A slow process enhances control of the necessary undercut profile and prevents over development, in which case the PMMA layer might collapse or break apart. The LOR is dissolved isotropically, hence creating a lower boundary on the minimum distance between lines. This is an inherent property of the wet-etch process and a distance of at least 1.5 times the vertical resist thickness is needed between structures. Metal deposition was carried out by thermal evaporation of aluminum or chromium (Fig. 1(e)). The lift-off process is carried out in two steps. First, a warm acetone bath is used to expand and dissolve the PMMA (Fig. 1(f)). This will create cracks in the metal layer on top of the PMMA and start an initial lift-off. The LOR is unaffected by the acetone and will thus prevent metal flakes from adhering to the silicon substrate. Subsequently, warm Remover PG (MicroChem dissolves the LOR layer and remove the remaining metal (Fig. 1(g)). Fabricated structures have been examined using SEM and AFM.

3. Results and discussion

The laser written structures typically consisted of 1 mm long line arrays and dot arrays. Arrays of 30 nm thick Cr dots with diameters ranging from 600 nm to 2 μm are displayed in Fig. 3(a)–(d). The dots were written in 300/700 nm thick PMMA/LOR using 15–50 mW laser power and 5 s dwell time. Cr lines with a width of 600 nm and a thickness of 30 nm were achieved using a 120/80 nm PMMA/LOR bi-layer with a laser power of 50 mW and a 50 ms dwell time (scan speed 0.01 mm/s) and are shown in Fig. 3(e). Various bi-layer thicknesses were investigated and it became clear that the smallest line widths were achieved with the thinnest bi-layer compositions investigated, 120/80 nm (PMMA/LOR). The PMMA layer should be so thin that low laser power is needed to open up windows in the bi-layer. Low laser power enables

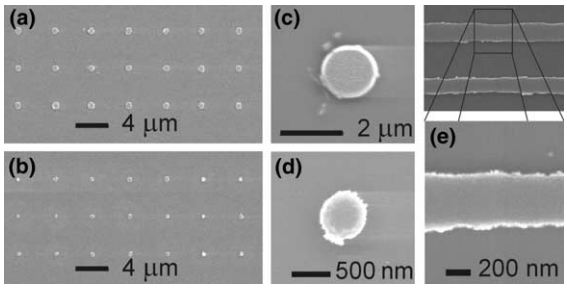

Fig. 3. SEM images of Cr metal dots and lines after lift-off. The laser dwell time for the dots was 5 s. (a and b) 100 nm thick Cr metal dot array having a 5 μm grid, after 300/700 nm thick PMMA/LOR lift-off. (a) Dot array having a 2 μm diameter (50 mW laser power). (b) Dot array having 1 μm diameter (15 mW laser power). (c) A 100 nm thick/2 μm diameter Cr metal dot. (d) A 30 nm thick/600 nm diameter Cr metal dot (30 mW laser power, using 120/80 nm thick PMMA/LOR). (e) Magnification of a 30 nm thick Cr metal line after lift-off using 120/80 nm thick PMMA/LOR (50 mW laser power and a scan speed of 0.01 mm/s). The lines are 500–700 nm wide and 1 mm long. Some resist residues and rip-off is evident in the images.

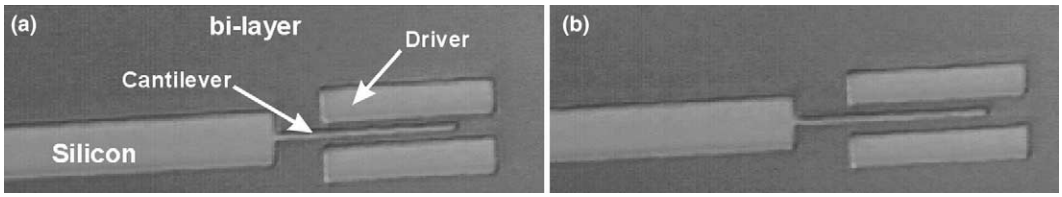

Fig. 4. Optical image showing structures just after laser patterning using 120/80 nm thick PMMA/LOR. The distance between the cantilever structure and the driver structures is set to 1 μm in (a) and 1.5 μm in (b), verifying that the technique can be used for creating complex structures. The cantilever length is 20 μm.

good control over the laser spot size, reducing the width of the Gaussian profile for evaporation. For thick bi-layer compositions lift-off with 100 nm thick Cr has been achieved, and thicknesses of at least 400 nm should be possible. The minimum line width for the thickest bi-layer composition, 300/700 nm PMMA/LOR, was roughly 1 μm. In order to display the flexibility of the technique, 30 nm thick Cr metal masks have been produced for the realization of NEMS. NEMS patterns which are used for fabrication of nanocantilevers for biosensing [7] are shown in Figs. 4 and 5. Fig. 4 shows that the line separation can be made very small without noticeable proximity effects and thus complex structures can be written in close vicinity. Fig. 5 shows that the cantilever line width can be controlled by varying the laser power at constant writing speed. The edge roughness, which is of the order of 100 nm, depends mainly on the mechanical resolution of the x–y stage. This effect can be reduced by increasing the writing speed, but there is a trade-off when increasing the scan speed since then also increased laser power is needed for patterning, which generally results in increased minimum line width.

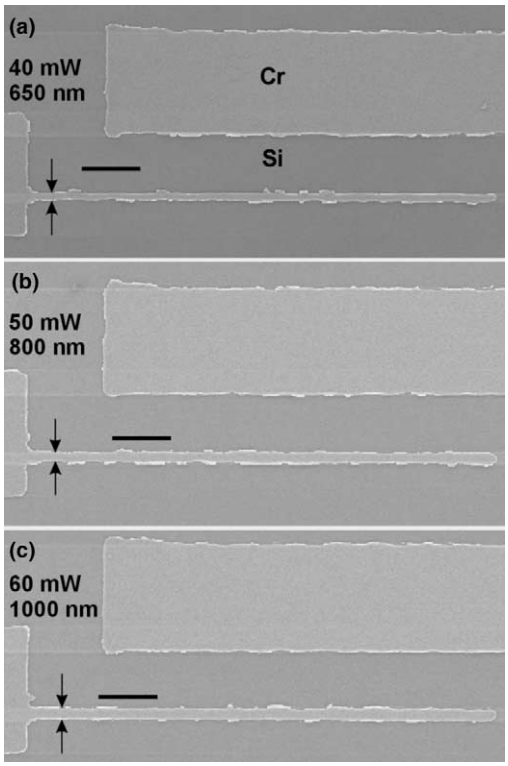

Fig. 5. SEM image showing the difference in line width after 30 nm thick Cr lift-off as function of laser power using an constant writing speed of 0.5 mm/s. The cantilever width is approximately 650 nm in (a), using 40 mW, 800 nm in (b), using 50 mW and 1 μm in (c), using 60 mW. The line edge roughness is roughly 100 nm which is partly due to the mechanical resolution of the x–y stage. The scale bars are 5 μm.

4. Conclusion

We have presented and discussed a laser lithography technique based on bi-layer resist in order to create an undercut profile for lift-off, enabling sub-micron line widths over large areas. The benefits of using lift-off based laser lithography is that the technique is robust, fast and flexible compared to EBL and suitable for NEMS/MEMS prototyping. Moreover, the technique is CMOS compatible. The lift-off process makes it possible to do lithography on rough surfaces (e.g. poly-Si) for which other lithography techniques, e.g. AFM lithography or local laser annealing are not suitable. Lift-off also enables ad-on structural patterning of thick metal. Additionally, it should be stressed that the method does not rely on ultra-

sonic agitation for the lift-off, but rather on a combination of solvents, reducing the risk of damaging fabricated nanostructures and also preventing metal residue adsorbing on the structures during lift-off. Finally, we have shown lift-off results in the shape of Cr dots and lines with a diameter and line width of 600 nm. Also metal masks for NEMS prototyping with the same line widths have been produced.

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Chapter 16

CMOS Post-Process Sequence

1. **Poly0 etch:** The poly0 layer is etched by anisotropic RIE for 7 minutes. Recipe *ef_aniso*: 32:8 sccm SF_6:O_2, p=80 mTorr, P=35W.

2. **HMDS:** The chip is baked in vacuum and HMDS treated for 30 minutes in order to improve the adhesion of the resist.

3. **Resist spin-coating:** AZ5214E is spin-coated at 1500 rpm for 30 seconds. Resulting in a 2.5 µm thick resist layer.

4. **Resist baking:** The resist is baked at 120°C for 1 minute.

5. **Photo lithography:** The chip is exposed for 60 seconds and is thereafter developed for 70 seconds using Nanomass mask1. This opens up holes in the nanoarea for the release wet etch.

6. **BHF underetching:** The 1 µm thick sacrificial $Si0_2$ is wet etched using BHF for 15 minutes at an etch rate of approximately 75 nm per minute.

7. **DI-water rinse:** Thorough rinse in DI-water for 5 minutes. The chip is not allowed to dry out which would cause stiction.

8. **Resist removal:** The chip is thoroughly rinsed with acetone in order to remove the resist mask without letting the chip to dry out.

9. **Release:** See Appendix 17 and 18.

Chapter 17

Freeze Drying

1. **Propanol rinse:** The chip is thoroughly rinsed in propanol without allowing the chip to dry out.
2. **Tert-butanol:** The chip is immersed in liquid tert-butanol which has been heated above the freezing point.
3. **Solidification:** The chip is placed on a ceramic cooling plate and the tert-butanol solidifies.
4. **Evaporation:** The cooling plate is placed evacuated and the solid tert-butanol evaporates slowly for about 1 hour.

Chapter 18

Plasma Release

1. **Acetone suspension:** The chip is placed in a small cup covered with acetone.
2. **Resist rinse:** Liquid resist is applied in large amounts until the liquid covering the chip is concentrated resist.
3. **Resist spin-coating:** The chip is spun at 3000 rpm for 30 seconds followed by baking at 90°C for 1 minute, which results in a 1.7 μm thick resist layer.
4. **Plasma release:** The resist is removed using oxygen plasma in a RIE. Recipe *cant_us*: 99:20 sccm O_2:N_2 for 10 minutes, p=300 mTorr and P=60W.