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***Abstract*— We report on the development of a submicron InP DHBT technology, optimized for the fabrication of ≥50-GHz-clock mixed-signal ICs. In-depth study of device geometry and structure has allowed to get the needed performances and yield. Special attention has been paid to critical thermal behavior. Various size submicron devices have been modeled using UCSD-HBT equations. These large signal models have allowed the design of 50-GHz clocked 50G Decision and 100G Selector circuits. The high quality of the measured characteristics demonstrates the suitability of this technology for the various applications of interest, like 100 Gbit/s transmission.**

I. INTRODUCTION

InP HBT technology has long been identified as a technology of choice for demanding applications, such as high bit-rate optical communications (53-107 Gbit/s), RF communications in higher frequency bands (E, W, G, i.e. 80-200+ GHz), and high bandwidth data conversion, thanks to its unique capability to provide both very high speed and large breakdown voltage. Mimicking Silicon, a roadmap toward higher performances, relying on scaling, has been proposed [1]. Various teams have reported on such advanced technologies [2-3] and on ICs using scaled InP HBTs for digital [4-5], analog [6-9] and data conversion [10-11] applications. Alcatel-Thales III-V Lab has been delivering for some times 40 Gbit/s mixed-signal ICs using its 1.5 µm technology [12]. To address present day applications, in particular 100+ Gbit/s transmission, and deliver ≥50-GHz-clock ICs, development of a submicron process was undertaken.

II. DEVICE OPTIMIZATION

A. Geometry & process optimization

To achieve ≥50 GHz clocking, it appears (rule of thumbs) that the transistor should have Ft/Fmax in the 250-300 GHz range. The vertical structure optimization (layer thickness reduction) and the geometry scaling have to be carefully balanced in order to achieve the expected improvements. To insure yield and process robustness, we have kept the self-aligned 3-mesa approach used in the previous generation. A specific tool (ACPAR-2) has been developed to assess the performance impact of the various – geometry (Figure 1) and structure – parameters.

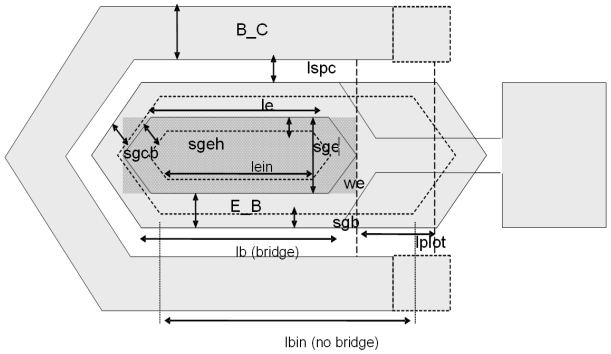

Figure 1: geometry parameters used in ACPAR-2

For example, Figure 2 illustrates the expected F_{MAX} for various underetching (S_{gE}) values, for two base contact width values (W_{cB}), demonstrating how critical this parameter is.

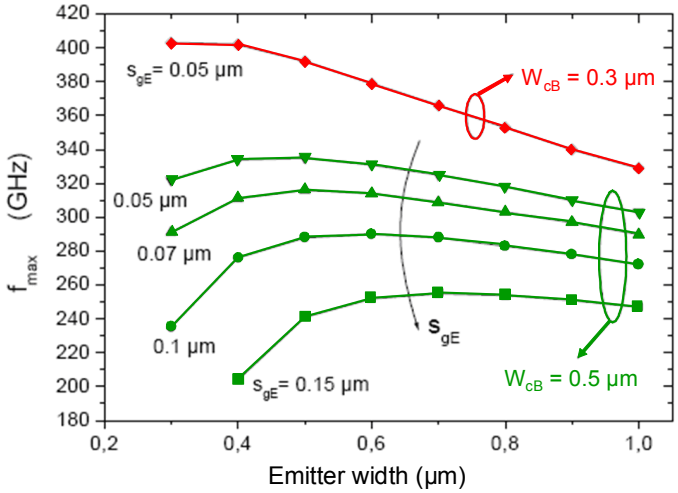

Figure 2: under-etching impact on Fmax, for 2 base contact width values

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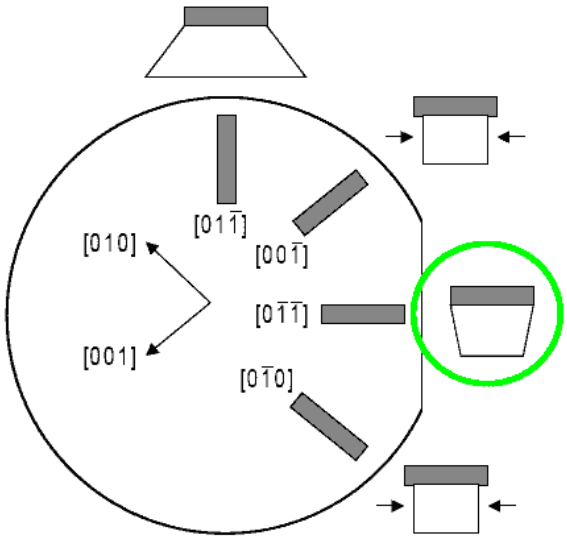

Figure 3: under-etching control w.r.t crystallographic axes

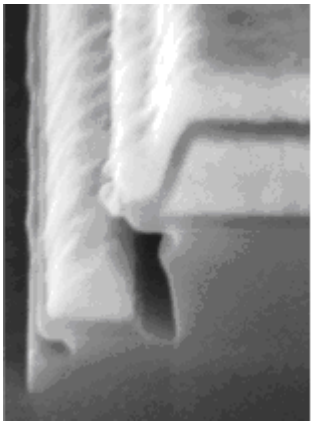

Figure 4: FIB device cut

As etching control is related to crystallographic axes (Figure 3) hexagonal geometry has been chosen with a fixed orientation. Figure 4 shows the device quality achieved through self-alignment and under-etching control.

ACPAR-2 allowed also to compare two approaches to tackle the extrinsic base resistance and collector capacitance problem, the bridge – lower capacitance – and the plug – lower resistance – (Figure 5). Bridge was predicted to yield better frequency performances, which was confirmed by actual measurements (Figure 6). However, less predictable features such as yield and robustness led us to rather use the plug devices for circuit fabrication.

B. Structure optimization

The devices were grown by GSMBE epitaxy; their structure is comprised of a 40 nm Emitter, a $8x10^{19}$ cm^{-3} Carbon-doped 28 nm graded Base and a $5x10^{16}$ cm^{-3} doped 130-250 nm composite Collector.

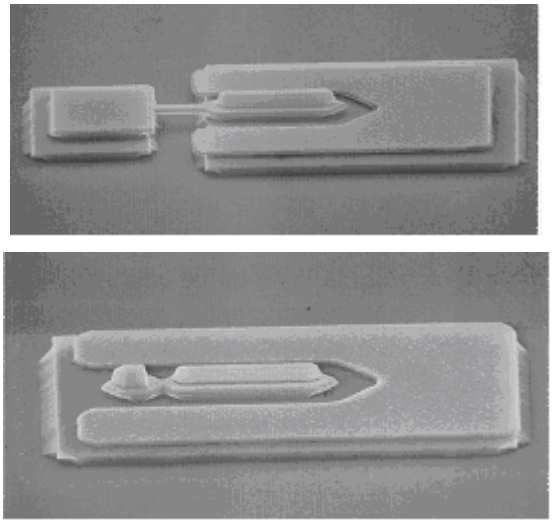

Figure 5: bridge (top) and plug (bottom) device microphotographs

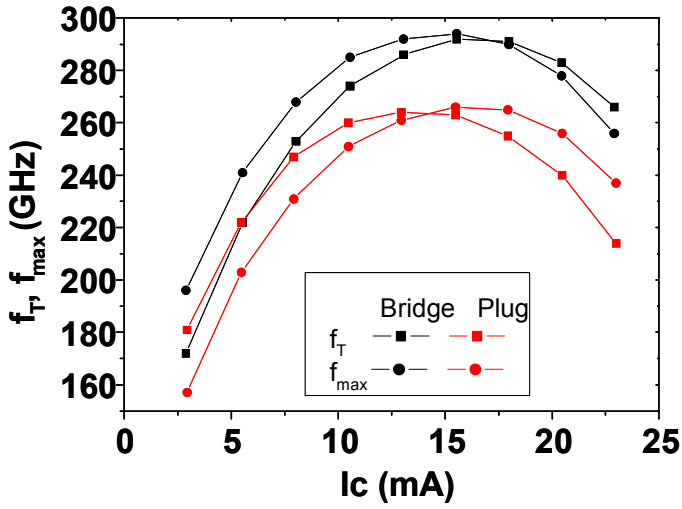

Figure 6: bridge (top) and plug (bottom) device performances

As the major contribution to F_T is the transit time in both Base and Collector, optimization has focused on the base-collector junction; we need to balance short transit time with breakdown voltage [which is a specific advantage of DHBTs], Kirk effect/blocking effect due to conduction band discontinuity and inter-valley scattering (Figure 7). A combination of an InGaAs spacer, a doping plane and quaternaries [13] has allowed to get simultaneously high BV_{CE0} = 4.75V, J_{Kirk} = 9mA/µm², and F_T = 290 GHz.

Thermal effects have been identified as a key issue for advanced HBTs [14]. For our devices, the InGaAs subcollector layer (which serves as both an etch-stop layer and to improve collector ohmic contact) has been identified as the major contributor to temperature rise, due to its poor (5 W/K.m) thermal conductivity. This layer thickness has been optimized [15] to significantly improve thermal behavior (30% overall thermal resistance reduction), while maintaining the frequency performances.

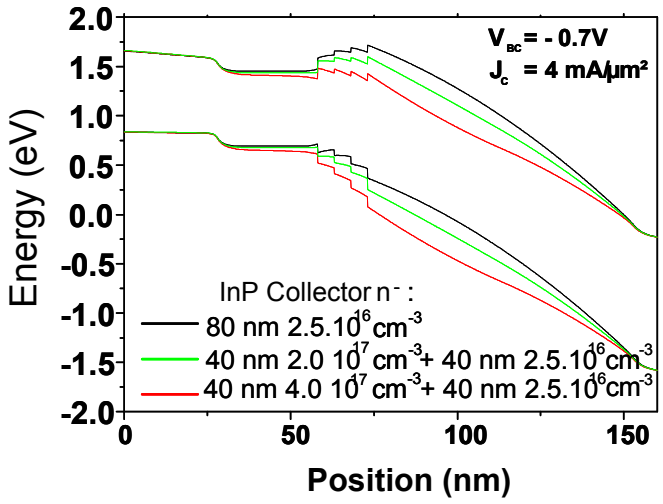

Figure 7: Example of band diagram for collector optimization

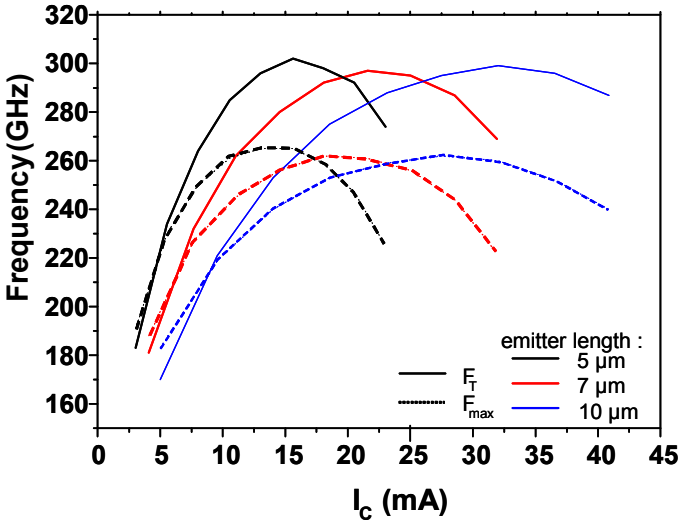

Figure 8: various size HBTs performances

III. Device Fabrication & Performances

As mentioned, a triple-mesa self-aligned process was used. 0.3 µm-wide Base and 0.7 µm-wide Emitter contacts were defined by E-beam lithography, while the other steps rely on optical lithography. Benzocyclobutene (BCB) is used for passivation, isolation and planarization. DC gain is about 20, $BV_{CE0} \cong 5V$, and Ft/Fmax are in the 250-300 GHz range for various (0.7x5-10 µm²) HBT dimensions (Figure 8). These performances are suitable for very high speed large-signal circuits design and fabrication.

IV. Modeling

For accurate circuit simulation, large signal modeling needs to take into account various physical effects specific to InP HBTs, such as forward transit time and base-collector capacitance modulation with bias, and saturation influenced by base-collector heterojunction behavior. Based on the methodology described in [16-18], parameters for an UCSD-like model were extracted from various bias small-signal measurements. Figure 9 illustrates the model accuracy, for both small-signal and C_{BC} modulation.

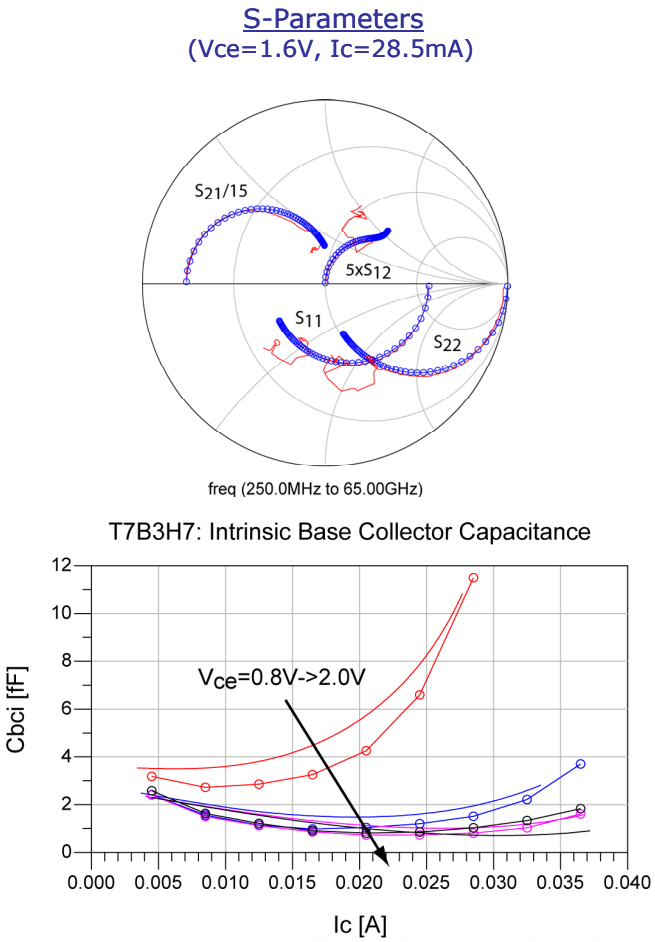

Figure 9: measurements vs. model comparison (rings are for model)

V. IC Design & Characterization

To assess the capability of this technology for 50 GHz clock mixed-signal ICs fabrication, two such circuits were first designed: (i) a 50 Gbit/s (full-rate) decision circuit and (ii) a 100 Gbit/s (half-rate) selector were designed, using the developed models. They are comprised of about 30 transistors of various size (from 5 to 10 µm-long 0.7 µm-wide HBTs).

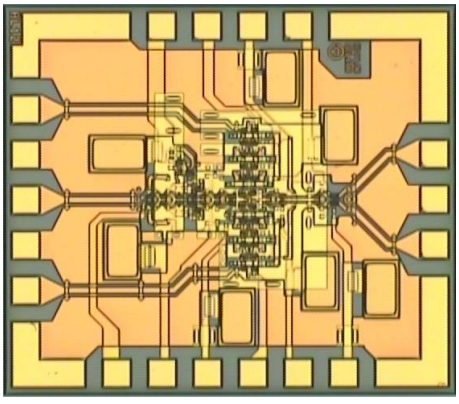

Figure 10: Selector circuit microphotograph

Three different wafers were processed, to assess reproducibility and yield. Good to excellent characteristics were achieved on all wafers, with yield ranging from 40% up

to 80%. Figure 10 show the microphotographs of the 1.4x1.6 mm² selector IC. Both ICs' eye diagrams, which were measured on-wafer, are shown on Figure 11. 50 Gbit/s input signals were provided, based on a commercial 4x12.5 Gbit/s PRBG and an in-house 50 Gbit/s MUX [19], to assess the functional performances of the circuits:

(i) for the decision circuit, the clock phase margin is 10 ps (180°) at 50 Gbit/s [and up to 15 ps (230°) at 43 Gbit/s]; rise and fall times are below 6.5 ps, and (scope-limited) RMS jitter is below 300 fs.

Thanks to the very high quality achieved, improved 100 Gbit/s (based on 50 GBaud modulation formats) transmission experiments are made possible.

(ii) For the selector circuit, 500 mV output swing has been obtained at 100 Gbit/s, with rise time below 6 ps and fall time below 5 ps; RMS jitter is less than 600 fs; vertical and horizontal eye opening are 54% and 66% respectively. This selector is the core of a selector-EML-driver, key building block for a 100 Gbit/s OOK transmission experiment being set up.

The very short rise and fall time, as well as the very low jitter, indicate that still higher than 50 GHz clock may be achievable; combined with the breakdown voltage high value, >100 Gbit/s large-signal ICs may be contemplated, such as a 107 Gbit/s OOK driver.

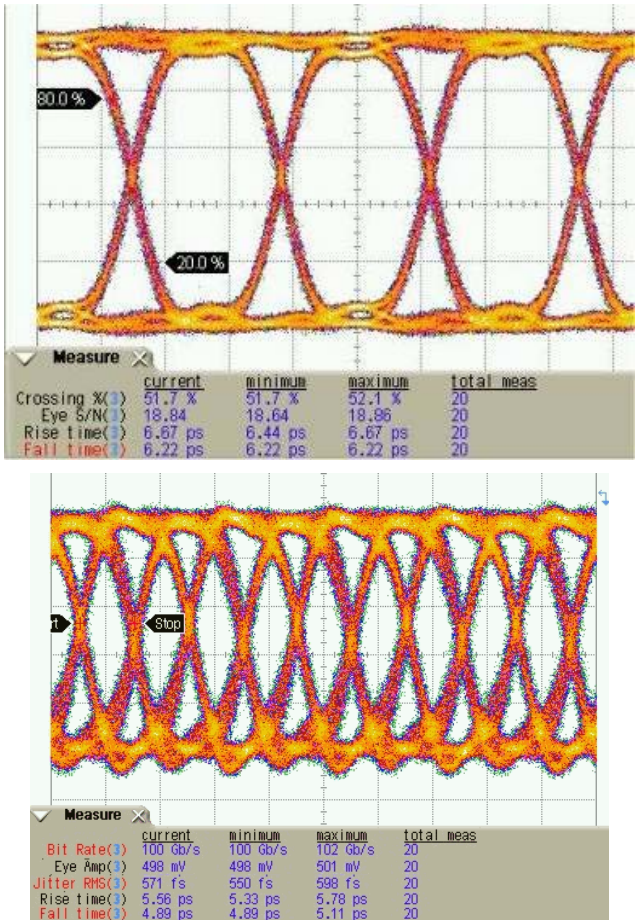

Figure 11: Decision (top) & Selector (bottom) ICs eye diagrams

VI. CONCLUSION

A submicron InP DHBT process has been developed, with special care devoted to structure optimization, thermal effects mitigation, and process robustness. Thanks to accurate modeling, meaningful circuits have been designed which demonstrate the suitability of this process for 100+ Gbit/s transmission, be it OOK or 50 GBaud. The large breakdown voltage will allow to design 107 Gbit/s driver.

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