Microwave and Millimeter-Wave Integrated Circuit Systems in Packaging

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Abstract

In this work, EM simulation tools were exploited to investigate the package and interconnect structures for millimeter-wave and high-speed communication systems. Precise prediction on properties of passive structures as well as active devices is achieved by using accurate EM simulation techniques developed in this work. Complex 3D EM designs and modelling can be successfully accomplished by using EM simulations.

As the foundation of the work, the general recommendations for EM simulations are firstly summarized according to two practical examples: design of a split ring resonator and investigation on multimode propagation in CPW structures. For the case of EM modelling of on-wafer measured passive components for millimeter-wave applications, a novel ground-ring excitation scheme with simple ground-signal-ground (G-S-G) probe models is proposed. The parasitic elements caused by the excitation structure are de-embedded by an extended "L-2L" calibration method. The excitation scheme and the related calibration method are validated by experimental results in the frequency range from 1 GHz to 65 GHz. The ground-ring excitation scheme is demonstrated as the only correct method for simulating CPW structures with finite ground planes for millimeter-wave applications.

By using the proposed ground-ring excitation scheme, the multimode propagation and dispersion characteristic of CBCPW structures up to 300 GHz are investigated by systematically analyzing the dimensions of the structures. The parasitic parallel plate consisting of ground planes and grounded dielectric slab outside the CPW structure are identified as the source of unwanted resonances and attenuation in CBCPW structures. Based on the recommendation derived from the investigation, a quartz-based 50 Ω CBCPW line with 1mm length was designed and exhibits less than 0.6 dB insertion loss up to 300 GHz in simulation results. EM simulations on the CBCPW with vias show the power leakage and patch antenna resonances in the structure. Vias are suggested to be placed at edge of CBCPW structures and with minimum distance to each other. The EM simulations on the CBCPW struc-

ture have to use the ground-ring excitation scheme, while traditional wave port excitation fails to identify the above phenomena.

The EM simulation techniques are further extended to the modelling of active devices. Full 3D EM models of photodetector (PD) chips have been developed to precisely predict the O/E relative response behavior of the devices. The model contains both *RC* bandwidth limitation and transit-time effect. Parasitic elements of the device must not necessary be known priori for the EM model in contrast to a circuit model. The full 3D EM model can be used to analyze parasitic effects of the chip for optimizations and design the 3D packaging structures of the chip. One PD chip for 100 Gbit/s Ethernet applications is modelled in the range from 1 GHz to 170 GHz for further chip packaging design, and the other one for THz photomixer applications is modelled to improve the output power of the device. More than 11 dB output power improvement at 700 GHz can be achieved by optimizing the structure on chip as predicted by EM simulations.

With the aid of accurate EM modelling an optimized PD module aiming at more than 100 Gbit/s Ethernet applications extends the 3-dB bandwidth from 75 GHz to 100 GHz. The simplified EM model of the module firstly suggests employing strategically placed vias in the CBCPW and enough bonding wires to connect the PD chip to the CBCPW to improve the insertion loss of the packaging structure. The O/E relative response of packaged PD modules from 1 GHz to 110 GHz has been precisely predicted by the full EM model of the module including the EM model of the PD chip. Dimensions and arrangement of bonding wires are further optimized to improve the transmission performance of the wire-bonding transition. Mode conversion from CPW mode to CBCPW mode at the transition between the PD chip and the CBCPW was identified as the major attenuation mechanism in the packaging structure. The mode matching is shown as a crucial issue in designing packaging and interconnection structures for millimeter-wave applications. This example demonstrates the capability of the developed EM design and modelling techniques to accomplish complex 3D packaging structures.

Resumé

I dette arbejde vil EM simuleringsværktøjer blive anvendt til at undersøge pakning og forbindelsesstrukturer til millimeterbølge- og højhastighedskommunikationssystemer. Præcise forudsigelser af egenskaberne for både passive strukturer og aktive komponenter er opnået ved brug af nøjagtige EM simuleringsteknikker udviklet i dette arbejde. Komplekst 3D EM design og modellering kan succesfuldt opnås ved brug af EM simuleringer.

Som fundament for arbejdet opsummeres først generelle anbefalinger for EM simuleringer i henhold til to praktiske eksempler: design af en split ring resonator og undersøgelse af multimode udbredelse i CPW strukturer. I tilfældet af EM modellering af målte on-wafer passive komponenter til millimeterbølge anvendelser, foreslås en ny ground-ring excitation metode med en simpel ground-signal-ground (G-S-G) probe model. De parasitiske elementer som opstår på grund af excitationsstrukturen bliver fjernet med en udvidet "L-2L" kalibreringsmetode. Excitationsmetoden og den tilhørende kalibreringsmetode er valideret mod eksperimentelle resulter i frekvensområdet fra 1 GHz til 65 GHz. Det demonstreres at ground-ring excitationsmetoden er den eneste korrekte metode til at simulerer CPW strukturer med endelig jord-plan ved millimeterbølgefrekvenser.

Ved brug af den foreslået ground-ring excitationsmetode kan multimode udbredelse og dispersion karakteristikken undersøges for CBCPW strukturer op til 300 GHz ved systematisk analyse af dimensionerne af CBCPW strukturerne. Den parasitiske parallelplade bestående af jordplanerne og den jordet dielektriske slab udenfor CPW strukturen er identificeret som en kilde til uønsket resonanser og dæmpning i CBCPW strukturer. Baseret på anbefalingerne udledt ud fra undersøgelsen er en quartz-baseret 50 Ohms CBCPW linje med 1mm længde designet og har ifølge simuleringsresultaterne mindre end 0.6 dB indsætningstab op til 300 GHz. EM simulering af CBCPW med via'er udviser læk af effekt og patch antenne resonanser i strukturen. Det forslås at placere via'er ved kanten af CBCPW strukturen og med minimum afstand til hinanden. EM simuleringen af CBCPW strukturer

skal benytte ground-ring excitationsmetoden da en traditionel wave-port excitation ikke kan identificere de ovenstående fænomener.

EM simuleringsteknikkerne er yderligere udvidet til modelleringen af aktive komponenter. En komplet 3D EM model af en fotodetektor chip er blevet udviklet for at præcist kunne forudsige den relative O/E respons for komponenten. Modellen indeholder både RC båndbredde begrænsning og transit-tids effekt. De parasitiske elementer af komponenterne behøves ikke nødvendigvis at være kendt på forhånd i EM modellen i kontrast til en kredsløbsmodel. Den komplette 3D EM model kan benyttes til at analysere parasitiske effekter på chippen i forbindelse med optimeringen og design af 3D pakningen af chippen. En fotodetektorchip til 100 Gbit/s Ethernet anvendelser er modelleret i området fra 1 GHz til 170 GHz for yderligere design af chip pakningen og en anden en til THz fotomikser anvendelser er modelleret for at forbedre udgangseffekten af komponenten. Ved at optimerer strukturen af chippen forudsiger EM simuleringerne at der kan opnås en forbedring af udgangseffekten på 11 dB ved 700 GHz.

Et optimeret fotodetektormodul forøger 3-dB båndbredden fra 75 GHz til 100 GHz til Ethernet anvendelser ved mere end 100 Gbit/s ved brug af nøjagtig EM modellering. Den simplificeret EM model for modulet anbefaler først at anvende strategisk placeret via'er i CBCPW strukturen og tilstrækkeligt mange bonde-tråde til forbindelsen af fotodetektor chippen til CPCPW for at forbedre indsætningstabet i pakkestrukturen. Den relative O/E respons af det pakkede fotodetektormodul fra 1 GHz til 110 GHz er blevet nøjagtigt forudset af den komplette EM model af modulet inklusiv EM modellen af fotodetektor chippen. Dimensioner og arrangementet af bonde-tråde er blevet yderlige optimeret for at forbedre transmissionsegenskaberne af bonde-tråd overgangen. Konvertering fra CPW mode til CBCPW mode ved overgangen mellem fotodetektorchippen of CBCPW er blevet identificeret som den mekanisme i den pakkede struktur der giver anledning til størst tab. Modetilpasning har vist sig som et vigtigt emne i designet af pakke og forbindelsesstrukturer til millimeterbølge anvendelser. Dette eksempel demonstrerer muligheden for at opnå komplekse 3D pakkestrukturer ved brug af de udviklede EM design og modelleringsteknikker.

Preface

This thesis is submitted as a part of the requirements to achieve the Ph.D. degree at the DTU Electrical Engineering, Technical University of Denmark. The Ph. D. study was carried from 01-02-2006 to 31-07-2009. From 10-07-2008 to 09-10-2008 and from 01-02-2009 to 31-04-2009, I left for absence from the Ph. D project. The three-year Ph. D program was financially supported by Technical University of Denmark. Professor Viktor Krozer was the supervisor and associate professor Tom K. Johansen was the co-supervisor of the project. I was with Heinrich Hertz Institut in Germany from 04-2008 to 10-2008 for six months for the external stay activity.

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Kgs. Lyngby, July 2009

Chenhui Jiang

Publication List

In the period of Ph. D. project, the following papers were published:

1. C. Jiang, V. Krozer, H-G. Bach, G. G. Mekonnen, and T. K. Johansen "Packaging of Photodetector Modules for 100 Gbit/s Applications Using Electromagnetic Simulations", Accepted in *EuMC 2009 Rome*, Sept. 2009

2. T. K. Johansen, V. Krozer, C. Kazmierski, C. Jany, and C. Jiang "Analysis of Hybrid-Integrated High-Speed Electro-Absorption Modulated Lasers Based on EM/Circuit Co-simulation",In Proc. *IMWS 2009*, Jan. 2009

3. C. Jiang, V. Krozer, H-G. Bach, G. G. Mekonnen, T. K. Johansen, R. Zhang and D. Pech "Electromagnetic Modelling and Optimization of Packaged Photodetector Modules for 100 Gbit/s Applications", In Proc. *APMC 2008 Hong Kong*, Dec. 2008

4. C. Jiang, G. G. Mekonnen, V. Krozer, T. K. Johansen, and H-G. Bach, "Packaging Aspects of Photodetector Modules for 100 Gbit/s Ethernet Applications", In Proc. *EuMC 2008 Amsterdam*, Oct. 2008

5. C. Jiang, T. K. Johansen, V. Krozer, G. G. Mekonnen and H-G. Bach, "Optimization of Packaging for PIN Photodiode Modules for 100Gbit/s Ethernet Applications", in Proc. *APMC 2007 Bangkok*, Dec. 2007

6. T.K. Johansen, V. Krozer, D. Hadziabdic, C. Jiang, A. Konczykowska, J.-Y. Dupuy, "A Novel Method for HBT Intrinsic Collector Resistance Extraction from S-Parameters", in Proc. *APMC2007 Bangkok*, Dec. 2007

7. T. K. Johansen, C. Kazmierski, C. Jany, C. Jiang, and V. Krozer, "Optimization of Integrated Electro-Absorption Modulated Laser Structures for 100 Gbit/s Ethernet Using Electromagnetic Simulation", in Proc. *IMOC 2007 Salvador*, Nov. 2007

8. T. K. Johansen, C. Jiang, D. Hadziabdic, V. Krozer, "EM Simulation Accuracy Enhancement for Broadband Modeling of On-Wafer Passive Components", in Proc. *EuMC 2007 Munich*, Oct. 2007

9. D. Hadziabdic, C. Jiang, T. K. Johansen, G.G. Fischer, and B. Heinemann, V. Krozer, "Deembedding and Modelling of pnp SiGe HBTs", in Proc. *EuMiC 2007 Munich*, Oct. 2007

10. C. Jiang, P. Andreani, U. D. Keil, "Detailed Behavioral Modeling of Bang-Bang Phase Detectors", in Proc. *APCCAS 2006 Singapore*, Dec. 2006

11. V. Krozer, T. K. Johansen, T. Djurhuus, C. Jiang, J. Vidkjaer, "Ultra-broadband Nonlinear Microwave Monolithic Integrated Circuits in SiGe, GaAs and InP", in Proc. *MIKON 2006 Krakow*, May. 2006

12. C. Jiang, T. K. Johansen, V. Krozer, "Conversion Matrix Analysis of GaAs HEMT Active Gilbert Cell Mixers", in Proc. *InMMiC 2006 Aveivo*, Jan. 2006

List of Figures

List of Tables

Contents

Chapter 1

Introduction

This chapter will first introduce the general background and research motivation of this work. Thereafter, a thesis overview will be provided.

1.1 Millimeter-wave Applications and Packaging Challenge

With the explosive evolution of data traffic and multimedia service all over the world, massive amounts of data have to be sent and received in the data communication systems due to the blooming services on the internet. These services have to transfer large volume data like high-resolution pictures, high-definition videos, voice, music, gaming, e-commerce, and peer-to-peer file sharing and so on [1]. Higher and higher speed internet is emergently required by millions of end users who demand above services. After the success of 10 Gbit/s optical Ethernet, the 100 Gbit/s optical Ethernet has been considered to be the ideal candidate for the next generation high speed data transmission system [2]. 100 Gbit/s optical series Ethernet exhibits higher data transmission speed, fewer opto-electronics and interconnects, less power consumption and heat dissipation problem, compared to its counterpart, 40 Gbit/s Ethernet [3].

Since the optical communication systems intend to transmit series data at the rate of 100 Gbit/s, the optical and electronic devices should functionally operate very well to at least at 100 GHz. At such high operation frequency, the effective design of packages and interconnects is quite challenging because of the electrical loss of electrodes, impedance mismatch along the RF path, and the loss due to the higher order modes and resonances in transmission line structures and launch transitions, as well as radiations. Those

package and interconnect effects were addressed before for lower bit rates (<40 Gbit/s) applications [4]. More serious problems will appear in the 100 Gbit/s systems because of the higher operating frequencies.

Hybrid opto-electronics packaging solution [5] has been used for the packaging of high-speed modules instead of traditional "multi-box" design [6, 7]. It should achieve high performance of signal integrity due to the low loss from the simplified packaging structures. Therefore, it is a trend to integrate as many functional chips as possible on one single substrate or within one module by using state-of-art packaging and interconnects technologies.

The high-speed optical communication system is not the only application aiming at over 100 GHz operation frequency. In addition to it, the millimeter-wave image systems for medical and security applications demand for high working frequency to achieve high resolution images. Furthermore, the aeronautic and astronautic area for radar systems and satellite communication systems also requires MMIC operation approaching sub-millimeter-wave range [8]. Millimeter-wave monolithic integrated circuits (mm-wave MMICs), such as mixers [9] and LNAs [10] operating above 200 GHz, and optoelectronic integrated circuits (OEIC), such as photodiode chips with 130 GHz bandwidth [11], have been recently developed and reported. Passive packaging and interconnects structures, however, may distort the high frequency signals due to high losses, multimode propagations and resonances. Therefore, successful design of packaging and interconnects in the millimeter-wave frequency range is crucial for maintaining the performance of entire high-speed and millimeter-wave systems.

Flip-chip, wire-bonding, and tape-bonding are widely used in multi-chip-module (MCM) packaging for interconnecting the chips based on different substrates. These technologies were compared in the aspect of the transmission performance up to 120 GHz [12]. During past years, the research activities have been carried out to investigate the behavior of flip-chip [13–18] and wire-bonding [19–24] interconnect technologies. Flip-chip technology is considered to hold superior performance compared with wire-bonding technology, because small solder bumps, whose dimensions are in the range of tens of micrometers, introduce less inductive parasitics. However, with the development of wire-bonding technology, the length of bonding wires can be fabricated below 200 μm. Compared to the wavelength in air at 100 GHz being around 3mm, the dimensions of bonding wires are fairly small. A comparable performance of wire-bonding technology can be expected as compared to flip-chip technology. Therefore, wire-bonding is another attractive interconnects solution in millimeter-wave applications with additional advantages such as robust, low cost, convenient fabrication process and high

thermal tolerance.

The objective of this thesis is to develop EM simulation methodologies and techniques for investigating the loss mechanism and parasitic effects in packaging and interconnects structures in millimeter-wave systems and high speed communications systems. The packaging and interconnects structures will be optimized and designed for millimeter-wave applications with the full knowledge of the relevant parasitic effects. While the operating frequency of applications approaches terahertz range [25], those parasitic effects get increasingly serious and heavily degrade the performance of the functional modules and chip devices. All these effects are related to their electromagnetic (EM) properties such as unexpected EM coupling and multimode phenomena.

Although EM simulations have been extensively utilized to analyze EM properties of microwave devices, the accuracy of simulation results was not always satisfactory. Actually, achieving accurate EM simulation results is not straightforward, because the accuracy of simulations is determined by several facts such as excitation setups, boundary conditions and so on. Developing techniques for accurate EM simulation is a vital part of the thesis. Besides summarizing general requirements for accurate EM simulations, the thesis proposes a novel ground-signal-ground (G-S-G) probe model in EM simulations for simulating on-wafer measurement setups. It is considered the only way to simulate on-wafer measured components. This excitation setup is further used for correctly exciting coplanar structures.

Accurate EM simulation techniques can not be used only for designing and optimizing package and interconnect structures but also universally for any problems related to EM issues including modelling active devices. The thesis work innovatively developed full 3D EM models of photodetectors. It is the first time that the full EM modelling has been extended into active device domain.

Therefore, this thesis work is an excellent foundation for future research activities dealing with EM modelling and EM designs for both passive structures and active devices. In the thesis work, EM simulations have been implemented to analyze transmission line structures, model active OEIC devices and packaged functional modules, and design comprehensive packaging structures.

1.2 Organization of the Thesis

The main part of the thesis is divided into six chapters.

Chapter 1 begins with an introduction to this work.

Chapter 2 focuses on the techniques for accurate EM simulations. EM simulations will be implemented throughout the thesis as powerful tools to analyze, optimize and design packaging and interconnects structures. The principles at each step of EM simulations are discussed based on two examples: design of slit ring resonators and investigation on multimode propagations in coplanar waveguides. A novel excitation scheme based on lumped ports as well as the de-embedding techniques is developed for accurately simulating on-wafer measured devices and coplanar structures .

Chapter 3 analyzes the propagation and dispersion characteristics of our conductor-backed coplanar waveguide (CBCPW) structures using EM simulations, because CBCPW structures are widely utilized in advanced packaging structures as on-chip interconnects and MCM interconnects. Both CBCPWs with and without vias were fabricated and measured to verify the accuracy EM simulations up to 100 GHz. It is verified that EM simulations are able to precisely predict the behavior of those structures and provide an access to the EM features of the structures. The approach for designing CPWs and CBCPWs by using EM simulations is summarized in the chapter.

Chapter 4 presents EM models of photodetectors (PDs), which are typical opto-electronic active devices. It is the first full EM models of active devices. The models precisely describe the O/E response behavior of PD chips. They are used to analyze the parasitic effects in the chip, optimize the passive structures of the chips, and design packaged modules containing PD chips.

Chapter 5 presents the packaging design of PD modules for 100 Gbit/s applications using EM simulations. This chapter integrates and utilizes the results from previous chapters. The investigation focused on optimizing the comprehensive packaging structures, which include wire-bonding interconnection, CPW-to-CBCPW transitions, CBCPW structures and CBCPW-to-coaxial transitions. A packaged PD module was developed accordingly and exhibits very good performance for 100 Gbit/s applications

Chapter 6, finally, summarizes the conclusions of this work.

Chapter 2

Accurate 3D Electromagnetic Simulation Techniques

The three dimension (3D) electromagnetic (EM) simulation is widely considered as a very powerful tool for designing passive structures in millimeter-wave applications, such as antennas, filters, packaging and interconnects, and other structures [26]. 3D EM simulations solve Maxwell's equations in a 3D spatial domains of the structure and provide EM field information. One may monitor the EM field distribution to analyze the EM characteristics of the designed structure. Important microwave parameters, such as S-parameters and propagation constants, can be derived after EM simulations for the purpose of passive device designs. However, with such wonderful tools it is not straightforward to obtain accurate simulation results. For instance, incorrect excitation setups can result in nonsense results at the end of simulations. Therefore it is necessary to develop a method to do accurate EM simulations. The technique of accurate 3D EM simulations will be discussed in this chapter.

This chapter will first summarize the commercial EM simulation tools which are popularly used nowadays. After the summary, two typical examples, namely the design of split ring resonators and the investigation on dispersion characteristics of coplanar waveguide (CPW) structure, are simulated to demonstrate accurate EM simulations based on the general principles. The general principles for achieving accurate EM simulation results are presented according to the flow chart of EM simulations. Furthermore, a novel excitation scheme for correctly exciting CPW structures is proposed. An excitation structure in the scheme models the setup of on-wafer measurements. This structure overcomes the drawbacks of wave port excitations

but brings additional parasitics. A relevant calibration method called "Extended L-2L Calibration Techniques" is developed to de-embed the parasitics from the excitation structures. The excitation scheme associated with the calibration method provides an accurate solution to model on-wafer measured devices and simulate CPW and conductor-backed CPW (CBCPW) structures by using EM simulations.

2.1 Overview of 3D EM Simulation Tools

This section will briefly summarize the most popular commercial 3D EM simulation tools. They are classified by the domains in which the simulator solves the EM problems. The domain is either time domain or frequency domain. For the time domain solver, the finite integration technique (FIT), finite difference time domain (FDTD) method and the transmission line method (TLM) are used in commercial tools. For the frequency domain solver, the tools numerically solve EM problems by using finite element method (FEM), FIT and the method-of-moments (MoM) [27]. All above numerical methods are able to discretize the device under test (DUT) in volume. However, the MoM has been used in the modelling of planar structures in which basis functions are expanded on specific surfaces; hence the EM simulation based on MoM is also called 2.5D EM simulations in these cases.

Time Domain Tools

In time domain simulations, a Gaussian signal with broadband spectra of interest is excited at the input port of the structure under investigation. The excited signal propagates through the entire structure. At the end of the simulation, the time responses at the output port or any other points of interest are derived when all output signals ideally decay to zero. The frequency response is obtained from the time response through using Fourier transform. According to the simulation procedure, one run of time domain simulation can generate the S-parameters in the whole frequency range of interest. However, the method is not adequate for devices with inherent high Q resonances. The injected EM power will take a very long time to decay to zero in this case. The simulation may take extremely long time until it converges in the ultimate.

CST MICROWAVE STUDIO [28] is a full 3D EM simulator using FIT method. The transient solver in CST MICROWAVE STUDIO is the main feature of the software.

Softwares based on FDTD include *FIDELITY*, *IMST Empire*, *Concerto-PR*, *QuickWave* and others.

Frequency Domain Tools

Frequency domain solvers typically discretize the solution domain, build a matrix, and invert the matrix to find the solution [29]. The solution domain needs be solved at each frequency point of interest. FEM is typically used in frequency domain tools. As a method of solving full 3D problems, FEM is very powerful to treat arbitrary objects. Even very detailed structures can be well treated in simulations. Automatic mesh refinement is the unique feature to this method [29]. The refinement is error-based by the basic formulation of the method. Since FEM can compute the multimode propagation in passive structures, mode conversions in structures can be observed in simulation results.

Although the response of the structure in frequency domain requires multi-simulation runs at different frequency points of interest, most of the frequency domain tools offer "fast sweep" option to scan the whole frequency range and compute the response in the frequency range by one simulation run. The fast sweep methods are based on asymptotic waveform evaluation (AWE) [30–32], the Padé via Lanczos method (PVL) [33–35], or an adaptive Lanczos-Padé sweep (ALPS) [36, 37]. With the increased accuracy of the "fast sweep" feature, it is very efficient for broadband simulations.

Ansoft HFSS [38] is a full 3D EM simulation software using FEM method. Most EM simulations in this thesis are implemented in Ansoft HFSS. The following discussion about the accurate EM simulation techniques is mainly carried out based on Ansoft HFSS. The accurate EM simulation methodology discussed in the following, however, is not only valid for Ansoft HFSS but is universal to any EM simulators.

2.2 General Principles for Accurate EM Simulations

Achieving accurate 3D EM simulation results is not so straightforward as it sounds. The nature of 3D EM simulations requires more manipulation than circuit-level simulations. The correct setups of EM simulations are essential for having accurate and reasonable results at the end of simulations. Fig.2.1 illustrates the procedure for performing 3D EM simulations. In the previous section, commercial EM simulation tools were briefly discussed.

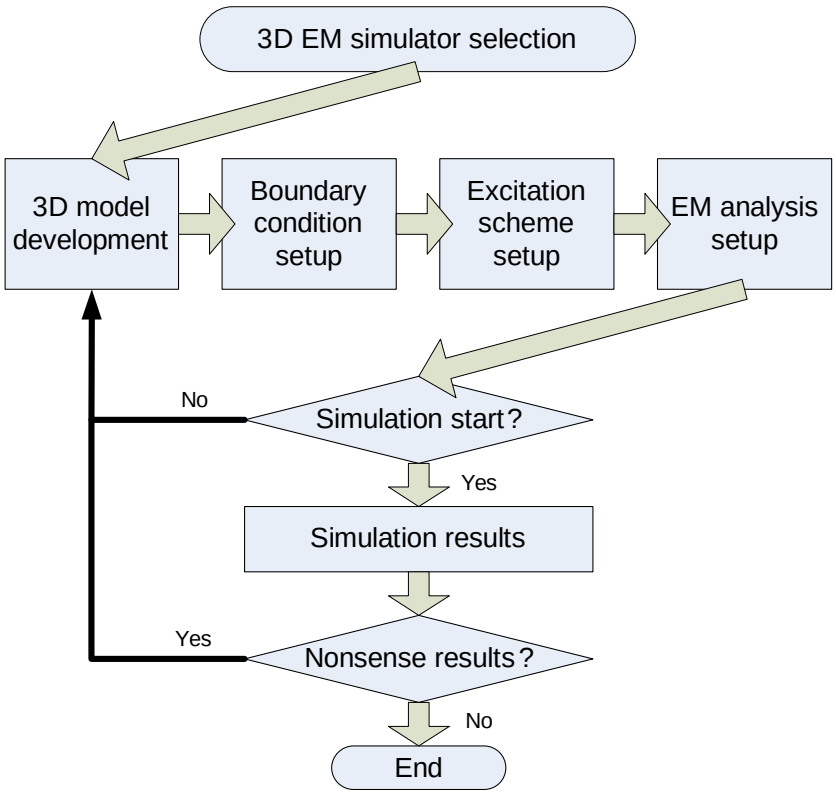


Figure 2.1: The flowchart of the EM simulation procedure.

After selecting the proper simulation tools, people need to go through all steps as indicated in Fig.2.1 starting with 3D model development of the structure under investigation to finally analyzing the simulation results. Any mistake occurring in any step may result in nonsense simulation results at the end of simulations.

Two examples are selected to illustrate the general principles of accurate EM simulations. One example is to design a split ring resonator. The other one is to investigate the multimode propagation property of coplanar waveguides. The procedure of the discussion on the examples is according to the flow chart of EM simulations. Ansoft HFSS is selected as the simulation tool for these two examples.

2.2.1 Example 1: Split Ring Resonator Designs (3D)

A split ring resonator (SRR) [39] design is selected as the first example to demonstrate the principles to be followed in accurate EM simulations. The SRR shows the similar resonance behavior as parallel LC tank, and the central frequency can be predicted by equivalent lumped inductance and capacitance [40, 41]. The precise prediction relies on the correct extracted values of lumped components of the circuit model. But, the EM model of the SRR can predict the center frequency without the parameter extraction. Only the dimensions and the material properties are required for the EM model.

3D Model Development

The prerequisite condition for precise EM modelling is to develop a precise 3D model of the structure under investigation. In this step, the 3D model should have the identical geometrical parameters as the real structure. The schematic of the SRR with geometry notations is shown in Fig.2.2. The ring resonator is rectangle and excited by a microstrip line. The values of the structure dimensions are listed at the right side of the schematic. The thickness of the substrate is 813 μm.

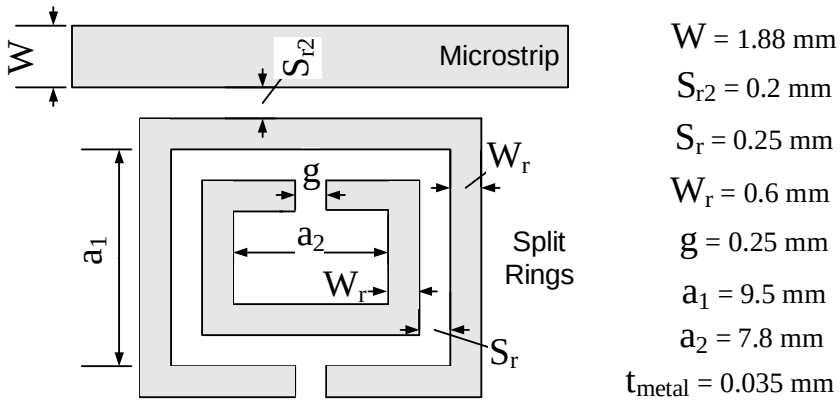


Figure 2.2: The schematic of two split ring resonators coupled to a microstrip line.

Fig.2.3 shows an EM model of the SRR in Ansoft HFSS. Two coupled split rings locate at both sides of the microstrip to balance the designed resonator and enhance the quality factor of resonance. The parameters in

Fig.2.2 are used in the EM model. The parametric design for geometrical structure development is highly recommended in building EM models. The meaningful parameters are very helpful for designing large-scale EM models with numerous objects. With parameters, the structure is easily optimized by tuning the parameter of interest.

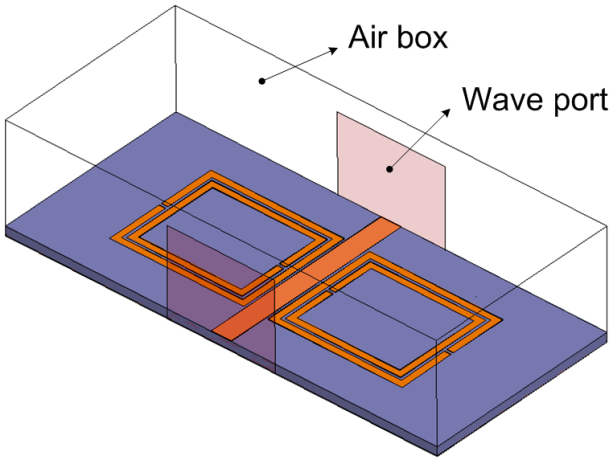


Figure 2.3: The model of a split ring resonator (SRR) coupled to a microstrip line in the EM simulator, *Ansoft HFSS*.

Another challenge in 3D model development is to assign the attributes of the materials in the model such as conductivity (σ), relative permittivity (ε_r), relative permeability (μ_r) and dielectric loss tangent ($\tan(\delta)$). The correct values of these parameters are the preconditions for the 3D EM model to accurately predict the EM behavior of the structure. Actually, the parameters of materials are hard to obtain with precision even if they are provided in the data sheet by the commercial dielectric providers.

For the SRR design, the metal is copper ($\sigma = 5.8 \times 10^7$ S/m) and the substrate of the SRR is Rogers RO4003(tm). The nominal ε_r of the material is 3.38, the μ_r is 1 and the $\tan(\delta)$ is 0.0027 at 10 GHz. But, the ε_r used in simulations should be 3.55 with 5% deviation. The value for simulation is suggested by the substrate vendor. If the ε_r and $\tan(\delta)$ in the model is not precise, the EM model can not correctly predict the resonance frequency and the Q factor of the SRR. Furthermore, these parameters of materials may be frequency dependent for the broadband application. The frequency dependent characteristic should also be included in the model. However, the analytical expression for such frequency dependence is not readily accessible

in libraries or handbooks. Therefore, the frequency dependent effect can be ignored during simulations if the approximation does not lead to significant errors.

Boundary Condition Setups

The EM simulations are normally performed within a finite region. The boundary conditions in the region are very important for deriving consistent simulation results compared to measurement results. The major principle of defining the boundary condition is resembling the case in the reality. For the SRR design, an air-box is defined as the solution region for the EM simulator, and the surface of the air-box expect for the bottom face is assigned by a "radiation boundary" which resembles an open area. The "radiation boundary" absorbs the EM wave as the solution region is electrically open. The bottom of the air-box is assigned by "perfect-E boundary" to resemble the metallic supporter for the SRR.

Besides defining the solution region close to the real case, some boundary condition may also alleviate the computation effort in the simulation. "Symmetric boundaries" may be placed at the symmetric plane of symmetric 3D models to reduce the size and complexity of the model by half. Since the SRR model is symmetric, the symmetric boundary can be put along the center-line of the microstrip. When the scale of EM models becomes large such as more than one pair of rings in the SRR, simplifying the model by symmetric plane is necessary to improve simulation efficiency.

Furthermore, some boundaries can improve the accuracy of the simulation or the flexibility of the model. The finite conductivity boundary can model the surface roughness loss, and the lumped element boundary introduces the possibility of utilizing lumped elements, such as resistors, capacitors and inductors, in 3D EM models.

Excitation Setups

3D EM models have to be excited to derive the relevant EM properties. Ports as a kind of unique boundaries in 3D EM simulators are usually used to excite models. They generate EM power and feed the power to 3D EM models. At the same time, ports also act as terminals at the other side of structures. The excited EM power with correct modes is the precondition to correctly compute the EM characteristics of the DUT. The characteristic parameters of the DUT like S-parameters highly depend on the excitation setups. Unfortunately, there is no simple and universal recipe for determining

ports for all cases. One has to deal with sorts of ports' geometries when determining the excitation schemes. There are generally two types of ports defined in simulation tools: one is the wave port, and the other one is the lumped port.

The EM model of SRR is excited by wave ports as demonstrated in Fig.2.3. As the excitation feature in 3D EM simulation, wave ports are special 2D structures to excite 3D models. They are always located at the boundary of the solution region. The EM simulator considers that the wave port is connected to a semi-infinite long waveguide which extends outside the solution region. The waveguide has the identical cross-section and material to the area defined by the wave port. The modes excited by the wave port are determined by natural modes of the wave guide. A 2D solver is used to determine the modes by solving Maxwell's equations. The solution is expressed by [38]

$$\nabla \times (\frac{1}{\mu_r} \nabla \times \overrightarrow{E}(x,y)) - k_0^2 \varepsilon_r \overrightarrow{E}(x,y) = 0 \tag{2.1}$$

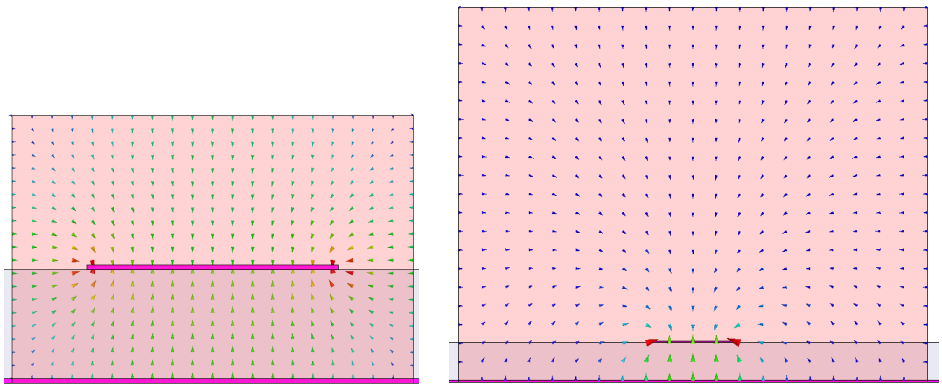
Wave ports have perfect-E boundary associated to the port periphery due to the definition of virtual semi-infinite long waveguide. This condition is ideal for exciting waveguide structures such as rectangular waveguides or coaxial cables. But, it is not the case for planar transmission lines such as microstrips or CPWs. The perfect-E boundary does not actually exist in the real measurement setups or the interfaces between planar transmission lines. Therefore, the artificial boundary of wave ports might possibly deteriorate the simulation results in this case.

Fig.2.4 shows excited modes on the microstrips by wave ports for SRR design. When the wave port is small as shown in Fig.2.4(a), the periphery of wave ports is close to the signal strip, unexpected coupling effect will be stimulated between the wave ports and the strip. The excited mode is no longer microstrip mode. The simulated port impedance is 39 Ω. It is calculated from values of power (P) and current (I) as follows [42]:

$$Z_c = \frac{P}{I \cdot I} \tag{2.2}$$

The power and current are computed directly from the simulated fields. The power passing through a port is equal to the following:

$$P = \oint_s \overrightarrow{E} \times \overrightarrow{H} \cdot d\overrightarrow{s} \tag{2.3}$$



(a) (b)

Figure 2.4: Excited modes on microstrips by wave ports: (a) with small size; (b) with large size.

where the surface integral is over the surface of the port. The current is computed by applying Ampere's law to a path around the port:

$$I = \oint_{l} \overrightarrow{H} \cdot d\overrightarrow{l} \tag{2.4}$$

When the wave port is enlarged as shown in Fig.2.4(a), the correct microstrip mode is excited and the port impedance is 47.8 Ω, which is close to the calculated characteristic impedance of the microstrip 48.7 Ω by *LineCalc* in Advanced Design System by Agilent Technologies. We also have to know that the parasitic rectangular waveguide mode might be excited if the wave port is too large. So the size of the wave port is critical for exciting the correct modes.

There are several rules of thumb for determining the size of wave ports. Fig.2.5 demonstrates the empirical rules for determining the size of wave ports while exciting different planar structures. For all the cases, the port peripheries contact the ground planes of the transmission lines. The periphery is the ground reference of the port as well as the ground reference of the transmission line. The width of the port hence should be wide enough to avoid the adjacence of the signal strip and the port periphery. For the microstrip and CBCPW, the ports do not only contact the backside ground plane but need to be high enough to keep vertical distance from the signal strip to the port periphery. For the CPW, the metallization layer should evenly separate the wave port vertically and the lower part of the port should

not exceed the substrate region.

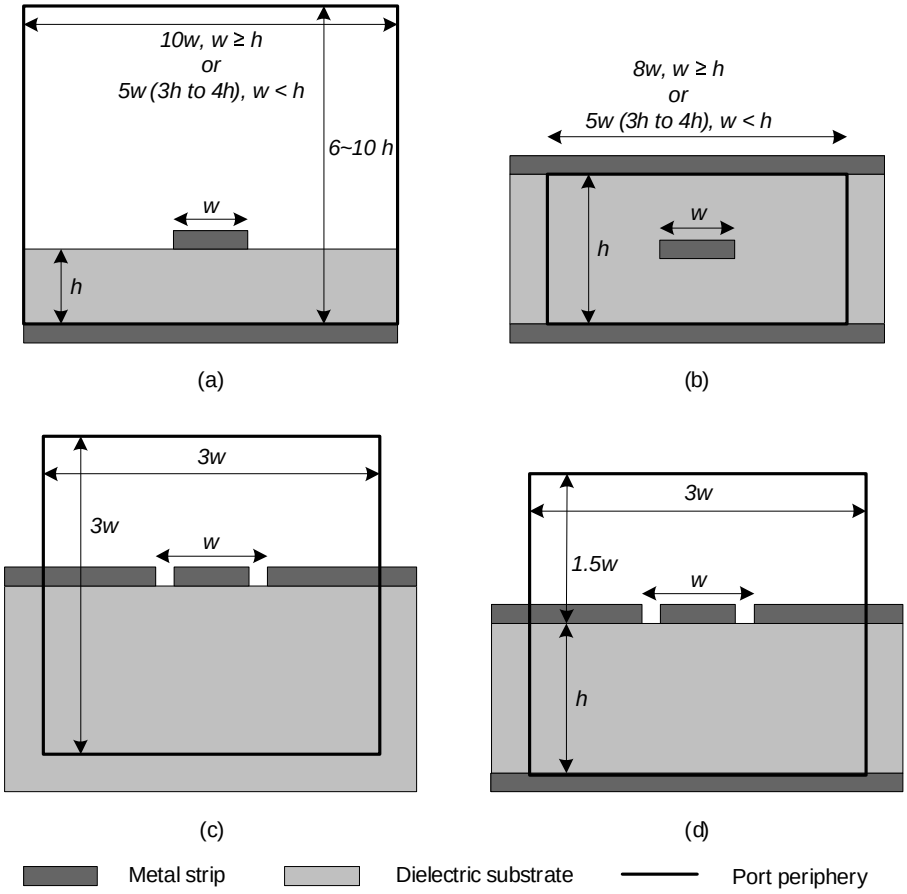


Figure 2.5: The wave port size specification for different planar transmission lines: (a) microstrip; (b) stripline; (c) coplanar waveguide; (d) conductor-backed coplanar waveguide.

EM Analysis Setup and Simulation Results Analysis

After the 3D models, boundary conditions and excitation schemes are properly settled, the setup of EM analysis determines the accuracy of the simulation due to the numerical solutions. The trade-off between the simulation accuracy and computation resource consumption is the main concern in this step. An appropriate EM analysis setup requires the verification by simula-

tion results. The discussion on the EM analysis setup hence combines with analyzing simulation results.

	f_{mesh} (GHz)	Mesh Size	Convergence (ΔS<0.02, 2 passes)	Sweeping Types	f_r (GHz)
$Sim1$	1.86	31124	No	fast	<1.77
$Sim2$	1.86	37870	No	fast	1.79
$Sim3$	1.86	212270	No	discrete	1.86
$Sim4$	1.90	308210	Yes	discrete	1.86
$Sim5/6$	2.00	68919	Yes	discrete/fast	1.83
$Meas$	—	—	—	—	1.86

Table 2.1: EM simulation setups and results summary for SRR designs. f_{mesh} refers to the frequency at which the solver implements adaptive meshing; f_r refers to the simulated resonant frequency.

The simulated insertion losses of the SRR with different EM analysis setups and convergence status are shown in Fig.2.6. The measured insertion loss is also plotted as a reference to determine the accuracy of simulation results. The measured resonant frequency is 1.86 GHz. The EM analysis setups are summarized in Table.2.1. The model was adaptively meshed at 1.86, 1.90 and 2.00 GHz, respectively. $Sim1$, $Sim2$ and $Sim3$ were adaptively meshed at 1.86 GHz because it is the measured resonant frequency.

The convergence criterion is set to be $\Delta S^1 < 0.02$. Two continuous converged adaptive passes are required in order to prevent that non-converged results appear after only one converged pass. $Sim1$ and $Sim2$ with below 40000 mesh cells do not converge at the end of adaptive meshing. The simulated resonant frequency approaches the measured one with the number of mesh cells increasing. Although $Sim1$ and $Sim2$ do not eventually converge, the coarse meshes consume less computation resource and generate results very quickly. The resonance behavior was predicted by EM simulations. Even if the simulated center frequencies are not precise, the EM analysis with coarse meshes is still suitable in the early phase of designs for optimizing the relevant structures.

When the number of mesh cells is more than 210,000 for $Sim3$, the simulated frequency is exactly same as the measured one, even though the adaptive meshing passes did not converge. The EM model was also meshed at 1.90 GHz in $Sim4$. The adaptive mesh passes converged with more than

[1]The ΔS is defined as the maximum change in the magnitude of the S-parameters between two consecutive passes.

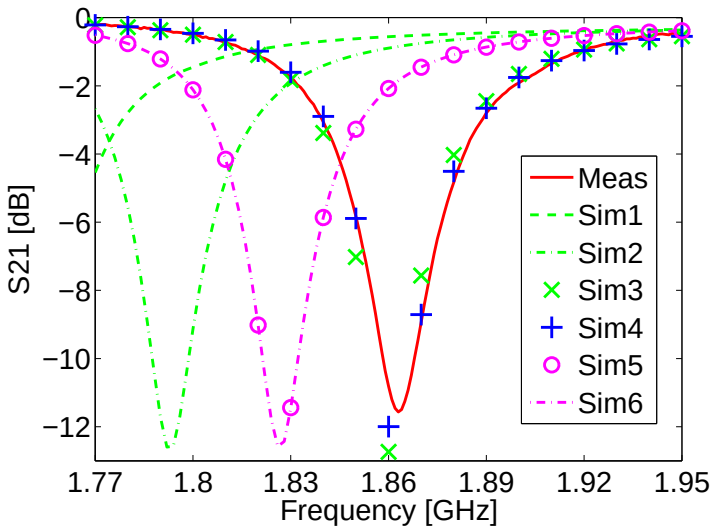


Figure 2.6: Simulated insertion losses of the SRR with different simulation setups and convergence statuses. The measurement result is also plotted as a reference.

0.3 million mesh cells ultimately. The simulated resonant frequency is still 1.86 GHz. The simulated insertion loss across the band almost overlaps the measured values. Therefore, the results by $Sim4$ are accurate and reliable. The fine meshes should be used in the final steps of designs when the simulation results compare to the measurement results, because the simulation requires very long time and a large amount of computation resource.

When the model is solved at 2 GHz for $Sim5$ and $Sim6$, the adaptive meshing converged with less than 70000 mesh cells. Although the adaptive meshing converged, the simulated resonant frequencies deviate from the measured one. Since the model was solved outside the resonance region for adaptive mesh generation, the resonance behavior of the DUT was not precisely simulated. The adaptive meshing converged with non-adequate mesh cells. The EM simulation results based on these mesh cells can not accurately characterize the SRR.

We can conclude that the resonant structure (narrow band applications) is suggested to be adaptively meshed within the resonance region for adaptive meshing. The converged mesh solved outside the resonance region are not reliable. The decisive factor is the absolute number of mesh cells. More mesh

cells result in more accurate results. Although $Sim3$ does not converge and $Sim4$ does not mesh the model at resonant frequency, the simulated resonant frequencies converged to one value which is exactly same as the measured one when the mesh cells are adequate.

$Sim5$ and $Sim6$ have almost the identical EM analysis setup except for the type of frequency sweeping. This discussion is just for frequency domain solver. $Sim5$ uses "discrete" sweeping and $Sim6$ uses "fast" sweeping. Simulation results from these two sweepings overlap with each other. It proves that "fast" frequency sweeping has the same accuracy as the "discrete" sweeping, which is usually considered as the most accurate sweeping method. "Fast" sweeping provides high resolution frequency characteristic without any simulation duration penalty. One whole frequency range sweeping is achieved by only one simulation run, but memory consumption is higher than "discrete" sweeping. $Sim3$ and $Sim4$ only use discrete sweeping due to the memory limitation. The problem can be solved by using computers with enough memory. "Fast" sweeping hence is believed to be the most efficient way to calculate the frequency response by frequency domain solvers.

2.2.2 Example 2: Multimode Propagations in CPWs (2D)

With the operation frequency of MMIC systems becoming higher and higher, the EM energy may not propagate as the dominant mode along the interconnection transmission lines or waveguides. The dominant mode may couple to other higher order modes when the operation frequency is higher than certain cut-off frequencies. The multimode propagation is the major attenuation mechanism and seriously degrades the performance of MMIC systems at very high frequencies.

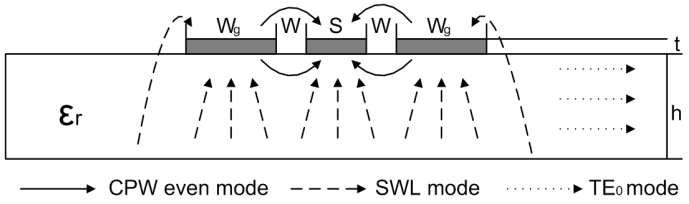


Figure 2.7: Cross section of a CPW with finite ground planes. Geometry parameters of the CPW and the relevant modes for the CPW are illustrated.

Fig.2.7 shows the cross section of a CPW with finite ground planes. Due

to the low dispersive characteristic and easy grounding structures, CPWs are widely used as chip-to-chip interconnections and on-chip interconnection lines. The height of the substrate is denoted by h, the thickness of metal, which is perfect electric conductor (PEC), is denoted by t, the width of the signal strip is denoted by S, the gaps between the signal strip and ground planes are denoted by W and the width of ground planes is denoted by W_g. The $S + 2W$ is referred as the width of the CPW structure. The ε_r is the relative dielectric constant of the substrate. The values for the parameters are list in Table.2.2. The width of the substrate is 1275 μm.

Parameters	W	S	W_g	h	t	ε_r
Values	25 μm	25 μm	100 μm	100 μm	5 μm	2.25

Table 2.2: Nominal dimensions of the CPW for the investigation on multimode propagation.

Three modes may propagate along the CPW as shown in Fig.2.7. The solid lines representing E-field vectors illustrate standard even CPW mode. The dashed lines and dot lines illustrate parasitic propagation modes, surface-wave-like (SWL) mode and TE_0 surface wave mode, respectively. The multimode propagation property of the structure can be obtained by using a 2D solver to analyze the cross sections of the interconnection structures.

Multimode excitation by wave ports is utilized to analyze the multimode propagations of the CPW. As the typical suggested scheme for exciting the CPW by wave ports, the periphery of wave ports should contact the CPW's ground planes to make sure that they are correctly grounded as shown in Fig.2.5(c). However, this setup will modify the feature of the CPW with finite ground planes. The uncovered substrate outside the ground planes will not be included in the simulation region. Therefore, the periphery of the wave port does not touch the finite ground planes of the CPW for currently investigating the modes in the CPW structure.

The width of the wave port is equal to the width of the substrate. The edge of the wave port touches with the edge of the substrate. Since the unwanted coupling between the substrate and the periphery of the wave port should be avoided, the width of the wave port can not be extended any more. The height of the wave port is 1000 μm, which is ten times of the thickness of substrate. The dimensions of the wave port are defined with large values to alleviate the influence due to the periphery of the wave port. But too large dimensions may introduce parasitic rectangular waveguide modes. The selected dimensions are appropriate, and coming simulation results will verify

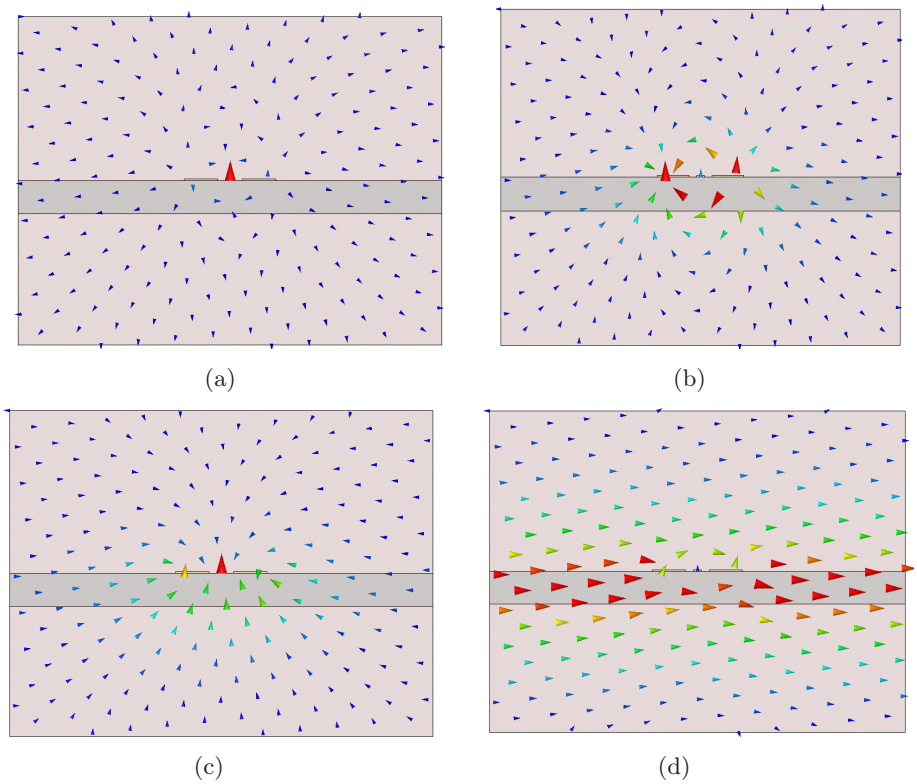
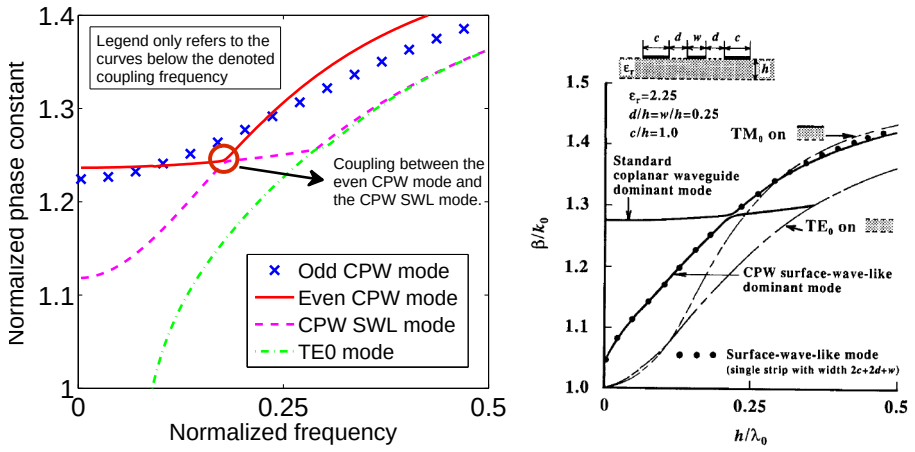


Figure 2.8: The electric field pattern of propagation modes in CPW with finite ground planes by electromagnetic simulation in Ansoft HFSS: (a) even CPW mode; (b) odd CPW mode; (c) CPW surface-wave-like (SWL) dominant mode; (d) The TE_0 surface wave mode in the lateral ungrounded dielectric slab.

this wave port definition. The line, where the metal layer locates, evenly divides the area of the wave port. For instance, if the lower side of the substrate touches the bottom periphery of the wave port, the DUT is not a CPW structure but a CBCPW structure. Therefore, the wave port with properly designed dimensions and placement is mandatory to obtain correct multimode propagation characteristics. Wave ports have to be defined as this section suggested and be verified by simulation and theoretical results.

Fig.2.8 shows the modes excited by the wave port. Besides three modes which are identical to the modes indicated in Fig.2.7, there is another mode called odd CPW mode which is shown in Fig.2.8(b). It appears because the ground planes of CPW are actually floating in the solution domain. The

solver considers the CPW as three coupled conductors. This mode hence naturally exists. This situation is normally avoided in reality since ground planes are connected to keep to be at the same potential.



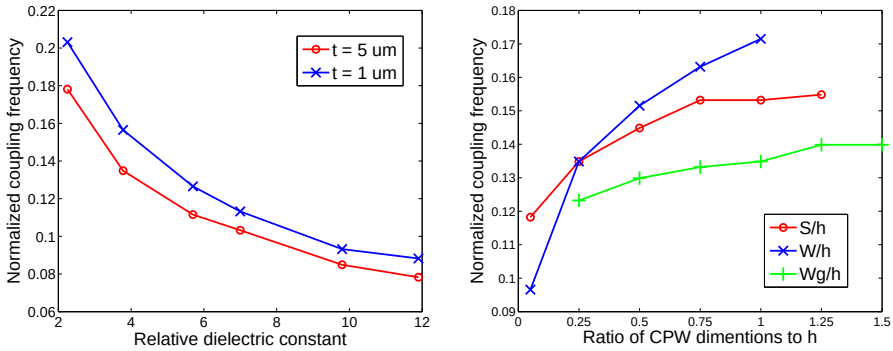
(a) (b)

Figure 2.9: Dispersion curves of CPW with finite ground planes. (a) Simulation results; (b) early published analyzed results.

Fig.2.9 shows the dispersion curves of the CPW with finite ground planes. The Y-axis is the normalized phase constant (β/k_0), and the X-axis is the normalized frequency (h/λ_0). Here, k_0 is the wave number in vacuum and λ_0 is the wavelength in free space. Some valuable conclusions can be obtained from the dispersion characteristic plot.

- When the frequency is low, odd CPW mode and even CPW mode have comparable normalized phase constants. Odd CPW mode is more dispersive than even CPW mode.
- The CPW SWL mode has zero cutoff frequency and is very dispersive. When the operation frequency increases, the coupling effect occurs between the CPW SWL mode and even CPW mode. The coupling region in the dispersion curve is indicated by a circle in the Fig.2.9(a).
- With the frequency increasing further, the dispersion curve of even CPW mode crosses the TE_0 surface wave mode. The bounded power of even CPW mode leaks into the TE_0 surface wave.

Due to the artificial PEC boundary of the wave port in EM simulation, the modes exited by the wave port are not exactly the same as the real open case. This simulation limitation explains the cutoff frequency of TE_0 surface wave, which should be theoretically zero. The simulated dispersion plot, Fig.2.9(a), is quite similar to the one published in early literatures [43], Fig.2.9(b). Both of them illustrate the coupling effect between the even CPW mode and SWL mode and TE_0 surface wave mode, which is considered to be the major attenuation mechanism in the finite-ground CPW transmission lines. The good agreement evidently proves the validation of the multimode excitation in EM simulations and it works for investigating multimode propagations by accurate EM simulations. The EM simulation only takes several minutes to obtain the dispersion curve.



(a) (b)

Figure 2.10: Simulated coupling frequencies from even CPW mode to CPW surface-wave-like mode. (a) The coupling frequencies with respect to different dielectric constants of substrate and two values of metal layer thickness: 1 μm and 5 μm; (b) The coupling frequencies with respect to the ratio of CPW dimensions to h while keeping other dimensions constant. The dielectric constant of the substrate applied in (b) is 3.78 as quartz glass.

The coupling between the even CPW mode and the CPW SWL mode is the dominant multimode propagation effect in CPW structures. The very narrow and close coupling region means very strong coupling effect among those two modes at that frequency [43, 44]. When the frequency is higher than the coupling frequency, the even CPW mode mostly leaks as the SWL mode. This leakage causes high transmission attenuation along the interconnection lines. The coupling frequency is determined by the dielectric constant of the substrate and the geometry parameters of the CPW. Fig.2.10 summa-

rizes the variation of the coupling frequency due to the material of substrate and the dimensions of the CPW. Fig.2.10(a) demonstrates that the coupling frequency decreases with the dielectric constant increasing and thinner metal layer results in higher coupling frequency. Higher dielectric constant makes the SWL mode more dispersive which result in lower coupling frequency.

Fig.2.10(b) demonstrates that the coupling frequency increases with all the ratios increasing. It is most sensitive to the gap (W) in the CPW structure and least sensitive to the width of ground plans. That is because the majority of EM energy exists in the gap. The gap dominates the characteristic impedance and the phase constant of the CPW. When the gap is quite narrow compared to the metal layer, the CPW looks mostly like a metallic plate with two negligible slots. The CPW mode is easier to couple to SWL mode at lower frequencies.

In this example, accurate analysis on the multimode propagation along CPW with finite ground planes is presented. Through using properly assigned wave ports with multimode excitation, the propagation modes in the CPW are correctly calculated by 2D solver. The reliability of the simulation results is proved by earlier published results. Simulating for the complete dispersion curves as shown in Fig.2.9 only takes a few minutes on normal PCs. This approach can be used to investigate multimode propagations of other interconnect structures.

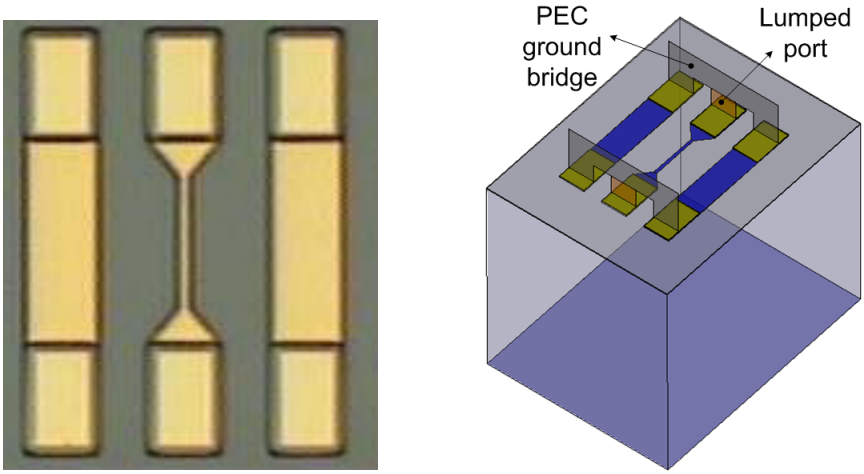
2.3 Accurate EM Simulations for On-Wafer Components

EM modelling of two port on-wafer measurements at millimeter-wave frequencies requires an exact excitation representation of the measurement setup, including the probes and the lines connecting the probes with DUT. The measurement probes usually possess ground-signal-ground (G-S-G) configuration and contact the CPW-like contacts while measuring the DUT. EM analysis of an embedding structure can be easily performed by using wave ports in EM simulations. However, as discussed in the last section, the wave ports have tendency of distorting the modes in the CPW and CBCPW structures. The coplanar ground lines and the lower ground plane can be shorted by the port edge like artificial via holes at the end of DUT. This distortion can be avoided by using a lumped port instead. Drawback of this method is that the parasitics of the port as well as of the structures connecting the port to the coplanar structure have to be removed.

This section concentrates on characterization of lumped port discontinu-

ities based on Ansoft HFSS simulations of a simple CBCPW line. Double-delay (L-2L) calibration method presented in [45] is used for that purpose. Reference [45] states that the method is only useful for purely shunting types of the discontinuities. This section will show that an extended L-2L calibration method developed in this work can also estimate and de-embed the series components of the discontinuity assuming a simple connection of a shunt capacitor and a series inductor.

2.3.1 EM Simulations on On-wafer Interconnection Line



(a) (b)

Figure 2.11: (a) Microphotograph of the on-wafer interconnect line structures; (b) Ansoft HFSS setup for the surrounding ground-ring excitation; Each port lies across a gap between the center conductor and the PEC ground bridge

Fig.2.11(a) shows an on-wafer interconnection line which will be used later for verifying the excitation schemes using lumped ports and the extended L-2L calibration method. The line is embedded in a finite ground coplanar waveguide (FG-CPW) transmission media with backside metallization as typically encountered in on-wafer measurements. The interconnection is made in 1 μm thick metal layer and is surrounded by a 3.8 μm thick polymide layer. The substrate of the device is a 650 μm thick InP with ε_r being 12.8. The pads for probe contacting are made of 5 μm thick metal. Conductivity of the metal is 3.33×10^7 S/m. On-wafer measurements were

performed in the frequency range from 250 MHz to 65 GHz using G-S-G probes with a pitch of 150 μm. The reference plane for the measurements was defined at the probe tips by standard SOLT ISS calibration [46].

An EM simulation setup in Ansoft HFSS resembling the on-wafer measurement is shown in Fig.2.11(b). Lumped ports are employed to excite the line. Infinitely thin perfect electric conductor (PEC) sheets connect the two lumped ports to the ground lines. The lumped ports associating with related PEC sheets model the G-S-G probes. They are vertically placed on the top of contact pads and the reference planes for the ports correspond to the measurement setup. This excitation setup is also called "ground ring", because the ground strips of the CPW are connected by PEC sheets forming a ring structure.

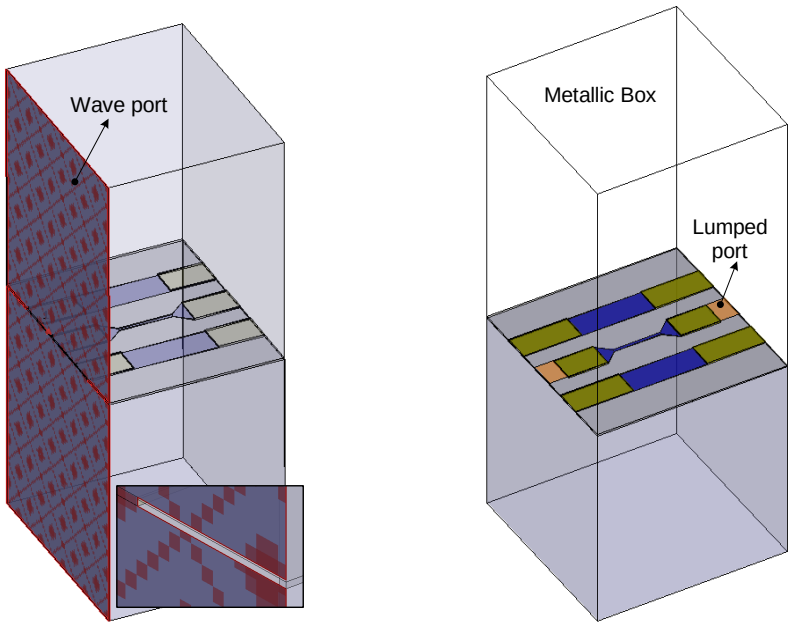


Figure 2.12: The interconnection line are excited by two different schemes in Ansoft HFSS: (a) wave ports; (b) lumped ports with a metallic box.

Two other typical excitation schemes are also used in simulating the interconnection line. One is a wave port excitation as shown in 2.12(a), and the other one is lumped port excitation with metallic box surroundings as shown in 2.12(b). In the case of the wave port excitation scheme no port discontinuity exists in the sense of parasitic elements due to the disconti-

nuity. The wave-port excitation scheme should excite a single quasi-TEM CPW mode consistent with general ideas of circuit theory. It is well-known, however, that the conductor backed FG-CPW structure supports several propagating modes [47]. To ensure the excitation of the correct mode the ground conductors and backside metallization need to be effectively tied together. For the simulation of the conductor backed FG-CPW structure this is normally assured by intersecting both the backside metallization and the ground conductors with the periphery of the wave-port which processes the PEC boundary condition. The lateral size of the wave ports, however, should be larger than three times the overall CPW ground-to-ground spacing in order to terminate the electric field on the ground conductors and not on the wave-port edge. This requirement can not be easily met for the FG-CPW structures investigated in this work unless so-called wave-port fingers are employed to assure that the ground conductors are tied together. The finger form on the wave port is shown in the inset of Fig.2.12(a). To be consistent with the reference plane during on-wafer measurements the simulated S-parameters are de-embedded at a distance into the structure.

In the case of lumped port excitation with metallic box surroundings, the on-wafer interconnection line is surrounded by a metallic box, which is typically associated with a shielded EM simulation. A lumped port located between the signal strip and the metallic box wall excites the structure. The ground conductors are extended to touch the metallic box wall. The size of the metallic box should be chosen such that no box resonances are possible in the frequency range of interest. Notice that the reference plane is set at the edge of the structure in this simulation.

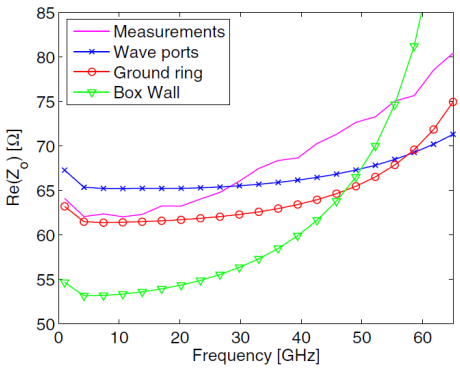


Figure 2.13: Measured and simulated characteristic impedance with different excitation schemes for the on-wafer interconnect line (1 GHz to 65 GHz).

In Fig.2.13, the characteristic impedance for the interconnect line, extracted from measured S-parameters is compared with the results obtained from the respective EM simulation setups. The method of extracting characteristic impedance from S-parameters is described in [48]. To determine the TEM equivalent characteristic impedance of the line, the ABCD-parameters are utilized as follows:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos(\beta l) & jZ_0 \sin(\beta l) \\ j \sin(\beta l)/Z_0 & \cos(\beta l) \end{bmatrix} \tag{2.5}$$

where βl is the electric length of the line and Z_0 is the characteristic impedance of the line. The Z_0 can be calculated by

$$Z_0 = \sqrt{\frac{B}{C}} \tag{2.6}$$

Although no port discontinuity should be associated with the wave-port excitation, the measurement and simulation results do not correlate well. In the wave-port setup the edge of the wave-port acts similar to vias in connecting the ground conductors to the backside metallization. In the actual on-wafer situation the probe ground is connected to the backside metallization through some unknown environmental impedance. Furthermore the wave-port fingers extend the width of the ground planes thus altering the characteristics of the FG-CPW at the excitation reference plane. As a result the wave-port excitation does not resemble the G-S-G probe excitation applied during on-wafer measurements leading to the observed deviation. The surrounding ground ring simulation result shows good agreement with measurement in the lower frequency region. At higher frequencies the deviation is caused by parasitic effects and higher order modes associated with the excitation scheme. The simulation result from the metallic box wall setup shows a large deviation from measurements even at low frequency. In addition to the difficulties already described in connection with the surrounding ground ring, the metallic box wall setup suffers from a shift of the reference plane compared to the on-wafer measurements.

2.3.2 The Extended L-2L Calibration in EM Simulations

None of the results directly obtained from EM simulation agrees the on-wafer measurement results very well as demonstrated previously. The simulation result by the surrounding ground-ring setup is a good candidate for further calibration because its setup is closest to the on-wafer measurement and

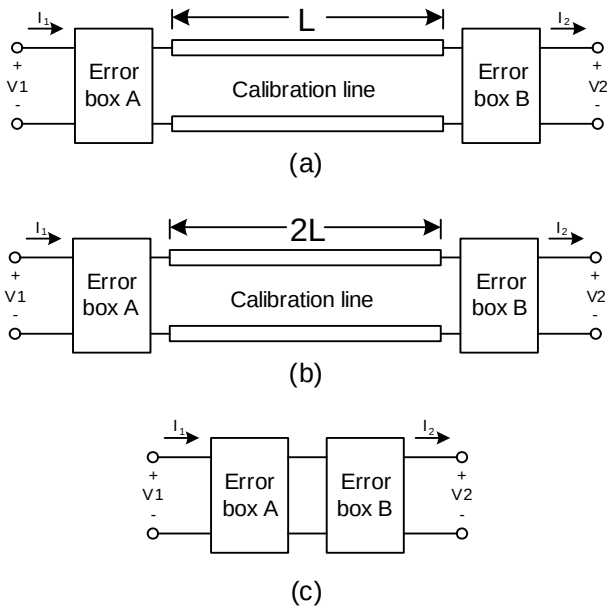


Figure 2.14: Principle of L-2L de-embedding method: (a) Two error boxes exist between ideal excitation and DUT, which is a CPW transmission line for the calibration purpose; (b) The length of the DUT is doubled, and error boxes still exist; (c) The ABCD matrix of two cascaded error boxes is obtained by the L-2L calibration method.

the cause of the simulation result deviation is considered to be the parasitics of the excitation structures. These parasitic elements are supposed to be extracted and removed by L-2L calibration method. The original L-2L calibration method [45] stated that only the purely shunt capacitance can be removed from the parasitics of the excitation. We will show that series elements may also be extracted and removed by the extended L-2L method.

Fig.2.14 shows the theoretical steps for L-2L calibration in EM simulations. Due to the existence of the excitation structure parasitics, there are two error boxes representing such parasitic effects between the lumped port excitation and the DUT in each figure. Two uniform CPW lines with length L and 2L, respectively, are selected as calibration lines for the L-2L calibration method. Other lines such as microstrips are not suitable for G-S-G probe model excitations. The identical surrounding ground ring excitation setup to the on-wafer interconnection line is adopted in simulating L-2L calibration lines. The simulated ABCD-parameters for the L-case are expressed

as

$$T_L = T_A T_{cali,L} T_B \tag{2.7}$$

where $T_{cali,L}$ are the ABCD-parameters of the CPW calibration line with length L, T_A and T_B are the ABCD-parameters of the error box A and the error box B, respectively. Similarly, the simulated ABCD-parameters for 2L-case are expressed as

$$T_{2L} = T_A T_{cali,2L} T_B = T_A T_{cali,L} T_{cali,L} T_B \tag{2.8}$$

The product of T_A and T_B, which is defined as T_{thru}, can be derived by using T_L and T_{2L} as expressed:

$$\begin{aligned} T_{Thru} &= T_L T_{2L}^{-1} T_L \\ &= T_A T_{cali,L} T_B \cdot (T_B^{-1} T_{cali,L}^{-1} T_{cali,L}^{-1} T_A^{-1}) \cdot T_A T_{cali,L} T_B \\ &= T_A \cdot (T_{cali,L} T_B T_B^{-1} T_{cali,L}^{-1}) \cdot (T_{cali,L}^{-1} T_A^{-1} T_A T_{cali,L}) \cdot T_B \\ &= T_A T_B \end{aligned} \tag{2.9}$$

From Eq.2.7 to Eq.2.9, only the product of two error box ABCD-parameters is available according to above calculations. It is not sufficient for eliminating the parasitic effects because the ABCD-parameters of the individual error box are necessary. Therefore, it was claimed that the L-2L calibration was only suitable for removing pure shunt admittance. However, the ABCD-parameters of the individual error box are available even if the circuit model of the error box contains series elements.

For the surrounding ground ring excitation scheme as shown in Fig.2.11(b) a parasitic capacitance can be associated with the fringing field in the vicinity of the lumped port and a parasitic inductance with current flow along the PEC bridge. The equivalent circuit model for the excitation scheme is shown in Fig.2.15(a) associated with the excitation structure and Fig.2.15(b) with an extended line. The voltage source of the lumped port, V_{port}, is assumed to be shunted by a pure capacitance C_{gap}, while the PEC bridge inductance, L_s, is assumed to be in series with the ground conductors of the FG-CPW extension line structure. Since the PEC bridge structure has two branches connected to the two ground strips of FG-CPW in parallel, each branch has double the inductance value as $2L_s$. The extension line (L_{ext}) in Fig.2.15(b) is added at each port to allow the higher order modes generated by the lumped port to decay before reaching the reference plane for model extractions. The influence of the extended lines must subsequently be removed by

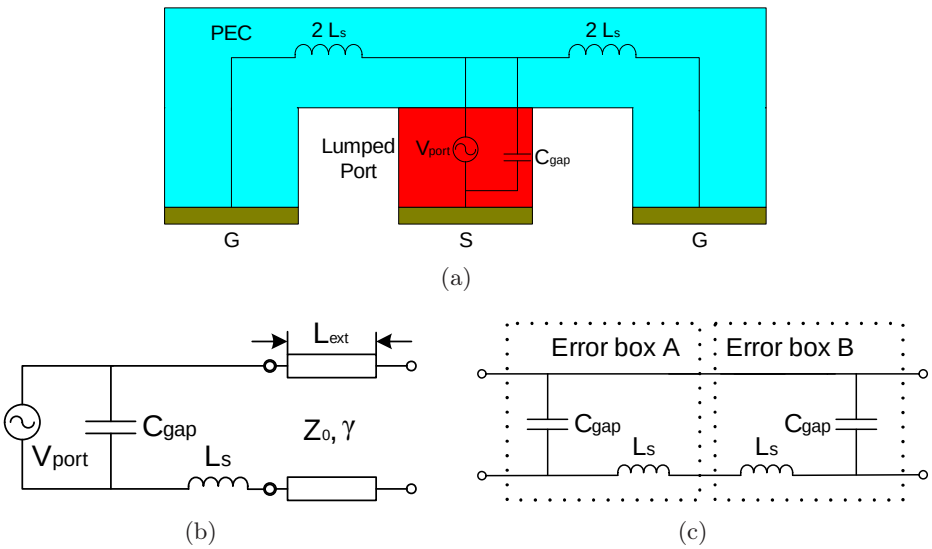


Figure 2.15: (a) Parasitic elements associating the structure of the surrounding ground-ring excitation setup; (b) equivalent circuit model for the parasitics in the ground ring excitation scheme including an extension line of length, L_{ext}; (c) the circuit model of two cascaded error boxes containing series inductances and shunt capacitances.

de-embedding. Fig.2.15(c) shows the equivalent circuit model of two cascaded error boxes due to the excitation structure. The ABCD-parameters of the cascaded error boxes can be expressed as

$$T_A T_B = \begin{bmatrix} A_{thru} & B_{thru} \\ C_{thru} & D_{thru} \end{bmatrix} \tag{2.10}$$

where

$$A_{thru} = 1 - 2\omega^2 L_s C_{gap} \tag{2.11}$$

$$B_{thru} = j2\omega L_s \tag{2.12}$$

$$C_{thru} = j2\omega C_{gap}(1 - \omega^2 L_s C_{gap}) \tag{2.13}$$

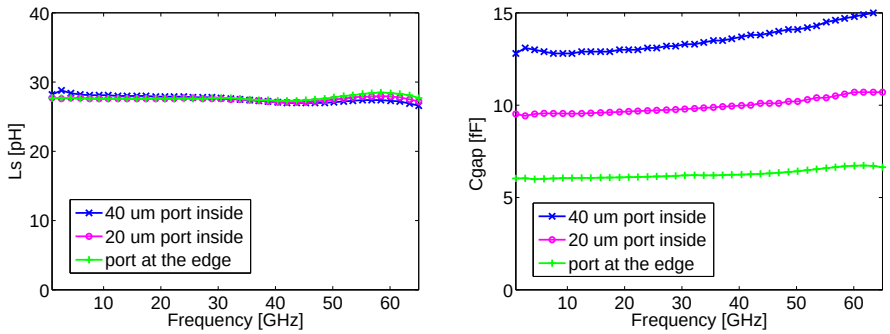
$$D_{thru} = 1 - 2\omega^2 L_s C_{gap} \tag{2.14}$$

where ω is the angular frequency. Based on Eq.2.12, the series inductance can be derived by

$$L_s = \frac{\mathrm{Im}(B_{thru})}{2\omega} \tag{2.15}$$

Through combining Eq.2.11 and Eq.2.13 the shunt capacitance can be expressed by

$$C_{gap} = \frac{1}{\omega}\mathrm{Im}\left(\frac{C_{thru}}{1 + A_{thru}}\right) \tag{2.16}$$



(a) (b)

Figure 2.16: Extracted values of ground ring parasitic elements using extended L-2L calibration method: (a) L_s; (b) C_{gap}. The extracted values with respect to different excitation structure locations are demonstrated.

The extracted values of the series inductance L_s and the shunt capacitance C_{gap} associated with the ground ring excitation scheme are shown in Fig.2.16. A nearly frequency independent series inductance L_s and shunt capacitance C_{gap} are observed for the parasitic elements validating the equivalent circuit model in Fig.2.15(b). The effects caused by the location of the excitation structure are also demonstrated in Fig.2.16. The related illustration of the excitation structure location is shown in Fig.2.17. The "port inside" indicated in Fig.2.17 is consistent with the one in Fig.2.16. It states how much the excitation structure moves inside the calibration line as well as how long the calibration line is outside the reference plane. As indicated in Fig.2.16, the excitation structure is placed at the edge of the calibration line, 20 μm and 40 μm inside the line, respectively. The series inductance L_s is independent of the excitation structure location. That is because the inductance is dominantly determined by the PEC bridge structure. It is almost independent of the location of the excitation structure. On the contrary, the shunt capacitance C_{gap} is strongly influenced by the excitation location. At 10 GHz, C_{gap} is about 13 fF, 9.5 fF and 6 fF when the excitation structure is placed at 40 μm, 20 μm and 0 μm (at the edge) inside the calibration line, respectively. Longer calibration line outside the reference plane results

in larger capacitance value. Furthermore, every 20 μm additional line corresponds to about 3.5 fF at 10 GHz for this structure. This linear relationship is due to the capacitive effect of the calibration lines. When the excitation structure is placed inside the calibration line, the error box does not only include the parasitics of excitation structure but also includes the calibration line outside the reference plane. The extra parasitic capacitance is linear to the length of the extra calibration line. Moreover, the capacitance becomes more dispersive when the extra line is longer. This is not a parasitic elements effect but a typical transmission line characteristic. Therefore, the shunt capacitance is only accurately derived while the excitation structure is placed at the edge of the calibration line. In this case, the series inductance L_s is about 28 pH and the the shunt capacitance C_{gap} is about 6 fF. For accurate model extraction of small-size on-wafer passive components such parasitics can not be neglected.

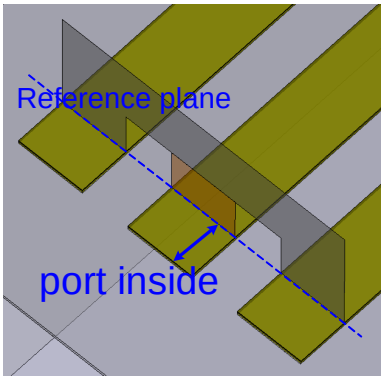
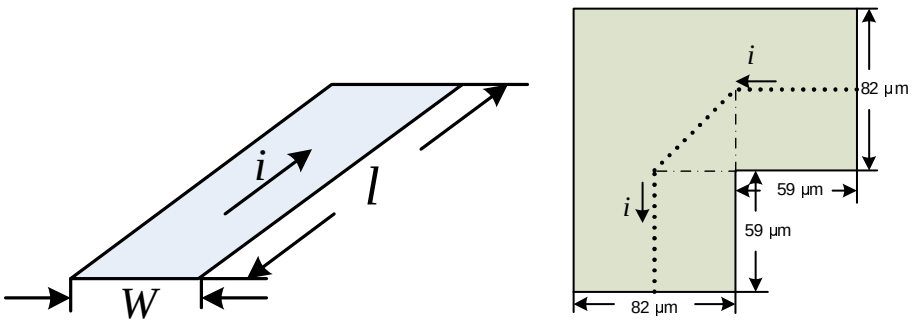


Figure 2.17: Illustration of the location of the excitation structure.

The extracted value of L_s can be approximately verified by an analytical expression for the self inductance of infinitely thin rectangular conductors as shown in Fig.2.18(a) [49]. The expression is written as

$$\begin{aligned} L_{self} = \frac{\mu}{6\pi}\Big\{3\ln[u+(u^2+1)^{\frac{1}{2}}] + u^2 + u^{-1} \\ +3u\ln\left[\frac{1}{u}+\left(\frac{1}{u^2}+1\right)^{\frac{1}{2}}\right] - \left[u^{\frac{4}{3}}+u^{-\frac{2}{3}}\right]^{\frac{3}{2}}\Big\}\cdot l \end{aligned} \tag{2.17}$$

where μ is the permeability of the 2D rectangular structure which is $4\pi \times 10^{-7}$H/m, $u = l/W$, l is the length of the rectangular which is along the current direction and W is the width of the rectangular. Using the Eq.2.17,



(a) (b)

Figure 2.18: (a) A 2D rectangular structure; (b) the half PEC bridge structure with geometry notations.

the partial self inductance of the half PEC bridge structure as shown in Fig.2.18(b) can be roughly estimated. The effective length (l_{eff}) of the structure is selected to be the length of the dot line in Fig.2.18(b). It is the medial axis of the bent 2D structure. l_{eff} is evaluated to be 176 μm, and the effective width W_{eff} is considered to be 82 μm. The self inductance is calculated as 74 pH. Since the structure is only half of the PEC bridge, the series inductance due to the PEC bridge is derived to be 37 pH. Although the value has an error to the extracted one, 28 pH, they still have the same order of the magnitude. The error comes from the inaccurate assumption on the complex PEC structure compared to the simple rectangular geometry. However, the theoretical derivation verifies the existence of the parasitic inductance and the roughly calculated one is at the same order as the extracted one.

Once the parasitics are known it is straightforward to remove their influence from the simulation results. The characteristic impedance for the interconnect line extracted from the EM simulation results after the extended L-2L method has been applied is shown in Fig.2.19. For comparison the characteristic impedance extracted from the uncorrected EM simulation results using the ground ring setup is repeated. The correlation with measurements has been clearly improved especially at increased frequencies where the uncorrected approach was unable to predict the measurement results. It should be noticed that a removal of the parasitic gap capacitance and ground ring inductance from the EM simulation results is not sufficient to obtain such accurate results. It is equally important to add the extension lines at each port to allow the higher order modes to decay to negligible levels before

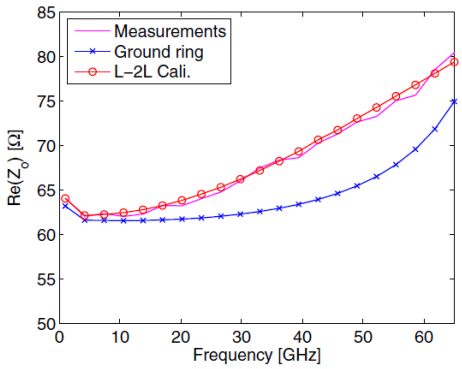


Figure 2.19: Measured and simulated characteristic impedance for on-wafer interconnect line. The simulated characteristic impedance by ground ring excitation scheme is calibrated by extended L-2L method.

reaching the reference plane for model extraction.

2.3.3 Summary

This section demonstrates an efficient calibration procedure, which improves the accuracy of results from EM simulations. This procedure is especially useful for modeling of passive integrated components. It has been shown that in standard EM simulations the excitation ports give rise to parasitics in the simulation domain, which can be modeled with an equivalent circuit comprised of a shunt capacitance and a series inductance. Comparison between measured and simulated results for an interconnect line provides excellent agreement if the simulation data are calibrated using the proposed model. Especially at increased frequencies this procedure ensures accurate results suitable for modeling purposes.

Chapter 3

Electromagnetic Modelling on Conductor-Backed Coplanar Waveguide

Since the coplanar waveguide (CPW) was first introduced by Wen [50] in 1969, it has been considered to be an ideal candidate for interconnecting and packaging functional modules in MMIC systems. Compared to its counterparts such as microstrip lines, the CPW enables simplified fabrication process [51] and possesses easy grounding capability and low dispersive propagation characteristic. Due to the ground planes surrounding the signal strip, the cross talk effects between nearby CPW lines are also very weak [52]. Since the CPW has been widely used in the MMIC systems, the propagation, dispersion and leakage mechanisms of CPW, conductor-backed CPW (CBCPW) and their variations have been comprehensively investigated by scientific researchers [18, 53–61].

A cross section of a CPW with semi-infinite[1] side ground planes is shown in Fig.3.1(a). S denotes the width of signal strip and W denotes the separation of the gap between the signal strip and ground planes. The width of the CPW structure is defined as $S + 2W$ because most of the EM energy of the primary CPW mode exists at this region. Metallization is widely applied at the bottom of CPW forming a CBCPW structure as shown in Fig.3.1(b). The backside metallization increases the capability of the waveguide in the aspects of heat sinking, shielding and mechanical strength. However, such

[1]The semi-infinite side ground plane in reality refers to the ground plane which is much wider than the width of the CPW structure ($S + 2W$) and extends to the edge of the substrate.

backside metallization can couple to the upside ground planes of CBCPW and excite unexpected parallel plate modes [18] which propagate along the waveguide or generate patch antenna mode resonances [62]. These parasitic propagation modes and resonances seriously degrade the transmission performance of CBCPW structures. Therefore CBCPW has to be carefully designed to achieve single mode propagation when it is used as interconnects and packaging structures in millimeter-wave applications. Several solutions have been proposed to prevent the leakage in the CBCPW from single mode propagation to parasitic modes, such as multi-layer substrate [53], optimizations on the dimensions of CBCPW [60] and using vias to short-circuit the ground planes [63].

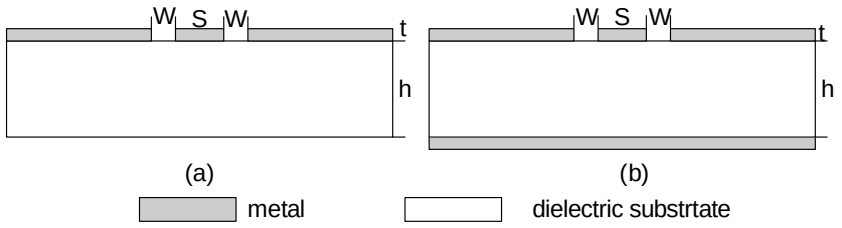


Figure 3.1: Cross sections of (a) CPW and (b) CBCPW with semi-infinite side ground planes[1].

Chapter 2 demonstrates well-developed accurate 3D EM simulation techniques. They are very powerful and efficient for investigating the EM behavior of the microwave devices and components, especially for simulating coplanar structures. The techniques will be used in this chapter to analyze the propagation and dispersion characteristic of conductor-backed coplanar waveguides (CBCPWs) and their relative variation such as CBCPW with vias. The investigation has to rely on the proposed ground-ring excitation scheme, because traditional wave port excitations fail to identify the EM behaviors of some coplanar structures. Accurate 3D EM simulation gives us a straightforward access to the propagation and dispersion nature of CBCPW structures. EM field patterns are also available in the EM simulation results for analyzing the propagation and resonances modes in the structure. These features provide an efficient method of designing packaging and interconnection structures for high speed and millimeter-wave applications.

3.1 Propagation and Dispersion in CBCPWs

3.1.1 CBCPWs with Semi-infinite Side Ground Planes

Propagation Modes

The fundamental propagation mode in the CBCPW with semi-infinite ground planes is illustrated schematically in Fig.3.2(a) as solid lines of the E-field. In reality, the semi-infinite ground planes are the ground planes extended to the edge of the substrate and much wider than the CPW structure. The CBCPW mode is a combination of a CPW mode and a microstrip mode due to the existence of the backside metallization. When the quasi-static condition is applied, the effective dielectric constant of the CBCPW mode, ε_{eff}, and characteristic impedance, Z_0, can be derived as [51]

$$\varepsilon_{eff} = \frac{1 + \varepsilon_r \dfrac{K(k')}{K(k)} \dfrac{K(k_3)}{K(k_3')}}{1 + \dfrac{K(k')}{K(k)} \dfrac{K(k_3)}{K(k_3')}} \tag{3.1}$$

$$Z_0 = \frac{60}{\sqrt{\varepsilon_{eff}}} \frac{1}{\dfrac{K(k')}{K(k)} + \dfrac{K(k_3)}{K(k_3')}} \tag{3.2}$$

where ε_r is the dielectric constant of the substrate, function $K(k)$ is the complete elliptic integral of the first kind,

$$k = \frac{S}{S + 2W} \tag{3.3}$$

$$k' = \sqrt{1 - k^2} \tag{3.4}$$

$$k_3 = \frac{\tanh(\dfrac{\pi S}{4h})}{\tanh(\dfrac{\pi(S + 2W)}{4h})} \tag{3.5}$$

$$k_3' = \sqrt{1 - k_3^2} \tag{3.6}$$

Because of the existence of the backside metallization and wide side ground planes, the CBCPW is eventually surrounded by parallel plate waveguides at both sides. The dominant CBCPW mode has a chance of leaking into the adjacent parallel plate waveguide as parallel plate mode. This leakage degrades transmission characteristic of the CBCPW due to the multimode propagation. Since the EM energy propagates completely within the

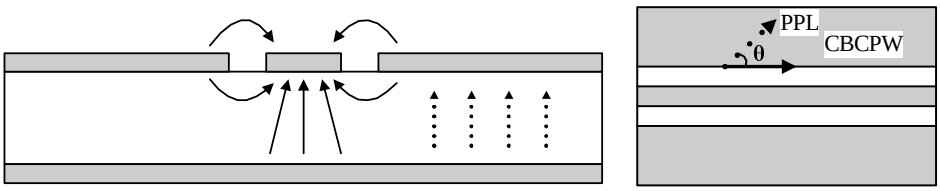


Figure 3.2: (a) Propagation modes in the CBCPW with semi-infinite ground planes: the CBCPW mode (solid lines) and parallel plate mode (dot lines); (b) leakage propagation plot.

dielectric material of the parallel plate waveguide, the effective dielectric constant of parallel plate mode is ε_r which is the relative dielectric constant of the CBCPW substrate. Fig.3.2(b) indicates the modes propagation along the CBCPW structure. The CBCPW mode propagates along the CBCPW structure and the parallel plate mode may leak from the CBCPW mode at the angle of θ, which can be calculated as [54]

$$\theta = \arccos\left(\sqrt{\frac{\varepsilon_{eff}}{\varepsilon_r}}\right) \tag{3.7}$$

If the ratio of ε_{eff} to ε_r is smaller than 1, the leakage angle exists. Otherwise the leakage will not occurs if the ratio is larger than 1, because the leakage angle does not exist. The calculated normalized dielectric constant ($\varepsilon_{eff}/\varepsilon_r$) of the CBCPW is presented in Fig.3.3. The calculation is based on the Eq.3.1 and Eq.3.3 to Eq.3.6. From Fig.3.3, we can conclude that the leakage angle θ always exists because the $\varepsilon_{eff}/\varepsilon_r$ is always lower than 1. That is the phase velocity of parallel plate mode is always slower than the one of CBCPW mode. This means that the leakage from CBCPW mode to parallel plate mode occurs regardless of any cutoff frequencies.

From Fig.3.3, we can also notice that ε_{eff} is not very dispersive with respect to k. But the thickness of the substrate evidently influences ε_{eff}. When the normalized thickness of the substrate approaches small value, the ε_{eff} becomes higher. Most EM power is confined in the substrate region instead of in the open space because the coupling between the signal strip and the backside ground plane becomes stronger. Simultaneously, the leakage angle θ approaches to zero, and the leakage rate will be small. However, the thin substrate also results in strong coupling between the top and bottom side ground planes. This coupling can excite patch antenna mode resonances, which will be discussed as following.

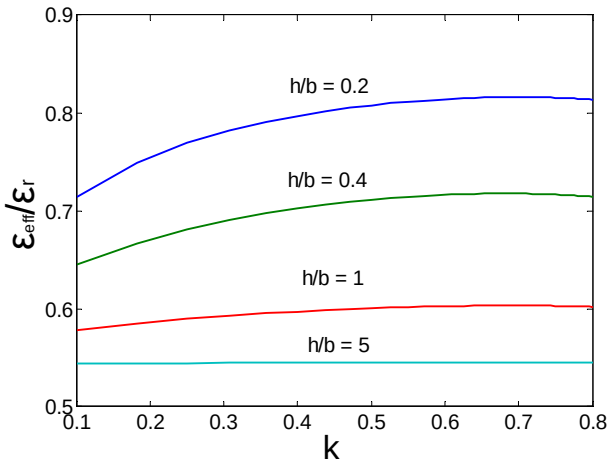
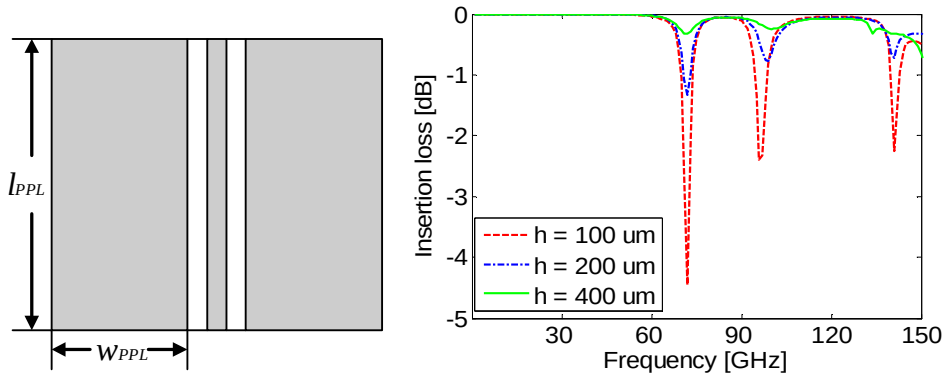


Figure 3.3: Calculated normalized effective dielectric constant, $\varepsilon_{eff}/\varepsilon_r$, of CBCPW as a function of the shape ratio $k = S/(S + 2W)$, with the normalized substrate thickness h/b as a parameters, where $\varepsilon_r = 11.9$ and $b = W + S/2$.

Patch Antenna Resonances

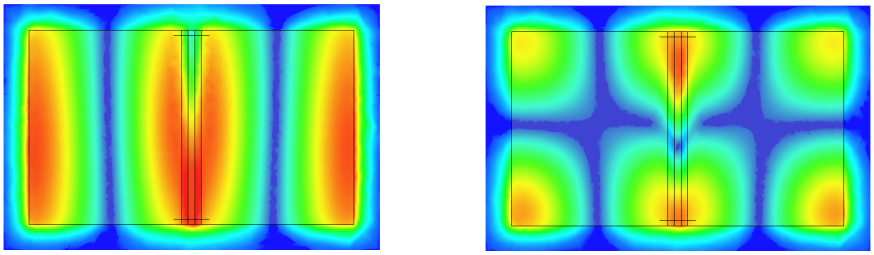
Fig.3.4(a) shows a top view of a CBCPW with wide side ground planes extended to the edge of the substrate, which represents the CBCPW with semi-infinite side ground planes. This structure is used to investigate the resonance phenomena in CBCPW structures by EM simulations. The ground ring excitation setup is used in the simulations. The width of the ground plane, w_{PPL}, is 600 μm, the length of the ground plane, l_{PPL}, is 760 μm, and the width of the signal strip (S) and the gap of the CPW structure (W) are both 25 μm. Since the ground plane is much wider than the CPW structure ($S + 2W$), the ground plane is equivalently considered to be semi-infinitely wide. Both conductor and dielectric material of the DUT are assigned to be lossless in the EM model, and the substrate material is Si (ε_r=11.9). This condition is also used in the subsequent discussions.

Fig.3.4(b) shows that the insertion loss of the DUT has several serious notches in the range of between 1 GHz and 150 GHz. The resonances seriously affect the transmission characteristic of the CBCPW. Fig.3.5 shows the electric field (E-field) patterns in the substrate at the first two resonant frequencies, 72 GHz and 96 GHz. They are typical patch antenna mode resonances [64, 65]. The resonance frequency is determined by the horizon-



(a) (b)

Figure 3.4: (a) The top view of the CBCPW with wide side ground planes; (b) the insertion losses with respect to the varied thickness of the substrate.



(a) (b)

Figure 3.5: E-field patterns in the substrate at resonant frequencies: (a) 72 GHz; (b) 96 GHz.

tal dimensions of the equivalent parallel plate (PPL) composed by ground planes. The dimension of the parallel plate is 600×760 μm^2. The resonant frequencies can be theoretically predicted by

$$f_{mn} = \frac{c_0}{2\pi\sqrt{\varepsilon_r}}\sqrt{\left(\frac{m\pi}{w_{PPL}}\right)^2 + \left(\frac{n\pi}{l_{PPL}}\right)^2} \tag{3.8}$$

where ε_r is the dielectric constant of the substrate, m and n are mode numbers of resonance, and w_{PPL} and l_{PPL} are the width and length of the equivalent parallel plate, respectively. The resonant frequencies of the exhibited mode in Fig.3.5 are f_{10} and f_{11}. f_{10} and f_{11} are 72.5 GHz and 92.3 GHz by applying Eq.3.8, respectively. They agree very well with the simulated

resonant frequencies. According to Eq.3.8, the resonance can be pushed out of the operation frequency range of the application by deceasing the size of side ground planes. Practically, the patch antenna mode resonance can also be suppressed by using vias to short-circuit ground planes.

The magnitudes of the notches vary with different thicknesses of the substrate as shown in Fig.3.4(b). It is obvious that the magnitude of the resonance is determined by the thickness of the substrate when the substrate material is fixed. The thinner is the substrate, the deeper are the notches. When the substrate is 400 μm thick, the notches in the insertion loss are almost negligible. In this case, the thickness of the substrate to the ratio of the CPW structure $(S + 2W)$ is 5.33. It can be concluded that the insertion loss of the CBCPW can be resonance free if the ratio, $h/(S + 2W)$, is larger than 6, when the substrate is Si-based. When the side ground planes are far way from the backside metallization due to the thick substrate, the coupling between the ground planes is much weaker than the coupling between the ground planes and the signal strip. Most of the EM energy is bounded within the CPW structure and hardly couples to the surrounding parallel plate waveguides and excites patch antenna mode resonances.

3.1.2 CBCPWs with Finite Side Ground Planes

As discussed in the last subsection, the backside ground plane of CBCPW is responsible for leakage from the CPW to the parallel plate waveguide and serious patch antenna mode resonances. A practical method of avoiding the resonances can be a reduction of the side ground plane width, known as CBCPW with finite side ground planes. As discussed previously, smaller dimensions of the side ground planes increase the resonance frequencies, which might be out of the frequency range of interest. Since the side ground planes sometimes do not extend to the edge of dielectric substrate, the CBCPW structure is also surrounded by conductor-backed dielectric slabs. Therefore, the dominant CBCPW mode has a chance of leaking into the substrate as shown in Fig.3.6. The leakage mode is TM_0 surface wave. Because of the backside metallization, the parasitic parallel plate mode still exists as shown in Fig.3.2(a). In addition to that, a microstrip-like mode also exists as shown in Fig.3.6.

A sample of CBCPW with finite ground planes is simulated to investigate the transmission characteristic of the structure. The simulation setup resembles the on-wafer measurement setup by using G-S-G probe model for the ground-ring excitation scheme. The substrate of the sample is Si ($\varepsilon_r =$

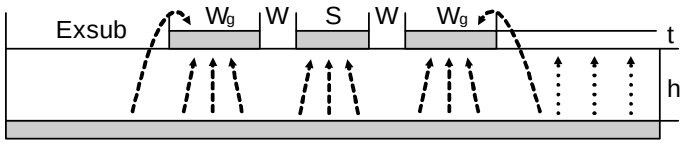


Figure 3.6: The cross section of a CBCPW with finite side ground planes; higher order propagation modes are plotted as microstrip-like mode with dashed lines and surface wave mode with dot lines.

11.9) and all materials are assigned to be lossless[2]. Dimension parameters of the CBCPW with finite side ground planes as indicated in Fig.3.6 are going to be investigated. They are the gap of the CPW structure (W), the width of the signal strip (S), the width of the ground planes (W_g), the width of the outside substrate ($Exsub$), the thickness of the substrate (h) and the thickness of the metal layer (t). A reference CBCPW is defined for the following investigation. When any of dimensions varies in the investigation, the other dimensions are fixed at the values of the reference sample. The dimension values of the reference CBCPW are listed in the Table 3.1. The characteristic impedance of the reference CBCPW is designed to be 50 Ω.

Dimensions	W	S	W_g	$Exsub$	h	t	Length
Values (μm)	25	25	100	200	100	5	760

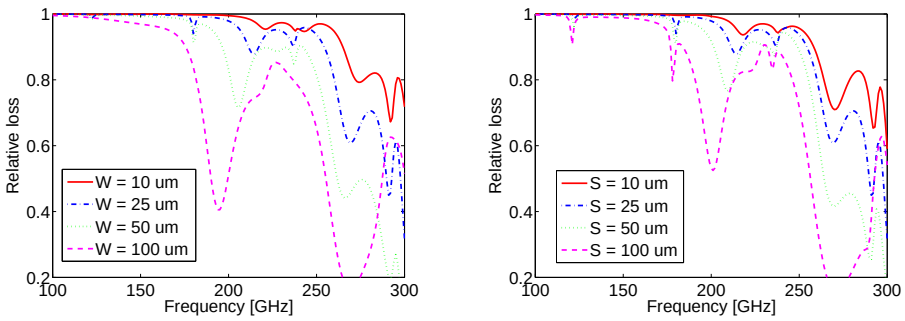
Table 3.1: Dimensions of the reference CBCPW.

Relative loss of the structure is selected to index the transmission characteristic of the CBCPW. It is defined as

$$L_R = \frac{\mid S_{21} \mid^2}{1- \mid S_{11} \mid^2} \tag{3.9}$$

It is a ratio of the transmitted power to the total power delivered on the device. When the L_R is 1, the structure is ideally lossless. When the relative loss of the structure is increased, the value of the L_R will decrease to 0. Another index of transmission characteristic is the group delay, which is a measure of the transit time of a signal through a device (CBCPW here). Poor performance of these two indexes may seriously deteriorate the bit error rate (BER) in high speed transmission systems. Therefore, they are very important to high speed signal transmission.

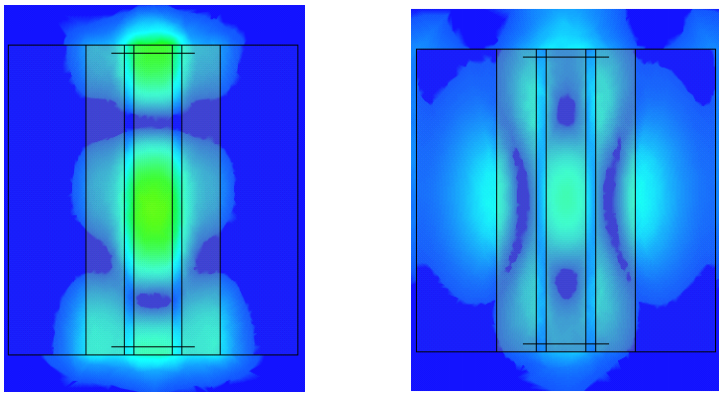
[2]The lossless metal is perfect electrical conductor (PEC) material, and lossless dielectric means the loss tangent $\tan(\delta) = 0$



(a) (b)

Figure 3.7: Simulated relative losses of the CBCPW while (a) varying the gap of CPW structures; (b) varying the width of signal strip.

Width of the gap (W) and the signal strip (S)



(a) (b)

Figure 3.8: E-field patterns in the substrate while $S = 100\ \mu m$ at: (a) 121 GHz; (b) 202 GHz.

In this section, the effects caused by the variation of gap and the signal strip of CPW structures are investigated. Both W and S are chosen as 10 μm, 25 μm, 50 μm and 100 μm while keeping other dimensions constant, even though very wide S and W will invalid the structure as CPW structures. Fig.3.7 shows that narrower gaps and signal strips result in lower relative loss. Wide gaps can not very well conserve EM power in CPW region as dominant CBCPW mode propagation. Wide signal strips easily excite other

modes than CBCPW mode, such as parallel plate mode and microstrip-like mode, because those modes have lower characteristic impedance. Comparing Fig.3.7(a) and Fig.3.7(b), we can see that the relative loss is more sensitive to the gap than the signal strip. Since the width of CPW structure is given by $S + 2W$, the fact of two before the W enhances the influence from the gap. Moreover, the EM power of CBCPW mode is dominantly confined in the gap region.

The curves of relative losses are not monotonic but contain some notches. The notches can be classified in two categories, one with spiculate shape and the other with obtuse shape. These two kinds of notches can be explicitly identified in the curves in Fig.3.7(b). The spiculate notches on the curve of $S = 50\ \mu m$ evenly distribute at 62 GHz (not shown), 121 GHz, 178 GHz, 235 GHz and 290 GHz, respectively. The E-field pattern in the substrate at 121 GHz in the case of $S = 100\ \mu m$ is shown in Fig.3.8(a), because the phenomena is significant in this case. There is a resonance pattern under the ground planes. The order number of the resonance can be counted as two, because the length of the CBCPW is twice of half wavelength long. Very little power leaks into the surrounding substrate in this case. Therefore, the spiculate notches are caused by the resonances in the parallel plate which is composed of ground planes.

The first obtuse notch in the curve of S = 100 μm is at 202 GHz. The E-field pattern at 202 GHz is shown in Fig.3.8(b). The power first leaks into the sideward parallel plates and excites the resonance in the surrounding substrate with backside metallization. The resonances in the conductor-backed dielectric slab hence result in obtuse notches in the relative loss curves. The EM simulations identify that loss mechanism in CBCPW structures is dominantly caused by the power leakage into the surrounding parallel plate composed of ground planes and the surrounding conductor-backed substrate at higher frequencies. The resonances excited by the leakage power seriously deteriorate the transmission performance of CBCPW structures. Smaller CPW dimensions, $S + 2W$, lead to lower loss of the structure.

Fig.3.9 shows the group delays of the CBCPW with different widths of signal strips. It is observed that wide signal strip causes large deviation of the group delay. This result is consistent to the higher relative loss caused by the wider signal strip. Besides the significant deviation, there are some spurs in the curves. They correspond to the spiculate notches in relative loss curves. The magnitude of the spur rises with the magnitude of the relative loss notches. For $S = 100\ \mu m$, the first two spurs below 150 GHz are tolerable for 100 Gbit/s transmission requirement, because the maximum deviation of the group delay is under 10 ps around 121 GHz [66]. However, higher

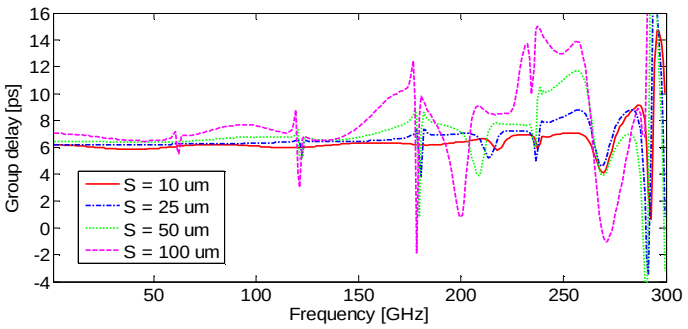


Figure 3.9: Simulated group delays of the CBCPW versus frequency with varied widths of signal strips

deviation will seriously influence the performance of high speed transmission such as the one around 178 GHz, which has the maximum deviation of more than 10 ps. It shows the fact that the CBCPW with 100 μm signal strip width is not suitable for, for instance, 170 Gbit/s data transmission, because unacceptable group delay variation may cause seriously high BER.

Referring to both relative loss and group delay, it is concluded that narrower CPW structures in CBCPWs have better high speed transmission performance. For example, the CBCPW with $S \leq 25\mu m$ and $W = 25\mu m$ can be exploited as interconnection up to 250 GHz applications.

Width of ground planes (W_g)

The width of ground planes determines the dimension of the parallel plate surrounding the CPW structure. As discussed previously, the EM energy may leak into the parallel plate and excite harmful resonances. Fig.3.10 shows the relative losses of the CBCPW with selected widths of ground planes W_g such as 50 μm, 100 μm, 200 μm and 400 μm. Comparing four relative loss curves, wider ground planes lead to lower first resonant frequency. The first strong resonance occurs below 100 GHz for $W_g = 400\mu m$. As mentioned in previous sections, the resonant frequencies can be theoretically predicted by Eq.3.8. Calculated and simulated resonant frequencies are compared in the Table 3.2. The resonance number in the first row is corresponding to the resonance in the relative loss curve for $W_g = 400\mu m$.

The dimension of the parallel plate is usually measured as $W_g \times L$, where L is the length of the CBCPW. When the dimension values of the parallel plate are applied to Eq.3.8, the resonant frequencies are calculated and

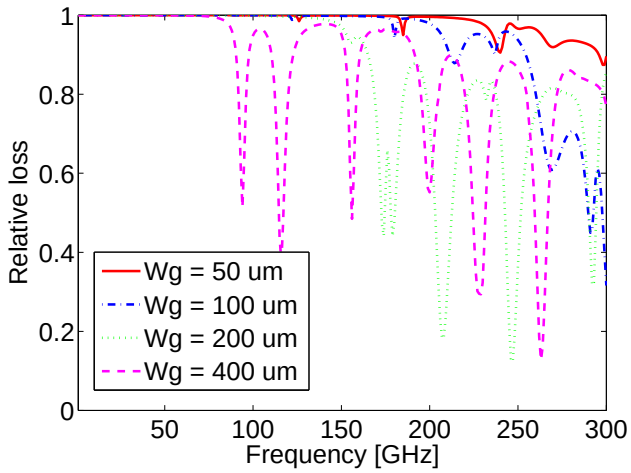


Figure 3.10: Simulated relative losses of the CBCPW while varying the width of ground planes

listed in Table 3.2. Considerable error exists between the calculated and simulated results at most resonant frequencies. That is because the resonant EM fields are not only confined in the parallel plate region but expand to the surrounding uncovered substrate. The calculated error can be calibrated by redefining the dimension of the parallel plate. In the new definition, the CBCPW is considered to be an entire parallel plate with two small slots in top metallization. Obviously, the new definition is based on a compulsory condition, which is that the width of the slot is much smaller than the one of the parallel plate. The width of newly defined parallel plate (W_{PPL}) can be expressed as $2W_g + 2W + S$. When the new dimension values of the parallel plate and new order numbers are applied, the calculated new resonant frequencies are listed at the lower part of the corresponding frequencies. Most calculated resonant frequencies approach the simulated ones. Based on the newly defined parallel plate, the resonance in the CBCPW can be theoretically predicted as patch antenna mode resonance if the slot of the CPW structure is much narrower than the ground planes.

However, the deviation of the calculated results at the third resonances (156 GHz) becomes slightly larger when the new parallel plate definition is applied. The E-field pattern at 156 GHz is shown in Fig.3.11(a). Most of resonant power is restricted under the ground planes region. The pattern under the ground plane exhibits typical patch antenna resonance with $m =$

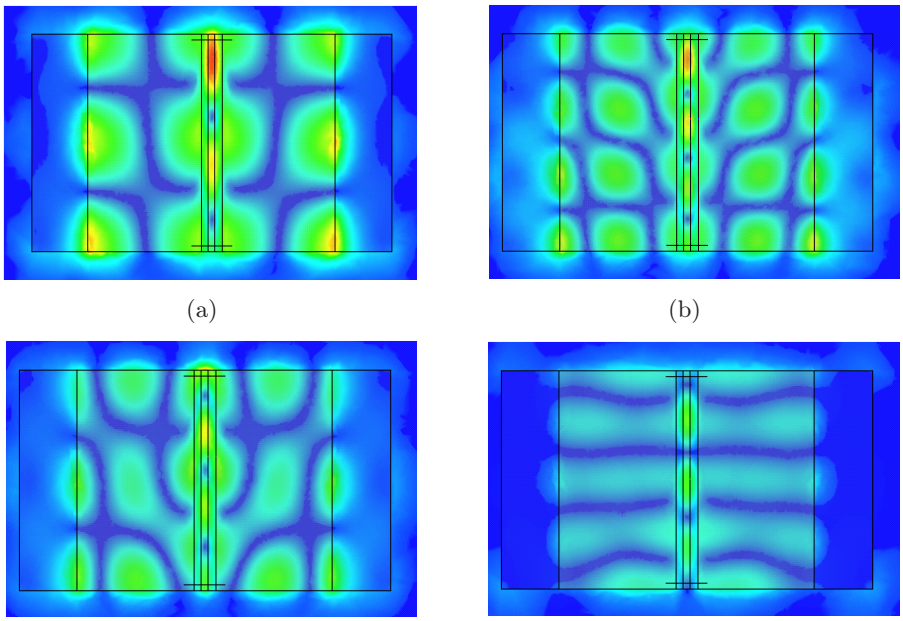


Figure 3.11: E-field patterns ($Wg = 400\ \mu m$) in the substrate at: (a) 156 GHz; (b) 263 GHz; (c) 229 GHz; (d) 229 GHz.

1 and $n = 2$. Therefore the resonant frequency is precisely predicted by considering the parallel plate composed of a solely ground plane. The E-field pattern at 263 GHz as shown in Fig.3.11(b) also exhibits patch antenna resonance, but it is not exactly same as the one in Fig.3.11(a). In the ground plane region, the distance from one maximum of the E-field to another is not exactly half wavelength along the width direction. If the CBCPW is entirely treated as a large parallel plate with two slots on top side, the maximums of the E-field can be regarded as evenly distributing along the width of the large parallel plate. As a result, the calculated resonant frequencies are closer to the simulated ones when the newly defined dimensions of the parallel plate are applied.

Two E-field patterns at 229 GHz are shown in Fig.3.11(c) and Fig.3.11(d). The order of the resonance in Fig.3.11(c) is close to "22", and the order in Fig.3.11(d) is close to "04", when only side parallel plate is considered. It is interesting that two different resonant modes occur at the same frequency and couple with each other. Because the pattern in Fig.3.11(d) is clear as patch antenna mode resonance under ground planes, the calculated resonant

Reson. nr.	HFSS (GHz)	f_{mn}	Calc. (GHz)	Error* (GHz)
1	94	f_{10}†	108.7	14.7
		f_{20}⋇	99.4	5.4
2	116	f_{11}	122.8	6.8
		f_{21}	114.7	1.3
3	156	f_{12}	157.8	1.8
		f_{22}	151.6	4.4
5	229	f_{22} (f_{04})	245.7 (228.9)	16.7 (0.1)
		f_{42}	229.4	0.4
6	263	f_{23}	277.0	14
		f_{43}	262.6	0.4

Table 3.2: Comparison of Simulated and Calculated Resonant Frequencies.
* Absolute value; † $W_{PPL} = W_g$; ⋇ $W_{PPL} = 2W_g + 2W + S$;

frequency by order "04" and using $W_{PPL} = W_g$ is close to the simulated one.

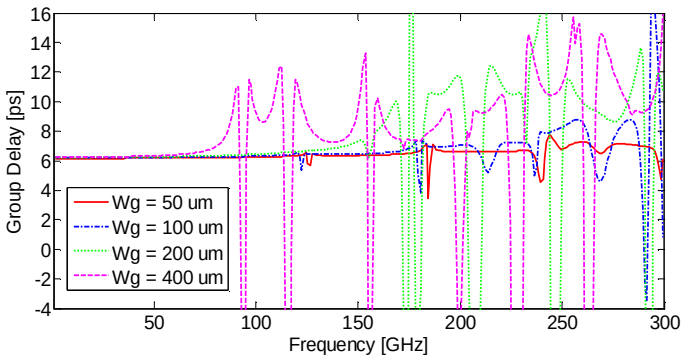


Figure 3.12: Simulated group delays of the CBCPW versus frequency while varying the width of ground planes.

Fig.3.12 shows the group delays of the CBCPW with different ground planes. Narrower ground planes result in less deviation of group delays. For $Wg = 400\mu m$, the first large deviation occurs around 94 GHz corresponding to the first resonant frequency. In this case, the sample can not be used in the application operating higher than 100 GHz.

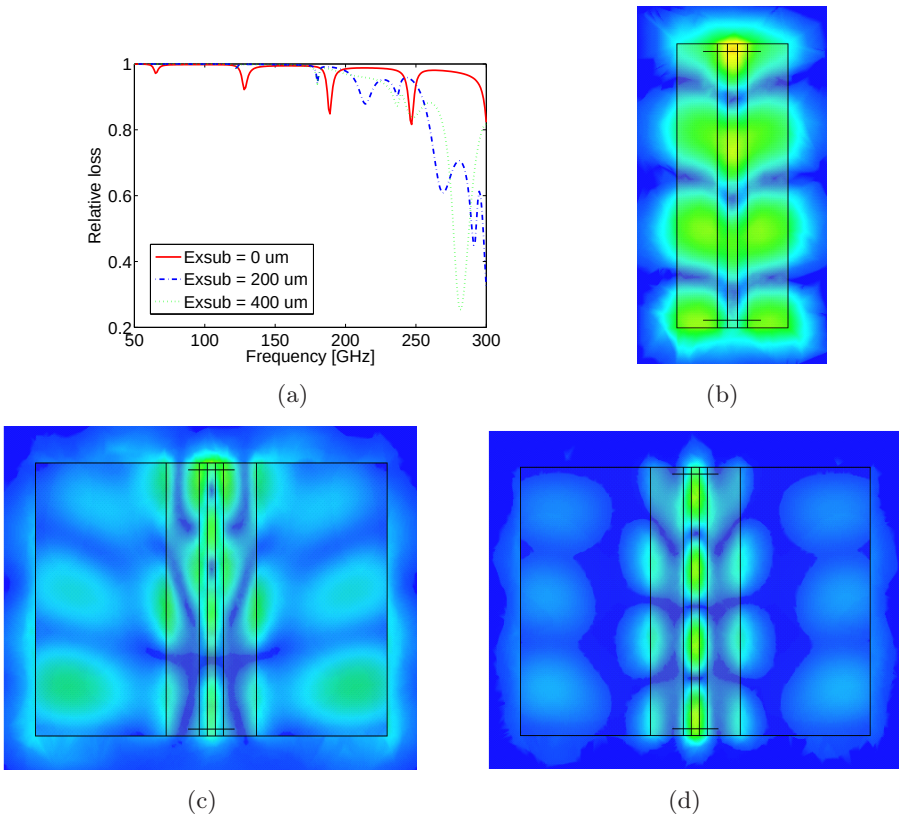


Figure 3.13: (a) simulated relative losses of the CBCPW while varying the width of extended substrate; (b) E-field pattern with $Exsub = 0\ \mu m$ at 189 GHz; (c) and (d) E-field patterns with $Exsub = 400\ \mu m$ at 282 GHz and 300 GHz, respectively.

Width of extended substrate ($Exsub$)

In this part, the effect of the substrate with backside metallization outside the CBCPW structure is investigated. The width of extended substrate, which is indicated in Fig.3.6 as $Exsub$, is selected to be 0 μm, 200 μm and 400 μm, respectively. When $Exsub = 0\mu m$, there is no extended substrate surrounding the CBCPW structure. The relative loss curve as shown in Fig.3.13(a) has periodic notches with increasing magnitude. The E-field pattern at 189 GHz is shown in Fig.3.13(b). Very strong resonant EM power is stored in the parallel plate composed of ground planes. The order of resonance can be clearly counted as three, which is consistent with the third

notch in the relative loss curve. Due the absence of the extended substrate, the EM power is mostly confined in the CBCPW region. Compared to the other two cases with the conductor-backed dielectric slab surrounding the CBCPW structure, the lowest relative loss is achieved with $Exsub = 0$ regardless of the resonant notches, but significant resonances are excited in the parasitic parallel plates.

When the conductor-backed substrate is extended outside the CBCPW structure, the EM power has the chance to leak into substrate modes. The leakage is discussed in previous sections. In this section, we find that the wider extended substrate causes more EM power leakage into the substrate mode and stronger excitation of resonance in the substrate. Fig.3.13(c) shows the resonant pattern at 282 GHz with $Exsub = 400\mu m$. Most of EM power leaks into the adjacent substrate and finally radiates into free space. The order of resonance is hardly recognized from the pattern. The E-field of the pattern is much stronger than the one at 300 GHz as shown in Fig.3.13(d). Both patterns show that there is a very strong EM power at the discontinuity from the parasitic parallel plate to the conductor-backed dielectric slab. It is the source of the power leakage into the substrate.

Thickness of the substrate (h)

Fig.3.14 shows the relative losses of the sample with different thickness of the substrate. The thickness is selected to be 100 μm, 200 μm and 300 μm. Two small notches in the curve of $h = 100\mu m$ at 122 GHz and 180 GHz are absent in the other two curves. The coupling effect between the side ground planes and the backside metallization becomes weaker for thicker substrates. Weak coupling effect leads to less power leakage from CBCPW mode to parasitic parallel plate mode propagations or resonances. In low frequency range, the relative loss of the sample with thicker substrate increases at lower frequencies than the one with thinner substrate and has higher relative loss. That is because the cutoff frequencies of surface-wave modes are lower when the dielectric slab is thicker. Therefore, the sample with thicker substrate has lower frequency at which CBCPW mode starts to leak into surface-wave modes.

Fig.3.15(a) shows the E-field pattern at 223 GHz while $h = 200\mu m$. At this frequency, CBCPW mode firstly leaks into the parallel plate. At higher frequencies, the leakage power excites a resonance in the substrate outside the ground planes. Fig.3.15(b) shows the E-field pattern at 200 GHz while $h = 200\mu m$. Most of EM power is under the CPW region. Very little power leaks into the parallel plate. The leakage power is not strong

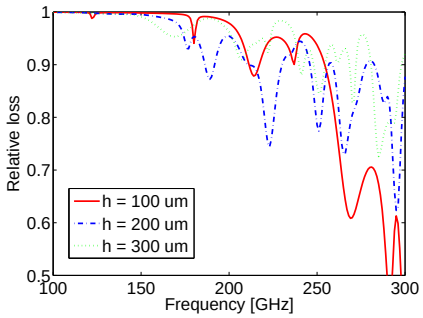
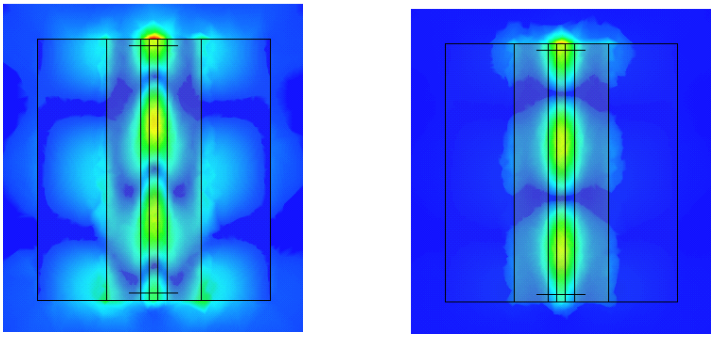


Figure 3.14: Simulated relative losses of the CBCPW while varying the thickness of the substrate.



(a) (b)

Figure 3.15: E-field patterns while $h = 200\ \mu m$ at (a) 223 GHz; (b) 200 GHz.

enough to excite the high surface-wave loss in the surrounding substrate. As a result, the leakage power into the surface-wave is lower in high frequency range, although thicker substrate has lower cutoff frequencies of surface-wave modes. As demonstrated in Fig.3.14, the sample with thicker substrate exhibits lower relative loss performance in the high frequency range.

3.1.3 Summary and Recommendations

This section systematically summarizes the propagation modes in CBCPW structures and analyzes the loss mechanism in the structures by using accurate 3D EM simulations. The characteristics of propagation modes and loss mechanism are determined by the dimensions of CBCPW structures. In

all simulations, the CBCPW is composed of lossless materials. Therefore, the loss in the CBCPW is only caused by the power leakage into parasitic modes and the radiation into free space. The conductor loss, which is also important in millimeter-wave applications, is not taken into account in this section.

For the CBCPW, the coupling effect between the upper side metallization and lower side metallization is considerable when the dimension of CPW regions $(S + 2W)$ is comparable to the thickness of the substrate. The dominant mode is called CBCPW mode. It is different from conventional CPW mode because it is a combination of the CPW mode and the microstrip mode. The power of CBCPW mode may leak into the adjacent parallel plate composed of side ground planes and backside metallization. The leakage power may leak further into the extended substrate outside the CBCPW structure and excite resonances in the substrate. Thicker substrate reduces the coupling effect between the ground planes and backside metallization. As a result, the resonance in the parallel plate surrounding CPW structure becomes weaker. Consistently, if the dimension of CPW structures is much smaller than the thickness of the substrate, the transmission performance of the CBCPW sample is better. In this case, CBCPW is equivalent to CPW because most of EM power is confined in the CPW region.

Several recommendations for practical designs using CBCPW are suggested as follows:

- Coupling effect between upper and lower metallization may be weak enough to be ignored if the ratio of h to $(S+2W)$ is larger than a certain number in the case of fixed substrate. For instance, the number is 6 when the substrate is silicon. The higher is the ratio, the less power leaks into the parasitic parallel plate.

- Keeping the width of ground planes narrow moves the resonant frequencies of patch antenna modes to higher frequency ranges, which may be outside the required operation frequency range.

- The material with low permittivity can be used as the substrate such as quartz. The substrate with low permittivities reduces the electrical dimensions of the CBCPW while keeping geometry dimensions. Large geometry dimensions alleviate the fabrication difficulties, and small electrical dimensions raise higher mode propagations and resonances to higher frequencies than the operation frequency range.

- The absence of extended substrate may keep the power from leaking into the adjacent substrate but strengthen the resonance in the parallel

plate. On the other hand, too wide extended substrate may excite strong resonances in the substrate in the interested frequency range. So the extended substrate should exist with narrow width.

The above suggestions provide principles of designing CBCPW structures with low loss and low dispersive characteristics. Any interconnection designs of CBCPW structures for high-speed and millimeter-wave applications have to follow those principles to achieve good transmission performance. With the increased operation frequency of microwave systems, the requirement of interconnection becomes more and more critical. Two CBCPW structures have been designed for at least 200 GHz applications. One CBCPW is based on silicon ($\varepsilon_r = 11.9$) and the other one is based on quartz ($\varepsilon_r = 3.78$). The dimensions of the CBCPW lines are listed in Table 3.3. They are selected according to the design recommendations.

Dimensions (μm)	W	S	W_g	$Exsub$	h	t	Length
Silicon	22.5	25	100	200	400	5	1000
Quartz	13	50	100	200	400	5	1000

Table 3.3: Dimensions of the CBCPW examples as high-speed interconnects.

Two CBCPW lines are designed to be 50 Ω characteristic impedance. The return loss of the structures can be neglected if they are excited by 50 Ω ports. The simulated insertion losses of sample structures are plotted in Fig.3.16. The solid curves are the insertion loss of the CBCPW structures with lossless materials, which are perfect electrical conductors and substrates with zero of dielectric loss tangent. CBCPWs based on Si and Quartz exhibit excellent transmission performance with less than 0.2 dB insertion loss up to 200 GHz. The performance of the CBCPW based on Si degrades seriously in the range of over 200 GHz with significant attenuation and notches. However, the CBCPW based on Quartz has less than 0.4 dB loss in the range of 200 GHz to 300 GHz. The substrate with low dielectric constant effectively extends the operation frequency range compared to the one with high dielectric constant. This example proves that a good CBCPW line should have large value of $h/(S + 2W)$, small width of ground planes and substrate with low dielectric constant.

In practical, the materials of CBCPW structures are lossy. Fig.3.16 also plots the insertion losses of the CBCPW structures with lossy materials as dashed curves. The conductor is gold, the $tan(\delta)$ of the Si is selected to be 0.01 and the $tan(\delta)$ of the quartz is selected to be 0.0001. The conductor loss is included by assigning DC thickness of the gold in EM simulations.

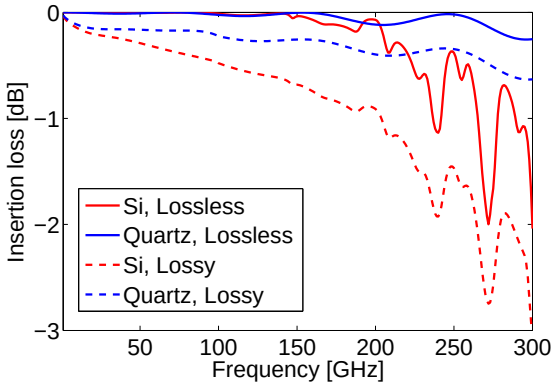


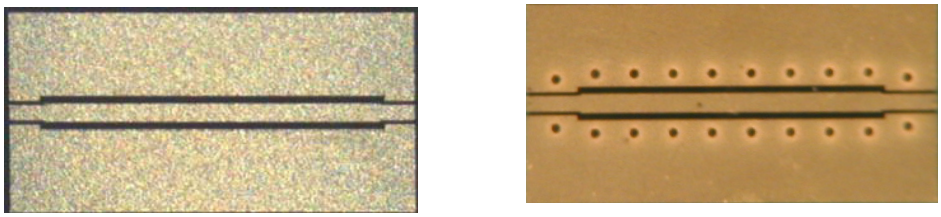
Figure 3.16: The simulated insertion loss of sample CBCPW structures.

Although the loss of the material is included, the CBCPW based on quartz only has less than 0.6 dB loss up to 300 GHz. The lossy materials do not change the profile of the insertion loss curve but only increase the insertion loss of the structure. Higher $tan(\delta)$ of Si brings more insertion loss than lower $tan(\delta)$ of quartz. Low loss material is preferred in designing CBCPW structures and any other interconnects.

3.2 CBCPWs with Vias

The parasitic parallel plate waveguide surrounding the CPW structure is the major cause of loss for CBCPW structures as discussed in the last section. The backside metallization and side ground planes are isolated by dielectric substrate and do not have the same electrical potential. The potential gap between two metal plates induces strong coupling effect when the operation frequency is high enough and the coupling area is large enough. A popular way to suppress such unwanted coupling effect is to short-circuit the top side and back side ground planes utilizing metallic vias in the substrate of CBCPWs. The topside and backside metallization will have the same potential due to the vias. Utilizing vias in packaging coplanar millimeter-wave MMICs was reported in several publications [67–70]. In order to suppress such parallel plate mode as much as possible, strategically placed vias were suggested. For example, vias should be placed as close to the gap in the CBCPW structure as possible in order to achieve optimal transmission characteristics [63].

3.2.1 EM simulations on CBCPV



(a) (b)

Figure 3.17: Photograph of (a) a CBCPW; (b) a CBCPW with vias.

Two CBCPW structures were fabricated as shown in Fig.3.17 by American Technical Ceramics (ATC). They are 4 mm long and 2 mm wide in total. The CBCPW devices consist two types of CBCPW structures. One is with narrow CPW structure and the other is with wide CPW structure. This design is invented for the future opto-electronics device packaging. For the narrow CPW structure at both ends of the device, the width of the signal strip S_1 is 152 μm and the gap W_1 is 43 μm. For the wide CPW structure in the middle of the devices, the width of the signal strip S_2 is 184 μm and the gap W_2 is 80 μm. Both CBCPW structures have 50 Ω characteristic impedance. The substrate is 100 μm thick quartz glass with standard $\varepsilon_r = 3.8$. Low permittivity material is used to push the higher order mode resonances out of the frequency range of the interest, which is from DC to 110 GHz. The metal layer of the CBCPW is 5 μm thick gold. One CBCPW does not have vias but the other one has vias short-circuiting the ground planes. Vias are placed evenly along the CBCPW and close to the gap of the CBCPW structure.

Both CBCPW devices were measured by a vector network analyzer with Ground-Signal-Ground (G-S-G) probes. The measured insertion losses of both devices are plotted in Fig.3.18. The CBCPW without vias exhibits higher insertion loss and more serious resonant notches than the CBCPW with vias. This comparison shows that the vias in the CBCPW structures significantly improve the transmission characteristics of the CBCPW structure. The loss mechanism due to the parasitic parallel plate is effectively alleviated by short-circuiting the ground planes using vias. The CBCPW structure with vias has only around 1dB insertion loss at 110 GHz.

In the insertion loss curve of the CBCPW without vias, an obvious notch exists at about 90 GHz. The notch is corresponding to a resonance at this frequency. The resonance pattern can be examined by analyzing the EM

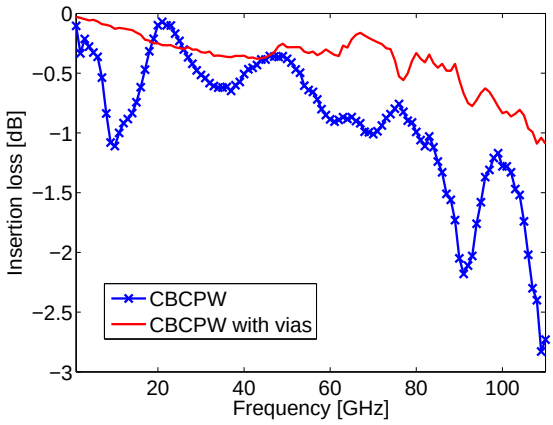
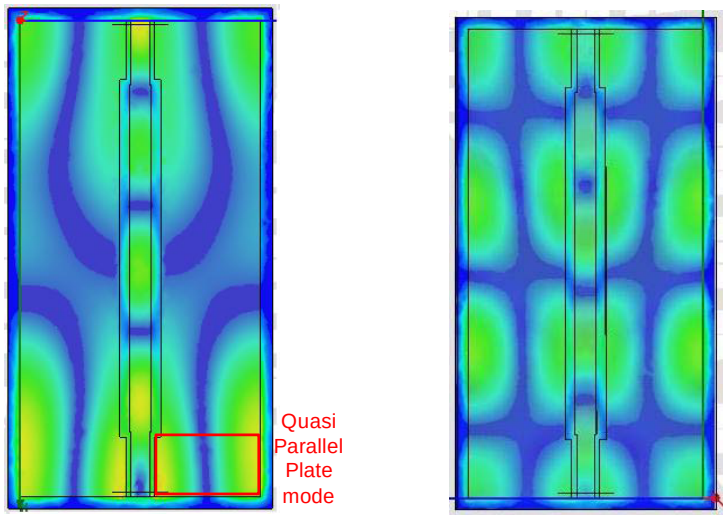


Figure 3.18: Measured insertion losses of the CBCPW and the CBCPW with vias.

field plot in the device. Fig.3.19(a) shows the E-field in the middle of the CBCPW substrate at 90 GHz from EM simulation results. Very strong EM energy exists in the parallel plate composed of ground planes. The pattern demonstrates a quasi parallel plate mode excitation at the end of the CBCPW structure as indicated in the Fig.3.19(a). Fig.3.19(b) also shows the E-field at 110 GHz, which is corresponding to the frequency point with highest insertion loss. A typical patch antenna mode is observed with the order of "3" and "1" along the longitudinal direction and the transverse direction, respectively. The resonance frequency of this mode can be theoretically predicted by Eq.3.8. Since the CBCPW with wide ground plane has the high insertion loss and serious resonances, such a structure is not suitable for the interconnection and packaging structures in high frequency applications up to 100 GHz.

As shown in Fig.3.18, the CBCPW with vias shows excellent transmission characteristic in the entire frequency range. In order to understand the characteristics of the CBCPW with vias, the structure is analyzed by EM simulations. Fig.3.20 shows the simulated insertion losses of the CBCPW with vias by different excitation schemes. The measured one is also in the plot as a reference. When we carefully analyze the measured curve, we notice that the insertion loss curve is not a smooth line. It has several slight notches and fast attenuation in high frequency range. However, the simulated insertion loss with wave port excitation does not have this features. It is a



(a) (b)

Figure 3.19: E-field in the middle of the CBCPW substrate at (a) 90GHz, (b) 110GHz.

perfect smooth line and almost constant between 60 GHz and 110 GHz. The simulation with wave port deviates from the measured one with a large error. If wave port excitation is used to analyze the characteristics of the CBCPW with vias, it is difficult to derive useful information from it. The fact again verifies that the wave port excitation is not suitable for simulations of coplanar structures, especially for the case with backside metallization. This conclusion has been made in Chapter 2.

The ground-ring excitation setup with G-S-G probe models is ideal for simulating the coplanar structures with backside metallization, as discussed in chapter 2. Beside the G-S-G probe model with rectangular-shape PEC bridge as shown in Fig.3.21(a), a newly proposed G-S-G probe model with tapered-shape PEC bridge is shown in Fig.3.21(b). The idea behind this proposal is to resemble the actual shape of the probes, which normally have tapered contacts. Simultaneously, the excited EM energy by the tapered-shape G-S-G probe model resembles more the CPW mode than the rectangular-shape G-S-G probe model. Such tapered-shape PEC sheet contains smaller parasitic inductance than its counterpart with right-angled bends.

As shown in Fig.3.20, the simulated insertion losses of the CBCPW by ground-ring excitation schemes are able to predict several features in the measurement such as the variation with frequency and the attenuation over

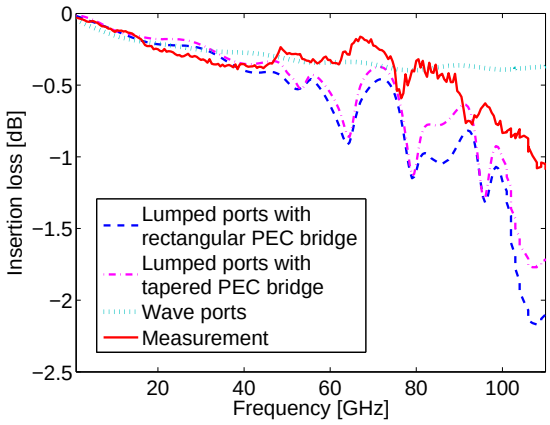
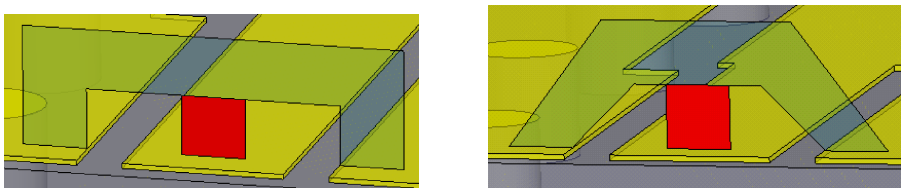


Figure 3.20: The simulated insertion losses of the CBCPW with vias by different excitation schemes.

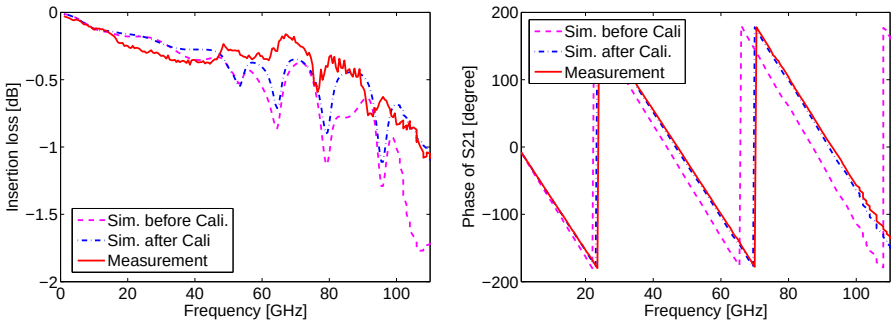


(a) (b)

Figure 3.21: G-S-G probe models in the round-ring excitation scheme in 3D EM simulations: (a) a lumped port with rectangular-shape PEC bridge; (b) a lumped port with tapered-shape PEC bridge.

60 GHz. The simulated insertion loss with tapered-shape G-S-G probe model is closer to the measured insertion loss than the one with rectangular-shape G-S-G probe model. The improvement is more significant in the high frequency range. It is because the discontinuity due to the excitation structure is alleviated by the newly proposed tapered structure, such as smaller parasitic inductance and quasi-CPW mode excitation.

Even with tapered G-S-G probe excitation, there is still difference between the simulated and measured insertion loss. The error is caused by the discontinuity due to the excitation structure even though it is minimized by the newly proposed excitation structure. The simulated insertion loss needs further calibration to remove the parasitic effect due to the artificial excita-



(a) (b)

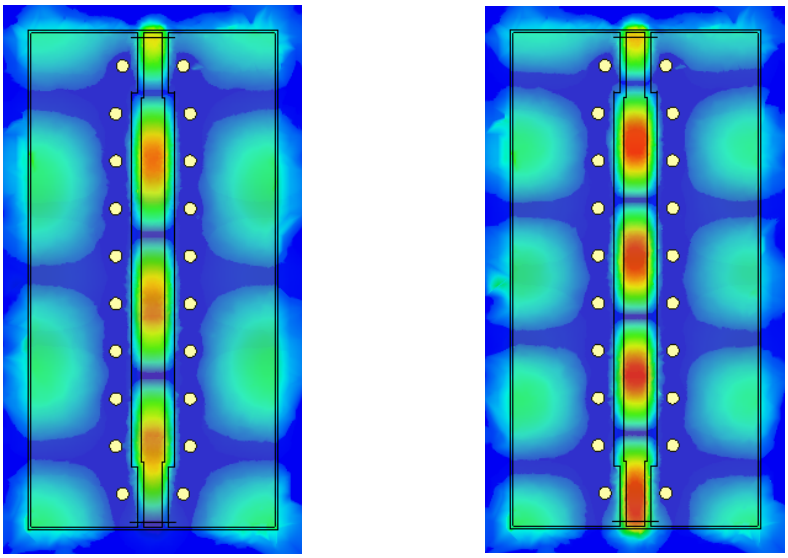
Figure 3.22: The comparison between the simulated results and the measurement results, while L-2L calibration technique is applied to improve the accuracy of the EM simulation: (a) insertion losses; (b) the phases of the S_{21}

tion structure by using the L-2L method as discussed in Chapter 2. When the calibration is applied, the simulated insertion loss gets close to the measured one and the simulated and measured phases overlap with each other. The EM simulation with G-S-G probe model excitation very accurately represents the behavior of CBCPW with vias in the broadband frequency range. Only with accurate EM models of CBCPW with vias, we can further analyze, optimize and design such structures based on EM models.

3.2.2 Resonances in the CBCPW with Vias

Some notch frequencies are observed in the both measured and simulated insertion loss of the CBCPW with vias. Fig.3.23 shows the E-fields in the substrate at two notch frequencies in the simulated insertion loss, which are at 79 GHz and 96 GHz, respectively. The E-field patterns exhibit typical patch antenna mode resonances. Another two resonances with lower order numbers are also demonstrated in the simulation results, although they are not significant in the measurements results.

The resonance frequencies can be predicted analytically by Eq.3.8 For the resonances shown in Fig.3.23, $m = 0.5$, and $n = 3$ for 79 GHz and $n = 4$ for 96 GHz, respectively. The measured, simulated and analytical resonance frequencies are listed in the Table3.4, using $w_{PPL} = 700$ μm representing the distance from the center of the vias to the edge of the upper ground planes, and $l_{PPL} = 3950$ μm which is the length of the upper ground planes. The



(a) (b)

Figure 3.23: The electric-field pattern in the substrate of the CBCPW with vias, (a) at 79 GHz, (b) at 96 GHz

resonance frequencies derived from the three different methods agree well with each other. It is evident that the vias can not eliminate the resonances completely, although they are placed very close to the slot of the CPW structure [63].

Frequency	Measurement	HFSS	Analytical
$f_{0.5,3}$ (GHz)	77	79	80.4
$f_{0.5,4}$ (GHz)	93	96	95.6

Table 3.4: Resonance frequencies comparison

Fig.3.23 reveals that the CBCPW mode energy leaks at the end of the CBCPW with vias to the patch antenna resonances. The impact of the distance d, which is indicated in the inset of Fig.3.24, between the end-via to the edge of the CBCPW, has been carried out, as depicted in Fig.3.24. It demonstrates that the closer the end-vias are placed to the edge of the CBCPW structure, the lower insertion loss and less significant resonances are visible. It is concluded that the energy leakage can be inhibited by placing vias close to the edge of the CBCPW structure. Moreover, the

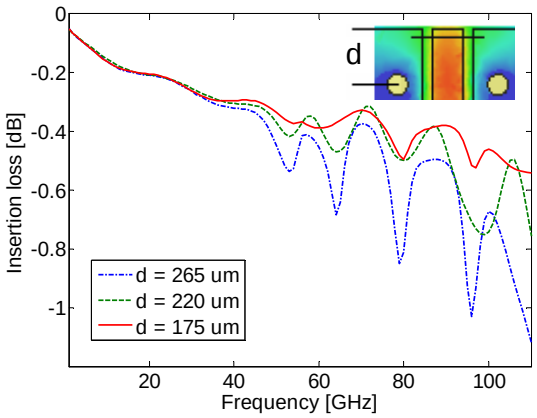


Figure 3.24: Simulated insertion losses of the CBCPW with vias for varied distances between the end vias and the edge of CBCPW.

energy leakage can also take place between vias if the distance between these is sufficiently large and should therefore be also chosen appropriately for the highest frequencies of operations.

3.2.3 Summary

In the EM simulation setup on the CBCPW with vias with wave port excitation, the periphery of the wave port short-circuits the upper and lower ground planes at the end of the CBCPW. This setup artificially prevents the energy leakage taking place at that area. Unrealistic transmission characteristic of the device is simulated by using wave ports. This is the main reason for the deviation of the simulation results from the measurement results. However, the unrealistic transmission characteristic due to wave port excitation is low loss and free of resonances. We can utilize this property to realize interconnects with excellent transmission characteristic in a broadband frequency range. Vias can be placed exactly at the edge of the CBCPW to suppress the energy leakage at the end of the CBCPW. The characteristic of the insertion loss will be notch free and the insertion loss at 110 GHz can be improved from over 1 dB to less than 0.5 dB.

An approach of designing CBCPW-based interconnects can be summarized at the end of this chapter:

1. EM models of CBCPW structures have to be firstly developed. The dimensions of the structure are determined by the specifications of appli-

cations such as impedance matching requirement and package spacing limitations.

2. The ground-ring excitation scheme with simple G-S-G probe models is mandatory to be used in EM simulations. This is the only correct excitation method for simulating coplanar structures.

3. Simulation results including S-parameters and field plots need to be analyzed to obtain the EM behavior of CBCPW structures. The optimization of CBCPW structures is based on the simulated EM property of the structure, for instance eliminating the notches in the transmission characteristic of the structure and reducing the insertion loss of the structure.

4. Keeping vias distance short and placing vias at the end of the CBCPW for short-circuiting the coupling between upper-side and backside ground planes are efficient to achieve excellent transmission characteristic of CBCPW structures.

Chapter 4

Electromagnetic Modelling on Photodetectors

A photodetector (PD) is a solid-state sensor that converts received optical signals into electrical signals. In order to achieve a high optical to electrical conversion efficiency and high bandwidth the p-i-n photodiode is widely used in PDs [71]. The p-i-n photodiode consists of an intrinsic absorbtion layer, sandwiched between a highly doped $n+$ and $p+$ layers which provide a space charge region. The optical power is absorbed by the p-i-n junction to generate electron-hole-pairs. As long as an external electric field exists, a current is induced. The high speed PDs are the key components in the receiver end of optical communication systems for hundreds gigabit per second data transmission [72]. In addition to the communication application, the PDs also works in terahertz (THz) range in photomixer applications for security screening and medical imaging [73, 74].

When the operation frequency approaches millimeter-wave range or even THz range, the parasitic effects in PD chips may seriously deteriorate the performance of the device. The bandwidth and absolute output power can be severely limited by the parasitic effects. These effects mainly originate from the electromagnetic (EM) property of PDs, such as the capacitive coupling between the anode and cathode of the photodiode. Therefore, developing EM models for the PD chips is an efficient way to investigate those unwanted effects and optimize the PD structures. The EM model of PDs can be further used in designing the packaging of the PD modules.

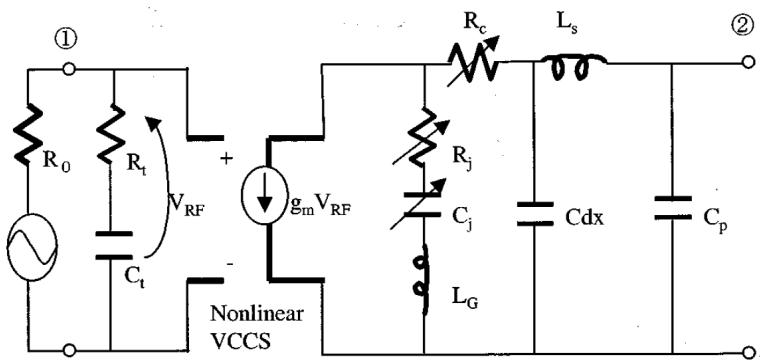


Figure 4.1: A small-signal circuit model of p-i-n photodiodes.

4.1 The Circuit Model of P-I-N Photodiodes

Fig.4.1 [75] shows a small-signal circuit model of p-i-n photodiodes. The model involves both the parasitic effects due to the passive structure on the photodiode chip and the transit-time effect of the p-i-n junction. Since the bandwidth of the photodiodes is considered to be independently affected by those two effects which have Gaussian response [76], the 3-dB bandwidth of PD, f_{3dB}, can be approximated as [72]

$$\frac{1}{f_{3dB}^2} = \frac{1}{f_t^2} + \frac{1}{f_{RC}^2} \tag{4.1}$$

Therefore, those two effects can be modelled separately. The passive RLC network at the right-hand side of the voltage-control-current source (VCCS) is the equivalent circuit of of parasitic elements, and the RC network (indicated as R_t and C_t) combined with the VCCS models the transit time effect. The leftmost voltage source associated with a series resistance, R_0, models the input optical signal source. R_0 is the source impedance. The nonlinearity of the VCCS can be approximated as linearity if the input power is at the small signal level. As reported by [75], a good linearity is observed if the input power is below 10 mW (10 dBm).The nonlinear VCCS as indicated in Fig.4.1 is universal for both small and large signal operation if the linearity is considered as a special case in the nonlinearity.

Although the circuit model can precisely predict the optical-to-electrical response, it is not convenient for optimizing the passive parasitics on the chip and designing 3D packaging structures for high frequency applications. In the circuit model, the precise values of the parasitic elements are extracted

by tuning the parameters to fit the measurement results. If full 3D EM models of PDs can be developed to describe the behavior of the device, the model will provide an straightforward access to the parasitics of the device and to the design of surrounding complex 3D structures for interconnecting and packaging the devices. Since the circuit model of PDs can be simplified as a linear two-port network in small signal operations, it is possible to realize full 3D EM model of PDs in EM simulators

4.2 Behavioral EM Models of Photodetectors

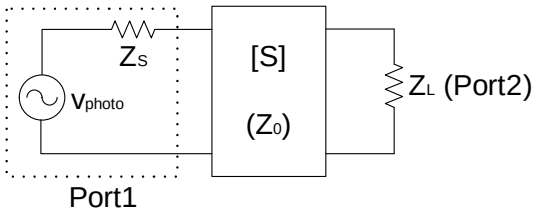


Figure 4.2: An EM behavioral model of PDs is represented by a two-port network.

EM models usually refer to passive structures in microwave and millimeter-wave applications. This section, however, will demonstrate that PDs as active devices can be modelled at behavioral level in EM simulations. Since PDs are opto-electronic (O/E) devices, the behavioral model for such devices intends to accurately describe the O/E response of the devices. The O/E response of PDs, R_{PD}, is defined as

$$R_{PD} = \frac{P_{el}}{P_{opt}} \tag{4.2}$$

where P_{opt} is the input optical power and P_{el} is the output electrical power. The O/E response is also the O/E power gain of the PD according to its definition. For any arbitrary EM model with two-port network, an S-matrix can be obtained from EM simulation results. As indicated in Fig.4.1, the PD circuit model is considered as a two-port network. Port ① generates optical input power and port ② collects the electrical output power. After generalizing the equivalent circuit of the PD by a two-port S-matrix, Fig.4.2 shows a block diagram of a two-port network for EM behavioral models of PDs. The port1 with a voltage source (v_{photo}) and a port impedance (Z_S)

generates the optical power. The port2 is the load of the PD to absorb the output power. The $|S_{21}|^2$ is equivalent to the power gain of the two-port network if the output and input ports are both matched [77]. Therefore, the S-parameter of the EM behavioral model, S_{21}, will be used to characterize the O/E response of the PDs in small signal operation.

Modelling P-I-N Junction

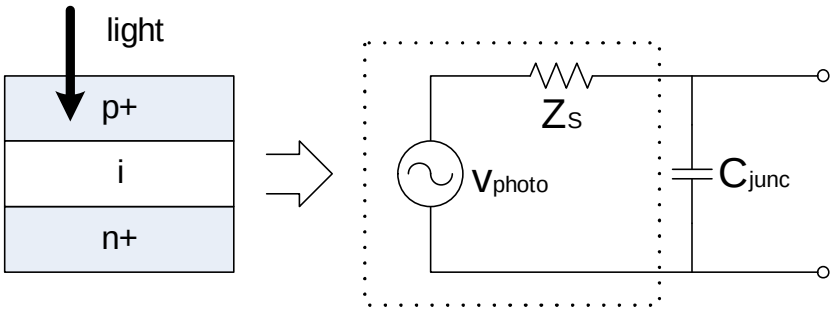


Figure 4.3: The structure of p-i-n junction and the equivalent circuit model of the p-i-n junction.

The active part of the PD is the embedded p-i-n junction, where the photocurrent is excited. The equivalent circuit model of the p-i-n junction and the schematic of the structure are shown in Fig.4.3. The p-i-n junction, which is illuminated vertically, is modelled by a power source consisting of a voltage source and the source impedance, and a junction capacitor, C_{junc}. The C_{junc} exists in the built-in parallel plate structure formed by isolated $p+$ and $n+$ layers. It can be modelled by a 3D p-i-n junction or a lumped element between two electrodes. The capacitor is the dominating effect which limits the output power and 3-dB bandwidth. Its value can be calculated by

$$C_{junc} = \frac{\varepsilon_0 \varepsilon_r A}{d_{abs}} \tag{4.3}$$

where ε_r is the relative dielectric constant of the intrinsic absorption layer, A is the area of the layer and d_{abs} is the thickness of the layer.

The power source can be modelled by a lumped port in EM simulators. The port will generate electrical power which represents the input optical power and deliver it to the load impedance through the passive structure of the PD. v_{photo} combined with Z_S is the model of lumped port as well

as the model of input power source. The source impedance, Z_S, has to be carefully determined based on different PDs, because it determines the portion of the power delivered to the PD EM model. For example, the high speed PD designed in 50 Ω impedance system requires 50 Ω source impedance to guarantee that maxim input power can be delivered to the PD. For the unknown impedance system, the impedance can be tuned by fitting the measurement results.

Equivalent Circuit Model for Transit-Time Effect

The 3-dB bandwidth is an important parameter to evaluate the performance of high-speed PDs. If the bandwidth of the PD is narrow, the bit-error-rates (BER) in data transmission systems increase dramatically. The output power in THz range may also not reach the required THz power. There are two major effects constraining the bandwidth of the PDs. One effect originates from the *RC* network due to the passive structure of the PDs, and the other one is from the transit-time effect because of the carrier drift. The total relative frequency response including *RC* and transit-time effects can be expressed in the frequency domain as

$$H_{PD}(\omega) = H_{RC}(\omega) \cdot H_t(\omega) \tag{4.4}$$

The *RC* network is intrinsically included in the passive structure of the EM model. The junction capacitor, C_{junc}, can be modelled by either 3D p-i-n junction or a lumped capacitance between the anode and the cathode. However, the transit-time effect is not straightforwardly included in EM models. The frequency response of the transit-time effect, $H_t(\omega)$, can be expressed as [71, 78]

$$H_t(\omega) = \frac{1}{\omega^2\tau_h^2}(1 - j\omega\tau_h - e^{-j\omega\tau_h}) + \frac{1}{\omega^2\tau_e^2}(1 - j\omega\tau_e - e^{-j\omega\tau_e}) \tag{4.5}$$

where τ_e and τ_h stand for the electron and hole transit times through the depleted layer to the contacts. The transit time can be calculated by $\tau_{e,h} = d_{abs}/v_{e,h}^{sat}$, where $v_{e,h}^{sat}$ is the saturated drift velocities of electrons and holes. The transfer function exhibits typical low pass characteristics in the frequency domain. In order to include this transfer characteristic in the EM behavioral model of PDs, an equivalent circuit model with similar characteristic has to be developed. A circuit with low pass property, as shown in Fig.4.4, is selected to model the behavior of the transit-time effect because the transit-time effect has typical low-pass characteristic in the frequency

domain. A LC network with a series L_t and a shunt C_t is inserted between the source impedance R_S and the load R_L. Both series inductance and shunt capacitance possess the capability of blocking high frequency signals. Furthermore, two elements for limiting high frequency signals enhance the flexibility of the equivalent circuit to model the transit-time effect. Another issue is that the circuit model can not be too complex, if it is going to be implemented in 3D EM simulator. Complicated circuit models in 3D EM simulations will introduce more interconnection structures, which bring unexpected parasitics in the model. Since there are only two components in the proposed circuit model, it is easy to be realized in the 3D EM model with very little parasitics.

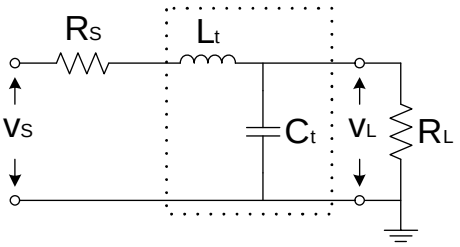


Figure 4.4: A LC low pass filter to model the transit-time effect.

The transfer function of the circuit model with respect to the input and output voltage is written as

$$H_v(\omega) = \frac{v_L(\omega)}{v_S(\omega)} = \frac{R_L}{R_S + R_L - \omega^2 L_t C_t R_L + j\omega(C_t R_S R_L + L_t)} \tag{4.6}$$

$H_v(s)$ is a second order low pass filter, which models the transfer characteristic of the transit-time effect. The frequency response of the circuit is determined by L_t and C_t. Fig.4.5 shows the frequency characteristics of the transit-time effect, $H_t(\omega)$ and the circuit model, $H_v(\omega)$. The transfer function of the circuit model is normalized to the DC value, $R_L/(R_S + R_L)$ in Fig.4.5. When the values of L_t and C_t are tuned, a good agreement between the frequency characteristics of transit-time effect and the circuit model can be achieved as demonstrated in Fig.4.5. The family of the solid curves are the $H_t(\omega)$ corresponding to different p-i-n junction structures with different intrinsic layer thicknesses. Through tuning L_t and C_t, the frequency characteristic of the circuit fits the characteristic of varied p-i-n junction structures very well. Therefore, the transit-time effect can be behaviorally modelled

by an equivalent circuit with a series inductor and a shunt capacitor. The lumped circuit should be placed between the power source and the electrodes of the photodiode. The input power delivered to the 3D structure will include transit-time effect, which is consistent with the case of real photodiode device. In the practical behavioral models of PDs, C_t is absorbed in C_{junc} because both of them are located between the same electrodes. So, the value chosen for C_{junc} should be slightly higher than the physical one, then C_{junc} and L_t can precisely model both the transit-time effect and the junction capacitance.

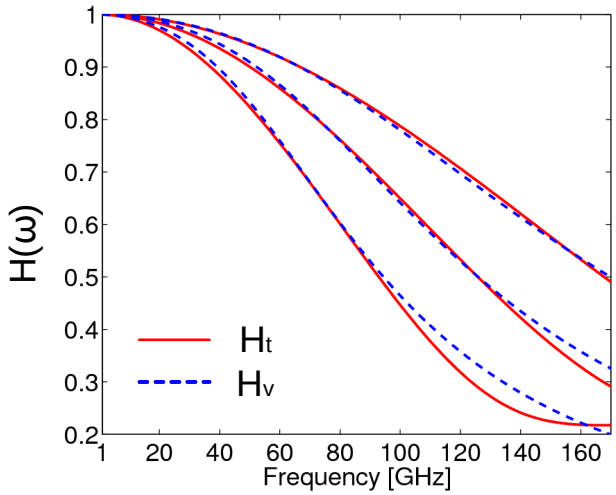


Figure 4.5: The transfer function of transit-time effect by Eq.4.5 and low pass filter by Eq.4.6: the solid lines refer to the transit-time effect for different p-i-n junction structures; the dashed lines refer to the circuit model with different parameters.

A Behavioral Model of A Broadband Photodetector

A broadband PD used in optical telecommunication systems is shown in Fig.4.6(a). It was developed by Heinrich Hertz Institut in Germany. The p-i-n junction is located in the center of the chip for sensing the incoming optical power. It is connected to the electrodes which exhibit a CPW structure. A 50 Ω matching resistance is connected to obtain broadband characteristic. The output ground-signal-ground (G-S-G) contact pads are also designed to be 50 Ω CPW for impedance matching. In the EM model of the PD

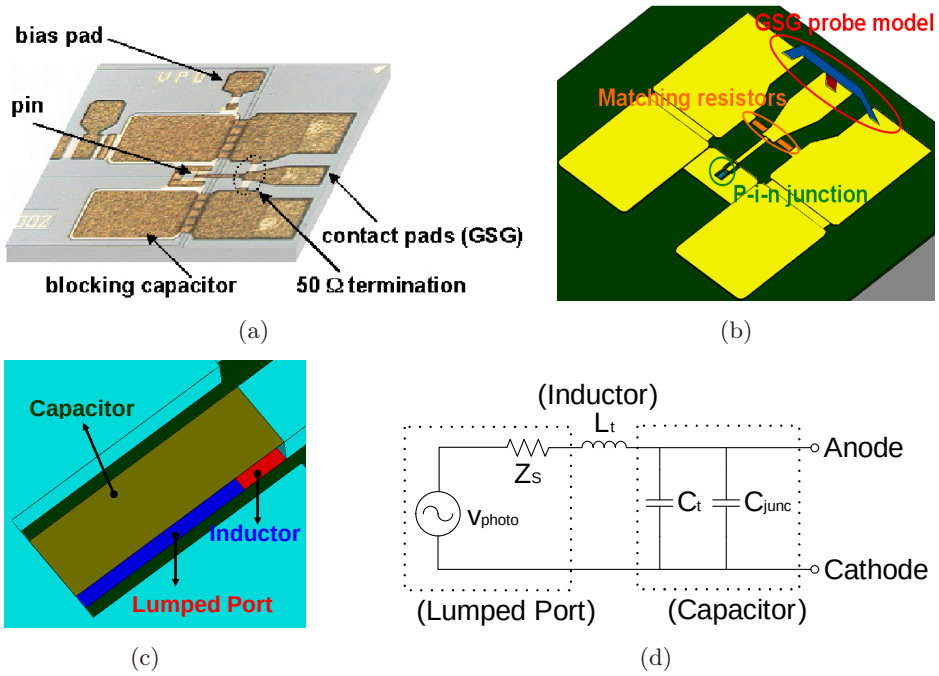


Figure 4.6: (a) The chip layout of the broadband PD; (b) the EM model of the broadband PD; (c) the EM model schematic of the p-i-n junction; (d) the equivalent circuit model of the p-i-n.

as shown in Fig.4.6(b), the passive structure resembles the real device such as identical metal layouts. The 50 Ω matching resistors are modelled by lumped elements at the exact place as it is on the device. A G-S-G probe model resembles the probe used in on-wafer measurements.

The simulated O/E response will be compared to the on-wafer measurement results. The EM model intends to reproduce the measurement setup in EM simulations. As discussed in chapter 2, the parasitic due to the G-S-G probe model has to be removed by EM calibration techniques to achieve accurate EM simulation results compared to the measurement results. The detailed schematic of the p-i-n junction is shown in Fig.4.6(c). A lumped port is in series with a lumped inductor. A lumped capacitor is parallel with them. The equivalent circuit model consistent to the p-i-n junction EM schematic is shown in Fig.4.6(d). The lumped port generates the input power. The inductor and capacitor model both transit-time effect and junction capacitance. Since the lumped port is connected to the well-designed 50 Ω impedance system, the port impedance is assigned to be 50 Ω to avoid

unwanted reflection at the interface between the port and the 3D structures. The input power can be delivered to the 3D structure without any additional loss.

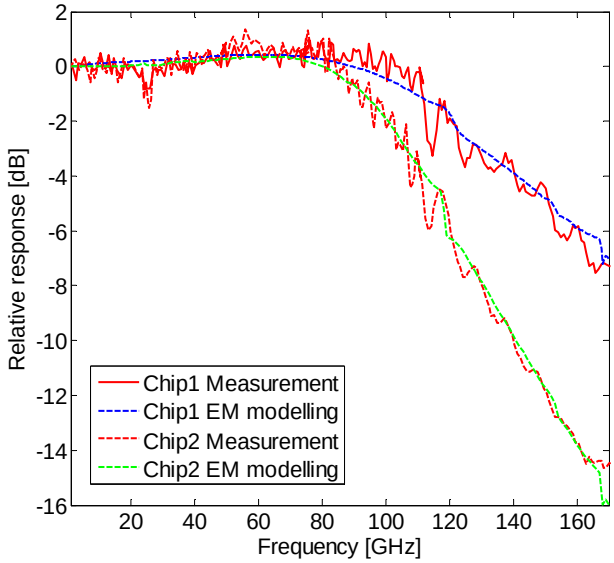
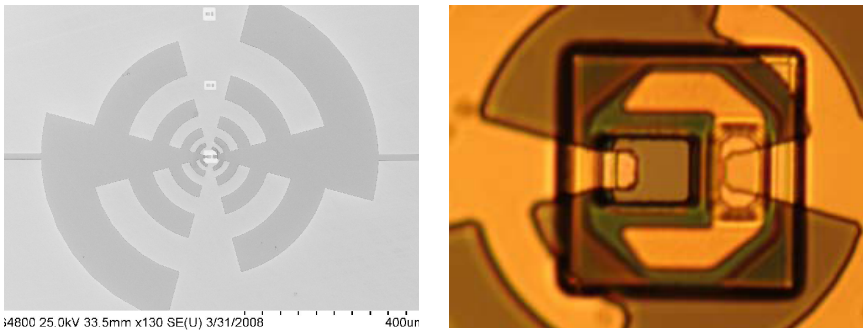


Figure 4.7: The comparison between the simulated and measured relative responses of the broadband PD.

When the model is meshed at 130 GHz, one simulation to obtain the frequency response in full frequency range runs for about 17 minutes on an Intel Core2 Duo CPU@3GHz PC with 3.5GB of RAM. S_{21} derived from EM simulations is the simulated O/E response of the PD. Fig.4.7 plots the comparison between the simulated and measured relative O/E responses of the broadband PD. The response is relative because it is normalized to the response at lowest frequency point. There are two types of PDs under investigation. They have almost identical chip design except for different p-i-n junction dimensions such as the thickness and area of the intrinsic layer. This fact means they have different transit-time effects and junction capacitances. Fig.4.7 demonstrates excellent agreement between the simulated and measured relative responses for different PDs. Through tuning of the values of the inductor and capacitor, the 3D EM behavioral model of the PD is valid for various p-i-n junction dimensions. The model will be utilized in further PD module packaging designs.

4.3 Optimization of Photodetectors for THz Photomixers

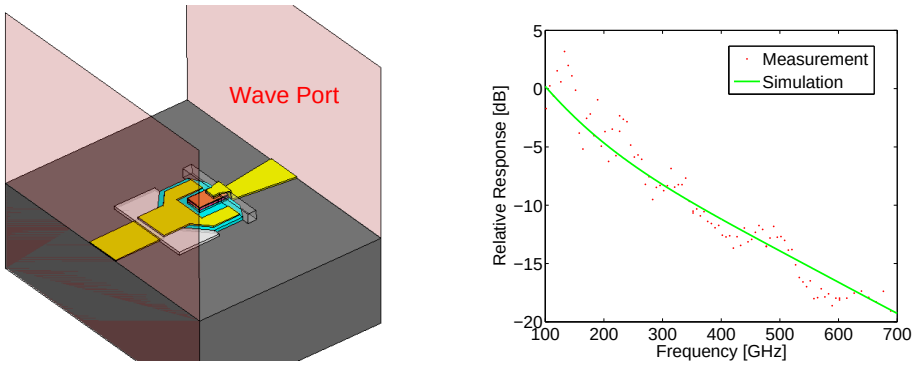


(a) (b)

Figure 4.8: Micro-photographs of a THz photomixer: (a) A PD with a logarithmic periodic antenna; (b) Detailed view of the PD.

PDs are not only used in optical telecommunication systems but also as photomixers for THz imaging applications. Fig.4.8 shows microphotographs of a photomixer. The chip consists of a photodiode and a logarithmic periodic antenna. When light illuminates the photodiode, the THz electrical power can be excited and then transmitted into free space through the antenna. Since the PD works in the THz range, the capacitive parasitics due to the EM coupling in the chip structure seriously limits the output power and the bandwidth. EM simulations on the chip may provide information on the parasitic effect and guide the optimization of the chip structure to minimize the capacitive parasitics and increase the output power. The following optimization approach is not only valid for the PD for THz photomixer applications but for general PDs. The PD for THz application is taken here as a good example to demonstrate the optimization method based on EM modelling.

Fig.4.9(a) shows the EM behavioral model of the PD chip with two wave ports to describe the O/E response of the PD chip. The process of developing the model is very close to the one presented in the last section. Two wave ports, which are placed at both edge of the chip substrate, act as the antenna loads on the chip. The characteristic impedance of the port is designed to be the impedance of the antenna. The relative output power delivered to



(a) (b)

Figure 4.9: (a) The EM model of a PD with two wave ports as antenna loads; (b) the comparison between the measured and simulated relative responses of the PD.

the antenna, P_{out}, can be expressed by S parameter as:

$$P_{out} = |S_{21}|^2 + |S_{31}|^2 \tag{4.7}$$

where the port1 excites the input electrical power converted from the incident light as the p-i-n junction does, and the port2 and port3 collect the output power at the antenna terminals connected to the anode and cathode of the PD, respectively. Fig.4.9(b) shows a good agreement between the simulated and measured relative responses of the PD. The accurate EM behavioral model is reliable for analyzing the EM properties of the PD. A big advantage of optimization by using EM models is that one does not need to extract parasitics on the chip. All the parasitics have been included in the EM model. Through optimizing the dimensions and materials of the device, the optimal design can be achieved.

A PD Device for On-wafer Measurement

A PD with G-S-G contact pads as shown in Fig.4.10(a) is developed to characterize the PD RF property by on-wafer measurements. The EM simulation for this purpose may exceed the frequency limitation of on-wafer measurements. This merit of EM simulations is very valuable for understanding the EM characteristics of the PD in THz range. The EM model of the PD with GSG probe is illustrated in Fig.4.10(c). It is quite similar to the model in the last section. The simulation results are reliable and accurate, because

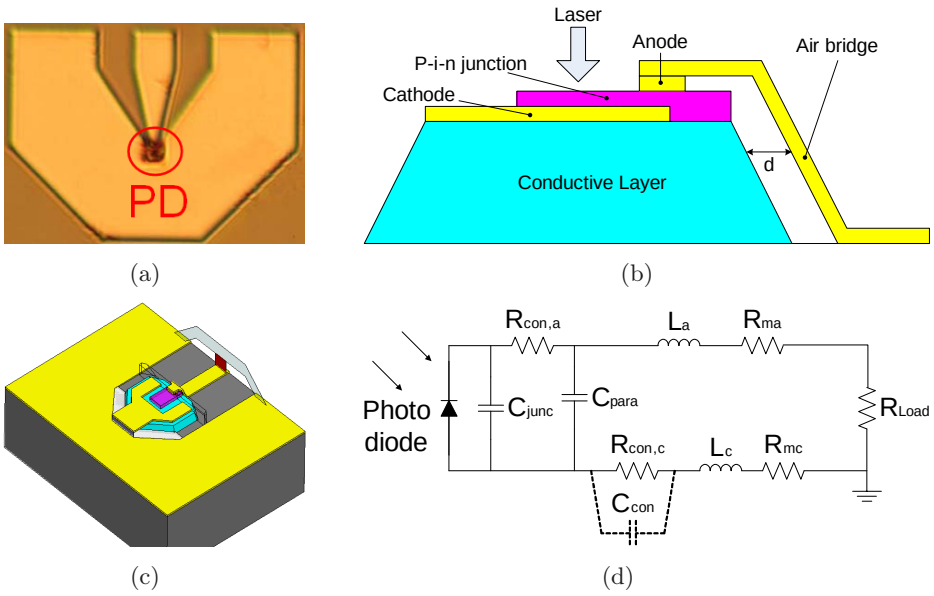
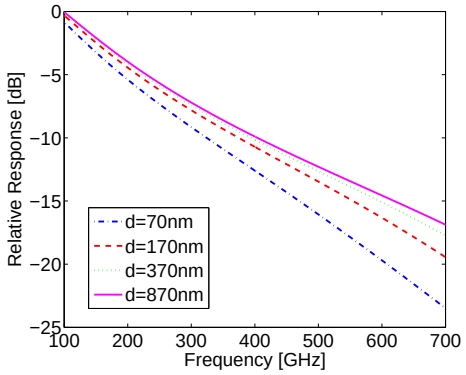


Figure 4.10: (a) A PD device for RF characterization; (b) cross section view of the PD; (c) EM model for the PD with GSG probe; (d) the equivalent circuit model of the PD.

the good agreement which is illustrated in Fig.4.9(b) proves the validation of the EM model of the PD.

The cross section of the PD structure is shown in Fig.4.10(b). The equivalent circuit model is demonstrated in Fig.4.10(d). The model is derived from the structure of the PD chip. The purpose of the circuit model is to better understand the electrical behavior of the PD. The value of the circuit component will not be extracted in the analysis and optimization procedure. The $R_{con,a}$ and $R_{con,c}$ are the contact resistors corresponding to the anode and cathode, respectively. The resistors originate from the non-perfect contact between the semiconductor material and the metal electrodes. C_{para} is the parasitic capacitance in the PD chip. It mainly comes from the capacitive coupling between the air-bridge structure and the conductive layer. L_a/R_{ma} and L_c/R_{mc} are the inductances and resistances from the anode-side and cathode-side metal contacts, respectively. The L_a should be much larger than L_c because of the air-bridge structure in the anode-side strip. The R_{ma} and R_{mc} is frequency dependent due to the skin-effect.

There are two RC bandwidth limitation networks in the equivalent circuit of the PD. One consists of C_{junc} and $R_{con,a}$. The other RC network consists



(a) (b)

Figure 4.11: (a) The simulated relative responses of the PD with varied distance between the conductive layer and the air-bridge, d, where $R_{con,a}/R_{con,c}$=100/10Ω; (b) the E-field pattern at 400 GHz d = 170 nm.

of C_{para}, $R_{con,c}$, R_{ma} and R_{mc}. In both RC networks, the capacitance plays an important role in limiting the output power of the PD. The C_{junc} is fixed when the dimension of the p-i-n junction is designed. However, the C_{para} can be minimized by reducing the coupling between the air-bridge and the conductive layer. Fig.4.11(a) plots the simulated relative responses while varying the distance between the air-bridge and the conductive layer, d which is indicated in Fig.4.10(b). In the process of developing the PD, silicon dioxide (SiO_2) is deposited on the top of conductive layer and below the air-bridge. The d depends on the thickness of SiO_2 attaching the side of the conductive layer.

Another important factor of limiting the O/E response of PDs is the contact resistors, $R_{con,a}$ and $R_{con,c}$. They are determined by the contact resistance (R_c) and the contact area (S_c) by

$$R_{con} = \frac{R_c}{S_c} \tag{4.8}$$

The contact resistances for the anode and the cathode are selected as $3.75 \times 10^{-6}\Omega \cdot cm^2$ and $10 \times 10^{-6}\Omega \cdot cm^2$, respectively. The anode contact area is 3.75 μm^2, and the cathode contact area is approximately 100 μm^2. The nominal contact resistors in Fig.4.11(a), $R_{con,a}$ and $R_{con,c}$, are 100 Ω and 10 Ω, respectively. They are modelled by lumped elements in the EM model. The simulated O/E response is normalized to the case when d = 870 nm. The

simulation results demonstrate that smaller d results in higher loss and faster attenuation, especially approaching THz range. Fig.4.11(b) shows the strong capacitive coupling between the air-bridge and the conductive layer. The electrical power may be confined within the chip due to the low impedance by the C_{para}. The undesired coupling can be weakened through presented increase in d. When d is increased from 370 nm to 870 nm, the improvement of the relative response is not significant. Therefore, the relative response can not be improved further when the d is larger than a criteria, for example d=1 μm in this case.

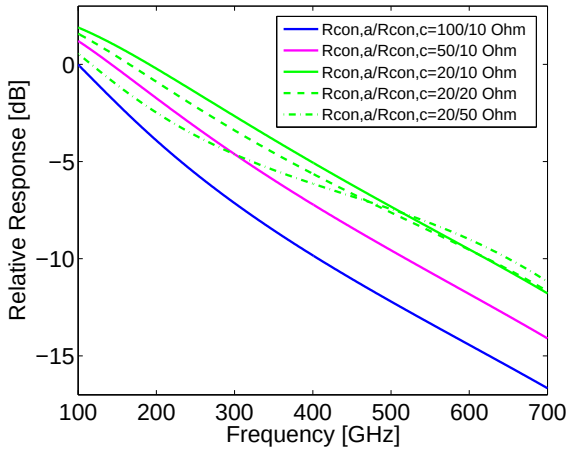


Figure 4.12: The simulated relative responses of the PD with varied contact resistance combination, where d = 870 nm.

The relative responses of PDs with several contact resistors combination are plotted in Fig.4.12. The d is assigned to 870 nm to minimize the parasitic capacitive coupling effect. The simulated O/E responses are normalized to the case when $R_{con,a}/R_{con,c}$ = 100/10 Ω. When the $R_{con,a}$ is reduced from 100 Ω to 20 Ω, the relative response is increased significantly. However, when the $R_{con,c}$ is increased from 10 Ω to 50 Ω, the degradation of the relative responses is not so significant as the $R_{con,a}$ increases. Furthermore, the relative responses overlap with each other over 450 GHz when $R_{con,a}$ is 20 Ω. At 700 GHz, the relative response with $R_{con,c}$=50 Ω is even the highest relative response. These results are contributed by the capacitive coupling between the conductive layer and the ground plane. As shown in Fig.4.13, a very significant E-field exists between the conductive layer and the ground

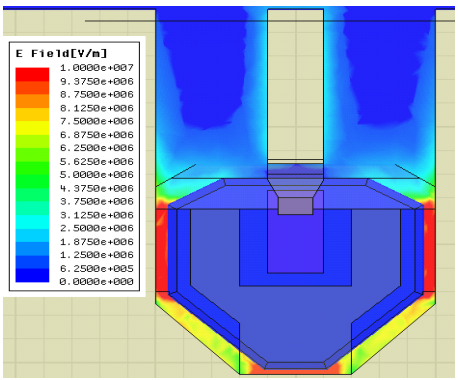


Figure 4.13: The E-field pattern at 400 GHz, where $R_{con,a}/R_{con,c}$=10/50 Ω.

plane. As plotted in 4.10(d), there is a capacitor, C_{con}, to model this effect. The impedance of the C_{con} decreases with the frequency increasing. The $R_{con,c}$ can be shorted by the C_{con} in THz range. As a result, the $R_{con,c}$ affects the relative response less than the $R_{con,a}$. On the other hand, the relative response can be improved by reducing the contact resistance or minimizing its effects by adding some intended capacitive coupling.

4.4 Summary

In this chapter, the methodology of developing EM behavioral models of PDs is provided. Using the method, two types of PDs are successfully analyzed and modelled. The models can accurately predict the O/E responses of the PDs. Two major bandwidth limitation effects, transit-time effect and RC effect, are both included in the model. The RC effect is built in the 3D passive structures and lumped elements, where the junction capacitance, C_{junc}, can be modelled by lumped elements or 3D junction structures. The characteristic of transit-time effect is model by an equivalent second order low-pass filter which consists of a series inductance (L_t) and a parallel capacitance (C_t). The model is valid for the PD with different dimensions of p-i-n junctions by tuning the lumped elements, which are C_{junc} (lumped model), C_t and L_t, accounting for those effects.

Based on the EM model, the PD for THz photomixer applications is investigated. The parasitic effects within the PD is revealed in simulation results. Minimizing the capacitive coupling effect between the air-bridge and the conductive layer and alleviating the effect of contact resistance is

suggested as the optimization scheme for improving the output power. Comparing the worst case (d = 70nm and $R_{con,a}/R_{con,c} = 100/10\ \Omega$) and the best case (d = 870nm and $R_{con,a}/R_{con,c} = 20/10\ \Omega$) which are discussed in the last section, the relative response can be improved by around 11 dB at 700 GHz from the worst to the best case.

The optimization on the PD based on EM modelling is not only valid for the PD for THz photomixer but also for general PD devices. The optimization approach can be further generalized for other active devices such as transistors and Schottky diodes. In the EM model of active devices, the dimensions and material parameters are required as input. The excitation for the EM model has to be place at the active region of the device. The frequency response of the device can be obtained in the simulation results as output. Compared to the optimization approach based on circuit models, the EM modelling approach has two major advantages. One advantage is that EM models do not need to extract parasitic values of devices. The parasitics have been intrinsically included in the EM model. The optimization is applied directly on the dimensions and materials of the device. The other advantage is that EM characteristic of the device is available for optimizations such as the EM field plots of the devices. It is very important for analyzing the EM behavior of the devices operating in the high frequency range which is approaching THz domain nowadays.

With the increasing computation capability of computers, the EM simulation time has been significantly reduced from hours to minutes level. This fact enhances the efficiency of the optimization based on EM modelling. Therefore, EM modelling is a very powerful, efficient and indispensable tool for optimizing not only passive but active devices.

Chapter 5

Packaging of Photodetector Modules for 100 Gbit/s Applications

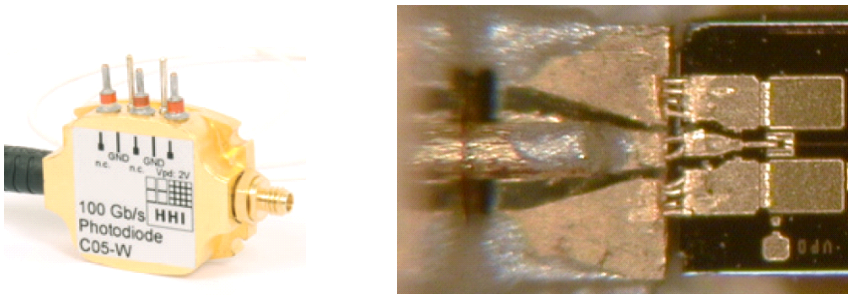
High-speed multi-gigabit networks are essential for future large volume data transmission like high quality videos. 100 Gbit/s single channel Ethernet systems are considered to be the next generation of Ethernet applications after the 10 Gbit/s Ethernet standard [2]. The optoelectronic transceiver working at the rate of 100 Gbit/s is crucial for realizing 100 Gbit/s Ethernet systems. The packaging of these high-speed components is very challenging when aiming at the rate of 100 Gbit/s, especially due to the multi-chip module (MCM) structures involving several chip-to-chip and/or chip-to-substrate transitions. In this chapter, we concentrate on the packaging aspects of the high-speed receiver front-end comprised of a high-speed photodetector (PD) with monolithically integrated fibre-connection and a MCM electrical connection.

There exist several methods to realize high-speed interconnects inside an MCM package. The most frequent solutions are wire-bonding and flip-chip interconnects. Generally, wire-bonding is regarded to be technologically easier to process, however, is not considered to be efficient at millimeter-wave frequencies. The parasitic effects such as the inductance due to the wire may degrade the performance of the system. On the other hand, flip-chip interconnect technology has been proven to exhibit low insertion losses, but at the expense of more complex technology. We will show that wire bonding can be efficiently used up to 110 GHz with very low losses, comparable or even lower than the flip-chip insertion losses. The design and optimization

on the packaging structure discussed in this chapter are based on previously presented accurate EM simulation techniques as well as EM modelling on the PD chips.

5.1 Packaging Structures of PD Modules

Fig.5.1(a) shows a picture of a packaged PD module. The PD chip is packaged in a metal box with input optical fiber on the left side, output electrical coaxial connector on the right side and the bias pins on the top of the module. The kernel device, a PD chip, is shielded by the packaging structure. A microphotograph of the packaging structure inside the module is shown in Fig.5.1(b). From the left to right, there are three components in the packaging structure. They are 1mm coaxial connector [79], a conductor-backed coplanar waveguide (CBCPW) and a PD chip. In Fig.5.1(b), only the launch body and launch pin of the connector are shown. There is an obvious gap between the connector and the CBCPW. As the interface between the chip and the output connector, the CBCPW bridges the chip to the coaxial connector. The pin of the 1 mm coaxial connector is directly soldered onto the signal strip of the CBCPW, and bonding wires are utilized to connect the PD chip to the CBCPW.



(a) (b)

Figure 5.1: (a) A packaged PD module; (b) a microphotograph of the inside view of the PD module packaging.

The packaging structure contains the CBCPW, the wire-bonding transition between the chip and the CBCPW and the transition between the coaxial connector and the CBCPW. It is currently limiting the performance of packaged PD modules. Careful design and optimization of the comprehensive packaging structure are crucial for minimizing the loss, resonance and multimode propagations caused by the package. It is very important to

achieve minimum impact of the package on overall frequency characteristics. Furthermore, the packaging structure used in the PD module is quite general, so the results and conclusions for packaging PD module are not only valid for this case, but are universally valid for other packaging cases for high-speed and high frequency applications.

5.2 Optimizations on the Coaxial-to-CBCPW Transition

As one of two major transition structures in the entire packaging scheme, the coaxial-to-CBCPW transition plays an important role in determining the performance of the packaging scheme. The design of the transition includes selecting suitable commercial coaxial connector, optimizing the interface between the connector and the CBCPW and avoiding the multimode propagation and higher mode resonances in the CBCPW.

5.2.1 The 1mm Coaxial Connector

In order to realize over 100 GHz application requirements, the output coaxial connector should possess very low loss from DC to over 100 GHz frequency range. The 11923A 1.0-mm female connector [79] launch assembly by Agilent is designed for ultra-high frequency (up to 110 GHz) coaxial signal transmission into a planar circuitry package. The reported insertion loss of the connector is no higher than 1dB from DC to 110 GHz.

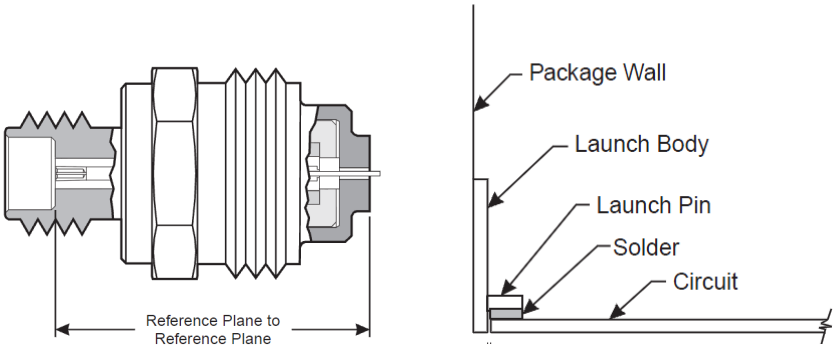


Figure 5.2: (a) Overview of the 1mm coaxial connector; (b) the detailed circuit mounting scheme.

Fig.5.2(a) shows the overview of the connector. The right most part is the launch part of the connector. It is the interface to the planar circuitry package. Fig.5.2(b) shows the detailed circuit mounting scheme. The extended pin is directly soldered on top of the planar circuit. There is a gap between the circuit and the launch body. Since we are only interested in the coaxial-to-CBCPW transition, the entire connector device is not taken into account in the investigation. Only the launch body and the launch pin are modelled in EM simulations. The inside diameter of launch body feedthru is typically $380 \pm 10\ \mu m$, the diameter of launch pin is $162 \pm 5\ \mu m$, and the length of extended launch pin is $320 \pm 50\ \mu m$. The characteristic impedance of the launch body of the connector, which is a typical coaxial line, can be calculated by [80]

$$Z_0 = \frac{1}{2\pi} \ln \frac{b}{a} \sqrt{\frac{\mu}{\varepsilon}} \tag{5.1}$$

where a is the diameter of the launch pin and b is the inside diameter of the launch body, μ and ε are the permeability and permittivity of air, which is the filling dielectric material in the connector, respectively. Z_0 calculated with nominal parameters, where $a = 162\ \mu m$ and $b = 380\ \mu m$, is 51.2 Ω, which matches the 50 Ω impedance system of the PD module.

The higher mode propagation in the transmission line is always harmful for high frequency applications. TE_{11} mode is the first order higher mode in the coaxial line. The cutoff frequency of the TE_{11} mode can be derived to be [80]

$$f_c = \frac{ck_c}{2\pi\sqrt{\varepsilon_r}} \tag{5.2}$$

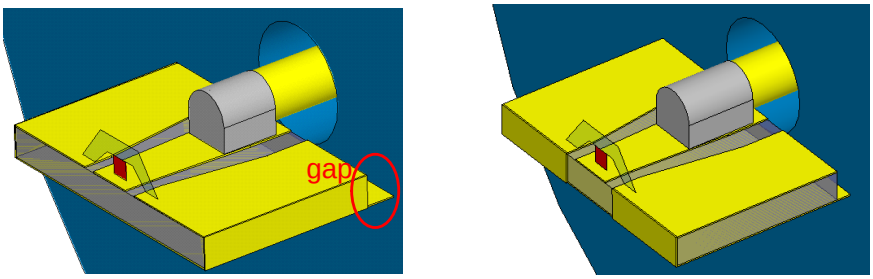
where c is the light velocity in vacuum, and k_c is often approximately estimated in practice by

$$k_c = \frac{2}{a+b} \tag{5.3}$$

The derived cutoff frequency is 352 GHz, which is much higher than the the frequency range of interest in this case. This is only the investigation for the launch body of the connector, not for the entire connector device. Therefore, the results derived here do not mean the connector can be used for up to 300 GHz applications.

5.2.2 CBCPW with Side Metallization

In the packaging scheme as shown in Fig.5.1(b), side metallization is applied on the CBCPW. The application of the side metallization is considered to short-circuit the top ground planes of CBCPW and its backside ground planes to prevent the parasitic parallel plate mode in the CBCPW. The material of the CBCPW substrate is quartz whose relative permittivity is 3.8. The substrate with low permittivity is selected to push the unwanted substrate mode out of the frequency range of interest. The substrate is 100 μm thick.



(a) (b)

Figure 5.3: The EM simulation setup for the coaxial-to-CBCPW transition where side metallization is applied (a) along the longitudinal direction of the CBCPW and (b) at the end of the CBCPW.

3D EM simulation setup for the coaxial-to-CBCPW connector transition is shown in Fig.5.3. A G-S-G probe model with a lumped port is used to excite the CBCPW side of the transition, and a wave port is used to terminate the connector side of the transition, which is not shown in the figure. The connector-side of CBCPW has wider CPW dimensions, $(S+2W)$, than the chip-side of CBCPW, which is supposed to connected to the PD chip. Both of them have been designed to be 50 Ω characteristic impedance. The dimensions of the CPW intend to match the dimensions of adjacent devices. Abrupt discontinuity between the devices should be avoided in the packaging structure. For the same reason, a tapered structure is utilized in the CBCPW to smooth the transition between two CPW dimensions. The length of the tapered CBCPW is designed to be 600 μm, which approaches the limitation of packaging fabrication. Shorter CBCPW structure is considered to bring less loss to the packaging. The side metallization along the longitudinal direction of the CBCPW is exploited to connect top ground planes with the backside ground plane as shown in Fig.5.3(a). As alternative, the side

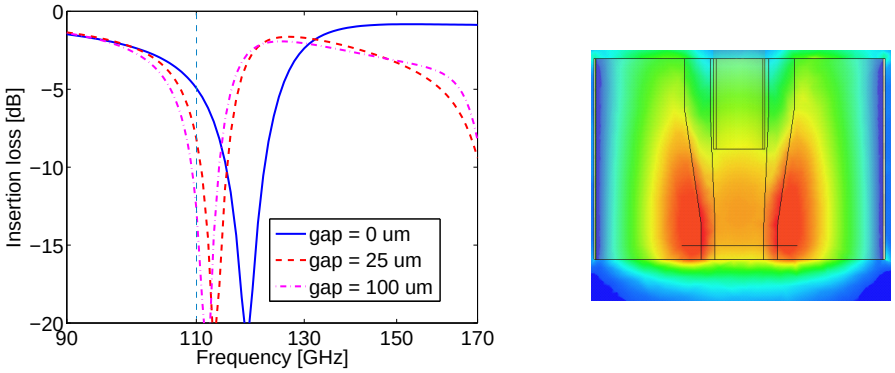


Figure 5.4: EM simulation results of the coax-to-CBCPW transition: magnitude of S_{21} with varied gap and the E-field at 110 GHz while gap = 25 μm.

metallization could also be applied at the end of the CBCPW as shown in Fig.5.3(b). It is proven by EM simulations that the low frequency transmission characteristic of the transition is very poor when top ground planes are not connected to the universal ground plane, because the top ground planes would be floating so that there is no current return path in the low frequency range. The gap between the CBCPW and connector shown in Fig.5.3 could influence the potential resonance in the transition.

The simulation results of the coaxial-to-CBCPW transition are shown in Fig.5.4. If only checking the insertion loss below 110 GHz, all the magnitudes of S_{21} with different gaps decrease very fast over 90GHz. The E-field in the substrate at 110GHz with the gap being 25 μm is also shown in Fig.5.4. A strong resonance field in the substrate is excited at the end of the CBCPW with side metallization. The field exhibits quasi-parallel plate mode with a quarter wavelength perpendicular to the longitudinal direction of the CBCPW. This resonance degrades the high frequency transmission performance through the transition in the frequency range of interest. When the EM simulations are extended to 170 GHz, notches appear in all cases between 110 GHz and 120 GHz. Apart from the resonances due to the parasitic parallel plate, the transition with no gap between the CBCPW and the connector shows the lowest insertion losses among all cases. Therefore, there should be no gap in the transition to achieve potential excellent transmission performance.

In the first optimization scheme, called "case 1", only one longitudinal end of the CBCPW is coated with side metallization. This optimization

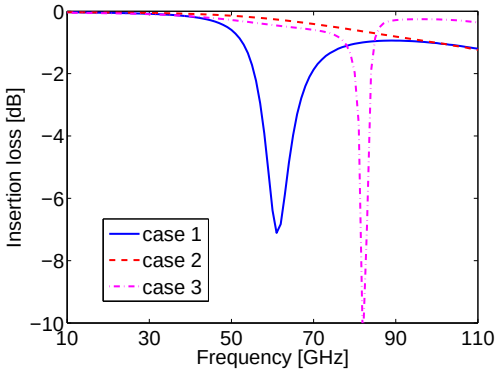


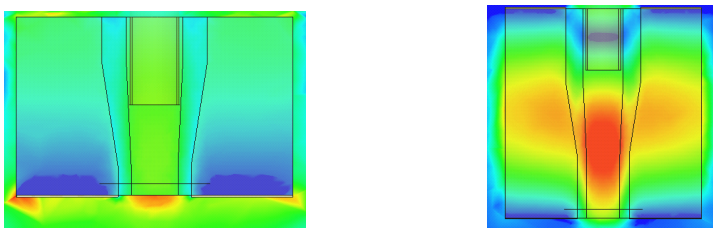
Figure 5.5: The insertion loss of the coaxial-to-CBCPW transition with different side metallization schemes: "case 1": only one side metallization is applied at the end of the 600 μm long CBCPW line; "case 2": both ends of the 600 μm long CPW line are coated by metallization; "case 3": both ends of the 1 mm long CBCPW line are coated by metallization.

increases the high frequency transmission property. The insertion loss of the structure is around -1.5 dB at 110 GHz, which is much lower than the case with longitudinal side metallization. However, a new resonance is introduced at 61 GHz as shown in Fig.5.5. The E-field in the substrate at the resonance frequency, which is shown in Fig.5.6(a), demonstrates a parallel plate mode with quarter wavelength, because one end of the parasitic parallel plate is shorted and the other end is open. The field pattern is similar to the one in the Fig.5.4 except for the orientation. When both ends of the CBCPW are covered by side metallization, which is called "case 2", the curve of the insertion loss is free of notches. Actually, the end side metallization at the chip side is equivalent to the "case 1" with $gap = 0\mu m$. The ground plane can be connected by the outer of the connector. However, if the CBCPW is extended to 1mm, which is called "case 3", a new resonance is observed. The corresponding E-field at the resonance frequency, which is shown in Fig.5.6(b), also exhibits parallel plate mode. It is half wavelength long with two zeros because both ends of the parallel plate are shorted. Both above resonance frequencies can be estimated by using

$$f_n = \frac{c}{2\sqrt{\varepsilon_r}} \cdot \frac{n}{d} \tag{5.4}$$

where n is the index of the mode order and d is the length along the orien-

tation of the resonance. The order numbers of resonance are 0.5 and 1 for quarter and half wavelength, respectively.



(a) (b)

Figure 5.6: E-field in the substrate at resonance frequency for (a) case1; (b) case3.

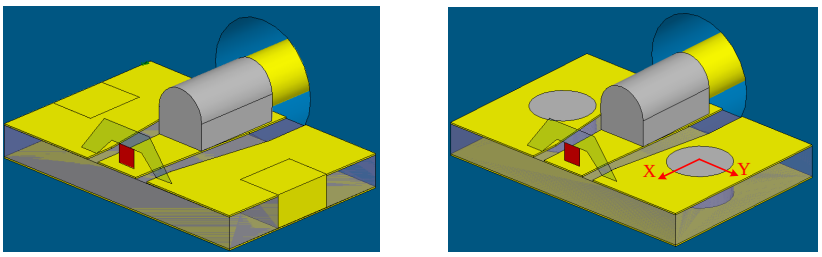
After investigating the transitions with different side metallization schemes, we conclude that the longitudinal side metallization is not suitable for high performance transmission in very high frequency range. Even though the resonance can be moved far away from the frequency range of interest by reducing the width of ground planes of the CBCPW, this operation is difficult to realize due to the limitation of fabrication technologies. The side metallization at both ends of the CBCPW effectively achieves good transmission property for the broadband requirement. However, this solution is only valid for the short CBCPW.

5.2.3 CBCPW with Metal Posts and Vias

Besides the side metallization on the CBCPW, another effective way to suppress the parallel plate mode is breaking the substrate mode resonance by inserting metal bricks in the substrate such as metal posts or vias.

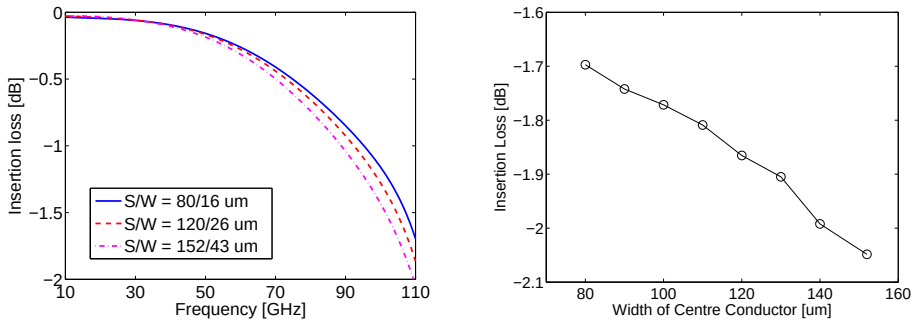
The metal post solution is illustrated in Fig.5.7(a). The posts connect top and backside ground planes to obtain excellent transmission property in the entire frequency range. The size and the location of the post should be optimized. It has to be sufficiently large to suppress the substrate mode resonance. However, being too large, they will influence the characteristic impedance of the CBCPW line, which is critical for keeping the correct propagation modes in the CBCPW. Posts should be placed in the middle of line's edge to keep the potential resonance far away from the concerned frequency range. In Fig.5.7(a), the metal posts are 200 μm long and 150 μm wide.

Fig.5.8(a) shows flat transmission properties are achieved by exploiting



(a) (b)

Figure 5.7: The EM simulation setup for the coaxial-to-CBCPW transition with (a) two metal posts and (b) two metal vias in the substrate.



(a) (b)

Figure 5.8: (a) transmission characteristic of the transition with different CPW dimensions; (b) insertion loss of the transition at 110 GHz versus center conductor widths of CPW structures while characteristic impedance is constantly 50 Ω

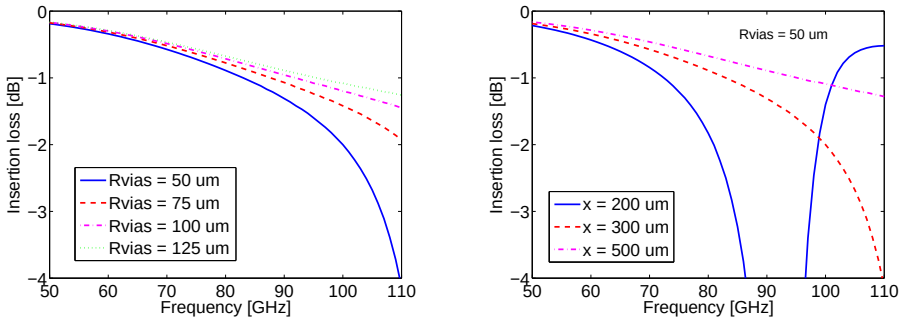
metal posts in the substrate. The transition is further optimized in the aspect of different CBCPW structures at the chip side. The characteristic impedance of the CBCPW keeps 50 Ω while varying the CPW dimensions. Table 5.1 summarizes the dimensions of the CBCPW under investigation.

The simulation results demonstrate that smaller CPW structure results in better transmission performance. Fig.5.8(b) shows the insertion losses at 110 GHz versus the width of the signal strip. When the CPW structure is smaller, the insertion loss gets lower. More EM power is confined in the CPW structure instead of the coupling between the signal strip and the backside ground plane. This is helpful to prevent the leakage from the propagation to the substrate modes. The limitation for this optimization is the fabrication

S (μm)	80	90	100	110	120	130	140	152
W (μm)	16	18	20	23	26	30	36	43

Table 5.1: Dimensions of the CBCPW with 50 Ω characteristic impedance. The substrate is quartz ($\varepsilon_r = 3.8$) with 100 μm thickness.

technology. Advanced commercial ceramic vendor is normally limited to 15 μm gaps between metal strips.



(a) (b)

Figure 5.9: The insertion loss of the coaxial-to-CBCPW transition with vias: (a) varying radius of the vias; (b) varying position of the vias.

As shown in Fig.5.7(b), applying vias in the substrate is an alternative scheme to the metal posts. Currently, we only discuss the case of one via at each side of ground planes. For the cylinder vias, the radius and the position of the vias may influence the transmission characteristic of the transition. Fig.5.9(a) shows the insertion losses of the transition with different vias. The via at each of the side ground plane regions is placed in the middle of the CBCPW along the Y direction as indicated in Fig.5.7(b). The center of the vias is 175 μm away from the edge of the CBCPW. The radius of the vias varies from 50 μm to 125 μm. It is observed that larger vias lead to better transmission performance. With the dimension of vias increasing, the potential quarter or half wavelength resonance is more and more inhibited by the vias. In other words, the length of resonance becomes shorter, so that the resonance frequency is moved out of the operation frequency range. However, the vias should not be so large as to destroy the transmission line structure for the dominant mode propagation.

In the real products development, vias with huge dimensions are not easy to be fabricated in the substrate. The substrate could be destroyed during

developing large vias. The position of vias can also be optimized. Fig.5.9(b) shows the insertion losses of the transition with vias which are placed at different positions. The vias move along the X-direction as indicated in Fig.5.7(b). The variable x in the inset of Fig.5.9(b) means the distance from the center of the vias to the connector side end of the CBCPW. The radius of the vias is kept 50 μm. It is observed that the insertion loss of the transition is very sensitive to the vias position. Better transmission performance is achieved when the vias are placed close to the end of the CBCPW at chip side. Although the diameter of the vias is fairly small compared to the best case in Fig.5.9(a) for R_{vias} = 150 μm, a comparable transmission characteristic is still achieved as shown in Fig.5.9(a) by properly placing the vias.

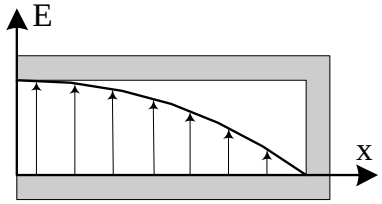


Figure 5.10: E-field distribution in a quarter wave length parallel plate resonator.

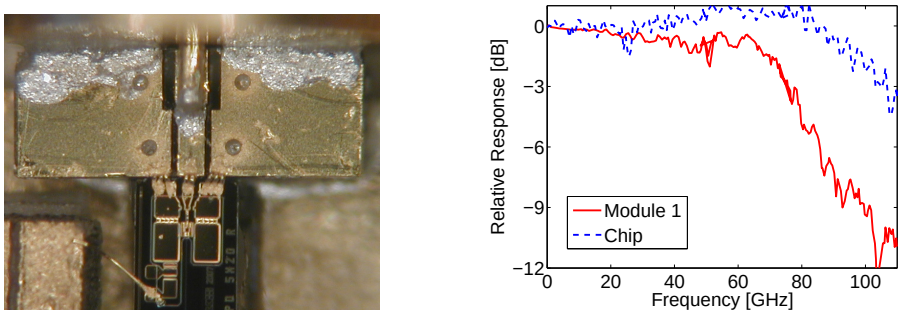
When there are no vias or side metallization in the CBCPW and the gap between the CBCPW and the connector is zero (filled by conductive glue), a potential quarter wavelength resonator is composed of ground planes and a substrate sandwiched between them. It is an equivalent parallel plate with one end open and the other one shorted. The first order resonant frequency can be calculated as 64.2 GHz by using Eq.5.4 with n = 0.5 and l = 600 μm. The strongest EM field part appears at the open end as shown in Fig.5.10. When the vias are placed close to the open end, the resonance pattern is effectively suppressed by short-circuiting two strongly electrically coupled ground planes. As demonstrated in Fig.5.9(b), the best transmission characteristic is achieved when the vias are 500 μm away from the connector side of the CBCPW.

5.2.4 Summary

According to the discussion on the coaxial-to-CBCPW transition, a brief summary for optimizing the transition can be drawn here. The objective of

the optimization is to achieve broadband low loss transmission characteristic from DC to 110 GHz. The multimode propagations and resonances should be avoided in the transition. The major problem in the transition is the resonance in the CBCPW structure due to the parasitic parallel plate mode. The gap between the connector and the chip is suggested to be zero by filling conductive glue. Side metallization, posts and vias are recommended to suppress the resonances. Side metallization can only move the resonance out of the operation frequency range by changing the orientation and the order of the resonances. Posts and vias suppress the resonances by destroying substrate of the resonator. When applying these solutions, they should effectively suppress the original resonances and will not introduce other resonances. Vias are considered as an effective and flexible method to suppress the resonances in the CBCPW.

5.3 EM Modelling on the Packaged PD Module



(a) (b)

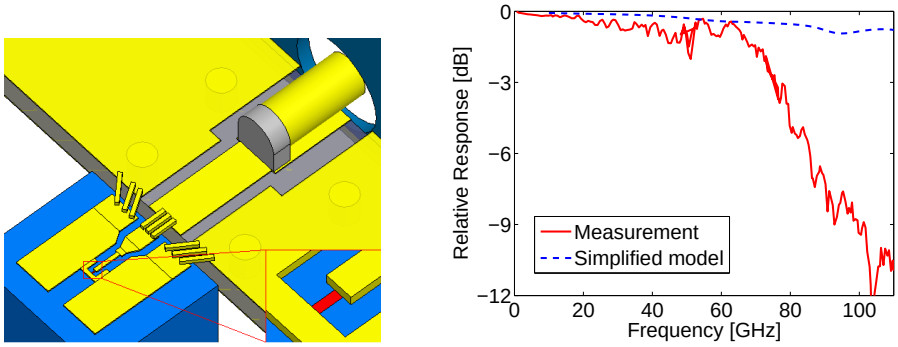
Figure 5.11: (a) A microphotograph for the inside view of a packaged PD module using a CBCPW with vias; (b) the measured relative response of the packaged "module 1" and the chip.

A PD module was fabricated as shown in the Fig.5.11(a). It is named after "Module 1". A wide CBCPW with vias is used in the packaging structure. Vias intend to eliminate the resonances caused by the CBCPW structure. Fig.5.11(b) shows the measured relative electro-optical (O/E) responses of the packaged PD module and the PD chip. The 3-dB bandwidth of the packaged PD module is only about 75 GHz, and the loss of the module is more than 9 dB beyond 100 GHz. The PD chip originally has more than

100 GHz 3-dB bandwidth. Narrower bandwidth and higher loss due to the packaging structure seriously degrade the performance of the PD module. Further optimization on the packaging structure using EM simulations is mandatory for improving the performance of the packaged PD module.

5.3.1 A Simplified Model

Fig.5.12(a) shows a HFSS simulation model for the PD module packaging including a PD chip, bonding wires, a CBCPW with vias and a launch body of a coaxial connector. It models the real packaging structure as shown in Fig.5.11(a). The photodiode in the PD chip is modelled by a lumped port as illustrated in the inset of Fig.5.12(a). The bonding wire interconnect is modelled using rectangular gold structures with appropriate dimensions. Vias arrangement in the CBCPW can be recognized in Fig.5.12(a). The gap between the connector and the CBCPW is filled by the conductive glue. The 1mm coaxial connector is modelled by an ideal coaxial cable line. Therefore, the loss due to the connector itself is ignored in the packaging model.



(a) (b)

Figure 5.12: (a) HFSS simulation model of the PD module packaging. The inset shows how a lumped port sits between anode and cathode acting as a photodiode. (b) The comparison between measured and simulated relative responses of the "module 1".

The EM model is called a simplified model, because all the components are completely floating without considering the housing of the PD chip, the bonding wires are roughly modeled by cuboid objects and the photodiode is simply modeled by a lumped port with 50 Ω impedance. Since the model is quite simple compared to the real case, several bandwidth limitation effects

in the PD module are not included in the EM model. For example, the PD chip with a simple lumped port has very broadband performance and the surrounding of the major transitions in the packaging structure is omitted in the model. The surrounding structure may influence the performance of the module.

Fig.5.12(b) plots the comparison between measured and simulated relative responses of the "module 1". Large discrepancy over 60 GHz is caused by the simplification in the EM model of the module. The insertion loss of the simple model can not precisely simulate the relative response of the module. More complex and accurate EM models are required to represent the real module. However, the simple model is still sufficient enough for investigating the impact of CBCPW with vias and bonding wires on the frequency response of the packaging at the early phase of the investigations.

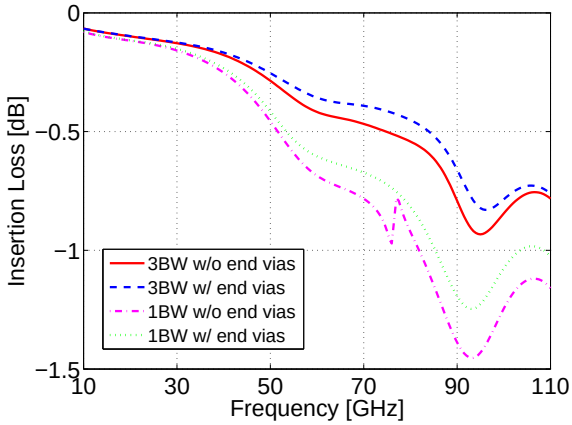
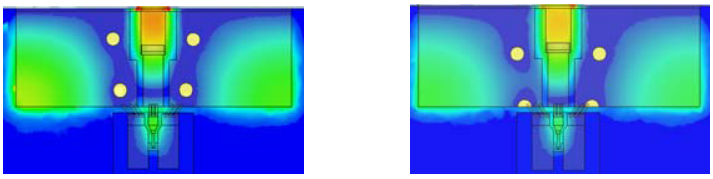


Figure 5.13: The simulated insertion losses of the different packaging schemes.

Several cases of packaging schemes have been analyzed using EM simulations and the results are presented in Fig.5.13. As discussed in the Chapter 3, vias can not completely eliminate the resonances in the CBCPW transmission characteristics due to the energy leakage at the end of the CBCPW. The simulated insertion loss for the packaging structure as illustrated in Fig.5.12(a) is shown in Fig.5.13 as the solid line. Although no obvious resonances exist in the insertion loss characteristic a strong E-field at the edge of CBCPW is visible at 77 GHz, as shown in Fig.5.14(a) . The pattern can be recognized as the patch antenna mode with both order numbers being 0.5.

In spite of the leakage the insertion loss is less than 1dB up to 110 GHz.



(a) (b)

Figure 5.14: (a) E-field of the original packaging structure at 77 GHz; (b) E-field of the packaging structure with the optimized vias arrangement at 77 GHz.

In order to prevent the energy leakage from the CBCPW mode to the substrate resonances, a pair of vias are moved to the edge of CBCPW while keeping the distance between vias at the minimum value limited by fabrication technology, which is 380 μm provided by the vendor. The insertion loss of the packaging structure with such optimization is shown in Fig.5.13 as the dashed line. The insertion loss of the package is improved by around 0.1 dB from 40 GHz to 110 GHz. However, the resonance is not eliminated completely by the optimization as shown in Fig.5.14(b). The EM energy still leaks between vias as well as the gap between the PD chip and the CBCPW. Further EM simulations demonstrate that EM energy leakage between vias can be completely eliminated by placing more vias in the substrate.

In the above simulations we have employed three bonding wires on each output pad of the PD chip for the chip-to-CBCPW transition. The number of bonding wires is also critical to the insertion loss of the packaging structure. Instead of three bonding wires on each pad, an interconnect with one bonding wire has also been studied as the dot curve in Fig.5.13. Compared to the cases with three bonding wires, the insertion loss in this case is at least 0.5 dB higher independent of the optimization of the vias in the substrate, as indicated by the dot-dash curve in Fig.5.13.

The packaging structure with flip-chip transition from the PD chip to the CBCPW is also investigated. An EM simulation model with flip-chip structure is built in HFSS, which is not shown here. The simulated insertion loss is illustrated in Fig.5.15. Flip-chip technology is normally considered to have superior performance as MCM interconnection than its counterpart such as wire-bonding in high speed applications. In this case, however, the insertion loss of the package with flip-chip transition is comparable to the ones with bonding wires. The optimized package with bonding wires even

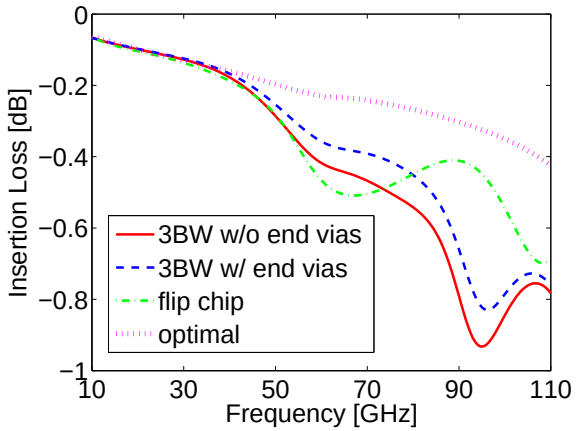


Figure 5.15: Simulated insertion loss of the packaging with flip-chip transition which compares to bonding wires. An insertion loss of an optimized packaging structure is plotted as a reference.

exhibits lower insertion loss below 80 GHz.

A significant improvement of the insertion loss of the simplified PD module model can be achieved by using an optimal packaging structure. As plotted in Fig.5.15, the optimized insertion loss is free of notches and slight attenuation in the range of 10 GHz to 110 GHz. The insertion loss at 110 GHz is slightly higher than -0.4 dB which is an excellent packaging performance.

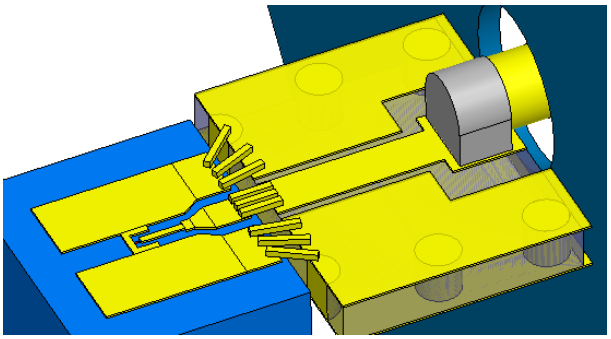
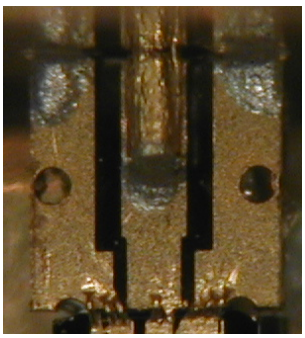


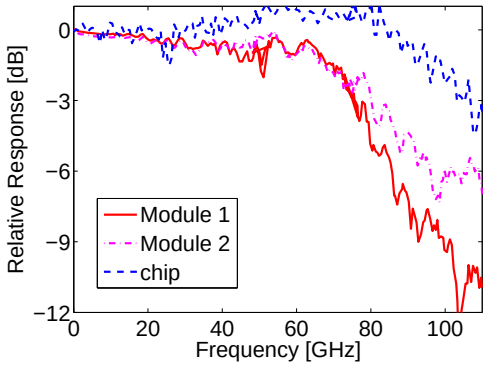
Figure 5.16: The simplified EM model of an optimized packaging structure.

Fig.5.16 shows the EM model of the optimized packaging structure. The model is still a simplified model. In the optimized packaging structure, several major modifications have been made to improve the transmission performance. The modifications are listed as follows:

- Three pair of vias are placed along the CBCPW to completely suppress the patch antenna mode resonances in the frequency range of interests.
- Width and length of ground planes are shortened to inhibit the influence of the CBCPW structure.
- The pin of the connector is cut to a reduced length. This modification minimizes the dimension of the transition of CBCPW-to-coaxial connector. The effect of impedance mismatch between the CBCPW and the CBCPW conductively glued with a cylinder (pin) is also alleviated.
- Bonding wires are evenly placed along the pads of the chip at the chip side. At the CBCPW side, the ends of bonding wires connecting ground planes are placed between the gap on the CBCPW and the vias. This arrangement tries to confine most of EM energy propagate along the CBCPW structure.



(a)



(b)

Figure 5.17: (a) The microphotograph of a packaged PD module; (b) Measured relative responses of packaged modules.

As shown in the Fig.5.17(a), a new module has been developed to verify the optimized solution based on EM simulations. In the new module, there are in total three pair of vias. Four vias are placed at the edge of the CBCPW

both at the connector side and the chip side. One pair of edge vias are visible at the chip side, and the other pair of edge vias are covered by conductive glue jointing the connector and the CBCPW. The width of the CBCPW is narrowed as suggested in the optimal packaging structure. The pin of the connector is hard to be manipulated due to the fragility of the connector. The short pin is also hard to be soldered on the signal strip of the CBCPW.

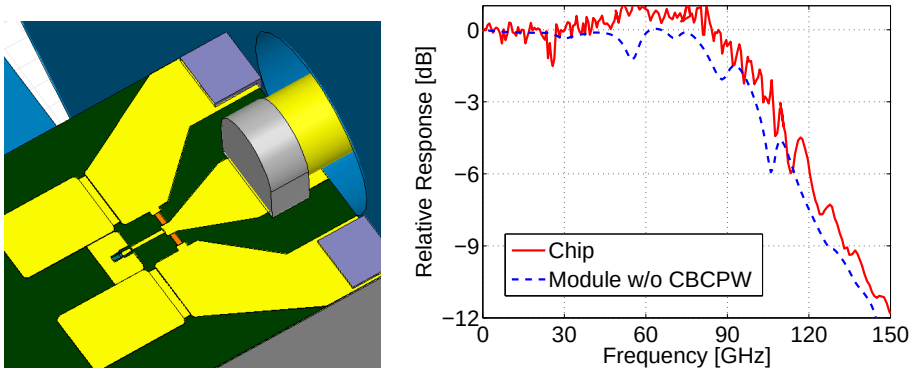
The measured relative response of the new module, which is "module 2", is plotted in Fig.5.17(b). Compared to the "module 1", the relative response is significantly improved in the frequency range over 75 GHz. The 3-dB bandwidth is improved by 5 GHz from 75 GHz and 80 GHz. The improved loss over 100 GHz is more than 5 dB. This improvement is very valuable for achieving low BER data transmission in 100 Gbit/s applications.

5.3.2 Packaging without CBCPW

In principle, the simpler is the packaging structure, the less degradation of the performance is caused by the packaging structure. Fig.5.18(a) shows an EM model of a packaged PD model without CBCPW structures. There is only a CPW-to-coaxial transition in this packaging scheme. The pin of the coaxial connector is directly conductively glued on the PD chip. The pin of the connector is short in the model to minimize its impact. The output CPW pad of the PD is designed to be 50 Ω characteristic impedance and fit the dimensions of the connector. The width of the signal pad is 140 μm and the gap of the CPW pad is 95 μm wide. Taper CPW structure on the chip is used to smooth the variation of the CPW dimensions.

The EM model of the module is not a simplified one. The behavioral model of the PD chip, which was presented in Chapter 4, is included in the model. From now on, the behavioral chip model is included in the following investigations. The model precisely describes the relative response of the PD chip. The housing of the chip, which is a metallic supporter, is also included in the model. The model of the module tries to resemble as close as to the prospective module to be fabricated.

The simulated relative response of the module and the measured relative response of the PD chip are plotted in Fig.5.18(b). The difference between them is the relative response attenuation due to the packaging structure. As expected for this scheme, the EM model predicts that the attenuation due to the packaging is slight because the difference is small. For instance, the relative response attenuation due to the packaging structure at 120 GHz is around 1.5 dB and keeps constant up to 150 GHz. According to the simulation results, we can conclude that this packaging scheme exhibits very



(a) (b)

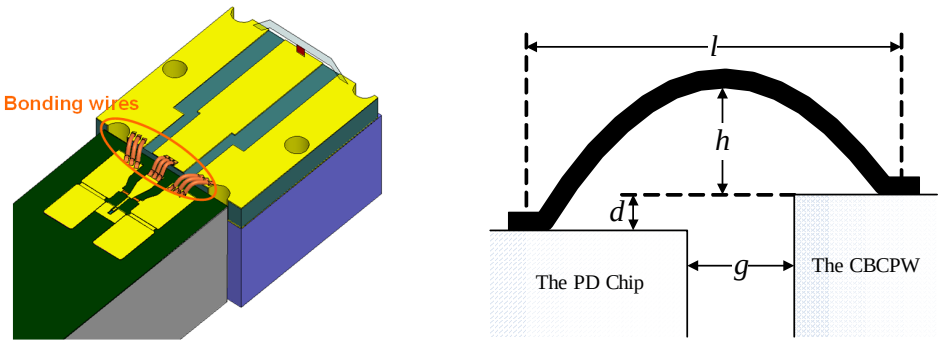
Figure 5.18: (a) EM model of the packaged PD module without CBCPW; (b) the comparison between the simulated relative response of the module and the measured relative response of the chip.

good low attenuation performance up to 150 GHz. It is an ideal candidate for packaging PD chips. This result also proves that excellent packaging structure should be a simple design.

However, the fabrication of this packaging scheme is not simple as it looks. One challenge is shortening the pin of the connector because the connector is very fragile. The other challenge is to directly apply conductive glue on the InP PD chip, which is also easily destroyed by strong mechanical force.

5.3.3 Optimization on Bonding-wires

Since the fabrication technology still need to be further developed to realize the packaging proposal in the last section, we need to come back to package chips by using the technology which is quite mature. CBCPW is still necessary in the packaging structure to connect the chip to the coaxial connector. The following optimization will focus on improving the performance of the "module 2". Although the performance of the packaged PD module is remarkably improved by optimizing the CBCPW with vias, there is still some room to improve the performance of the packaging structure by optimizing other components in the packaging structure. In this section, we are going to investigate the wire-bonding transition between the PD chip and the CBCPW.



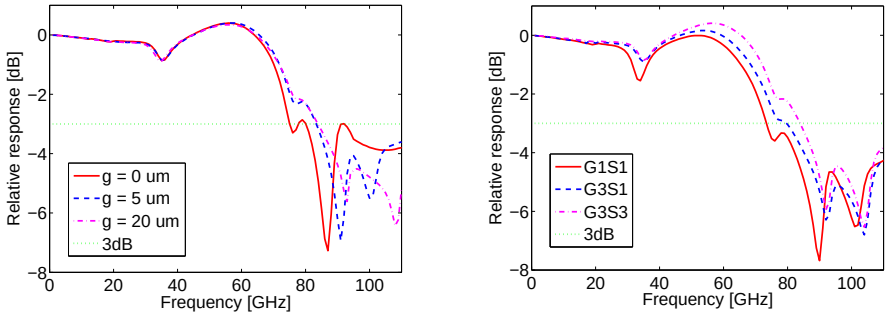
(a) (b)

Figure 5.19: (a) The EM model of the PD chip-to-CBCPW wire-bonding transition; (b) Schematic view of the bonding wires.

In the simple model of the packaged module, the bonding wires are simply modelled by cuboid objects. And, only the influence of number of bonding wires is briefly investigated. As the major interconnection structure in the packaging, the wire-bonding should be carefully investigated using EM simulation. Fig.5.19(a) shows the the EM behavioral model used to analyze the impact of the wire-bonding interconnect up to 110 GHz. Three bonding wires connect each pad of the chip to the signal (S) or ground (G) strips of the CBCPW, respectively. In the EM model, a metallic brick is included to support the CBCPW because the PD chip is based on 500 μm thick InP and the CBCPW is based on 100 μm quartz. A suitable metallic support is selected to make the chip and the CBCPW are at the same horizontal level for easy wire-bonding. The supporter is actually a part of the wire-bonding transition.

The transmission characteristic of wire-bonding interconnects is considered to be influenced by the arrangement of bonding wires, the number of bonding wires in the transition, and the geometry of the bonding wires. The geometry parameters of the bonding wires includes the length of the wires (l), the height of the wires (h), the horizontal level difference (d) and the gap (g) between the chip and the CBCPW. The parameter abbreviations are indicated in Fig.5.19(b). These parameters will be systematically analyzed using EM simulations. The diameter of bonding wires is 20 μm.

Selected simulated relative responses of the wire-bonding interconnects are shown in Fig.5.20 and Fig.5.21. The attenuation of all the curves becomes very serious beyond 60 GHz, which is similar to the measured characteristic of the module as shown in Fig.5.17(b). Therefore, the transitions from the



(a) (b)

Figure 5.20: Simulated relative responses of chip-to-CBCPW wire-bonding transitions: (a) $g = 0$ μm, 5 μm and 20 μm; (b) different numbers of bonding wires indicated by "GxSy": x and y means the numbers of bonding wires connecting the ground (G) and signal (S) strips, respectively, where $g = 20$ μm.

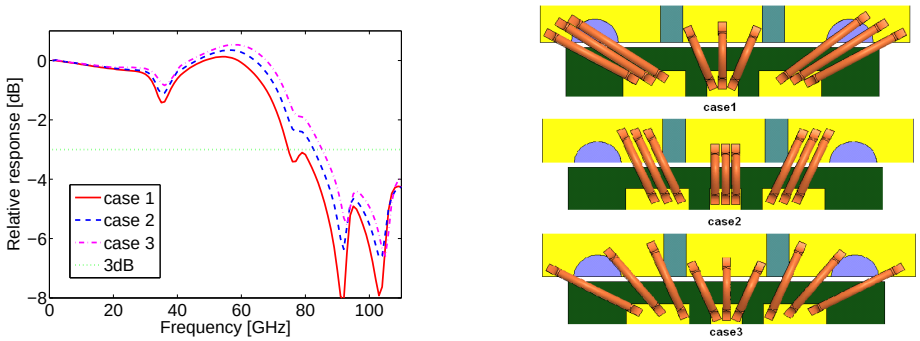
chip to the CBCPW are identified to be the major bandwidth limitation of the PD module. Fig.5.20(a) demonstrates that there should be an optimized gap between the chip and the CBCPW to avoid fast attenuation beyond 60 GHz and the deep notch around 90 GHz. Fig.5.20(b) shows that more bonding wires result in better relative response. Fig.5.21(a) and Fig.5.21(b) show that bonding wires connecting ground strips should be placed close to the gap of CBCPWs and all wires should spread well along the width of strips.

Important	Negligible, (within a certain range)
Gap (g)	Length (l), (S: 60 μm $\sim$ 100 μm; G: 90 μm $\sim$ 150 μm)
Number	Height (h), (10 μm $\sim$ 50 μm)
Arrangement	Horizontal level difference (d), (-20 μm $\sim$ 40 μm)*

Table 5.2: Summary for the parameters of wire-bonding transition.

* Negative value means chips are higher than CBCPWs.

The impact of various parameters in wire-bonding interconnects for transmission characteristic is summarized in the Table5.2. The length and height of bonding wires and the horizontal level difference do not too much influence the characteristic of the wire-bonding within the specified ranges. When numbers of bonding wires are placed separately across the strips of CBCPWs as well as an optimized gap is kept, more than 10 GHz bandwidth



(a) (b)

Figure 5.21: (a) Simulated relative responses of chip-to-CBCPW wire-bonding transitions with three typical arrangements of bonding wires as illustrated in (b), where $g = 20$ μm.

improvement can be achieved compared to the worst case. We also notice that optimization of bonding wires does not significantly improve the fast attenuation beyond 60 GHz. Further investigation and optimization of the transition from the PD chip to the CBCPW are required.

5.3.4 Generalized CPW-to-CBCPW Transition

Since output pads of MMICs and OEICs, such as the PD chip of interests, are normally CPW structures and CPW/CBCPW are widely used as on-chip interconnection due to their low dispersion and easy grounding merits, chip-to-chip and chip-to-substrate transitions can be generalized as CPW-to-CBCPW and CPW-to-CPW transitions. As shown in Fig.5.22, a typical CPW-to-CBCPW transition utilizing wire-bonding technology represents a generalized PD chip to CBCPW wire-bonding interconnection as shown in Fig.5.19(a). The support below the CBCPW is in general chosen to adjust the height of two chips. Several via holes are fabricated in the CBCPW to suppress unwanted multimode propagation and resonances. The EM model of bonding wires resembles the real case. The insertion loss of the CPW-to-CBCPW transitions with different supportive bricks is shown in Fig.5.23 (red curves). Resonances exist in low frequency range, and fast attenuation of the insertion losses starts at 60 GHz. In the EM model of the transition, all the dielectric materials are lossless and only conductive loss of the metal is included in simulations. Both CBCPW and CPW are low loss structures and have 50 Ω characteristic impedance. Therefore, the dominant attenuation

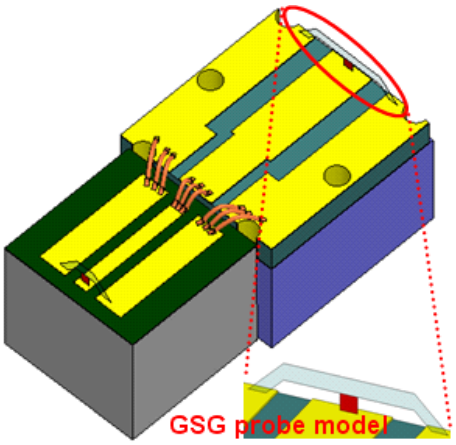


Figure 5.22: An EM model of a CPW-CBCPW wire-bonding transition; the excitation structure is enlarged as an inset.

contribution must come from the transition from the CPW to the CBCPW structure.

Fig.5.24 shows the electric field pattern at the gap between the CBCPW and CPW at 100 GHz, when the supportive brick is metallic. The pattern is neither CPW mode nor CBCPW mode. The strongest part of the E-field directly faces the metallic brick. A significant part of the EM power does not propagate from one chip to another but leaks into the gap between the chips. The leakage power radiates to free space or reflects back to the CPW. If the supportive brick is dielectric, the resonance and fast attenuation are less pronounced but still serious. Conclusively, the insertion loss in the transition is dominantly caused by the mode conversion from CPW mode to CBCPW mode and secondarily due to the metallic support. The mode mismatching effect is not significant in the low frequency range but leads to serious problems in the high frequency range.

A straightforward way to solve the problem is to avoid the mode mismatch in chip-to-chip transitions when interconnecting two chips with much diverse substrate thicknesses. A CPW with 50 Ω characteristic impedance is considered to replace the CBCPW and the metallic brick. The insertion loss of CPW-CPW wire-bonding transition is demonstrated in Fig.5.23, where two chips have similar substrate thickness. A significant improvement of insertion losses is achieved over 60 GHz, and the resonances in low frequency range also disappear. The promising result shows that the CPW-CPW tran-

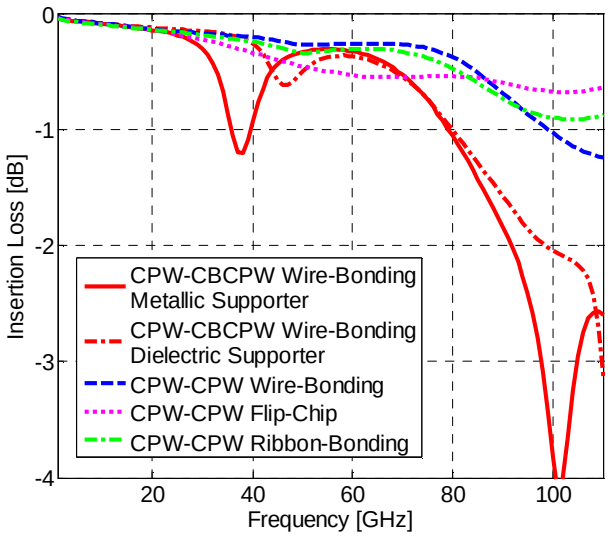


Figure 5.23: Insertion losses of interconnections with different integration technologies.

sition using wire-bonding only has 1 dB loss at 100 GHz. Two other state-of-art MCM technologies, flip-chip and ribbon-bonding, are also applied in CPW-CPW transitions. The insertion losses of the three interconnection technologies are comparable with each other. In details, wire-bonding has the lowest insertion loss below 85 GHz. This result clearly establishes that wire-bonding is an effective and low-cost interconnection technology for W-band applications among all the state-of-art MCM technologies.

5.3.5 New Packaging Design for PD Modules

Since the major bandwidth limitation and loss mechanism in the PD packaging is located at the PD chip to CBCPW transition due to the mode mismatch from CPW mode to CBCPW mode, utilizing a CPW with thick substrate instead of a CBCPW supported by a metal brick is considered to be a solution to enlarge the bandwidth and reduce the loss of the packaging structure.

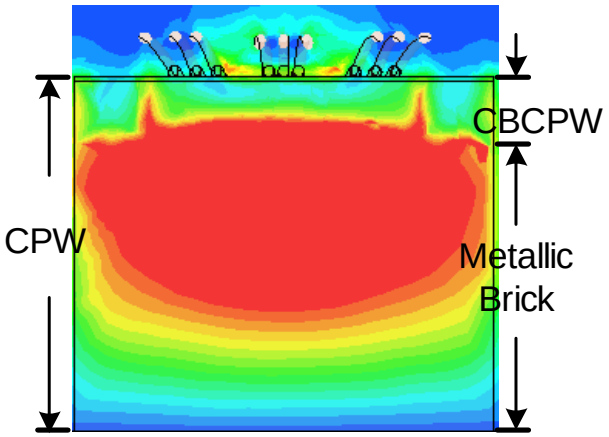


Figure 5.24: Electric field pattern at the CPW-CBCPW transition with a metallic brick at 100 GHz

The Packaging of PD Module with CPW

Based on the accurate EM behavioral model of photodiode chips, the EM model of packaged PD module is developed. Fig.5.25 shows the top view and side view of the EM model of packaged PD module. The model resembles the "module 2" which is illustrated in Fig.5.17(a). The model consists of a launch body of 1mm coaxial connector, a CBCPW structure with a metal supporter, bonding wires connecting the CBCPW to the photodiode chip, conductive glues for interconnection and an EM model of a photodiode chip. Therefore, the EM model of the packaged PD module includes all passive components in the packaging structure, a kernel active component and two major transitions which are the chip-to-CBCPW transition and the CBCPW-to-coaxial transition.

A very good agreement between measurement and the EM modeled relative responses of the original PD module is achieved as shown in Fig.5.26(b). "Original Module" denotes the module which is originally packaged by using CBCPW, and "New Module" denotes the module which is newly packaged by using CPW with thick substrate. The fast attenuation beyond 60 GHz is associated with the chip-to-CBCPW transition, which is similar to the curves in Fig.5.20. The wire-bonding CPW-CBCPW transition from the PD chip to the CBCPW is identified as the dominant contribution to the fast attenuation.

In the EM model of the new module as shown in Fig.5.26(a), a CPW with

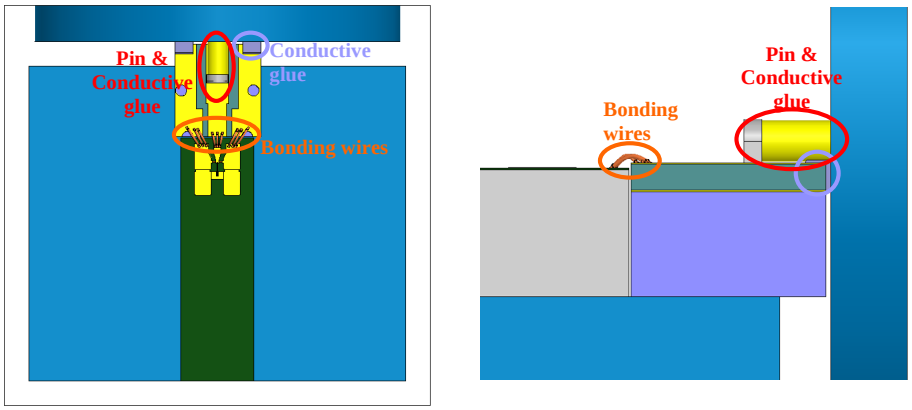
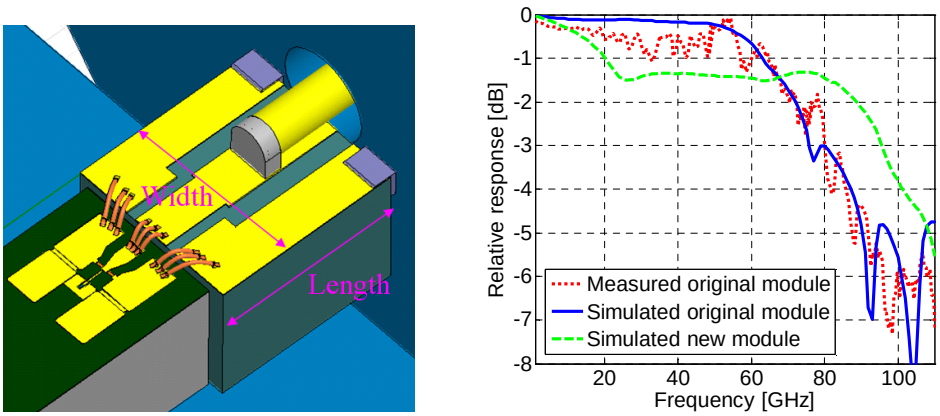


Figure 5.25: The top view and side view of the EM model of packaged PD module.

a comparable height to the PD chip replaces the CBCPW and the metallic support. The length of the CPW is 760 μm and the width of the CPW is 700 μm. The layout of the top metal layer is identical to the metal layer of the "original module". The mode conversion loss in the module packaging is eliminated by this solution as stated previously. As plotted in Fig.5.26(b), the 3-dB bandwidth of the "new module" is about 95 GHz with improvement of approximately 15 GHz as compared to the "original module". Since the CPW is not designed for 50 Ω characteristic impedance, the "new module" has lower relative response than the "original module" in the low frequency range because of impedance mismatch between the PD chip and the CPW. Another merit of using thick CPW structure is that the packaging fabrication of procedure is simplified. For instance, vias do not need to be developed in the CPW.

A PD module has been fabricated to verify the performance of the module utilizing the packaging structure with equivalent thick CPW. The "equivalent" thick CPW means the CPW is developed based on a CBCPW. The CBCPW is firstly manipulated by removing the backside metallization. A quartz brick is selected to support the original CBCPW without backside metallization, and dielectric glue is used to combine these two components together. The metal layer layout is the same as the original CBCPW. Therefore, the newly developed CPW is not optimized for the PD packaging purpose. It is just used to verify the mode mismatch effect in CPW-to-CBCPW transitions.



(a) (b)

Figure 5.26: (a) EM of the PD module using CPW; (b) measured and simulated relative responses of the original PD module with CBCPW and new PD modules with thick CPW.

Measurement results in Fig.5.27 demonstrate that the relative response of the new preliminary module becomes flat in the range of 60 GHz to 100 GHz when a thick CPW is used. It proves the mode conversion loss from the CPW output of the PD chip to the CBCPW is completely eliminated in the new module. A remarkable improvement in relative response is achieved above 80 GHz, and the 3-dB bandwidth is up to 100 GHz. The high loss in the low frequency range below 80 GHz can be improved by avoiding the impedance mismatch and inhomogeneous CPW substrate in the new packaging structure.

Optimization on the Packaging with CPW

After the CPW is verified to be an ideal candidate in the PD packaging, the characteristic impedance and the impedance transition of the CPW are also required for further optimization. They are determined by the width of the signal strip (S) and the gap of CPW (W). The characteristic impedance of the output CPW pads of photodiode chips is designed to be 50 Ω. The characteristic impedance of the 1mm coaxial connector is also 50 Ω. Therefore, the characteristic impedance of the CPW, which bridges the chip to the connector, should be 50 Ω to avoid impedance mismatch in the packaging structure. Because the dimensions of the connector and the chip are not similar, the dimension of the CPW needs to vary from chip side to con-

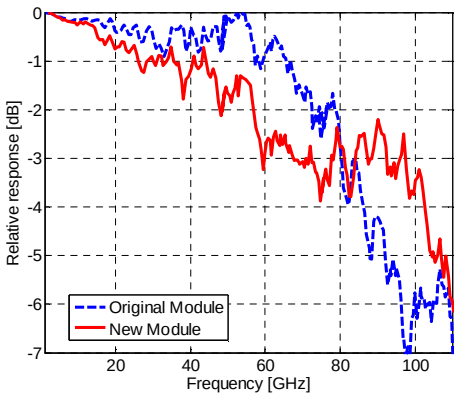
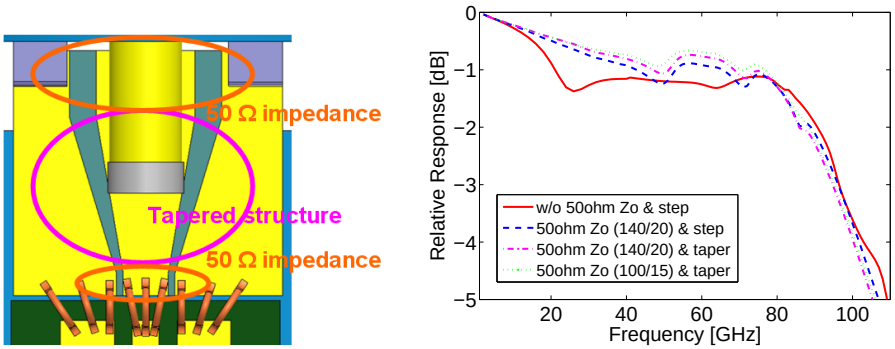


Figure 5.27: Measured relative responses of the original module using CBCPW and the new module using CPW.

nector side. Compared to step transition in CPW structure as shown in Fig.5.26(a), the taper CPW transition from chip side to the connector side is recommended as shown in Fig.5.28(a). The characteristic impedance of CPW is designed to be 50 Ω for both sides. At the connecter side, the CPW conductive glued with the pin of the connector is similar to a CPW with a very thick signal strip. The influence from the pin of the connector at the connector side on the characteristic impedance has to be considered.

Fig.5.28(b) shows the simulated relative responses of the module with different CPW structures. The solid curve is the relative response of the module using the equivalent CPW. Even though the 3-dB bandwidth is close to 100 GHz, the relative response exhibits relatively high loss in the low frequency range. This low frequency loss may be due to the mismatch of the characteristic impedance of the CPW and the 50 Ω and due to the step transition in the CPW. When the characteristic impedance of the CPW is firstly designed to be 50 Ω (dashed curve), the relative response below 70 GHz is improved. The number in the curve legend (nr./nr.) indicates S/W at the chip side with the unit being "μm". When the CPW transition secondly changes from step to tapered shape (dot-dash line), the relative response improves further below 70 GHz. Although inductive effect due to the step impedance transition may have a peaking effect in the high frequency range, the lower loss due to the taper transition in low frequency range is preferred in the packaging designs. If the CPW dimension $(S + 2W)$ is more compact while keeping 50 Ω, less EM power in CPW propagating mode may leak to

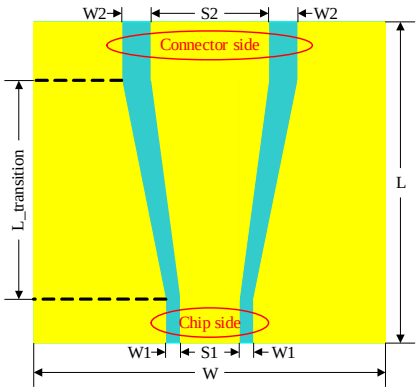


(a) (b)

Figure 5.28: (a) EM model of the PD module packaging using CPW; (b) simulated relative responses of the PD modules with different CPW characteristic impedances and impedance transitions: tapered and stepped.

other modes for achieving better transmission performance. The dot curve shows that smaller CPW dimension improves the relative response below 70 GHz.

After summarizing all above simulation results for optimizing the CPW, the layout of the optimized CPW is shown in Fig.5.29(a), and the suggested values for the corresponding parameters are listed in Fig.5.29(b), where h is the thickness of CPW substrate and other parameters are stated in Fig.5.29(a). The length and width of the CPW, which are indicated in Fig.5.26(a), are suggested to be short and possess comparable width to the PD chip, respectively. However, since these dimensions are not critical, the CPW can be tolerant to larger size for the easier fabrication. The gap of the CPW structure is suggested to be small. Two S/W combinations are provided in the table. The gap between metal strips being 15 μm is the limitation of a ceramic vendor. Thickness of the CPW substrate is the same as the nominal thickness of the PD chip. The length of the CPW impedance transition is suggested to be long enough to enhance the smoothing impedance variation. The substrate material of the CPW is suggested to be quartz because of its low dielectric constant. Based on the provided optimization scheme for CPW, the high low frequency loss problem in the first module using equivalent CPW should be solved. Simulation results have demonstrated the improved relative response below 70 GHz.



(a)

Parameters	Suggested value (μm)
S1	140/100
W1	20/15
S2	220
W2	60
L	500
W	600
L_transition	350
h	500

(b)

Figure 5.29: (a) The schematic of the CPW with parameters; (b) a table for listing the value of optimized CPW parameters.

5.4 Summary and Perspective

This chapter presented the design of PD module packaging for 100 Gbit/s applications. The procedure of design is based on accurate and reliable EM simulations. EM simulations efficiently identify the source of bandwidth limitation and loss mechanism in the packaging structure, because precise simulation of the EM behavior of the packaged PD module is possible. Simultaneously, EM simulation provides a powerful tool for optimizing the packaging structure. This approach is an alternative to the EM/circuit co-simulation method, because all the circuit elements are included in the concerned EM model. The latest packaged PD module exhibits very good relative response, which provides 3-dB bandwidth up to 100 GHz. The further optimization shows that lower loss in the low frequency range is achievable.

The packaging structure of PD module is comprehensive. It includes wire-bonding interconnection, CPW or CBCPW, and the CPW/CBCPW-to-coaxial transition. Wire-bonding technology has been proven to achieve comparable performance to flip-chip technology for millimeter-wave applications if the bonding wires are well developed. The mode conversion loss from CPW mode to CBCPW mode has been demonstrated for the first time by EM simulations. Furthermore, the structures for packaging PD module, such as bonding wires and CPW/CBCPW structures, are widely used in other millimeter-wave integrated circuit systems in packaging. The results in this chapter are quite general instead of specific for the PD packaging design.

The investigation in the PD module packaging provides an access to fully understand the obstacles and difficulties in packaging such devices working in the millimeter-wave range or even the submillimeter-wave range.

Chapter 6

Conclusions

In this Ph.D thesis work, the package and interconnect structures in millimeter-wave and high-speed communication systems were investigated using accurate and reliable EM simulations. As the foundation of the work, the accuracy of EM simulations has been improved by employing novel excitation schemes for coplanar structures. The EM simulations with improved accuracy make it possible to predict the EM properties of the microwave structures. This feature guarantees that EM designs result in first pass success. Furthermore, the EM modelling and designs based on EM simulations were extended to the active device domain. Full 3D EM models of photodetector chips have been developed to predict the O/E response of the devices.

In addition to summarizing the general principles for accurate EM simulations based on two practical EM design examples, this thesis proposes a novel excitation scheme for the first time to simulate on-wafer measured passive components. A ground-ring excitation scheme based on lumped ports resembles the real on-wafer measurement setup and a simple ground-signal-ground (G-S-G) probe model is exploited in EM simulations. This excitation setup avoids the inevitable drawbacks caused by other excitation schemes such as wave ports, which are usually considered as an effective way to excite most EM models. When the working frequency enters millimeter-wave range, the parasitic inductance and capacitance, which are at the scale of "fF" and "pH", respectively, from the G-S-G probe model seriously affects the simulation results, and therefore calibration simulations have to be added. The extended L-2L calibration technique is utilized to extract both the shunt parasitic capacitance and series parasitic inductance and de-embed them. Very good agreement between the measurement and simulation results after calibration is achieved from DC to 65 GHz. The ground-ring setup has

been used to excite coplanar structures throughout the thesis work. It is demonstrated to be the only correct scheme to excite coplanar structures.

Since the CBCPW structure is very popular in interconnecting chips in MMIC systems, the propagation and dispersion characteristics of CBCPW transmission lines based on single layer substrate were studied by using the accurate EM simulation techniques. The existence of the parallel plates and the grounded dielectric slab surrounding the CPW structure inevitably results in the parallel plate mode propagation, patch antenna mode resonances and surface wave mode leakage in CBCPW structures. The dimensions of the CBCPW structure were systematically analyzed. It is found that a CPW structure with much smaller dimensions than the thickness of the substrate prevents the leakage from the CPW mode to the parasitic modes and low dielectric constant material should be used as the substrate to minimize the electrical length of interconnection structures. A single layer quartz-based CBCPW structure with 1mm length, which is designed according the above recommendations, exhibits less than 0.6 dB loss up to 300 GHz in EM simulations.

Although placing vias in CBCPW structures is considered as a solution for achieving excellent transmission performance of CBCPW structures, the power leakage from the CPW structure to the surrounding parallel plate is still observed in both measurement and EM simulation results. The developed correct EM model of the CBCPW structure with vias has to be based on our ground-ring excitation scheme. Placing vias at the edge of CBCPW structure and keeping the distance between vias as close as possible increase the frequency at which the power leakage takes place. A 4 mm long 50 Ω CBCPW structure with vias based on quartz is expected to have less than 0.5 dB insertion loss at 110 GHz.

The EM modelling technique has been extended to the domain of active devices. P-I-N photodiode devices have been modelled at the behavioral level in EM simulations in the thesis work. It is the first proposed full 3D EM model for active devices. The behavioral 3D EM models of photodetectors precisely describe the optical-electrical responses of the devices. Besides *RC* bandwidth limitation, the transit-time effect is also included in the EM model. Therefore, the electrical power introduced into the passive structure of the PD model contains the bandwidth limitation due to the transit-time effect. One benefit of using full 3D EM models is that one does not have to extract parasitic elements in the circuit model. The other benefit is that circuit/EM co-simulation can be avoided when the complex structures surrounding active devices need to be designed and optimized. With the improved capability of computers, the simulations on full 3D EM model take

only tens of minutes. The simulation time is acceptable for practical designs. One PD model for 100 Gbit/s applications has been developed for further module packaging design. Another PD model has been developed for THz photomixer applications in order to improve the output power. Simulation results demonstrate that the expected THz output power can be improved by 11 dB at 700 GHz. Using EM models of active devices is demonstrated as an efficient approach to optimize the devices and design surrounding packages and interconnects.

The packaging of PD module for 100 Gbit/s applications is designed by using previously developed accurate EM simulation techniques. The performance degradation due to the packaging structure has been successfully identified by the EM model of the module. The packaged PD module comprehensively includes a 1 mm coaxial connector, a CBCPW structure, and a PD chip. The parallel plate mode resonance is found to be the major problem of affecting the transmission characteristic of the coaxial-to-CBCPW transition. Developing vias to short the electric field maxima of the resonance is suggested to suppress the resonance in CBCPW structures.

A simplified model of the module is not sufficient to model all the attenuation effects of the packaging structure. But an optimal packaging scheme is proposed based on the simplified model. Flat transmission characteristic and 0.4 dB insertion loss of the packaging structure is predicted. This scheme was verified by experimental results with more than 5 dB loss deduction at 110 GHz and 5 GHz bandwidth improvement. An ideal packaging scheme by directly soldering a coaxial connector on the PD chip exhibits no more than 1.5 dB attenuation up to 150 GHz due to the packaging structure. Because of the limitation of the practical packaging technology, CBCPW is still required to connect the chip to the connector with wire-bonding technology. Optimizations on the bonding wires dimensions and arrangement improve the relative response of the module.

A full EM model of the module based on the EM model of the PD chip precisely describes the relative response behavior of the packaged PD module. Mode conversion from CPW mode to CBCPW mode was identified as the major loss mechanism in the packaging structure after other mechanisms have been eliminated. Simultaneously, wire-bonding technology was proved to possess comparable transmission performance to flip-chip technology in millimeter-wave frequency range. CPW with comparable thick substrate to the PD chip was suggested to replace the CBCPW with a supportive metallic brick. More than 100 GHz 3-dB bandwidth was predicted by simulation results. Experimental results verified the proposed packaging scheme by using thick CPW structure. It is concluded that mode matching is a crucial

issue in designing packaging structures for high frequency applications.

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