Single Conversion stage AMplifier - SICAM

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SIngle Conversion stage AMplifier - SICAM

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To Elena and Emma,
for their endless love and devotion

Preface

The work presented in this thesis is part of the project "SICAM - SIngle Conversion stage AMplifier", funded by the Danish Energy Authority under the EFP2002 program, J.nr. 1273/02-0001. The project was carried out at the Ørsted·DTU Automation department within its Power Electronics Group (PEG) during the period November 15^{th} 2002 to December 31^{st} 2005. On the industry side, the cooperation with Bang & Olufsen ICEpower a/s in Kgs. Lyngby has given additional quality to the project, by emphasizing its relevance and importance within the extremely "crowded" consumer audio market.

Part of the work concerning the direct audio power amplifiers for portable applications and their digital modulators was conducted during my 1,5 months long external research stay in the Laboratory for Low Power Management and Integrated SMPS at the University of Toronto in Canada, under the supervision of Professor Aleksandar Prodić.

First I would like to express deepest gratitude to my supervisor Professor Michael A.E. Andersen for taking me as his Ph.D. student to work on this highly interesting topic, providing unbounded support for my wide research interests, managing the practical issues about the demanding project, as well as spending lots of hours on fruitful discussions and sharing his vast knowledge. Together with the colleagues from the Power Electronics Group and the Ørsted·DTU Department, they are most responsible for making me feel so comfortable and secure.

The practical relevance and technical appeal of the project would be much less pronounced, if it was not for the tremendous effort shown by my second supervisor Lars Petersen, from the cooperating company Bang & Olufsen ICEpower. His curious remarks and on-place questions have always provoked me to rejudge the conclusions and find a way out of the large maze I was put into when undertaking this project. The enthusiastic B&O ICEpower employees showing me around the labs and attending my presentations helped me build a serious approach so needed when tackling such a relevant subject.

Another thanks goes to my external research supervisor Professor Aleksandar Prodić from the University of Toronto, for allowing me to spend a challenging few weeks in his "fully digital world" and sharing his ideas and opinions, making the time spent in Toronto an unforgettable experience.

During these three stressful years of hard work, tight schedules and numerous obligations, I have always found a peaceful shelter and source of endless joy and fulfilment in my closest family - my wife Elena and our little daughter Emma. I would like to thank you for being always by my side and showing me that the most important things in life cannot be represented by equations, expressed in numbers nor measured in physical units...

Kongens Lyngby *Petar Ljušev*

December 2005

Abstract

This Ph.D. thesis presents a thorough analysis of the so called SICAM - SIngle Converter stage AMplifier approach to building direct energy conversion audio power amplifiers. The mainstream approach for building isolated audio power amplifiers today consists of isolated DC power supply and Class D amplifier, which essentially represents a two stage solution, where each of the components can be viewed as separate and independent part. The proposed SICAM solution strives for direct energy conversion from the mains to the audio output, by dedicating the operation of the components one to another and integrating their functions, so that the final audio power amplifier represents a single-stage topology with higher efficiency, lower volume, less board space, lower component count and subsequently lower cost.

The SICAM approach is both applicable to non-isolated and isolated audio power amplifiers, but the problems encountered in these two cases are different. Non-isolated SICAM solutions are intended for both AC mains-connected and battery-powered devices. In non-isolated mains-connected SICAMs the main idea is to simplify the power supply or even provide integrated power factor correction (PFC) functions, while still maintaining low component stress and good audio performance by generally decreasing the input voltage level to the Class D audio power amplifier. On the other hand, non-isolated battery-powered SICAMs have to cope with the ever changing battery voltage and provide output voltage levels which are both lower and higher than the battery voltage, while still being simple and single-stage energy conversion solutions. In isolated SICAMs the isolation transformer adjusts the voltage level on the secondary side to the desired level, so the main challenges here are decreasing the size of the magnetic core and reducing the number and size of bulky reactive components as much as possible.

The main focus of this thesis is directed towards the isolated SICAMs and especially the so called isolated SICAM with non-modulated transformer voltages. The latter is found to be the most interesting isolated SICAM solution for the modern multichannel audio power amplification systems, since all of the output stages corresponding to the different audio channels can reuse the same input stage and transformer core. While the proposed approach tends to be very simple from topological perspective and allows for reduction of reactive component count, the commutation of the load current in the output bridge and the bridge itself are much more complicated than their Class D predecessors.

The main contribution of the thesis can be found in the thorough analysis of the present topologies for isolated SICAMs, as well as the numerous structural improvements and several newly proposed control methods for alleviating the problem of load current commutation and high-performance control of the whole SICAM. Another significant contribution is the presentation of several interesting topologies and associated control principles in the field of non-isolated SICAMs for mains-connected and portable audio amplifiers.

Resumè (Abstract in Danish)

Denne Ph.D. afhandling giver en grundig analyse af den så kaldte SICAM - SIngle Converter stage AMplifier fremgangsmåde til opbygning af audio effektforstærkere til direkt energiomforming. Den aktuelle fremgangsmåde til opbygning af isolerede audio effektforstærkere i dag består af en isoleret DC elforsyning efterfulgt af en Klasse D audio effektforstærker, som faktisk repræsenterer to-trins løsning, hvor hver halvdel kan ses som seperat og uafhengig del. Den foreslåede SICAM-løsning stræber efter så direkte energiomforming fra lysnetindgangen til audioudgangen som overhovedet muligt, ved at dedikere virkningsmåden af delene til hinanden og integrere deres funktioner således, at den endelige audio effektforstærker repræsentere en en-trins topologi med højere effektivitet, mindre volumen, mindre printareal, færre komponenter og dermed lavere omkostninger.

SICAM fremgangsmåden kan bruges til både uisolerede og isolerede audio effektforstærkere, men problemstillingerne som i de to tilfælde er i grunden meget forskellige. Uisolerede SICAMs anvendes til både lysnettilsluttede og batteridrevne apparater. Hovedideen i de uisolerede lysnettilsluttede SICAMs er at forenkle spændingsforsyningen og lave PFC-funktion, mens det lav komponentstress og den god audioperformance bevares ved at reducere indgangsspændingen til Klasse D forstærkeren. Uisolerede batteridrevne SICAMs skal klare den varierende batterispænding og skabe en udgangsspænding, som er både lavere og højere end batterispænding, men de skal stadigvæk være simple og en entrins energiomformer. I transformatoren i isolerede SICAMs designes spændingsniveauet på sekundæren til det ønskede niveau og derfor er de vigtigste udfordringer her at reducere volumen af den magnetiske kerne og reducere antallet af reaktive komponenter så meget som muligt.

Hovedfokus i denne afhandling ligger på isolerede SICAMs og især de såkaldte isolerede SICAM med umodulerede transformatorspændinger. Den ovennævnte omformer er den mest interessante SICAM-løsning til multikanalens audio effektforstærkersystemer, fordi alle udgangstrinnene kan bruge det samme indgangstrin og den samme transformatorkerne. Den foreslåede løsning er meget enkelt fra en topologiside og tillader reduktion af antalet of reaktive komponenter på sekundærsiden, men kommuteringen af belastningsstrømmen i udgangstrinnet og udgangstrinnets ombygning selv er mere indviklet end i Klasse D forstærkeren.

Afhandlingens hovedbidrag findes i den grundige analyse af nuværende topologier for isolerede SICAMs, såvel som flere strukturele forbedringer og nogle foreslåede kontrol metoder til at forbedre kommuteringen af belastningsstrømmen i udgangstrinnet og realisere højperformance styring af hele SICAM-trinnet. Det anden væsentlige bidrag er fremvisningen af adskillige interessanter topologier og deres styrestrategier til uisolerede SICAMs til lysnettilslutning og brbare audio effektforstærkere.

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List of Abbreviations

AC - Alternating Current
AM - Amplitude Modulation
CCM - Continuous Conduction Mode
DC - Direct Current
DCM - Discontinuous Conduction Mode
DFS - Double Fourier Series
EMC - ElectroMagnetic Compatibility
EMI - ElectroMagnetic Interference
ESR - Equivalent Series Resistance
ESL - Equivalent Series Inductance
GLIM - Global Loop Integrating Modulator
HF - High Frequency
HV - High Voltage
IC - Integrated Circuit
LF - Low Frequency
LV - Low Voltage
M/S - Master/Slave
ODF - Overdimensioning Factor
PAE - Pulse Amplitude Error
PDM - Pulse Density Modulation
PLD - Programmable Logic Device
PSRR - Power Supply Rejection Ratio
PTE - Pulse Timing Error
PWM - Pulse Width Modulation
RCD - Resistor-Capacitor-Diode
RHPZ - Right Half-Plane Zero
RMS - Root Mean Square
SICAM - SIngle Conversion stage AMplifier
SOHF - Self-Oscilating High Frequency-link converters
SPRC - Series-Parallel Resonant Converter
SRC - Series Resonant Converter
SMPS - Switching-Mode Power Supply
THD+N - Total Harmonic Distortion + Noise
UPS - Uninterruptible Power Supply
ZCS - Zero Current Switching
ZVS - Zero Voltage Switching

1

Introduction

"Even the longest journey starts with the first step."

- Confucius

By definition, sound represents an acoustical or mechanical longitudinal pressure wave motion in an elastic medium, like gas, liquid or a solid. The audible frequency range is starting from around 20 Hz and ending around 20 kHz, but it is quite dependant on the persons age and other personal dispositions. There are many different sound sources, like a vibrating body (ex. vocal cords), throttled air stream (ex. whistle), thermal (ex. gas heating), explosion (ex. firecracker), arc (ex. thunder), aeolian or vortex. It is interesting to notice that most of the aforementioned natural sound sources have their counterparts in the man-made musical instruments and other artificial objects from our everyday life. On the other hand, the ultimate sound receiver, neglecting any intermediate sound storage, is the human ear consisting of the external ear, ear drum, middle ear bones, membrane and cochlea. Its complex structure leads to many interesting phenomena studied entirely by the science of psychoacoustics and finding many useful technical applications, like for example the advent of advanced human-hearing models for developing highly efficient audio compression algorithms.

The need for audio sound amplification stems from the fact that most of the natural or artificial sound sources today create just modest sound pressure levels, which are usually not sufficient to effectively address the public and cover larger ambient. On the other hand, audio power amplification is unavoidable when reproducing prerecorded materials, no matter whether the storage has an analog or a digital format. Despite of the first mechanical audio power amplifiers using a wooden horn for amplifying the grooves embossed on a cylinder or disk played back through a phonograph or gramophone, modern audio power amplifiers are entirely electrical devices using some kind of electrodynamic (moving coil or ribbon), electrostatic or piezoelectric loudspeaker as their output. The very low power conversion efficiency of the most common electrodynamic loudspeakers emphasizes even more the need for electrical audio power amplification.

The aim of this chapter is to make a short review of the common audio power amplification techniques, starting with the linear amplification as the oldest one and moving to the switching-mode power amplification as the latest and most promising one. At the end, the SICAM project will be presented as the newest and most radical contribution to the switching-mode audio power amplification, developed for simplicity and effectiveness by making the energy conversion from AC mains to audio output straightforward and achieving the additional benefits of reduced volume and board space, less complexity, lower component count and subsequently lower cost.

1.1 Linear audio power amplifiers

The linear audio power amplifier is characterized by having its output power devices, being vacuum tubes, bipolar junction transistors (BJTs), field effect transistors (FETs)

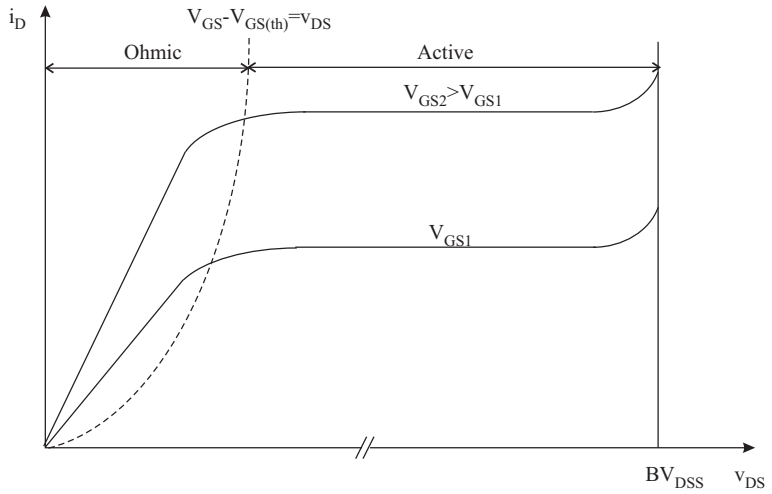

Fig. 1.1. I-V characteristics of MOSFET

or some other semiconductor technology, operated in the linear part of their corresponding current-voltage (I-V) characteristic, shown for the MOSFET in Fig. 1.1. In this case, the MOSFET is operated with low gate-source voltages and is said to be in its active region [13]:

$$v_{GS} - V_{GS(th)} < v_{DS} \tag{1.1}$$

where v_{GS} is the gate-source voltage, $V_{GS(th)}$ is the gate-source threshold voltage and v_{DS} is the drain-source voltage. As shown in Fig. 1.1, in the active region of the MOSFET the drain current i_D is function only of the applied gate-source voltage v_{GS}. At the same time, the drain-source voltage v_{DS} can be in a very large span of voltages up to the breakdown voltage BV_{DSS}, creating quite large conduction losses in the device:

$$P_{FET,con} = v_{DS} \cdot i_D \gg 0 \tag{1.2}$$

A scheme of a MOSFET output stage of a single-ended linear audio power amplifier is depicted in Fig. 1.2, while the power supply voltages and load voltage are shown in Fig. 1.3. The scheme also includes the connection points of the control feedforward and control feedback signals.

When looking in Fig. 1.3, it can be concluded that the output power devices in linear audio power amplifiers act as voltage- or current-controlled variable resistors, dropping across them the part of the voltage $\Delta v_{M1}, \Delta v_{M2}$ being the difference between the fixed

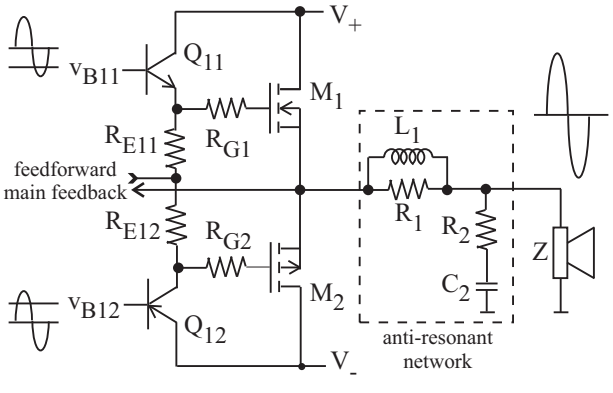

Fig. 1.2. Linear audio power amplifier with MOSFETs

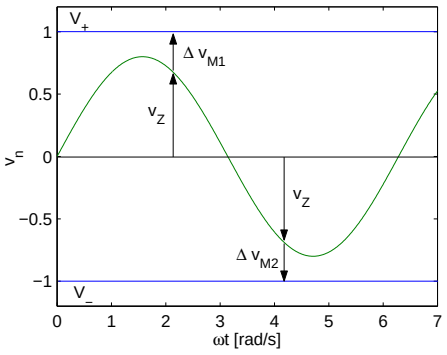

Fig. 1.3. Power supply voltage and load voltage with linear audio power amplifier

or variable split power supply voltages V_+, V_- and the desired load voltage v_Z across the impedance Z, while conducting the whole load current. As mentioned earlier, this leads to huge power dissipation in the active devices, which is comparable and often even higher than the useful output power in the load.

There exist different classes of linear audio power amplifiers [14]:

- **Class A:** Large pre-bias voltage/current is applied in the output stage, resulting in continuous conduction of both the low-side and high-side active devices throughout the cycle of the signal waveform. High linearity and performance are combined with huge power losses.
- **Class B:** Each of the active devices conducts only through the corresponding half of the cycle of the signal waveform. Due to the non-ideality of the active devices, crossover distortion is created when the signal waveform passes through zero.
- **Class AB:** Sufficient pre-bias voltage/current is applied to the Class B power amplifier, so that any crossover distortion is avoided. Combines good audio performance with satisfactory efficiency.
- **Class C:** Active devices are conducting less than half of the cycle of the signal waveform. Due to the higher level of signal distortion it is used only in Radio Frequency (RF) power amplifiers / transmitters.
- **Class B2, B3 ... BN:** Multiple active devices operate on multiple power supply rails to improve the efficiency of the Class B audio power amplifier depending on the signal waveform amplitude. Complex solution with improved efficiency compared with the conventional Class B.
- **Class G:** Linear audio power amplifier is operated with a variable power supply voltage. Highly efficient solution, but the complexity is transferred from the audio power amplifier to the power supply.

Although a thorough treatment of the different linear audio power amplifier classes is beyond the scope of this thesis, it can be mentioned that the large power losses accompanying the operation of the linear audio power amplifier are major obstacle to the trend of product integration. Latter is especially pronounced in the higher power range, where the output devices of the linear power amplifiers must be mounted on bulky heat sinks quite away from the temperature sensitive electronics. On the other end of the power range, the low power linear audio power amplifiers not only yield shorter battery operation time due to the inherent inefficiency of the output power stage, but also cause electronics overheating problems in the tightly crowded space of the modern portable devices. Therefore, linear audio power amplifiers on the consumer market today are being more and more replaced with the switching-mode audio power amplifiers, which tend to outperform the former amplifiers in terms of power efficiency and prospects for high-level integration.

1.2 Switching-mode audio power amplifiers

In the switching-mode audio power amplifier, the active devices are operated as switching elements by driving them deep into saturation or in off-state, rather than being linear elements with controlled variable resistance. As shown below, this has tremendous effects on the efficiency of the output power stage.

In the case of a MOSFET, switching-mode operation refers to operating the MOSFET alternatively in blocking state and in its ohmic region [13], where for the latter the gate-source voltage v_{GS} obeys:

$$v_{GS} - V_{GS(th)} > v_{DS} > 0 \tag{1.3}$$

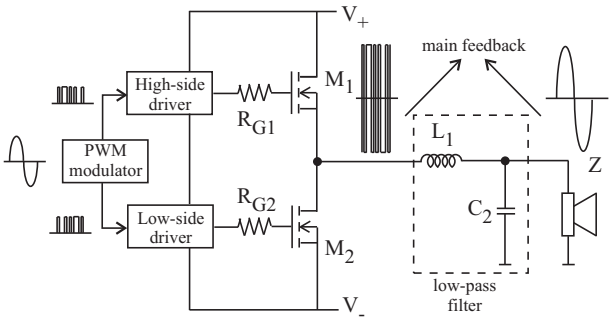

Fig. 1.4. Switching-mode audio power amplifier with MOSFETs

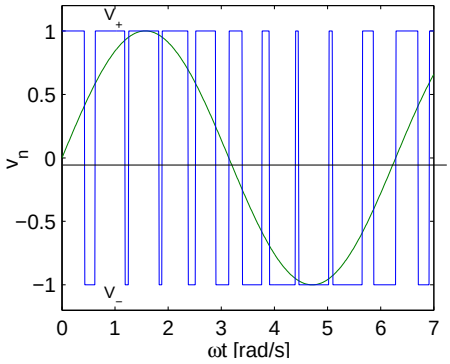

Fig. 1.5. PWM bridge voltage and load voltage with switching-mode audio power amplifier

When looking on the MOSFET $I - V$ characteristic shown in Fig. 1.1, this translates to either driving the MOSFET with large gate-source voltage v_{GS} to conduct large drain currents i_D with just a minor drain-source voltage v_{DS} or completely removing the gate drive to turn-off the device and collapse the drain current i_D, while blocking the entire power supply voltage across its drain-source. As a result of the switching-mode operation where either the drain-source voltage v_{DS} is negligible during the MOSFET on-state or the drain current i_D equals the very small drain-source leakage current I_{DSS} during the off-state, the conduction losses of the MOSFET approach zero:

$$P_{FET,con} = v_{DS} \cdot i_D \approx 0 \tag{1.4}$$

A scheme of a MOSFET output stage of a single-ended switching-mode audio power amplifier, usually referred as half-bridge Class D amplifier is depicted in Fig. 1.4, while the bridge voltage and load voltage are shown in Fig. 1.5.

Coding of the desired signal waveform with just two power supply levels V_+ and V_- necessitates some kind of modulation, either being Pulse Width Modulation (PWM), Pulse Frequency Modulation (PFM), Pulse Density Modulation (PDM) or some other hybrid type. Turning to the most common and popular type of modulation for Class D amplifiers, that is PWM, according to the number of levels this modulation principle can be further subdivided in two (AD) and three (BD) level, while according to the carrier shape there is further subdivision into single-sided (S) and double-sided (D) [14]. In particular, Fig. 1.5 shows double-sided two level (NADD) PWM coding of the signal waveform, the frequency of which is for the purpose of clarity comparable to the switching frequency of the output stage.

As a result of the fact that the bridge voltage, being the output voltage at the midpoint of the MOSFET totem pole, has only two or three voltage levels equal to the power supply rails and/or ground respectively, there is significant amount of off-band switching harmonics which are usually filtered out with second order low-pass LC filter placed in front of the loudspeaker, as depicted in Fig. 1.4. This is the price one needs to pay for reducing the energy of the high frequency (HF) switching harmonics and its sidebands, in order to avoid subsequent excessive losses in the conventional loudspeaker [15] or comply with the Electro-Magnetic Compatibility (EMC) standars. The problem with the possible Electro-Magnetic Interference (EMI) from the rapidly changing currents flowing through the Class D amplifier input lines is an issue, too.

Equation (1.4) predicts almost zero conduction losses of the ideal MOSFET operated in switching-mode, but unfortunately the real-life power MOSFETs, as shown in Fig. 1.6 are non-ideal switching elements which have a finite on-resistance of the conducting channel R_{DS}, leading to some conduction losses. On top of that, they have parasitic capacitances

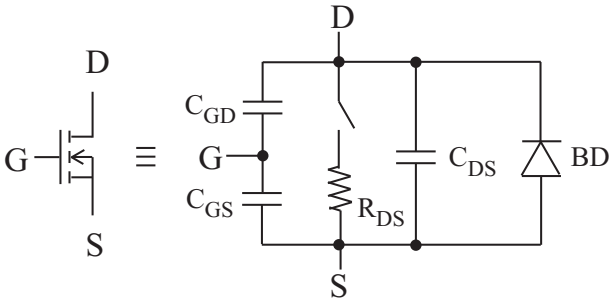

Fig. 1.6. Equivalent scheme of MOSFET

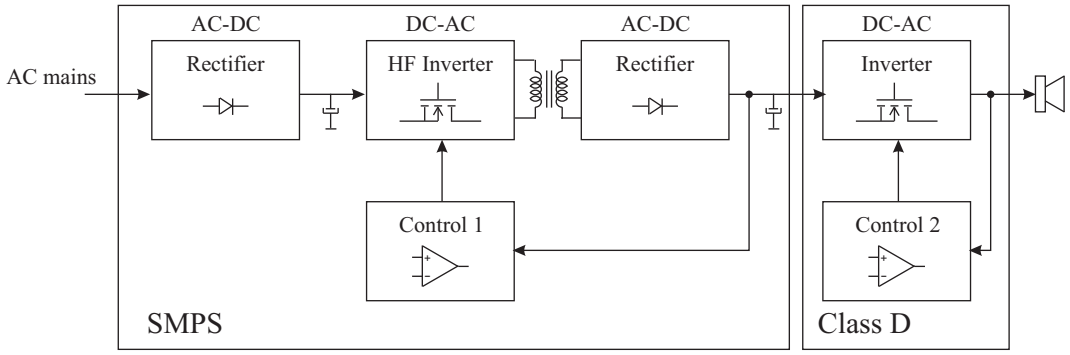

Fig. 1.7. Block diagram of completely switching-mode audio power amplifier

between the different electrodes, limiting their switching speed, which results in switching losses at each MOSFET state transitions. Both the conduction and switching losses of the power MOSFETs lead to power losses, which together with the losses in other components of the Class D audio power amplifier decrease its efficiency to a level which is still significantly higher than the one of a Class AB linear audio power amplifier.

One of the usually overseen components when discussing Class D audio power amplifiers is the power supply. No matter whether the application is AC mains-powered or battery-powered, some kind of AC-DC or DC-DC power supply is needed to create DC-bus link with sufficient voltage and low impedance, so that the audio performance of the amplifier throughout the whole power and frequency range is up to the expectations. Similar to the audio power amplifier, the power supply can be either linear or switching-mode, with the latter being the best choice in applications where the efficiency, weight, size and power density matter. The power supply itself is usually much more complex than the Class D amplifier itself, especially when it is to provide safety isolation from the AC mains with a minimum size magnetics and high efficiency, involving several energy conversion steps. A simple block diagram of a completely switching-mode audio power amplifier with a Switching-Mode Power Supply (SMPS) and a Class D audio power amplifier is shown in Fig. 1.7. The latter clearly presents the numerous energy conversions needed to transform the electrical energy from the input AC mains to the audio output. It also shows that in the common switching-mode audio power amplifier, SMPS and Class D audio power amplifier are connected through a DC-bus, i.e. a DC-link which separates this two units and enables greater flexibility by allowing SMPSs and Class D amplifiers from different manufacturers to get perfectly along, as long as the DC-bus has the right voltage level, sufficient power rating and low enough output impedance. Most usually, there is no communication between the SMPS and Class D amplifier and they both run their own feedback loops for rejecting any disturbances on the input power lines or power stage errors (except for the Class D audio power amplifiers with digital inputs, which are usually run in open loop and feedback is replaced by error precompensation).

If η_i represents the efficiency of the i-th energy conversion step in the audio power amplification chain, the total efficiency of the audio power amplifier is product of the corresponding efficiencies:

$$\eta_{tot} = \prod_{i=1}^{N} \eta_i \tag{1.5}$$

Since the efficiency of each of the conversion steps is smaller than one due to the unavoidable losses associated with each energy transformation, the total efficiency is much smaller than the efficiency of each of the constitutive parts. Equation (1.5) clearly emphasizes the improvement in efficiency resulting from possible reduction of number of energy conversion steps.

1.3 SICAM project and problem definition

Recalling the lessons learned in the previous section, significant improvements can be expected from the possible reductions in the complexity of the present completely switching-mode audio power amplifiers, by seamlessly integrating the SMPS and Class D audio power amplifier into one or two closely dedicated stages. The resulting highly integrated audio power amplifier is referred to as **SIngle Conversion stage AMplifier - SICAM** and is the subject of thorough examination in this thesis.

The technological possibility allowing for this total integration is the similar principle of operation of both the SMPS and Class D audio power amplifier, i.e. energy processing by alternately switching their active elements. This allows for dedication of the SMPS to the Class D audio power amplifier and vice versa, which excludes operation of the same SMPS with some other conventional Class D amplifier of the type described in Section 1.2. Even more, the roles of the two aforementioned units in creating the audio output become so intertwined, that there is no way of drawing firm borders between the power supply and the audio power amplifier anymore. Along with this integration of the corresponding power stages comes an integration of the control functions into a single unit, which further simplifies the resulting audio power amplifier. A simple block diagram of a SICAM, without any implications on its structure, is given in Fig. 1.8.

The aforementioned dedication of the SMPS to the audio power amplifier in SICAMs is being shown in a rather arbitrary way in Fig. 1.9. For example, the energy sent from the front-end SMPS to the audio amplification stage can be in a form of:

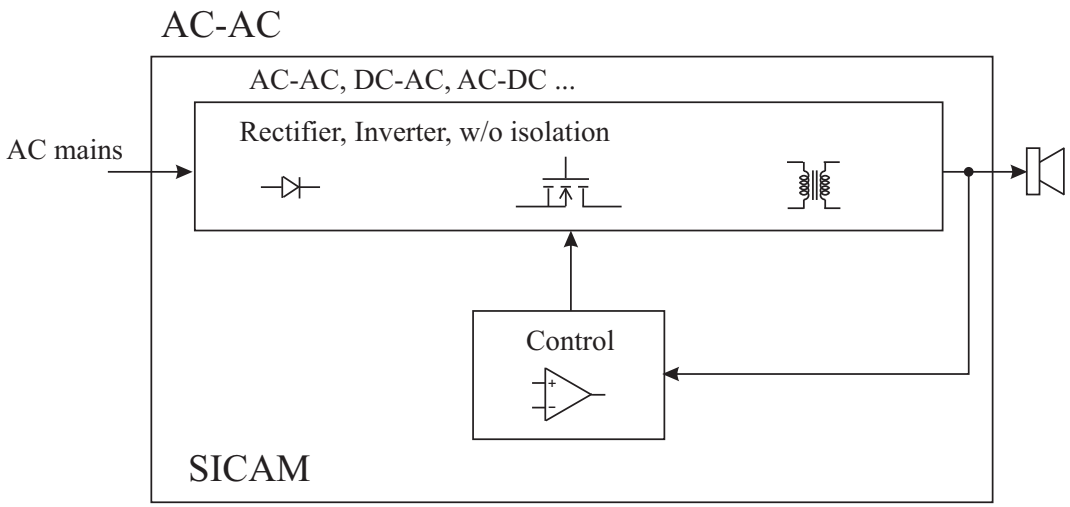

Fig. 1.8. Simple block diagram of SICAM

- 2-phase phase-shifted AC voltage which can provide continuous power flow to a matrix converter-type audio power amplifier,
- HF AC voltage from a resonant type SMPS is being delivered to a cycloconverting audio power amplifier,
- 2-phase DC voltage is being used by DC-DC audio power amplifiers connecting the load in differential mode,
- DC voltage is interfacing Class D audio power amplifier with a simple SMPS, etc.

The aforementioned approaches are by no means the only possible ones, and they are merely presented to show the myriad of feasible solutions, although not all of them with the same performance/cost ratios. The number of approaches increases even more with the fact that SICAM is supposed to address both the isolated and non-isolated direct energy conversion, since in certain instances where the audio power amplifier is entirely enclosed within a nonconductive box together with the loudspeaker, there is no need for providing isolation. Therefore, a proper definition of SICAM which is both general and applicable is:

> *"SICAM presents any power converter topology which strives for as direct energy conversions as possible from the power source to the audio output, within the given constraints."*

The main driving force behind the proposed higher level of integration and dedication between units is the wish for much more efficient switching-mode audio power amplifiers with even smaller form factors, higher power densities, lower component count and eventually the lower production cost that follows. It is also quite appealing for the Active Transducer (AT) [16] approach for direct conversion of the mains power into acoustic output in one simplified topological stage, like in the active loudspeaker systems and dedicated subwoofer units. Graphical comparison of the linear amplifier, switching-mode Class D amplifier and SICAM on the Level of integration / Cost scale is depicted in Fig. 1.10.

The targeted efficiency and Total Harmonic Distortion + Noise (THD+N) of SICAMs can be summarized in the following few points:

- <0.6% idle losses relative to full output power,
- >54% efficiency at 1% of full output power,
- >80% efficiency at full output power, and
- decent audio performance and low distortion (ex. THD+N<0.1%).

Although high energy conversion efficiency and low THD+N levels are very important for the acceptance of the SICAM audio power amplifier on the market, it is believed that there are some other factors like product simplicity, reliability, volume, power density, component count and eventually cost which will be the prime movers for the companies

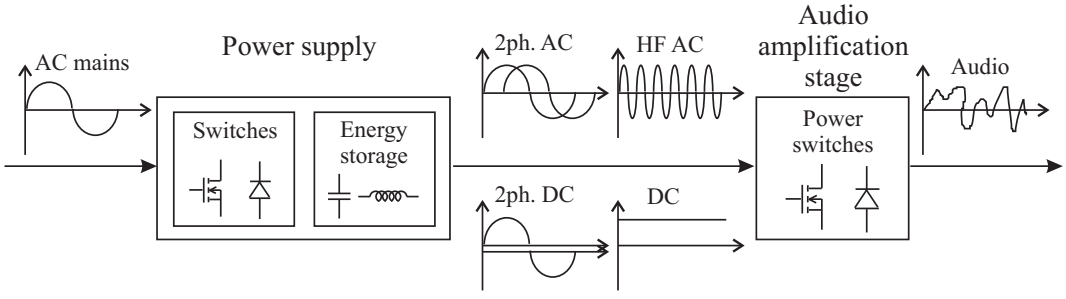

Fig. 1.9. Dedication of the SMPS to the audio power amplifier in SICAM

to push SICAM into technology development and later as products on the market. This is especially true if comparable power efficiency and THD+N like the present Class D solutions can be achieved, or they are such that at least some specific segments of the audio market can be targeted.

The addressed power range is 50 W to 500 W, which means that the power source for SICAM is intended to be single-phase AC-mains. For higher power range, some power factor correction (PFC) i.e. input current shaping according to the input voltage should be considered.

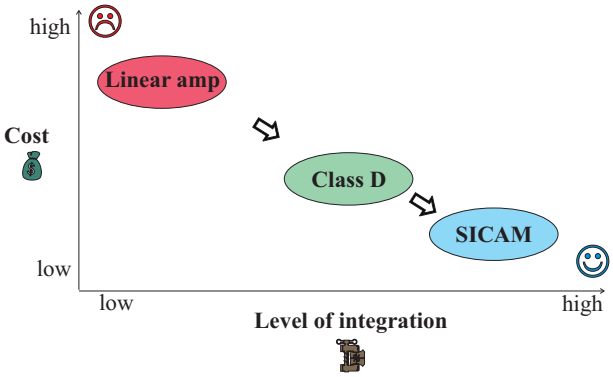

Fig. 1.10. Comparison of linear amplifiers, switching-mode amplifiers and SICAMs

This Ph.D. thesis should be looked upon in the light of the Confucius' proverb from the beginning of the chapter: it is just the first step to wider recognition, acceptance and continuing research of the possibilities for direct energy conversion with different SICAM-type converters not only for audio amplification, but also for Uninterruptible Power Supplies (UPSs), converters for renewable energy sources like Photo-Voltaics (PVs) and Fuel Cells (FCs), as well as general power conversion.

1.4 Need for energy storage on a single-phase AC-mains

One of the general issues that sheds some light on the limitations of the SICAM approach is the essential need for some energy storage during the intervals with low or zero input voltage of the single-phase AC-mains.

Rate at which electrical energy is supplied to the load is called electrical power, and its instantaneous value $p(t)$ can be found as a product of the voltage instantaneous value $u(t)$ and current instantaneous value $i(t)$:

$$p(t) = u(t)i(t) \tag{1.6}$$

AC-mains voltage has the form of a sinusoidal function:

$$u(t) = U_m sin(\omega t) \tag{1.7}$$

where $\omega = 2\pi f$ [rad/s] is the AC mains voltage angular frequency, f [Hz] is the frequency and t [s] represents the time.

From equations (1.6) and (1.7) it turns out that, at instants where mains voltage equals zero ($n\pi$ where n is an integer), i.e. at zero crossings there is no energy transferred to the load (unless the input current is infinite $i(t) \rightarrow \infty$, which is certainly not a viable assumption). Moreover, rate at which electrical grid supplies energy to the load is greatly reduced and performance is compromised in some vicinity of the zero crossing points.

In some appliances zero crossings of the main voltage does not disturb the operation of the device, especially if they represent slow processes which respond to the voltage effective value $U_{ef} = U_m/\sqrt{2}$ (ex. electroheating process, where the heater's power equals U_{ef}^2/R). In the audio appliances, where the audio effect and content are created on a time scale which is comparable or much shorter than the incidents of AC-mains zero voltage, on a continuous basis, any minor failure to provide the necessary power causes a major disturbance of the audio signal and adversely affects the high fidelity of the sound. In order to overcome this problem, some energy storage elements are introduced in the power supply, thus providing the energy needed for the audio amplification stage when AC mains voltage lacks the ability to do that.

This is a basic limitation of the mains-connected SICAM, since it cannot be constructed without some kind of a power supply, that will provide uninterrupted energy supply for audio conversion. Therefore, SICAM is intended to be a dedicated and closely interconnected two stage system, like the one depicted in Fig. 1.9, which has an input stage for power conditioning and storage (i.e. a power supply), and output switching audio stage.

Going back to the principles, power supply should convert and store the electrical energy into some other type of energy during the positive and negative half-cycles of the input AC mains voltage. Then it should retrieve it back around the zero crossing points, or deliver it to the load at a constant rate throughout the whole operating period. Electrical energy can be converted into:

- Magnetic energy - magnetic field (inductor),
- Electrostatic energy - charge (capacitor),
- Mechanical kinetic energy (ex. a flywheel),
- Mechanical potential energy (ex. a mass m elevated on higher ground in gravitational field),
- Chemical energy (battery), etc.

Except for the first two choices - the magnetic and electrostatic energy, all other types of energy have a low rate of conversion from and to electrical energy because of the high inertia they possess. Although the inductor and capacitor also possess some amount of inertia, described by their inductance L and capacitance C, they are exclusively used in the power supplies for the purpose of storing electrical energy.

SICAM doesn't impose any limitations on the form of the power supply output. It may seem that there is a huge array of different possible combinations of power supplies and subsequent power converter topologies, but their number is substantially reduced if one reconsiders the necessary conditions, that emerge from the SICAM and audio sound definitions, as well as viable regulations:

- Power supply must be capable of delivering/receiving electrical energy to/from the audio amplification stage at any time moment with the desired rate offering full dynamics,
- Power supply should incorporate a minimal number of switches (preferably unidirectional), possibly having a topology or providing some algorithm for lowering the switching and conduction losses, introduce low-level control (ex. for PFC) or make use of uncontrollable switches (ex. diodes), which will reduce the number of switch drivers,
- Switching audio stage should incorporate a minimal number of switches (preferably unidirectional), tending to minimize the losses without compromising the audio quality and providing high-level control to deal with plant uncertainties and perturbations,
- Both the power supply and audio amplification stage should incorporate fewer energy storage reactive components,
- Number of energy conversions should be kept as low as possible, and

- Power supply or audio amplification stage must provide galvanic isolation from the electrical grid if the voltage levels on the parts of the electric circuit that can be externally accessed are greater than the regulatory limits.

It seems adequate at this point to mention some of the trade-offs that are likely to be encountered in the quest for the ultimate direct single-stage audio power amplifier. As already mentioned, one of the main drivers behind the research in SICAMs are the savings that are expected to result from the tighter integration between the switching-mode power supply and the Class D audio power amplifier. These savings are sometimes too optimistically expected to arise from the reduced component count or the replacement of reactive components with semiconductor switches, without thorough analysis of the switch stress. Unfortunately, what the examples in other power electronics fields, like for example Power Factor Correction (PFC), show is that along with the transition from multi-stage to single-stage topologies with reduced component count the stress of this few switches tends to increase significantly, leading unexpectedly to lower reliability and higher component cost. The main intention of this discussion is to point out that moving to single-stage audio power amplifiers does not necessarily imply achieving a competitive edge with regard to the present state of the art two-stage approaches, and the advantages must be carefully analyzed by close comparison of units with similar specifications.

1.5 Thesis outline

The Ph.D. thesis is divided into two major parts: Part I is dealing with non-isolated SICAM topologies for both single-phase AC-mains and battery connected devices and Part II is dealing entirely with the isolated SICAM topologies.

Part I starts with the study of the applicability of the general matrix converter topologies to non-isolated SICAMs. Afterwards, focus is shifted to non-isolated SICAM topologies which are using rectification of the AC-mains voltage combined with DC storage capacitors to provide continuous power flow for the subsequent audio power amplification stage. At the end, some interesting SICAM topologies for battery powered devices, capable of stepping-up the input voltage are presented, along with appropriate digital control algorithms.

Part II begins with an introduction to the very complex topic of direct audio power amplification in a presence of isolation transformer. The subsequent chapters propose different topologies and several control approaches, capable of properly addressing most of the design challenges and achieving satisfactory performance while still being reliable and simple. Some combinations of SICAM topologies and control methods have been built as prototypes and the results are summarized in separate chapters. Although the main focus in the second part of the thesis is given to the group of isolated SICAMs with so called non-modulated transformer voltages, which are especially appealing for multichannel audio applications, one of the chapters will present very simple isolated SICAM with modulated transformer voltages based on common flyback converter. The final chapter in this part describes an especially interesting design of integrated magnetics, which can be used in all SICAMs to reduce the number of magnetic cores and thus save precious board space.

The thesis is finished with some concluding remarks and several appendices, dealing in detail with mathematical and other matters referenced throughout the thesis.

Part I

Non-isolated SICAMs

2

Matrix SICAM

"You know that I write slowly. This is chiefly because I am never satisfied until I have said as much as possible in a few words, and writing briefly takes far more time than writing at length. "

- Carl Friedrich Gauss

2.1 Matrix converters

Direct AC-AC energy conversion using matrix converters is considered to be the most general one [17],[18]. Matrix converter is capable of direct transformation of sinusoidal voltage level and frequency without any energy storage components, but some limitations apply [19]. In fact, maximum output voltage level is dependent on the input voltage amplitude and use of some reactive components is compulsory, in order to provide input current and output voltage filtering. However, these filtering reactive components have very low energy storage capability and therefore it can be assumed that in matrix converters at each point of time there is a balance between the energy taken from the utility grid and the energy transferred to the load.

Important advantages of the matrix converter are:

- Sinusoidal input and output waveforms, less higher order harmonics and no subharmonics,
- Bidirectional flow of energy,
- Minimal size reactive components (for filtering purposes), and
- Adjustable power factor [20].

A matrix converter with M input lines, N output lines and switches at their intersections is presented in Fig. 2.1, where sources are of a voltage type and loads of a current type.

State of each switch S_{ij} can be represented by its switching function H_{ij}, where:

$$H_{ij} = \begin{cases} 0, & \text{if switch } S_{ij} \text{ is OFF} \\ 1, & \text{if switch } S_{ij} \text{ is ON} \end{cases}, \; i = 1, 2, ..., M \text{ and } j = 1, 2, ..., N \tag{2.1}$$

In each horizontal (output) line there can be only one switch turned on, otherwise there will be a parallel connection of two ideal voltage sources on the input side, which in general have different instantaneous voltages. Therefore, a voltage condition can be defined as following:

$$H_{1j} + H_{2j} + ... + H_{Mj} = 1 \text{ , i.e. } \sum_{i=1}^{M} H_{ij} = 1 \tag{2.2}$$

At the same time, there must be a path for the output current from the ideal current sources to flow, resulting in the next current condition for the input lines:

$$H_{i1} + H_{i2} + ... + H_{iN} > 1 \text{ , i.e. } \sum_{j=1}^{N} H_{ij} > 1 \tag{2.3}$$

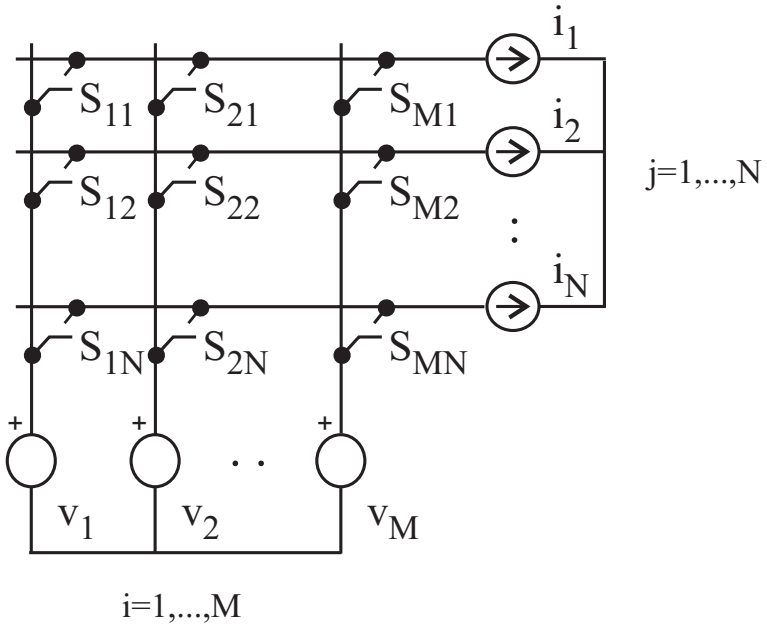

Fig. 2.1. M-phase to N-phase matrix converter

Matrix converter structure can be simplified by introducing a central tap in the M^{th} input line, by moving the voltage source V_M to each of the $M-1$ input lines to leave the M^{th} input line empty, or even connecting it directly to the N^{th} output line, thus eliminating the need for switches in that output line, according to the voltage condition (2.2). Latter situation is shown in Fig. 2.2.

Input voltages and output currents can be regarded as independent quantities, since their trajectory or time change is dictated by the electrical grid or the source requirements. Switching strategies of matrix converters largely depend upon the desired output voltages,

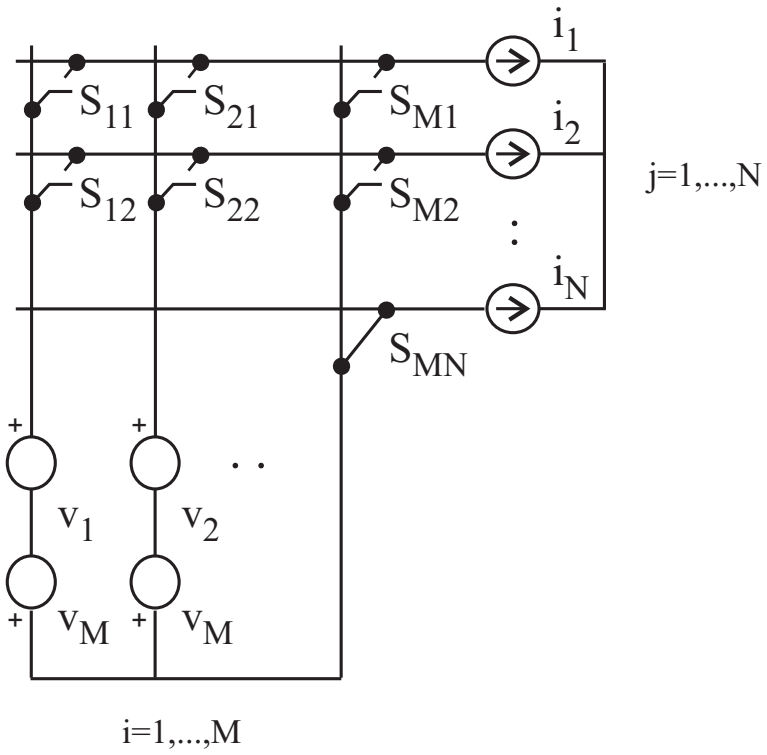

Fig. 2.2. M-phase to N-phase matrix converter with central tap in the M-th line

which are controlled to satisfy specific load demands. Input currents can be also an object of control to mitigate some power quality concerns, like low THD and providing PFC.

The subject of the following sections will be the problem of constructing single-phase output i.e. an AC audio signal, from a single-phase input AC voltage. Since this proves to be impossible, number of input phases will be increased, until the output characteristics fulfill the demands.

2.2 Single-phase AC to single-phase AC matrix converter

Single-phase AC to single-phase AC matrix converter is shown in Fig. 2.3. It has two input and two output lines, so it requires four switches.

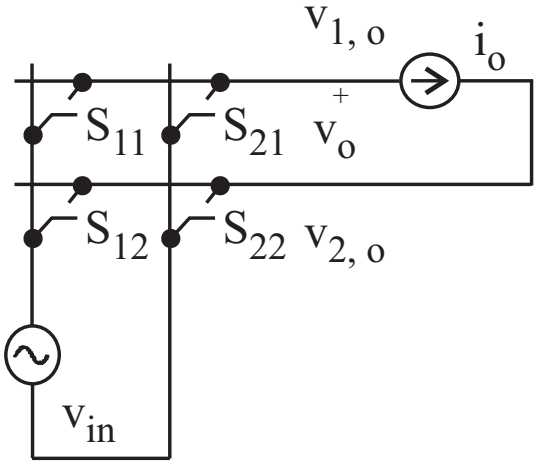

Fig. 2.3. Single-phase to single-phase matrix converter

Voltage condition (2.2) and current condition (2.3) in the case of the matrix converter shown in Fig. 2.3 transform to:

$$H_{11} + H_{21} = 1\ ,\ H_{12} + H_{22} = 1 \tag{2.4}$$

Input voltage has the following sinusoidal waveform:

$$v_{in} = V_{in,max} \sin(\omega_{in} t) \tag{2.5}$$

Output voltage v_o across the load can be found as a difference between the voltages of the output lines:

$$v_o = v_{1,o} - v_{2,o} = H_{11} v_{in} - H_{12} v_{in} = (H_{11} - H_{12}) v_{in} \tag{2.6}$$

Input current is sum of the currents flowing through the output lines:

$$i_{in} = (H_{11} - H_{12}) i_o \tag{2.7}$$

Before proceeding to further analysis, it is useful to determine the nature and characteristics of the switches S_{ij}. This can be done by looking at the direction of the blocking voltages v_{ij} when switched off and conducting currents i_{ij} when switched on.

Blocking voltages across the switches are:

$$\begin{aligned}
&S_{11} : v_{11} = v_{in} - v_{1,o} = v_{in} - H_{11} v_{in} = (1 - H_{11}) v_{in} \\
&S_{21} : v_{21} = 0 - v_{1,o} = -H_{11} v_{in} \\
&S_{11} : v_{12} = v_{in} - v_{2,o} = v_{in} - H_{12} v_{in} = (1 - H_{12}) v_{in} \\
&S_{22} : v_{22} = 0 - v_{2,o} = -H_{22} v_{in}
\end{aligned} \tag{2.8}$$

Conducted currents through the switches are:

$$\begin{aligned} &S_{11} : i_{11} = H_{11} i_o \\ &S_{21} : i_{21} = H_{21} i_o \\ &S_{11} : i_{12} = -H_{12} i_o \\ &S_{22} : i_{22} = -H_{22} i_o \end{aligned} \tag{2.9}$$

Since input voltage v_{in} and output current i_o are AC by nature, it is clear that the blocking voltage (2.8) and the conducted current (2.9) for each switch will have both polarities/directions. Therefore, matrix converter must consist of bidirectional switches capable of blocking either voltage polarity and conducting current in either direction. This conclusion is general and it applies to all of the AC-AC matrix converters throughout this chapter.

All the switching states and the corresponding instantaneous values of the output voltage for the single-phase AC to single-phase AC matrix converter are given in Table 2.1. Time intervals t_0, t_1 and t_2 satisfy $t_0 + t_1 + t_2 = T_s$, where $T_s = 1/f_s$ is the switching interval.

Switches ON	v_o	time interval
S_{11}, S_{22}	v_{in}	t_1
S_{11}, S_{12}	0	t_0
S_{21}, S_{12}	$-v_{in}$	t_2
S_{21}, S_{22}	0	t_0

Table 2.1. Switching states of a single-phase AC to single-phase AC matrix converter

Average value of the output voltage $v_{o,av}$ during one switching interval T_s, can be found in a following way:

$$v_{o,av} = \frac{1}{T_s}(t_1 v_{in} - t_2 v_{in}) = \frac{t_1 - t_2}{T_s} v_{in} \tag{2.10}$$

When input voltage v_{in} (2.5) equals zero, equation (2.10) reveals near zero average output voltage, and its value depends on the duration of the switching interval T_s. The bounding region for the output voltage in the case of a single-phase AC to single-phase AC matrix converter is shown in Fig. 2.4, with the input voltage normalized $-1 \leq v_{in,n} \leq 1$.

The undertaken analysis, as well as the bounding region shown in Fig. 2.4 prove that single-phase AC to single-phase AC matrix converter is not capable of constructing the desired output voltage waveform. In other words, its structure imposes certain limitations, of which the frequency of the output voltage being integer multiple of the input voltage frequency is the most serious one.

Authors in [21] and [22] have come to similar conclusion, emphasizing the frequency step-up and output voltage step-down capabilities, beside the restriction of output fundamental voltage being phase-locked to the input voltage.

Employing the conservative approach in [19], one can obtain even more stringent restrictions upon the output voltage waveform, generated from a single-phase AC mains voltage. In the most general case, single-phase output voltage v_o is synthesized from a set of input voltages $v_{in,h}, h = 1, ..., n$. During each switching interval T_s, output voltage v_o is constructed by connecting the output to different input lines. Therefore, this fundamental inequality holds in each interval:

$$\min_{h=1,...,n} v_{in,h}(t) \leq v_o(t) \leq \max_{h=1,...,n} v_{in,h}(t) \tag{2.11}$$

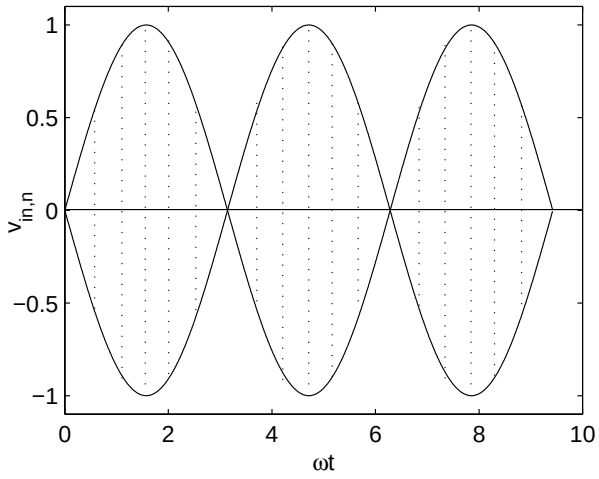

Fig. 2.4. Bounding region for the output voltage of a single-phase to single-phase matrix converter

Establishing the upper bound (UB_i) and the lower bound (LB_i) of the input voltages:

$$UB_i(t) = \max_{h=1,\ldots,n} v_{in,h}(t) \ , \ LB_i(t) = \min_{h=1,\ldots,n} v_{in,h}(t) \tag{2.12}$$

and the upper bound (UB_o) and the lower bound (LB_o) of the output voltage:

$$UB_o(t) = \max v_o(t) \ , \ LB_i(t) = \min v_o(t) \tag{2.13}$$

then the inequality (2.11) can be rewritten in the following form:

$$LB_i(t) \leq v_o(t) \leq UB_i(t) \tag{2.14}$$

When striving for equal performance of the matrix converter throughout the operating time, output voltage can be restricted to obey the following inequality:

$$\min_t UB_i(t) \geq \max_t UB_o(t) \tag{2.15}$$

According to the entries in Table 2.1, single-phase AC to single-phase AC matrix converter can apply both positive and negative input voltage across the load. Therefore, the set of input voltages actually consists of:

$$\begin{aligned} v_{i,1} &= v_{in} = V_{in,max} \sin(\omega_{in} t) \\ v_{i,2} &= -v_{in} = V_{in,max} \sin(\omega_{in} t - \pi) \end{aligned} \tag{2.16}$$

From Fig. 2.4 it follows that both upper and lower bounds of the set of input voltages are zero:

$$\min_t UB_i(t) = \max_t LB_i(t) = 0 \tag{2.17}$$

leading to zero output voltage $v_o = 0$, which is certainly a very conservative conclusion, but clearly shows the fundamental limitations imposed upon the single-phase AC to single-phase AC matrix converter with sinusoidal input voltage.

2.3 Two-phase AC to single-phase AC matrix converter

From the points learned in the previous section it becomes clear that single-phase AC-input matrix converter is not capable of creating the power flow dynamics, which is

necessary for driving a high fidelity audio system. The fundamental limitation are the regular zero-crossings of the input AC voltage, which asks for either some kind of energy storage or an alternative voltage source used during the periods of low input voltage. In order to preserve the ultimate advantage of the matrix converter with regard to avoiding any energy storage on the input side, it is interesting to reconsider designing a matrix converter with two input phases and their voltages having the same amplitudes and frequencies, but being out of phase for ϕ radians. It should be noted, however, that in the case where the second-phase voltage is derived from the first-phase voltage with some kind of power processing, this can be referred to as introducing some kind of energy storage for the periods of time with low input voltage on the first phase.

In Fig. 2.5 the phase lag of the input voltages is $\phi < \pi/2$. At the same figure both positive and negative polarities of input voltages are presented, since matrix converter should be capable of applying them to the load, for the sake of increased functionality. Maximums and minimums of the lower and upper bounds correspondingly are situated at the intersections of the different sinewaves. When $\phi \leq \pi/2$, minimum of the upper bound ($\min_t UB_i(t)$) and maximum of the lower bound ($\max_t LB_i(t)$) are established at the intersections of positive and negative sinewaves of input voltages (bold horizontal lines). When $\phi \geq \pi/2$, minimum of the upper bound ($\min_t UB_i(t)$) and maximum of the lower bound ($\max_t LB_i(t)$) are established at the intersections of positive sinewaves of input voltages and at the intersections of negative sinewaves of input voltages, correspondingly (dash-dotted horizontal lines). According to the phase angles marked in Fig. 2.5, the following applies when both voltages have the same amplitude:

$$\begin{aligned} \min_t UB_i(t) &= \begin{cases} \sin\frac{\phi}{2} & \text{, for } 0 \leq \phi \leq \frac{\pi}{2} \\ \sin\left(\frac{\phi}{2}+\pi\right) & \text{, for } \frac{\pi}{2} \leq \phi \leq \pi \end{cases} \\ \max_t LB_i(t) &= \begin{cases} -\sin\frac{\phi}{2} & \text{, for } 0 \leq \phi \leq \frac{\pi}{2} \\ -\sin\left(\frac{\phi}{2}+\pi\right) & \text{, for } \frac{\pi}{2} \leq \phi \leq \pi \end{cases} \end{aligned} \tag{2.18}$$

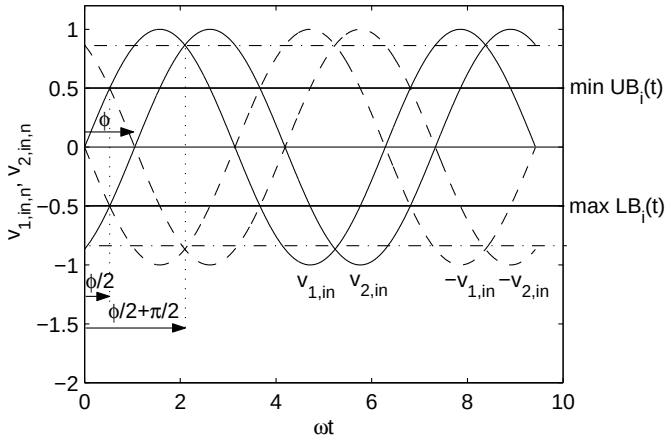

Fig. 2.5. Upper and lower bounds of the input voltages of a two-phase to single-phase matrix converter

It is rather straightforward to show that maximal available $\min_t UB_i(t)$ and minimal available $\max_t LB_i(t)$ will be reached as soon as the previously mentioned different bounds for $\phi \leq \pi/2$ and $\phi \geq \pi/2$ merge. This will happen for phase lag in excess of $\pi/2$ radians, that leads to symmetrical two-phase system. This case is shown in Fig. 2.6, and bounds are equal to:

$$\begin{aligned} &\min_t UB_i(t) = \sin\tfrac{\pi}{4} = \tfrac{\sqrt{2}}{2} = 0,707 \\ &\max_t LB_i(t) = -\sin\tfrac{\pi}{4} = -\tfrac{\sqrt{2}}{2} = -0,707 \end{aligned} \tag{2.19}$$

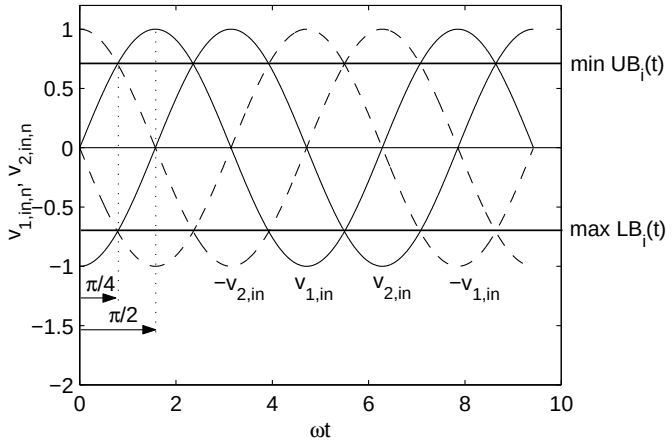

Fig. 2.6. Upper and lower bounds of the input voltages of a two-phase to single-phase matrix converter in the optimal case $\phi = \pi/2$

Therefore the optimal set of two AC input voltages should have the following form:

$$\begin{aligned} v_{1,in} &= V_{in,max}\sin(\omega_{in}t) \\ v_{2,in} &= V_{in,max}\sin(\omega_{in}t - \tfrac{\pi}{2}) \end{aligned} \tag{2.20}$$

Two-phase AC to single-phase AC matrix converter can be built in several ways, like:

- 2ph-AC to 1ph-AC matrix converter without a central tap,
- 2ph-AC to 1ph-AC matrix converter with fixed central tap, and
- 2ph-AC to 1ph-AC matrix converter with switched central tap

These will be subject of investigation in the next three sections.

2.3.1 2ph-AC to 1ph-AC matrix converter without a central tap

2ph-AC to 1ph-AC matrix converter without a central tap is shown in Fig. 2.7. As mentioned previously, all switches S_{ij} are bidirectional.

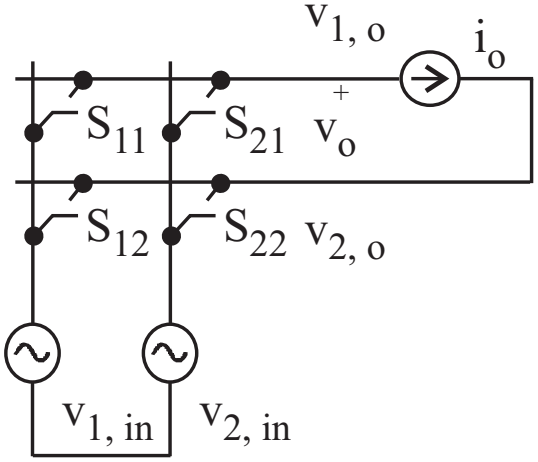

Fig. 2.7. 2ph-AC to 1ph-AC matrix converter without a central tap

2ph-AC to 1ph-AC matrix converter without a central tap is similar to the 1ph-AC to 1ph-AC matrix converter, where the two input lines are now subject to input voltage difference equal to:

$$v_{in} = v_{1,in} - v_{2,in} \tag{2.21}$$

and this difference is a sinewave with the same frequency and bigger amplitude than both the input voltages. So, there is still a voltage zero crossing problem.

Due to the aforementioned problem, it can be concluded that 2ph-AC to 1ph-AC matrix converter without a central tap can not offer any advantages over the 1ph-AC to 1ph-AC matrix converter, as it is clear from the switching states shown in Table 2.2 and the bounding region in Fig. 2.8.

Switches ON	v_o	time interval
S_{11}, S_{22}	$v_{1,in} - v_{2,in}$	t_1
S_{11}, S_{12}	0	t_0
S_{21}, S_{12}	$v_{2,in} - v_{1,in}$	t_2
S_{21}, S_{22}	0	t_0

Table 2.2. Switching states of a two-phase AC to single-phase AC matrix converter without a central tap

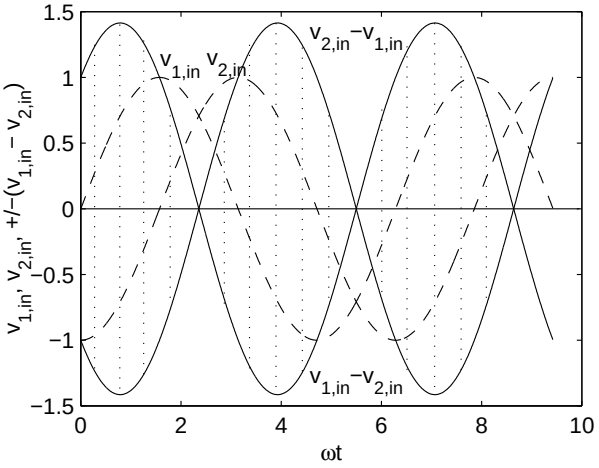

Fig. 2.8. Bounding region for the output voltage of a 2ph-AC to 1ph-AC matrix converter without a central tap

2.3.2 2ph-AC to 1ph-AC matrix converter with fixed central tap

2ph-AC to 1ph-AC matrix converter with fixed central tap is shown in Fig. 2.9. All switches S_{ij} are bidirectional.

2ph-AC to 1ph-AC matrix converter with fixed central tap offers less switching combinations, and their number is equal to the number of available switches in the first output line. The list of switching states is provided in Table 2.3.

Average output voltage can be found using the following equation:

$$v_{o,av} = \frac{1}{T_s}(t_1 v_{1,in} + t_2 v_{2,in}) = \frac{1}{T_s}\begin{bmatrix} t_1 & t_2 \end{bmatrix}\begin{bmatrix} v_{1,in} \\ v_{2,in} \end{bmatrix} \tag{2.22}$$

Using equation (2.22) one can conclude that when both input voltages are positive (for $\pi/2 < \omega t < \pi$) or negative (for $3\pi/2 < \omega t < 2\pi$), only positive or negative output

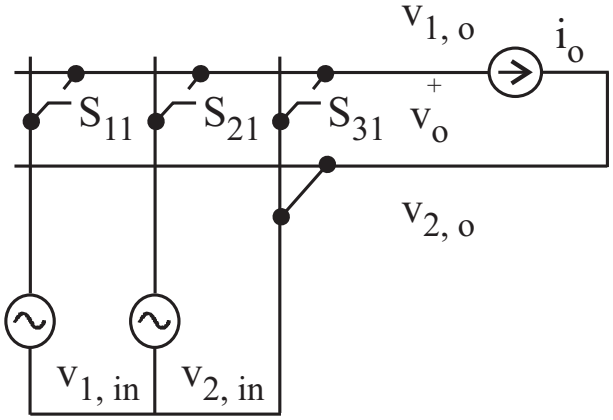

Fig. 2.9. 2ph-AC to 1ph-AC matrix converter with fixed central tap

Switches ON	v_o	time interval
S_{11}	$v_{1,in}$	t_1
S_{21}	$v_{2,in}$	t_2
S_{31}	0	t_0

Table 2.3. Switching states of a two-phase AC to single-phase AC matrix converter with fixed central tap

voltages can be reconstructed by the matrix converter, correspondingly. Reason for this is the incapability of the matrix converter to provide negative polarities of the input voltages, because of the lack of controllable switches in the second output line of the matrix converter. Bounding region for the output voltage is shown in Fig. 2.10.

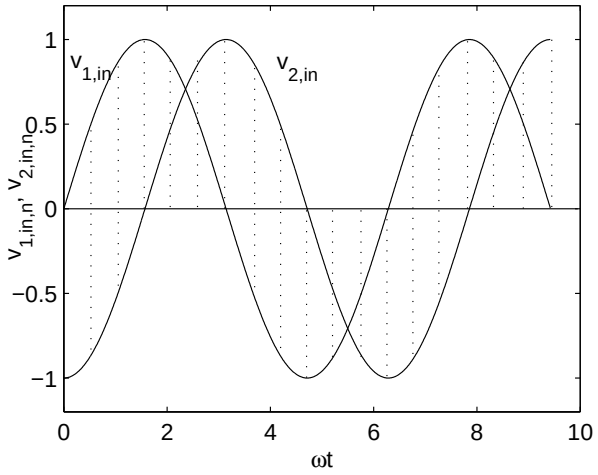

Fig. 2.10. Bounding region for the output voltage of a 2ph-AC to 1ph-AC matrix converter with fixed central tap

2.3.3 2ph-AC to 1ph-AC matrix converter with switched central tap

2ph-AC to 1ph-AC matrix converter with switched central tap is shown in Fig. 2.11. All switches S_{ij} are bidirectional.

2ph-AC to 1ph-AC matrix converter with switched central tap offers more switching combinations, on behalf of increased number of switches. The list of switching states is provided in Table 2.4.

Average output voltage $v_{o,av}$ can be found using the following equation:

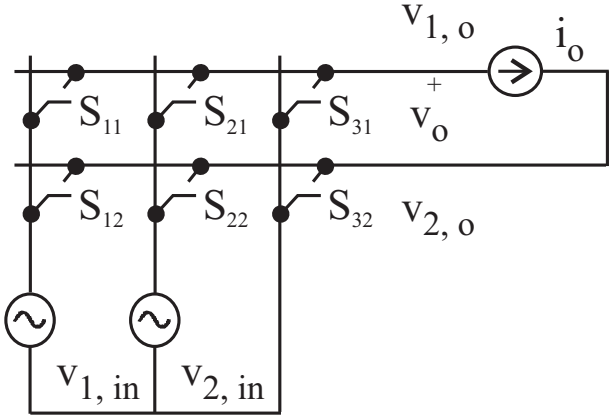

Fig. 2.11. 2ph-AC to 1ph-AC matrix converter with switched central tap

Switches ON	v_{out}	time interval
S_{11}, S_{12}	0	t_0
S_{11}, S_{22}	$v_{1,in} - v_{2,in}$	t_{1-2}
S_{11}, S_{32}	$v_{1,in}$	t_1
S_{21}, S_{12}	$v_{2,in} - v_{1,in}$	t_{2-1}
S_{21}, S_{22}	0	t_0
S_{21}, S_{32}	$v_{2,in}$	t_2
S_{31}, S_{12}	$-v_{1,in}$	t_{-1}
S_{31}, S_{22}	$-v_{2,in}$	t_{-2}
S_{31}, S_{32}	0	t_0

Table 2.4. Switching states of a two-phase AC to single-phase AC matrix converter with switched central tap

$$\begin{aligned} v_{o,av} &= \frac{1}{T_s}[v_{1,in}(t_1 - t_{-1} + t_{1-2} - t_{2-1}) + v_{2,in}(t_2 - t_{-2} + t_{2-1} - t_{1-2})] = \\ &= \frac{1}{T_s}\begin{bmatrix} t_1 - t_{-1} + t_{1-2} - t_{2-1} & t_2 - t_{-2} + t_{2-1} - t_{1-2} \end{bmatrix} \begin{bmatrix} v_{1,in} \\ v_{2,in} \end{bmatrix} \end{aligned} \tag{2.23}$$

All time intervals shown above form one switching interval T_s:

$$T_s = t_0 + t_1 + t_2 + t_{-1} + t_{-2} + t_{1-2} + t_{2-1} \tag{2.24}$$

When applying the switching strategy for the 2ph-AC to 1ph-AC matrix converter with switched central tap, seven different time intervals should be determined according to the desired output voltage. Two time intervals can be found using the equations (2.23) and (2.24), so there are five degrees of freedom left to the switching strategy. Therefore, a suitable strategy for determining single values for the time intervals in (2.23) should be established.

Complexity of the switching strategies can be reduced if some switching patterns and correspondingly some time intervals are avoided, like t_{1-2} and t_{2-1}. In this case the bounding region for the output voltage is shown in Fig. 2.12, providing enough margin for synthesizing high quality audio sound. The average value of the output voltage is given by the following equation:

$$v_{o,av} = \frac{1}{T_s}[v_{1,in}(t_1 - t_{-1}) + v_{2,in}(t_2 - t_{-2})] = \frac{1}{T_s}\begin{bmatrix} t_1 - t_{-1} & t_2 - t_{-2} \end{bmatrix} \begin{bmatrix} v_{1,in} \\ v_{2,in} \end{bmatrix} \tag{2.25}$$

and for the switching interval T_s:

$$T_s = t_0 + t_1 + t_2 + t_{-1} + t_{-2} \tag{2.26}$$

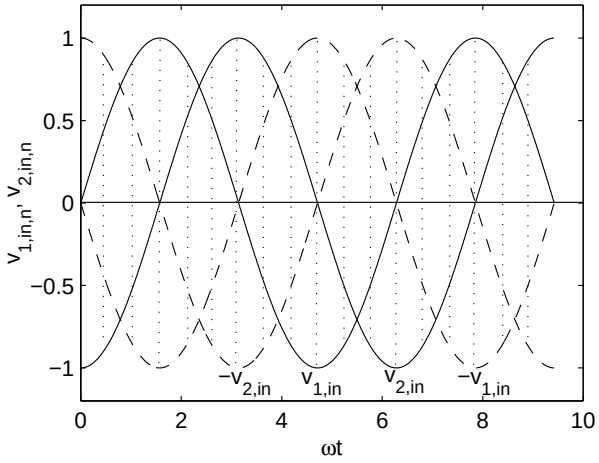

Fig. 2.12. Bounding region for the output voltage of a 2ph-AC to 1ph-AC matrix converter with switched central tap

As a conclusion, the simplest matrix converter which can be appropriately designed to provide uninterrupted power flow to single-phase load at audio frequencies has two input voltages and a switched central tap. This topology of a matrix converter and especially the corresponding control methods will be investigated in detail in the next few sections.

2.3.4 Switching strategies for 2ph-AC to 1ph-AC matrix converter with switched central tap

Strategy with reduced number of switchings

This switching strategy tries to reduce the number of switchings and therefore switching losses, by using the trial-and-error method to solve the equation (2.25). This method is employed by using two switching states, one of them being zero output voltage switching state for reconstructing the desired output voltage.

The procedure can be stated for the k-th switching interval as follows:

Try to solve one of the four equations:

$$v_{out}^k = \frac{t_j^k}{T_s} v_{j,in}^k \text{ where: } j = 1, 2, -1, -2 \tag{2.27}$$

with t_j^k satisfying the condition $0 < t_j^k \leq T_s$.
Then, the time interval t_0^k of the zero output voltage is:

$$t_0^k = T_s - t_j^k \tag{2.28}$$

Changing from the switching state that corresponds to the time interval t_j^k to the switching state for zero output voltage takes only one switching, since in each group of switching states in Table 2.4 there is one zero voltage switching pattern. This will cause only one switch to change state in the interior of the switching interval T_s, or two or three switchings during the whole interval T_s, depending on the switching state used in the previous interval and the one to be used in the following switching interval.

Changing between the time intervals t_j^k and t_0^k, which means connecting the load only to one of the positive or negative polarities of the input phase voltages is enough, since the envelope of the boundary region for this strategy corresponds to the one depicted in Fig. 2.12. Any other combination of three or more switching states does not offer any advantage, since the maximal value for the output voltage can not leave the bounding region.

Looking from the point of reduced switching losses, having only one switch change its state during the switching interval T_s looks certainly favorable. However, due to symmetry concerns and in order to reduce the input current and the output voltage ripple along with the associated HF harmonic content, it may be necessary to divide the zero voltage time interval t_0^k in two separated subintervals with same duration $t_0^k/2$ and apply the nonzero voltage time interval t_j^k in the middle.

This strategy with reduced number of switchings can be altered to include those switching states which produce the output voltages $v_{1,in}-v_{2,in}$ and $v_{2,in}-v_{1,in}$, and will be referred to as modified strategy with reduced number of switchings.

Diagonal switching strategy

There are two different approaches to diagonal switching: type A and type B, as shown in Fig. 2.13.

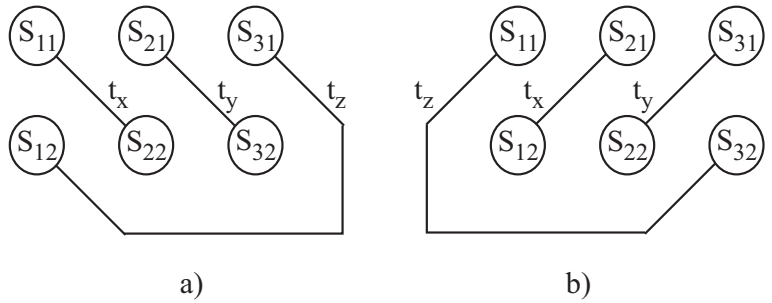

Fig. 2.13. Diagonal switching: a) type A and b) type B

In both cases only three different switching states are used, without any zero output voltage state. For simplicity, each of the three time intervals are indexed with x, y and z consecutively t_x, t_y and t_z, and their meaning is like the following:

- type A: $\mathbf{t_x} \rightarrow t_{1-2}$, $\mathbf{t_y} \rightarrow t_2$ and $\mathbf{t_z} \rightarrow t_{-1}$
- type B: $\mathbf{t_x} \rightarrow t_{2-1}$, $\mathbf{t_y} \rightarrow t_{-2}$ and $\mathbf{t_z} \rightarrow t_1$

The bounding region for the diagonal switching - type A is shown in Fig. 2.14 and it proves to be slightly bigger than the bounding region for the previous unmodified switching strategy with reduced number of switchings. However, number of switches changing state is increased to four in the interior of the switching interval T_s, or six in the whole T_s. This results in greater switching losses.

The average output voltage in the diagonal switching - type A, is calculated using the following equation:

$$v_{o,av} = \frac{1}{T_s}[v_{1,in}(t_x - t_z) + v_{2,in}(t_y - t_x)] \tag{2.29}$$

and the switching interval is:

$$T_s = t_x + t_y + t_z \tag{2.30}$$

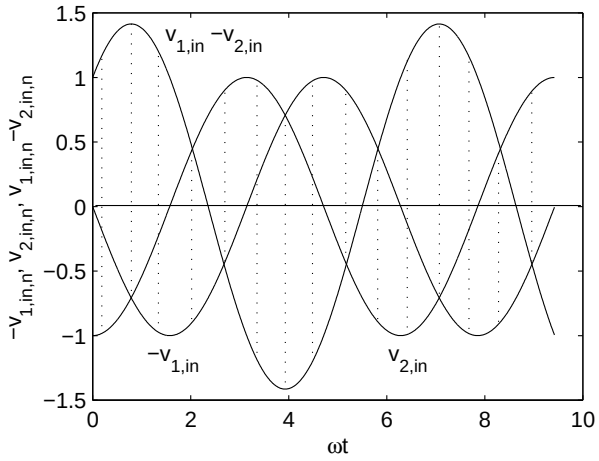

Fig. 2.14. Bounding region for the output voltage of a 2ph-AC to 1ph-AC matrix converter with switched central tap in case of diagonal switching strategy - type A

In the diagonal strategy there is only one degree of freedom, since two time intervals can be found from the equations (2.29) and (2.30).

By eliminating, for example, the time interval $t_z = T_s - t_x - t_y$, the average output voltage equation (2.29) becomes:

$$v_{o,av} = \frac{1}{T_s}[v_{1,in}(2t_x + t_y - T_s) + v_{2,in}(t_y - t_x)] \tag{2.31}$$

The procedure can be stated for the k-th switching interval as follows:

Start increasing the time interval t_x^k from 0 to T_s until time interval t_y^k is found that satisfies both the equation (2.31) and inequality $0 \leq t_y^k \leq T_s - t_x^k$, i.e.:

$$t_y^k = \frac{T_s v_{out,av}^k + (T_s - 2t_x^k)v_{1,in}^k + t_x^k v_{2,in}^k}{v_{1,in}^k + v_{2,in}^k} \in [0, T_s - t_x] \tag{2.32}$$

Then, time interval t_z^k is simply determined from:

$$t_3^k = T_s - t_1^k - t_2^k \tag{2.33}$$

The aforementioned procedure is also shown on the time diagram in Fig. 2.15, where (s) marks the point at which the solution (2.32) was found.

Phasor-based switching strategy

Space-vector modulator for 3ph-AC to 3ph-AC matrix converter is presented in [23], based on the indirect-transfer-function approach undertaken in [24]. Space-vector modulation principle in 3ph-to-3ph AC to AC matrix converters [25] offers higher voltage gain and less harmonic distortion in the input current and output voltage than other modulation techniques. However, implementation of these techniques to the 2ph-AC to 1ph-AC matrix converter with switched central tap is by no means straightforward. Similar approach can

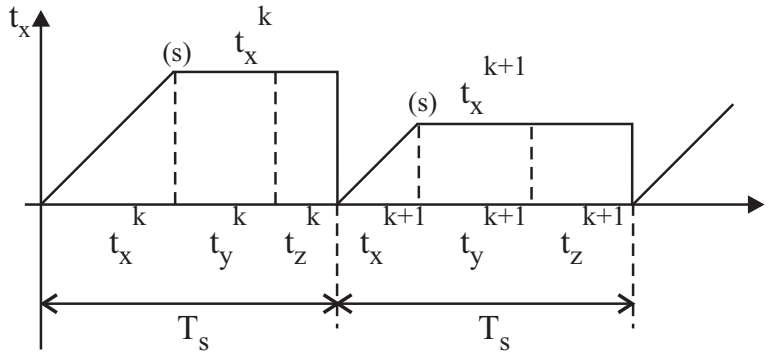

Fig. 2.15. Time diagram for the diagonal switching strategy - type A

be designed using input voltage complex phasors, which is here referred as to phasor-based switching strategy.

The set of input sinusoidal voltages with 90° phase shift and having the same angular frequency $\omega = \omega_{in}$ given with the equation (2.20), can be represented by using complex phasors $\overline{v}_{1,in}, \overline{v}_{2,in}$ rotating clockwise in the complex plain, as shown in Fig. 2.16.

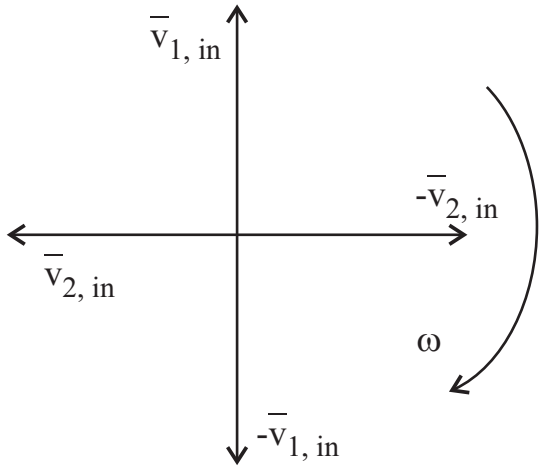

Fig. 2.16. Phasor diagram for input voltages

At the same time, the output voltage can have an arbitrary value due to the arbitrary shape of the time waveform and it is irrational to connect any frequency or phase angle to the latter. Assuming that this single value of the output voltage represents some distance from the center of the complex coordinate system, it can be located on a top of a radius vector named $\overline{v}_{out}$. As this vector is not moving, the same relation with the phasor quantities of the input voltages will be kept if this radius vector is moving in the counterclockwise direction with angular frequency ω and the phasors of the input voltages standing still. The situation is depicted in Fig. 2.17.

According to the polarity of the output voltage and the value of the angle ωt, one can put the output radius vector into corresponding sector, as shown in Table 2.5.

After the sector is found, from Table 2.6 the exact right (a) and the left (b) input phasors can be determined, being either $\pm\overline{v}_{1,in}$ or $\pm\overline{v}_{2,in}$. Combining this phasors during one switching interval T_s will reconstruct the desired average of the output voltage $v^k_{o,av}$:

$$v^k_{o,av} = \frac{t^k_a}{T_s} v^k_{a,in} + \frac{t^k_b}{T_s} v^k_{b,in} \tag{2.34}$$

where the time intervals t^k_a and t^k_b are found from the orthogonal projections $v^k_{a,out}$ and $v^k_{b,out}$ of the output phasor $\overline{v}_{out}$ onto the right and left input voltage vector correspondingly:

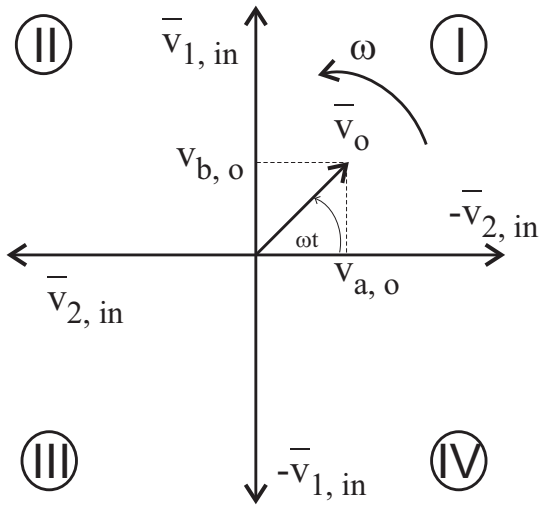

Fig. 2.17. Phasor diagram for input voltages and output voltage

Sector	$v_o^k > 0$	$v_o^k < 0$
I	$0 \leq \omega t^k \leq \pi/2$	$\pi \leq \omega t^k \leq 3\pi/2$
II	$\pi/2 \leq \omega t^k \leq \pi$	$3\pi/2 \leq \omega t^k \leq 2\pi$
III	$\pi \leq \omega t^k \leq 3\pi/2$	$0 \leq \omega t^k \leq \pi/2$
IV	$3\pi/2 \leq \omega t^k \leq 2\pi$	$\pi/2 \leq \omega t^k \leq \pi$

Table 2.5. Sectors and corresponding output voltage polarities and angles ωt^k

$$\begin{aligned} t_a^k &= \frac{v_{a,out}^k}{|v_{a,in}|} T_s \\ t_b^k &= \frac{v_{b,out}^k}{|v_{b,in}|} T_s \\ v_{a,out}^k &= |v_{out}^k \cos(\omega t^k)| \\ v_{b,out}^k &= |v_{out}^k \sin(\omega t^k)| \end{aligned} \tag{2.35}$$

It should be stressed that the angular frequency ω is continuously corrected by checking the moments when input voltages are passing through zero, i.e. determining the phase through Phase-Locked Loops (PLLs).

Sector	a	b
I	-2	1
II	1	2
III	2	-1
IV	-1	-2

Table 2.6. Sectors and corresponding sector's right and left vectors

When t_a^k and t_b^k are determined, zero voltage vector time interval is calculated by the following simple equation:

$$t_0^k = T_s - t_a^k - t_b^k \tag{2.36}$$

For the purpose of pulse symmetry, switching patterns for the right and the left vector should be appropriately divided on the either side of the central zero voltage vector, like shown in Fig. 2.18.

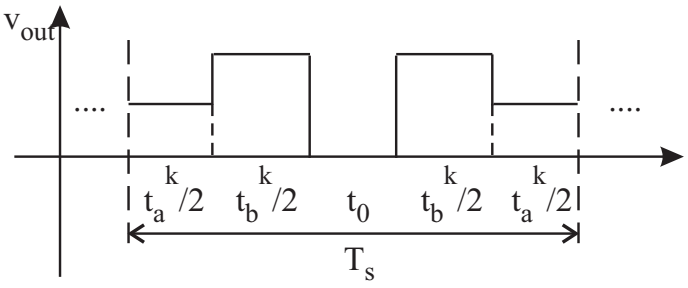

Fig. 2.18. Distribution of switching patterns' time intervals through one switching interval T_s

2.3.5 Obtaining another phase- lagging/leading voltage from AC-mains

In one of the previous sections it was concluded that matrix converter with a single AC output needs at least two phase-shifted voltages. Principles for obtaining another phase-shifted voltage, which lags or leads the mains voltage can be divided mainly in two groups:

- Passive methods: using only reactive elements - inductors and capacitors, and
- Active methods: using dedicated switching-mode converter topologies.

Passive methods for obtaining another phase-shifted voltage

Each of these methods is characterized by including some reactive elements in the circuit, which will cause some phase lag/lead in the circuit current. When this current is passed, for example, through a serial or parallel resistor, corresponding voltage drop lags/leads the input voltage from the AC mains.

However, adding some reactive elements between the AC mains voltage and the load can cause the output voltage to have slightly smaller amplitude than the input one, creating imbalances in the supply of the 2ph-AC to 1ph-AC matrix converter. The added reactive components tend to be bulky because of the required phase-shifts close to 90° at the frequency of the AC-mains voltage. Even more, this can make the phase-shifted voltage appear as a rather high impedance voltage source at higher frequencies, which results in the output voltage from the passive phase-shifter being especially sensitive to load variations.

In the following analysis a complex representation of the sinusoidal voltages and currents in steady-state will be used, in order to simplify the calculations. Let the input voltage v_s have the following time domain and complex notation representations:

$$\begin{aligned} v_s(t) &= \sqrt{2}V_s \sin(\omega t) \\ \underline{V_s} &= V_s \angle 0^\circ \end{aligned} \tag{2.37}$$

The following analysis of simple circuit combinations comprising of capacitor C, inductor L and resistive load R is provided just to illustrate some possibilities, although their feasibility is limited by the aforementioned problems of requiring large reactive components to achieve the needed phase-shift. As already mentioned, the load being in this case one of the input phases of a matrix converter is modelled as load resistance R to simplify the analysis, although some other representation like constant power sink might be more appropriate when dealing with switching-mode power converters.

- $L - R$ **series circuit:**

$$\underline{V_R} = R\underline{I_L} = \frac{R}{R + j\omega L}\underline{V_s} \tag{2.38}$$

and the corresponding amplitude and phase of the load voltage are:

$$\begin{aligned} |\underline{V_R}| &= \frac{R}{\sqrt{R^2+(\omega L)^2}}V_s \\ \angle\underline{V_R} &= -\arctan\frac{\omega L}{R} \end{aligned} \tag{2.39}$$

When $\omega L \gg R$, the load voltage amplitude and phase become:

$$\begin{aligned} |\underline{V_R}| &\approx \frac{R}{\omega L}V_s \\ \angle\underline{V_R} &\approx -90^\circ \end{aligned} \tag{2.40}$$

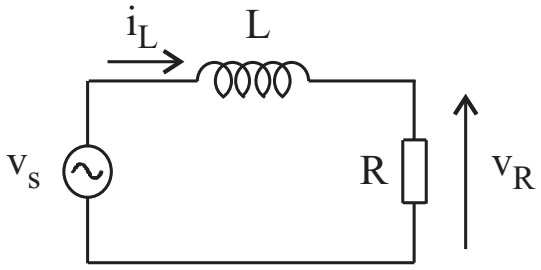

Fig. 2.19. $L-R$ series circuit

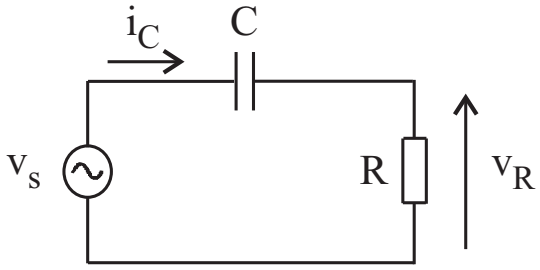

Fig. 2.20. $C-R$ series circuit

- $C-R$ **series circuit:**

$$\underline{V_R} = R\underline{I_C} = \frac{R}{R-j\frac{1}{\omega C}}\underline{V_s} \tag{2.41}$$

and the corresponding amplitude and phase of the load voltage are:

$$\begin{aligned} |\underline{V_R}| &= \frac{R}{\sqrt{R^2+\frac{1}{(\omega C)^2}}}V_s \\ \angle\underline{V_R} &= \arctan\frac{1}{\omega RC} \end{aligned} \tag{2.42}$$

When $1/\omega C \gg R$, the load voltage amplitude and phase become:

$$\begin{aligned} |\underline{V_R}| &\approx \omega RCV_s \\ \angle\underline{V_R} &\approx 90^\circ \end{aligned} \tag{2.43}$$

- $L-C-R$ **series circuit:**

$$\underline{V_R} = R\underline{I_L} = \frac{R}{R+j(\omega L-\frac{1}{\omega C})}\underline{V_s} \tag{2.44}$$

and the corresponding amplitude and phase of the load voltage are:

$$\begin{aligned} |\underline{V_R}| &= \frac{R}{\sqrt{R^2+(\omega L-\frac{1}{\omega C})^2}}V_s \\ \angle\underline{V_R} &= -\arctan\frac{\omega L-\frac{1}{\omega C}}{R} \end{aligned} \tag{2.45}$$

In case of resonance $\omega L = 1/\omega C$, the load voltage amplitude and phase become:

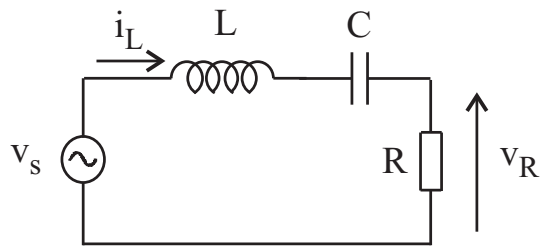

Fig. 2.21. $L-C-R$ series circuit

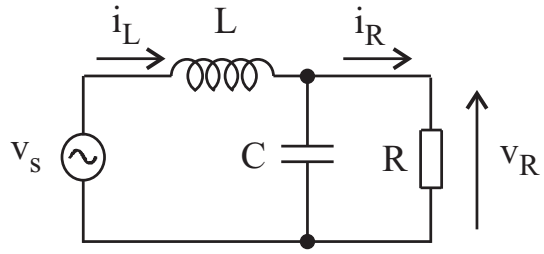

Fig. 2.22. $L-C-R$ parallel circuit

$$\begin{aligned} |\underline{V_R}| &\approx V_s \\ \angle \underline{V_R} &\approx 0^\circ \end{aligned} \tag{2.46}$$

When $L \to 0$ or $C \to \infty$ one obtains the $C-R$ or $L-R$ series circuit, which were explained in the previous two paragraphs.

- $L-C-R$ **parallel circuit:**

$$\underline{V_R} = R\underline{I_R} = \frac{R}{(R-\omega^2 RLC)+j(\omega L)}\underline{V_s} \tag{2.47}$$

and the corresponding amplitude and phase of the load voltage are:

$$\begin{aligned} |\underline{V_R}| &= \frac{R}{\sqrt{R^2(1-\omega^2 LC)^2+(\omega L)^2}}V_s \\ \angle \underline{V_R} &= -\arctan\frac{\omega L}{R(1-\omega^2 LC)} \end{aligned} \tag{2.48}$$

In case of resonance $\omega L = 1/\omega C$, the load voltage amplitude and phase become:

$$\begin{aligned} |\underline{V_R}| &\approx \frac{R}{\omega L}V_s \\ \angle \underline{V_R} &\approx -90^\circ \end{aligned} \tag{2.49}$$

It is clear that from all of the circuits presented, only the $L-C-R$ parallel circuit can offer -90° phase shift of the output voltage without requiring any huge values for the inductance L or the capacitance C. The only condition, which should be fulfilled is $\omega L = 1/\omega C$. However, in order to keep with some safety precautions, like not allowing the output voltage to raise significantly above the levels of the input voltage, one must insure that the resonant circuit will be appropriately loaded (small resistance R comparable to the impedance of the series inductor ωL). If this can not be guaranteed, or the resonant circuit is loaded in pulses, adding a fixed minimal resistance R_{min} in parallel to the load or even adding some silicon switches and passive nets in between can mitigate the voltage conditions on the load side.

The load in all of these examples was taken to be a constant value linear resistance R. Matrix converter connected at the power supply output can not be regarded as linear load, since it is by its switching nature hardly nonlinear. These conditions can be mitigated by employing some low-pass filtering on the matrix converter input, as well as employing advanced control methods for power factor correction. On the other hand, some silicon switching components can be added to the passive power supply used for obtaining another phase, which will, when suitably controlled, diminish the effects of the varying load. This represents an active method and it is subject of discussion in the following section.

Active methods for obtaining another phase-shifted voltage

Active methods refer to constructing another phase-shifted voltage by using some power converter topology. This actually corresponds to building a dedicated power supply, where the output voltage has the same form and frequency as the input AC-mains voltage, but the phase is shifted to around 90°.

The most obvious choice for building the aforementioned power supply is certainly the resonant converter. It is characterized with near sinusoidal output voltages (depending on the operation mode), low electromagnetic interference (EMI), less switching losses allowing for greater operating frequencies [26]. There are plenty of different approaches, and the parallel-loaded resonant converter is probably the most favorite, due to its unique features [27], [28]. Unlike the series loaded resonant converter (SLRC), parallel-loaded resonant converter (PLRC) [26]:

- appears as a voltage source and hence is better suited for multiple outlets,
- does not possess inherent short-circuit protection capability, which is a drawback, and
- can step up (boost) as well as step down (buck) the voltage, unlike the SLRC which can operate only as a step-down converter.

However, it seems very difficult to construct an AC-AC resonant converter that is capable of synthesizing a 90° phase-shifted sinusoidal voltage with frequency of 50 Hz, which is powered directly from the same AC-mains (although a 100 Hz voltage with lower amplitude can be easily reconstructed). Therefore, a DC power supply must be present in front of the resonant converter, in order to allow for some energy storage in its reactive components, as shown in Fig. 2.23. Parallel resonant LC circuit is tuned to angular frequency $\omega = 2\pi f = 1/\sqrt{LC}$, where $f = 50$ Hz is the frequency of the AC mains voltage, which clearly leads to rather bulky reactive components for the resonant tank. A dedicated control unit should be used to drive the switches in the resonant converter, in order to construct an output voltage that lags/leads the AC mains input-voltage for 90°. Since the switching frequency should be $f_s = f = 50$ Hz for getting output voltage with the same frequency, some control over the output voltage magnitude can be provided by using, for example, different duty ratios of the gate pulses [29].

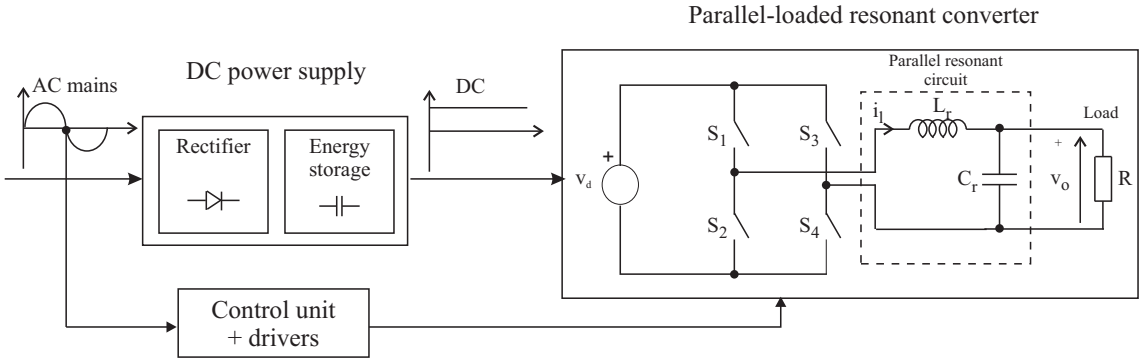

Fig. 2.23. Parallel-loaded resonant converter used for obtaining another voltage phase

Another active method as an alternative to the aforementioned PLRC comprises of Voltage Source Inverter (VSI) with the same DC input voltage like in the case of the PLRC, except for the fact that it is operated with much higher switching frequency in PWM mode to reconstruct another phase-shifted AC-voltage with AC-mains frequency.

However, the reviewed power converters for creating another phase-shifted voltage represent additional burden for the already complex matrix converter based SICAM and are

definitely not reconsidered as very appealing solution from either perspective. Therefore, the following sections will analyze thoroughly the passive parallel LC approach to creating another phase-shifted voltage for use in 2ph-AC to 1ph-AC matrix SICAM.

2.4 Matrix SICAM with *LC*-network

For further analysis, a two-phase switched-central-tap matrix converter (2ph SCT MC) with an LC passive network is chosen. For larger output voltage margin, an LC-network being resonant at the input voltage frequency ω_{in} is required, but other designs are possible too. Its scheme is shown in Fig. 2.24 and it will be referred to in the following paper as MC-based SICAM or matrix SICAM with an LC-network.

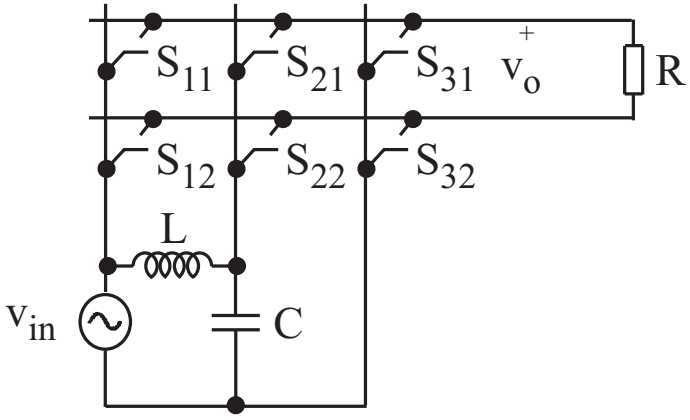

Fig. 2.24. MC-based SICAM with an LC-network

It was already shown in Section 2.3.3 that a matrix converter with switched central tap offers the greatest number of possible switching states and the output voltage margin is the largest, on behalf of more complex switching strategy and greater number of bidirectional switches. There are exactly three general equivalent topologies of the input voltage source v_{in} and the LC-network with respect to the load resistance R position: load resistance can be either in parallel with the input voltage source v_{in} i.e. unloading the LC-network - Fig. 2.25a or it can be in parallel with the capacitor C or the inductor L, and thus loading the LC-network - Fig. 2.25b,c.

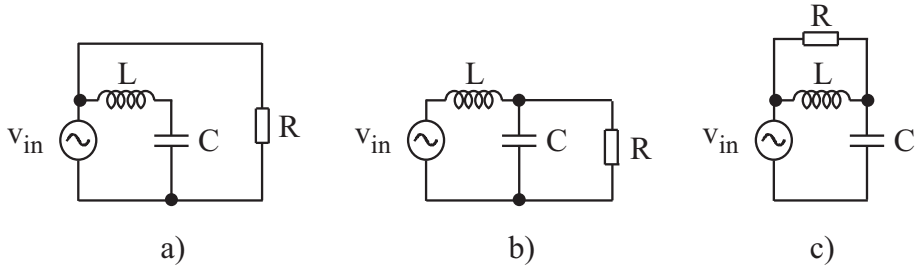

Fig. 2.25. General topologies: a) $v_{in} \| R$, b) $L \| R$ and c) $C \| R$

It is interesting to make a short analysis of the capacitor and inductor voltages in the case of unloaded LC-network using complex domain analysis and phasors at frequency $\omega = \omega_{in}$.

$$\underline{V_C} = \underline{Z_C} \cdot \underline{I_C} = \frac{1}{j\omega C} \frac{\underline{V_{in}}}{j\omega L + \frac{1}{j\omega C}} = -\frac{V_{in}}{\omega^2 LC - 1} = \frac{V_{in}}{\omega^2 LC - 1} \angle 180^\circ \tag{2.50}$$

$$\underline{V_L} = \underline{Z_L} \cdot \underline{I_L} = j\omega L \frac{\underline{V_{in}}}{j\omega L + \frac{1}{j\omega C}} = \frac{\omega^2 LCV_{in}}{\omega^2 LC - 1} \angle 0^\circ \tag{2.51}$$

Equations (2.50) and (2.51) show that both voltages are either in phase or with phase difference of π radians with the input voltage. During this state the load is connected across the input voltage source, and this connection can be used as long as the output voltage is high enough. However, when choosing the LC-network to be resonant at the input voltage frequency $\omega^2 = 1/LC$, which is surely desirable for providing better output voltage margin when switching as shown in Section 2.3.3, the amplitudes of the capacitor and the inductor voltages become theoretically infinite:

$$V_C = \frac{V_{in}}{\omega^2 LC - 1} \to \infty \tag{2.52}$$

$$V_L = \frac{\omega^2 LCV_{in}}{\omega^2 LC - 1} \to \infty \tag{2.53}$$

Following the latter analysis, it is concluded that switching states which lead to unloaded LC-network should be avoided, especially if the LC-network is made to be resonant or nearly resonant at the input voltage frequency. The revised list of switching states in the case of MC-based SICAM with an LC-network is given in Table 2.7.

Switches ON	v_{out}	time interval	status
S_{11}, S_{12}	0	t_0	unloaded LC - not allowed
S_{11}, S_{22}	$v_{1,in} - v_{2,in}$	t_{1-2}	$L\|R$
S_{11}, S_{32}	$v_{1,in}$	t_1	unloaded LC - not allowed
S_{21}, S_{12}	$v_{2,in} - v_{1,in}$	t_{2-1}	$L\|R$
S_{21}, S_{22}	0	t_0	unloaded LC - not allowed
S_{21}, S_{32}	$v_{2,in}$	t_2	$C\|R$
S_{31}, S_{12}	$-v_{1,in}$	t_{-1}	unloaded LC - not allowed
S_{31}, S_{22}	$-v_{2,in}$	t_{-2}	$C\|R$
S_{31}, S_{32}	0	t_0	unloaded LC - not allowed

Table 2.7. Switching states of an MC-based SICAM with LC-network

Except for restricting the MC-based SICAM in applying certain switching states, another approach can be employed. By applying an external permanent constant-valued resistor R_a in parallel with the capacitor C, like shown in Fig. 2.26, the resonant LC-network can be permanently loaded and reliable operation guarantied. However, this also leads to additional power losses in excess of:

$$P_{R_a} = \frac{V_{C,rms}^2}{Ra} \tag{2.54}$$

which can be very high, provided the resonant LC-network is properly loaded. Therefore, it is advantageous to use only the load impedance for loading the LC-network.

In the following sections it will be assumed that the load is completely represented by its resistance R. The influence of the output filter will be analyzed in Section 2.4.6.

2.4.1 Analysis of matrix SICAM switching between $L\|R$ and $C\|R$

After taking a closer look at Table 2.7, it appears that each of the allowed switching states either connects the load R in parallel with the inductor L, or in parallel with the capacitor C.

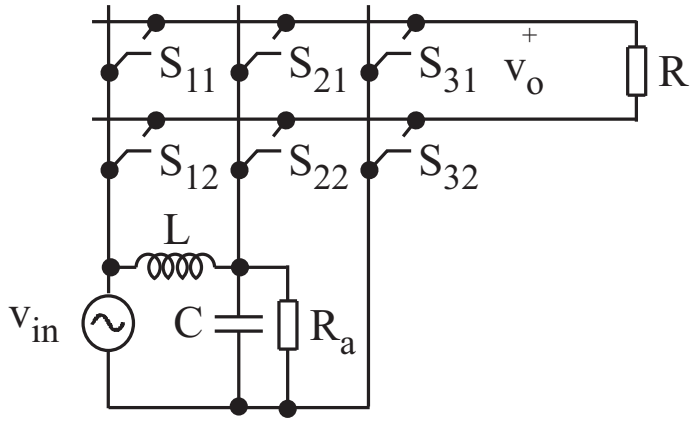

Fig. 2.26. Loading the LC-network with an additional resistor R_a

For the sake of simplicity, the capacitor C voltage will be determined for each of the two cases in steady-state, using complex domain phasors at input voltage frequency $\omega = \omega_{in}$. Then the inductor L voltage can be simply determined by subtracting the capacitor C voltage from the input voltage v_{in}.

- $C\|R$: Output voltage v_o is equal to the voltage across the capacitor C:

$$\underline{V_o} = \underline{V_C} \tag{2.55}$$

Capacitor C voltage phasor is:

$$\underline{V_C} = \frac{C\|R}{j\omega L + C\|R}\underline{V_{in}} = \frac{\frac{R\frac{1}{j\omega C}}{R+\frac{1}{j\omega C}}}{j\omega L + \frac{R\frac{1}{j\omega C}}{R+\frac{1}{j\omega C}}}V_{in} = \frac{R}{R(1-\omega^2 LC) + j\omega L}V_{in} \tag{2.56}$$

Capacitor voltage magnitude and phase are:

$$|V_C| = \frac{R}{\sqrt{R^2(1-\omega^2 LC)^2 + (\omega L)^2}}V_{in} \qquad \angle V_C = -\arctan\frac{\omega L}{R(1-\omega^2 LC)} \tag{2.57}$$

When a resonant LC-network is used, yielding $\omega^2 = 1/LC$, capacitor voltage magnitude and phase become:

$$|V_C| = \frac{R}{\omega L}V_{in} \qquad \angle V_C = -90^\circ \tag{2.58}$$

- $L\|R$: Output voltage v_o is equal to the voltage across the inductor L:

$$\underline{V_o} = \underline{V_L} = \underline{V_{in}} - \underline{V_C} \tag{2.59}$$

Capacitor C voltage phasor is:

$$\underline{V_C} = \frac{\frac{1}{j\omega C}}{L\|R + \frac{1}{j\omega C}}\underline{V_{in}} = \frac{\frac{1}{j\omega C}}{\frac{Rj\omega L}{R+j\omega L} + \frac{1}{j\omega C}}V_{in} = \frac{R + j\omega L}{R(1-\omega^2 LC) + j\omega L}V_{in} \tag{2.60}$$

Capacitor voltage magnitude and phase are:

$$|V_C| = \sqrt{\frac{R^2 + (\omega L)^2}{R^2(1-\omega^2 LC)^2 + (\omega L)^2}} \cdot V_{in} \qquad \angle V_C = \arctan\left(\frac{\omega L}{R} - \frac{\omega L}{R(1-\omega^2 LC)}\right)$$

(2.61)

When a resonant LC-network is used, leading to $\omega^2 = 1/LC$, capacitor voltage magnitude and phase become:

$$|V_C| = \sqrt{1 + \left(\frac{R}{\omega L}\right)^2} \cdot V_{in} \qquad \angle V_C = -\arctan\frac{R}{\omega L} \tag{2.62}$$

Voltages of both general topologies for the case $R/\omega L = 1$ and a resonant LC-network are shown in Fig. 2.27. Output voltages are marked with a bold line, and voltages for the topologies $C\|R$ and $L\|R$ are clearly marked with subscript indexes C and L. Input voltage is represented with $v_{1,in}$ and the capacitor voltage is the second phase voltage $v_{2,in}$.

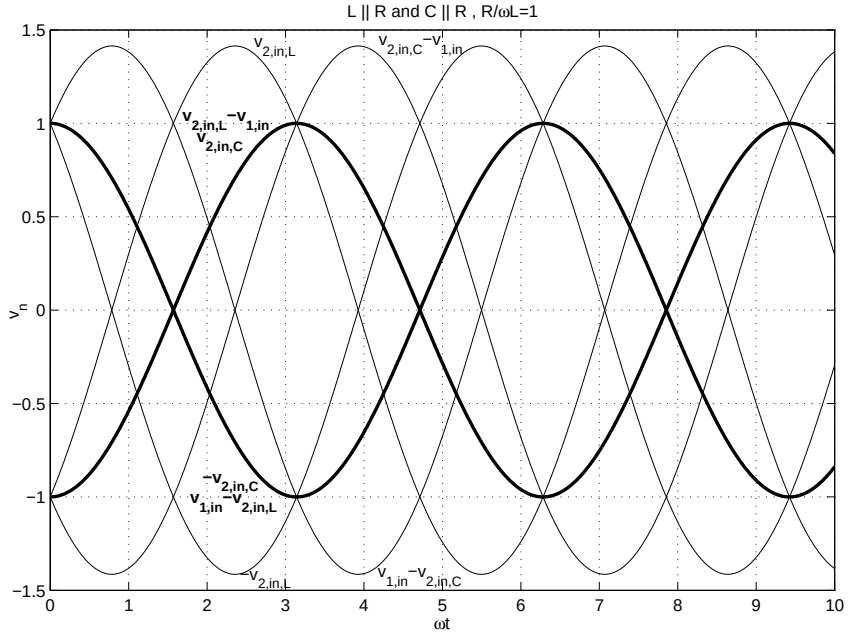

Fig. 2.27. Steady-state voltages in MC-based SICAM with resonant LC-network and $R/\omega L$=1

From Fig. 2.27 it is apparent that both steady-state output voltages for the cases $C\|R$ and $L\|R$ are the same. This leads to a conclusion that when the analysis is based only on the steady-state sinusoidal components of the output voltages without any intermediate switching between the two load arrangements $C\|R$ and $L\|R$, the performance of the MC-based SICAM using an LC-network is poor, with zero output voltage margin. This is result of the output voltages being in phase (or a phase difference being π) for both $C\|R$ and $L\|R$ general topologies.

This conclusion can be extended to non-resonant LC-networks, by observing the phase of the steady-state sinusoidal output voltages. When MC-based SICAM operates in $L\|R$ topology, the output voltage is:

$$\underline{V_{out}} = \underline{V_L} = \underline{V_C} - \underline{V_{in}} = \left[\frac{R + j\omega L}{R(1-\omega^2 LC) + j\omega L} - 1\right] V_{in} = \frac{R\omega^2 LC}{R(1-\omega^2 LC) + j\omega L} V_{in} \tag{2.63}$$

Output voltage phase in this case is:

$$\angle V_L = -\arctan\frac{\omega L}{R(1-\omega^2 LC)} \tag{2.64}$$

which is equal to the output voltage phase in (2.57) when $C\|R$.

For the purpose of audio band output voltage construction, it is required that the MC-based SICAM using an LC-network must switch between the two general topologies $C\|R$ and $L\|R$. At the switching instant, both the capacitor voltage v_C and the inductor current i_L cannot have a leap, so there is only a change in the waveform slope. In order to satisfy the initial conditions in terms of capacitor voltage and inductor current, exponential i.e. DC transient components are induced. These transient components in the capacitor voltage and inductor current fade out with a time constant which depends upon the capacitance C, inductance L and load resistance R, and they change the shape of the steady-state output voltage waveforms. Switching between $C\|R$ and $L\|R$ and back each half period of the input voltage in smartly determined instants, an envelope of the output voltage possible waveforms i.e. an output voltage margin can be created which never approaches zero. Fig. 2.28 presents only the approximate waveforms of the MC-based SICAM, when switching from $C\|R$ to $L\|R$ and back. Again the input voltage is represented with $v_{1,in}$ and the capacitor voltage is the second phase voltage $v_{2,in}$.

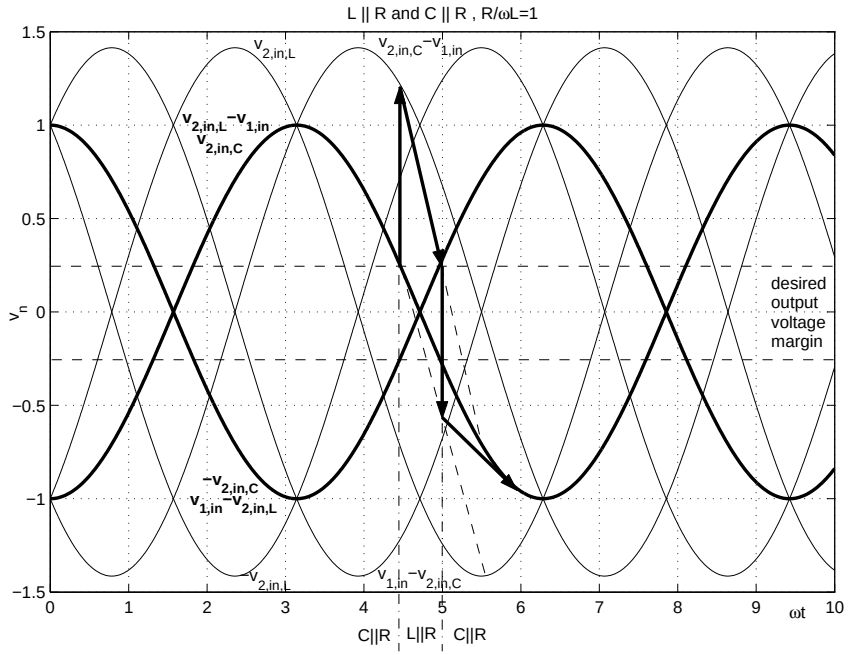

Fig. 2.28. Approximate transient voltages in MC-based SICAM with resonant LC-network and $R/\omega L$=1

Like shown in Fig. 2.28, switching from $C\|R$ topology to $L\|R$ topology occurs at the instant when the output voltage, which in case of $C\|R$ is equal to the capacitor voltage $v_o = v_{2,in,C}$, reaches the desired output voltage margin from outside. Then it is changed to $L\|R$ topology, and the output voltage equals the difference between the input voltage and the capacitor voltage $v_o = v_{2,in,L} - v_{1,in}$ (i.e. the inductor voltage). However, when switching it is clear that capacitor voltage $v_{2,in,C}$ at that instant will remain unchanged, so the output voltage will depart the sinusoid $v_{2,in,L} - v_{1,in}$ and follow the waveform $v_{2,in,C} - v_{1,in}$, like in the case of $C\|R$. As DC transient components start to fade out the output voltage tends to reach the steady-state inductor voltage waveform $v_o \to v_{2,in,L} - v_{1,in}$, again approaching the desired output voltage margin from outside. As soon as the output voltage reaches the margin, load is switched i.e. displaced from topology

$L\|R$ to $C\|R$ and the output voltage again becomes equal to the capacitor voltage instant value $v_o = v_C$, which is slightly bigger than the steady state one $v_{2,in,C}$ for the case $C\|R$ because of the DC transient components. This way the envelope of the output voltage can stay out of the desired output voltage margin, provided:

- Switching from $C\|R$ to $L\|R$ and back occurs at correct instants, when maximal output voltage is out of the desired output voltage margins, and
- Time constants of the LCR circuit, dominated by the capacitor value C, are long enough to support a DC transient component of the capacitor voltage during the whole of the time being in one of the general topologies.

It should be stressed, however, that the time diagram shown in Fig. 2.28 is only approximate one, since the induced DC transient components of the capacitor voltage will change the appearance of the capacitor voltage waveform, which will more or less differ from a sinusoidal one (depending on the time spent in each of the general topologies $C\|R$ and $L\|R$).

In the following subsections an exact time domain analysis of the two general topologies $C\|R$ and $L\|R$ will be undertaken.

2.4.2 Time domain analysis of the two load combinations

As mentioned before, operation of the matrix SICAM with LC-network is restricted to two load combinations - $C\|R$ and $L\|R$. The differential equations describing the capacitor voltage v_c in this two cases are solved in the Appendix A.1 and the results are given below:

- $C\|R$:

$$v_C(t) = A_C e^{t/\tau_1} + B_C e^{t/\tau_2} + D_C \sin\omega_{in}t + E_C \cos\omega_{in}t \tag{2.65}$$

where the constants in the solution are given with the following expressions:

$$\begin{aligned}
A_C &= \frac{-\frac{dv_{C0}}{dt} + v_{C0}s_2 - E_C s_1 + \omega_{in}D_C}{s_2 - s_1} \\
B_C &= \frac{\frac{dv_{C0}}{dt} - v_{C0}s_1 + E_C s_2 - \omega_{in}D_C}{s_2 - s_1} \\
D_C &= \frac{\omega_L^2(\omega_L^2 - \omega_{in}^2)}{(\omega_L^2 - \omega_{in}^2)^2 + (\omega_R\omega_{in})^2}V_{in} \\
E_C &= -\frac{\omega_R\omega_L^2\omega_{in}}{(\omega_L^2 - \omega_{in}^2)^2 + (\omega_R\omega_{in})^2}V_{in} \\
\omega_R &= \tfrac{1}{RC} \\
\omega_L &= \tfrac{1}{\sqrt{LC}}
\end{aligned} \tag{2.66}$$

and the time constants are:

$$\tau_{1,2} = \frac{2}{-\omega_R \pm \sqrt{\omega_R^2 - 4\omega_L^2}} \tag{2.67}$$

- $L\|R$:

$$v_C(t) = A_L e^{t/\tau_1} + B_L e^{t/\tau_2} + D_L \sin\omega_{in}t + E_L \cos\omega_{in}t \tag{2.68}$$

where the constants in the solution are given with the following expressions:

$$
\begin{aligned}
A_L &= \frac{-\frac{dv_{C0}}{dt} + v_{C0}s_2 - E_L s_1 + \omega_{in} D_L}{s_2 - s_1} \\
B_L &= \frac{\frac{dv_{C0}}{dt} - v_{C0}s_1 + E_L s_2 - \omega_{in} D_L}{s_2 - s_1} \\
D_L &= \frac{\omega_L^2(\omega_L^2 - \omega_{in}^2) + (\omega_R \omega_{in})^2}{(\omega_L^2 - \omega_{in}^2)^2 + (\omega_R \omega_{in})^2} V_{in} \\
E_L &= -\frac{\omega_R \omega_{in}^3}{(\omega_L^2 - \omega_{in}^2)^2 + (\omega_R \omega_{in})^2} V_{in} \\
\omega_R &= \tfrac{1}{RC} \\
\omega_L &= \tfrac{1}{\sqrt{LC}}
\end{aligned}
\tag{2.69}
$$

and the time constants are:

$$
\tau_{1,2} = \frac{2}{-\omega_R \pm \sqrt{\omega_R^2 - 4\omega_L^2}} \tag{2.70}
$$

From the solutions for the capacitor voltage in the two aforementioned load combinations it becomes clear that they include not only sinusoidal components created by the input voltage but also transient components, which depend on the initial conditions and decay with a time constant being a function of the values of the LC-network. It is due to the latter transient components that the waveforms of the supply voltages start to depart one from another and create enough output voltage margin.

2.4.3 HF switching of matrix SICAM for constructing the audio waveform

The analysis presented in the previous few sections handled about establishing the desired output voltage margin by using the appropriately timed switching between $C\|R$ and $L\|R$ topologies. The envelopes of the maximal and minimal output voltage coincide with the capacitor voltage $\pm v_C$, when load is connected across the capacitor C ($C\|R$) and $\pm(v_{in} - v_C)$, when load is connected across the inductor L ($L\|R$). The exact desired output voltage value is situated somewhere within the output voltage margin, so it can be reconstructed only by HF switching of the load between the positive and negative polarity of the capacitor C or inductor L voltage in a predetermined way.

All the possible topologies for the MC-based SICAM with loaded LC-network are shown in Fig. 2.29. When MC-based SICAM is in $C\|R$ topology, it resides in configuration $\boxed{2}$ for time period t_2 and in configuration $\boxed{\text{-}2}$ for time period t_{-2}. The output voltage average equals:

$$
v_{o,av} = \frac{1}{T_s}(t_2 v_c - t_{-2} v_c) = (d_2 - d_{-2}) v_c \tag{2.71}
$$

where $T_s = t_2 + t_{-2}$ represents the switching interval for $C\|R$, $d_2 = t_2/T_s$ and $d_{-2} = t_{-2}/T_s$ represent the duty cycles for configurations $\boxed{2}$ and $\boxed{\text{-}2}$, correspondingly.

When MC-based SICAM is in $L\|R$ topology, it resides in configuration $\boxed{\text{1-2}}$ for time period t_{1-2} and in configuration $\boxed{\text{2-1}}$ for time period t_{2-1}. The output voltage average equals:

$$
v_{o,av} = \frac{1}{T_s}[t_{1-2}(v_{in} - v_c) + t_{2-1}(v_c - v_{in})] = (d_{1-2} - d_{2-1})(v_{in} - v_c) \tag{2.72}
$$

where $T_s = t_{1-2} + t_{2-1}$ represents the switching interval for $L\|R$, $d_{1-2} = t_{1-2}/T_s$ and $d_{2-1} = t_{2-1}/T_s$ represent the duty cycles for configurations $\boxed{\text{1-2}}$ and $\boxed{\text{2-1}}$, correspondingly.

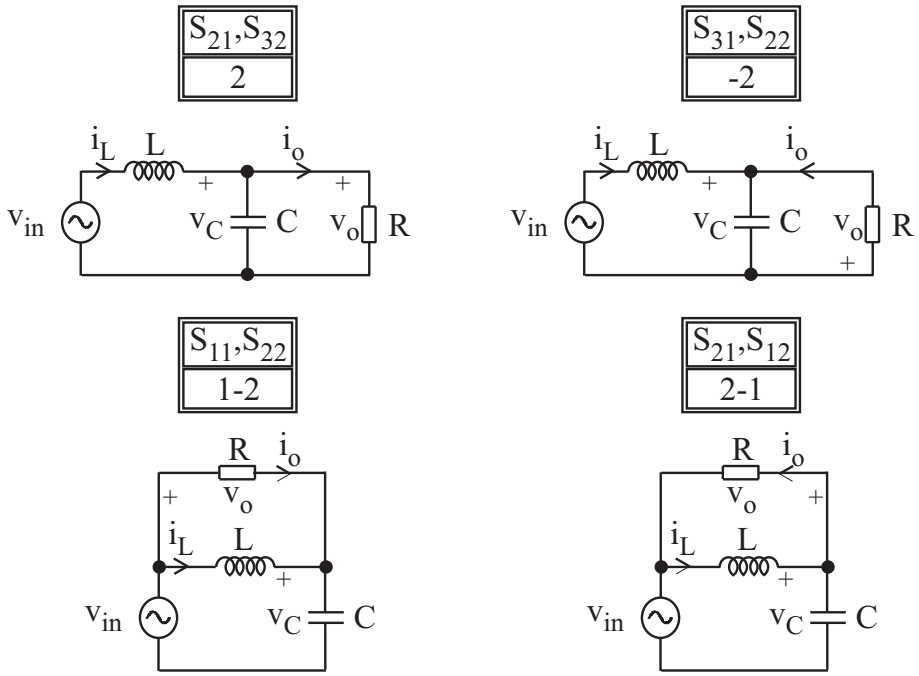

Fig. 2.29. Possible topologies for the MC-based SICAM with loaded LC-network

While equations (2.71) and (2.72) describe the dependence of the output voltage on the absolute values of the various duty cycles and the input and capacitor voltage, the small-signal behavior of the output voltage when perturbations are present in the circuit quantities can be found by using the state-space averaging approach described in Appendix A.2.

2.4.4 Design of matrix SICAM with resonant *LC*-network

Design of each matrix SICAM with LC-network starts with a list of audio performance specifications: maximum output power P_o, target audio bandwidth f_{audio} and load impedance $Z_o = R$. While the target audio bandwidth primarily affects the values of the output filter components and the switching frequency, the maximum output power and the load impedance affect the selection of the LC-network values.

The output power is defined as:

$$P_o = \frac{V_{o,rms}^2}{R} \tag{2.73}$$

which leads to the following expression for the maximal rms value of the output voltage:

$$V_{o,rms} = \sqrt{RP_o} \tag{2.74}$$

and assuming sinusoidal output voltage the following expression for its maximal peak value is obtained:

$$V_{o,pk} = \sqrt{2}V_{o,rms} = \sqrt{2RP_o} \tag{2.75}$$

Maximal peak value of the output voltage (2.74) is important, since it determines how big is the desired output voltage margin. Failing to preserve this margin will lead to reduced output power, while increasing the margin will lead to conservative approach with bulky components, like for example bulky capacitor C resulting in large time constants for the DC transient components, leading to inefficient and expensive design.

After an insight in the specifications and the way they affect the output voltage margins has been obtained, it can be proceeded to defining some important design parameters. The first one is the resonance coefficient a, which states how much the resonant frequency of the LC-network ω_L differs from the input voltage angular frequency $\omega_{in} = \omega$:

$$a = \frac{\omega_L}{\omega_{in}} = \frac{1}{\omega\sqrt{LC}} \tag{2.76}$$

The second one is the impedance ratio b, which determines how large is the inductor impedance ωL in comparison with the load impedance Z_o:

$$b = \frac{Z_o}{\omega_{in} L} = \frac{R}{\omega L} \tag{2.77}$$

Design parameters a and b can be brought into close connection with the circuit voltages and currents for different topologies and are therefore equivalent to using the capacitance C and inductance L. After design parameters are found which satisfy the specifications, they are used to determine the capacitance C and inductance L by the following relationships:

$$\begin{aligned} L &= \frac{R}{\omega b} \\ C &= \frac{1}{L\omega_L^2} = \frac{\omega}{R}\frac{b}{\omega_L^2} = \frac{b}{Ra^2\omega} \end{aligned} \tag{2.78}$$

In the Appendix A.1 where the time domain analysis of the two general topologies $C\|R$ and $L\|R$ is undertaken, it is shown that the DC transient components of the capacitor voltage have the same exponential elements $e^{s_{1,2}t}$, defined by:

$$s_{1,2} = \frac{-\omega_R \pm \sqrt{\omega_R^2 - 4\omega_L^2}}{2} = -\frac{\omega_R}{2}\left(1 \pm \sqrt{1 - 4\frac{\omega_L^2}{\omega_R^2}}\right) = -\frac{\omega_R}{2}\left(1 \pm \sqrt{1 - 4\frac{b^2}{a^2}}\right) \tag{2.79}$$

since:

$$\frac{\omega_L^2}{\omega_R^2} = \frac{R^2C^2}{LC} = \frac{R^2}{(\omega L)^2}\omega^2 LC = \frac{b^2}{a^2} \tag{2.80}$$

In all of the cases where $a^2 < 4b^2$, exponents $s_{1,2}$ become two complex conjugates, which means that DC component is actually consisting of a product of exponentially decaying waveform and a sine/cosine components:

$$A_i e^{s_1 t} + B_i e^{s_2 t} = A_i e^{-\frac{\omega_R}{2}t} e^{\sqrt{1 - 4\frac{b^2}{a^2}}t} + B_i e^{-\frac{\omega_R}{2}t} e^{-\sqrt{1 - 4\frac{b^2}{a^2}}t} \tag{2.81}$$

The real part of the exponents $s_{1,2}$ is:

$$s_0 = \frac{\omega_R}{2} = \frac{1}{2RC} \tag{2.82}$$

and the associated time constant τ_0 is:

$$\tau_0 = \frac{1}{s_0} = 2RC \tag{2.83}$$

One of the conditions for proper operation of an MC-based SICAM with an LC-network mentioned in Section 2.4.1 was having enough long LCR circuit time constants, which will support the DC transient components of capacitor voltage for a longer time. Now one can state it even more explicitly: the time constant τ_0 should be comparable to the time interval t_C spent in $C\|R$ and to the time interval t_L spent in $L\|R$. Approximately it should amount around a quarter of the input voltage period $20ms/4 = 5ms$, since the topology is switched four times during one period of input voltage. This can also limit the minimum allowed value of the capacitance C.

The other important design issue is the value of the reactive current. When using bulky inductors and capacitors in a SICAM for the higher power range, this may be an important limitation too. Averaging principle on the two general topologies can be used to determine the reactive component of the input current.

- $C\|R$: [2],[-2]
  Input current in time domain is given with the equation:

$$i_{in,C} = i_L = i_R + i_C = \frac{v_C}{R} + C\frac{dv_C}{dt} \tag{2.84}$$

  or when taking (A.21) into consideration:

$$\begin{aligned} i_{in,C} = {} & A_C\big(\frac{1}{R} + Cs_1\big)e^{s_1 t} + B_C\big(\frac{1}{R} + Cs_2\big)e^{s_2 t} + \\ & + \big(\frac{D_C}{R} - C\omega_{in}E_C\big)\sin\omega_{in}t + \big(\frac{E_C}{R} + C\omega_{in}D_C\big)\cos\omega_{in}t \end{aligned} \tag{2.85}$$

  where A_C, B_C, D_C and E_C are given by the relations (A.20) and (A.24). If the transient components and the sine component, which is in phase with the input voltage, are neglected, the following relation for the maximum value of the input current reactive component in $C\|R$ topology is obtained:

$$I_{in,C,react,max} = \frac{E_C}{R} + C\omega_{in}D_C \tag{2.86}$$

- $L\|R$: [1-2],[2-1]
  Input current in time domain is given with the equation:

$$i_{in,L} = i_C = C\frac{dv_C}{dt} \tag{2.87}$$

  or when taking (A.45) into consideration:

$$i_{in,L} = Cs_1A_Le^{s_1 t} + Cs_2B_Le^{s_2 t} - C\omega_{in}E_L\sin\omega_{in}t + C\omega_{in}D_L\cos\omega_{in}t \tag{2.88}$$

  where A_L, B_L, D_L and E_L are given by the relations (A.44) and (A.48). If the transient components and the sine component, which is in phase with the input voltage, are neglected, the following relation for the maximum value of the input current reactive component in $L\|R$ topology is obtained:

$$I_{in,L,react,max} = C\omega_{in}D_L \tag{2.89}$$

Now, an averaging on a time scale comparable to the input voltage period $T_{in} = 1/f_{in} = 20ms$ can be undertaken, leading to the following averaged maximum value of the input current reactive component:

$$I_{in,react,max} = d_C I_{in,C,react,max} + d_L I_{in,L,react,max} = d_C\big(\frac{E_C}{R} + C\omega_{in} D_C\big) + d_L C\omega_{in} D_L \quad (2.90)$$

where $d_C = 2t_C/T_{in}$ and $d_L = 2t_L/T_{in}$ represent the duty cycles in $C\|R$ and $L\|R$ topology, correspondingly.

It is interesting to determine the input current reactive component when the LC-network is designed to be resonant at input frequency. In that case D_C, E_C and D_L, E_L are determined by (A.25) and (A.49), correspondingly , which leads to:

$$I_{in,react,max} = \big[- d_C \frac{1}{R} \frac{\omega_{in}}{\omega_R} + d_L C\omega_{in}\big] V_{in,max} = (d_L - d_C) C\omega_{in} V_{in,max} \quad (2.91)$$

The result is rather surprising, since it shows that whenever the duty cycles d_C and d_L are chosen to satisfy $d_C = d_L$, there will be no input current reactive component. This conclusion does not suggest anything about when the switching should occur, but it is desired that one tries to commute the input current into another direction as soon as the input voltage changes the polarity, just to stay in phase with it.

2.4.5 Design example of matrix SICAM with resonant *LC*-network

This section will briefly show the approach to select the most important components of the matrix SICAM, based on given specifications.

The specifications in terms of target power range P_o, target audio bandwidth f_{audio} and load impedance $Z_o = R$ are given in Table 2.8.

P_{out}	500 W
f_{audio}	20 Hz - 20 kHz
R	8 Ω

Table 2.8. Design specifications for matrix SICAM with LC-network

From the target power range, the peak output voltage $V_{o,pk}$ can be easily calculated using (2.75):

$$V_{o,pk} = \sqrt{2RP_o} = \sqrt{2 \cdot 8 \cdot 500} \approx 90V \quad (2.92)$$

This peak output voltage will determine the desired output voltage margins ($\pm$90 V).

Since the target audio bandwidth is 20 Hz - 20 kHz, the corner frequency of the output filter can be set to, for example, $f_{cf} = 25$ kHz. Satisfactory output voltage ripple should be expected if the switching frequency is, for example, at least ten times higher than the output filter corner frequency $f_s = 10 f_{cf} = 250$ kHz and thus the switching interval is $T_s = 1/f_s = 4$ μs.

The goal in this section is to design matrix SICAM with a resonant LC-network, which will provide best performance in terms of output voltage margin. At the same time, the impedance of the inductor at the input frequency ω_{in} is chosen to be equal to the load impedance $Z_o = R$. Therefore both design parameters a and b in (2.76) and (2.77) are equal to 1, $a = b = 1$.

Choosing $a = b = 1$ leads to the following values for the inductance L and capacitance C, according to equations (2.78):

$$\begin{aligned} L &= \frac{R}{\omega b} = \frac{8}{2\pi 50 \cdot 1} = 25.5mH \\ C &= \frac{b}{Ra^2\omega} = \frac{1}{8 \cdot 1 \cdot 2\pi 50} = 398\mu F \end{aligned} \quad (2.93)$$

Selection of capacitor C value in (2.93) leads to the following time constant τ_0, as defined in (2.83):

$$\tau_0 = 2RC = 2 \cdot 8 \cdot 398 \cdot 10^{-6} = 6.4ms \tag{2.94}$$

The time constant $\tau_0 = 6.4$ ms is very close to a quarter of the input voltage period 20 ms/4=5 ms. Therefore, it is expected that there will be enough time for the DC transient components in the capacitor voltage to support the output voltage when switching between the two switching general topology and maintain the desired output voltage margin.

To avoid any reactive component in the input current one could choose $d_C = d_L = 0.5$, as stated in Section 2.4.4.

2.4.6 Influence of the output low-pass filter L_f, C_f

The scheme of the matrix SICAM with LC-network and output low-pass filter added between the converter and the load is shown in Fig. 2.30. Again, purely resistive load R is assumed.

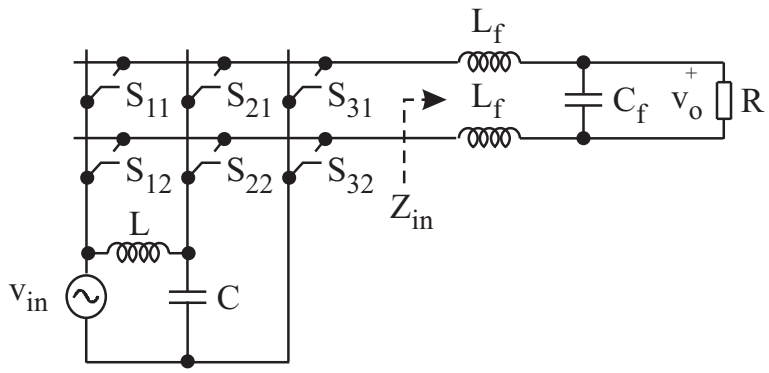

Fig. 2.30. Matrix SICAM with LC-network and output low-pass filter

Adding some inductance to the load on the output side of the matrix converter leads to commutation problems of the bidirectional switches. Actually, a basic problem of the matrix converter is the absence of a freewheeling path to the load. This is alleviated by using different switch commutation techniques based on input voltage polarity or load current direction measurement [30], as thoroughly explained in Section 6.2.1.

The biggest problem with introducing the output filter is its frequency dependent input impedance characteristic $Z_{in}(\omega)$:

$$Z_{in}(s) = \frac{R + sL_f + s^2RL_fC_f}{1 + sRC_f} \tag{2.95}$$

As it was mentioned earlier, the LC-network on the input side is made bulky and resonant at the input voltage frequency ω in order to store enough energy in it during the periods with low input voltage and maintain satisfactory output voltage margin. Unfortunately, such a big input filter must be properly loaded on the output side in order to avoid excessive voltage surge in the capacitor and inductor voltage and therefore excess reactive currents. Since the matrix converter has switching frequency which is significantly higher than the mains frequency, the output filter cannot be reconsidered as purely resistive anymore but is likely to be dominated by the reactance of the output filter inductor, as shown on the diagram in Fig. 2.31. This diagram is showed for low-pass

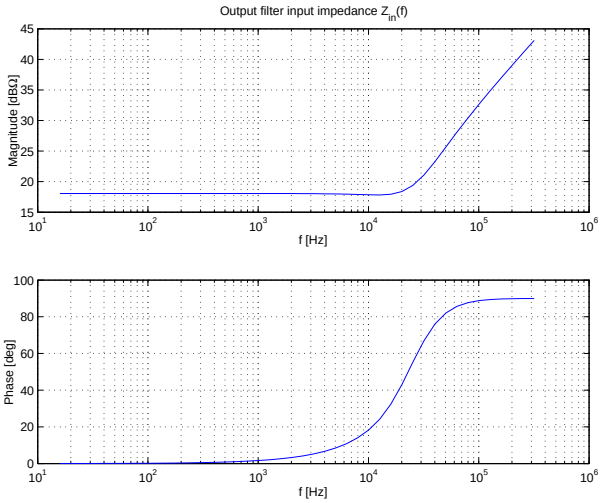

Fig. 2.31. Frequency characteristic of the input impedance $Z_{in}(f)$ of the output filter

output filter designed the same way like in [31] and the components of a second-order Butterworth filter with a load of $R = 8\ \Omega$ are $L_f = 36\ \mu H$ and $C_f = 560$ nF.

All these aforementioned drawbacks of the matrix SICAM with LC-network when output filter L_f, C_f is added for filtering the switching harmonics across the load are seriously hampering the application prospects of this non-isolated SICAM topology.

2.4.7 Open-loop control principles

Open-loop control techniques should provide means for varying the output voltage of the matrix SICAM with LC-network according to the audio reference signal in a simple and satisfactory way without closing the feedback loop. Switching strategies presented in Section 2.3.4 are computationally intensive and are better suited for digital implementation on a Digital Signal Processor (DSP) with lower switching frequencies of the matrix SICAM. For the high switching frequencies required by the audio applications the analogue implementation of the PWM modulator seems mush better suited.

The main challenge of the open-loop control techniques for matrix converters is the need to cope with the slowly varying input voltage, i.e. to provide high enough power supply rejection ratio (PSRR). This is usually accomplished by implementing input voltage feedforward to change correspondingly the conduction times of the bidirectional switches.

Without feedforward of the input voltage, the only possibility for improving performance is through closed-loop control and feedback of the output voltage, which will correct for the variations in the input voltage once their effects appear in the output voltage. From the closed-loop control principles, it is supposed that one-cycle nonlinear control techniques, like the one presented in [32] should provide best performance for the matrix SICAM. In the center of the one-cycle control principle is the integrator element, which integrates the applied voltage across the load and determines the switching instants based on the equality of that integral to the desired, reference value. Thus, these controllers can easily cope with the varying input voltage by providing equal Volt-seconds on a cycle-by-cycle basis despite of any disturbances. Their suitability for matrix SICAM is therefore result of the very good power supply rejection ratio (PSRR) and the fast response. However, these methods were not investigated herein.

In this section, two different PWM open-loop control principles will be investigated, which are appropriate for implementation in analog domain: amplitude modulation (AM) of the triangular carrier and Δ modulation technique.

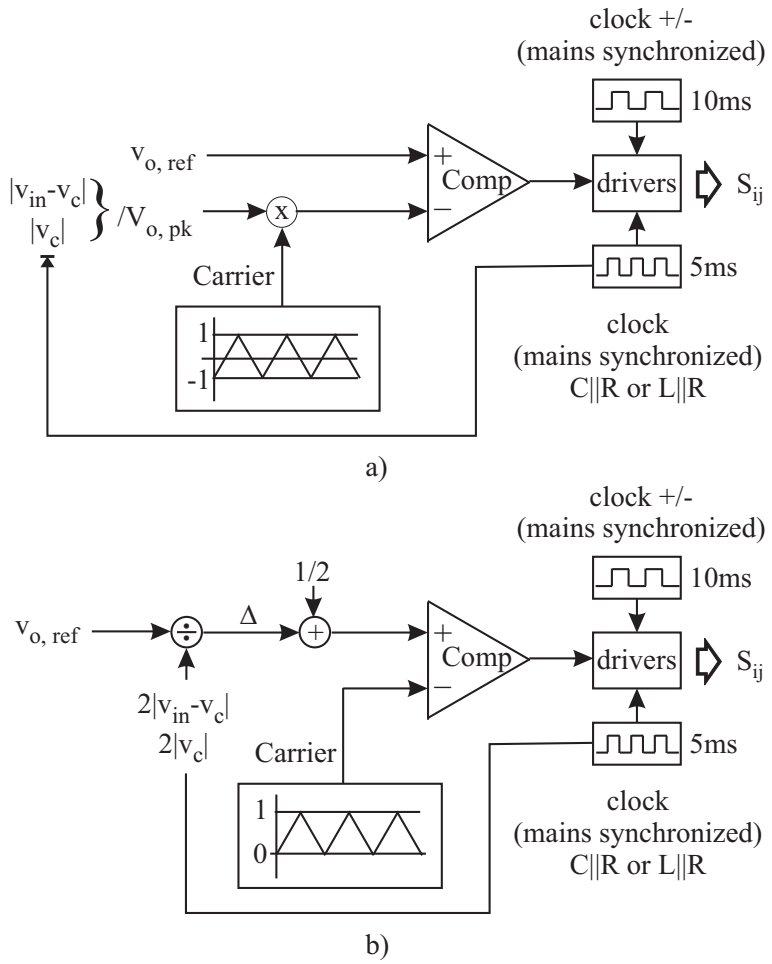

Fig. 2.32. Open-loop control principles: a) AM of the triangular carrier and b) Δ modulation technique

AM of the triangular carrier

Open-loop control technique called AM of the triangular carrier is shown in Fig. 2.32a. The idea behind it is to make an amplitude modulation (AM) of the fixed-frequency triangular carrier according to the available output voltage margin. Unfortunately, this necessitates use of multiplying element.

This technique can be developed in analytical way by noting that the average output voltage of the matrix SICAM is:

$$v_o = d_+V_+ + d_-V_- = (d_+ - d_-)V_+ = \Delta d V_+ \tag{2.96}$$

where d_+ is the duty cycle of the load being connected to the positive output voltage V_+ and d_- is the duty cycle of the load being connected to the negative output voltage V_-, with $d_+ + d_- = 1$ and $V_- = V_+$ being result of the specific way the matrix SICAM with LC-network is operated.

The difference of the positive and negative duty cycle is simply expressed as:

$$\Delta d = \frac{v_o}{V_+} = \frac{v_o}{kV_{om}} \tag{2.97}$$

where $V_{om} = V_{o,pk}$ represents the desired minimum output voltage margin, being in general equal to the peak output voltage $V_{o,pk}$. When the design of the matrix SICAM with LC-network has been done in a proper way which guarantees that the voltage of the rails is always bigger than the output voltage margin $V_+ \geq V_{om}$, then the coefficient $k \geq 1$. In

simple words equation (2.97) says that whenever there are variations in the input voltage of the matrix SICAM, the difference of the duty cycles d_+ and d_- must be inversely proportional to the coefficient k expressing the amount of that variation in respect to the output voltage margin V_{om}.

The duty cycles d_+ and d_- are determined by the intersections of the output voltage reference $v_{o,ref}$ and the triangular carrier with peak value xV_{crm} in the PWM modulator, as shown in Fig. 2.33, where x is the scaling factor which relationship to the coefficient k is to be determined.

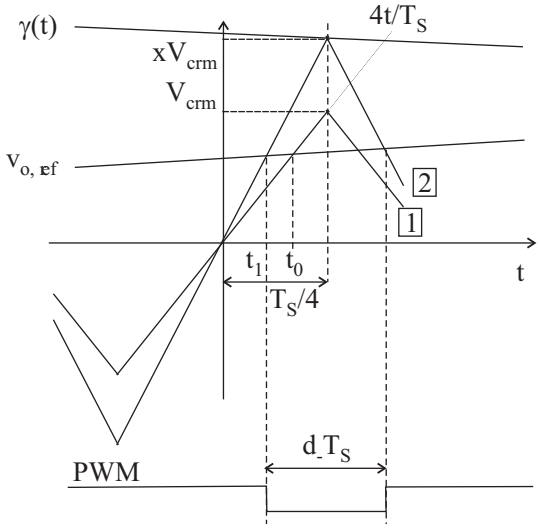

Fig. 2.33. AM of triangular carrier

The duty cycle with negative voltage d_- is:

$$d_- = \frac{T_s}{2} - \frac{v_{o,ref}}{2xV_{crm}} \tag{2.98}$$

which gives the following difference of the duty cycles:

$$\Delta d = d_+ - d_- = 1 - 2d_- = \frac{v_{o,ref}}{xV_{crm}} \tag{2.99}$$

By comparing (2.97) and (2.99), x can be expressed as:

$$x = \frac{V_{om}}{V_{crm}} \frac{v_{o,ref}}{v_o} k \tag{2.100}$$

The gain of the matrix SICAM with PWM modulator and externally created triangular carrier is:

$$k_a = \frac{v_o}{v_{o,ref}} = \frac{V_{om}}{V_{crm}} \tag{2.101}$$

which replaced in (2.100) leads to the following final value for the scaling factor x:

$$x = k \tag{2.102}$$

Equation (2.102) verifies the applicability of AM of the triangular carrier to cope with the variations of the input voltage, but also states that the peak value of the triangular

carrier xV_{crm} must be scaled exactly with the coefficient k in order to reject completely the variations of the input voltage.

In Fig. 2.32a, output voltage margin is following the capacitor voltage $\pm v_C$ when the matrix SICAM is in $C\|R$ topology, or the inductor voltage $\pm v_L = \pm(v_{in} - v_C)$ in $L\|R$ topology. The output voltage margin is normalized in respect to the peak output voltage needed $V_{o,pk}$ and this limit corresponds to the peak of the triangular carrier. Output voltage reference is restricted to $-1 < v_{o,ref} < 1$, or the input modulating signal is defined as sine wave consisting of a modulation index $0 < m < 1$ at input frequency f_m in the audio band. PWM pulses are obtained on the output of the comparator unit with the output voltage reference $v_{o,ref}$ and the AM triangular carrier xv_{cr} as inputs.

Driver block with its two clocks should be also considered as an important part of the modulation technique, since it redirects the driving pulses to the correct bidirectional switches. The $C\|R$,$L\|R$ clock with time base $t_C = t_L$ =5 ms guides the switching between different general topologies $C\|R$ and $L\|R$, according to which topology offers a greater possible output voltage. The $+/-$ clock with time base 10 ms tells the driver circuitry whether the voltage of the upper output rail compared to lower output rail is positive or negative, and this clock is synchronized with the changes in the $C\|R$,$L\|R$ clock output.

From a modulation standpoint, the multiplication of the triangular carrier with a factor $k = v_C/V_{o,pk}$ or $k = (v_{in} - v_C)/V_{o,pk}$ which pulsates with the input voltage frequency ω leads to different frequency spectrum of the PWM output signal in the AM of the triangular carrier technique. The most common method for analysis of PWM problems is the Double Fourier Series (DFS) presented in [33]. Indeed, when the frequency of the modulation wave ω_m and the frequency of the carrier ω_c are incommensurable, the only way to complete the analysis is to use a Fourier series from two independent parameters - DFS. However, the problem of the AM of the triangular carrier seems to be a multi-dimensional problem, since the amplitude of the triangular carrier is multiplied with a signal $\gamma(t)$ which contains harmonics of the input frequency ω_{in}. This signal is periodic and can be represented by Fourier series in a following way:

$$\gamma(t) = \frac{\alpha_0}{2} + \sum_{n=1}^{\infty} \left[\alpha_m \sin(n\omega_{in}t) + \beta_m \cos(n\omega_{in}t)\right] \tag{2.103}$$

where α_n, β_n are Fourier coefficients:

$$\begin{aligned} \alpha_n &= \tfrac{1}{\pi} \textstyle\int_0^{2\pi} \gamma(t) \cos(n\omega_{in}t) d(\omega_{in}t) \\ \beta_n &= \tfrac{1}{\pi} \textstyle\int_0^{2\pi} \gamma(t) \sin(n\omega_{in}t) d(\omega_{in}t) \end{aligned} \tag{2.104}$$

Although it seems logical to extend DFS to Multiple Fourier Series (MFS), the following simple analysis will show the introduction of harmonics at the input voltage frequency ω_{in} in the driving PWM signal by the AM of the triangular carrier technique. The analysis is based on the common triangular carrier waveforms and AM triangular carrier waveforms depicted in Fig. 2.33.

When common triangular carrier waveform $\boxed{1}$ is used, switching occurs at instant t_0 when the output voltage reference $v_{out,ref} = m \sin \omega_m t$ and triangular carrier waveform $\boxed{1}$ $4t/T_s$ are equal:

$$\frac{4t_o}{T_s} - m \sin \omega_m t_0 = 0 \tag{2.105}$$

where $T_s = 1/f_s = 2\pi/\omega_s$ is the switching interval.

By using DFS presented in [33], it can be concluded that in this case the PWM signal consists of the fundamental harmonic at the modulation frequency $m \cdot \omega_m$, switching harmonics $k \cdot \omega_s$ and intermodulation harmonics $\pm n \cdot \omega_m + k \cdot \omega_s$.

On the other hand, in the case of the AM of triangular carrier technique, condition for switching is fulfilled at instant t_1 where the output voltage reference $v_{o,ref} = m \sin \omega_m t$ equals the AM triangular carrier waveform $\boxed{2}$ $4t/T_s \cdot \gamma(t)$:

$$\frac{4t_1}{T_s}\gamma(t_1) - m \sin \omega_m t_1 = 0 \tag{2.106}$$

Dividing the equation (2.106) with $\gamma(t_1)$ the following expression is obtained:

$$\frac{4t_1}{T_s} - \frac{m \sin \omega_m t_1}{\gamma(t_1)} = 0 \tag{2.107}$$

Comparing equation (2.107) with equation (2.105) it is concluded that a simple sinusoidal output voltage reference $v_{o,ref} = m \sin \omega_m t$ in the case of constant triangular carrier has been replaced with a complex equivalent output voltage reference $v_{o,ref}^{eq} = m \sin \omega_m t/\gamma(t)$ in the case of AM. Therefore, harmonics and interharmonics associated with the input voltage frequency ω_{in} and its multiples should be expected in the PWM signal too.

The aforementioned PWM driving signal from the comparator section is subsequently used to drive the power stage with bidirectional switches, which applies the varying input voltage across the load. Due to the positive effect of the input voltage feedforward to amplitude modulate the triangular carrier, the fundamental of the input modulating signal will be precisely amplified despite of the variations in the input voltage, but the output voltage will also incorporate some of the harmonics and interharmonics of the feedforwarded input voltage found in the PWM driving signal, which are very unlikely to be completely cancelled by the varying input voltage.

Δ modulation technique

Open-loop control technique called Δ modulation is shown in Fig. 2.32b.

Assuming that during one switching interval T_s the input voltage does not change $V_+, V_- = const$, then by choosing both duty cycles to be equal $d_{+0} = d_{-0} = 0.5$ the average of the output voltage will equal zero. d_{+0}, d_{-0} are called zero output voltage duty cycles. Duty cycles d_+, d_- can be expressed using the zero output voltage duty cycles d_{+0}, d_{-0} and the Δ duty cycle in the following way:

$$\begin{aligned} d_+ &= d_{+0} + \Delta = 0.5 + \Delta \\ d_- &= d_{-0} - \Delta = 0.5 - \Delta \end{aligned} \tag{2.108}$$

Using the Δ duty cycle, the average output voltage (2.96) becomes:

$$v_o = [(d_{+0} + \Delta) - (d_{-0} - \Delta)]V_+ = 2\Delta V_+ \tag{2.109}$$

Equation (2.109) can be used to calculate the Δ duty cycle:

$$\Delta = \frac{v_o}{2V_+} = \frac{k_a v_{o,ref}}{2kV_{om}} = \frac{k_a}{2V_{om}} \cdot \frac{v_{o,ref}}{k} \tag{2.110}$$

As shown in (2.109), instead of modifying the triangular carrier this modulation technique modulates the reference output voltage $v_{o,ref}$ in synchronism with the variations in the

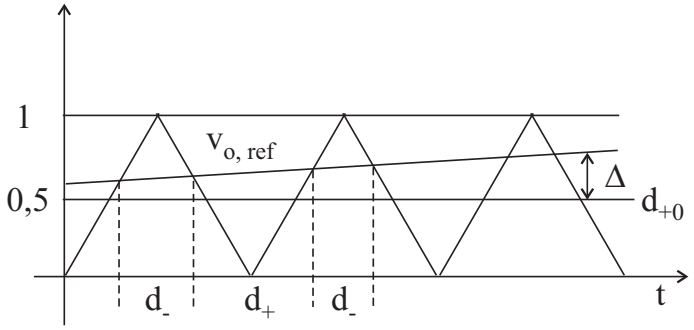

Fig. 2.34. Δ modulation control principle

input voltage, expressed through the coefficient k. This unfortunately necessitates use of division element. The waveforms of the proposed Δ modulation principle are shown in Fig. 2.34.

The role of the clocks in Fig. 2.32b is the same as in the previous AM of the triangular carrier.

2.4.8 Simulations of matrix SICAM with *LC*-network

In this section, the results from Orcad PSpice simulations of 500 W / 8 Ω matrix SICAM with resonant LC-network designed in Section 2.4.5 will be presented. All simulations were made with AM of the triangular carrier open-loop control technique.

First simulation was performed with purely resistive load R. Simulation was made with output voltage reference having a form of sine wave with modulation index m=0.8 at frequency 10 kHz. Time diagrams of the output voltage v_o, its Fast Fourier Transform (FFT) up to 1 MHz and up to 30 kHz are presented in Fig. 2.35, while the input voltage v_{in}, capacitor voltage v_C, inductor voltage v_L, input current i_{in}, capacitor current i_C, inductor current i_L and AM of triangular carrier are shown in Fig. 2.36.

Since in this case the matrix SICAM is driving purely resistive load, the envelope of the output voltage actually represents the output voltage margin. From the top diagram in Fig. 2.35 it can be concluded that this output voltage margin is sufficient for this power range, and maybe a slight readjustment of the time instants when configuration $L\|R$ is changed to $C\|R$ can even lead to its improvement. The switching harmonics present in the output voltage of the purely resistive load do not allow seeing the 10 kHz modulating wave, but it is apparent in the FFT of the output voltage at the bottom diagram in Fig. 2.35. On the middle FFT diagram of the output voltage in Fig. 2.35 the switching harmonics $n \cdot f_s$ and intermodulation sidebands $n \cdot f_s \pm k \cdot f_{ref}$ are clearly visible.

The same simulations with output filter instead of a resistive load R were also performed, giving quite different results. Again, the simulation was made with output reference in a form of a sine wave with modulation index m=0,8 at frequency 10 kHz. Time diagrams of the output voltage v_{out}, its FFT up to 1 MHz and up to 30 kHz are presented in figure 2.37, while the input voltage v_{in}, capacitor voltage v_C, inductor voltage v_L, input current i_{in}, capacitor current i_C, inductor current i_L and AM of triangular carrier are shown in figure 2.38.

From the FFT of the output voltage in Fig. 2.37 it can be seen that, like in the pure resistive load case, there are some DC and low frequency components in the output voltage, which are certainly not desired. These are regarded to the open loop modulation principles and the pitfalls of the AM of triangular carrier modulation technique. However, now the presence of a low-pass filter on the load side which has a significant input impedance at the switching frequency leads to relative unloading of the resonant LC-network and

thus to creation of immense capacitor voltage and inductor current shown in Fig. 2.38. This represents a huge stress for the reactive and switching components of the matrix SICAM, which totally disqualifies it from further practical examination. At the FFT of the output voltage at the middle diagram in Fig. 2.35 the switching harmonics $n \cdot f_s$ and intermodulation sidebands $n \cdot f_s \pm k \cdot f_{ref}$ are clearly visible too.

2.5 Conclusion about matrix SICAMs

Matrix converter capability for direct energy conversion without any reactive components (except for EMC filtering purposes) of the fixed input set of AC voltages to the output set of AC voltages with arbitrary amplitudes and frequencies looks highly appealing for use in SICAM. However, it was shown in previous sections that this conversion from a single-phase AC mains is neither straightforward, nor simple. The fundamental problem of unavoidable zero voltage crossings of the single sinusoidal input voltage asks for some kind of energy storage, which again promotes use of reactive components in the, otherwise, almost totally silicon-based matrix converter. It was found that the desired implementation of a matrix SICAM is the 2ph-AC to 1ph-AC matrix converter with switched central tap.

For implementing the proposed matrix SICAM another voltage must be provided that leads/lags the single-phase input voltage for certain phase angle, optimally 90°. It is suggested that this can be done by using a single-phase AC-mains and an *LC*-network being resonant or nearly resonant at the mains frequency to derive the other phase-shifted input voltage. In real implementations poorer performance should be expected, since the voltage in other phase will rarely be shifted for exactly 90° nor will have the same amplitude as the input one. This will cause lowering of the bound margin $|max_t LB_i(t)| - |min_t UB_i(t)|$ as defined in (2.12) and (2.18), and subsequently will decrease the allowed range for the output voltage reference.

Some other drawbacks are:

- Increased complexity of the power supply, which now must provide another phase-shifted voltage with certain strict requirements upon its phase lag and amplitude,
- Six bidirectional switches must be used in the proposed matrix converter topology, which increases the product cost, emphasizes the problem of the load current commutation [34] and adds significantly to the complexity of the converter and the gate drive circuitry, when compared to the other isolated and non-isolated solutions presented in the later chapters,
- Huge voltage and current stress on all reactive and switching components due to unloading of the resonant *LC*-network makes the matrix SICAM totally incompatible for use with output low-pass filter, and
- Matrix converters cannot provide galvanic isolation, which is a safety concern and requires galvanic isolation somewhere in the energy conversion chain if there is a chance for the user to physically access and touch the amplifier board or the loudspeaker.

Although the three phase matrix converter is very well investigated and is highly competitive to the common three phase rectifier-inverter schemes with DC-bus, the single-phase matrix converter is hampered by the bulky phase-shifting *LC*-network and does not seem to offer any distinct advantages when compared to the AC-mains connected, non-isolated SICAMs with Class D audio power amplifiers presented in the next chapter. However, the proposed single-phase matrix SICAM with *LC*-network is a very interesting AC-AC converter topology from a scientific point of view. Much of its limitations and

problems with the LC-network for providing another phase-shifted voltage were revealed in the previous chapters, together with a fairly simple analysis, as well as simple design approach and lots of design considerations. It was concluded that bulky high voltage rating capacitor C and bulky high current rating inductor L are needed to achieve a resonant LC circuit with satisfactory long DC transient components which will guarantee large enough output voltage margin. Open loop control issues were also addressed, by proposing simple PWM methods appropriate for analog implementation with externally created triangular carrier. Some simulation results have been shown to give a better insight into operation of the matrix SICAM with phase-shifting LC-network.

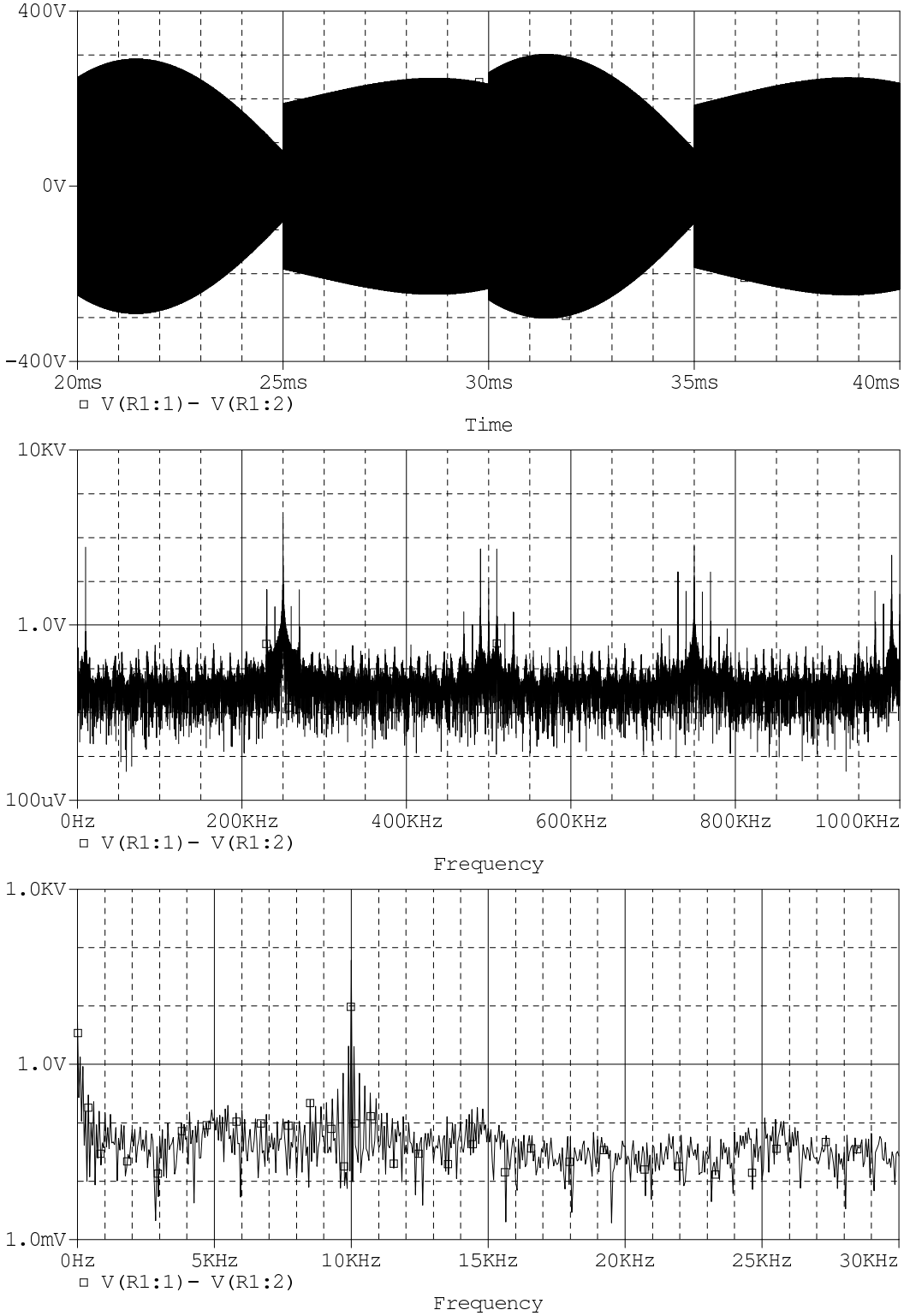

Fig. 2.35. Matrix SICAM with *LC*-network and purely resistive load (m=0,8, f=10 kHz) - Top: Output voltage v_{out}, Middle: FFT up to 1 MHz, Bottom: FFT up to 30 kHz

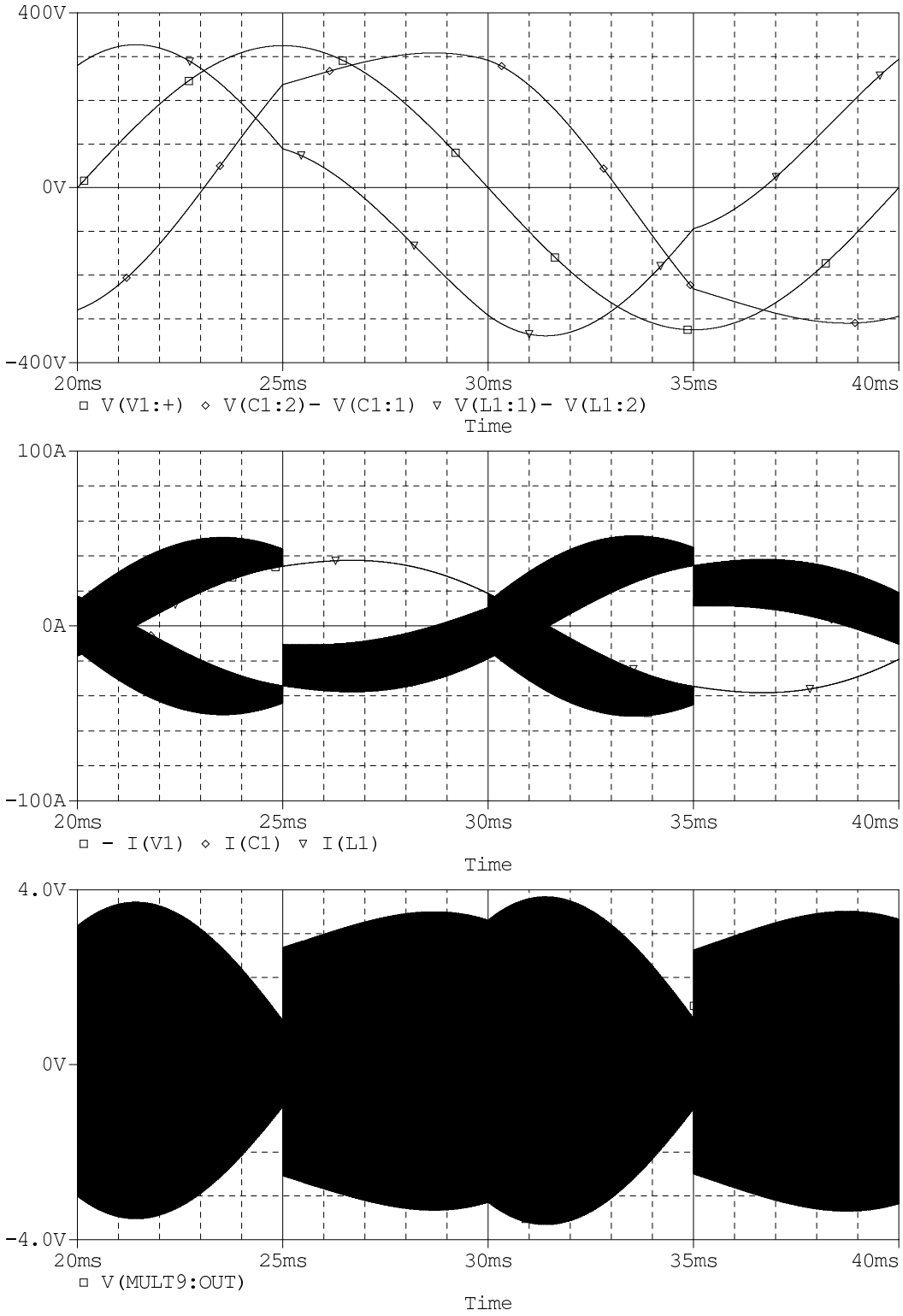

Fig. 2.36. Matrix SICAM with *LC*-network and purely resistive load (m=0,8, f=10 kHz) - Top: Input voltage v_{in}, capacitor voltage v_C and inductor voltage v_L, Middle: Input current i_{in}, capacitor current i_C and inductor current i_L, Bottom: AM of triangular carrier

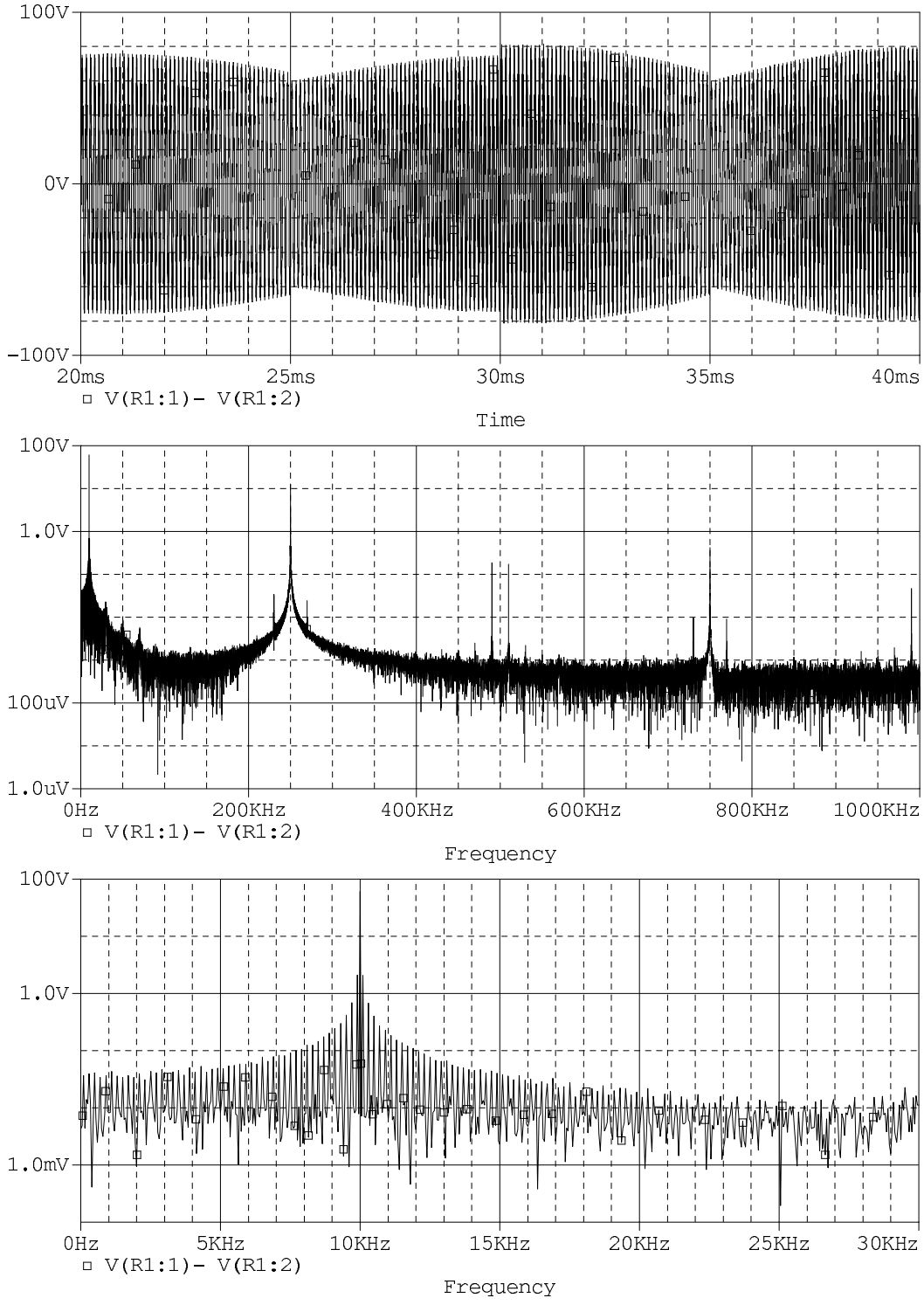

Fig. 2.37. MC-based SICAM using an *LC*-network (m=0,8, f=10 kHz) - Top: Output voltage v_{out}, Middle: FFT up to 1 MHz, Bottom: FFT up to 30 kHz

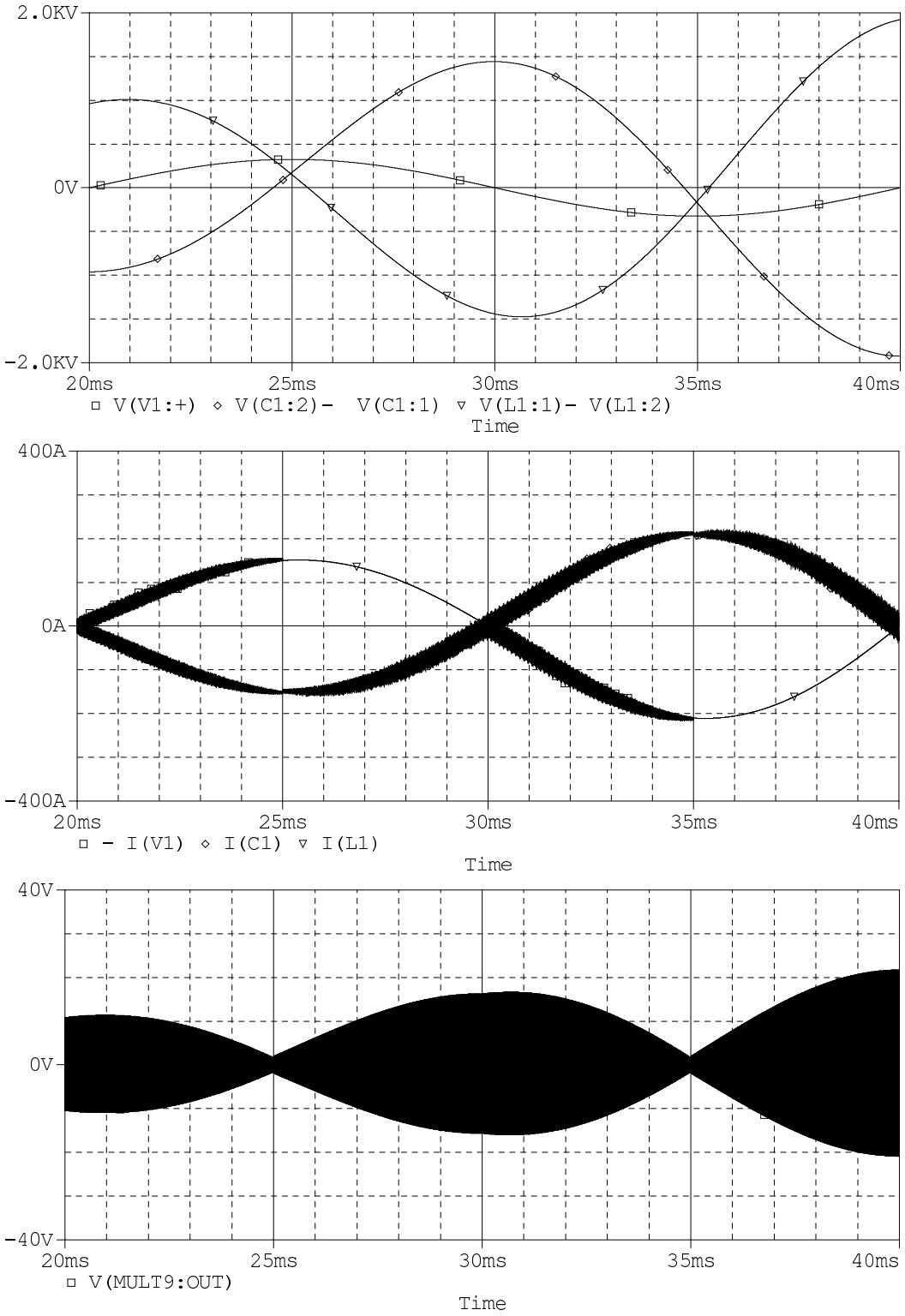

Fig. 2.38. MC-based SICAM using an *LC*-network (m=0,8, f=10 kHz) - Top: Input voltage v_{in}, capacitor voltage v_C and inductor voltage v_L, Middle: Input current i_{in}, capacitor current i_C and inductor current i_L, Bottom: AM of triangular carrier

3

AC-mains connected Class D audio power amplifiers as SICAMs

"If the only tool you have is a hammer, you will see every problem as a nail."

- Abraham Maslow

This chapter deals with non-isolated, directly AC-mains connected Class D audio power amplifiers. The main advantage of this approach, when compared to the previously presented matrix SICAMs, is that the necessary energy storage to cope with the regular zero crossings of the input AC-mains voltage can be very effectively provided with a DC-bus and unipolar electrolytic capacitors across it, combining very large charge capacity with a small case size. Since the energy conversion from the input AC-mains to the loudspeaker is performed as straightforward as possible, all these approaches can be referred to as non-isolated SICAMs.

3.1 Non-isolated DC power supply

Schematic of the non-isolated DC power supply with some of the voltage and current waveforms, as well as a block diagram of the rectifier are given in Fig. 3.1.

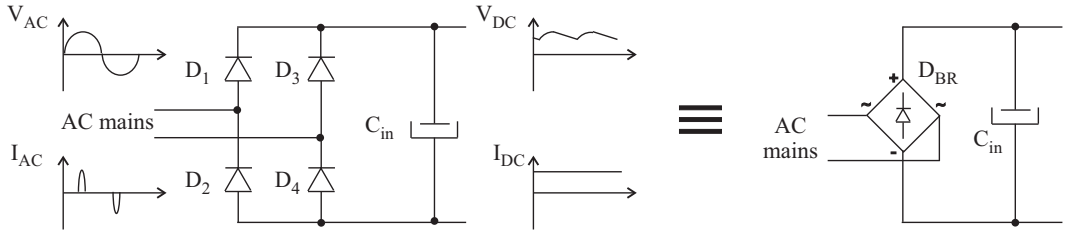

Fig. 3.1. Non-isolated DC power supply

Taking a closer look at the voltage and current waveforms in Fig. 3.1 it becomes apparent that the power flow from the AC-mains has a pulsative nature, in accordance to the charging of the energy storage capacitor around the peak of the mains voltage. On the other hand, power flow at the output is assumed nearly constant, which means that the mains rectifier is averaging the power drawn from the utility grid by the help of the storage capacitor following the rectifiers.

The development of design equations for the mains rectifier and input energy storage capacitor will follow the lines given in [35].

Mains rectifier and storage capacitor are supplying both the output power P_o and all the losses in the downstream electronics P_{loss}, giving a total input power P_{in} equal to:

$$P_{in} = P_o + P_{loss} = \frac{P_o}{\eta} \tag{3.1}$$

where η is the efficiency of the electrical energy conversion in SICAM.

The energy supplied from the AC mains during a full wave of the AC input voltage with duration $T_{ac} = 1/f_{ac}$ is:

$$W_{in} = P_{in}T_{ac} = \frac{P_{in}}{f_{ac}} \tag{3.2}$$

Energy from the mains W_{in} is delivered to the input energy storage capacitor C_{in} only during the time when the rectified AC mains voltage is higher that the energy storage capacitor voltage V_{Cin}. In the case of a full bridge rectifier, a half of the whole input energy $W_{in}/2$ is delivered each half-cycle of the AC mains voltage and in steady-state this leads to the following balance of energies:

$$\frac{W_{in}}{2} = \frac{1}{2}C_{in}(V_{Cin,pk}^2 - V_{Cin,min}^2) \tag{3.3}$$

where $V_{Cin,pk}$ and $V_{Cin,min}$ are the peak and minimum voltage of the input energy storage capacitor C_{in}, depicted in Fig. 3.2.

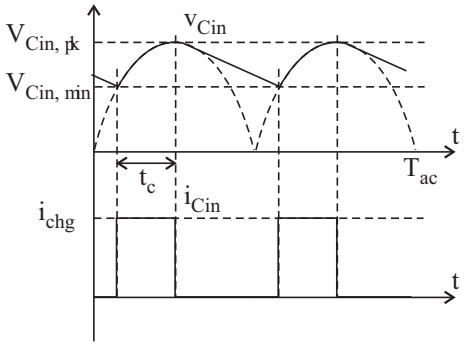

Fig. 3.2. Voltage and current of the input storage capacitor

Minimum value of the input energy storage capacitor $C_{in,min}$ to get the minimum voltage of $V_{Cin,min}$ is thus given with the following equation:

$$C_{in,min} = \frac{W_{in}}{V_{Cin,pk}^2 - V_{Cin,min}^2} \tag{3.4}$$

The minimum voltage of the input energy storage capacitor is very important quantity for the SICAM design, since all downstream switching electronics must be flexible enough to cope with the large variation of the input voltage, which usually comes down to having enough available duty cycle variation range to provide the desired output voltage. This problem is even more pronounced in isolated SICAMs, where the minimum input voltage determines the necessary transformer turns ratio n to achieve the desired peak output voltage with maximum duty cycle. When the AC mains voltage is at its maximum, the fixed turns ratio of the transformer will cause unnecessary high voltage stress on the output stage switches, if it is allowed for the minimum input voltage to be significantly lower than the peak input voltage.

The recharging time t_c is found by noting that:

$$V_{Cin,min} = V_{Cin,pk}\cos(2\pi f_{ac}t_c) \;\Rightarrow\; t_c = \frac{\arccos(\frac{V_{Cin,min}}{V_{Cin,pk}})}{2\pi f_{ac}} \tag{3.5}$$

By assuming constant charging current i_{chg} during the recharging period t_c, its magnitude is found to be:

$$i_{chg} = \frac{\Delta Q}{t_c} = \frac{C_{in}(V_{Cin,pk} - V_{Cin,min})}{t_c} \tag{3.6}$$

The RMS charging current flowing through the input energy storage capacitor is found by subtracting the DC component of the charging current from the total charging current:

$$I_{chg,rms} = \sqrt{I_{chg}^2 - I_{dc}^2} = \sqrt{i_{chg}^2 t_c \frac{2}{T_{ac}} - i_{chg}^2 \left(t_c \frac{2}{T_{ac}}\right)^2} \tag{3.7}$$

The total RMS input capacitor current is calculated by adding the discharging component of the capacitor current to the charging component from (3.7):

$$I_{Cin,rms} = \sqrt{I_{chg,rms}^2 + I_{dis,rms}^2} \tag{3.8}$$

Equations presented in this section are equally applicable to non-isolated and isolated SICAMs.

3.2 Class D audio power amplifier with non-isolated DC power supply

The simplest possibility for creating a non-isolated SICAM is to connect a Class D audio power amplifier to the non-isolated and unregulated DC power supply presented in Section 3.1. The resulting audio amplification topology with a full-bridge Class D audio power amplifier is depicted in Fig. 3.3.

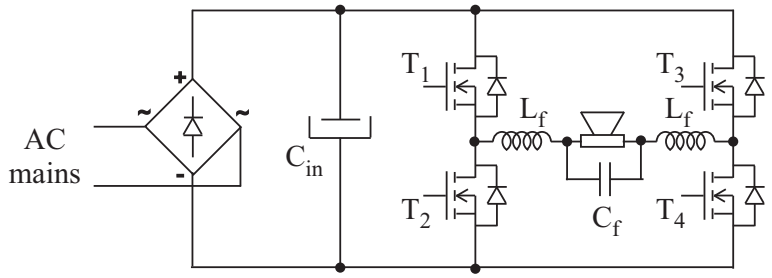

Fig. 3.3. Class D audio power amplifier with non-isolated DC power supply

The main features of the Class D audio power amplifier with non-isolated DC power supply are the compact structure of the resulting amplifier unit and the very efficient energy storage in the input capacitor C_{in}, being a result of the higher voltage on the DC-bus. This eventually increases the hold-up time in case of temporary input voltage dropout and leads also to much smaller form factors.

However, using higher input voltages to the Class D audio power amplifier includes some necessary compromises, like for example the need for high blocking voltage active devices (MOSFETs in Fig. 3.3), able to withstand the maximum rectified AC-mains voltage. The maximum blocking voltage $V_{BR,DSS}$ of the active device determines the minimum width of the lightly doped epitaxial layer (in the case of an N-type MOSFET it is usually referred to as N^-), increasing the on-resistance $R_{ds,on}$ of the device and the corresponding voltage drop during conduction. The exact relation of the on-resistance $R_{DS,on}$ to the maximum blocking voltage $V_{BR,DSS}$ depends primarily on the internal structure of the active device. For example, for the most of the conventional Power MOSFET structures

with predominantly planar gate structure and die surface area A_{die}, the relation for $R_{DS,on}$ is:

$$R_{DS,on} \sim \frac{(V_{BR,DSS})^{2.5}}{A_{die}} \tag{3.9}$$

while the same relation for 3-dimensional complimentary p/n column structure with trenches, like in the CoolMOS technology, shows significant improvement and is moving toward:

$$R_{DS,on} \sim \frac{(V_{BR,DSS})^{2}}{A_{die}} \tag{3.10}$$

This clearly shows the reduction of conduction losses, which can be achieved by moving to lower blocking voltage devices by decreasing the input voltage to the Class D audio power amplifier.

As a conclusion, the switching devices with higher blocking voltage in the directly mains-connected Class D audio power amplifier exhibit higher conduction losses due to the higher on-resistance $R_{DS,on}$, when compared to the low voltage devices used in the conventional Class D audio power amplifiers, which are selected only on the basis of the desired output power and the load impedance. As an example, a common load impedance of 8 Ω asks for peak voltage of $V_{o,pk} = 40$ V to produce output power of $P_o = 100$ W, while the voltage of the DC-bus on a European AC-mains 230 V/50 Hz is $V_{dc} = 325$ V nominal. In other words, the desired output voltage is produced with a very narrow variation of the duty cycle of the corresponding switching legs, which is maybe only an order of magnitude bigger than the dead (blanking) time inserted between the switching of the active devices in a single switching leg and therefore leads to excessive THD. The distortion of the Class D audio power amplifier with neglected effect of the output filter ripple current is given by the following equation [14]:

$$THD = \frac{\sqrt{\sum_{i=2}^{N_{max}} b_i^2}}{MV_{ps} - \frac{4t_{bl}V_{ps}}{\pi T_s}} \tag{3.11}$$

where M is the modulation index, V_{ps} is the power supply voltage, t_{bl} is the blanking (dead) time, $T_s = 1/f_s$ is the switching period, N_{max} is the number of distortion harmonics taken into account and the Fourier coefficients a_n, b_n of the resulting distortion waveform are given by:

$$\begin{aligned} a_0 &= 0 \\ a_n &= 0 \\ b_n &= -2\frac{t_{bl}}{T_s}V_{ps}\frac{sin(n\frac{\pi}{2})}{n\frac{\pi}{2}} = 2\frac{t_{bl}}{T_s}V_{ps}\frac{(-1)^n}{(2n-1)\frac{\pi}{2}} \end{aligned} \tag{3.12}$$

The above THD equations assume ideal power stage, where the audio distortion is created only during the short blanking time intervals. However, in a real power stage additional audio distortion is created as a result of the nonlinear characteristics of the antiparallel freewheeling diodes, when the load current diverts from the MOSFET channel with on-resistance $R_{DS,on}$ to its body diode because of the higher voltage drop in the channel.

This effect is likely to be even more pronounced in directly mains-connected Class D audio power amplifiers, where MOSFETs are required to have blocking voltage somewhat higher than the rectified mains voltage and thus higher on-resistance.

It can be seen from equations (3.11) and (3.12) that THD of the Class D audio power amplifier increases with the increasing power supply voltage V_{ps} which proves the fact that the directly mains-interfaced Class D audio power amplifier will be worse performer. This setback is even more pronounced because of the need to increase the blanking time t_{bl}, because at such a high input voltages any shoot-through can lead to large and dangerous short-circuit currents and it certainly takes more time for the drain-source voltage V_{DS} to completely slew to the final value.

Since the Class D audio amplification technology has been thoroughly explained elsewhere [14], the discussion about non-isolated SICAMs in this chapter will focus on other aspects, like alleviating the problems with the high voltage on the DC-bus in the straightforward implementation or integrating an extra PFC capability in the conventional Class D audio power amplifier.

3.3 Class D audio power amplifier with step-down PFC front-end

One of the ways to alleviate the aforementioned problems with the directly mains-connected Class D audio power amplifiers is to decrease the input voltage to the Class D audio power amplifier by introducing a step-down PFC front-end, as shown in Fig. 3.4.

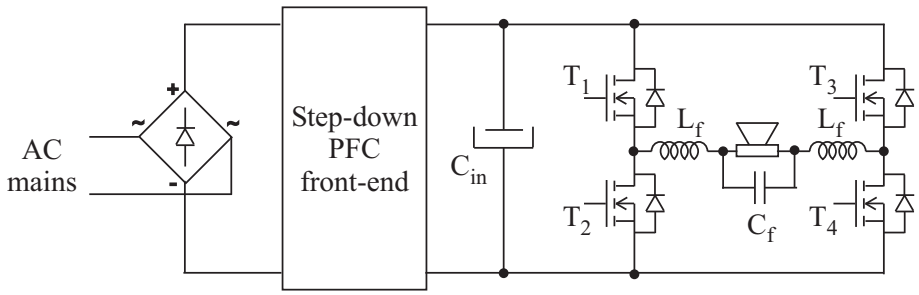

Fig. 3.4. Class D audio power amplifier with step-down PFC front-end

The most common way of providing PFC capability to the switching-mode power supplies is by implementing a boost stage front-end, which beside of acting as power factor corrector with stepped-up output voltage has an inductor on the input side, featuring continuous or discontinuous current and alleviating the Electro-Magnetic Compatibility (EMC) requirements. As noted before, high output voltage of the PFC can have adverse effects on the Class D audio power amplifier performance and therefore the boost PFC front-end is not an interesting approach to follow.

One possible choice of a PFC front-end is the SEPIC [1] shown in Fig. 3.5, which is capable of producing lower output voltages than the peak mains voltage. It has the advantages of being a single switch topology with an inductor on the input side, alleviating the EMC problems. Additionally, by coupling the two inductors in the topology and introducing some intentional leakage inductance in series with the input inductor, the inductor ripple current can be completely diverted from the input side to the internal coupled inductor and therefore reduce the need for input EMC filtering.

Unfortunately, the SEPIC PFC preregulator is characterized with much higher voltage and current stress on the main switch when compared to the common boost PFC prereg-

ulator, which becomes even more pronounced with much lower output voltages than the input voltage. This becomes clear from the buck-boost static transfer characteristics of the output voltage and the input current in the SEPIC case:

$$\begin{aligned} V_o &= \frac{D}{1-D} V_{in} \\ I_{in} &= \frac{D}{1-D} I_o \end{aligned} \tag{3.13}$$

where V_{in}, I_{in} and V_o, I_o are the input and output voltage and current of the SEPIC PFC front-end, correspondingly.

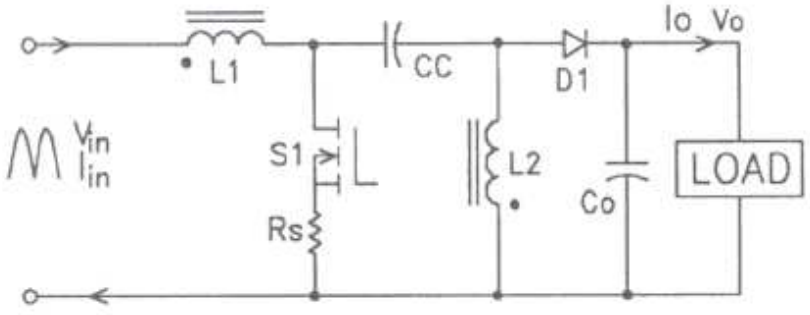

Fig. 3.5. SEPIC PFC preregulator [1]

Another possible choice is selection of boost-buck derived PFC topologies like the Sheppard-Taylor topology [36] and alike or more complex PFC schemes, like for example the non-isolated and isolated EWIRAC [37]. No matter what is the actual step-down PFC topology, a very interesting optimization problem can be set to find the optimal DC-bus voltage at the output of the PFC which leads to minimal overall losses of the PFC and Class D audio power amplifier, with as low as possible cost and acceptable audio perfromance.

3.4 Combined Class D audio power amplifier and PFC

The group of combined Class D audio power amplifiers and PFCs comprises of topologies where the whole or part of the Class D audio power amplifier plays some role in the shaping of the input current i.e. it is part of the PFC circuit. Unfortunately, the functions and the operation of an audio power amplifier and a PFC are not very similar, so that two degrees of control freedom in the Class D audio power amplifier are by all means necessary. These two degrees of control freedom are found only in the full-bridge amplifier topologies, like the one shown in Fig. 3.6.

The duty cycles of the two totem poles i.e. switching legs 1 and 2 can be represented as sums of an idling duty cycle $0 \leq D_0 \leq 1$ and variable duty cycles $0 \leq \Delta d_1, \Delta d_2 \leq 0.5$:

$$\begin{aligned} d_1 &= D_0 + \Delta d_1 \\ d_2 &= D_0 + \Delta d_2 \end{aligned} \tag{3.14}$$

It is worth noting that during the duty cycle duration $d_1 \cdot T_s$ and $d_2 \cdot T_s$ both lower switches (T_2, T_4) in the switching legs are on and the upper switches (T_1, T_3) are off. Both the idling duty cycle D_0 and the variable duty cycles $\Delta d_1, \Delta d_2$ can be independently set, but their corresponding sums must always represent a realizable duty cycle $0 \leq d_1, d_2 \leq 1$.

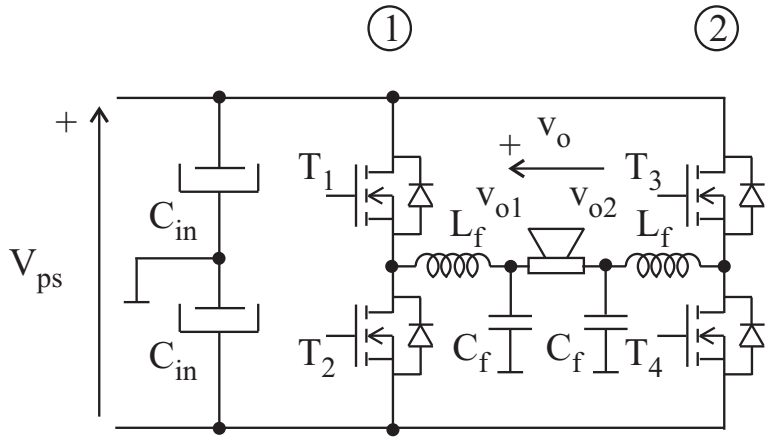

Fig. 3.6. Full-bridge Class D audio power amplifier

In conventional Class D audio power amplifier with appropriate input voltage, the value of the idling duty cycle is selected in the middle $D_0 = 0.5$.

The output voltages at both ends of the loudspeaker v_{o1} and v_{o2} referenced to ground are given by the following equations:

$$\begin{aligned} v_{o1} &= \frac{1-2d_1}{2}V_{ps} \\ v_{o2} &= \frac{1-2d_2}{2}V_{ps} \end{aligned} \tag{3.15}$$

The two degrees of freedom can be expressed as separate control of the differential mode voltage v_d being the load voltage and the common mode voltage v_c being the average load voltage to ground:

$$\begin{aligned} v_d &= v_{o1} - v_{o2} = (d_2 - d_1)V_{ps} = (\Delta d_2 - \Delta d_1)V_{ps} \\ v_c &= \frac{v_{o1} + v_{o2}}{2} = [1 - (d_1 + d_2)]V_{ps} = [1 - (2D_0 + \Delta d_1 + \Delta d_2)]V_{ps} \end{aligned} \tag{3.16}$$

It can be concluded that by selecting the two variable duty cycles to have the same magnitudes, but opposite signs $\Delta d = -\Delta d_1 = \Delta d_2$, the differential mode and the common mode load voltages become decoupled one from another and can be separately controlled with the variable duty cycle Δd and the idling duty cycle D_0 correspondingly:

$$\begin{aligned} v_d &= v_{o1} - v_{o2} = 2\Delta d V_{ps} \\ v_c &= \frac{v_{o1} + v_{o2}}{2} = (1 - 2D_0)V_{ps} \end{aligned} \tag{3.17}$$

The calculation of the variable duty cycle Δd starts by recognizing that the differential mode voltage across the loudspeaker is in fact the desired load voltage $v_o = v_d$ and therefore:

$$\Delta d = \frac{v_o}{2V_{ps}} \tag{3.18}$$

and the idling duty cycle D_0 is free to select as long as the resulting duty cycles of the switching legs d_1, d_2 are realizable i.e. $0 \leq d_1, d_2 \leq 1$ even at maximum output voltage. As a result of this limitation, all changes in the duty cycle difference are limited to $0 \leq \Delta d \leq 0.5$, which corresponds well with the expression (3.18) and the fact that at maximum duty cycle the output voltage of the full-bridge amplifier is $v_o = \pm V_{ps}$. This

is graphically represented in Fig. 3.7, where the power supply voltage is $V_{ps} = 100$ V and the maximum output voltage is $V_{o,max} = 40$ V. With the given voltage levels, the maximum difference duty cycle $\Delta d_{max} = 0.2$ and the idling duty cycle can vary in the range $D_0 = [0.2, 0.8]$.

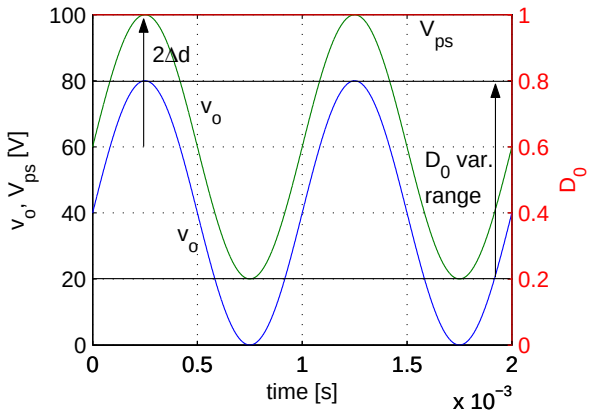

Fig. 3.7. Variations in the output voltage and duty cycles

These conclusions will be used in the following few sections to simplify the construction of combined Class D audio power amplifier and PFC stage, by reusing one or two of the switching legs.

3.4.1 Combined Class D audio power amplifier and boost PFC

Combined Class D audio power amplifier with a boost PFC front-end is depicted in Fig. 3.8. As it is shown, one switching leg of the Class D audio power amplifier is used as a boost active switch with synchronous rectifier. The two degrees of freedom when selecting the differential mode and common mode load voltage mean that the load voltage v_o can be set independently of the operation of the boost converter, which shapes the input current i_{in} while trying to keep constant voltage on the DC-link energy storage capacitor C_{in}, v_{Cin}.

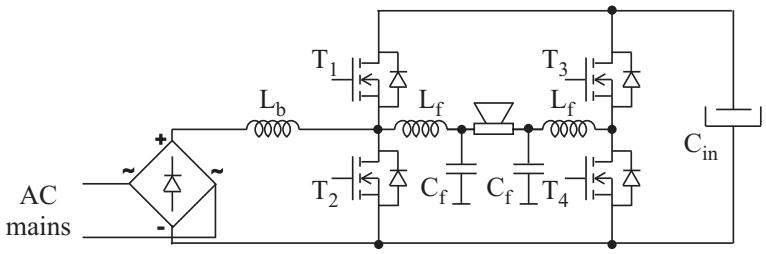

Fig. 3.8. Combined Class D audio power amplifier and boost PFC

The main disadvantage of the combined Class D audio power amplifier with boost PFC is the high voltage across the energy storage capacitor C_{in} which is always higher than the peak input voltage $v_{Cin} > v_{in,pk}$. As discussed in the previous section, high input voltage to the Class D audio power amplifier necessitates using higher blocking voltage active devices and leads to increased conduction losses and lower audio performance with increased THD. However, the topology looks very interesting from a theoretical point of view, since it looks very compact and strongly reminds of the single-stage PFCs [38], [39].

The analysis of operation of the combined Class D audio power amplifier with boost PFC front-end in Continuous Conduction Mode (CCM) through state-space averaging is presented in Appendix B.1. The four different connections in the operation of the combined Class D audio power amplifier and boost PFC are shown in Fig. 3.9. Stepping through the different possible connections is performed according to the sign of the output voltage, and is shown in Fig. 3.9 with the plus and minus sign.

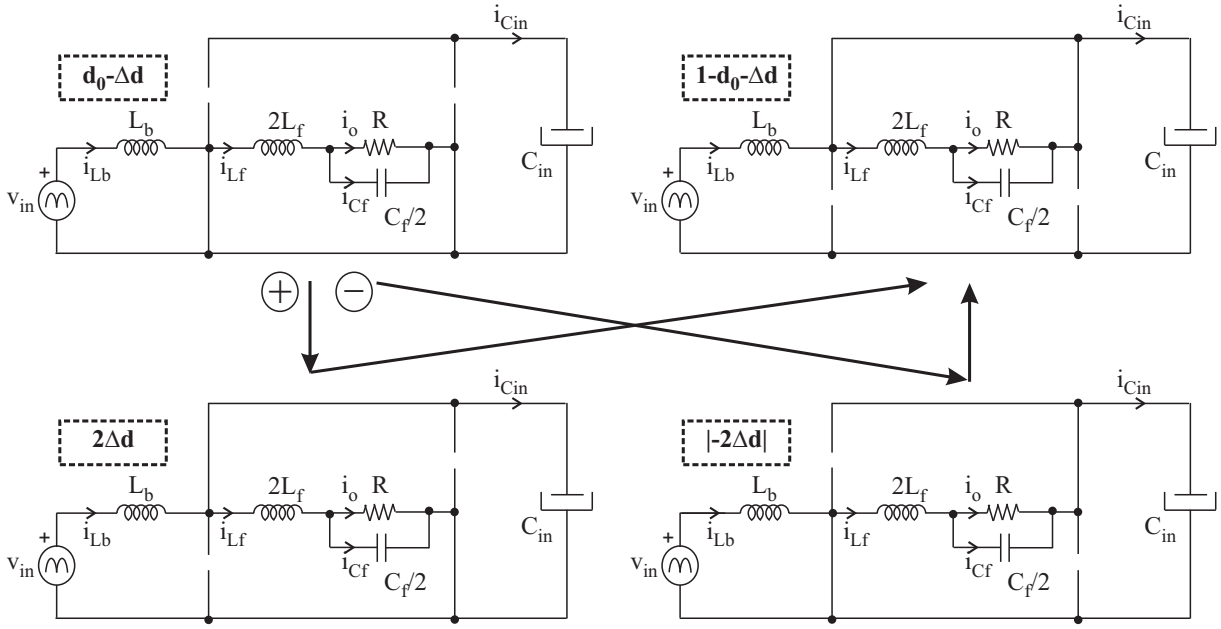

Fig. 3.9. Possible connections in the combined Class D audio power amplifier and boost PFC

The differences in the models for positive and negative output voltages stem from the fact that the boost PFC is asymmetrical in regard with the full-bridge Class D audio power amplifier and this translates to slight changes in the models. Although this does not seem to cause any problems, symmetrical operation can be achieved by using two boost inductors in arrangement shown in Fig. 3.10.

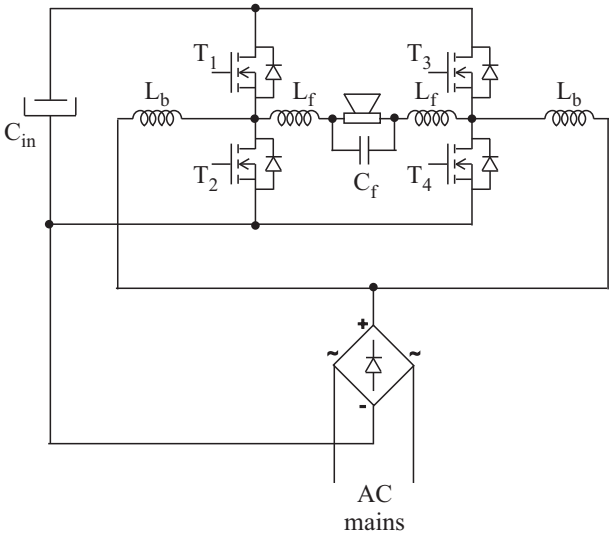

Fig. 3.10. Combined Class D audio power amplifier and boost PFC with two boost inductors

The DC-model of the combined Class D audio power amplifier and boost PFC developed in Appendix B.1 for positive output voltages is:

$$\begin{aligned} V_{Cin} &= \frac{V_{in}}{1 - D_0 + \Delta D} \\ V_o &= 2\Delta D V_{Cin} \\ I_{Lb} &= \frac{2\Delta D I_{Lf}}{1 - D_0 + \Delta D} \\ I_{Lf} &= \frac{V_o}{R} = I_o \end{aligned} \tag{3.19}$$

and for negative output voltages is:

$$\begin{aligned} V_{Cin} &= \frac{V_{in}}{1 - D_0 - \Delta D} \\ V_o &= -2\Delta D V_{Cin} \\ I_{Lb} &= -\frac{2\Delta D I_{Lf}}{1 - D_0 - \Delta D} \\ I_{Lf} &= \frac{V_o}{R} = I_o \end{aligned} \tag{3.20}$$

The maximum variation of the steady-state value of the duty cycle ΔD used to provide the desired output voltage can be found from the second equation in (3.19):

$$\Delta D_{max} = \frac{V_{o,max}}{2V_{Cin}} \tag{3.21}$$

As a result of the limitation on the maximum duty cycle ΔD_{max} there is a limitation on the maximum and minimum steady-state value of the idling duty cycle D_0:

$$\begin{aligned} D_{0,min} &= \Delta D_{max} \\ D_{0,max} &= 1 - \Delta D_{max} \end{aligned} \tag{3.22}$$

since all realizable duty cycles are between 0 and 1. This essentially means that the idling duty cycle D_0 is free to vary in a range $[D_{0,min}, D_{0,max}]$, thus leaving enough space for the duty cycle difference ΔD to reconstruct even the highest peaks of the output voltage.

The idling duty cycle D_0 is used to shape the input current i_{in}, while trying to maintain as constant capacitor voltage v_{Cin} as possible, and it can be determined for positive output voltages from the first equation in (3.19):

$$D_0 = \frac{(1 + \Delta D)V_{Cin} - V_{in}}{V_{Cin}} = (1 + \Delta D) - \frac{|V_{in,pk} \sin(\omega t)|}{V_{Cin}} \tag{3.23}$$

which gives the maximum and minimum idling duty cycles D_0 for $sin(\omega t) = 0$ and $sin(\omega t) = 1$, respectively:

$$\begin{aligned} D_{0,min} &= 1 + \Delta D_{min} - \frac{V_{in,pk}}{V_{Cin}} = 1 - \frac{V_{in,pk}}{V_{Cin}} \\ D_{0,max} &= 1 + \Delta D_{max} \overset{limit}{\longrightarrow} 1 \end{aligned} \tag{3.24}$$

Comparing the results in (3.24) with (3.22) it becomes apparent that the required maximum idling duty cycle of $D_{0,max} = 1$ cannot be reached due to the need for reproducing

audio at the same time. Using the minimum idling duty cycle in (3.24), as well as the expressions in (3.21) and (3.22), the following relation for the minimum capacitor voltage $V_{Cin,min}$ can be developed:

$$\begin{aligned} D_{0,min} &= 1 - \frac{V_{in,pk}}{V_{Cin}} = \Delta D_{max} = \frac{V_{o,max}}{2V_{Cin}} \\ \Rightarrow \quad V_{Cin,min} &= V_{in,pk} + \frac{V_{o,max}}{2} \end{aligned} \tag{3.25}$$

Similar analysis can be performed with the DC-model for negative output voltages, which will give the following relationship between the idling duty cycle D_0 and the input voltage:

$$D_0 = (1 - \Delta D) - \frac{|V_{in,pk} \sin(\omega t)|}{V_{Cin}} \tag{3.26}$$

and the following minimum capacitor voltage $V_{Cin,min}$:

$$\begin{aligned} D_{0,min} &= 1 - \Delta D_{max} - \frac{V_{in,pk}}{V_{Cin}} = \Delta D_{max} = \frac{V_{o,max}}{2V_{Cin}} \\ \Rightarrow \quad V_{Cin,min} &= V_{in,pk} + V_{o,max} \end{aligned} \tag{3.27}$$

The final value for the capacitor voltage is the maximum of the minimums in (3.25) and (3.27), i.e. $V_{Cin,min} = V_{in,pk} + V_{o,max}$.

A block diagram of the control circuit for the combined Class D audio power amplifier and boost PFC front-end is depicted in Fig. 3.11. Unfortunately, full PFC operation cannot be achieved due to the aforementioned limitation on the realizable duty cycles $0 \leq d_1, d_2 \leq 1$, by which the minimum and maximum idling duty cycles are $d_{0,min} = \Delta d_{max}$ and $d_{0,max} = 1 - \Delta d_{max}$. These problems are alleviated with lower output power Class D audio power amplifiers or lower impedance loudspeakers, which results in lower peak output voltage levels $V_{o,pk}$ and subsequently lower duty cycle variations Δd_{max}.

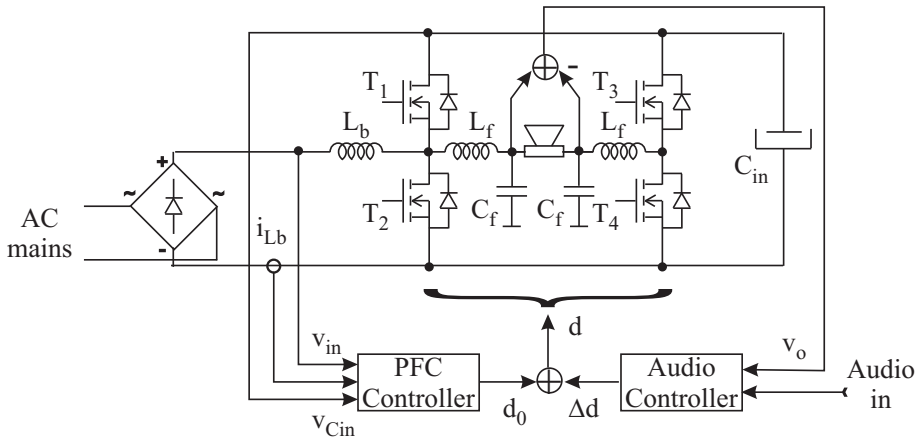

Fig. 3.11. Control diagram of a combined Class D audio power amplifier and boost PFC

Simulation of combined Class D audio power amplifier and boost PFC

Operation of the combined Class D audio power amplifier and boost PFC from Fig. 3.8 was tested by simulation. The resulting waveforms are given in Fig. 3.12.

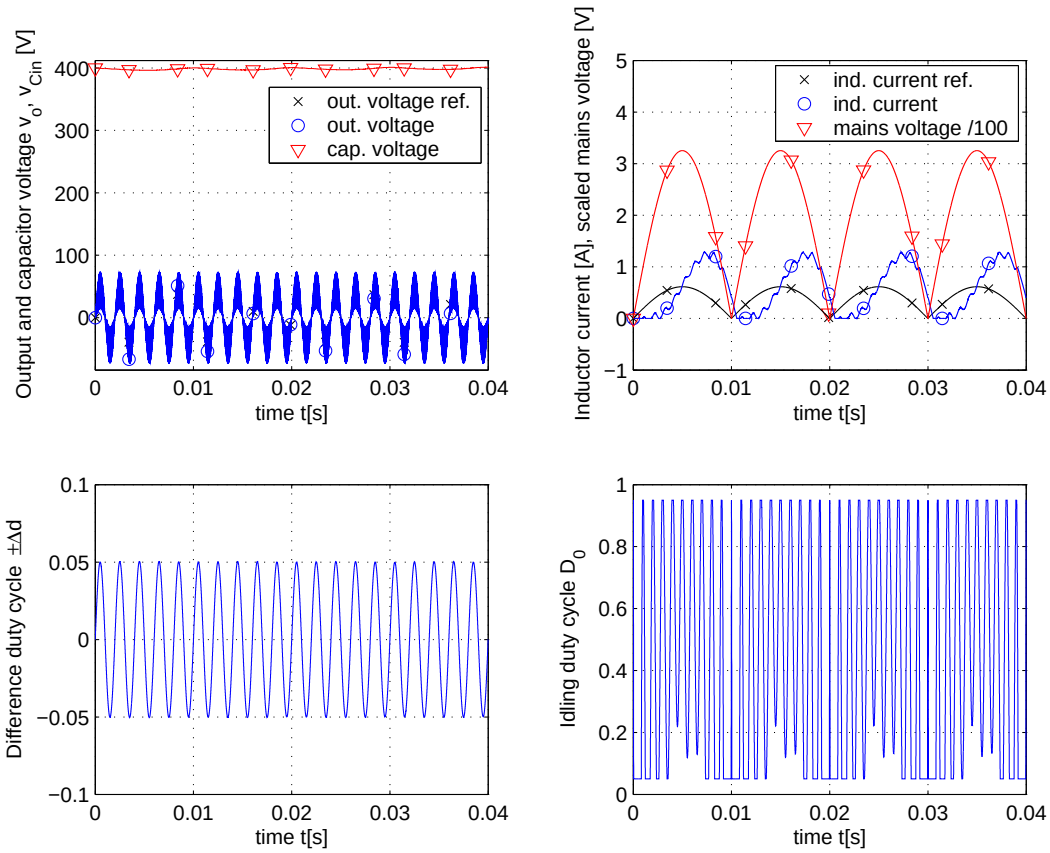

Fig. 3.12. Simulated waveforms of combined Class D audio power amplifier and boost PFC

The converter was operated in open loop, where the difference duty cycle Δd was calculated from (3.19) and (3.20) to be:

$$\Delta d = \pm \frac{v_o}{2V_{Cin}} \tag{3.28}$$

and the idling duty cycle D_0 is:

$$D_0 = \frac{(1 \pm \Delta d) I_{Lb,ref} \mp 2\Delta d \frac{v_o}{R}}{I_{Lb,ref}} \tag{3.29}$$

where the reference boost inductor current $I_{Lb,ref}$ was derived from the rectified AC mains voltage.

The output voltage waveform in Fig. 3.12 follows the output voltage reference in a satisfactory way, except that the output voltage ripple is excessive. If full audio bandwidth operation and maximally linear response are required, then the output LC filter must start attenuating at higher frequencies and is not so effective at the switching frequency. One possible way of alleviating this is using a higher order output filter or significantly increasing the switching frequency. The voltage ripple in the energy storage capacitor C_{in} is at double frequency of the AC-mains voltage and is result of the difference between the pulsating power delivered from the AC-mains and power consumed by the load. The variations in the difference duty cycle Δd follow the output voltage reference, as required.

Boost inductor current is distorted, but in principle its shape resembles the shape of the rectified AC-mains voltage. The insufficient slope of the inductor current near the zero of the mains voltage is a problem pertinent to every boost-type PFC, and has nothing to do with the particular topology and the limitations imposed on the idling duty cycle D_0. The variations in the idling duty cycle D_0 are shown in the last diagram in Fig. 3.12 and both its minimum and maximum value are clearly visible.

3.4.2 Combined Class D audio power amplifier and buck-boost PFC

The main advantage of buck-boost PFC is in the lower DC-bus voltage, which alleviates the problems with the high input voltage Class D audio power amplifiers. Buck-boost operation is achieved through active rectification of the net voltage by adding controlled switches in the mains rectifier and sometimes a freewheeling diode, as shown in Fig. 3.13. The latter switches have bidirectional voltage capability, which means that they can block both voltage polarities, but have just unipolar current capability. One possible implementation of the switch is given in Fig. 3.13d.

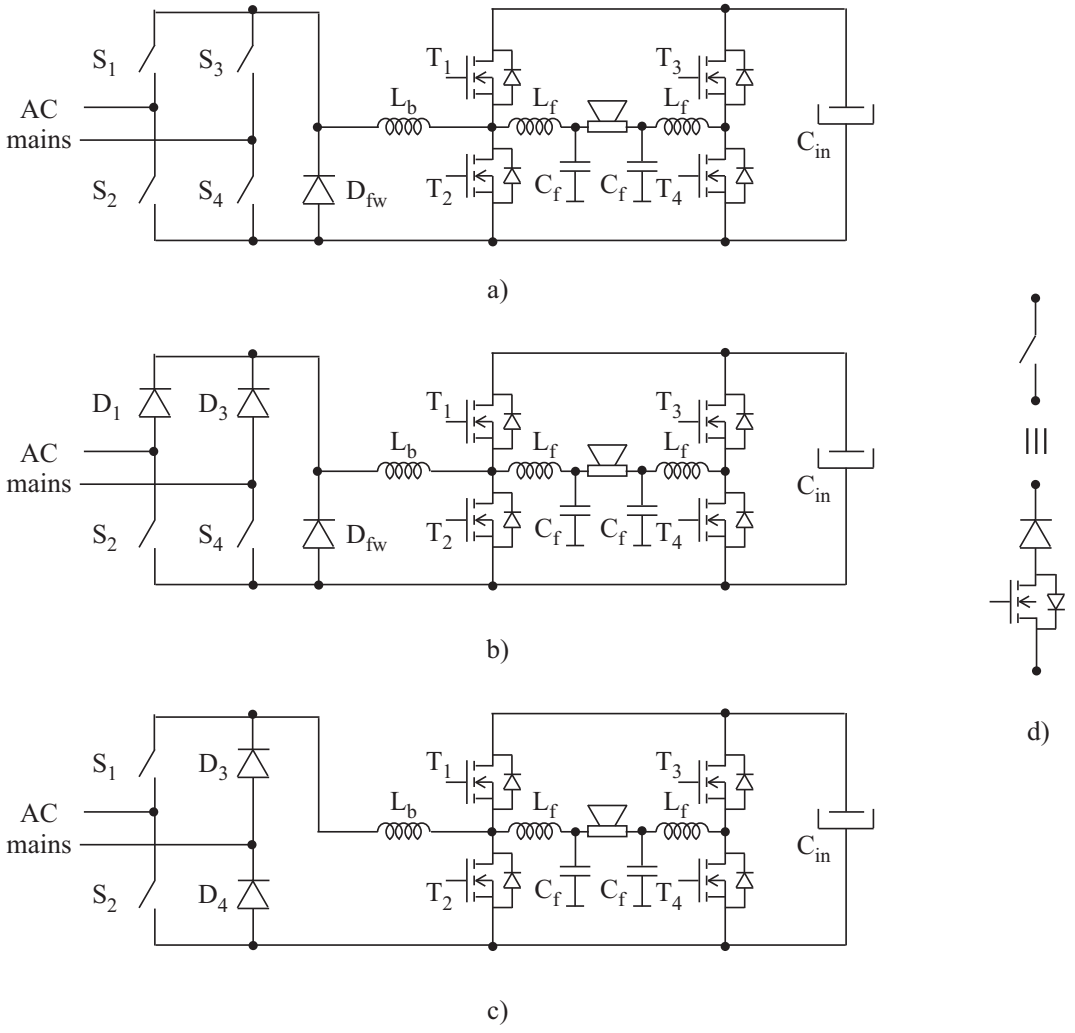

Fig. 3.13. Combined Class D audio power amplifier and buck-boost PFC: a) with 4 switches and a freewheeling diode, b) with 2 switches and a freewheeling diode, c) with 2 switches, and d) one possible realization of the switch

Switches in the active rectifier can be operated either in synchronism with the switches in the Class D audio power amplifier, or they can be operated independently i.e. asynchronously with the same or with different switching frequency and phase. One distinct advantage of the independent operation of the proposed buck-boost PFC, when compared to the previously presented boost PFC and synchronously-operated buck-boost PFC, is that the active rectifier has much greater control of the input current.

The disadvantages of this non-isolated SICAM approach lie in the active rectifier, which necessitates few active switching devices with complex gate drives, as well as the need for ultra-fast diodes with low reverse recovery charge, instead of using regular and cheap

mains rectifiers. At the same time, switching the active rectifier leads to interrupted input current, which necessitates use of large EMC filters on the input side. On the other hand, it is clear that synchronous operation of the active rectifier and Class D audio power amplifier, although somewhat simpler than the independent control, does not allow for very large variation of the idling duty cycle D_0 since the supply voltage across C_{in} is supposed to be only slightly higher than the maximum output voltage.

The analysis of the synchronous operation of combined Class D audio power amplifier and buck-boost PFC front-end in CCM through state-space averaging is presented in Appendix B.2. The four different connections in the operation of the combined Class D audio power amplifier and buck-boost PFC are shown in Fig. 3.14. Stepping through the different possible connections is performed according to the sign of the output voltage, and is shown in Fig. 3.14 with the plus and minus sign.

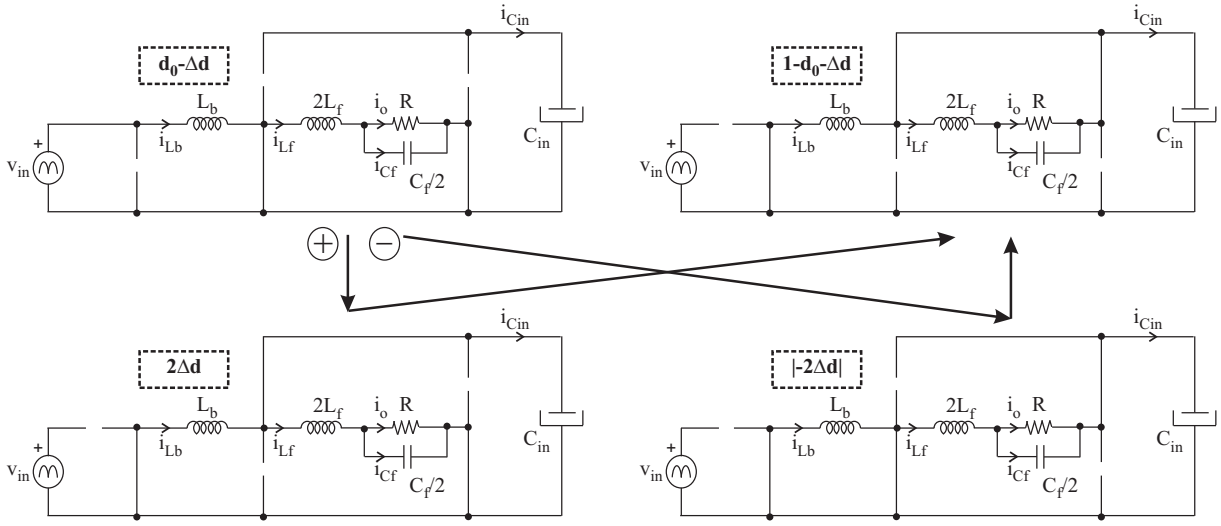

Fig. 3.14. Possible connections in the synchronously-operated combined Class D audio power amplifier and buck-boost PFC

The DC-model of the combined Class D audio power amplifier and buck-boost PFC in synchronous operation mode, developed in Appendix B.2 for positive output voltages is:

$$\begin{aligned} V_{Cin} &= \frac{(D_0 - \Delta D)V_{in}}{1 - D_0 + \Delta D} \\ V_o &= 2\Delta D V_{Cin} \\ I_{Lb} &= \frac{2\Delta D I_{Lf}}{1 - D_0 + \Delta D} \\ I_{Lf} &= \frac{V_o}{R} = I_o \end{aligned} \tag{3.30}$$

and for negative output voltages is:

$$\begin{aligned} V_{Cin} &= \frac{(D_0 - \Delta D)V_{in}}{1 - D_0 - \Delta D} \\ V_o &= -2\Delta D V_{in} \\ I_{Lb} &= -\frac{2\Delta D I_{Lf}}{1 - D_0 - \Delta D} \\ I_{Lf} &= \frac{V_o}{R} = I_o \end{aligned} \tag{3.31}$$

The same limitations on the duty cycle difference ΔD and idling duty cycle D_0 given in (3.21) and (3.22) are also valid here.

In contrast to the case of the boost PFC, in synchronously-operated buck-boost PFC the idling duty cycle D_0 controls both the bucking and boosting action of the PFC. The variations in the idling duty cycle D_0 are such as to shape the input current i_{in} according to the input voltage, while maintaining as constant capacitor voltage v_{Cin} as possible, and it can be determined for positive output voltages from the first equation in (3.30):

$$D_0 = \frac{V_{Cin}}{V_{in} + V_{Cin}} + \Delta D = \frac{V_{Cin}}{|V_{in,pk} \sin(\omega t)| + V_{Cin}} + \Delta D \tag{3.32}$$

which gives the maximum and minimum idling duty cycles D_0 for $sin(\omega t) = 0$ and $sin(\omega t) = 1$, respectively:

$$\begin{aligned} D_{0,min} &= \frac{V_{Cin}}{V_{in,pk} + V_{Cin}} \\ D_{0,max} &= 1 + \Delta D_{max} \xrightarrow{limit} 1 \end{aligned} \tag{3.33}$$

Comparing the results in (3.33) with (3.22) it is again clear that the required maximum idling duty cycle of $D_{0,max} = 1$ cannot be reached due to the need for reproducing audio at the same time.

The buck-boost PFC is capable of creating both lower and higher input capacitor voltages v_{Cin} than the mains peak voltage $V_{in,pk}$, but the lowest input capacitor voltage V_{Cin} will be essentially limited by the maximum output voltage $V_{o,max}$, so that always $V_{Cin} > V_{o,max}$. When the input capacitor voltage is chosen such that it is only slightly higher than the maximum output voltage, the maximum duty cycle difference is $\Delta D_{max} \approx 0.5$ and the idling duty cycle is nearly constant $D_0 \approx 0.5$. This, however, prohibits the synchronously operated buck-boost PFC and Class D amplifier from accommodating larger variations in the input voltage. The only way of solving this problem is by increasing the input capacitor voltage v_{Cin} to allow for bigger changes in the idling duty cycle D_0, which by itself is very similar to the boost PFC approach and therefore is not so interesting.

Similar analysis can be performed with the DC-model for negative output voltages in (3.31), which will give the following relationship between the idling duty cycle D_0 and the input voltage:

$$D_0 = (1 - 2\Delta D)\frac{V_{Cin}}{|V_{in,pk} \sin(\omega t)| + V_{Cin}} + \Delta D \tag{3.34}$$

The analysis of the asynchronous operation of combined Class D audio power amplifier and buck-boost PFC front-end in CCM is made using the connection diagrams in Fig. 3.15 and is given in detail in Appendix B.3.

The DC-model of the combined Class D audio power amplifier and buck-boost PFC in asynchronous operation mode, developed in Appendix B.3 for positive output voltages i.e. switching sequences $I - III$ is:

$$\begin{aligned} V_{Cin} &= \frac{D_a V_{in}}{1 - D_0 + \Delta D} \\ V_o &= 2\Delta D V_{Cin} \\ I_{Lb} &= \frac{2\Delta D I_{Lf}}{1 - D_0 + \Delta D} \\ I_{Lf} &= \frac{V_o}{R} = I_o \end{aligned} \tag{3.35}$$

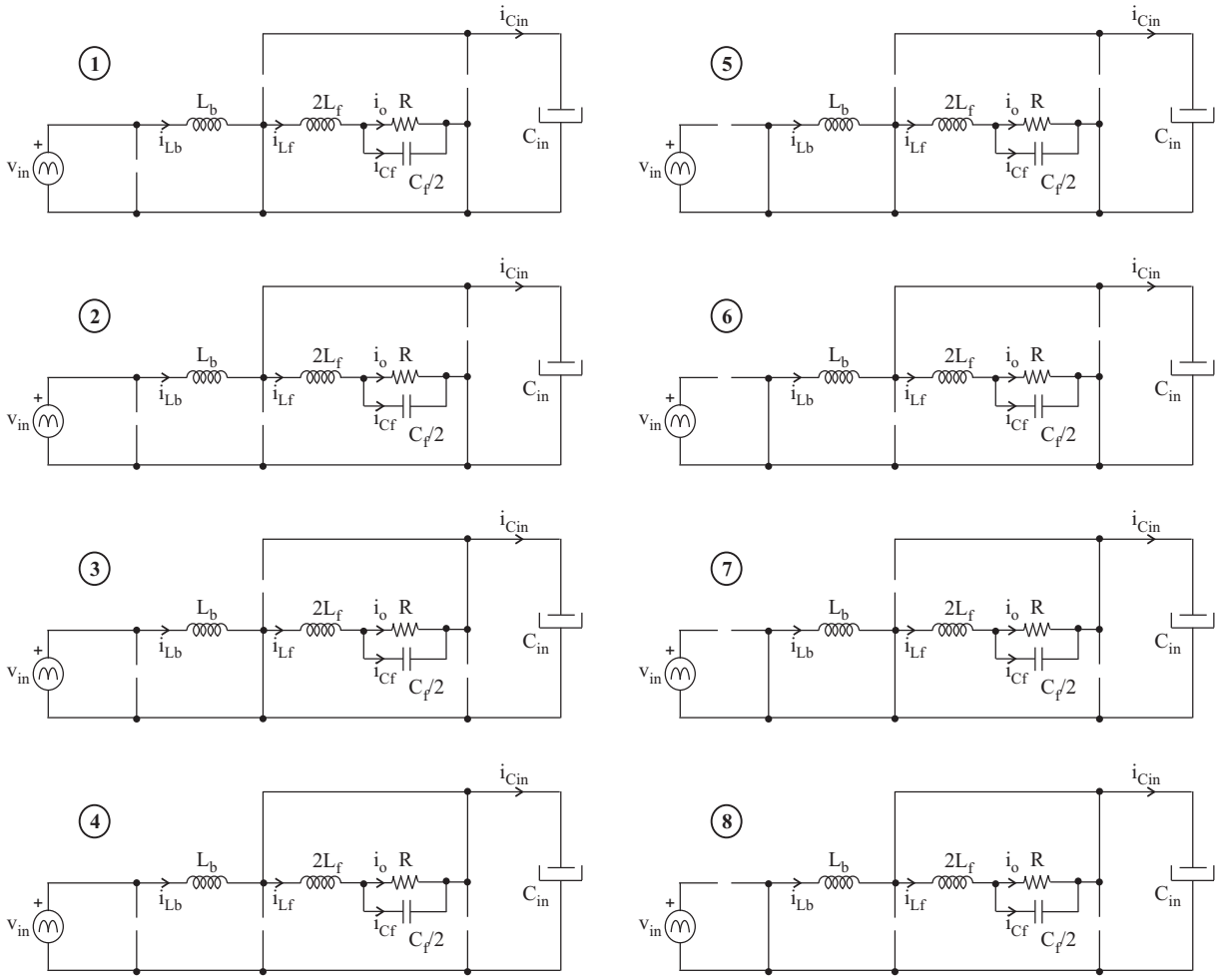

Fig. 3.15. Possible connections in the asynchronously-operated combined Class D audio power amplifier and buck-boost PFC

and for negative output voltages varies among:

$$\begin{aligned} V_{Cin} &= \frac{D_a V_{in}}{1 - D_0 - \Delta D} \\ V_o &= -2\Delta D V_{Cin} \\ I_{Lb} &= -\frac{2\Delta D I_{Lf}}{1 - D_0 - \Delta D} \\ I_{Lf} &= \frac{V_o}{R} = I_o \end{aligned} \tag{3.36}$$

for $d_a < (d_0 - \Delta d)$,

$$\begin{aligned} V_{Cin} &= \frac{D_a V_{in}}{1 - D_a - 2D_0} \\ V_o &= -2\Delta D V_{Cin} \\ I_{Lb} &= -\frac{2\Delta D I_{Lf}}{1 - D_0 - \Delta D} \\ I_{Lf} &= \frac{V_o}{R} = I_o \end{aligned} \tag{3.37}$$

for $(d_0 - \Delta d) < d_a < (d_0 + \Delta d)$, and

$$\begin{aligned} V_{Cin} &= \frac{D_a V_{in}}{1 - D_0 + \Delta D} \\ V_o &= -2\Delta D V_{Cin} \\ I_{Lb} &= -\frac{2\Delta D I_{Lf}}{1 - D_0 - \Delta D} \\ I_{Lf} &= \frac{V_o}{R} = I_o \end{aligned} \tag{3.38}$$

for $(d_0 + \Delta d) < d_a < 1$.

The same limitations on the duty cycle difference ΔD and idling duty cycle D_0 given in (3.21) and (3.22) are also valid here.

As seen in (3.35), the asynchronously operated buck-boost PFC can control the input current and the output voltage in buck mode by varying the duty cycle D_a of the switches in the active rectifier, while in boost mode the same can be done by the idling duty cycle D_0. In buck mode of PFC operation the voltage across the input capacitor is lower than the input voltage $V_{Cin} < v_{in}$ and the expression for the duty cycle D_a with positive output voltage in all switching sequences and negative output voltage in switching sequence VI is obtained from the first equation in (3.35):

$$D_a = (1 - D_0 + \Delta D)\frac{V_{Cin}}{V_{in}} \tag{3.39}$$

and in boost mode $V_{Cin} > v_{in}$ for the idling duty cycle D_0:

$$D_0 = (1 + \Delta D) - D_a \frac{V_{in}}{V_{Cin}} \tag{3.40}$$

However, instead of using D_a and D_0 exclusively in buck or boost mode respectively, their variations can be combined across operating modes in a way that assures that both duty cycles are realizable and satisfy $0 \leq D_a \leq 1$ and $\Delta D_{max} \leq D_0 \leq 1 - \Delta D_{max}$, while improving the performance. For example, when the idling duty cycle D_0 has reached its maximum value in (3.40) with low input voltage, the duty cycle of the active rectifier D_a can be increased in order to maintain the desired input capacitor voltage V_{Cin}. In other words, combined variations of D_a and D_0 lead to extended operation range of the asynchronously-operated combined buck-boost PFC and Class D audio power amplifier, but it essentially experiences the same limitation in the boost mode like the aforementioned boost PFC and synchronously-operated buck-boost PFC, since the maximum idling duty cycle is limited to $D_{0,max} = 1 - \Delta_{max}$.

Similar analysis can be performed with the DC-model for negative output voltages in switching sequences IV and V, with the only difference that in the switching sequence V the duty cycle of the active rectifier governs not only the operation in buck mode, but also assists boosting of the output voltage.

The block diagram of the control circuit for the combined Class D audio power amplifier and buck-boost PFC front-end is very similar to the one for the combined Class D audio power amplifier and boost PFC, shown in Fig. 3.11.

3.5 Conclusion

The greatest challenges of the non-isolated directly mains-connected SICAMs are the relatively high rectified mains voltage and the wish for providing very compact and essentially single-stage designs with some extra features, like PFC.

It was shown in this chapter that there are ways of alleviating some of the aforementioned problems, by providing separate step-down PFC front ends which make possible using of lower input voltage Class D audio power amplifiers. This, however, results in essentially a two stage approach with all the drawbacks in terms of efficiency and complexity which come with it.

It was also shown that by giving up on the wish to use lower input voltage Class D audio power amplifier, combined Class D audio power amplifier and boost PFC front-end can be built in a simple manner by just adding an additional boost inductor(s). Eventually, by introducing active rectifier at the mains input, both PFC capability and lower input voltage Class D audio power amplifier can be integrated in a single unit to bring a single-stage amplification topology with built-in buck-boost PFC front-end. Certain limitations are common to all these combined approaches and stem from reusing the full-bridge Class D audio power amplifier and the extra degree of freedom i.e. the varying load common-mode voltage, which can be independently set as long as it does not interfere with the reproduction of audio signals in the differential-mode voltage.

4

SICAM for portable devices

" ... In the intuitive mind the principles are found in common use, and are before the eyes of everybody. One has only to look, and no effort is necessary; it is only a question of good eyesight, but it must be good, for the principles are so subtle and so numerous, that it is almost impossible but that some escape notice. Now the omission of one principle leads to error; thus one must have very clear sight to see all the principles, and in the next place an accurate mind not to draw false deductions from known principles."

- From "Thoughts", Blaise Pascal

According to the project description given in Section 1, SICAM is highly compact audio power amplification solution with or without isolation and is intended for operation on AC mains voltage. However, this does not mean that there are no problems with efficient and compact audio power amplification in portable devices i.e. battery powered devices. The main challenges in this area are low and strongly variable battery voltage V_{bat} depending on the state of charge, which significantly affects the highest achievable audio output power level with the common buck-type topologies, like the Class D audio power amplifiers. Today, most of the switching solutions for portable devices consists of some type of full bridge topology in order to maximize the load voltage swing, in this case being equal to the battery voltage $\pm V_{bat}$.

For powering loudspeakers with higher impedance or for achieving higher audio output power levels with battery powered devices, the easiest solution seems to be using a battery voltage booster, followed by a linear or Class D audio power amplifier. This essentially represents a two stage approach, which is likely to have lower efficiency when compared with some single stage topology.

This chapter deals with the development of topology and digital control principle for a single-stage audio power amplifier for portable devices, capable of boosting the output voltage with respect to the input battery voltage. Since all voltage step-up topologies (boost, buck-boost, etc.) experience very nonlinear output characteristics which are only somewhat linearized with the application of analog feedback, the main goal of the presented work is to develop a digital modulator structure that is capable of linearizing the transfer characteristics of the proposed nonlinear amplifier in open-loop operation.

4.1 Single-stage step-up audio power amplifier topology for portable applications

As mentioned in the introductory part, low and variable battery voltage limits the highest achievable audio output power. For example, the common Li-Ion battery as used in today's mobile phones has a nominal voltage of $V_{bat} = 3.6$ V, but the actual voltage strongly depends on the state of charge and varies from $V_{bat,max} = 4.2$ V with fully charged battery down to $V_{bat,min} = 2.5$ V when battery is depleted. Buck-type audio power amplifiers in

the face of the Class D audio power amplifier can create output voltage which is always lower than the battery voltage $v_o < V_{bat}$.

The main goal of the new amplifier topology for battery-powered devices to be developed is to be able to achieve higher audio output powers and at the same time maintain that output level despite of the decreasing battery voltage. This clearly asks for boost or buck-boost -type topology, which can step-up the battery voltage to higher levels.

The main problem of the boost and buck-boost DC-DC converter topology with regard to amplifier applications is that they cannot produce alternating output voltage for driving a loudspeaker, since they perform merely a transformation of one input DC voltage level to another output DC voltage level. However, by using two identical boost or buck-boost DC-DC converters connected to the loudspeaker in a differential mode, load voltages of both polarities can be easily produced by properly controlling the switching devices. While the loudspeaker is being supplied by the amplifiers differential-mode voltage, both terminals of the loudspeaker are riding on the amplifiers common-mode voltage. The circuit diagram of the proposed double-boost SICAM, also known under the name of push-pull boost converter [40], [41] is given in Fig. 4.1.

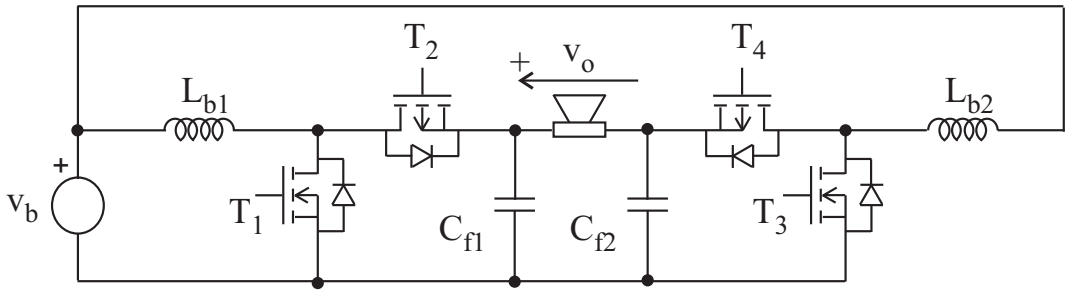

Fig. 4.1. Double boost SICAM

Operation of the double-boost SICAM can be divided into two separate parts, depending on the output voltage polarity. For positive output voltages $V_{Cf1} > V_{Cf2}$, T_4 is kept turned on and T_3 turned off, while switches T_1 and T_2 are operated in PWM fashion, thus assuring that capacitor voltage V_{Cf1} is increasing over the battery voltage V_b and average capacitor voltage V_{Cf2} is equal to the battery voltage $V_{Cf2} = V_b$. For negative output voltages $V_{Cf1} < V_{Cf2}$, T_2 is kept turned on and T_1 turned off, while switches T_3 and T_4 are operated in PWM fashion, thus assuring that capacitor voltage V_{Cf2} is increasing over the battery voltage V_b and average capacitor voltage V_{Cf1} is equal to the battery voltage $V_{Cf1} = V_b$. Operation of the double-boost SICAM is summarized in Table 4.1.

Output voltage	T_1	T_2	T_3	T_4
+	d	(1-d)	0	1
-	0	1	d	(1-d)

Table 4.1. Switching states of the double-boost SICAM

The four different connections in the operation of the combined double-boost SICAM are shown in Fig. 4.2. Stepping through the different possible connections is performed according to the sign of the output voltage, and is shown in Fig. 4.2 with the plus and minus sign.

The detailed DC and small-signal AC analysis of the double-boost SICAM operation is given in Appendix C. Especially interesting is the DC-model of the double-boost SICAM

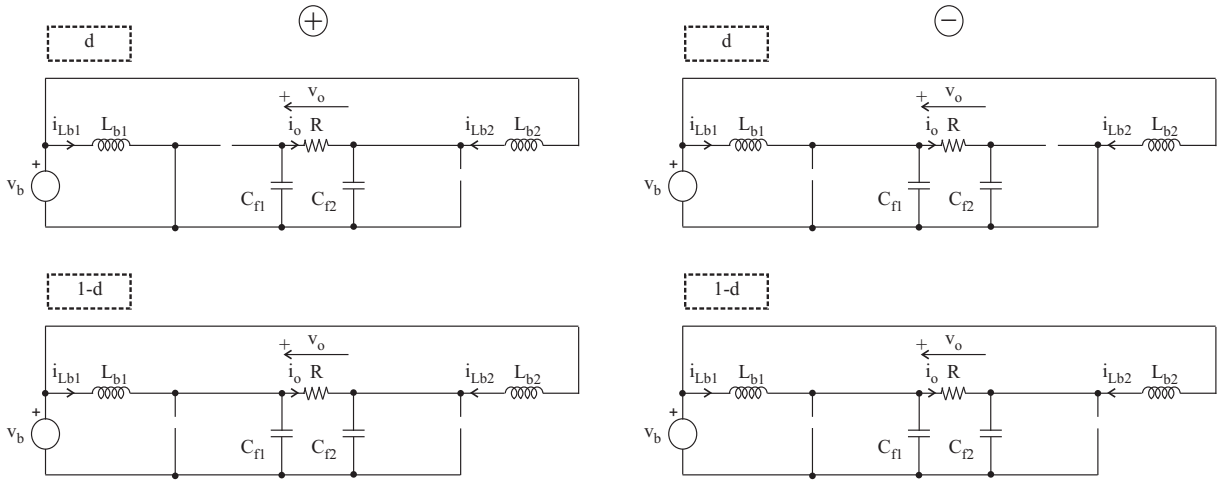

Fig. 4.2. Possible connections in the double-boost SICAM

(C.13) for positive output voltages:

$$\begin{aligned}
0 &= V_b - (1-D)V_{Cf1} \quad &\Rightarrow \quad V_{Cf1} &= \frac{V_b}{1-D} \\
0 &= V_b - V_{Cf2} \quad &\Rightarrow \quad V_{Cf2} &= V_b \\
0 &= -\frac{V_{Cf1} - V_{Cf2}}{R} + (1-D)I_{Lb1} \quad &\Rightarrow \quad I_{Lb1} &= \frac{V_{Cf1} - V_{Cf2}}{(1-D)R} \\
0 &= \frac{V_{Cf1} - V_{Cf2}}{R} + I_{Lb2} \quad &\Rightarrow \quad I_{Lb2} &= -\frac{V_{Cf1} - V_{Cf2}}{R}
\end{aligned} \tag{4.1}$$

and (C.14) for negative output voltages:

$$\begin{aligned}
0 &= V_b - V_{Cf1} \quad &\Rightarrow \quad V_{Cf1} &= V_b \\
0 &= V_b - (1-D)V_{Cf2} \quad &\Rightarrow \quad V_{Cf2} &= \frac{V_b}{1-D} \\
0 &= -\frac{V_{Cf1} - V_{Cf2}}{R} + I_{Lb1} \quad &\Rightarrow \quad I_{Lb1} &= \frac{V_{Cf1} - V_{Cf2}}{R} \\
0 &= \frac{V_{Cf1} - V_{Cf2}}{R} + (1-D)I_{Lb2} \quad &\Rightarrow \quad I_{Lb2} &= -\frac{V_{Cf1} - V_{Cf2}}{(1-D)R}
\end{aligned} \tag{4.2}$$

The most important conclusion from both (4.1) and (4.2) is that:

$$V_o = V_{Cf1} - V_{Cf2} = \pm\frac{D}{1-D}V_b \tag{4.3}$$

which shows that the differential mode voltage i.e. the load voltage of the double boost SICAM can have either polarity and can be either lower for $D < 0.5$ or higher for $D > 0.5$ than the battery voltage V_b, which is beneficial for portable applications. Unfortunately, the relation between the duty cycle D and the output voltage V_o is strongly nonlinear and it resembles the one of the buck-boost converter, although the basic building block of the amplifier is the boost converter.

4.2 Digital audio modulator for the double-boost SICAM

In the last few years, there has been an ongoing public discussion about whether the analog or the digital modulating approach will prevail in the future. However, it seems that both

approaches have their distinct advantages and certain preferred types of applications, which guarantee their presence on the market in near future. No matter what the result of this "battle" will be in few years, it is a fact that most of the audio sound sources today have a digital format and coding in telecommunications is becoming almost entirely digital. Therefore, it is of an utmost interest, especially in small form portable devices, to perform a straightforward transformation of the PCM or other digital audio code into PWM, capable of driving the switches in the switching-mode audio power amplifiers. This has also some unique advantages in a sense that different digital audio processing algorithms can be implemented in the same digital hardware to give an extra flexibility. For most of the commercial applications, the aforementioned fully digital audio power amplifiers are constrained to operate in open-loop mode, since adding a very fast and high resolution analog-to-digital converter (ADC) to close the feedback loop significantly adds to their cost.

Among the advantages of the digital modulators for switching-mode audio power amplifiers, one being especially appealing for the double-boost SICAM and possibly for all other boost and buck-boost type audio power amplifiers is the ease of designing nonlinear modulators. While in analog audio power amplifiers the modulator is essentially linear and compensation of all the nonlinearities in the power amplifier stage is performed via the feedback, fully digital audio power amplifiers can account and precompensate for the nonlinearities of the subsequent stages in the digital modulator, which makes possible high performance operation of the aforementioned strongly nonlinear amplifiers even without any feedback.

The work presented in this section will focus entirely on the design of a nonlinear digital modulator for the double-boost SICAM. For most of the time, the implementation of the digital modulator follows the guidelines for the design of digital modulators for Class D audio power amplifiers given in [14], [42], [43], [44]. This means that digital modulator is implemented using oversampling and noise shaping within $\Sigma - \Delta$ modulator to reduce the digital code resolution without any adverse effects on the Signal-to-Noise Ratio (SNR) within the audio band. The reduction of the resolution i.e. the number of bits b alleviates the practical implementation of the digital PWM ($DPWM$), by using lower clock rates and reducing power consumption in the latter. In order to account for the nonlinearity of the subsequent double-boost SICAM with nonlinear output characteristics, the design of a special digital precompensator will be described.

4.2.1 Implementation of the digital modulator

The complete digital modulator is depicted in Fig. 4.3.

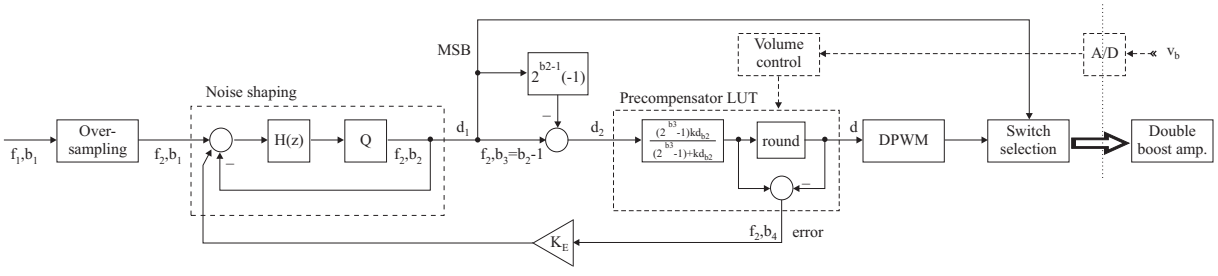

Fig. 4.3. Digital modulator for the double-boost SICAM

As shown in Fig. 4.3, the audio PCM bitstream enters the oversampler, where the wordlength is maintained and sampling rate is changed from f_1 to f_2:

$$f_2 = OSR \cdot f_1 \tag{4.4}$$

where OSR is the oversampling rate. In this way, the new sampling rate f_2 becomes significantly higher than the signal bandwidth f_b, $f_b \ll f_2/2$, so the same quantization noise associated with the bit resolution of b_1 is evenly redistributed within the new Nyquist bandwidth $f_2/2$ to yield much better SNR within the signal bandwidth f_b. Another advantage of the oversampling is that there is enough space to perform noise shaping with $\Sigma - \Delta$ modulators, where the noise within the signal bandwidth f_b is reduced on behalf of large increase of the noise out of the signal bandwidth. The amount of oversampling OSR depends on the particular application, but for the portable audio amplification there are at least three reasons that make high OSRs appealing:

- Portable devices need low power audio power amplifiers, in a range of few Watts. For such applications, active power devices are likely to be very small and integrated on a single silicon chip, so they can operate with very high switching frequencies and tolerable switching losses, which in turn reduces the size of the output filter,
- With high OSRs, the nonlinear effects of Uniform PWM (UPWM) become negligible and there is no need for correction algorithms [14], which significantly simplifies the whole design,
- Another advantage of the high OSRs is that very good SNR can be obtained even with lower order of the noise filter $H(z)$ in the $\Sigma - \Delta$ modulator, which does not only save significant amount of hardware, but also makes the modulator stable with higher modulation indexes.

For example, the target can be to implement a digital modulator with high OSR of 64x or 128x with just a second order noise shaping, which is conditionally stable for all modulation indexes. The use of first order noise shaping in audio applications is usually avoided due to the pronounced idle tones.

At the output of the $\Sigma - \Delta$ noise shaper, the bit resolution is decreased from b_1 to b_2 bits in the quantizer Q by taking just b_2 of the most significant bits, usually in the range of 4 to 8 bits. In contrast with the 1-bit $\Sigma - \Delta$ modulators where the effective gain of the quantizer Q is ill-defined and strongly depends on the dynamics of the input signals (higher input signal amplitude $\Rightarrow$ less gain), the effective gain of the quantizer Q in the case of higher resolution $\Sigma - \Delta$ noise shapers is much better defined, which alleviates the design process and improves its stability.

So far, the proposed digital modulator has the form of a conventional digital modulator for Class D audio power amplifier. The output of the $\Sigma - \Delta$ noise shaper represents the duty cycle d_1, which in conventional full-bridge Class D audio power amplifier is proportional to the output voltage $v_o = (1 - 2d_1)V_{ps}$. This duty cycle d_1, however, cannot be used directly in a double-boost SICAM. The polarity of the amplified signal determines the mode of operation of the switches, according to Table 4.1, and within each mode of operation the duty cycle d moves independently between 0 and 1, $0 \leq d \leq 1$. Therefore, it is of utmost importance to define the digital code which corresponds to the zero of the audio signal, in order to select the proper mode of operation (positive or negative output voltage) and determine the duty cycle. Duty cycle is represented by the distance from the zero code to the waveform. For midriser ADCs, the zero of the audio signal corresponds to two neighboring digital codes (01...1 and 10...0), while in midtread ADCs, this corresponds to a single digital code (10...0). For midtread ADCs, situation with 4-bit resolution is shown in Fig. 4.4. d_{b1} and d_{b2} are the binary, digital representations of the duty cycles d_1 and d_2, $0 \leq d_1, d_2 \leq 1$.

With midtread ADCs, where the zero code is situated at 10...0, selection of the operation mode can be made simply by looking at the Most Significant Bit (MSB). Therefore

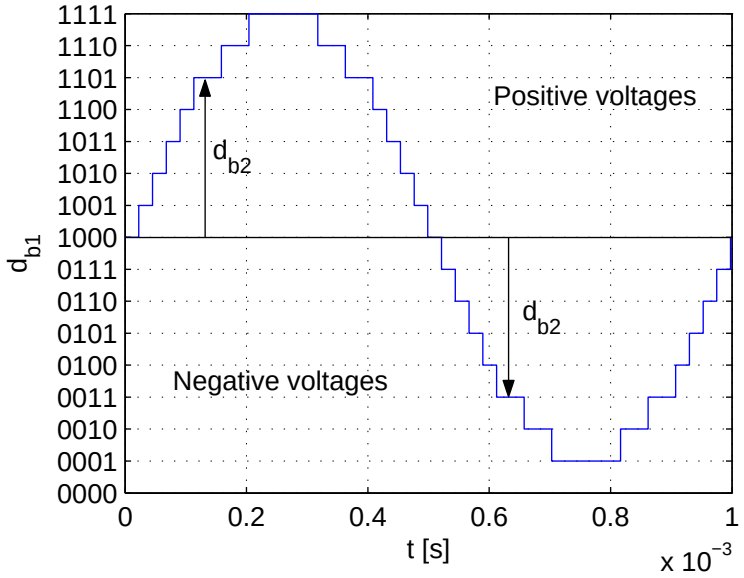

Fig. 4.4. Digitized sinewave with corresponding duty cycles for double-boost SICAM

in the subsequent DPWM stage only $b_3 = b_2 - 1$ bits of the duty cycle d_1 are used, but the effective resolution is still b_2 bits. Input duty cycle d_2 to the precompensator module for midtread ADC is calculated in the following way:

$$d_{b2} = \begin{cases} d_{b1} - 2^{b_2-1} \ , & d_{b1} \geq 2^{b_2-1} \\ 2^{b_2-1} - d_{b1} \ , & d_{b1} < 2^{b_2-1} \end{cases} \tag{4.5}$$

which corresponds to taking the Least Significant Bits (LSBs) after the MSB for positive output voltages, and taking the two's complement of the same LSBs for negative output voltages. For midriser ADC, precompensator input duty cycle d_2 is calculated by:

$$d_{b2} = \begin{cases} d_{b1} - 2^{b_2-1}(-1) \ , & d_{b1} \geq 2^{b_2-1}(-1) \\ 2^{b_2-1}(-1) - d_{b1} \ , & d_{b1} < 2^{b_2-1}(-1) \end{cases} \tag{4.6}$$

which has the same effect upon d_1 like the above mentioned one, with the additional remark that at each sampling instant the zero code alternates between $2^{b_2-1} - 1$ and 2^{b_2-1} (01...1 and 10...0, represented by (-1) in (4.6)). This has the average effect of precisely positioning the zero code between the two neighboring digital codes, which can be compared with the effect of dithering, but in a very deterministic way. Of course, randomly positioning the zero code between the two adjacent digital codes is also possible, with slight complications in hardware.

Static output transfer function of the double-boost SICAM (4.3) shows strongly nonlinear behavior. In Fig. 4.5, this output characteristic is compared with the buck-type Class D amplifier. In the same diagram, dashed line represents the desired output characteristic, which is linear like in the buck-type Class D amplifier and is higher at the ends than the battery voltage v_b like in the double-boost SICAM.

In order to linearize the strongly nonlinear static transfer function of the double-boost SICAM (4.3), a goal is set to make the output voltage v_o of the double-boost SICAM exhibit linear relationship with the duty cycle d_2:

$$v_o = \frac{d}{1-d} v_b = k d_2 v_b \tag{4.7}$$

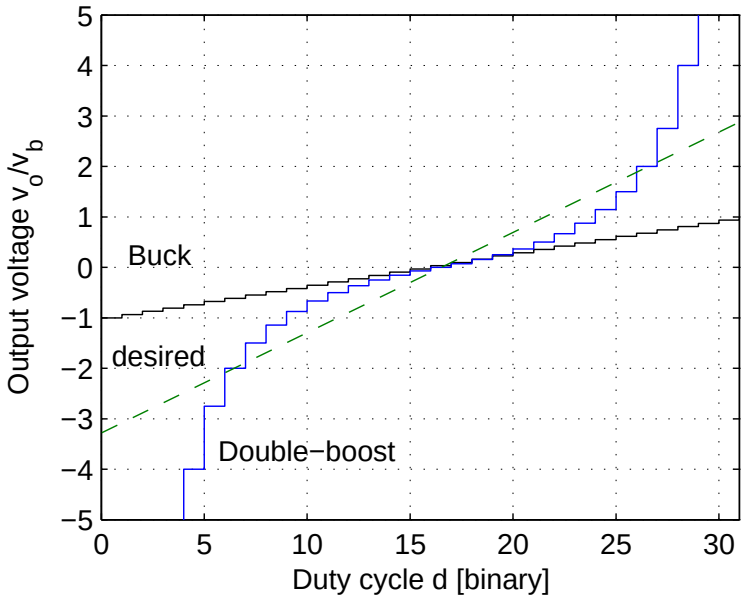

Fig. 4.5. Static transfer functions of the buck converter and double-boost SICAM

which leads to the following equation for the precompensator operation:

$$d = \frac{kd_2}{1 + kd_2} \tag{4.8}$$

or when the duty cycle is represented by integer numbers in the digital implementation:

$$d_b = round\left(\frac{(2^{b_2-1} - 1)kd_{b2}}{(2^{b_2-1} - 1) + kd_{b2}}\right) \tag{4.9}$$

where d_b and d_{b2} are binary, digital representations of d and d_2, and $round()$ represents the rounding operation.

The meaning of the parameter k is to adjust the maximum output voltage with full duty cycle, and for boosting operation it is always selected $k > 1$. In Fig. 4.5, it is equal to $k = 3$.

Due to the finite resolution of both d_b and d_{b2}, it is not possible to accurately calculate the division in (4.8), which inherently leads to error very similar to the quantization error. For the case $k = 3$, the precompensator Look-Up Table (LUT) is given in Table 4.2, where the exact $error$ and the quantized $error_b$ with $b_4 = 2$ bits resolution are defined as:

$$\begin{aligned} error &= \frac{(2^{b_2-1} - 1)kd_{b2}}{(2^{b_2-1} - 1) + kd_{b2}} - d_b \\ error_b &= \begin{cases} 1\,, & error > 0 \\ 0\,, & error = 0 \\ -1\,, & error < 0 \end{cases} \end{aligned} \tag{4.10}$$

The output characteristic of the precompensated double-boost SICAM is shown in Fig. 4.6. It is visible that the linearization through precompensation is not complete, due to the introduced error when calculating the precompensated duty cycle d.

Error caused by the division in (4.8) and finite resolution of the duty cycles is shown in the third column of Table 4.2. It has a form of quantization error, so it is very similar to the error caused by reducing the word length within the $\Sigma - \Delta$ noise shaper. Latter error has been effectively rejected within the signal band by feeding back the new duty cycle

d_{b2}	d_b	$error$	$error_b$ (2 bits)
0	0	0	0
1	3	-0.5000	-1
2	4	0.2857	1
3	6	-0.3750	-1
4	7	-0.3333	-1
5	8	-0.5000	-1
6	8	0.1818	1
7	9	-0.2500	-1
8	9	0.2308	1
9	10	-0.3571	-1
10	10	0	0
11	10	0.3125	1
12	11	-0.4118	-1
13	11	-0.1667	-1
14	11	0.0526	1
15	11	0.2500	1

Table 4.2. Precompensator Look-Up Table (LUT) for $k = 3$

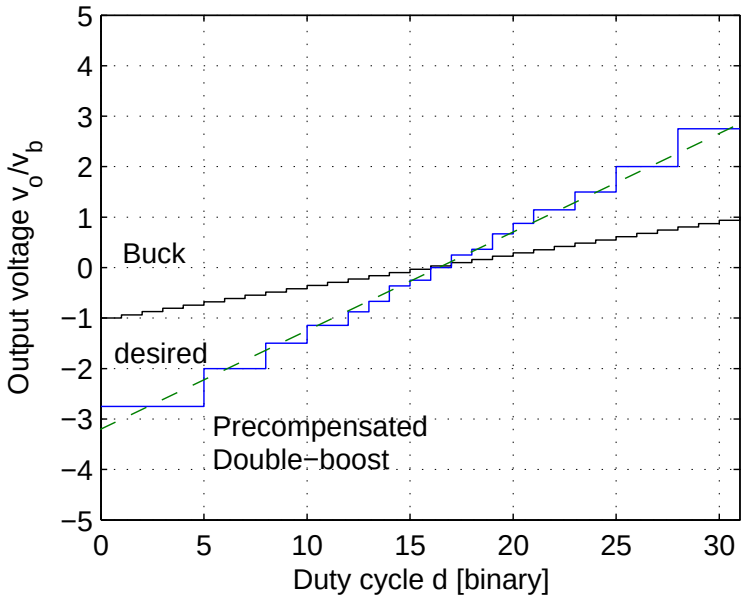

Fig. 4.6. Static transfer functions of the buck converter and precompensated double-boost SICAM

with reduced word length back to the noise shaping filter. The same idea can be used for the former division error $error$, so the digitized error $error_b$ from the precompensator LUT can be brought back to the $\Sigma - \Delta$ noise shaper for correction, after being multiplied with corresponding gain K_E.

Digitized error $error_b$ can be represented by arbitrary number of bits b_4, with $b_4 = 2$ being the minimum number of bits for implementation. Digitizing the error with more than two bits leads to better performance, but also requires bigger LUT and therefore more hardware.

At the same time, by calculating several LUTs like the one in Table 4.2 for different linearization coefficients k, volume control in several steps can be implemented by simply switching among the LUTs corresponding to increasing or decreasing k. Unfortunately, when moving to small k with input duty cycles d_2 spanning the whole range, the output duty cycle d starts to "exercise" just few DPWM levels, which in turn significantly worsens the resulting SNR and reduces dynamic range.

Much better approach for volume control and stabilizing the output voltage v_o despite of the changes in the battery voltage v_b is to use slow and cheap A/D converter measuring the battery voltage v_b. By intentionally decreasing or increasing the digital code corresponding to the measured battery voltage, the digital modulator can be "fooled" to reduce or increase the output duty cycle d, thus achieving effective volume control.

Finally, the switch selector block in Fig. 4.3 redirects the precompensated duty cycle d to the selected set of switches according to the output voltage polarity, as shown in Table 4.1. This block can also incorporate the necessary blanking or dead times, if they are not implemented in the MOSFET drivers.

4.2.2 Precompensator noise

As it was already mentioned, the error (4.10) introduced at the output of the precompensator LUT is essentially quantization noise, i.e. a result of the inability of the precompensator LUT to accurately represent the result of the division in (4.8) due to the finite resolution of the duty cycle d_b.

The similarity of the latter error with the quantization error at the output of the $\Sigma-\Delta$ noise shaper is just in the mechanism of creation, but the effects are rather different. The usual assumption in $\Sigma-\Delta$ modulators is that the quantization noise is evenly spectrally distributed i.e. it is white noise, which becomes increasingly coarse definition as the number of output bits in the $\Sigma-\Delta$ modulator is decreased. This simplification enables simple linear representation of the $\Sigma-\Delta$ modulator as gain followed with a noise summation point [43] and leads to rather simple derivation of the corresponding Signal Transfer Function (STF) and Noise Transfer Function (NTF).

Precompensator noise on the other hand is likely to be strongly colored, so calculating its RMS value is not so straightforward. The approach undertaken here is to open the error feedback loop from precompensator LUT to the $\Sigma-\Delta$ noise shaper and calculate the error RMS value as a result just of the inaccurate mapping of the input to the output duty cycles in the precompensator. The noise due to the reduced number of bits is already accounted for in the $\Sigma-\Delta$ modulator noise and in the case of ideal precompensation of the nonlinearity of the double-boost SICAM in (4.3) via the duty cycle transformation (4.8), the aforementioned $\Sigma-\Delta$ quantization noise will just appear in the output voltage scaled by the amplification factor k of the power stage.

The amplitudes of the division error (4.10) at the output of the precompensator for each and every input duty cycle can be easily calculated as shown in Table 4.2. The only unknown when calculating the noise RMS value is therefore the time intervals of each of the errors. The number of levels in the quantized sinusoidal waveform in Fig. 4.4 corresponding to changes in the duty cycle d_{b2} is:

$$N_l = 2^{b_2-1} \tag{4.11}$$

With midtread representation of the digital code, the zero of the reference sinewave is situated at (10...0) i.e. at 2^{b_2-1} and the properly scaled sinewave function will have the following form:

$$y = M(2^{b_2-1} - 0.5)sin(\omega_m t) \tag{4.12}$$

where M is the modulation index, $(2^{b_2-1} - 0.5)$ is the maximum value of the reference sinewave and ω_m is the modulation angular frequency.

As a result of the rounding to the nearest integer performed in the quantizer of the $\Sigma-\Delta$ noise shaper, the start time instant t_{ns} and the end time instant t_{ne} of the n^{th} level in the digitized sinewave coincide with the instants when the waveform encounters:

$$\begin{aligned} y_{1s} &= 0 & y_{1e} &= 0.5 \\ y_{2s} &= 0.5 & y_{2e} &= 1.5 \\ y_{3s} &= 1.5 & y_{3e} &= 2.5 \\ &... & &... \\ y_{ns} &= n - 1.5 & y_{ne} &= n - 0.5 \end{aligned} \tag{4.13}$$

which leads to the following equalities:

$$\begin{aligned} M(2^{b_2-1} - 0.5)sin(2\pi f_m t_{ns}) &= n - 1.5 \\ M(2^{b_2-1} - 0.5)sin(2\pi f_m t_{ns}) &= n - 0.5 \end{aligned} \tag{4.14}$$

and the following expressions for the time instants t_{ns} and t_{ne}:

$$\begin{aligned} t_{ns} &= \frac{1}{2\pi f_m} \arcsin\left(\frac{n - 1.5}{M(2^{b_2-1} - 0.5)}\right) \\ t_{ne} &= \frac{1}{2\pi f_m} \arcsin\left(\frac{n - 0.5}{M(2^{b_2-1} - 0.5)}\right) \\ \Delta t_n &= t_{ne} - t_{ns} \end{aligned} \tag{4.15}$$

It should be noted that when complex numbers are obtained for the time instants in (4.15) this essentially means that there is no intersection point with the sinewave and the corresponding n^{th} digital level is not used at all, $t_{ns} = t_{ne} = 0$. On other hand, for the first level $t_{1s} = 0$ and for the last used digital level l with non-zero duration $t_{le} = T_m/4$.

To all of the time intervals Δt_n corresponding to the duration of the corresponding n^{th} digital level, division errors like those in Table 4.2 can be associated and this repeats four times per sinewave period, due to the quarter-wave and half-wave symmetry. Thus, the precompensator noise RMS value is calculated using the following expression:

$$e^2_{pr,rms} = \frac{1}{T_m}\int_0^{T_m} error^2(t)dt = 4f_m \sum_{n=1}^{N_l} error_n^2 \Delta t_n \tag{4.16}$$

Precompensator RMS noise levels $e_{pr,rms}$ with $b_2 = 5$ as a function of the modulation index M and the amplifier gain k are depicted in Fig. 4.7. It is clearly visible that the error exhibits minimums for certain amplifier gains k, when the division error is minimal because the digitized duty cycles are very close to the ideal ones obtained with infinite resolution. This gives rise to the idea that for the same output power level, a particular combination of modulation index M and amplifier gain G can be found which leads to best SNR and lower THDN.

4.2.3 Simplified control block diagram

The simplified control block diagram of the proposed digital control for double boost SICAM with all the associated transfer functions is shown in Fig. 4.8.

The main two blocks at the control diagram are the $\Sigma - \Delta$ noise shaper and the precompensator LUT.

The dynamics of the $\Sigma - \Delta$ noise shaper can be easily represented by the gain of the quantizer c and two linear transfer functions - Signal Transfer Function $STF_{\Sigma\Delta}$ and Noise Transfer Function $NTF_{\Sigma\Delta}$:

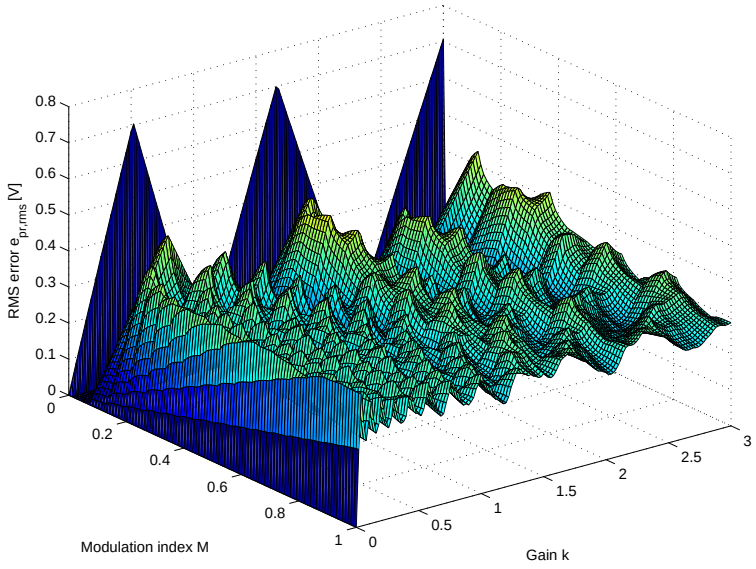

Fig. 4.7. Precompensator RMS noise levels $e_{pr,rms}$ with $b_2 = 5$

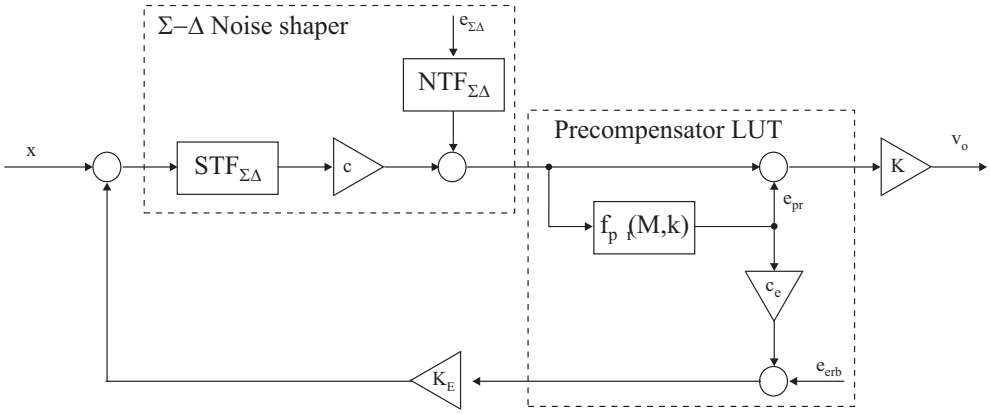

Fig. 4.8. Simplified control block diagram of digitally controlled double-boost SICAM

$$\begin{aligned} STF_{\Sigma\Delta}(z) &= \frac{H(z)}{1+H(z)} \\ NTF_{\Sigma\Delta}(z) &= \frac{1}{1+H(z)} \end{aligned} \tag{4.17}$$

where $H(z)$ is the noise loop filter from Fig. 4.3.

The useful signal x comes out of the $\Sigma - \Delta$ modulator after being low-pass filtered in the audio band by the $STF_{\Sigma\Delta}$ and amplified by the quantizer Q gain c. At the same time, the quantization error $e_{\Sigma\Delta}$ is assumed to be white noise and thus not correlated with the input signal x, so it is represented by an independent and separate input. Before summing it with the useful signal at the output of the $\Sigma - \Delta$ noise shaper, this quantization error is high-pass filtered by the $NTF_{\Sigma\Delta}$, which essentially removes the bulk of the noise from the audio band and pushes it to higher frequencies in an extended range provided by the oversampling.

As already mentioned in Section 4.2.2, it can be assumed that the high-pass filtered quantization noise $e_{\Sigma\Delta}$ from the noise shaper appears straightforward in the output voltage after being amplified by the linearized double-boost SICAM gain k. The division error e_{pr} from the precompensator LUT is summed with the useful signal and the quantization noise from the $\Sigma - \Delta$ noise shaper just before the amplification k in the double-boost

SICAM, but its dependance on the precompensator input signal is a complex nonlinear function of the modulation index M and linearized amplifier gain k, as already shown in Section 4.2.2. Part of that division error is being returned back to the $\Sigma-\Delta$ noise shaper, but as a result of the quantization of the aforementioned error, additional noise e_{erb} is injected in the feedback loop. Finally, the quantized division error $error_b$ is amplified by the feedback gain K_E and enters the $\Sigma-\Delta$ noise shaper. What is expected here is that by the action of the noise loop filter $H(z)$ in the $\Sigma-\Delta$ noise shaper some of the precompensator division error will be rejected in the audio band and some of the noise will be shifted to inaudible frequencies. Since the input signal to the precompensator contains both the processed useful signal x and quantization error $e_{\Sigma\Delta}$ from the $\Sigma-\Delta$ noise shaper, they both affect the precompensator division error e_{pr} and thus are fedback for second time to the $\Sigma-\Delta$ noise shaper. However, the effects of this additional feedback on rejection of quantization error $e_{\Sigma\Delta}$ and precompensator division error e_{pr} are very difficult to study analytically and thus extensive simulation results will be presented in the next section.

4.3 Simulation of the double-boost SICAM with digital modulator

In order to compare the performance of the double-boost SICAM with the proposed digital modulator with and without feedback from the precompensator LUT to the $\Sigma-\Delta$ modulator, a set of simulations in Matlab Simulink was performed. The digital modulator uses already oversampled 1 kHz sinewave with variable modulation index, resolution of b_1 =16 bits and sampling frequency of f_2 =1.024 MHz. $\Sigma-\Delta$ modulator is 2nd order with CRFB (cascade of resonators in feedback) structure shown in Fig. 4.9, reducing the word length to b_2 =5 bits. The optimal second order Noise Transfer Function (NTF) for OSR=128 was obtained using the $synthesizeNTF$ function from the $\Delta-\Sigma(delsig)$ toolbox for Matlab [45]:

$$NTF=\frac{z^2-2z+1}{z^2-1.225z+0.4415} \tag{4.18}$$

leading to the following noise-shaping filter function

$$H=\frac{0.775z-0.5585}{z^2-2z+1} \tag{4.19}$$

which encompasses one delay z^{-1} from the input to the output and thus renders the digital system realizable .

CRFB noise shaper coefficients are obtained by using $realizeNTF$ function from the same Matlab toolbox, leading to optimal coefficients given in Table 4.3. To simplify the practical implementation, these coefficients were rounded to the nearest fraction with power-of-two denominator, as given in Table 4.3. NTF with rounded coefficients becomes:

$$NTF=\frac{z^2-2z+1}{z^2-1.25z+0.5} \tag{4.20}$$

Some of the waveforms and numerical results of the normalized output voltage v_o/v_b are shown in Fig. 4.10 to Fig. 4.16, with the details for the modulation index M, coefficient k and number of bits b_4 given in the title of the figures.

By comparing Fig. 4.10 and Fig. 4.11, as well as Fig. 4.12 and Fig. 4.14, it becomes apparent that closing the feedback with the duty cycle error from the precompensator

	a_1	a_2	g_1	b_1	b_2	b_3	c_1	c_2
optimal	0.2162	0.5585	0	0.2162	0.5585	1	1	1
rounded	0.25	0.5	0	0.25	0.5	1	1	1

Table 4.3. Optimal and rounded CRFB noise-shaper coefficients

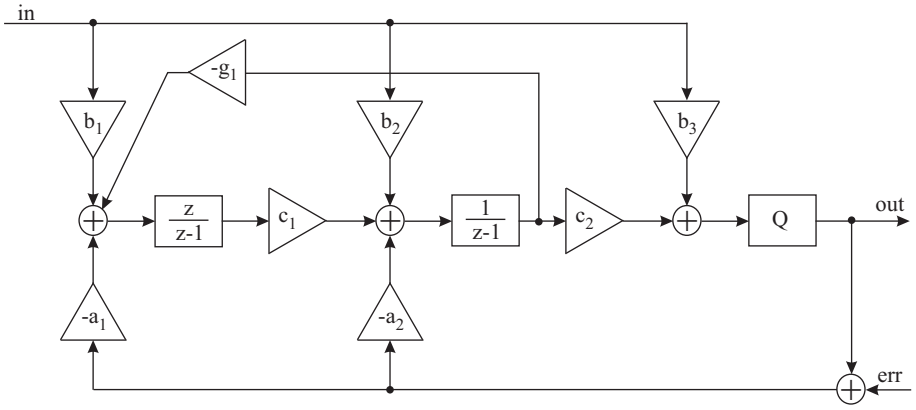

Fig. 4.9. CRFB $\Sigma - \Delta$ noise-shaper structure

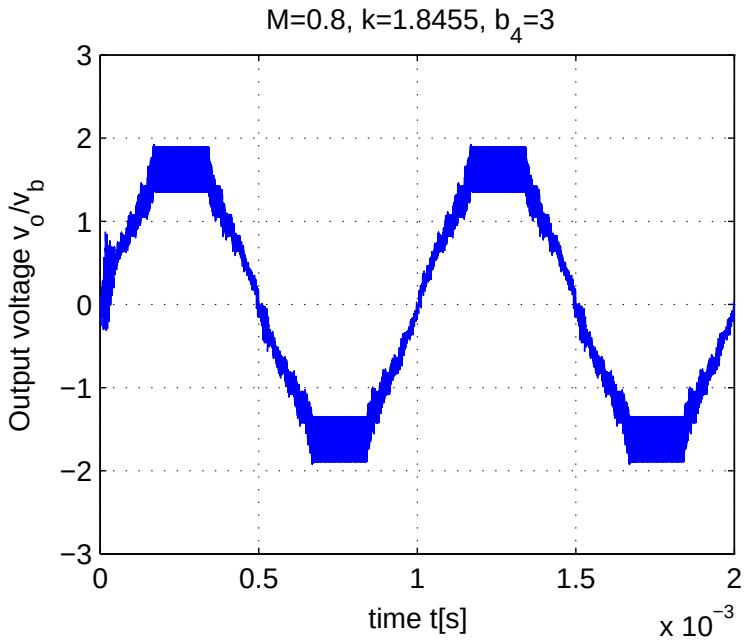

Fig. 4.10. Normalized output voltage v_o/v_b of the fully-digital double-boost SICAM without feedback from the precompensator

LUT to the summing point of the $\Sigma - \Delta$ noise shaper significantly improves the linearity of the double-boost SICAM. In terms of THD+N, latter is almost halved by introducing the feedback.

The effects of changing coefficient k on the double-boost SICAM with digital modulator with and without feedback from the precompensator are shown in Fig. 4.13 and Fig. 4.15. As mentioned earlier, using different LUTs calculated for different coefficients k as volume control has an adverse effect on the THD+N results.

Finally, the performance of the digital modulator with different resolution for the division error b_4 is shown in Fig. 4.16. It seems like $b_4 = 3$ bits is the optimal choice on "performance/size of LUT" scale.

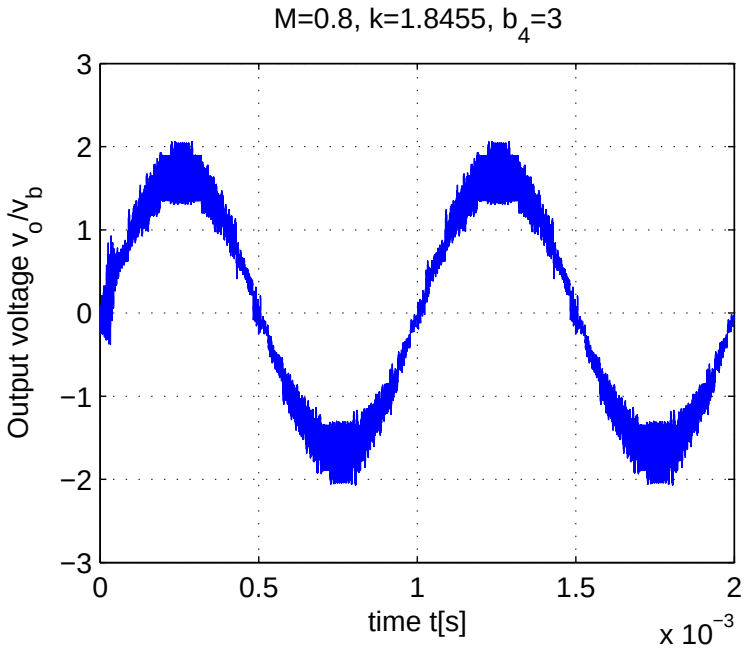

Fig. 4.11. Normalized output voltage v_o/v_b of the fully-digital double-boost SICAM with feedback from the precompensator

4.4 Conclusion

Switching-mode audio power amplifiers with output voltage step-up characteristics based on the boost and buck-boost converters are very appealing solution for portable, battery

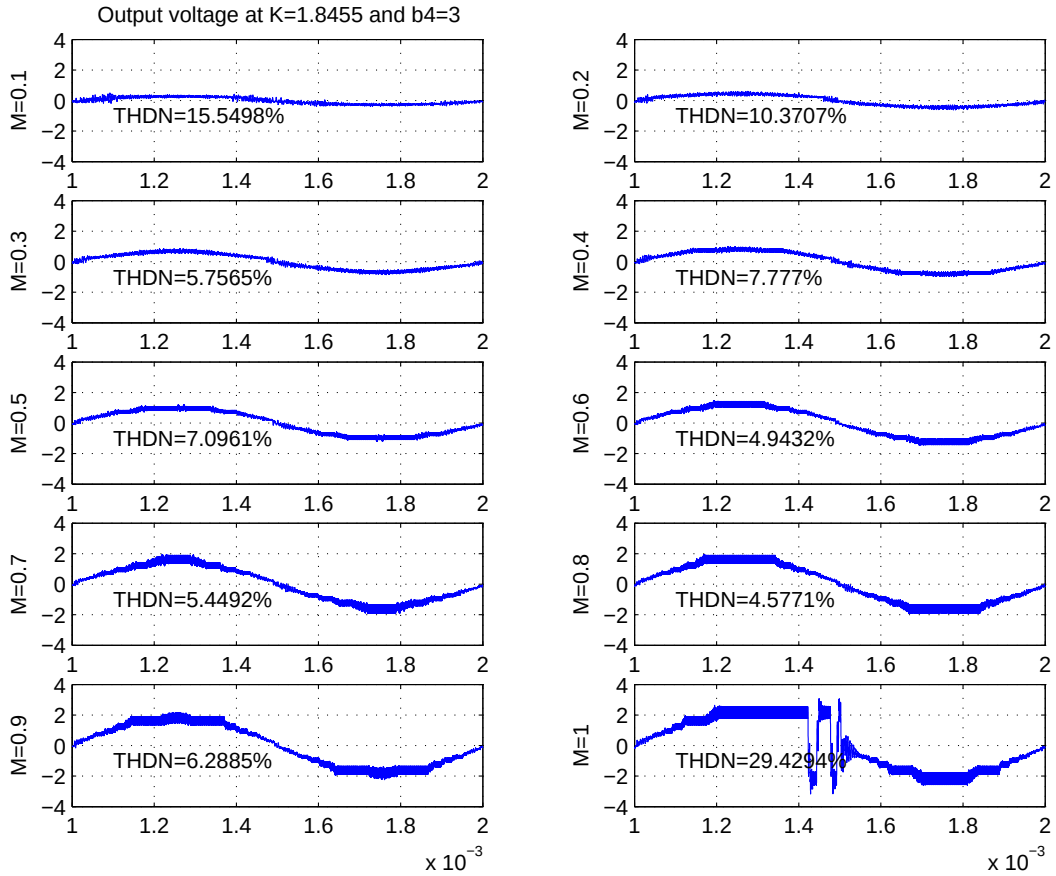

Fig. 4.12. Normalized output voltage v_o/v_b of the fully-digital double-boost SICAM without feedback from the precompensator as a function of the modulation index M

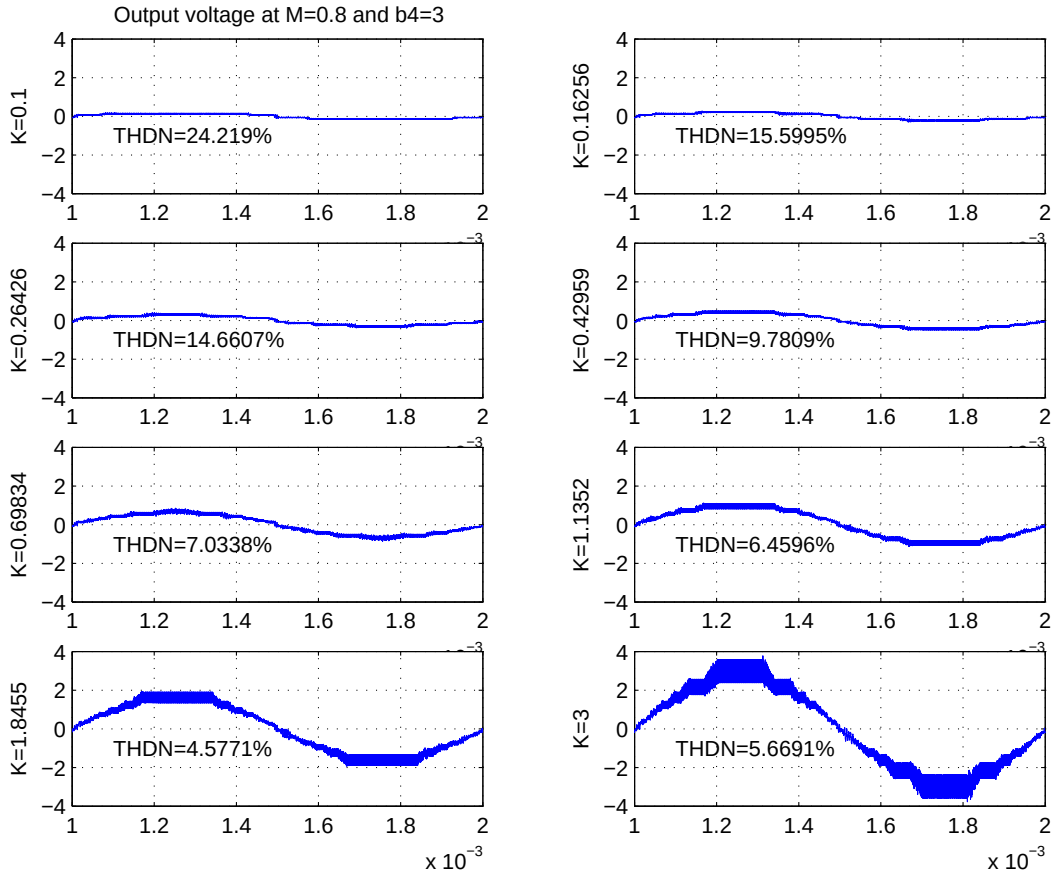

Fig. 4.13. Normalized output voltage v_o/v_b of the fully-digital double-boost SICAM without feedback from the precompensator as a function of the selected linearizing coefficients k

powered devices. One of them, the so called double-boost SICAM or push-pull boost converter was presented in this chapter. The main obstacle towards its greater acceptance is its very nonlinear static transfer function, as well as the need for two separate inductors, which are very difficult to integrate in Integrated Chip (IC) solution.

Along with the double-boost topology and its DC and AC small-signal analysis, a new digital modulator was presented, which is capable of linearizing the open-loop transfer function from the digital audio input to the output voltage. It consists of an oversampler, $\Sigma - \Delta$ noise shaper for reducing the data word length, precompensaion unit in a form of LUT which maps the incoming duty cycles into a set of linearizing outgoing duty cycles, as well as a DPWM unit and switch selector. In order to improve the level of linearization of the output characteristics, the division error when calculating the linearizing duty cycles is fed back into the $\Sigma - \Delta$ noise shaper. An extensive set of simulations is performed to verify the operation of the double-boost SICAM with the proposed digital modulator with and without feedback from the precompensator unit.

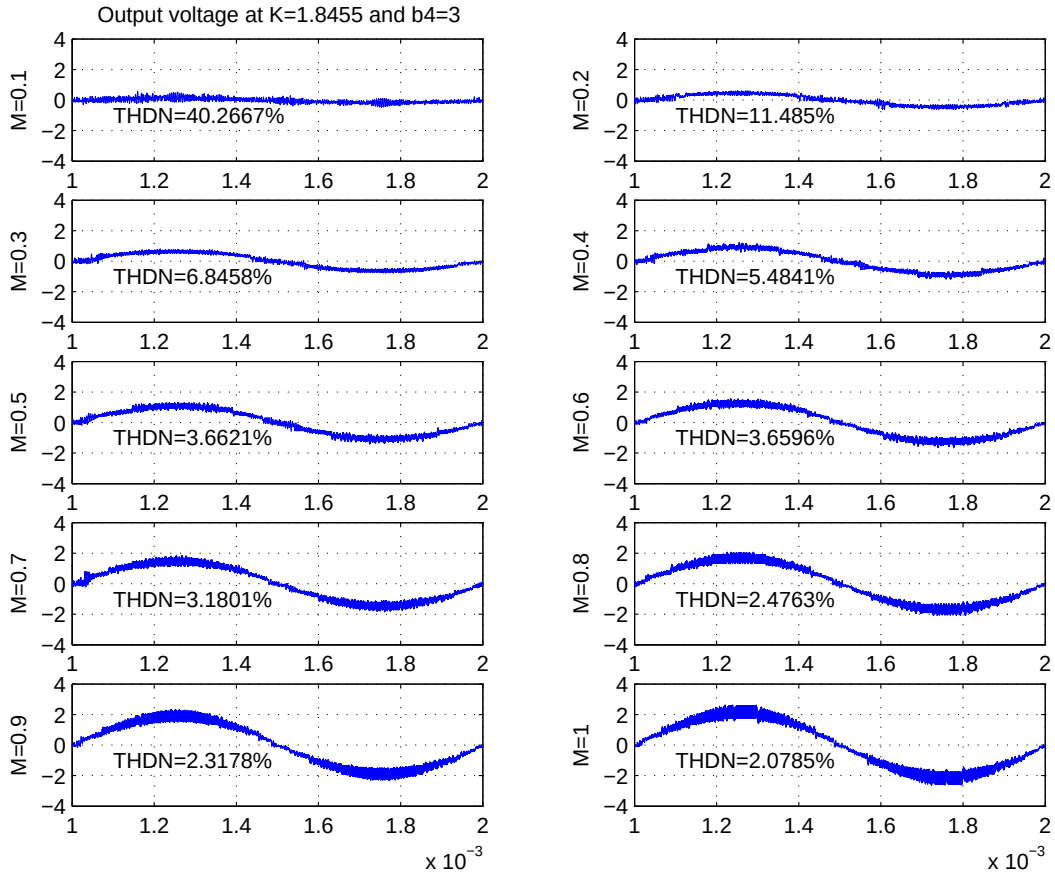

Fig. 4.14. Normalized output voltage v_o/v_b of the fully-digital double-boost SICAM with feedback from the precompensator as a function of the modulation index M

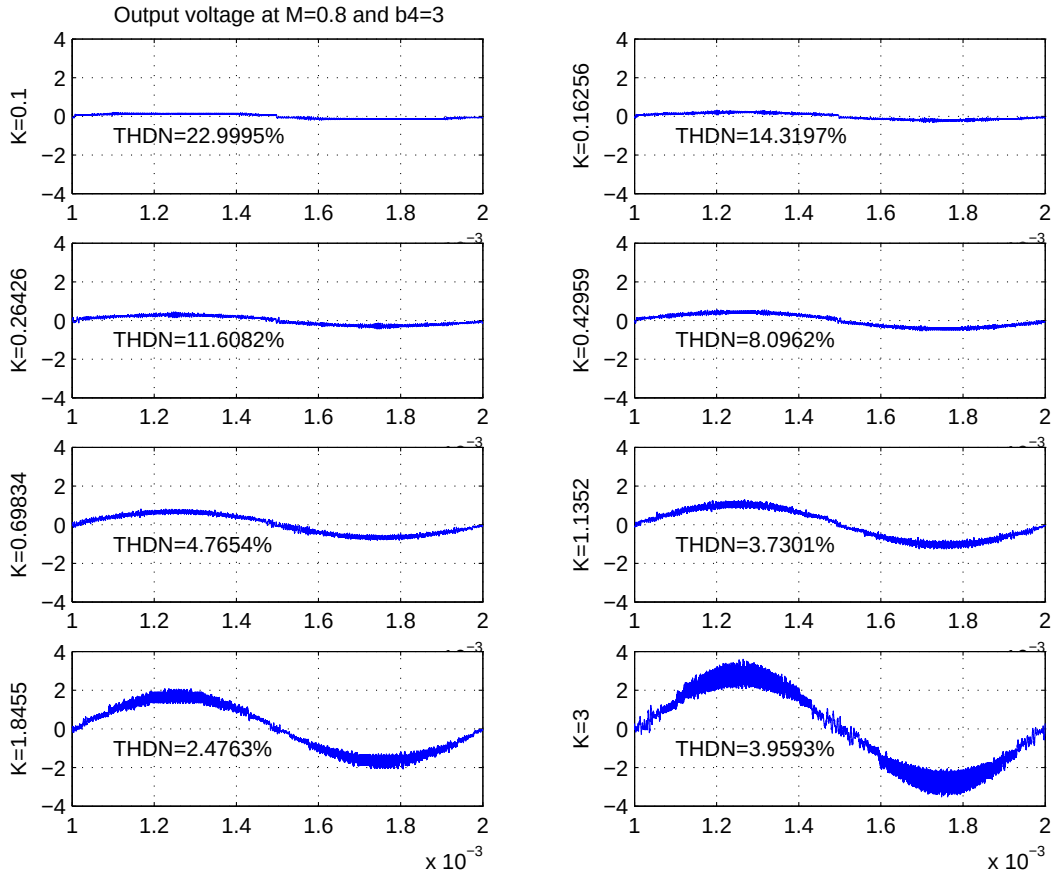

Fig. 4.15. Normalized output voltage v_o/v_b of the fully-digital double-boost SICAM with feedback from the precompensator as a function of the selected linearizing coefficients k

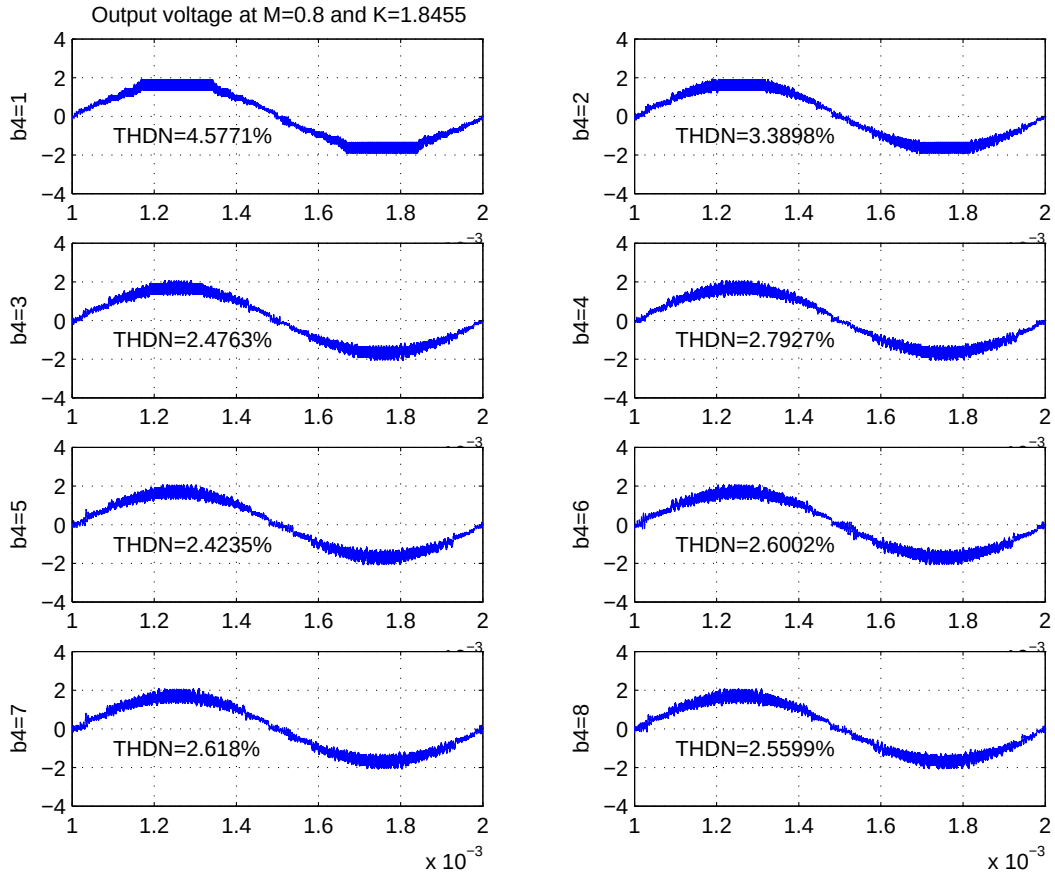

Fig. 4.16. Normalized output voltage v_o/v_b of the fully-digital double-boost SICAM with feedback from the precompensator as a function of the number of bits b_4

Part II

Isolated SICAMs

5

Introduction to isolated SICAMs

"How wonderful that we have met with a paradox. Now we have some hope of making progress."

- Niels Bohr

The greatest part of the research and prototyping work within the SICAM project was done in the field of isolated SICAMs. And that is not peculiar, since the roads to non-isolated single-stage switching-mode audio power amplification presented in Part I seem somewhat straightforward. On the other hand the requirement for providing isolation in a form of a transformer has tremendous impact on the possible SICAM solutions and the level of engineering effort needed. Isolated SICAMs are also a safety requirement whenever there is a possibility for the user to touch on purpose or unintentionally some of the metal parts of the amplifier, which will be most often the case.

All of the SICAM solutions and topologies which will be subject of investigation in the next chapters will use bridge rectifier for the AC-mains voltage and DC storage capacitor for intermediate energy storage during the periods with low input voltage. It is believed that this solution is the most cost effective solution for overcoming the power supply problems from a single-phase AC-mains utility grid. Therefore the goal of constructing a SICAM represents in fact a challenge of designing compact isolated DC-AC converters.

This introductory chapter will predominantly deal with the basic energy conversion principles for isolated power converters utilizing small High Frequency (HF) transformers. The structure of the proposed isolated SICAM solution based on HF-link converter will be briefly described, with a special focus on the use of so called bidirectional or four-quadrant (4Q) switches in the output stage. At the end, thorough patent investigation in the field of isolated direct converters with HF-link will be given.

5.1 Conventional solution with isolated SMPS and Class D audio power amplifier

The conventional Class D audio power amplifier with switching-mode power supply is shown in Fig. 5.1. On the mains side, line rectifier charges a large capacitor A, which is used to store energy from the line and overcome the problems of regular input voltage zero-crossings, i.e. it averages the input power, as already described in Section 3.1. In order to be able to use small isolation transformer, the inverter on the input side of the power supply is driven with high-frequency gate signals to reduce the amount of magnetic flux swing. On the secondary side, transformer voltage is rectified once again and well filtered, so that the stiff intermediate DC-bus with bulky capacitor B is used to interface with a Class D audio power amplifier. This makes it easy for the amplifier to achieve excellent audio performance, although its Power Supply Rejection Ratio (PSRR), which quantifies the ability of the Class D amplifier to hinder power supply perturbations from appearing in the audio output, may be low. It is however clear that this conventional solution features unnecessary redundancy and complexity, like for example the two energy

buffering capacitors A and B instead of just one on the input side, as well as multiple and separate control loops around the power supply and the Class D amplifier. It should be stressed that despite of the redundancy of capacitor B with regard to overcoming the regular input voltage zero crossings, it is of ultimate importance for Class D amplifier operation since it helps the DC bus maintain constant voltage and provide path for the reactive load current. At the same time, the energy flow is unidirectional throughout the whole power supply, while the bidirectional power flow is kept just between the power supply output capacitor B and the Class D audio power amplifier. This leads to a common problem when reproducing low frequency signals with single-ended audio power amplifiers known as power supply pumping [46], where the capacitors B in the intermediate DC bus are asymmetrically charged and discharged leading to imbalance and improper operation.

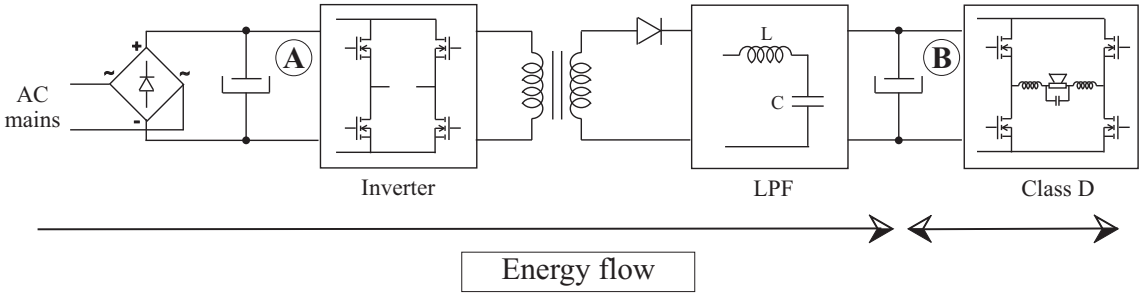

Fig. 5.1. Conventional Class D audio power amplifier with isolated SMPS

5.2 Isolated audio power amplification through HF-link conversion

The direct non-isolated energy conversion approach without any reactive components, except for filtering purposes, has been successfully utilized in three-phase matrix converters [19]. In the aforementioned converters the output voltage and frequency can be easily adjusted by using bidirectional switches and the three-phase utility grid provides continuous power flow. Unfortunately, the single-phase utility grid limits the applicability of the matrix converter, since the regular zero crossings of the input voltage ask for some sort of input side energy buffering. Therefore, SICAMs cannot be made in a single stage and without any reactive components, but nonetheless the solution allows for direct energy conversion in two closely dedicated and interconnected stages.

When isolation from the mains is mandatory, High Frequency (HF) -link converters [47], [48] represent an interesting alternative, which is also applicable for a single-phase grid. Single-phase direct converters, like the one shown in Fig. 5.2, can use the same mains rectifier with energy storage capacitor A like the conventional audio power amplifier, but the intermediate DC bus with the rectifiers and the associated Low-Pass Filter (LPF) on the secondary side has been replaced with a high frequency AC link. As a result of this transformation there is one energy conversion less when compared to the conventional solution, but the audio power amplifier is more complex, since it incorporates bidirectional switches capable of blocking both transformer voltage polarities and conducting in both current directions. A bidirectional bridge asks for advanced control techniques for commutating the load current between the incoming and outgoing switches, since there is no diode freewheeling path as in conventional Class D amplifiers. Nonetheless, the approach

is feasible and has been reported with regard to converters for Uninterruptible Power Supplies (UPS) and renewables [49], [50], [51].

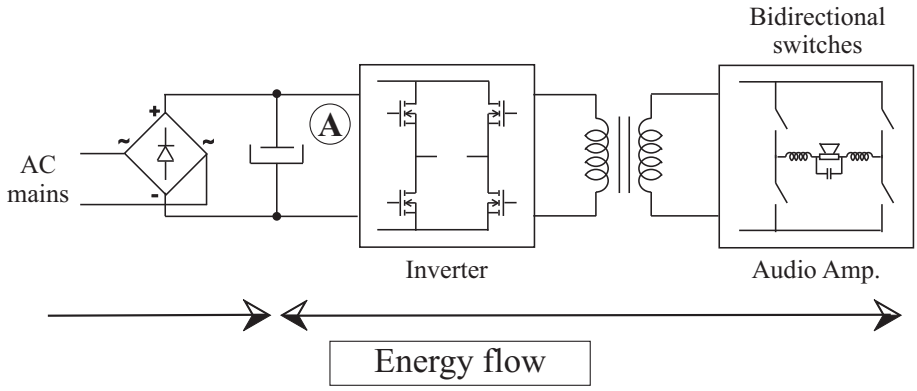

Fig. 5.2. Direct conversion audio power amplifier

Another advantage of the direct energy conversion amplifier is that the energy flow is bidirectional over the HF-link i.e. the isolation transformer, which makes it resistant to the notorious problem of power supply pumping with single-ended Class D amplifiers. On the other side, since there is no intermediate energy storage on the secondary side, all the reactive power flow from the load to the amplifier and peak load power must be supplied from the primary side, which leads to overdimensioned primary switching stage. However, together with the promises of simplified design, higher efficiency, reduced number of reactive components, less redundancy and prospects for high-level integration, HF-link-based SICAM represents a highly competitive technology.

5.3 Frequency domain analysis of different PWM SICAM solutions

In the following sections a frequency domain analysis of different SICAMs that utilize PWM will be undertaken. It is by no means the only modulation approach that can be successfully implemented in a SICAM, but when compared to some of the alternative modulation principles like for example Pulse Density Modulation (PDM), PWM can achieve satisfactory performance and bandwidth with lower switching frequency.

5.3.1 Time domain and frequency domain operations of power electronics

For the discussions in the next few sections, it is interesting to analyze the operations performed by half-bridge and full-bridge switching stages in time and frequency domain. The schematics of the half-bridge and full-bridge switching stages are given in Fig. 5.3 and Fig. 5.4.

For the half-bridge switching stage, time domain and frequency domain operation represent:

- time-domain **multiplication**:

$$v_1(t) = v_g(t) \cdot s_1(t) \tag{5.1}$$

- frequency-domain **convolution**:

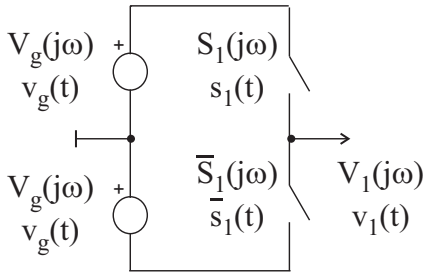

Fig. 5.3. Half-bridge schematic with the associated voltages and switching functions

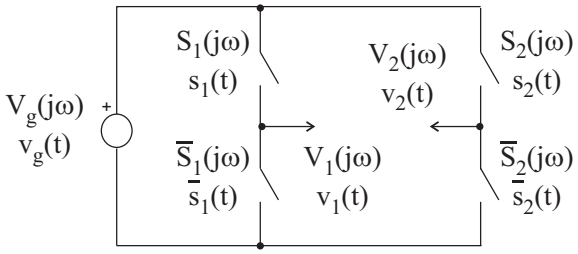

Fig. 5.4. Full-bridge schematic with the associated voltages and switching functions

$$V_1(j\omega) = V_g(j\omega) * S_1(j\omega) = \int_{-\omega}^{+\omega} V_g(j\nu) S_1(j\omega - j\nu) d\nu \tag{5.2}$$

For the full-bridge switching stage, time domain and frequency domain operation represent:

- time-domain **multiplication and subtraction**:

$$v_1(t) - v_2(t) = v_g(t) \cdot [s_1(t) - s_2(t)] \tag{5.3}$$

- frequency-domain **convolution and subtraction**:

$$V_1(j\omega) - V_2(j\omega) = V_g(j\omega) * [S_1(j\omega) - S_2(j\omega)] = \int_{-\omega}^{+\omega} V_g(j\nu)[S_1(j\omega - j\nu) - S_2(j\omega - j\nu)] d\nu \tag{5.4}$$

An example of the time domain waveforms and frequency domain spectrum of a full-bridge with 1 kHz test signal is depicted in Fig. 5.5. It can be observed that because of the subtraction of the frequency spectrums of the switching functions S_1 and S_2 there is an effective doubling of the switching frequency in the resultant switching function $S_1 - S_2$ i.e. the switching harmonics at $(2n+1)f_s$ are missing.

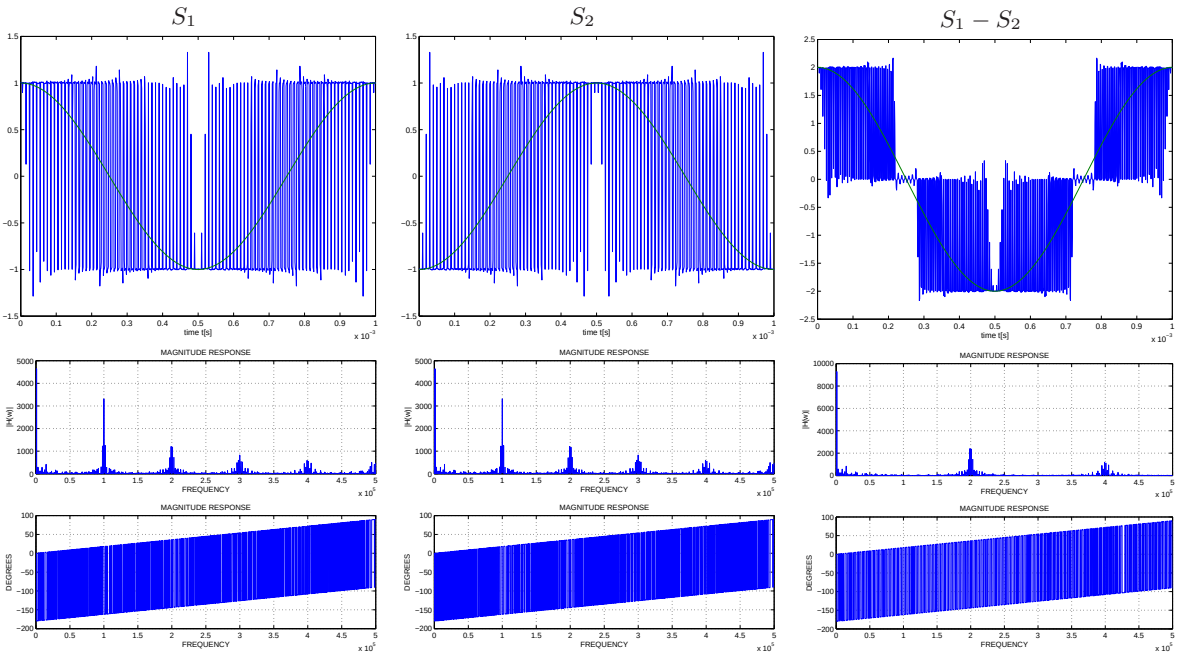

Fig. 5.5. Time and frequency domain analysis of full-bridge switching stage

5.3.2 Audio amplification with only a primary side switching stage

Before proceeding to the frequency domain analysis of different SICAMs, it is interesting to analyze the possibility of building an isolated direct audio power amplifier with a switching stage only on the primary side, as shown in Fig. 5.6. The reference audio signal with the Signal Spectrum (SS) made entirely from the audio baseband enters the PWM modulator. The SS of the PWM modulator output depends on the carrier shape (ex. single-sided or double-sided) and the number of levels (ex. 2-level or 3-level), but is always including the modulating audio signal baseband, carrier harmonics as well as their intermodulation product sidebands [33]. When the output of the PWM modulator is directly used to drive the input stage, the Power Spectrum (PS) of the transformer voltage has a low frequency (LF) content that can extend down to 20 HZ and therefore demands huge isolation transformer. Therefore this approach is regarded as economically unsound, i.e. all of the practical SICAMs must have switching stages on both sides of the isolation barrier in a form of a small high frequency (HF) transformer. In the following sections, the switching stage on the primary side of the HF transformer will be referred as primary-side stage, input stage or inverter stage, and the switching stage on the secondary side will be referred as secondary-side stage, output stage or bidirectional bridge.

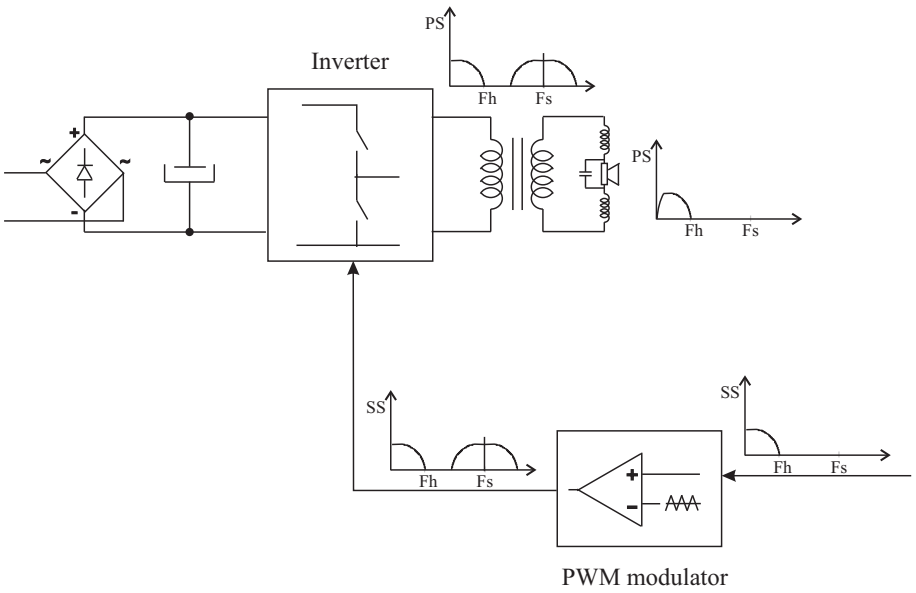

Fig. 5.6. Isolated audio power amplifier with only a primary-side switching stage

5.3.3 Coding and decoding of the audio signals for isolated amplifiers

Previous example showed that some signal processing is needed before sending the train of PWM rectangular pulses from the PWM modulator to the gates of both switching stages. The signal processing can be divided into two phases: coding, where the entire LF audio baseband is inserted into the sidebands around the HF carrier harmonics and decoding, which restores the audio baseband on the secondary side of the isolation barrier. The following example should clarify the aforementioned concepts.

The frequency spectrum of different natural sampled PWM waveforms F_{NxDx} has been derived in [33]. The Fourier series of a 2-level double-sided PWM signal F_{NADD} is given with the following equation:

$$F_{NADD}(t) = M\cos(\omega_m t) + 2\sum_{m=1}^{\infty} \frac{J_o(m\pi\frac{M}{2})}{\frac{m\pi}{2}} \sin\left(\frac{m\pi}{2}\right)\cos(m\omega_c t) + \\ + 2\sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty} \frac{J_n(m\pi\frac{M}{2})}{\frac{m\pi}{2}} \cdot \sin\left(\frac{(m+n)\pi}{2}\right)\cos(m\omega_c t + n\omega_m t) \tag{5.5}$$

where M is the modulation index, ω_m is the angular frequency of the modulating audio signal, ω_c is the angular frequency of the triangular carrier, J_n is Bessel function of the first kind with order n, m and n are integer numbers. The PWM signal F_{NADD} in time domain and frequency domain is shown in Fig. 5.7 and Fig. 5.8, correspondingly.

One possible way to eliminate the audio baseband in F_{NADD} is to invert the polarity of each second PWM pulse, which is known to produce LF-free voltage waveform and allows for building smaller isolation transformer [3]. The inversion process is equivalent to multiplication in the time domain of the 2-level double-sided PWM signal $F_{NADD}(t)$ with a train of rectangular pulses $F_r(t)$ synchronized with the triangular carrier, or equivalently convolution of the corresponding magnitude and phase spectra in the frequency domain, which effectively removes the LF audio baseband.

The Fourier series of a train of rectangular pulses synchronized with the triangular carrier is given by:

$$F_r(t) = \frac{4}{(2k-1)\pi}\sin[(2k-1)\omega_c t] \tag{5.6}$$

where k is an integer number. The rectangular pulse train F_r in time domain and frequency domain is shown in Fig. 5.9 and Fig. 5.10, correspondingly.

The resultant waveform with the coded baseband becomes:

$$F_{NADD}(t)\cdot F_r(t) = \frac{2M}{(2k-1)\pi}\{\sin[(2k-1)\omega_c t + \omega_m t] + \sin[(2k-1)\omega_c t - \omega_m t]\} + \\ + 2\sum_{m=1}^{\infty}\frac{4J_o(m\pi\frac{M}{2})}{m(2k-1)\pi^2}\sin\left(\frac{m\pi}{2}\right)\cdot\{\sin[(2k+m-1)\omega_c t] + \sin[(2k-m-1)\omega_c t]\} + \\ + 2\sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty}\frac{4J_n(m\pi\frac{M}{2})}{m(2k-1)\pi^2}\sin\left(\frac{(m+n)\pi}{2}\right)\cdot \\ \cdot\{\sin[(2k+m-1)\omega_c t + n\omega_m t] + \sin[(2k-m-1)\omega_c t - n\omega_m t]\} \tag{5.7}$$

Equation (5.7) above shows that the LF audio baseband has been coded into the sidebands around the HF switching harmonics. The resultant PWM signal $F_{NADD}\cdot F_r$ in time domain and frequency domain is shown in Fig. 5.11 and Fig. 5.12, correspondingly. Notice that there is no LF content in the frequency spectrum of the coded waveform in Fig. 5.12.

The decoding process represents nothing else than another multiplication of the resultant waveform $F_{NADD}(t)\cdot F_r(t)$ in (5.7) with the same rectangular pulse train $F_r(t)$ in (5.6), which is always done at the secondary side to restore the original audio baseband. During this process the polarity of the coded pulses is inverted once again to restore the original pulse sequence from the PWM modulator and its LF audio content. In frequency domain this corresponds to convoluting the corresponding frequency spectra of the coded waveform $F_{NADD}(t)\cdot F_r(t)$ and the rectangular pulse train $F_r(t)$, which effectively extracts the audio information from the sidebands of the switching harmonics and restores them at the original frequencies in the audio baseband.

Looking at the constitutive parts of the coded waveform (5.7), it can be noticed that while $F_{NxDx}(t)$ contains LF audio content, the rectangular pulse train $F_r(t)$ has only HF content, just like the coded PWM signal $F_{NxDx}(t) \cdot F_r(t)$. This means that both $F_{NxDx}(t) \cdot F_r(t)$ and $F_r(t)$ can be used to transfer energy from the mains through the isolation barrier to the secondary side, with minimum size transformer. In the former case, the audio coding is done on the primary side and the audio decoding and restoration of the original LF content is performed on the secondary side of the transformer. In the latter case, both the audio coding and the decoding are performed on the secondary side, but supplemented with the energy-transferring HF rectangular voltage waveform on the primary side. The analysis of the two aforementioned SICAM approaches will be subject of the following sections.

5.3.4 SICAM with modulated transformer voltages

SICAM with modulated transformer voltages [3],[52], shown in Fig. 5.13, uses the coded 3-level double-sided PWM signal $F_{NBDD}(t) \cdot F_r(t)$ to drive the primary switching stage and the transformer. On the secondary side, the bidirectional bridge is driven with the same rectangular pulse train $F_r(t)$ to restore the audio baseband. The main advantage of this approach is that the transformer voltage contains periods with zero voltage each switching period, during which the commutation of the secondary side bidirectional bridge is performed. The aforementioned benefit is achieved by shortly turning on both the incoming and outgoing bidirectional switches during the periods with zero transformer voltage, which does not create short-circuit current on the primary side and at the same time provides an uninterrupted path for the load current. As a side effect, output stage switching losses are decreased too. However, this approach necessitates separate transformers and input stage for each audio channel, which is not economically feasible in the modern multi-channel audio systems.

In order to achieve good audio performance, the switching frequency of the output stage needs to be very high, in the order of few hundreds of kHz. Since the switching of both stages in this approach must be simultaneous to perform load current commutation the switching frequency of the input stage will be rather high, too, which can create significant switching losses in the primary side active devices.

From a practical viewpoint, there are also problems with creating additional voltages for control biasing on both the primary and the secondary, as well as creating power supplies for the secondary-side isolated gate drives, if needed. Since the power transformer voltages are modulated in accordance with the amplified audio signal, power flow to any auxiliary winding put on the same leg with the main transformer will be variable and input signal dependant. This in turn asks for adding additional auxiliary transformers and switching stages on the primary side or using line transformers with post regulators, which unavoidably adds to the product cost.

5.3.5 SICAM with non-modulated transformer voltages

SICAM with non-modulated transformer voltages [53], [9], shown in Fig. 5.14, is driving the primary stage and the transformer with the 50% duty cycle rectangular waveform $F_r(t)$. The rest of the coding and decoding is done on the secondary side, where the bidirectional bridge is driven with the coded PWM signal $F_{NxDx}(t) \cdot F_r(t)$. The main benefit of the presented approach is the possibility of supplying power to multiple output stages with the same primary stage and transformer, as well as easy derivation of auxiliary voltages for control biasing or isolated gate drive power supplies by fitting additional

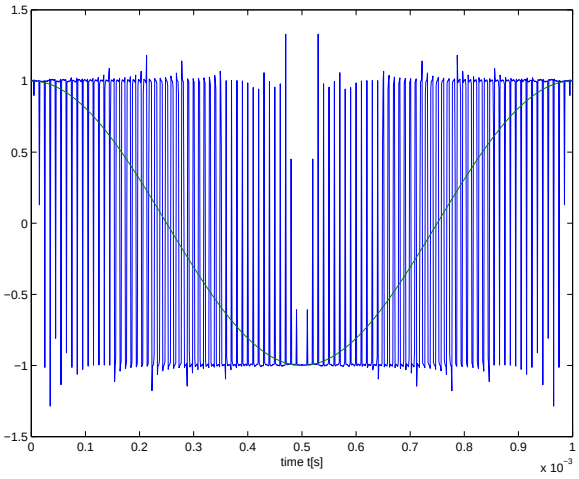

Fig. 5.7. 2-level double-sided PWM signal F_{NADD}

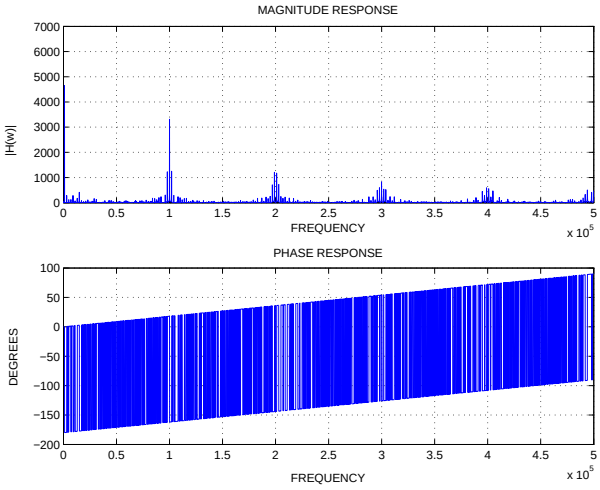

Fig. 5.8. Frequency spectrum of F_{NADD}

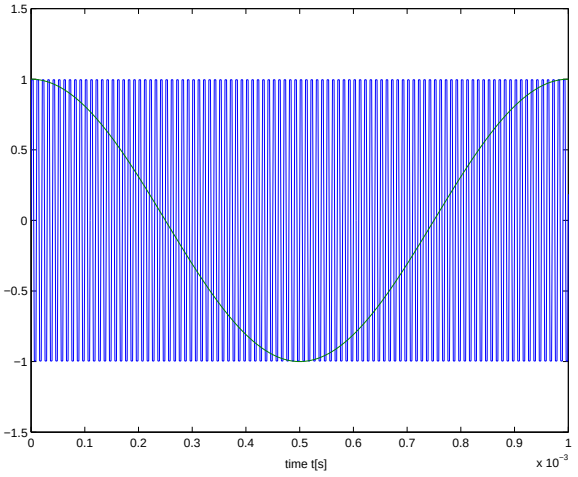

Fig. 5.9. Rectangular pulse train F_r

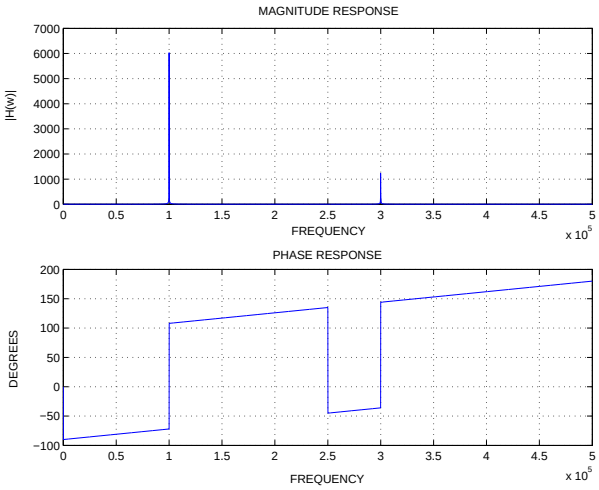

Fig. 5.10. Frequency spectrum of F_r

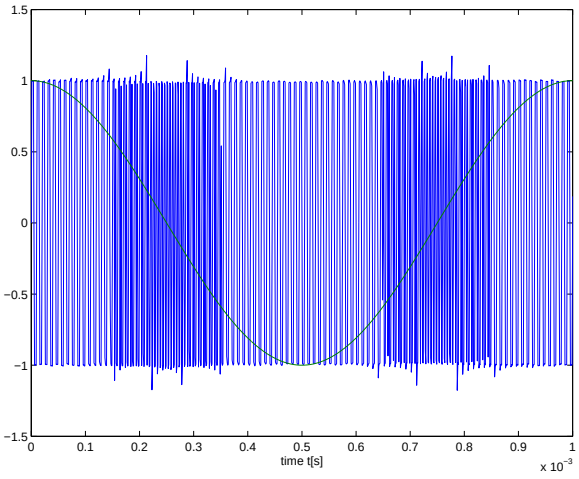

Fig. 5.11. Resultant PWM signal $F_{NADD} \cdot F_r$

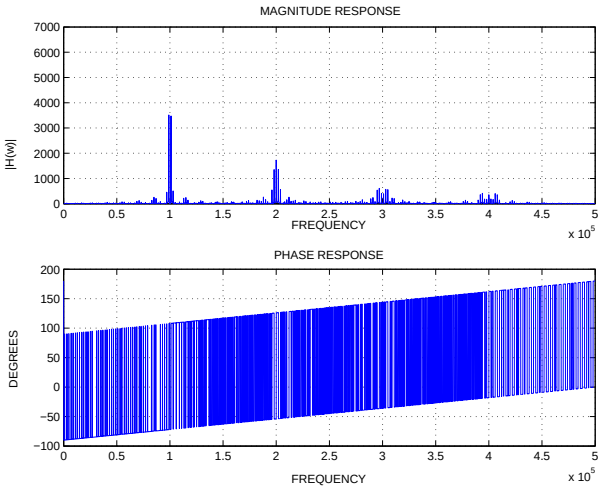

Fig. 5.12. Frequency spectrum of $F_{NADD} \cdot F_r$

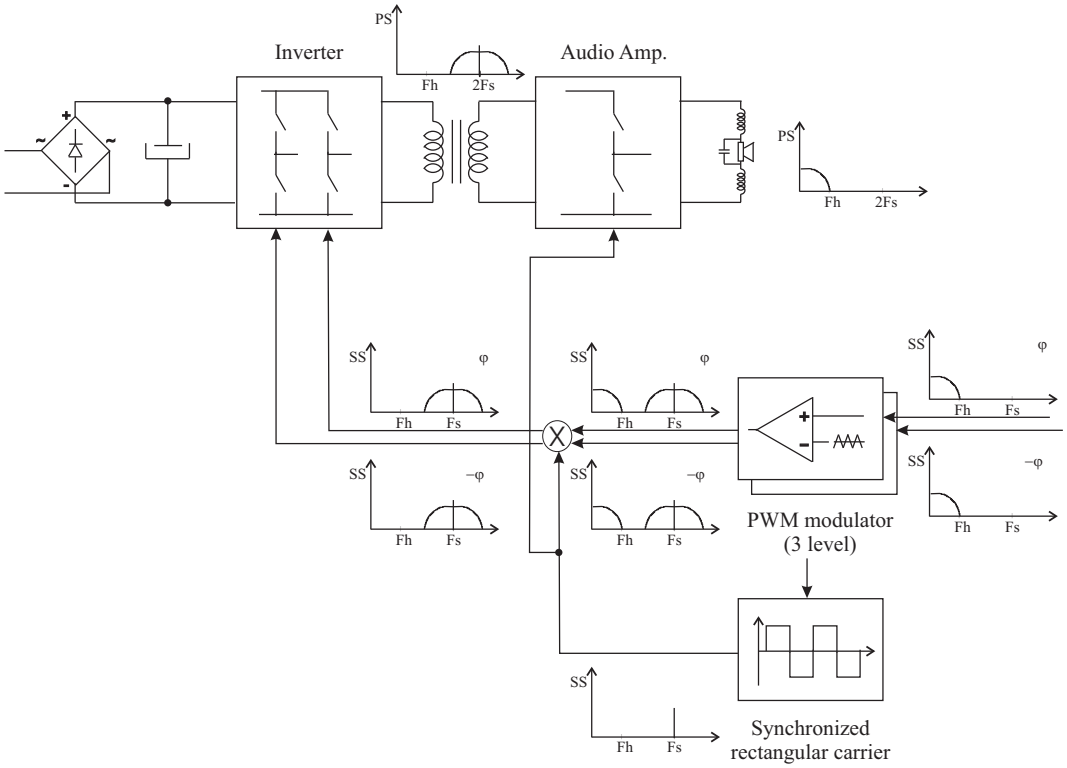

Fig. 5.13. SICAM with modulated transformer voltages

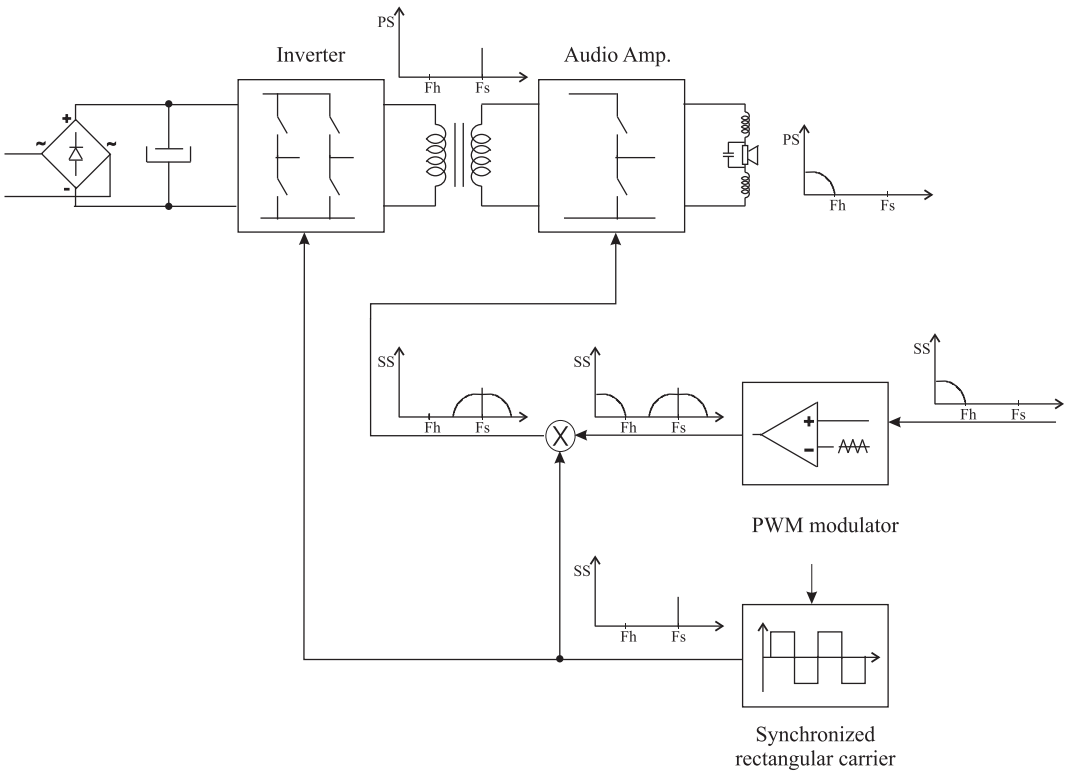

Fig. 5.14. SICAM with non-modulated transformer voltages

windings on the same core. It is also favorable for the conducted differential-mode Electro-Magnetic Interference (EMI), since the full duty cycle operation causes the input stage to draw line current almost continuously (if the short dead time is neglected), so the only remaining problem is the common-mode noise.

However, with this approach, the commutation of the load current in the secondary side bidirectional bridge becomes rather involved, since in principle there are no instants with zero transformer voltage that can alleviate the commutation. Therefore, the commutation of the bidirectional bridge depends heavily on using load voltage clamps [9], [54] or advanced commutation techniques [53], [30]. Due to the numerous advantages of the SICAMs with non-modulated voltages, this approach has been chosen for implementation and is discussed in detail in the next sections and chapters.

5.4 Developing SICAMs from SMPSs

The simplest way of developing direct audio conversion topologies is starting with a particular power supply scheme and extending its capabilities, like shown in Fig. 5.15. Firstly, the power supply control bandwidth is increased over the intended power bandwidth i.e. over the highest frequency of the signal to be amplified, resulting in tracking power supply with variable DC output voltage. This is usually done by decreasing the size of the output low-pass filter so that its frequency response is flat over all the frequencies of interest and then drops rapidly to attenuate the switching harmonics. At the same time, the switching frequency of the SMPS is somewhat increased, to help achieve higher bandwidth. In order to complete the construction of the direct audio power amplifier, bidirectional power flow capability is added to the tracking power supply by replacing all the unidirectional components (for example, the secondary-side rectifiers) with bidirectional switches. At the end, a suitable controller is designed in a way that provides enough gain with sufficient phase margin throughout the power bandwidth, so that the resultant amplifier distortion and output impedance are kept low. These development steps are shown on the example of half-bridge SMPS in Fig. 5.16.

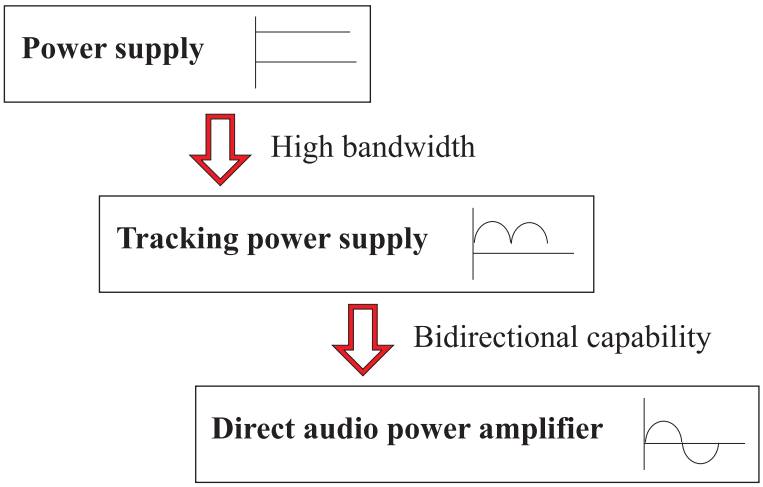

Fig. 5.15. SICAM development steps

5.5 Bidirectional switches and gate drives for isolated SICAMs

5.5.1 Bidirectional switch arrangements

A single quadrant switch (1QSW) is capable of conducting in only one current direction and blocking only one voltage polarity. Its output characteristic is therefore completely

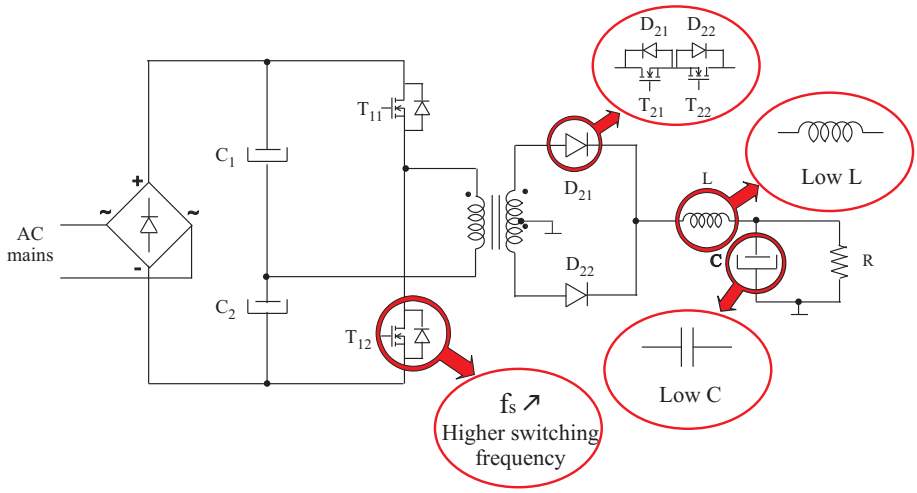

Fig. 5.16. Reworking a half-bridge SMPS for SICAM operation

placed in a single quadrant of the V-I plane. Representatives of this group are simple switching elements like diode, BJT, IGBT etc.

A two quadrant switch (2QSW) operates in two quadrants of the V-I plane. It can be:

- Voltage 2QSW - it is capable of blocking voltages of both polarities, but it conducts current in only one direction; voltage 2QSW is usually constructed by series connection of a diode and a transistor (BJT,IGBT) and is shown in Fig. 5.17a; and
- Current 2QSW - it is capable of conducting current in both directions, but it blocks voltage of only one certain polarity; this switch is usually made of an antiparallel pair of a diode and a transistor and is shown in Fig. 5.17b.

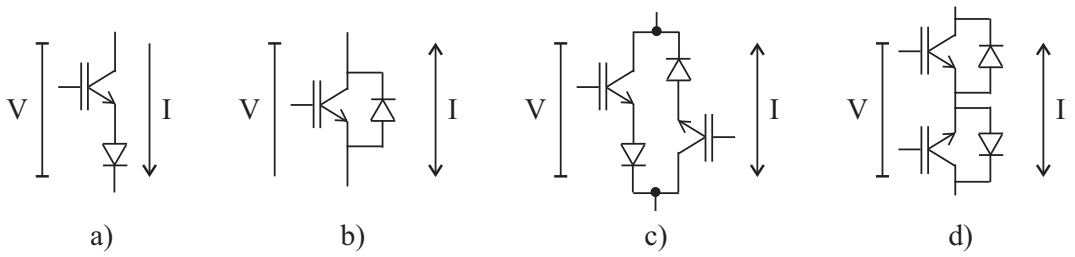

Fig. 5.17. a) Voltage 2QSW, b) Current 2QSW, c) Antiparallel connection of two voltage 2QSW, d) Antiseries connection of two current 2QSW

It should be stressed, however, that because of the MOSFET being a representative of majority carrier devices and because of its internal antiparallel body diode, there is a possibility of conduction of currents with both directions through the MOSFET's single type semiconductor channel. This makes the MOSFET itself a current 2QSW. MOSFET voltage 2QSW can be obtained by adding a series diode, thus effectively blocking one possible current direction.

Four quadrant switch (4QSW) or a fully bidirectional switch is constructed by antiparallel connection of two voltage 2QSWs as depicted in Fig. 5.17c, or by antiseries connection of two current 2QSWs as depicted in Fig. 5.17d. In the cases where the 4QSW consists of two anti-parallel voltage 2QSWs, the current paths for different current directions are clearly separated, and each of the current directions can be separately controlled. This feature is not so obvious for the 4QSW consisting of two current 2QSW, where these two cases are distinguished:

- Both current paths are closing through the same element (for ex. MOSFET), so without measuring the current sign one cannot determine the zero-crossing point to block a certain current direction by turning off the element completely, or
- Both current paths are clearly separated, but one path is closing through a passive, uncontrollable semiconductor element (diode), thus resulting in possible blocking of only one distinctive current direction.

A way to control the current direction of a 4QSW consisting of two current 2QSW emerges only after combining the two 2QSW together.

In SICAMs, bidirectional switches (4QSW) are required in the output stage of the HF-link audio power amplifier. As mentioned earlier, these are capable of blocking voltages with both polarities and conducting currents in both directions. Turning to practical implementation, except for the JFET being a single bidirectional component shown in Fig. 5.18d, all other bidirectional switches are comprised of few discrete components - diodes and, for example, MOSFETs:

- Four diodes and a MOSFET in a bridge configuration, shown in Fig. 5.18a. This arrangement requires a single MOSFET and has just a single isolated gate drive, but necessitates 4 discrete diodes. There are always two diodes and a MOSFET in the load current path, which creates significant conduction losses. There is no possibility of controlling the load current direction.
- Two diodes and two MOSFET in a configuration with separate load current paths, shown in Fig. 5.18b. This arrangement requires two MOSFETs with two isolated gate drives, but necessitates just two discrete diodes. There is always a diode and a MOSFET in the load current path. Load current direction can be controlled by switching on and off the corresponding MOSFETs, since this 4QSW is antiparallel connection of two voltage 2QSW.
- Two MOSFETs in a back-to-back i.e. common-source connection, shown in Fig. 5.18c with or without two discrete diodes. This arrangement requires two MOSFETs with a single isolated gate drive and if MOSFET body diodes are not good enough, two discrete diodes. Load current path can pass through the conductive channels of both MOSFETS, or if the voltage drop in the channel is excessive, the load current can divert into one of the body diodes or outer discrete diodes. Load current direction can be controlled by switching on and off the corresponding MOSFETs.

The selection of a MOSFET as an active switching element in audio power amplifiers is due to its very high switching speed, pleasant switching characteristics as a result of the MOSFET being majority carrier device (no minority space charge and thus no tailing current), ease of control through the isolated gate, positive thermal coefficient which helps paralleling of MOSFETs, as well as low conduction losses in the conductive semiconductor channel. At the same time the diodes must be of the ultra-fast type, due to the high switching frequency of the proposed audio power amplifiers.

For audio power amplifiers, the common-source arrangement in Fig. 5.18c without discrete diodes seems to be the best choice from simplicity and cost/performance ratio perspective. By wisely choosing the MOSFETs in this arrangement, load current can be predominantly passed through the MOSFET channel and not through the body diodes, which guarantees very good efficiency, low conduction losses and low distortion (caused usually by body diode conduction at higher load current levels). However, going into extremes is by no means advantageous, since choosing a large die MOSFETs, which even at full load current have voltage drops much smaller than the body diode voltage drop, will certainly reduce the conduction losses but will inevitably increase the switching losses due to the much slower switching characteristics.

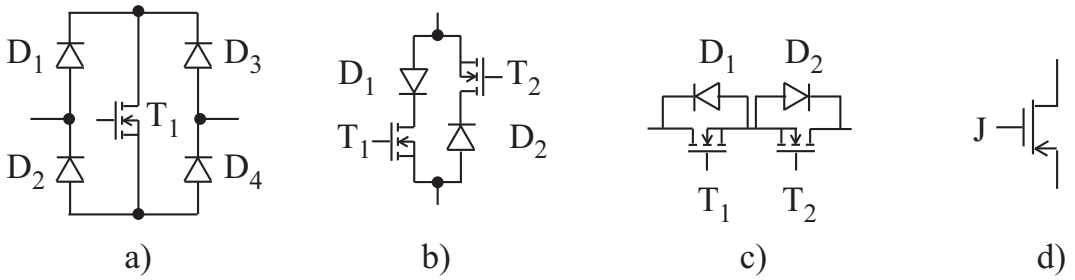

Fig. 5.18. Different arrangements of bidirectional switches (4QSW)

Another emerging technology is the power JFET, which is rather appealing since it is a single bidirectional component with potentially very small conduction losses. Unlike the bidirectional switches in Fig. 5.18b,c, JFET has no possibility of controlling the load current direction and the safe-commutation switching strategies from Section 6.2.1 are not applicable. Due to its normally-on characteristics and the existence of either rather low breakdown voltage JFETs [55] or emerging very high voltage SiC devices [56], [57], it has still a limited usage in the common power conversion topologies and is predominantly used as a solid-state switch in different battery powered device. As the breakdown voltages increase, it will certainly become an interesting alternative for building bidirectional switches, but only in certain type of isolated SICAM applications where load voltage clamps are used for commutating the load current.

The conduction performance of all 4QSWs in Fig. 5.18 in terms of audio was tested using a linear amplifier and by measuring the corresponding THD+N before and after the switch. The simplified diagram of the test bench is shown in Fig. 5.19, while the results are shown in Figs. 5.20-5.23. MOSFETs used were International Rectifier's IRF520N, discrete diodes were On Semiconductor's MUR820 and JFET was Lovoltech's LD1107N.

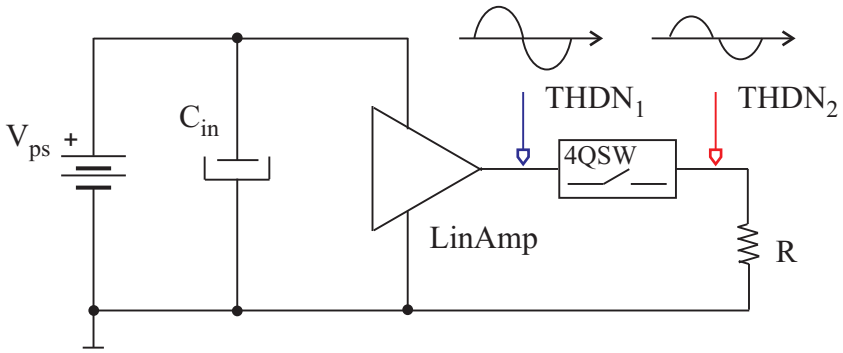

Fig. 5.19. Test bench for bidirectional switches (4QSW)

From the measured THD+N in Figs. 5.20-5.23 of the bidirectional switches in Fig. 5.18 with sinusoidal input voltage it can be concluded that the common source connection of two MOSFETs and the single JFET 4QSW have the best prospects for audio applications, since their internal structure assures that the semiconductive medium for the largest range of output voltages exhibits resistive characteristics. This means that when reproducing sinusoidal reference with certain frequency, the voltage drop across the on-resistance $R_{DS,on}$ of the aforementioned switches will consist only of the fundamental component,

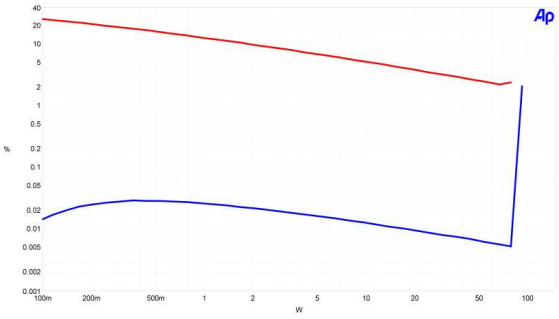

Fig. 5.20. THD+N as function of power at 1 kHz for 4QSW with one MOSFET and four diodes in Fig. 5.18a measured before (bottom) and after (top) the 4QSW

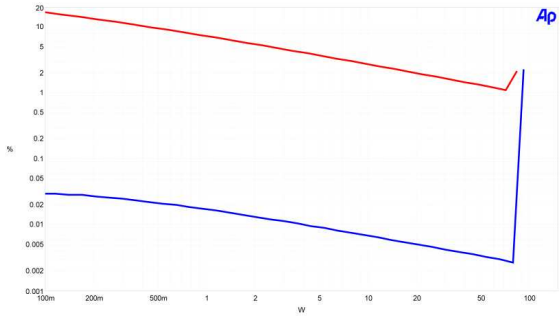

Fig. 5.21. THD+N as function of power at 1 kHz for 4QSW with two MOSFETs and two diodes in Fig. 5.18b measured before (bottom) and after (top) the 4QSW

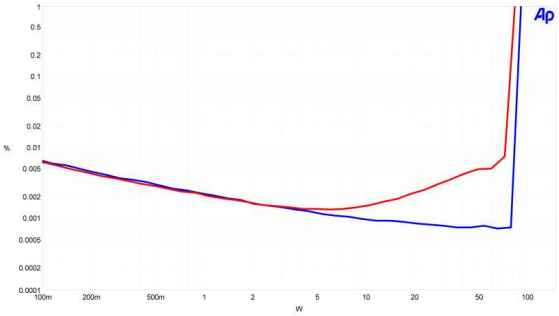

Fig. 5.22. THD+N as function of power at 1 kHz for 4QSW with two common-source connected MOSFETs in Fig. 5.18c measured before (bottom) and after (top) the 4QSW

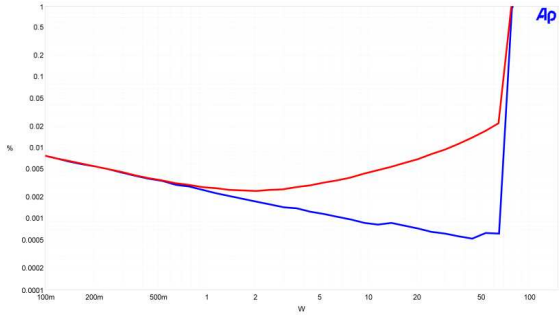

Fig. 5.23. THD+N as function of power at 1 kHz for 4QSW with just a single Junction FET shown in Fig. 5.18d measured before (bottom) and after (top) the 4QSW

which although decreases the fundamental of the output voltage does not severely affect the overall THD+N.

In the cases of the single MOSFET and four diodes 4QSW or the two MOSFETs and two diodes 4QSW with separate current paths there are always one or two diodes in the current path. This leads to crossover distortion around 0 V with sinusoidal input voltages because of the threshold voltage of the diode $V_{D,th} > 0$ below which the diode is not conducting. On the other hand, during conduction the diode voltage drops are significantly nonlinear because of the nonlinear output characteristic of the diode, which can be only approximately modelled by its dynamic resistance R_D. These two effects cause tremendous audio distortion which is visible in the measurements.

A very good review of the bidirectional switch implementation and safe commutation is given in [30], with some subsequent modifications and improvements presented in [34], [58], [59].

5.5.2 Gate drives for bidirectional switches

Pulse transformers for bidirectional switch gate drive

Pulse transformers are very often used for gate drive in either unipolar or bidirectional switches. They are very simple and reliable, have small form factors and provide both isolation and voltage level adjustment. Their speed of response is very fast and they have high bandwidth, but their performance deteriorates in presence of leakage inductance, which limits the rise time of the gate current.

In order to avoid DC-bias of the magnetic core, pulse transformers are usually driven from unipolar, single-ended logic with a series DC-voltage blocking capacitor, or with a symmetrical, bipolar gate drive. Pulse transformers are best suited for driving MOSFETs with nearly constant or slowly varying duty cycles, which leave enough time for the transient processes in the DC-blocking capacitor to elapse without disturbing too much the on- and off-gate voltage levels.

Generally speaking, with bidirectional switches there is no need for high level of safety isolation, since pulse transformers perform mere voltage level shifting and generally do not cross the mains isolation barrier. Therefore, pulse transformer can be wound with bifilar wire to minimize the leakage inductance, as long as the turns ratio is 1:1, which is not always the case. If there is a need for voltage level adjustment, like for example when interfacing low voltage logic to power MOSFETs gate or when the gate voltage swing on the primary side is reduced due to the presence of DC-voltage blocking capacitor, higher transfer ratios 1:n are inevitable and bifilar windings do not seem realizable.

When power transfer through the pulse transformer is limited and unsatisfactory because of the leakage inductance, a possible way for alleviating it is to use the pulse transformer for mere gate signal transfer, while the total MOSFET gate drive is provided by a separate, low output impedance isolated power supply and gate drive circuitry referenced to the MOSFET source. In this way the pulse transformer can be very small, since it is allowed to saturate during normal operation and only the timing of the rising and falling edges matters.

In some lower performance isolated gate drives for bidirectional switches, the pulse transformer can be used for both gate signal and power transfer, but their speed of response can be sluggish. Therefore, they do not seem interesting for the high switching frequencies required by audio power amplifiers.

Optocouplers for transferring gate drive signals

Optocouplers provide very high level of isolation and rejection of common mode noise, which makes the operation of the converter much more reliable. However, they require separate isolated power supply referenced to the MOSFET source for providing the gate drive of the bidirectional switch, since they perform only level shifting. However, audio power amplifiers use very high switching frequencies and therefore those optocouplers commonly found in the error feedback of the isolated off-line SMPS cannot be used in most of the cases. Instead, some of the faster optocouplers for telecommunication applications are better suited, but their price is also somewhat higher.

New level shifter for bidirectional switch gate drive

Level shifters are often used in the high-side drivers of half-bridge and full-bridge topologies to transfer the signals to the higher voltage level associated with the upper MOSFET. Gate drive power is usually obtained from a boost capacitor being charged during the conduction of the lower MOSFET or with some type of charge pump. However, these level shifters are only intended for operation on positive voltages, i.e. every excessive voltage spike below ground on the source pin of the upper MOSFET can lead to latch-up or destruction of the driver IC.

The conventional grounding scheme of the single-ended HF-link converter is shown in Fig. 5.24a, where the center tap of the transformer and one load terminal are grounded. In this case, it is assumed that two isolated power supplies and gate drivers are present and their corresponding ground points are connected to the MOSFET common-source

points of the two bidirectional switches. Voltages at the common source points of both bidirectional switches $T_{21} - T_{22}$ and $T_{23} - T_{24}$ with respect to ground can be both positive and negative, depending on the transformer voltage polarity and bidirectional switch gate voltage. The grounding point is common for both the power amplifier and control section. This, however, prohibits using a conventional high-side level shifter for transferring the gate signal to the gate driver of each bidirectional switch, for the reasons of logic latch-up or possible driver destruction mentioned in the last paragraph.

With the newly proposed grounding scheme for HF-link converters in Fig. 5.24a, level shifting is made easier because the common-source point of both bidirectional switches can have only negative voltages. If positive voltage is applied across the bidirectional switch, the body diode of either T_{22} or T_{24} will immediately clamp it to the ground, while the body diodes of T_{21} and T_{23} will block it.

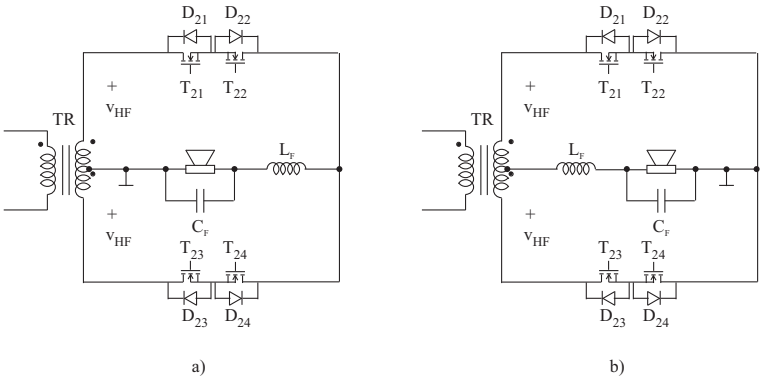

Fig. 5.24. a) Conventional grounding scheme for HF-link converters and b) Newly proposed grounding scheme for easy level shifting

New negative voltage-tolerant level shifter and gate driver is depicted in Fig. 5.25. The heart of the level shifter is the P-type MOSFET T_1, which works together with the active pull-down resistive divider $R_1 - R_2$ to turn on and off the bidirectional switch $T_{23} - T_{24}$. BJTs T_2 and T_3 form the gate driver, which is supplied by an isolated power supply with voltage V_{ISP}. Together with the control biasing voltage V_{CC} and the power amplifier, they all share the same ground connection.

Capacitor C_{FB} forms a positive feedback around the gate driver that helps turning-off the bidirectional switch, which is troublesome because of the parasitic capacitance of the P-type MOSFET T_1. Problem is pronounced when the parasitic capacitance C_{DS} is being charged after bidirectional switch turn-off with negative HF-link voltage $v_{HF} < 0$, which causes capacitive current to flow through the resistive divider $R_1 - R_2$ and immediately turn-on again the bidirectional switch.

5.6 Other possible approaches for isolated SICAMs

Some of the other possible approaches for isolated SICAMs include resonant primary stages, where HF-link voltage has sinusoidal or nearly sinusoidal form. Due to the sinusoidal shape of the voltages and currents, these input stages are known to have low ElectroMagnetic Interference (EMI) and low switching losses, as a result of the zero-voltage switching (ZVS) and/or zero-current switching (ZCS). As another advantage of the sinusoidal output voltage of the resonant input stage, zero voltage or near zero voltage intervals become longer and it is much easier to commutate the load current between the

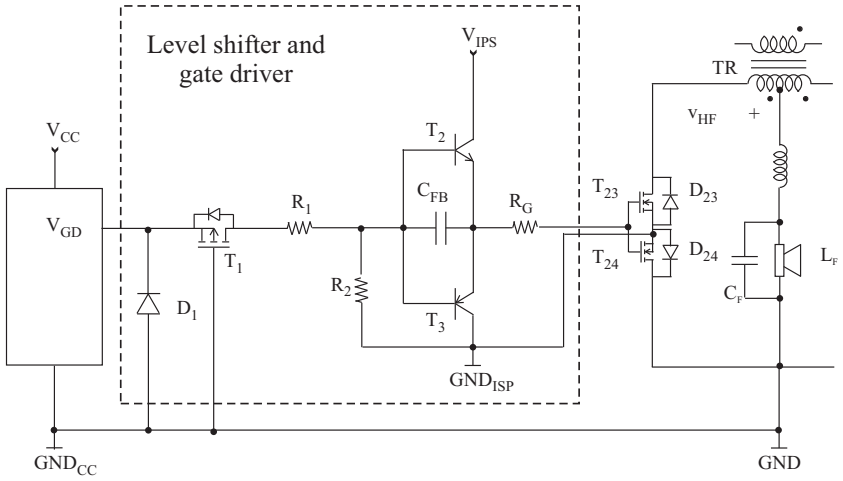

Fig. 5.25. Negative voltage-tolerant level shifter and gate driver

outgoing and incoming bidirectional switches in the SICAM output stage by shortly overlapping their conduction. This makes the resonant power supplies and resonant SICAM input stages very interesting for high switching frequency operation.

On the other hand, resonant power converters are characterized with higher output impedance, which makes their operation especially load dependent. This can represent a problem when the load of the resonant input stage consists of a bidirectional output stage performing full-bandwidth audio power amplification, since the dynamics of the load is tremendous. And even more, by avoiding rectification on the secondary side load current is allowed to flow both in and out of the resonant tank, which significantly perturbs the resonant tank voltage. Control of resonant tank voltage is also challenging, since it asks for either variable frequency operation or using phase shifted PWM in full-bridge input stages. Some of the other problems include reduced efficiency of the resonant input stage in case of reactive current flow, which circulates between the elements of the resonant tank and causes losses in the switches without ever flowing to the load. Latter can be alleviated by carefully choosing the resonant tank topology (series $L-C$, parallel $L-C$, series-parallel $L-C_p-C_s$).

Although resonant converters are used in many advanced applications and are known technology, it was decided for the SICAM project to proceed with the hard switched power converters. However, a short review of some resonant converter topologies for input stage in isolated SICAMs will be given in Section 6.1.3.

5.7 Patent investigation

This section will review some of the patents in the field of isolated SICAMs for different applications, i.e. some protected general principles for isolated DC-AC conversion in a single stage.

Patent [2] is one of the earliest patents which deals with the so called "Phase demodulated high frequency bridge inverter" and is dated before probably the first published scientific paper on HF-link conversion [47]. It belongs to the group of SICAMs with non-modulated transformer voltages, where HF-link voltage has symmetrical rectangular waveform with 50% of duty cycle and no intervals with zero output voltage. Its block diagram is shown in Fig. 5.26. Bidirectional switches in the output stage are constructed from 4 diodes and single bipolar switch in full-bridge configuration, but no information can be found about the way load current commutates between the switches belonging to

the same leg, except that they are driven in complementary way one immediately after the other. Switching instants of the secondary side 4QSWs is found by phase-shifted PWM using two PWM modulators fed with the same externally created sawtooth carrier as first input and the reference signal or its inverse as second input correspondingly to drive each of the switching legs.

The inventor in [3] proposes the arrangement in Fig. 5.27, which is very similar to the previous one in the topology, but it differs a lot in the control principle since it is SICAM with modulated transformer voltages. The HF-link voltage is three-level PWM according to the reference voltage, but the LF content from the audio waveform is recovered by inverting each second pulse from the PWM pulse train, as already explained in Section 5.3.4. A simple push-pull input stage used on the primary side in general does not always guarantee a 3-level PWM transformer voltage, because in HF-link converters the reflected load current on the primary side during the dead time intervals of the input stage will cause the input stage freewheeling diodes to conduct and clamp transformer voltage to either polarity of the DC supply voltage. However, in this specific case, turning all the bidirectional switches on in the full-bridge output stage during the input stage dead time intervals is used to restrict the load current from flowing through the transformer by freewheeling it in the output stage, thus the voltage across the transformer is supposed to collapse to zero. This is, however, likely to be troublesome due to, firstly, the magnetization current flowing in the transformer primary and the stored magnetic energy in the leakage inductance, which is going to cause reversal of transformer voltage polarity and conduction of one of the input stage antiparallel diodes immediately after switching off the opposite primary switch. Secondly, the same moment when one of the primary switches which conducted the load current is switched off there will be immediate commutation of the load current into one of the input stage freewheeling diodes, depending on the load current direction, and the DC supply voltage with certain polarity will be applied across the transformer, so it is not clear how all four 4QSWs in the output stage will be turned on at the same time to freewheel the whole load current entirely in the output stage.

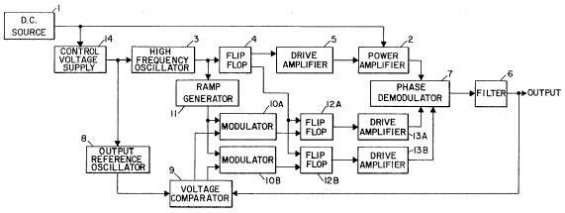

Fig. 5.26. Circuit diagram from [2]

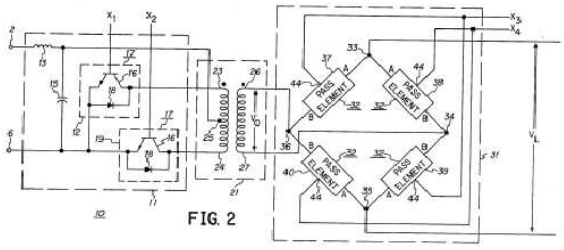

Fig. 5.27. Circuit diagram from [3]

Patent application [4] is similar to the previous one in both the topology and control principle, and it introduces a full-bridge 3-level PWM switching inverter on the primary side to alleviate the aforementioned problems, as depicted in Fig. 5.28. Beside the pure PWM, this patent also proposes Pulse Amplitude Modulation (PAM) by holding the width and the frequency of the pulses the same and just switching between different taps on the secondary winding of the transformer to change the amplitude of the applied voltage.

Inventors in [5] propose a "Phase modulated switchmode power amplifier and waveform generator" where both the input and the output stage are operated with full duty cycles, and the recovery of the audio signal across the load is obtained by phase shifting the switching of the output stage bidirectional switches with respect to the primary-side inverter. Thus this solution, shown in Fig. 5.29, belongs to the group of SICAMs with

non-modulated transformer voltages, but the switching frequencies of both stages must be equal. In one of the proposed embodiments, the input stage is made resonant, so that the HF-link voltage has sinusoidal nature and therefore short zero voltage intervals for performing output stage load current commutation. However, it is not clear how safe load current commutation will be performed in the other half of switching instants where transformer voltage is different than zero, and especially in the hard switched case.

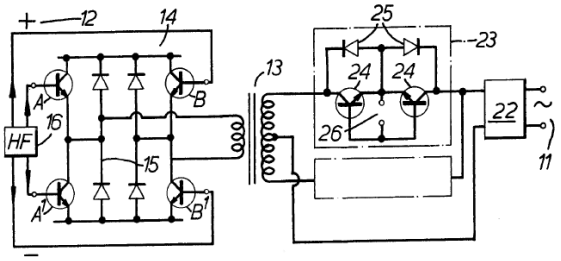

Fig. 5.28. Circuit diagram from [4]

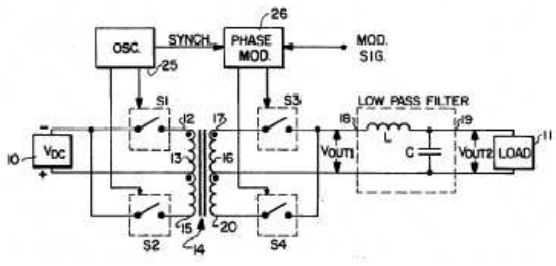

Fig. 5.29. Circuit diagram from [5]

Patent [6] proposes a redundant system with two low-pass output filters for reconstructing the audio signal, illustrated in Fig. 5.30, where the one operates only with positive voltages and the other one only with negative voltages. The switching output stage then connects directly the load terminals to the one or the other output filter, according to the desired polarity of the output voltage. The switching of the polarity selecting switches occurs only at zero output voltage, which significantly reduces switching losses and is certainly beneficial from load current commutation perspective, but it is not clear how alternatively loading and unloading the LC low-pass filters will affect the reliability of the amplifier without any passive damping networks to reduce the presumably very high quality factor Q of the filter.

The inventor of [7] presents a "Power conversion system" which is in fact a SICAM with modulated transformer voltages and is shown in Fig. 5.31. The operation of the topology with GTOs in the output stage is explained in detail together with the control principle, although it is mentioned that depending on the application other switch types can be used. What essentially happens in the output stage is that by having turned on both the outgoing and the incoming switch, the short circuit current flowing through the secondary winding of the transformer and limited by its leakage inductance will perform commutation of the load current to the incoming GTO switch and the outgoing GTO switch will seize conducting naturally. When using MOSFET in the output stage this particular solution cannot be applied to commutate the load current, because the short circuit current can flow and increase in either direction, but there are still some periods with zero transformer voltage which can be used for that purpose.

Patent [8] refers to "Synchronous modulation circuit" of an isolated SICAM with non-modulated transformer voltages shown in Fig. 5.32, where based on the HF-link voltage polarity the PWM modulator determines the correct gate driving signals for the bidirectional switches. Unfortunately, nothing is mentioned about the way 4QSW in the output stage need to be operated in order to avoid short-circuiting of the transformer secondary and still provide an uninterrupted path for the load current.

Inventor in [9] shows a similar invention like the phase-modulated SICAM from [5], but now the problem of the load current commutation is solved by using a dissipative RC clamp with rectifier diodes shown in Fig. 5.33 and connected both before and after the switches, thus appropriately handling the stored magnetic energy in both the transformer leakage inductance and output filter during the short dead-time intervals.

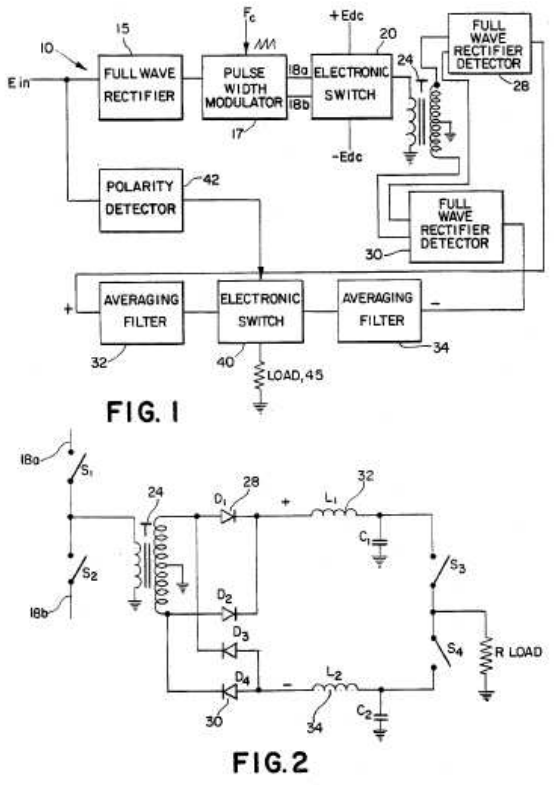

Fig. 5.30. Circuit diagram from [6]

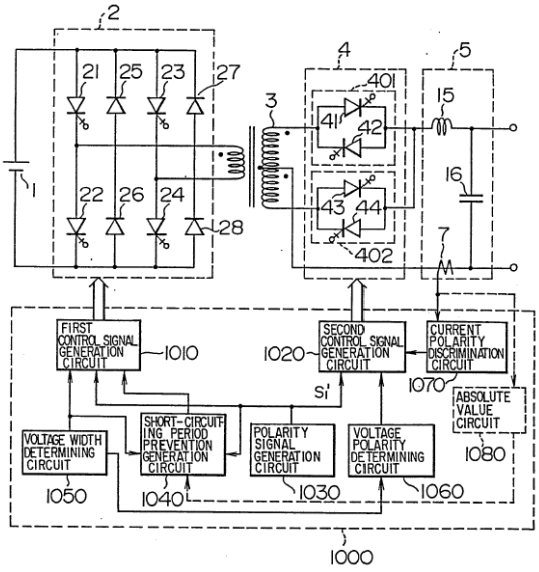

Fig. 5.31. Circuit diagram from [7]

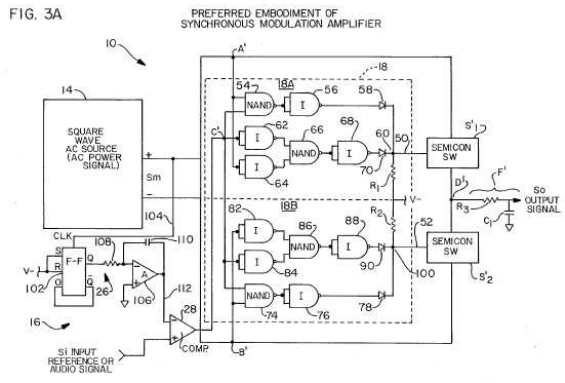

Fig. 5.32. Circuit diagram from [8]

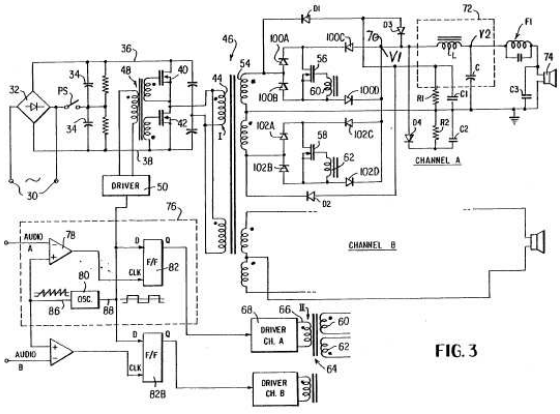

Fig. 5.33. Circuit diagram from [9]

Patent [10] proposes "Reduction of switching losses in phase-modulated switch-mode amplifier" shown in Fig 5.34 and similar to the one presented in [5], referring to SICAMs with modulated transformer voltages by inserting intervals with zero voltage in the transformer waveform, effectively using the 3-level PWM capability of a full-bridge input stage.

Patent [11] proposes a new Class N of simple and low component count audio power amplifiers with direct energy conversion in Fig 5.35, i.e. SICAMs with modulated transformer voltages, which are being subsequently synchronously demodulated on the secondary side. However, it is very difficult to avoid the impression that this simplicity is achieved on behalf of less flexibility and reliability. In all embodiments with a single switch input stage, it is clear that primary current can be conducted just in the direction of the antiparallel body diode. Since in SICAMs there is no intermediate energy storage on the secondary side, the load current with single-ended output stages must be reflected to the primary side, but this might not be possible for one direction of the reflected current. This problem is alleviated with some of the full bridge-type embodiments of output stages, where the load

current can be freewheeled in the output stage during the off-time of the primary switch. Another significant drawback is that the resetting of the magnetic core with single-switch topologies necessitates separate demagnetization winding or using two-switch topologies, but this limits the effective duty cycle to around 50%. As a side effect, for the same output power the secondary-side voltage must be around two times higher, which increases the stress exerted on the output stage switches and dictates use of switches with higher blocking voltage and higher on-resistance. Even in the cases when push-pull, half-bridge or full-bridge is used in the input stage, their control is such that just one switch or set of switches is operated on and off for certain polarity of the output voltage, which means that the transformer polarity during the corresponding off-time will depend on the direction of the freewheeling reflected load current, which can lead to severe saturation of the magnetic core.

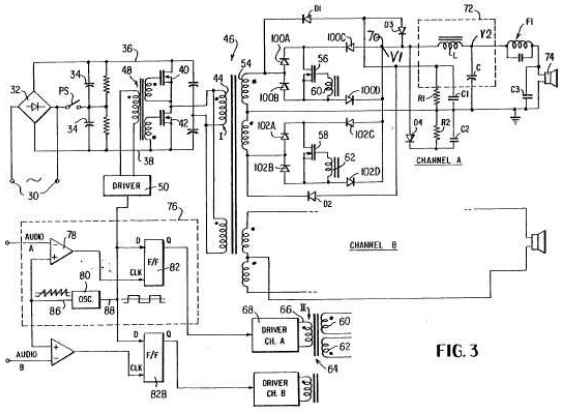

Fig. 5.34. Circuit diagram from [10]

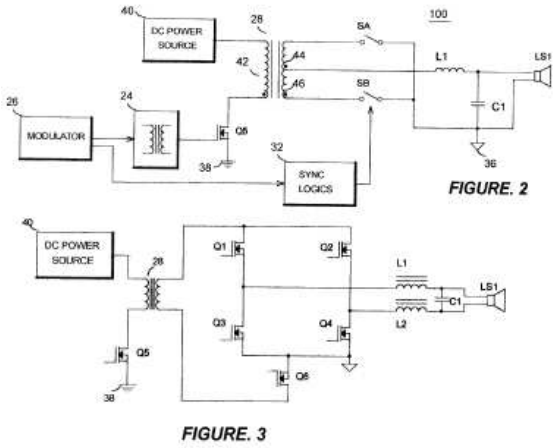

Fig. 5.35. Circuit diagram from [11]

The inventor of [12] proposes the system shown in Fig. 5.36 which represents SICAM with 3-level phase-modulated PWM transformer voltage, which has intervals with zero transformer voltage used for commutating the load current in the output stage by shortly overlapping the conduction of two bidirectional switches. In the implementation of the switching sequence it is very similar to [5] and [10].

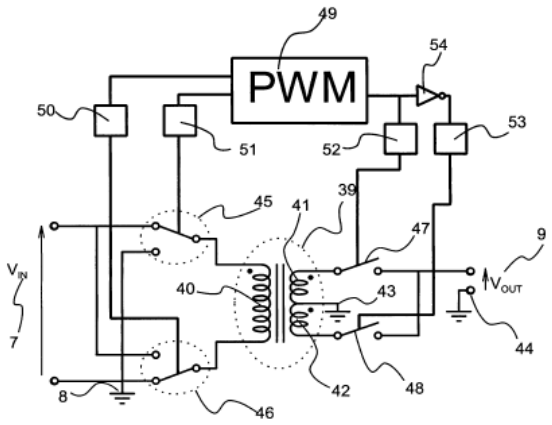

Fig. 5.36. Circuit diagram from [12]

5.8 Conclusion

There are many different approaches to creating isolated SICAMs, and despite of the minor differences between them, they can be all roughly divided into two groups: isolated SICAMs with modulated transformer voltages and isolated SICAMs with non-modulated transformer voltages.

It was shown that while SICAMs with 3-level PWM modulated transformer voltages and zero voltage intervals have the advantage of alleviating the problem of load current commutation in the output stage through overlapping the conduction of the bidirectional switches during those intervals, they are not economically feasible for multi-channel audio systems and have some practical implementation drawbacks.

On the other hand, SICAMs with 2-level non-modulated transformer voltages have the advantage of reusing the primary stage and transformer in multi-channel audio systems and alleviate the construction of additional auxiliary power supplies, but are unfortunately characterized by troublesome commutation of the load current between the outgoing and incoming bidirectional switch in the output stage. The topologies and control methods which will be presented in the next two chapters will concentrate almost entirely on solving the aforementioned load current commutation problem in SICAMs with non-modulated transformer voltages.

In this chapter several possible arrangements of bidirectional switches were presented. They all have distinct advantages and drawbacks, but it was shown that the 4QSW with common-source connection of two MOSFETs is the preferred one for audio applications, since it necessitates just two discrete components and a single isolated power supply for the gate drive, while at the same time providing low distortion and almost linear and purely resistive behavior at lower output levels. Even more, with a special load grounding technique, a simple level shifter and driver can be constructed for driving the bidirectional switches without need for expensive transformers and optocouplers.

Most of the patents in the field of HF-link converters describe isolated SICAMs with modulated transformer voltages, which are not very appropriate for audio applications, especially not for multichannel audio. Just few of them propose isolated SICAMs with non-modulated voltages, but in most of the cases the commutation of the load current in the output stage is not handled appropriately or leads to large amount of power loss. Therefore it is believed that there is still space for improvements in the field of HF-link conversion, as it will be shown in the following chapters.

6

Topologies for isolated SICAMs

"God does not care about our mathematical difficulties. He integrates empirically."

- Albert Einstein

It was already shown in Chapter 5 that the only economically feasible isolated SICAM is the one with switching stages on both the primary and the secondary side, separated by HF-link transformer. In this case, special modulation techniques can be used so that the HF-link transformer does not "see" the LF content of the audio signal to be amplified and thus its size is decreased. It was also shown that from a multi-channel audio perspective, as well as some already mentioned practical considerations, the SICAM approach with non-modulated transformer voltages is advantageous.

In this chapter, main focus will be on the topologies for isolated SICAMs with non-modulated transformer voltages. The input stage and the output stage will be dealt with separately, but bearing in mind that they are to be dedicated one to another and connected with an isolation transformer as HF-link.

6.1 Input stage

6.1.1 Introduction

The input stage of the isolated DC-AC SICAM shown in Fig. 5.2 should accept the electrical energy from the grid in a form of DC voltage from a simple AC-DC power supply (mains rectifier and storage capacitor) and transfer it through the isolation barrier, i.e. over the HF transformer. Since in the class of DC-AC SICAMs discussed in this chapter audio reference is not used in any way to modulate the transformer voltages, the input stage only role is to transfer the energy received from the power supply to the secondary side according to the output stage demands and this is what solely limits the possible output voltage waveform.

Turning to magnetics basics and Faraday and Ampere laws, it is known that magnetic energy can be stored in a piece of magnetic material by applying DC or AC electrical current through an excitation coil wound around the magnetic core, called also primary winding. It is assumed that beside the excitation winding, one or more windings are situated on the same core too. Although the character of the current through the excitation coil used for energy transfer can be freely selected, one should be aware that even in the case of DC current, energy is impressed into the magnetic core during the transient process of magnetization, which is actually characterized with variable voltages across the coil. When the transient process has ended, in the DC steady-state situation no voltages are induced in either the excitation winding or the rest of the windings. The internal magnetic flux build-up Φ of the magnetic core is determined by the time integral of the induced voltage v_i :

$$\Phi = \frac{1}{N} \int_0^t v_i(\tau) d\tau \tag{6.1}$$

where N is the number of turns of the excitation coil.

In the case of the electrical energy transfer through a HF isolation transformer with two windings - primary and secondary, there is no need for storing energy in the magnetic core, but rather transferring it over. This means that there is no need for air gaps in the magnetic core in order to reduce the magnetization inductance and increase the stored energy associated with it. So, a symmetrical AC voltage waveform v_1 should be applied across the transformer primary winding during one switching period T_s to cause magnetic flux Φ reset at the end of each complete switching action of the input stage:

$$\Phi = \frac{1}{N_1}\int_0^{T_s} v_1(\tau)d\tau = 0 \tag{6.2}$$

where N_1 is the number of turns of the primary winding.

The magnetic flux swing in the common magnetic core will induce voltage v_2 across the secondary winding, given by:

$$v_2 = N_2\frac{d\Phi}{dt} \tag{6.3}$$

where N_2 is the number of turns of the secondary winding.

When an operational output stage is connected to the transformer secondary winding, induced voltage will cause a current through it, in that way closing the cycle of energy transfer through the transformer. Although this discussion may seem notorious, it leads to an important conclusion. In this class of isolated DC-AC SICAMs, there is no known limitation on the waveform of the AC voltage applied across the transformer primary winding by the input stage, except for it being symmetrical, or at least having an average value of zero during one switching cycle T_s to allow for magnetic core flux reset:

$$v_{1,av} = \frac{1}{T_s}\int_0^{T_s} v_1(\tau)d\tau = 0 \tag{6.4}$$

It can be, however, noted that a designer should prefer transformer waveforms which transfer the same power with lowest peak voltage values, in this way reducing the stress on the switches in the subsequent output stage. This means that flat rectangular waveforms are preferred over some odd-shape waveforms with very high crest factors, except for the cases where these waveforms have other advantages, like Zero Voltage Switching (ZVS) or Zero Current Switching (ZCS) and reducing EMI with resonant converters.

If it is difficult to conclude about the shape of the applied primary voltage waveform, its frequency can be certainly discussed. It is widely recognized that, regarding the magnetic design, the switching frequency i.e. the frequency of the applied AC voltage waveform should be increased in order to decrease the magnetic flux swing Φ (6.1) and the corresponding magnetic induction swing B, which leads to smaller magnetic components and cheaper designs. Limiting factor for the switching frequency is in the way the energy losses are created in the combination of the input stage and the HF transformer.

As far as this basic magnetic transformer overview is concerned, it may seem that the energy transfer is lossless. However, this is not the case, since losses are created in the transformer magnetic core as hysteresis losses and eddy-current losses, as well as in the windings as DC conduction losses and AC skin and proximity effects. These losses are not constant, but they are strongly dependent and increase with the frequency and magnitude of the voltages and currents applied to the windings, which will define the magnetic flux levels. The applied primary voltage waveform is created by the switching action of the switches in the input stage, which also represents a lossy process even when no load

current, except the transformer magnetization current is flowing through them. These are the so called switching losses, which are predominantly dependent on the MOSFET parasitic components, frequency of the switching as well as on the magnitude levels of the conducted current being switched and reverse voltage being blocked. On the other hand, conduction losses of the saturated switches are dependent on the components internal resistance and conducted currents, and are therefore frequency independent. Eventually, it is concluded that the switching frequency selection of the input stage should be approached very cautiously, and a suitable optimization method should be developed to determine the best operating point of the compound "input stage+transformer" which is capable of delivering the necessary power to the output stage with minimal losses and at the same time keeping the input stage volume and cost low.

Another important factor when discussing the input stage is the audio performance of the output stage. Although not obvious at this point, the switching frequency of the input stage will affect the performance of the audio amplifying output section in terms of generated HF voltage switching harmonics, since there is no noise decoupling through the conventional DC-bus capacitors. This will primarily depend on the type of the control scheme used to operate the input and the output stage, but in general terms some level of synchronized operation is preferred. This, in turn, will set a limit on the possible set of input stage switching frequencies. In another PWM method for HF-link converters to be presented later, the frequency of the HF-link also appears as a frequency of the output voltage ripple. Therefore, the switching frequency of the input stage should be high enough not to interfere with the control structure of the output stage, and to be far away from the baseband of interest. Otherwise, audio performance deterioration should be expected or even instability can be induced by severe switching within the output stage closed-loop control bandwidth.

6.1.2 Topologies for the input stage

It is certainly advantageous to create an input stage which would operate with higher switching frequencies (hundreds of kiloHertz), leading to smaller HF transformer and EMI filter on the mains side, and at the same time having low losses, thus improving the efficiency of the overall SICAM. Taking a look at the input stage only, an important limiting factor are the switching losses, which can become especially severe when considering the magnitude of the DC voltage rectified directly from the mains. Therefore, special attention should be payed to those topologies or control strategies which can provide lower switching losses on expense of minor extra cost or extra control effort. On the other hand, hard-switched inverter topologies with advanced switching components can provide a simple and reliable solution with comparable performance.

Following topologies were found interesting for further research:

- **Resonant converters**: series, parallel or series-parallel (LCC) - especially popular for high frequency and lower power converters, offering very low switching losses and sinusoidal output waveforms with low THD and EMI, but lack of suitable design techniques as well as some application-specific drawbacks make them a less preferable choice,
- **Soft-switched ZVS PWM inverters** with an emphasis on phase-shift control - an extension to the classical full-bridge PWM converters which can provide near zero switching losses (ZVS) for a wide range of load currents, only with minor changes in the control algorithm and possible addition of capacitors and inductor, and
- **Hard-switched PWM inverters** found in many conventional SMPS for commercial applications.

6.1.3 Resonant converter as input stage

When compared to the "classical" class D audio power amplifiers, the unrestricted SICAM structure itself should provide topological means for lowering the losses and improving efficiency. That is why the resonant converters, which are known for their energy efficiency and compact design at high switching frequencies, appear to be an interesting alternative to investigate for an input stage. Associated voltage and current waveforms are almost purely sinusoidal, so it is possible to use a train of this sinusoidal voltage pulses in the output stage to construct the desired audio output voltage using PDM or to create larger pulses with variable width to resemble traditional PWM.

Resonant converters can be found in several different topologies, depending on the topology of the switches or the resonant tank structure. Apart from resonant-switch converters, which are not investigated herein, the most popular switching topologies for resonant converters are class E, class D, half-bridge and full-bridge [13]:

- **Class E** resonant converters comprise of only one active switch, but its high voltage and current stress (peak switch voltage $U_{sw,p} \approx 3.5V_d$ and peak voltage current $I_{sw,p} \approx 3I_d$) severely aggravate the practical implementation, especially when the converter is supposed to switch the DC input voltage rectified directly from the AC mains.
- **Class D** i.e. totem pole resonant converter combines lower voltage and current stress with low component count - only one switch more than the class E resonant converter.
- **Half-bridge** and **full-bridge** resonant converter topologies also have lower component stress like the Class D resonant converter, but the component count increases.

Due to the aforementioned advantages, Class D resonant switching converter is preferred over all of the other resonant approaches.

In the basic resonant converters, the resonant tank can consist from: series LC in Fig. 6.1a, parallel LC in Fig. 6.1b and series-parallel LCC in Fig. 6.1c.

However, some problems associated with the implementation of resonant converters appear right away. For example, a lack of suitable "engineering" time-domain design methods for exact representation of resonant converter waveforms leads to using approximate frequency-domain methods [60], [61], [62], [63], [64], i.e. sinusoidal analysis at the dominant frequency, depending on the excited modes of the resonant tank by the switching action of the converter itself. Time-domain approaches [65], [66] are found to be too complex, offering accuracy and flexibility (both continuous and discontinuous conduction modes of the resonant converter) which is for most of the times actually not needed.

Beside the analysis problem, some technical and performance problems were found even more restrictive and this will be explained in detail in few subsections, regarding the corresponding resonant converter topology.

It should be emphasized, however, that all of the authors of resonant converter references found in the literature were using resonant converters in rectification schemes, so there is actually little reference [67] to resonant converters used in combination with subsequent bidirectional bridge or cycloconverter for creating AC waveforms.

Series resonant converter (SRC)

In the SRC shown in Fig. 6.1a, both resonant elements L, C_s are in series with the load. This has an advantage of having a DC blocking capacitor in series with the HF transformer, thus successfully avoiding any DC saturation. The efficiency at idle is very high, since there can be no circular current through the resonant tank at no load. SRC can only step down the output voltage, which for a converter operated from rectified AC mains voltage is not a disadvantage, since the desired output voltage will be always lower.

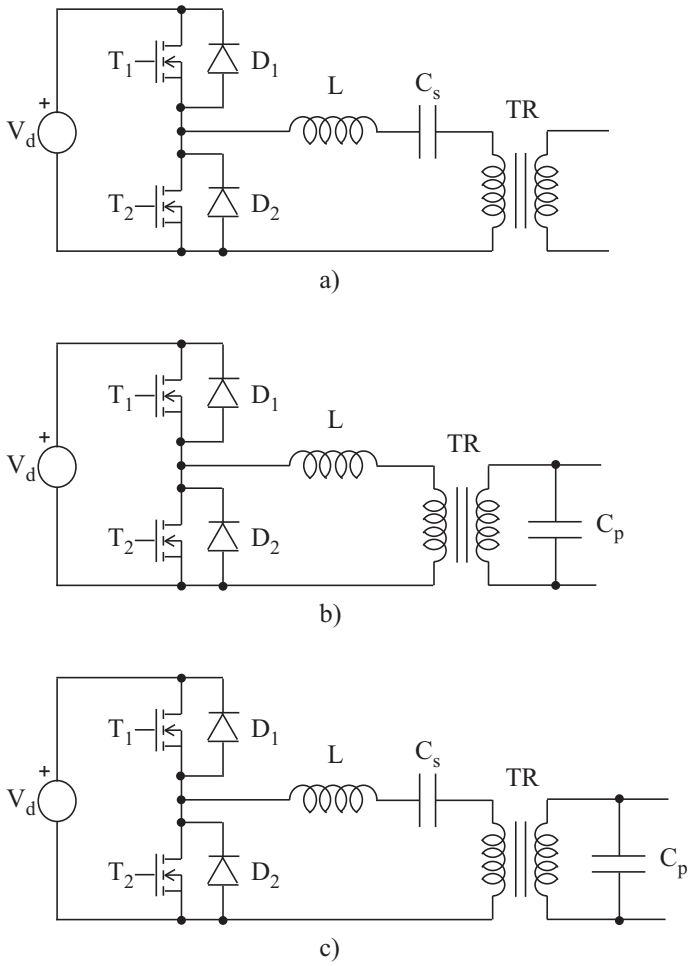

Fig. 6.1. Class D resonant converter types: a) series LC, b) parallel LC and c) series-parallel LCC

The main disadvantages are caused by the same elements, which were regarded as the major benefit of the topology. When reconsidering higher power levels and higher ripple load currents, the series capacitor C_s can become bulky, thus compromising the light design of the SICAM. Output voltage control at lighter loads is problematic, so a wide range of switching frequencies is required in order to compensate for small load variations. When operating near the resonant frequency $f_s \approx f_r$, output short circuit can result in huge overvoltages because of the undamped resonant tank, so a fast control loop is a necessity.

Parallel resonant converter (PRC)

In the PRC shown in Fig. 6.1b, the capacitor C_p appears in parallel to the load. The converter itself has a voltage step-up and voltage step-down properties, depending on the switching frequency f_s to resonant frequency f_r ratio f_s/f_r, which is certainly an advantage over the SRC. And even more: output voltage control with wide range of load variation is achieved with smaller switching frequency adjustments. This means that even at light load, output voltage control can be unaffected. Another important feature of PRC is that even when operating at switching frequencies near the resonant frequency of the resonant tank $f_s \approx f_r$, output short circuit current is essentially limited by the inductor L impedance.

The major drawback of PRC is due to the circular currents flowing in the resonant tank L, C_p even without any load applied, resulting in very low power efficiency at idle. On the other hand, at light load the quality factor of the resonant tank Q rises, so fast output voltage control must be used to avoid any possible overvoltages.

Series-parallel resonant converter (SPRC)

SPRC shown in Fig. 6.1c attempts to take advantage of the best features of SRC and PRC and at the same time mitigate some of their drawbacks. That is why a Class D SPRC is a resonant converter of choice for many rectifying HF applications [29], [63], [64], [65], [68], [69], [70]. Therefore, a series-parallel LCC resonant converter was reconsidered for use in an isolated DC-AC SICAM, instead of the simpler SRC and PRC.

From an analysis point of view, SPRC is desirable since all the transformer parasitics can be suitably incorporated in the calculations by moving all the transformer leakage inductance to the primary and adding it to the inductor L and at the same time moving the parasitic winding capacitance to the secondary side and adding it to the capacitor C_p.

Characteristics of resonant converters when used in a SICAM

It is clear that the use of any resonant converter in an isolated DC-AC SICAM is far more demanding than the use of latter in a rectifier. Using a bidirectional bridge in the output stage, loaded with an output low pass filter and a loudspeaker essentially emerges as a widely and rapidly varying load, depending on the audio reference. One important example is the use of 2-level or 3-level PWM [14]. When using 2-level modulation, the combination of output filter and loudspeaker is always connected to the both ends of the resonant converter, thus resulting in higher no-load losses, but the resonant tank is never unloaded. The case of 3-level modulation is shown in Fig. 6.2, where a series-parallel LCC resonant converter is loaded with bidirectional full-bridge amplifier, just to get rid of these losses, but on expense of introducing some common-mode noise. The direction of the load current is the same in all of the depicted cases. In the "normal" case, current is being delivered from the resonant tank to the load, like when switches $S_1 - S_4$ are turned on. Sometimes the combination of the output filter and the loudspeaker will be connected to the same upper or lower rail essentially unloading the resonant converter and causing overvoltages on the parallel tank capacitor C_p, like when switches $S_1 - S_3$ are turned on. And even more, when returning the stored energy in the output filter and load to the resonant converter through the output stage bidirectional bridge, like when switches $S_2 - S_4$ are turned on, load current can charge the capacitors C_p, C_s to even greater voltage values and also cause unexpected rise of output voltage. Latter voltage variations happen at very short timescale and are very hard to compensate for, no matter how fast the control loop is.

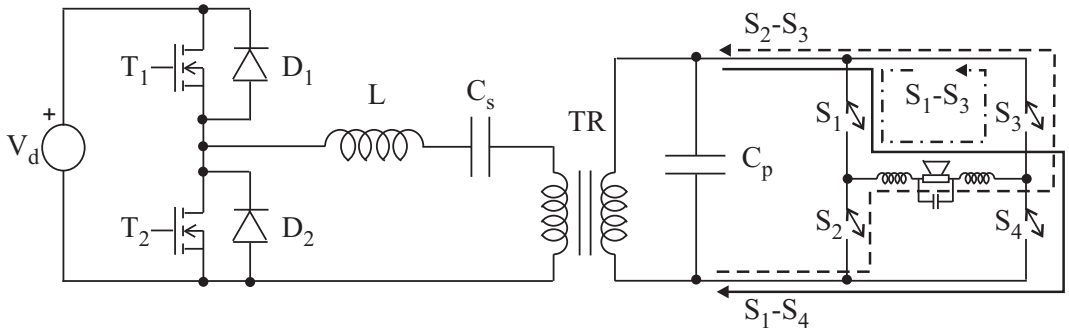

Fig. 6.2. Series-parallel LCC resonant converter loaded with bidirectional full-bridge amplifier

In conclusion: the resonant converter load current can have any direction and magnitude sustained by the loudspeaker output low-pass filter and a bidirectional bridge state, which from the resonant converter control perspective can not be predicted. Resonant

tank components L, C_s, C_p cause the resonant converter to have high output impedance, resulting in rapid output voltage perturbations which are strongly dependent on the varying load characteristics, i.e. on the switching action of the subsequent output stage. This is a major drawback which makes the use of a resonant converter without fast output voltage feedback control loop almost impossible to manage.

SPRC's output impedance $Z_o(s)$ is obtained by short-circuiting the voltage source, which essentially connects the series combination of L and C_s in parallel with C_p:

$$Z_o(s) = \frac{\frac{1}{sC_p}(sL + \frac{1}{sC_s})}{sL + \frac{1}{sC_s} + \frac{1}{sC_p}} = \frac{s^2LC_s + 1}{s^3LC_pC_s + sC_s(1 + \frac{C_p}{C_s})} \tag{6.5}$$

which is shown graphically for $L = 11.6\mu H$ and $C_s = C_p = 5.88nF$ in Fig. 6.3 and is significant even at frequencies comparable to the switching frequency.

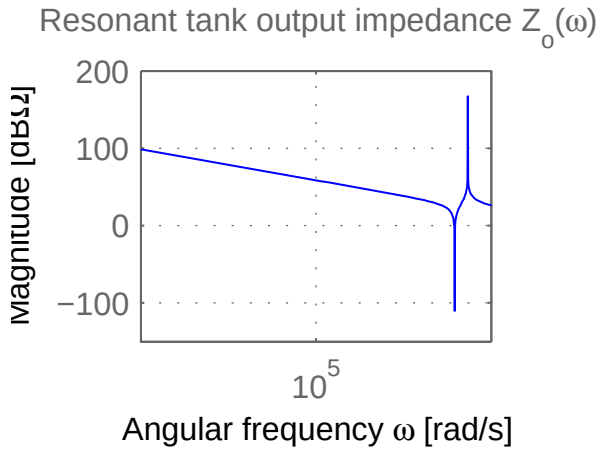

Fig. 6.3. Output impedance of an SPRC for $L = 11,6\mu H$ and $C_s = C_p = 5,88nF$

The following means for control of the resonant converter output voltage are feasible:

- Frequency control - widely used method for creating variable output voltage, due to the frequency dependant output characteristics of the resonant converters; generally this is not a desired solution since almost constant frequency operation is preferred to guarantee the same performance of the input stage all over the possible operational range and to obtain pulses with the same width or same area (Volt-seconds) for use in PDM output stage,
- Duty cycle control - this type of control is reported in [29], but it fails to achieve the desired performance, since for switching duty ratios different from $D = 0.5$ DC-offset is introduced to the resonant tank input voltage, i.e. the totem pole switches start acting as rectifiers with variable output voltage, and
- Phase control - introduced in [71]; consists of two phase-shifted PWM totem-poles forming a class D inverter with the resonant tank and the HF transformer connected in between the middle points of the poles or with two resonant tanks starting from the poles and connecting the HF transformer to the ground.

When the method of frequency control is used upon some of the resonant converters, the preferred working frequency is usually above the resonant frequency. By switching the converter at a fixed frequency higher than the resonance point of the resonant tank, the $L - C_s - C_p$ combination appears as predominantly inductive load, causing the current to lag the applied input voltage. Because of the load current conduction through the diode

antiparallel to the observed transistor whenever the opposite transistor switches off, ZVS is obtained at turn-on. By applying small capacitor in parallel to the transistor, ZVS at turn off can be achieved as well, due to the time needed for the load current to charge this dummy capacitor. Therefore, operating the resonant converters above the resonant frequency is superior in terms of switching losses and performance [61].

The method of phase control certainly looks appealing, since full control of the resonant converter output voltage can be achieved by changing the amount of energy injected into the resonant tank, and not actually changing the frequency of switching. However, this is done on expense of additional totem pole with two active switches and still the large output impedance of the resonant tank limits the performance of the input stage, making it a less preferable choice for a SICAM.

6.1.4 Soft-switched ZVS PWM inverter as input stage

Introduction to ZVS PWM inverters

Decreasing the energy loss in the input stage of a SICAM is a desirable feature, so instead of using a hard-switched PWM inverter a soft-switched ZVS PWM inverter can be implemented [72], [73], [74]. It has completely the same structure as a hard-switched PWM inverter, but the switching events are little bit altered. ZVS results in decreased switching losses, as well as reduced transistor voltage resonant ringing, which can be observed during rapid hard switching. The principle of operation will be described using Fig. 6.4.

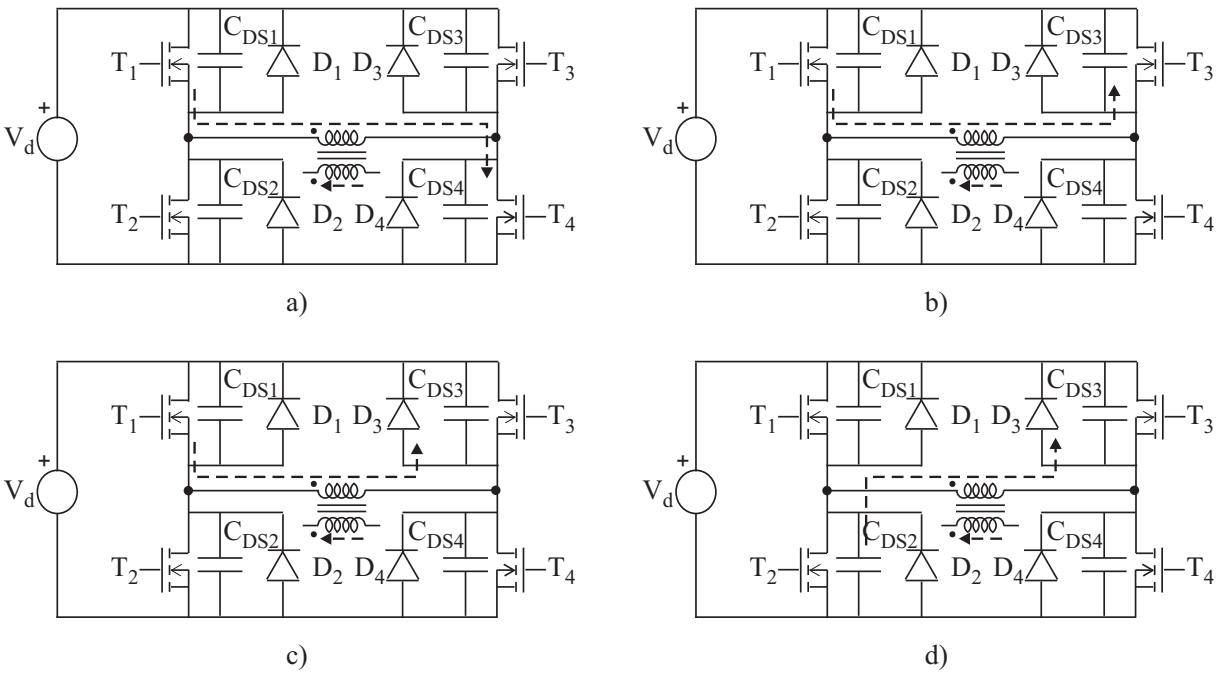

Fig. 6.4. ZVS PWM inverter: a) power delivered to the load, b) capacitance of T_3 gets discharged, c) freewheeling cycle and d) capacitance of T_2 gets discharged

The main benefit of the ZVS PWM inverter results from the intentionally programmed delay between the turn-off of one transistor and the turn-on of other transistor in a single bridge leg. During this time, no transistor in that leg conducts, and the freewheeling current sustained by the inductive nature of the load, the transformer magnetizing inductance and the transformer leakage inductance discharges the drain-to-source parasitic capacitance of one of the MOSFETs, and charges the other, allowing the ZVS. The phases of one half-cycle of output voltage are shown in Fig. 6.4 and are described as follows:

a. Diagonal transistors T_1 and T_4 are conducting, so power is delivered from the source and through the transformer to the load. Drain-to-source capacitance C_{DS3} of T_3 is charged to $+V_d$ and voltage across the drain-to-source capacitance C_{DS4} of T_4 is almost zero, i.e. C_{DS4} is discharged. Current flowing through the transistors consists from the reflected load current $(N_2/N_1)I_{load}$ and the magnetizing current I_m.
b. T_4 turns off, so the capacitance C_{DS4} gets charged and C_{DS3} gets discharged by the primary current, raising the voltage of the middle point from $0V$ to $+V_d$. This action continues until the body diode of T_3 or external diode D_3 turn on to clamp the voltage across it to one voltage drop. Turn-off of transistor T_4 is lossy, but adding an additional small external capacitance across it can keep the voltage to near zero Volts until the current through the MOSFET channel is completely switched off.
c. As soon as the voltage across T_3 reaches zero volts, transistor T_3 is turned on, producing no switching loss, i.e. ZVS at turn-on occurs. Applied voltage across the transformer is zero.
d. Transistor T_1 is now turned off, so the primary current is now diverted into the parasitic capacitances of T_1 and T_2, charging the C_{DS1} and discharging the C_{DS2}. When the voltage across T_2 reaches zero volts, it will be turned on in a non-dissipative manner, so a programmed delay must be provided for ZVS at turn-on to take place. Again, T_1 turn-off is lossy and T_2 turn-on is lossless.

It should be noted that the nature of ZVS of the two switching legs differs. In the right one the primary current consists of the reflected load current and the magnetizing current, while in the left one the dominant role in the ZVS is played by the energy stored in the primary leakage inductance of the transformer, since load current is freewheeled by the secondary side rectifiers, as described in [72].

This description corresponds to the case of switching only one leg at a time. Assuming that before switching of one inverter leg, the voltage across the transformer primary was equal to the DC bus voltage $+V_d$, then after the process of charge displace and transistor turn-off has ended the primary voltage will be zero. This situation will last until switching is performed in the second leg, resulting in reverse DC bus voltage $-V_d$ across the transformer primary. The output voltage average can be controlled by altering the delay in switching the second leg, so the converter operated in this way is referred as Phase-shift ZVS PWM inverter. The advantage of this approach is that only one MOSFET is to be turned-off and only one to be turned-on, resulting in electrical charge being displaced using the primary current between only these two parasitic drain-source capacitances. Phase-shift ZVS PWM inverter output voltage v_1 and associated switching waveforms for T_1, T_2, T_3 and T_4 are shown in Fig. 6.5a.

When both legs are switched at the same time - simultaneously, the same action of displacing the electrical charge between the MOSFET parasitic capacitances occurs. However, in this case instead of two, all of the MOSFET parasitic capacitances play a significant role at the same time. Eventually, this leads to even higher demand for energy stored in the transformer leakage and magnetizing inductances. Actually, the same switching action occurs in classical PWM inverters using the dead time instead of the programmed delay. Whenever both legs of the PWM inverter are switched simultaneously in a prescribed way using previously calculated delays to facilitate the ZVS by the freewheeling of the primary current, it will be referred as Simultaneous ZVS PWM inverter. Simultaneous ZVS PWM inverter output voltage v_1 and associated switching waveforms for T_1, T_2, T_3 and T_4 are shown in Fig. 6.5b.

At this point, a very important remark should be made. In the presently available references [72], [73], [74], soft-switched ZVS PWM inverter is used in conjunction with a

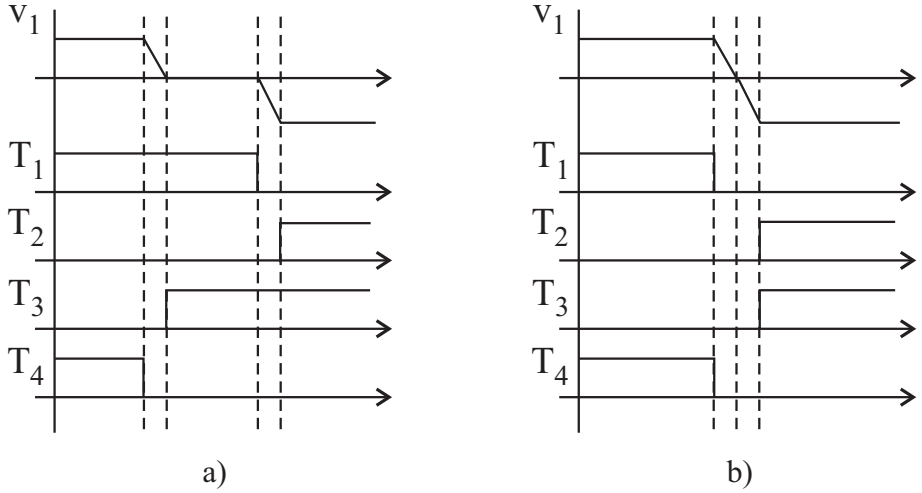

Fig. 6.5. ZVS PWM inverter output voltage v_1 and switching waveforms: a) phase-shift ZVS PWM inverter and b) simultaneous ZVS PWM inverter

rectifier on the secondary side, which results in a highly predictable primary and secondary winding current direction. In this case, energy is always transferred from the source to the secondary side rectifier. Reflected load current, as shown in Fig. 6.4 always helps the magnetizing current to displace the charge between the MOSFETs output capacitances, thus leading to ZVS at turn-on. As already mentioned in the description of the switching process, MOSFET turn-off is still lossy except in the cases when small capacitive snubbers are added in parallel to the MOSFETs.

When soft-switched ZVS PWM inverter is used with bidirectional bridge as an output stage, rectifier diodes are removed, so the primary and secondary winding current directions depend on the applied audio reference, as well as the load current direction in the output low-pass filter prior to the switching instant. Now the energy transfer can be in either direction, i.e. energy can be also regenerated from the load to the energy storage capacitor on the primary side. This makes the analysis more complex, since the primary current can be also in opposite direction from the magnetizing current, effectively aggravating the ZVS at turn-on. In this limit case, when the load current reflected to the transformer primary dominates over the magnetizing current causing total current in the opposite direction, instead of two diagonal MOSFETs, current is conducted using the corresponding antiparallel or MOSFET body diodes. This in turn results in ZVS at turn-off, and turn-on becomes a lossy process. This obviously has a resemblance with ZVS and ZCS of the resonant converter, in which it depends upon the leading/lagging character of the resonant current. The phases of one half-cycle of output voltage with a large reflected load current in opposite direction from the magnetizing current are shown in Fig. 6.6 and are described as follows:

a. Diagonal transistors T_1 and T_4 are turned on, which results in positive voltage applied across the transformer primary, but the reflected load current is flowing through the diodes D_1 and D_4 in opposite direction. This means that energy is regenerated from the load at the secondary side via the transformer to the energy storage capacitor at the primary side. Drain-source capacitance C_{DS3} of T_3 is charged to $+V_d$ and voltage across the drain-source capacitance C_{DS4} of T_4 is equal to the diode D_4 voltage drop ($V_{D_4} \leq 1V$), i.e. C_{DS4} is discharged. Current flowing through the diodes consists from the reflected load current $(N_2/N_1)I_{load}$ minus the magnetizing current I_m.

b. T_4 turns off, but the capacitance C_{DS4} can not get charged since reflected load current is flowing through the antiparallel diode D_4, keeping the voltage at near zero Volts. Turn-off of transistor T_4 is therefore lossless (ZVS) at turn-off.
c. Transistor T_3 is turned on, producing switching loss because of the voltage across it $V_{T_3} = V_d - V_{D_4} \approx V_d$. Reflected load current is diverted to discharge the parasitic output capacitance C_{DS3} of transistor T_3 and at the same time charge the capacitance C_{DS4}. As soon as this transient process has ended, the applied voltage across the transformer is zero.
d. Transistor T_1 is turned off in a lossless manner (ZVS at turn-off) and the reflected load current continues to freewheel through T_3 and D_1. Transistor T_2 is now turned on with the full DC bus voltage across it, causing large switching loss at turn-on. Current is diverted from the diode D_1 to the opening channel of transistor T_2, charging C_{DS1} and discharging C_{DS2}.

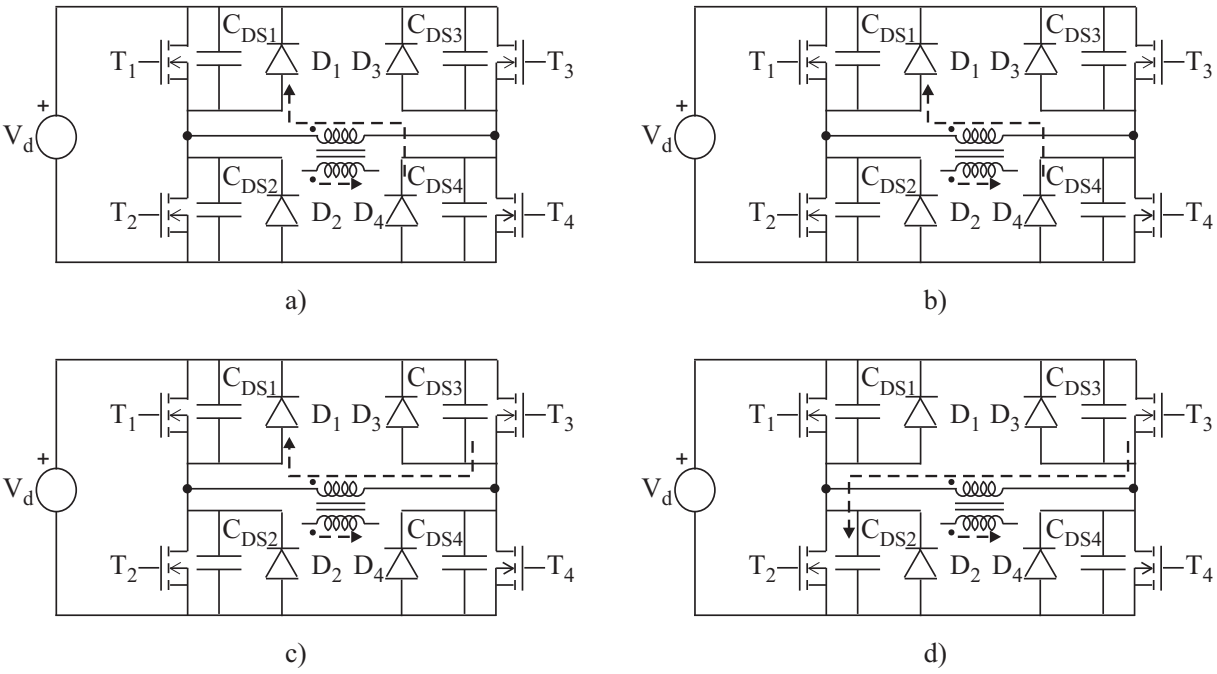

Fig. 6.6. ZVS PWM inverter with reflected load current in opposite direction from the magnetizing current: a) power regenerated from the load through D_1 and D_3, b) T_4 is turned off with ZVS, c) capacitance of T_4 gets charged and T_3 gets discharged and d) capacitance of T_1 gets charged and T_2 gets discharged

What happens in between these limit cases, when the reflected load current is opposing the magnetizing current, but is not enough to cause the total current in opposite direction and ZVS at turn-off? Obviously, the switching losses at turn-on will be reduced but not completely eliminated, if the magnetizing current was designed to solely displace the charge between the parasitic capacitances without any help from the load current. From this perspective, an intention is to have large magnetizing inductance yielding small magnetizing current, since this will make the region of partly lossy switching transitions smaller in width. As a result ZVS will depend mostly on the load current reflected to the transformer primary side. Switching losses regions in relation with the load current magnitude and direction for two different magnetizing currents $I_{m1} = 2I_{m2}$ are shown in Fig. 6.7.

Compared with the resonant converters where operation above resonance is preferred, in the ZVS PWM inverters preferred state of operation is ZVS at turn-on i.e. energy transfer from the source to the load. In this case ZVS at turn-off can be achieved by

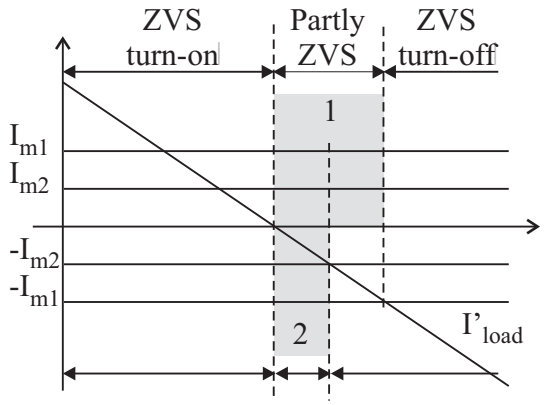

Fig. 6.7. Soft-switched PWM inverter switching losses dependance on reflected load current I'_{load} for two different magnetizing currents $I_{m1} = 2I_{m2}$

adding small external capacitors in parallel with the MOSFETs, which is usually done in the resonant converters too.

Analysis of ZVS in soft-switched full-bridge PWM inverters

In order to simplify the analysis, in the following section only the case when the load current facilitates the ZVS at turn-on or the load current being zero will be investigated.

Several problems become clear right away: if in the classical full-bridge PWM converters the aim is to moderately increase the magnetizing inductance in order to decrease the magnetizing current and the conduction losses associated with it, in the case of ZVS PWM converter magnetizing current must be of a certain level to facilitate the ZVS when the load current is insufficient to do so. If this is not done, at light loads the input stage will experience high switching losses and low conduction losses, while at heavy loads the input stage will be in ZVS offering low switching losses, while the conduction losses will increase. Sometimes, in order to allow ZVS at turn-off, additional external capacitances can be added to keep the drain-source voltage near zero until the MOSFETs completely turn off.

Charging/disharging of parasitic C_{DS} and any other external capacitances is done using the transformer primary current. One can distinguish the following cases:

- Input stage was delivering power to the output stage just prior to switching. The primary current consists from the reflected secondary (load) current and the magnetizing current. This is the most favorable case, resulting in almost sure ZVS of the input soft-switched PWM stage.
- Output stage disconnected the load prior to the switching action (freewheeling in the output stage, if provided, ceased to transfer energy back to the input stage), but the core itself is still magnetized since no opposite direction Volt-seconds were applied to reset it. Only magnetizing current is flowing through the transformer primary, and if designed properly, this should be enough to guarantee ZVS of the primary stage.
- The worst case appears when the output stage has disconnected the load, and the core itself is reset prior to the switching due to the, for example, freewheeling action of the output stage effectively shortening the secondary. In this case there is no magnetizing current, so the ZVS must be accomplished by the resonant action of energy stored in the transformer leakage inductance.

The necessary switching delay time for each of the legs will be calculated for the worst case, where only the energy in the leakage inductance facilitates the ZVS of the input stage. In this case, the leakage inductance plus any additional inductance of the

leads in the input stage forms a resonant circuit with the output parasitic drain-source capacitances of the turning-off and turning-on transistors. The process of charge displace is finished in a time interval equal to one-fourth of the resonant period:

$$t_{d,res} = \frac{T}{4} = \frac{2\pi\sqrt{L_r C_r}}{4} = \frac{\pi}{2}\sqrt{L_r C_r} \tag{6.6}$$

where $L_r = L_l + L_{add}$ is the resonant inductance, consisting of the leakage inductance L_l and any additional inductance in the loop L_{add} and C_r is the resonant capacitance.

Special attention should be payed to determine the resonant capacitance C_r. It consists from the paralleled output capacitances of two affected transistors as well as the parasitic capacitance of the transformer primary (usually very low). Simple derivation in [73] followed also herein, but with a slight alteration at the end can determine it very precisely.

The output capacitance of a MOSFET C_{oss} is usually given in a datasheet for applied drain-source voltage of $V_{oss} = 25V$, but it is far away from being constant. It is depletion dependent capacitance and therefore decreases nonlinearly with increase of drain-source voltage:

$$C_{DS}(V_{DS}, n) = C_{oss}\left(\frac{V_{oss}}{V_{DS}}\right)^n \tag{6.7}$$

where n is usually between 1/2 and 1/3.

Energy stored in the output capacitance can be calculated in the following way:

$$E = \int vidt = \int v\frac{dQ}{dt}dt = \int vdQ = \int V_{DS}C_{DS}(V_{DS}, n)dV_{DS} \tag{6.8}$$

which using the equation (6.7) transfers to:

$$E = C_{oss}V_{oss}^n \int V_{DS}^{1-n}dV_{DS} = \frac{C_{oss}V_{oss}^n V_{DS}^{2-n}}{2-n} \tag{6.9}$$

Taking n=1/2:

$$E = \frac{2}{3}C_{oss}V_{oss}^{\frac{1}{2}}V_{DS}^{\frac{3}{2}} \tag{6.10}$$

or when having two output capacitances in parallel, like in the case of the switching instant shown in Fig. 6.8a being investigated now:

$$E = \frac{4}{3}C_{oss}V_{oss}^{\frac{1}{2}}V_{DS}^{\frac{3}{2}} = \frac{1}{2}\cdot\frac{8}{3}C_{oss}V_{oss}^{\frac{1}{2}}V_{DS}^{\frac{3}{2}} \tag{6.11}$$

which, when compared with the widely known expression for the energy stored in a capacitor $E = 1/2 \cdot CV^2$, leads to the final result for the resonant capacitance:

$$C_r = \frac{8}{3}C_{oss} + C_{add} \tag{6.12}$$

where C_{add} represents the additional interwinding capacitance of the primary.

When switching both inverter legs at the same time (simultaneous ZVS PWM), drain-source capacitances appear on the place of each of the MOSFETs in the full bridge, like shown in Fig. 6.8b. This essentially connects the paralleled output capacitances of each

leg in series together and with the resonant inductance L_r, which results in two times lower resonant inductance compared with (6.12):

$$C_{r,sim} = \frac{4}{3}C_{oss} + C_{add} \tag{6.13}$$

Although this means that the resonant time $t_{d,res}$ in (6.6) has decreased for a factor of $\sqrt{2}$, the actual demand of magnetic energy stored in the resonating inductance for charge displace has increased by a factor of 2, since now there are two MOSFET capacitances which should be discharged and their charge displaced. It should be noticed, however, that the role of the DC-blocking capacitor C_{DC} during these transitions is only marginal, since its high capacitance keeps it discharged during normal operation and experiencing very low impedance at the high switching frequencies.

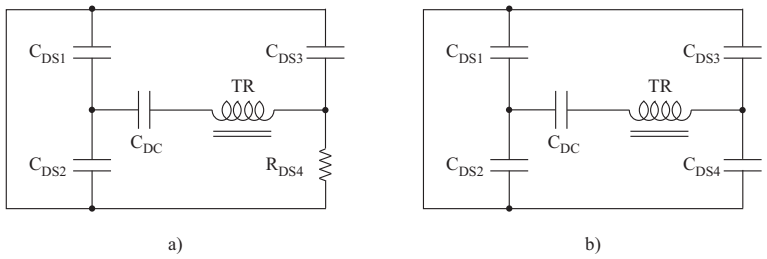

Fig. 6.8. Determining the resonant capacitance C_r when switching: a) single leg and b) both legs at the same time

After the initial resonant delay time $t_{d,res}$ has been determined, the minimum value of the magnetizing current $I_{m,min}$ can be calculated, which can store enough magnetic energy in the leakage inductance of the transformer to perform the charge displace. Using the equation (6.11) and the magnetic energy stored in the leakage inductance:

$$\frac{1}{2}L_l I_{m,min}^2 = \frac{4}{3}C_{oss}V_{oss}^{\frac{1}{2}}V_{DS}^{\frac{3}{2}} \tag{6.14}$$

the final expression for the minimum magnetizing current becomes:

$$I_{m,min} = 2\sqrt{\frac{2}{3}\frac{C_{oss}V_{oss}^{\frac{1}{2}}V_{DS}^{\frac{3}{2}}}{L_l}} \tag{6.15}$$

Minimum magnetizing current $I_{m,min}$ will be achieved with a maximum magnetizing inductance $L_{m,max}$:

$$L_{m,max} = \frac{\Phi}{I_{m,min}} = \frac{V_{in}t_{on}}{I_{m,min}} \tag{6.16}$$

where the leakage inductance L_l has been neglected.

In most of the cases, the transformer is designed using some method where the total losses in the transformer, consisting of core and copper losses, are minimized choosing the number of primary windings and the wounding technique (interleaving, paralleling several windings with smaller diameter -Litz wire etc.). Of course, this may lead to a design where the minimum leakage inductance and maximum magnetizing inductance are already set, and the latter is too large to cause enough magnetizing current to facilitate the ZVS. Gapping the magnetic core will help to increase the leakage inductance and decrease the magnetizing inductance, which in turn has a positive effect upon the magnetic energy stored in the transformer leakage inductance. This will also lead to slight

linearization of the magnetic core characteristic, making it less susceptible to DC saturation and flux creepage. However, the energy efficiency will be compromised due to the increased magnetizing current at all output powers, but especially at idle. So, a sort of an optimization procedure should be undertaken to determine the optimal ratio of the switching and conduction losses, which will lead to lowest overall losses at idle.

Other approaches has been investigated in literature too, like adding an inductor or even saturable inductor in series with the transformer primary winding [72], which allows ZVS operation of the converter down to very low loads. In the first approach the amount of stored magnetic energy in the primary path i.e. the resonant inductance L_r is increased by adding extra inductance and not by increasing the transformer magnetizing current, like in the case of gapping the magnetic core. In the latter case, the saturable inductor used in conjunction with a DC-blocking capacitor is released during freewheeling when the primary current reaches zero Amperes and it holds it that way, so ZCS at both turn-on and turn-off of particular switches is observed [75].

No matter the means used to achieve ZVS, caution should be exercised not to rely solely on the calculated values for the resonant delay. This is especially true in the unloaded output stage case. In the cases where the implemented resonant delay $t_{d,res}$, calculated according to (6.6) is low, and the magnetizing current is unable to perform the charge displace in the programmed time due to the unrealistically low maximum magnetizing inductance $L_{m,max}$, the transistor in one leg is turned-on although the output capacitance of the other transistor is not fully charged. This means that a large inrush source current will flow through the output capacitance of the turning-off transistor, which will facilitate the complete discharge displacement and eventually lead to complete turn-off of the desired transistor. This is certainly not desired, but otherwise very conservative delays should be implemented resulting in huge performance degradation. Therefore, some trade-offs must be done and this is especially important at higher DC-bus voltages, when the charge stored in the MOSFET's output capacitance is correspondingly large.

One possible approach is the following: calculate the maximal (very conservative) delay time $t_{d,max}$ to discharge one output capacitance and compare it with the resonant delay time $t_{d,res}$ (6.6). An assumption is made, that the input stage is unloaded, so that the constant magnetizing current I_m is the only current performing the charge displace.

$$\begin{aligned} t_{d,max} &= \frac{Q}{I_m} = \frac{1}{I_m}\int_0^{V_{in}} C dV = \frac{2L_m}{V_{in}T_s}\int_0^{V_{in}} C_{oss}\big(\frac{V_{oss}}{V}\big)^n dV = \\ &= \frac{2L_m}{V_{in}T_s} C_{oss} V_{oss}^n \frac{V^{1-n}}{1-n}\Big|_0^{V_{in}} = \frac{2L_m}{V_{in}T_s} C_{oss} V_{oss}^n \frac{V_{in}^{1-n}}{1-n} = \frac{2L_m C_{oss}}{T_s(1-n)}\big(\frac{V_{oss}}{V_{in}}\big)^n \end{aligned} \tag{6.17}$$

which for $n = 1/2$ becomes:

$$t_{d,max} = \frac{4L_m C_{oss}}{T_s}\sqrt{\frac{V_{oss}}{V_{in}}} \tag{6.18}$$

In the cases where this maximum delay time $t_{d,max}$ is several times bigger than the resonant delay time $t_{d,res}$, it makes no sense in using either of them, since using $t_{d,max}$ results in huge performance degradation and using $t_{d,res}$ results in large capacitive inrush current and stress. Therefore, letting the half of the charge stored in the output capacitance to be displaced by the magnetizing current I_m and and the rest of it with the short-circuit current I_{sc} makes an interesting alternative. Because of the nonlinear dependance of the output capacitance from the applied voltage (6.7), a coefficient a is introduced which determines at which drain-source voltage $V_{DS} = aV_{in}$ the half of the charge Q is already displaced:

$$\begin{aligned}
&\frac{Q}{2} = \int_0^{aV_{in}} C_{oss}(\frac{V_{oss}}{V})^n dV = \int_{aV_{in}}^{V_{in}} C_{oss}(\frac{V_{oss}}{V})^n dV \\
&\int_0^{aV_{in}} V^{-n} dV = \int_{aV_{in}}^{V_{in}} V^{-n} dV \\
&\frac{V^{1-n}}{1-n}\Big|_0^{aV_{in}} = \frac{V^{1-n}}{1-n}\Big|_{aV_{in}}^{V_{in}} \\
&(aV_{in})^{1-n} = V_{in}^{n+1} - (aV_{in})^{1-n} \\
&2a^{1-n}V_{in}^{1-n} = V_{in}^{1-n} \\
&\Rightarrow\ a = (\frac{1}{2})^{\frac{1}{1-n}}
\end{aligned} \tag{6.19}$$

which for $n = 1/2$ gives:

$$a = \left(\frac{1}{2}\right)^2 = 0,25 \tag{6.20}$$

Following the same procedure in (6.17), the half-charge delay time $t_{d,hc}$ can be determined:

$$\begin{aligned}
t_{d,hc} &= \frac{Q}{I_m} = \frac{1}{I_m}\int_0^{aV_in} C dV = \frac{2L_m}{V_{in}T_s}\int_0^{aV_in} C_{oss}(\frac{V_{oss}}{V})^n dV = \\
&= \frac{2L_m}{V_{in}T_s} C_{oss} V_{oss}^n \int_0^{aV_in} V^{-n} dV = \frac{2L_m}{V_{in}T_s} C_{oss} V_{oss}^n \frac{V^{1-n}}{1-n}\Big|_0^{aV_{in}} = \\
&= \frac{2L_m}{V_{in}T_s} C_{oss} V_{oss}^n \frac{a^{1-n}V_{in}^{1-n}}{1-n} = \frac{2L_m C_{oss}}{T_s(1-n)} a^{1-n}\big(\frac{V_{oss}}{V_{in}}\big)^n
\end{aligned} \tag{6.21}$$

which for $n = 1/2$ becomes:

$$t_{d,hc} = \frac{4L_m C_{oss}}{T_s}\sqrt{a}\sqrt{\frac{V_{oss}}{V_{in}}} = \frac{1}{2}\cdot\frac{4L_m C_{oss}}{T_s}\sqrt{\frac{V_{oss}}{V_{in}}} = \frac{1}{2}t_{d,max} \tag{6.22}$$

So, reducing the maximum delay time to half allows the inrush capacitive current to displace the other half of the charge stored in the output capacitance of the MOSFET much faster than the magnetizing current itself.

Utilization of the primary side DC-blocking capacitor in series with the transformer is usually referred as unsuitable engineering practice. Leaving aside the increased volume and price of the product, adding a series capacitor to cope with any primary side imbalance is potentially dangerous in terms of unequal charging (i.e. voltage) of the capacitor during the positive and negative half-cycles, thus resulting in uneven alternate primary voltage pulses applied across the secondary side load. Therefore, larger blocking capacitance C_b is needed to mitigate the situation and lower the imbalance voltage ΔV as a result of unequal charging ΔQ during each of the half periods ($\Delta V = \Delta Q/C_b$). Although the wish is to avoid this approach, it is still a practice of choice when compared with the other techniques to cope with the imbalance problem, like the current-mode control and different balancing techniques for the primary current, which necessitate use of current transformers [76].

At the end, it is emphasized that the necessary delays for the legs of the ZVS PWM inverter largely depend on the character of the output stage. In the case of a simple rectifier like in [72], [73], [74], both legs can have different delays due to the different currents which displace the charge in each of them: in one leg the charge displacement is always done

with the reflected load current through the output inductor (current source) plus the magnetizing current and in the other leg the charge displacement is always resonant with the leakage inductance. However, in the case of an output stage in a form of a bidirectional bridge governed by a superimposed audio reference, input stage can not know what is the exact configuration of the initiated bidirectional switches, so the necessary delay times may vary at a large scale. Designing it conservatively for the worst case seems to be the only solution, which tends to fit all of the cases, except maybe for the lightest loads, when the load current actually is not so large and the conduction and switching losses are already low.

6.1.5 Hard-switched DC-AC inverter as input stage

The topology of the full-bridge hard-switched DC-AC inverter is the same as the one shown in Fig. 6.4 for the ZVS PWM inverter, except that there are no additional capacitors and inductors to reduce the switching losses and the necessary blanking (dead) time is much lower than resonant delay time $t_{d,res}$. Other commonly used hard-switched DC-AC inverter topologies include the push-pull and half-bridge topologies, where the component stress is generally lower and performance is higher than the simple single switch topologies.

As already mentioned in previous sections, many advanced soft-switched inverter topologies like the resonant converters and ZVS PWM inverters have found wide usage in conventional isolated SMPS and other DC-DC converters. Not many applications are reported with the latter technologies in DC-AC converters, and especially not in the very challenging HF-link converters this part of the thesis is dealing with, where no DC-bus is existing on the secondary side. The main advantage of the HF-link converter, but also its Achilles' heel, is the non-existence of intermediate energy storage on the secondary side, which can dampen any difference between the energy sourced by the input stage and consumed by the output stage. This was shown to be, for example, the greatest problem with the resonant input stages, where the unrestricted load current flow between the input and the output stage becomes a large source of perturbations of the resonant tank voltage. On the other hand, ZVS PWM inverter without any capacitor on the secondary side will have HF-link voltage with shape far from rectangular, since all those (relatively) long charging and discharging processes of the switches' parasitic capacitances will immediately be seen by the output stage and the load. Due to the high switching frequency of the input and output stage in a SICAM audio power amplifier, this ZVS operation and the associated load voltage disturbances can potentially lead to lower audio performance.

When compared to all the previous technologies, it is believed that the hard-switched DC-AC inverter input stage can provide the most uniform voltage levels and continuous power flow needed by the output stage for best audio performance. Together with the wide variety of topologies suited for each and every output power level, simple control principles, as well as the continuous development of better power semiconductor components for improved efficiency, hard-switched inverters were selected as input stage in SICAM.

6.1.6 Integration of the inverter input stage within the SICAM

DC-AC inverters being either push-pull, half-bridge or full-bridge, have a desirable property of low output impedance, which makes the output voltage almost unaffected even by large load current variations. The output voltage they produce has a rectangular form, which results in two possible implementations:

- **PDM** - AC HF rectangular-shape pulses are created on the secondary side of the HF transformer, which are then used by the PDM output stage to create train of positive

and negative voltages across the load to resemble the desired audio signal, as shown in Fig. 6.9a, or

- **PWM** - AC rectangular-shape pulses with a frequency chosen to optimize the losses and the volume of the input stage and HF transformer are transferred to the output stage, then subsequently chopped and inverted by the bidirectional bridge according to the audio reference in a PWM manner, as depicted in Fig. 6.9b.

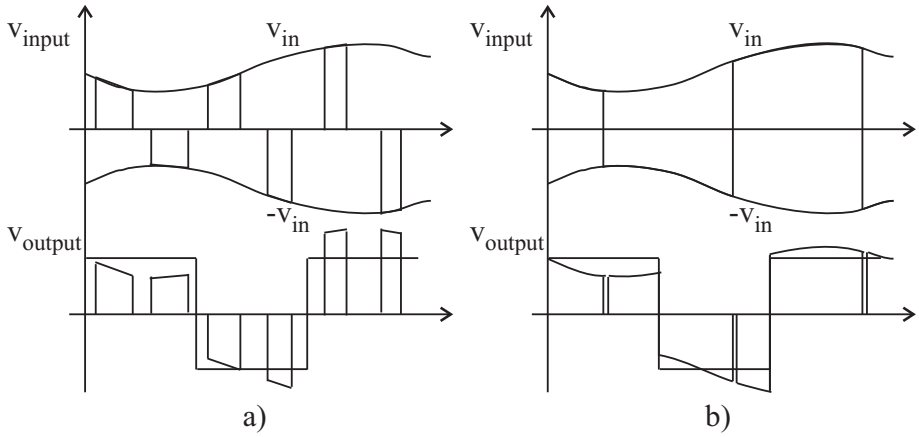

Fig. 6.9. Input and output stage output voltage waveforms: a) PDM and b) PWM, with the dashed line showing the desired output stage output voltage

For PDM SICAM, a phase-shifted version of the full-bridge HF ZVS PWM inverter input stage can be advantageous, since the duration of the power pulses can be altered according to the input voltage magnitude to deliver the same pulse area (Volt-seconds) at any moment, which will decrease the burden imposed on the output stage control circuitry. For the approaches with modulated transformer voltages, modulating the pulse width can give another additional degree of freedom to improve the audio performance and reconstruct the desired audio waveform, beside the pulse density variable.

For a simple PWM SICAM, ZVS PWM inverter with medium switching frequency and maximum duty cycle can be used, since energy must be transferred to the output stage continuously all the time. This makes it also easier for obtaining auxiliary power supplies for control biasing and isolated gate drives.

For satisfactory audio performance it is necessary that the switching frequency is very high, which makes possible to achieve control bandwidth several times higher than the audio signal bandwidth. What is the exact switching frequency needed will primarily depend on the selected modulation and control principle, but it is widely known that PWM compared to PDM requires much lower switching frequency for providing the same control bandwidth, which makes PWM a preferred choice over PDM.

6.1.7 Overdimensioning of the input stage in SICAMs

One very important issue to be discussed at this point is the need for overdimensioning the input stage in isolated SICAM based on the HF-link conversion principle [77], in order to be able to handle the reactive power flow from the load back to the output stage. In the conventional solution with a separate SMPS and Class D audio power amplifier, this reactive energy is stored in the DC-link capacitors, and its flow back to the primary side is prohibited by the presence of the secondary-side rectifiers. These two quite different cases are shown in Fig. 6.10 with half-bridge on the primary side and single-ended audio power amplifier on the secondary side.

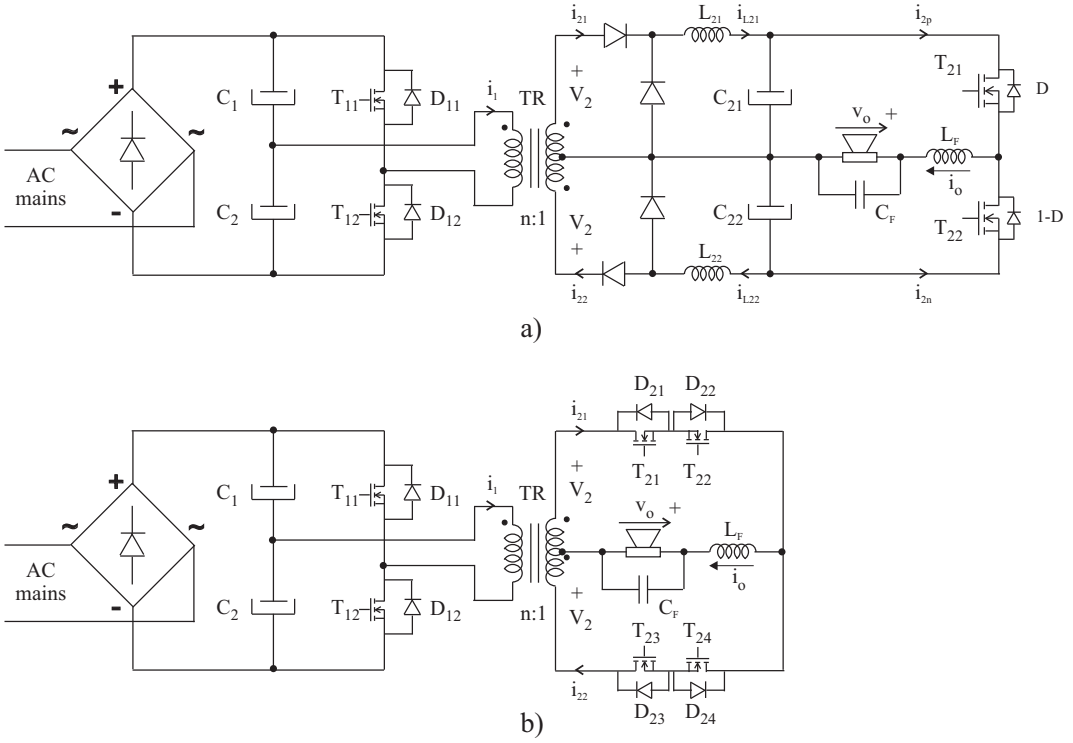

Fig. 6.10. Electrical scheme: a) Conventional SMPS + Class D audio power amplifier and b) SICAM

Calculation of the input stage overdimensioning factor ODF for SICAM with regard to the conventional SMPS and Class D audio power amplifier solution can be performed by comparing the currents drawn from the input stage in both cases:

$$ODF = \frac{I_{1,SICAM}}{I_{1,SMPS}} \tag{6.23}$$

It is expected that the input stage overdimensioning factor is bigger than 1, $ODF > 1$, since the input stage in SICAMs must handle both the active and reactive power flow.

In the case of the conventional SMPS and Class D audio power amplifier shown in Fig. 6.10a, average currents through the upper and lower MOSFET are defined as:

$$\begin{aligned} I_{2p} &= DI_o \\ I_{2n} &= -(1-D)I_o \end{aligned} \tag{6.24}$$

where D is the upper MOSFET duty cycle and the load current I_o through a resistive load R for a sinusoidal reference is:

$$I_o = \frac{V_o}{R} = \frac{V_m \sin(2\pi f_m t)}{R} \tag{6.25}$$

where I_o and V_o are equal to the load current i_o and load voltage v_o with neglected switching ripple, while V_m and f_m are the modulating sinewave magnitude and frequency correspondingly.

Output voltage of the Class D audio power amplifiers is:

$$V_o = (2D-1)V_2 \tag{6.26}$$

which leads to the following expression for the duty cycle D:

$$D = \frac{1}{2}\left(1 + \frac{V_o}{V_2}\right) \tag{6.27}$$

Combining equations (6.25) and (6.27), following expressions for the average MOSFET currents in (6.24) are obtained [78]:

$$\begin{aligned} I_{2p} &= \frac{1}{2}\left(1+\frac{V_o}{V_2}\right)\frac{V_o}{R} \\ I_{2n} &= -\frac{1}{2}\left(1-\frac{V_o}{V_2}\right)\frac{V_o}{R} \end{aligned} \tag{6.28}$$

The waveforms of the average MOSFET currents of the Class D audio power amplifier I_{2p} and I_{2n} with $R = 8\ \Omega$, $V_2 = 45$ V, $V_m = 40$ V and $f_m = 1$ kHz are depicted in Fig. 6.11. It is visible that during half of the modulating period $T_m = 1/f_m$ there is current flow from the load to the capacitors C_{21} and C_{22} on the secondary-side DC-bus.

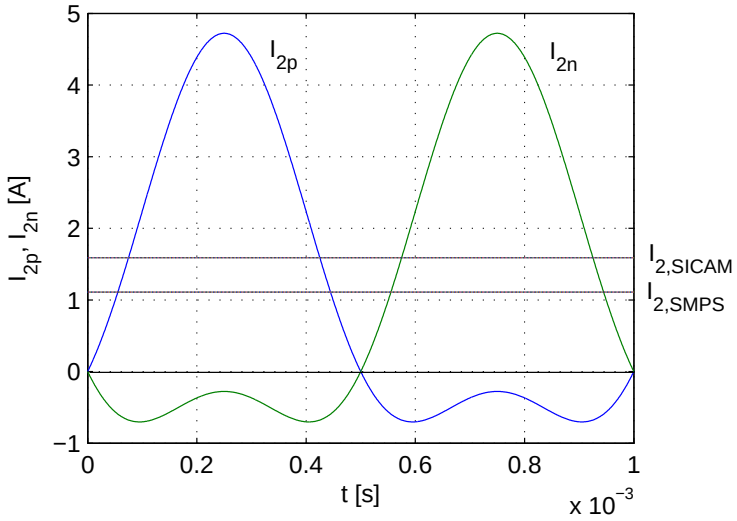

Fig. 6.11. Class D audio power amplifier average MOSFET currents and average secondary-side SMPS and SICAM currents

If the operation of the conventional SMPS and Class D audio power amplifier is analyzed in steady-state, there must be a charge balance on both capacitors in order to obtain the same capacitor voltage after each of the modulating periods T_m. This means that the regenerated charge from the load to the capacitors compensates some of the charge being transferred from the capacitors to the load during the generating mode, so that the input stage needs to supply just their difference. In this way, the average SMPS output inductor current $I_{L2} = I_{L21} = I_{L22}$ is calculated to be:

$$\begin{aligned} I_{L2} &= \frac{1}{T_m}\int_0^{T_m}\frac{1}{2R}\left(V_o+\frac{V_o^2}{V_2}\right)dt = \frac{1}{2RT_m}\int_0^{T_m}\left[V_m\sin(2\pi f_m t)+\frac{V_m^2\sin^2(2\pi f_m t)}{V_2}\right]dt = \\ &= \frac{1}{2RT_m}\left[-\frac{V_m T_m}{2\pi}\cos(2\pi f_m t)\Big|_0^{T_m}+\frac{V_m^2 T_m}{2V_2}-\frac{V_m^2 T_m}{8\pi V_2}\sin(4\pi f_m t)\Big|_0^{T_m}\right] = \frac{V_m^2}{4RV_2} \end{aligned} \tag{6.29}$$

Assuming input stage operation with 50% duty cycle, average primary side current in the case of conventional SMPS and Class D audio power amplifier is:

$$I_{1,SMPS} = \frac{1}{n}I_{2,SMPS} = \frac{1}{n}\left(\frac{I_{L21}}{2}+\frac{I_{L22}}{2}\right) = \frac{1}{n}I_{L2} = \frac{V_m^2}{4nRV_2} \tag{6.30}$$

where $n = N_1/N_2$ is the transformer turns ratio.

When doing the same calculation for the SICAM case, it becomes clear that both the active and the reactive portion of the switch currents i_{21} and i_{22} are processed by the input stage. To simplify the analysis, first it will be neglected for a moment that the HF-link voltage is alternating, which results in the bidirectional switches currents i_{21} and i_{22} being equal to the Class D currents i_{2p} and i_{2n} correspondingly. Afterwards it is recognized that when the HF-link voltage starts perpetually to change the polarity the equality does not hold anymore, but the Class D currents can still be associated with the equivalent positive and negative voltage sources in the HF-link. This means that the average secondary-side SICAM current during a modulating period T_m can be calculated from the average MOSFET current values of the Class D audio power amplifier I_{2p} and I_{2n} from (6.28) as:

$$\begin{aligned} I_{2,SICAM} &= \frac{|I_{21}|+|I_{22}|}{2} = \frac{|I_{2p}|+|I_{2n}|}{2} = \\ &= \frac{1}{2RT_m}\left[\int_0^{T_m/2}\left(V_o+\frac{V_o^2}{V_2}\right)dt - \int_{T_m/2}^{T_m}\left(V_o+\frac{V_o^2}{V_2}\right)dt\right] = \\ &= \frac{1}{2RT_m}\left[-\frac{V_mT_m}{2\pi}\cos(2\pi f_m t)\Big|_0^{T_m/2} + \frac{V_m^2T_m}{4V_2} - \frac{V_m^2T_m}{8\pi V_2}\sin(4\pi f_m t)\Big|_0^{T_m/2} + \right. \\ &\left. + \frac{V_mT_m}{2\pi}\cos(2\pi f_m t)\Big|_{T_m/2}^{T_m} - \frac{V_m^2T_m}{4V_2} + \frac{V_m^2T_m}{8\pi V_2}\sin(4\pi f_m t)\Big|_{T_m/2}^{T_m}\right] = \frac{V_m}{\pi R} \end{aligned} \tag{6.31}$$

and the average primary-side SICAM current is:

$$I_{1,SICAM} = \frac{1}{n}I_{2,SICAM} = \frac{V_m}{\pi nR} \tag{6.32}$$

From equations (6.30) and (6.32), the SICAM input stage overdimensioning factor ODF in (6.23) becomes:

$$ODF = \frac{I_{1,SICAM}}{I_{1,SMPS}} = \frac{4V_2}{\pi V_m} = \frac{4}{\pi M_{max}} \tag{6.33}$$

where M_{max} is the maximum modulation index. The lowest achievable ODF is $ODF_{min} = 4/\pi = 1.27$ for $M_{max} = 1$.

For the example shown in Fig. 6.11, $I_{2,SMPS}$=1.11 A, $I_{2,SICAM}$=1.59 A and ODF=1.43, which equals to 43% overdimensioning of the SICAM input stage when compared to the input stage of the conventional SMPS and Class D audio power amplifier with the same specifications.

6.2 Output stage

6.2.1 Commutation of the load current in the output stage through safe-commutation switching sequences

In order to be able to block both voltage polarities that appear on the AC HF-link, the output stage of a SICAM must consist from bidirectional switches i.e. 4QSWs already presented in Section 5.5. However, due to the specific implementation of 4QSW, the freewheeling path for the load current which is pertinent to the Class D amplifier active switch with antiparallel diode is lost. This means that during the switching between

the outgoing and the incoming 4QSW, the designer must provide an uninterrupted load current path without short circuiting the transformer secondary, if there is voltage across it. If the load current is disrupted, dangerously large induced voltage spikes will develop across the output filter inductor, which can drive the MOSFETs in the bidirectional switches into avalanche mode or even destroy them.

The scheme of a full-bridge output stage with clearly separated and controllable load current paths (4QSW is antiparallel connection of two voltage 2QSWs) is given in Fig. 6.12.

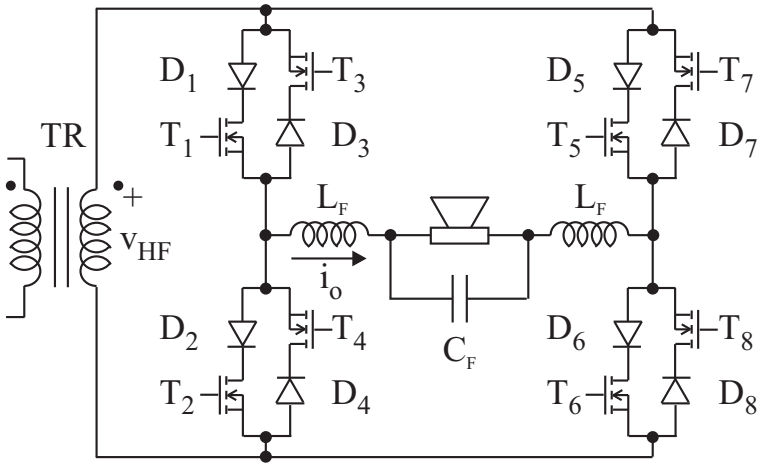

Fig. 6.12. Full-bridge bidirectional SICAM output stage

This bidirectional bridge can be also referred to as a single-phase to single-phase matrix converter. This makes the matrix converter commutation techniques applicable to the aforementioned audio output stage. However, some limitations when transferring from the largely exploited three-phase case [30], [34], [58], [59] to a single-phase are observed.

The simplest strategies for commutation of the load current in the bidirectional switches, which consist of providing a dead-time between the switching of the outgoing and incoming switch or allowing an overlap, result in disrupted load current or short circuited source voltage correspondingly, so they are both theoretically and practically unusable. The only case where overlap in the conduction of the incoming and outgoing bidirectional switch is allowed is in the intervals with zero voltage across the transformer when 3-level PWM HF-link voltage is used.

The basic commutation strategies therefore are:

- **Current controlled** - the commutation strategy is relying on accurate determination of the load current i_o direction, so that the switching sequence provides continuous current path without allowing a short circuit of the source; and
- **Voltage controlled** - the commutation strategy is based on the HF-link voltage v_{HF} polarity, so that right switches are chosen which not result in any violation of the electrical laws.

Regarding the structure of the bidirectional bridge in Fig. 6.12, current controlled commutation can be accomplished using the switching pattern in Table 6.1 and voltage controlled commutation using the switching pattern in Table 6.2. Stepping through the switching sequences is performed with a short delay in order of several tens of nanoseconds, just to allow the load current to commutate from the outgoing set to the incoming set of switches.

outgoing switches	i_o	off ↘	on ↗	off ↘	on ↗	incoming switches
1,6 & 3,8	> 0	3,8	4,7	1,6	2,5	2,5 & 4,7
	< 0	1,6	2,5	3,8	4,7	
2,5 & 4,7	> 0	2,5	1,6	4,7	3,8	1,6 & 3,8
	< 0	4,7	3,8	2,5	1,6	

Table 6.1. Current controlled commutation sequence of the bidirectional bridge in Fig. 6.12

outgoing switches	v_{HF}	on ↗	off ↘	on ↗	off ↘	incoming switches
1,6 & 3,8	> 0	4,7	1,6	2,5	3,8	2,5 & 4,7
	< 0	2,5	3,8	4,7	1,6	
2,5 & 4,7	> 0	3,8	2,5	1,6	4,7	1,6 & 3,8
	< 0	1,6	4,7	3,8	2,5	

Table 6.2. Voltage controlled commutation sequence of the bidirectional bridge in Fig. 6.12

Both presented strategies have some practical pitfalls. Current controlled commutation strategies are very popular in the motor drives community, since the load current is a measured quantity in order to accomplish field oriented control and for protection purposes. However, large current measurement and accurate current zero-crossing detection in a same current sensor are two counteracting goals, since for current measurements (for ex. in motor drives) a wide range of load currents should be accommodated, while for zero current detection very low noise and high accuracy environment with very small currents should be provided. Therefore, poor results in whole range operation are reported with current controlled commutation only because of the low sensitivity, high noise and offset levels of the present state-of-the-art current sensors. Significant advantage of this approach is that load current can change its direction even when the commutation process has started. In that case, the other current direction will be usually prohibited, so the load current will settle at zero until the commutation process has ended.

Voltage controlled strategies are facing the same problems of inadequate measuring sensors like the current controlled strategies, despite of the additional volume and price burden imposed by their installation. However, they have an another disadvantage - input voltage reversal during a commutation is not allowed since this can result in having wrong switches turned on with possible disastrous results.

Combination of both techniques are also investigated in some references. In these approaches the alternative strategy is used whenever the first strategy enters into the uncertainty region where the voltage/current sign can not be accurately determined. Unfortunately, in the case of both voltage and current sign being uncertain, further switching can be catastrophic. To avoid this some retarding or prohibition techniques are executed where the switching is avoided as long as the voltage and/or current signs are uncertain, but the quality of the output voltage and input current are therefore compromised.

There are some three-phase techniques which can be used to overcome the pitfalls of the aforementioned strategies, like replacement [59] and prevention [58]. These consist of a smart commutation algorithm which changes the order of switching between the phases where the input line voltage sign is not certain by putting the third phase for safe commutation in between. Basically this results in shifting from one uncertain commutation to two certain, but more lossy commutations. Since in the case of the single-phase bidirectional bridge for audio-output stage there is no other phase to safely commute to, another approach must be found.

Voltage controlled commutation is usually regarded as inferior to the current controlled commutation because of the incapability of successfully finishing the commutation if the

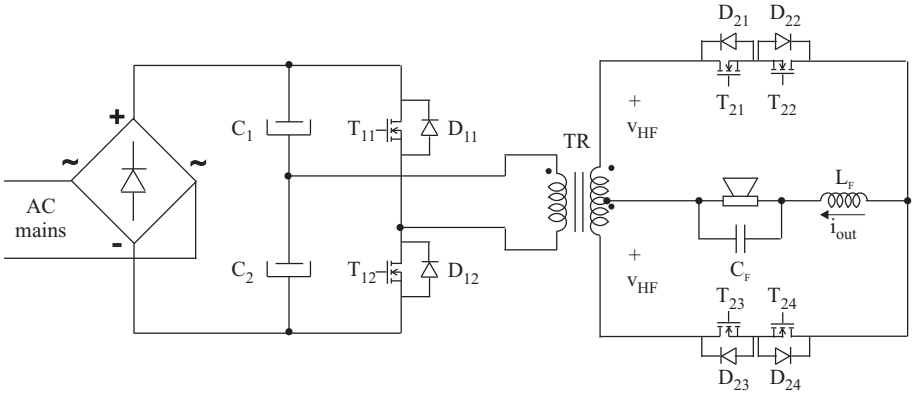

Fig. 6.13. Scheme of SICAM with single-ended output stage

input voltage sign changes during the process. This problem is especially emphasized in the case of three-phase matrix converters, since the input voltage is taken right from the utility grid as it is, so there is nothing the converter on the user side can do to mitigate the commutation. However, in the particular case presented in this thesis, the output stage of the SICAM is actually powered by the output voltage of the DC-AC inverter input stage, operation of which is completely under user control. This means that by wisely operating the input stage, every possible HF-link voltage polarity change during an output stage commutation can be avoided. Therefore, the only safe-commutation switching algorithm to be investigated herein is the voltage controlled sequence.

The voltage controlled switching sequence for the case of single ended output stage with common-source bidirectional switches in Fig. 6.13 is shown in Table 6.3. The depicted SICAM topology with a half-bridge inverter on the primary side and single-ended amplifier on the secondary side is found very appropriate and simple enough for the intended output power range and includes common-source bidirectional switches, which are characterized with probably the best characteristics for audio applications of all other bidirectional switches presented in Section 5.5.

Table 6.3. Voltage controlled commutation sequence - natural commutation (○) and forced commutation (●)

outgoing switch	v_{HF}	i_o	on ↗	off ↘	on ↗	off ↘	incoming switch
21,22	>0	>0	23	21 ●	24	22	23,24
		<0	23	21	24 ○	22	
	<0	>0	24	22	23 ○	21	
		<0	24	22 ●	23	21	
23,24	>0	>0	22	24	21 ○	23	21,22
		<0	22	24 ●	21	23	
	<0	>0	21	23 ●	22	24	
		<0	21	23	22 ○	24	

The voltage controlled commutation sequence presented in Table 6.3 depends only on the polarity of the HF-link voltage v_{HF}. The table, however, includes also the direction of the load current i_o which determines whether the load current commutation will be forced or natural.

In other words, output stage switches are operated on and off in a prescribed manner that provides alternative path for the load current without short-circuiting the transformer at all times. Except for the short periods when the input stage is switching, the transformer voltage i.e. the voltage of the HF-link v_{HF} has known and easily determinable polarity, so the switching of the output stage can safely proceed through the voltage controlled

commutation sequence given in Table 6.2. Stepping through the latter sequence is done by inserting short delays Δt_d, as shown in Fig. 6.14.

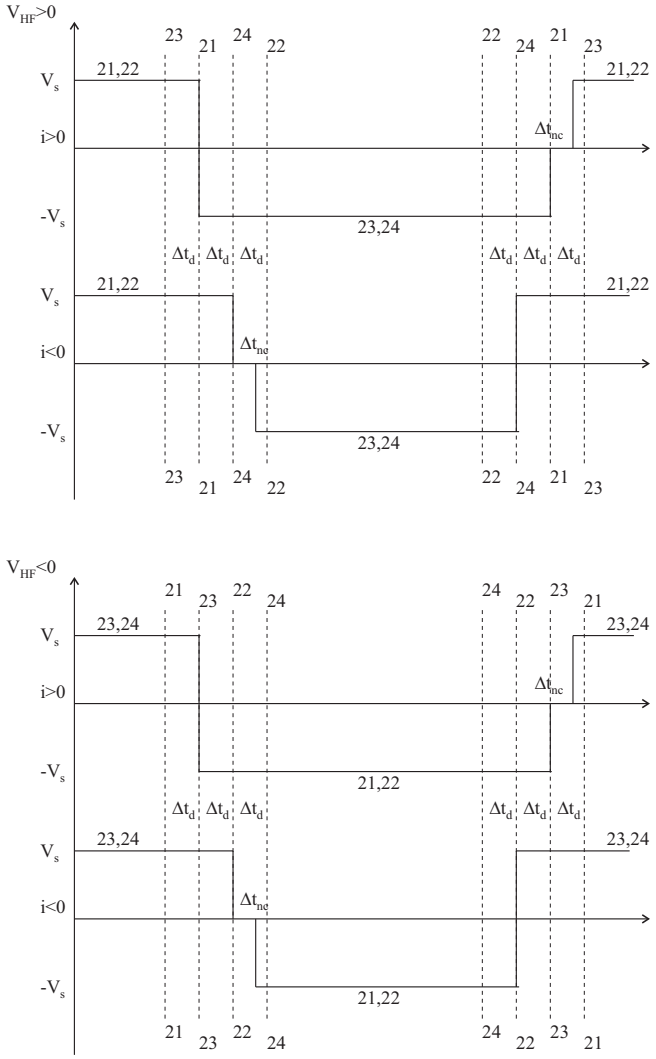

Fig. 6.14. Commutation diagrams with positive and negative HF-link voltages and load currents

Commutation of the load current from the outgoing to the incoming switches can be done either in a forced way, by turning off the switch which is conducting the load current, or in a natural way, by turning on one of the incoming switches and applying the correct transformer voltage that causes transfer of the load current from the outgoing to the incoming switch. The slew rate of the load current during natural commutation is limited by the leakage inductance of the transformer secondaries and the applied voltage and this determines the time it will take for the natural commutation to finish:

$$\Delta t_{nc} = 2L_{sl}\frac{|i_o|}{2V_s} = \frac{L_{sl}|i_o|}{V_s} \tag{6.34}$$

where L_{sl} is the leakage inductance of a single secondary, i_o is the instantaneous value of the load current and V_s is the value of the HF-link voltage. During natural commutation, bridge output voltage is equal to zero, since the equal leakage inductances in each of the switching branches act as an inductive voltage divider.

With regard to switching losses, the forced current commutation is lossy since it represents hard switching of the MOSFET which was conducting the whole load current. However, natural current commutation is lossless because of the fact that the current

rise in the switch is limited by the transformer secondary leakage inductances, so that incoming switch is turning on with essentially zero current (ZCS). However, if the duration of the natural commutation is longer than the inserted delay time, $\Delta t_{nc} > \Delta t_d$, when the current-carrying outgoing switch is turned off the natural commutation will turn into forced commutation, with just a fraction of the load current being switched off. It is therefore beneficial to keep the leakage inductance of the transformer secondary to a low value, in order to speed up the commutation process and decrease the associated voltage distortion.

It can be concluded that the voltage controlled commutation sequence represents a very simple way of implementing safe-commutation techniques in SICAMs, but the only thing that needs to be resolved is avoiding simultaneous switching of the input and the output stage, i.e. guaranteeing constant polarity of the HF-link voltage during the whole commutation sequence. This will be subject of investigation in some of the control methods presented in Chapter 7.

Regarding the practical implementation of the safe-commutation switching sequence from Table 6.3, it represents a finite state machine shown on the right-hand side in Fig. 6.15. It has two stable states S_1 and S_2, which depend on the polarity of the PWM modulator output V_{pwm} and possibly on the polarity of the HF-link voltage V_{HF} (V_{HF} shown in parenthesis at S_1 and S_2). This possibility is to include changeover of the bidirectional bridge state immediately after the change of the HF-link polarity, or at another instant within the switching period to decrease the switching frequency, as shown in the optimized PWM control method in Section 7.2.2. The safe-commutation finite state machine has also six astable states, in which the direction of the movement depends on the polarity of the PWM modulator output and HF-link voltage but the actual stepping through the states is determined by the time delay t_d. The two states P_1 and P_2 on the left-hand side in Fig. 6.15 just change between each other according to the output voltage polarity and can be used for selecting and multiplexing the outputs from different PWM modulators in the optimized PWM control method in Section 7.2.2.

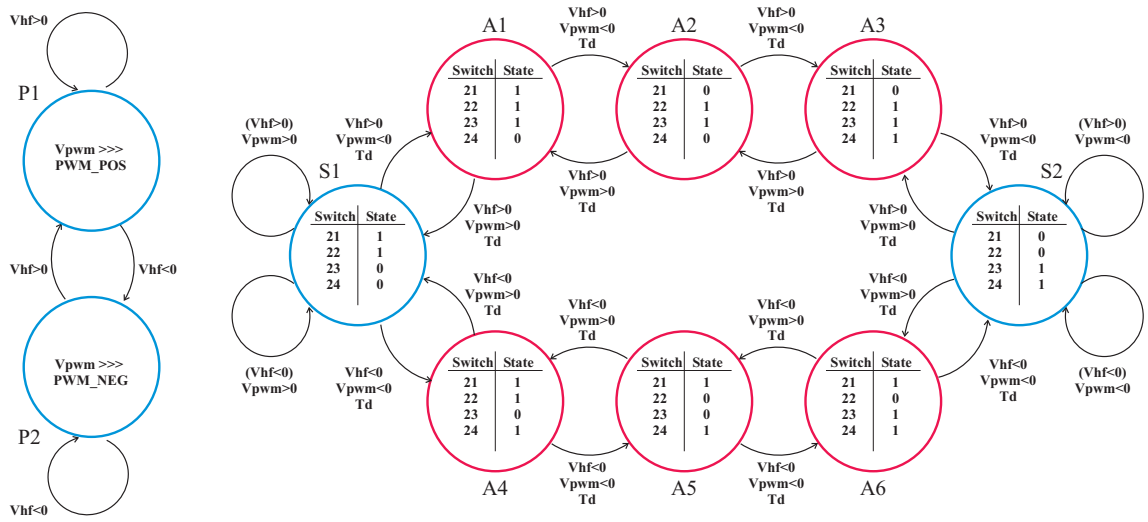

Fig. 6.15. State diagram of the safe-commutation switching sequence

The most flexible implementation of the finite state machine is in Programable Logic Device (PLD) in a synchronous way or asynchronous way. In the synchronous way, stepping through the safe-commutation switching sequence is performed synchronously with a fixed external clock and that is why this implementation requires least hardware resources. The clock rate of the external clock determines the commutation time delay $\Delta t_d = 1/f_{clk}$.

Unfortunately, clock impulses are not synchronized with the PWM modulator output, so there can be different time intervals from the moment the PWM modulator output changes state till the moment the commutation sequence actually starts. On the other hand, the asynchronous finite state machine has the commutation time delays Δt_d between the corresponding commutation steps implemented in hardware as gate logic delays, and although it is supposed to be the best performer it also requires most hardware from the PLD chip.

Effects of commutation delay on audio distortion

The ideal PWM amplification process is linear and does not introduce any distortion within the audio baseband. However, the PWM process as implemented in real hardware is far from ideal and its audio performance can suffer from nonlinearities introduced either in the PWM modulator or the power amplifier section. Looking at the PWM modulator, performance can suffer from carrier nonlinearity through acceleration or deceleration of the slopes i.e. carrier distortion, caused either by intrinsic nonlinear slope generation or ripple voltage feedback from the power section, which cannot be distinguished from the actual modulating signal by the PWM modulator comparator itself [79]. In the conventional Class D switching power stage [80], errors arise as a result of the blanking i.e. dead - time, delays and finite rise and fall times, known as Pulse Timing Errors (PTE), as well as power supply perturbations and finite switch impedances, known as Pulse Amplitude Errors (PAE). The switching power stage of the proposed SICAM amplifier is prone to all the aforementioned errors, except for the blanking error, which due to the specific safe-commutation switching strategy appears as commutation delay error and features slightly different characteristics. These will be topic of the present section.

By inspection of the commutation diagram in Fig. 6.14 for the case with positive and negative current, it turns out that the average voltage error v_e is given by:

$$v_e = \begin{cases} -\dfrac{(2\Delta t_d + \Delta t_{nc})V_s}{T_{c2}}\,, i_0 > 0 \\ \dfrac{(2\Delta t_d + \Delta t_{nc})V_s}{T_{c2}}\,, i_0 < 0 \end{cases} \tag{6.35}$$

where the natural commutation interval Δt_{nc} is given in (6.34) and depends on the load current, which causes the distortion to appear as load dependent. The time period T in equation (6.35) stands for the switching period of the output stage, and in the case of the optimized PWM method from Section 7.2.2 it is equal to the time period of the PWM modulator triangular carrier T_{c2}.

The two different cases of distortion, where the maximum natural commutation interval $\Delta t_{nc,max}$ occurring at maximum load current is either shorter or longer than the commutation delay Δt_d, are given in Fig. 6.16. The hatched area corresponds to the bridge voltage distortion in a conventional Class D audio amplifier [80], while the rest of it is specific to the safe-commutation switching strategy with the proposed SICAM.

Fourier series coefficients for the non-hatched area under the voltage error curve in Fig. 6.16 with $\Delta t_{nc,max} > \Delta t_d$ are:

$$a_{1,0} = 0$$

$$a_{1,n} = 0$$

$$b_{1,n} = \frac{2L_{sl}I_m}{\pi T_{c2}V_s}\left\{\frac{\sin[(2n-2)\frac{2\pi}{T_m}t_{10}]}{2n-2} + \frac{\sin[2n\frac{2\pi}{T_m}t_{10}]}{2n}\right\} + \frac{4\Delta t_d V_s}{\pi T_{c2}}\frac{\cos[(2n-1)\frac{2\pi}{T_m}t_{10}]}{2n-1}$$

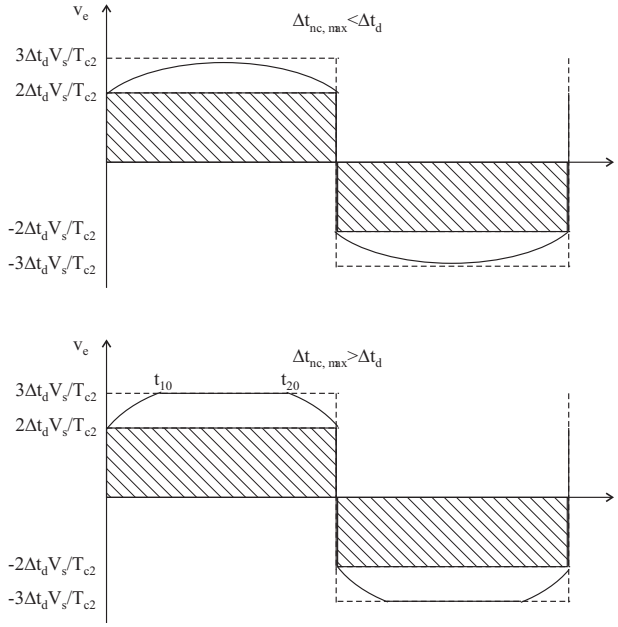

Fig. 6.16. Average voltage error with $\Delta t_{nc,max} < \Delta t_d$ (above) and $\Delta t_{nc,max} > \Delta t_d$ (below)

(6.36)

where L_{sl} is the secondary-side leakage inductance, $I_m = MI_{o,max}$ is the peak value of the load current, $V_s = |v_{HF}|$ is the secondary-side absolute voltage value, T_m is the period of the modulation signal, $n \in \mathbf{Z}^+$, t_{10} and t_{20} are the instants when $\Delta t_{nc} = \Delta t_d$:

$$\begin{aligned} t_{10} &= \frac{1}{\omega_m} \arcsin\left(\frac{\Delta t_d V_s}{L_{sl} I_m}\right) \\ t_{20} &= \frac{T_m}{2} - t_{10} \end{aligned} \tag{6.37}$$

In the case when $\Delta t_{nc,max} < \Delta t_d$ there is no distortion introduced by the non-hatched area in Fig. 6.16, except for the linear error causing change of the fundamental value by a factor of $-(L_{sl}I_m)/(T_{c2}V_s)$.

Fourier series coefficients for the hatched area in Fig. 6.16, corresponding to conventional Class D amplifier distortion, are given by:

$$\begin{aligned} a_{2,0} &= 0 \\ a_{2,n} &= 0 \\ b_{2,n} &= -2\frac{\Delta t_d}{T_{c2}} V_s \frac{sin(n\frac{\pi}{2})}{n\frac{\pi}{2}} = 2\frac{\Delta t_d}{T_{c2}} V_s \frac{(-1)^n}{(2n-1)\frac{\pi}{2}} \end{aligned} \tag{6.38}$$

In general, the total harmonic distortion (THD) caused by the commutation delay is given by:

$$THD = \frac{\sqrt{\sum_{i=2}^{N_{max}} (b_{1,i} + b_{2,i})^2}}{MV_s + b_{1,1} + b_{2,1}} \tag{6.39}$$

which in the case of $\Delta t_{nc,max} < \Delta t_d$ leads to:

$$THD_1 = \frac{\sqrt{\sum_{i=2}^{N_{max}} (b_{2,i})^2}}{MV_s - \frac{L_{sl} I_m}{T_{c2} V_s} - \frac{4\Delta t_d V s}{\pi T_{c2}}} \tag{6.40}$$

and in the case of $\Delta t_{nc,max} > \Delta t_d$ to:

$$THD_2 = \frac{\sqrt{\sum_{i=2}^{N_{max}} (b_{1,i} + b_{2,i})^2}}{MV_s + b_{1,1} - \frac{4\Delta t_d V_s}{\pi T_{c2}}} \tag{6.41}$$

The presence of filter ripple current causes the THD of the SICAM to decrease as the output current i.e. the modulation index M decreases. This is result of the fact that within one carrier period T_{c2} in Fig. 6.14 the switch current changes the polarity, thus effectively cancelling the voltage error of two subsequent commutations and giving no average voltage error. Therefore, the reduced THD of the SICAM at low modulation indexes can be taken into account the same way as in the conventional Class D amplifier [80]:

$$THD = \frac{\Delta(\alpha_I) \sqrt{\sum_{i=2}^{N_{max}} (b_{1,i} + b_{2,i})^2}}{MV_s + \Delta(\alpha_I)(b_{1,1} + b_{2,1})} \tag{6.42}$$

where α_I is the ripple current factor, which depends on the modulation index M and the maximum values of the load current $I_{o,max}$ and filter ripple current $I_{fr,max}$ in the following way:

$$\alpha_I = \frac{I_{fr,max}}{I_m} = \frac{I_{fr,max}}{M \cdot I_{o,max}} \tag{6.43}$$

and the THD correction factor $\Delta(\alpha_I)$ is:

$$\Delta(\alpha_I) = \begin{cases} 0 & , I_m \leq I_{fr,max} \\ \frac{\frac{\pi}{2} - \arcsin(\alpha_I)}{\frac{\pi}{2}} & , I_m > I_{fr,max} \end{cases} \tag{6.44}$$

THD vs. power curves for a SICAM with safe-commutation and no additional control feedback loops in a case when $V_s = 71$ V, filter inductance $L = 42$ μH, modulation index M=0-0.65 and four different secondary-side leakage inductances L_{sl}=0, 1 μH, 2 μH and 5 μH are depicted in Fig. 6.17. It can be noticed that the presence of leakage inductance in the secondary-side winding of the transformer causes additional distortion of the output voltage due to the natural commutation delay Δt_{nc}, which can not be longer than the commutation delay Δt_d. Therefore, the SICAM THD cannot be lower than the THD of a Class D amplifier with similar specifications (bottom curve $L_{sl} = 0$ μH in Fig. 6.17), but also not higher than the case with very large leakage inductance (top curve $L_{sl} = 5$ μH in Fig. 6.17), when the natural commutation is rather slow and is essentially replaced entirely by forced commutation after the commutation delay Δt_d. The small circles on the curves show the moment when the natural commutation turns into partly forced commutation $\Delta t_{nc} > \Delta t_d$, resulting in sudden increase of the THD. The curves in Fig. 6.17 also show the need for adding a control with feedback, which will linearize the output stage and effectively decrease the distortion by the amount of gain within the frequency band of interest.

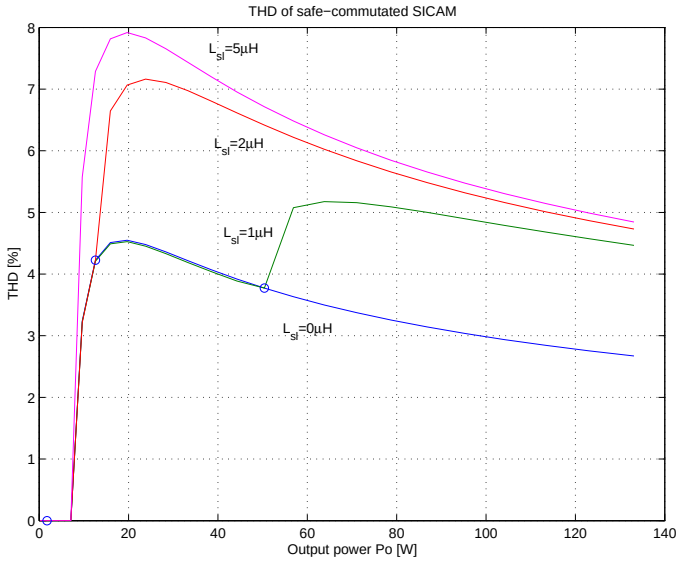

Fig. 6.17. THD of a safe-commutated SICAM with different secondary-side leakage inductances

6.2.2 Commutation of the load current in the output stage with load clamps

The main drawback of the load current commutation with safe-commutation switching sequence is the involved control strategy which needs to guarantee that switching the input and the output stage is not simultaneous. At the same time the intentionally inserted commutation delay times when advancing through the safe-commutation switching sequence give additional rise to output voltage distortion. On the reliability side, the proposed safe-commutation switching sequence alone does not allow for safe shutdown of the amplifier, if the secondary side gate-drive of the bidirectional switches is suddenly lost when there is a large amount of stored magnetic energy in the output filter and the load.

The simplest load current commutation strategy for the output stage of a SICAM would ideally resemble switching of the Class D audio power amplifier with blanking (dead) time t_{bl}. The biggest problem with this approach is that in Class D audio power amplifiers the load current continues to freewheel through the MOSFET antiparallel diodes during the dead time, while bidirectional switches in SICAM output stage do not possess such a freewheeling path. In order to create it, there must be an output filter and loudspeaker clamp added to the output stage, which will provide an alternative path for the load current and clamp the load voltage when all the switches are turned off. The load clamp, being a clamp of both the output filter and the loudspeaker, is shown as a block diagram in Fig. 6.18.

As depicted in Fig. 6.18, when both bidirectional switches are turned off, load current is diverted through a fast rectifier bridge to a clamp capacitor C_3, while the load voltage is clamped to latter capacitor voltage. In order to keep the complexity of the clamp low, direction of the power flow during the dead time is always from the load to the clamp capacitor and not vice versa, because of the rectifier bridge. Limiting the capacitor voltage to reasonable levels by maintaining a charge balance is very important in this case, so a dissipative clamp with a parallel resistor [9] or active clamp with an isolated SMPS returning the energy back to the primary side DC-bus [54], [81] is necessary. For more demanding applications, load clamp can be made bidirectional [49] and then power is regenerated back from the clamp capacitor to the same place where it was harnessed, i.e. on the secondary side.

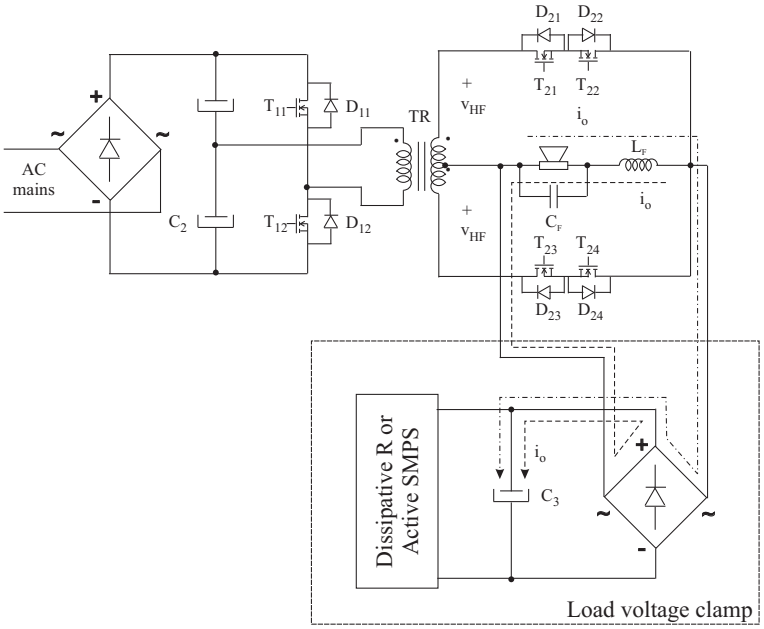

Fig. 6.18. Isolated SICAM with output filter and load clamp

The arrangement of the clamp and its connection to the output stage shown in Fig. 6.18 assumes that the secondary transformer leakage inductance is negligible, or similar clamp or snubber circuitry is present across the secondary winding. An extension of the clamp with different connection points can be used to receive the energy stored in both the secondary leakage inductance and load [9].

Another advantage of the clamping technique for commutating the load current in the output stage is the possibility of using a JFET as bidirectional switch, as already mentioned in Section 5.5. In the output stage with JFETs, there is no way of implementing safe-commutation switching techniques, since turning off the JFET results in immediate blocking of all current directions.

The implementation of the capacitive voltage clamp offers some unique benefits, which are not found elsewhere. The most prominent one is the increased safety against induced overvoltages in the case of loosing a secondary side gate-drive for bidirectional switches or other malfunctions that interrupt the usual load current path, which is functionally analogous to the three-phase matrix converter dissipative safety clamp. Another disputable advantage of the active capacitive voltage clamp, which returns the clamped energy back to the primary side energy storage capacitor, is the marginally improved ride-through capability of the SICAM in the case where AC mains input voltage is decreased or even lost for a very short period of time, during which the auxiliary converter feeds some charge from the clamp capacitor-dump to the primary side storage capacitor and supports the amplifier operation.

Comparing the lossy dissipative clamp with the ideally lossless active clamping technique, it becomes clear right away that the former is not suitable for the SICAM solution, which promotes simplicity and compactness together with high efficiency. Therefore, the rest of this chapter will deal with the active clamping technique, its operation principles, design issues and control techniques.

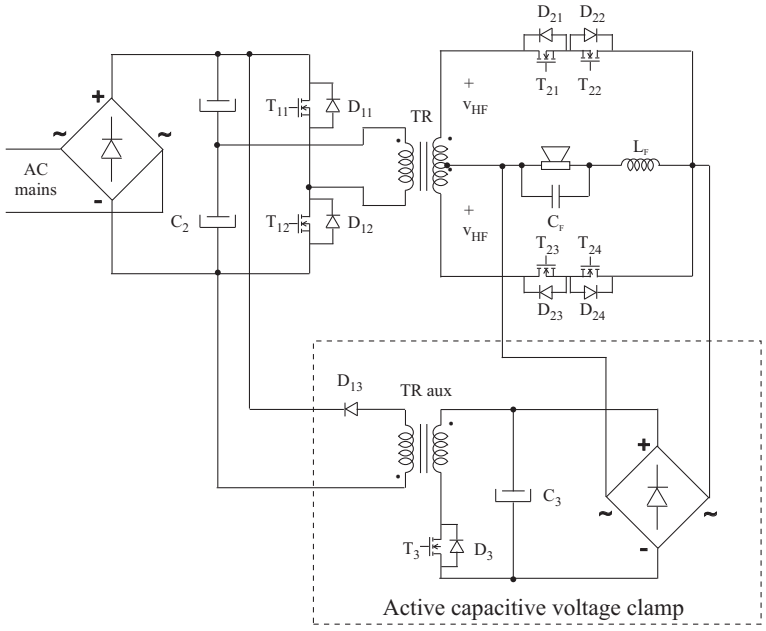

Fig. 6.19. Isolated SICAM with an active capacitive voltage clamp

6.2.3 SICAM with active capacitive voltage clamp

Topology and operation basics

The proposed SICAM with active capacitive voltage clamp, shown in Fig. 6.19, solves the commutation problem by allowing very short dead or blanking time t_{bl} between the outgoing and incoming switches, and in the meantime clamping the output filter and load voltage by diverting the load current i_o into the clamp capacitor C_3 through a very fast full-bridge rectifier. This creates clamp current i_{cl} with pulse shape, shown on the top diagram of Fig. 6.20, where the pulse magnitude is equal to the instantaneous value of the load current and pulse duration is equal to the blanking time t_{bl}.

The clamp itself is called active, since the energy dumped in the clamp capacitor during the short dead time intervals of the secondary side switches is not dissipated, but is instead returned to the primary side with a simple, small, isolated single-switch auxiliary converter, shown in the lower right corner in Fig. 6.19 as a flyback converter. The auxiliary converter is operated in a way that regulates the clamp capacitor voltage V_{cl} to a value that is slightly higher than the highest transformer secondary voltage expected during high voltage on the input line $V_{s,max}$, so that the clamp capacitor is charged only during the dead time interval and not throughout the rest of the switching interval. Although the task looks almost the same as in a common flyback converter, the regulated quantity is not the output voltage but the voltage of the clamp capacitor. Therefore, this active clamping technique poses some new challenges in the design of the auxiliary converter.

Since the clamp is connected in parallel with the combination of only the output filter and the loudspeaker, it is very important to keep the transformer secondary side leakage inductance as low as possible, which will limit the ringing during the dead time intervals due to the stored magnetic energy to a minimum.

Although the particular implementation of the SICAM with active capacitive voltage clamp depicted in Fig. 6.19 features half-bridge inverter on the primary side and single-ended amplifier on the secondary side, the selection of input and output stage topologies is performed separately for each design case to minimize component stress and is depending predominantly on the input voltage and output power levels.

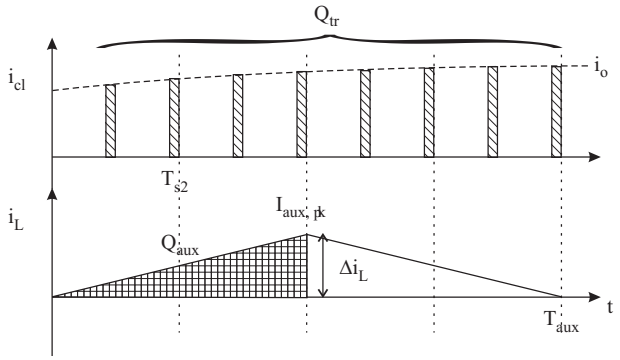

Fig. 6.20. Time waveforms of the active clamp

Clamp and auxiliary converter design

When compared to similar dissipative solutions [9] where a properly chosen resistor is used to dissipate the energy dumped in the clamp capacitor and keep the clamp voltage from raising abnormally even at highest loading, the active clamp approach gives much higher efficiency. This is done, however, on expense of increased complexity and cost due to several additional power components, but the auxiliary converter itself processes only a small fraction of the total audio power amplifier power, so it is rather small and cheap to implement.

For comparison purposes, the power dissipated in a dissipative clamp resistor R_{cl} is almost independent of the SICAM instantaneous output voltage, since the clamp capacitor is always charged through the clamp rectifier to at least the transformer secondary voltage:

$$P_{dis} = \frac{V_s^2}{R_{cl}} \tag{6.45}$$

On the other hand, using an active load voltage clamp with auxiliary converter preserves and regenerates the charge dumped in the clamp capacitor. By regulating the clamp capacitor voltage to values slightly higher than the HF-link voltage $v_{cl} > v_{HF}$, charge is being dumped into the clamp capacitor only during the blanking (dead) time periods and not directly from the primary side during normal operation, except for the start of operation. These blanking time periods happen twice per switching period of the output stage, so the duty cycle of the clamp current can be defined as $D_{cl} = 2t_{bl}/T_{s2}$. Assuming that sinusoidal load current with peak value of $I_{o,pk}$ and variable modulation index M is diverted into the clamp at the switching frequency of the bidirectional bridge $f_{s2} = 1/T_{s2}$ and with duration equal to its blanking time t_{bl}, the average current into the clamp $I_{cl,av}$ is:

$$I_{cl,av} = D_{cl} I_{o,av} = 2t_{bl} f_{s2} \frac{2}{\pi} M I_{o,pk} \tag{6.46}$$

and its RMS value $I_{cl,rms}$ is:

$$I_{cl,rms} = I_{o,av} \sqrt{D_{cl}} = \frac{2}{\pi} M I_{o,pk} \sqrt{2t_{bl} f_{s2}} \tag{6.47}$$

Power handled by the auxiliary converter P_{cl} of the active clamp is calculated as:

$$P_{cl} = V_{cl} I_{cl,av} = 2V_{cl} t_{bl} f_{s2} \frac{2}{\pi} M I_{o,pk} \tag{6.48}$$

and the active clamp power loss is just a fraction of P_{cl}, depending on the efficiency of the active clamp converter η_{cl}:

$$P_{loss,cl} = \eta_{cl}(P_{cl}) \cdot P_{cl} \tag{6.49}$$

The design of the clamp starts with the selection of the clamp capacitor $C_{cl} = C_3$. The primary task of the selection process is to limit the voltage ripple ΔV_{cl} during normal operation or emergency shutdown. By assuming that the bulk of the clamp capacitor voltage ripple in normal operation is due to its internal equivalent series resistance (ESR), the following selection rule can be written for the clamp capacitor ESR:

$$ESR_{max} = \frac{\Delta V_{cl,max}}{I_{o,pk}} \tag{6.50}$$

During emergency shutdown all the stored energy in the output filter inductor is converted into electrostatic energy in the clamp capacitor. The worst case for this situation is when the converter is shut down at the peak value of the inductor current $I_{o,pk}$, when the magnetic energy stored in the inductor L_f is largest:

$$E_{L,pk} = \frac{1}{2} L_f I_{o,pk}^2 \tag{6.51}$$

Neglecting the presence of the auxiliary converter due to the unavoidable time delay before it catches up with the increased clamp voltage, as well as the output filtering capacitor which is much smaller in size than the clamp capacitor, the inductor current will divert entirely into the clamp capacitor and cause increase of its voltage ΔV_{cl} and its stored energy amounting to:

$$\Delta E_{Ccl} = \frac{1}{2} C_{cl} \Delta V_{cl}^2 \tag{6.52}$$

If the maximum allowed increase of clamp capacitor voltage during emergency shutdown is $\Delta V_{cl,max}$, from (6.51), (6.52) and $E_{L,pk} = \Delta E_{Ccl}$ the clamp capacitor capacitance is limited to:

$$C_{cl,min} = L_f \left(\frac{I_{o,pk}}{\Delta V_{cl,max}} \right)^2 \tag{6.53}$$

At the same time, the clamp capacitor must be able to handle the maximum RMS capacitor current $I_{Ccl,rms}$, which comprises of the RMS clamp current $I_{cl,rms}$ and RMS capacitor discharge current $I_{dis,rms}$:

$$I_{Ccl,rms} = \sqrt{I_{cl,rms}^2 + I_{dis,rms}^2} \tag{6.54}$$

The design of the clamp auxiliary converter is started by selecting an appropriate isolated converter topology and mode of operation. In most of the cases discontinuous conduction mode (DCM) flyback converter will be the best choice, since it is the simplest isolated converter topology and the discontinuous mode operation allows for low inductance value of the flyback transformer, leading to minimum size magnetics.

After the topology and the operating mode of the auxiliary converter have been chosen, the inductance value L_{aux} of the inductor in the auxiliary converter, i.e. the flyback transformer magnetizing inductance in this particular case, is to be calculated. The most important quantity for its selection is the maximum transferred charge $Q_{tr,max}$ from the load to the clamp capacitor during one period of the auxiliary converter operation $T_{aux} = 1/f_{aux}$. Due to the discontinuous conduction mode of the auxiliary converter and the steady-state balance of the clamp capacitor voltage, the transferred charge from the load

to the clamp which is the sum of the hatched areas on the top diagram in Fig. 6.20 is equal to the transferred charge from the clamp to the primary side, which is represented by the crosshatched area on the bottom diagram in Fig. 6.20. Maximum transferred charge occurs at maximum output:

$$Q_{tr,max} = \frac{f_{s2}}{f_{aux}} I_{o,pk} t_{bl} \tag{6.55}$$

The maximum charge $Q_{aux,max}$ which can be transferred from the clamp capacitor to the primary side with DCM auxiliary converter is calculated by using its peak inductor current $I_{aux,pk}$ and the maximum duty cycle D_{max}:

$$Q_{aux,max} = \frac{1}{2} I_{aux,pk} D_{max} T_{aux} = \frac{V_{cl} D_{max}^2}{2 L f_{aux}^2} \tag{6.56}$$

This limits the maximum inductance L_{max} of the auxiliary converter operating in DCM needed to entirely regenerate the maximum dumped charge $Q_{tr,max}$:

$$L_{aux,max} = \frac{V_{cl} D_{max}^2}{2 Q_{tr,max} f_{aux}^2} = \frac{V_{cl} D_{max}^2}{2 f_{s2} f_{aux} I_{o,pk} t_{bl}} \tag{6.57}$$

Other operating modes of the auxiliary converter are also possible, like combining continuous conduction mode CCM with large load currents and DCM with low load currents, but as already mentioned pure DCM operation leads to smallest size magnetics.

Control of the active clamp auxiliary converter

In order to synthesize the controller for the clamp auxiliary converter, it is necessary to have its dynamics in a form of a small-signal AC model. Derivation of the latter is significantly affected by the fact that the controlled quantity is the clamp capacitor voltage i.e. the source voltage, instead of the load voltage as with the conventional SMPS.

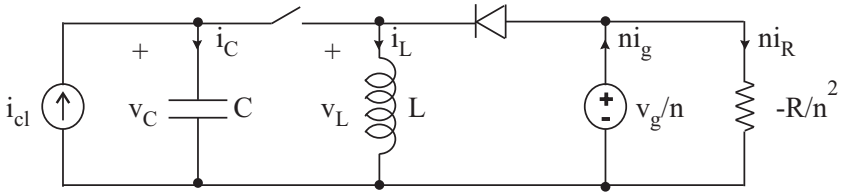

Fig. 6.21. Buck-boost auxiliary converter

The small-signal AC model of the aforementioned flyback auxiliary converter can be developed by using the converter diagram in Fig. 6.21, where n represents the transfer ratio of the flyback transformer and negative resistance $-R$ models the whole HF-link converter with its control loops. The transfer functions of the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM) flyback auxiliary converter differ, so they will be developed separately. The development of the equations for the CCM flyback auxiliary converter is given in Appendix D.1 and for the DCM flyback auxiliary converter in Appendix D.2.

By following the same steps like in [60], after the performed averaging of the equations during d and d' and perturbation of the variables, neglecting the second order terms

leads to the following AC and DC equations for the CCM flyback auxiliary converter in Fig. 6.21:

$$\begin{aligned}
\underline{AC}: \; L\frac{di_L}{dt} &= Dv_C + V_C d + \frac{D'}{n}v_g - \frac{V_g}{n}d \\
C\frac{dv_C}{dt} &= -Di_L - I_L d + i_{cl} \\
ni_g &= D'i_L - I_L d - \frac{n}{R}v_g \\
\underline{DC}: \; V_C &= -\frac{D'}{nD}V_g \\
I_L &= \frac{I_{cl}}{D} \\
I_g &= \frac{D'}{n}I_L - \frac{V_g}{R}
\end{aligned} \tag{6.58}$$

By rewriting the AC equations (6.58) in Laplace s-domain and setting $v_g = i_{cl} = 0$, the CCM control-to-clamp-voltage transfer function $G_{vcd,ccm}$ is obtained:

$$G_{vcd,ccm} = \left.\frac{v_c}{d}\right|_{v_g=i_{cl}=0} = \frac{V_g}{nD^2} \cdot \frac{1 - \frac{snLI_{cl}}{DV_g}}{1 + \frac{s^2LC}{D^2}} \tag{6.59}$$

DCM control-to-clamp-voltage transfer function $G_{vcd,dcm}$ is obtained through the small-signal averaged switch model of the DCM flyback auxiliary converter, depicted in Fig. 6.22.

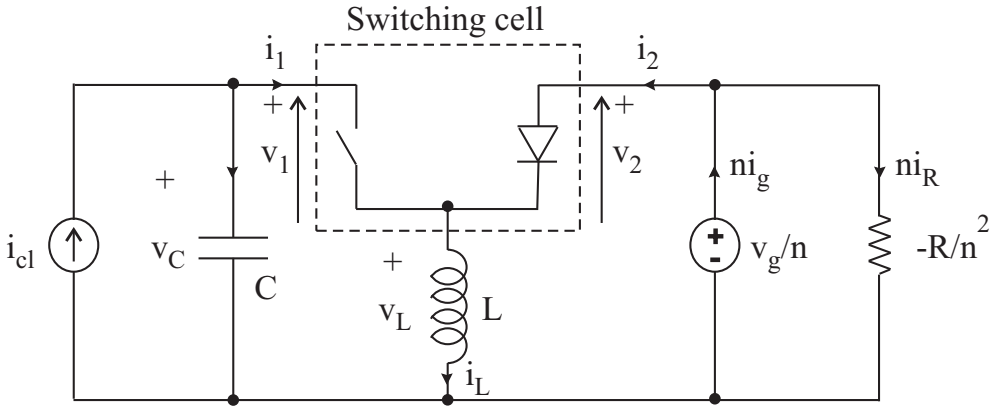

Fig. 6.22. Averaged switch model of the DCM flyback auxiliary converter

The control-to-clamp-voltage transfer function $G_{vcd,dcm}$ of the DCM flyback auxiliary converter is calculated in the Appendix D.2 and is repeated here:

$$G_{vcd,dcm} = \left.\frac{v_c}{d}\right|_{v_g=i_{cl}=0} = \frac{f_1(1-h_2) + j_2(r_1 + sL)}{(1-k_C)(1-h_2) - (r_1 + sL)(g_c - sC)} \tag{6.60}$$

where the coefficients in (6.60) are obtained by differentiating the input voltage v_1 and the output current i_2 of the averaged switch network:

$$v_1 = (1-d)v_C + d\frac{v_g}{n} - \frac{2Li_Lv_g}{ndT_sv_C} = \gamma_1(v_g, v_C, i_L, d) = k_g v_g + k_C v_C + r_1 i_L + f_1 d$$

$$\begin{aligned}
k_g &= \left.\frac{\partial\gamma_1(v_g, V_C, I_L, D)}{\partial v_g}\right|_{v_g=V_g} = \frac{D}{n} - \frac{2LI_L}{nDT_sV_C} \\
k_C &= \left.\frac{\partial\gamma_1(V_g, v_C, I_L, D)}{\partial v_C}\right|_{v_C=V_C} = (1-D) + \frac{2LI_LV_g}{nDT_sV_C^2} \\
r_1 &= \left.\frac{\partial\gamma_1(V_g, V_C, i_L, D)}{\partial i_L}\right|_{i_L=I_L} = -\frac{2LV_g}{nDT_sV_C} \\
f_1 &= \left.\frac{\partial\gamma_1(V_g, V_C, I_L, d)}{\partial d}\right|_{d=D} = -V_C + \frac{V_g}{n} + \frac{2LI_LV_g}{nD^2T_sV_C}
\end{aligned} \tag{6.61}$$

and:

$$i_2 = i_L - \frac{d^2T_sv_c}{2L} = \gamma_2(v_C, i_L, d) = g_C v_C + h_2 i_L + j_2 d$$

$$\begin{aligned}
g_C &= \left.\frac{\partial\gamma_2(v_C, I_L, D)}{\partial v_C}\right|_{v_c=V_C} = -\frac{D^2T_s}{2L} \\
h_2 &= \left.\frac{\partial\gamma_2(V_C, i_L, D)}{\partial i_L}\right|_{i_L=I_L} = 1 \\
j_2 &= \left.\frac{\partial\gamma_2(V_C, I_L, d)}{\partial d}\right|_{d=D} = -\frac{DT_sV_C}{L}
\end{aligned} \tag{6.62}$$

The small-signal equivalent model of the DCM flyback auxiliary converter is depicted in Fig. 6.23.

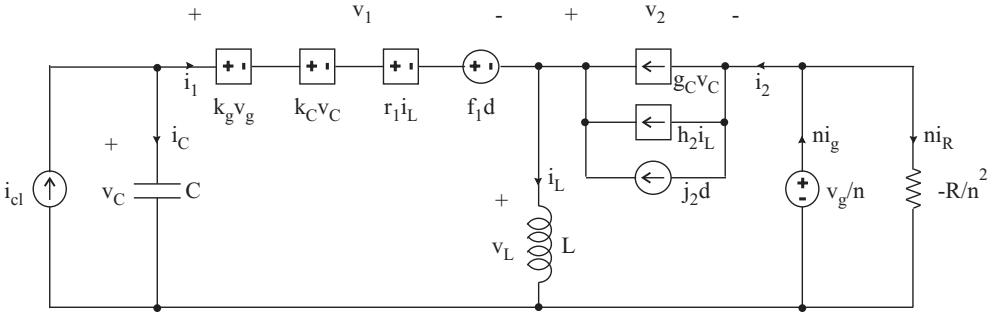

Fig. 6.23. Small-signal AC model of DCM flyback auxiliary converter

The use of current-mode control simplifies the control synthesis by essentially removing the pole associated with the inductor dynamics and making the inductor current a controlled quantity. This is, however, more important with the CCM auxiliary flyback converter where the inductor pole appears at lower frequencies, than with the DCM auxiliary flyback converter, where the inductor pole is already shifted to high frequency comparable to the switching frequency.

From the practical viewpoint, increase in the clamp capacitor voltage should result in larger duty cycle as to regenerate more charge from the clamp, i.e. the controller should be built around a non-inverting amplifier. To alleviate the control design, current-mode control of the auxiliary converter can be implemented on a standard SMPS control

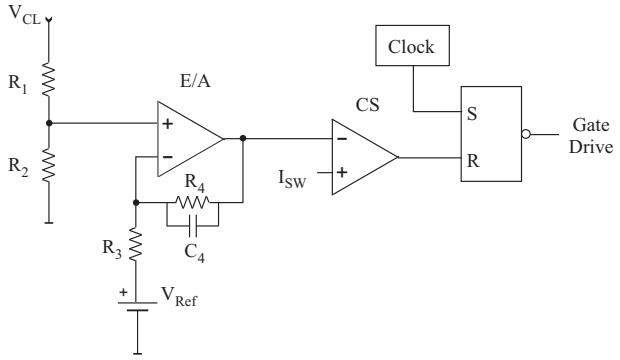

Fig. 6.24. Current-mode control of the auxiliary converter

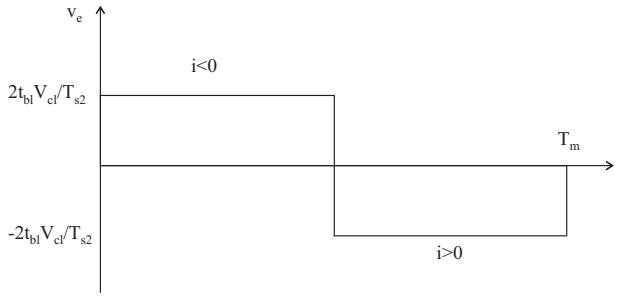

Fig. 6.25. Average voltage error v_e of the SICAM with active capacitive voltage clamp

chip, like shown in Fig. 6.24, where both the inverting and non-inverting pin of the error amplifier are accessible to build a non-inverting compensator.

Audio distortion in SICAMs with active capacitive voltage clamp

The distortion mechanism in the SICAM with active capacitive voltage clamp is very similar to the one in the conventional Class D amplifiers [80]. The only difference is that during the blanking time periods t_{bl} the load voltage is equal to the clamp capacitor voltage V_{cl} and the average voltage error v_e, shown in Fig. 6.25 is:

$$v_e = \begin{cases} -\dfrac{2t_{bl}V_{cl}}{T_{s2}}\,, i_0 > 0 \\ \dfrac{2t_{bl}V_{cl}}{T_{s2}}\,, i_0 < 0 \end{cases} \tag{6.63}$$

Fourier coefficients of the voltage error in (6.63) are given by the following equations:

$$\begin{aligned} a_0 &= 0 \\ a_n &= 0 \\ b_n &= -2\frac{t_{bl}}{T_{s2}}V_{cl}\frac{sin(n\frac{\pi}{2})}{n\frac{\pi}{2}} = 2\frac{t_{bl}}{T_{s2}}V_{cl}\frac{(-1)^n}{(2n-1)\frac{\pi}{2}} \end{aligned} \tag{6.64}$$

and the Total Harmonic Distortion (THD) of the open-loop SICAM power stage with active capacitive voltage clamp is:

$$THD = \frac{\sqrt{\sum_{i=2}^{N_{max}} b_i^2}}{MV_s - \dfrac{4t_{bl}V_{cl}}{\pi T_{s2}}} \tag{6.65}$$

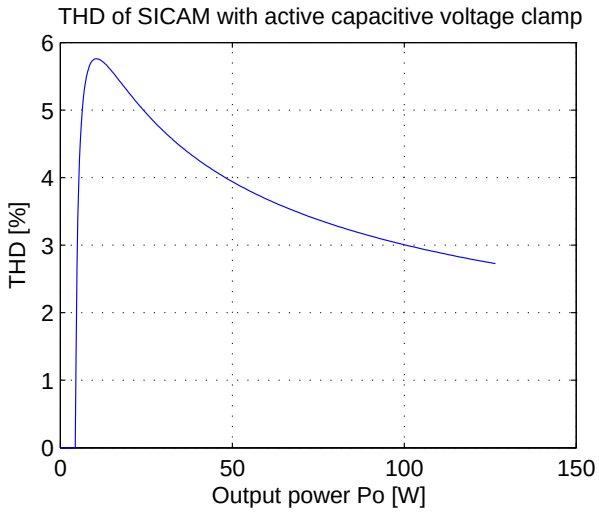

Fig. 6.26. THD of SICAM with active capacitive voltage clamp

The presence of filter ripple current causes the THD of the SICAM to decrease as the output current i.e. the modulation index M decreases. This is result of the fact that within one switching period T_{s2} the switch current changes the polarity, thus effectively cancelling the voltage error of two subsequent load current commutations and giving no average voltage error. Therefore, the reduced THD of the SICAM at low modulation indexes can be taken into account the same way as in the conventional Class D amplifier [80].

THD simulation of the SICAM with active capacitive voltage clamp operating in open loop with constant output stage switching frequency $f_{s2} = f_{c2} = 300$ kHz and modulation signal of $f_m = 1$ kHz is shown in Fig. 6.26. In the simulation secondary-side voltage is $V_s = 45$ V, clamp voltage is $V_{cl} = 50$ V and blanking time is $t_{bl} = 75$ s.

6.3 Output impedance of isolated SICAMs

One of the distinct advantages of the conventional amplifier solution with isolated SMPS and Class D audio power amplifier connected via DC-bus is that the bulky decoupling capacitors on the DC-bus act as a very low impedance for a wide range of frequencies. This has a very positive effect on the audio performance of the Class D audio power amplifier, where the closed-loop gain additionally decreases the output impedance of the Class D audio power amplifier to provide very high damping ratio, being a ratio of the load to output impedance.

The situation with SICAM is much worse, since there is no DC-bus with low impedance on the secondary side. Simplified schematic of SICAM up to the output of the bidirectional bridge, with an equivalent scheme of the transformer TR and switch impedances Z_{SW1}, Z_{SW2} referred to the secondary side, is shown in Fig. 6.27. Low impedance voltage source can only be found on the primary-side DC-bus with energy storage capacitors, which for the purpose of the following discussion will be regarded as ideal voltage source v_{in}. From that point up to the output of the bidirectional bridge and further to the loudspeaker there are several impedances on the current path which create certain voltage drops. Even more, due to the finite impedances of the transformer and the switches, at each switching instant there are significant oscillations in the bridge output voltages as a result of reactive energy circulation between inductive and capacitive elements in transformer and active switches.

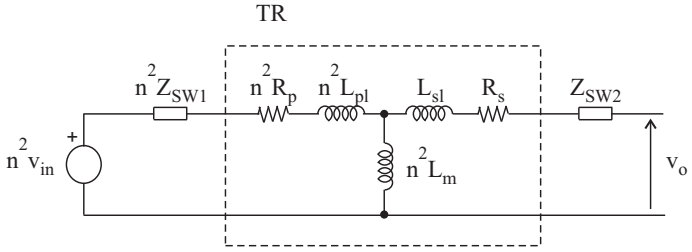

Fig. 6.27. Simplified schematic of SICAM for determining output impedance

The resultant output impedance looked from the output of the bidirectional bridge is:

$$Z_{out,bb} = \left(n^2 \cdot \sqrt{Z_{SW1}^2 + (R_p^2 + \omega^2 L_{pl}^2)}\right) || \left(n^2 \omega^2 L_m^2\right) + \left(\sqrt{Z_{SW2}^2 + (R_s^2 + \omega^2 L_{sl}^2)}\right) \approx$$
$$\approx \sqrt{n^4 Z_{SW1}^2 + Z_{SW2}^2 + (n^2 R_p + R_s)^2 + \omega^2 (n^2 L_{pl} + L_{sl})^2)} \tag{6.66}$$

where $n = N_2/N_1$ is the transformer transfer ratio, Z_{SW1} and Z_{SW1} are the switch impedances in the input and the output stage respectively, R_p and R_s are the resistances of the primary and secondary winding of the transformer, L_{pl} and L_{sl} are the leakage inductances of the primary and secondary winding of the transformer and L_m is the magnetizing inductance of the transformer.

Especially problematic part of the output impedance is the secondary-side leakage inductance of the transformer L_{sl}, which creates problems with the switching of the output stage and commutation of the load current with both the safe-commutation switching strategies and load voltage clamps. Reducing the transformer leakage inductance is possible through interleaving of the transformer windings and increasing the height of the winding window, to increase the magnetic reluctance of the leakage magnetic path.

From audio performance perspective, the finite output impedance of the input stage and transformer creates additional problems in the case of multichannel SICAM, where all the channels share the same input stage and transformer primary, as already described in Section 5.3.5. In this case, the common coupling point of all audio channels is by no means a low impedance point, so there can be significant channel crosstalk caused by voltage drops created from the channel currents flowing through the input stage switch impedances Z_{SW1}, primary winding resistance R_p and leakage inductance L_{pl} on Fig. 6.27.

6.4 Power losses and efficiency calculation in SICAMs

In the following sections the efficiency of different SICAM approaches will be compared through calculating the power losses in different stages. Calculations will be focused on the case with half-bridge input stage and single-ended bidirectional output stage, as showed previously in Fig. 6.13 and Fig. 6.19. Extending the presented equations for other topologies is straightforward and is not reconsidered herein.

6.4.1 Current and voltage levels in SICAMs

Each audio design starts with some specifications, and the most important are:

- Input voltage range - AC mains (Ex. $V_{in,rms} = 200 - 250$ V)
- Sinusoidal output power (Ex. $P_o = 100$ W)
- Load impedance (Ex. $Z = R = 8\ \Omega$)

The RMS output voltage $V_{o,rms}$ is calculated using the output power P_o and the load impedance $Z = R$:

$$V_{o,rms} = \sqrt{P_o R} \tag{6.67}$$

The peak value of the output voltage for sinusoidal waveform is:

$$V_{o,pk} = \sqrt{2} \cdot V_{o,rms} = \sqrt{2 P_o R} \tag{6.68}$$

The peak value of the output (load) current for sinusoidal waveform is:

$$I_{o,pk} = \frac{V_{o,pk}}{R} \tag{6.69}$$

Assuming sinusoidal audio signal reference, the RMS value of the load current is found to be:

$$I_{o,rms} = \frac{I_{o,pk}}{\sqrt{2}} \tag{6.70}$$

and the average value of the rectified sinewave current is:

$$I_{o,av} = \frac{2}{\pi} I_{o,pk} \tag{6.71}$$

In order to determine the maximum voltage on the secondary side of the transformer $V_{2,max}$, peak output voltage $V_{o,pk}$ is divided by the maximum achievable modulation index M_{max} (limited by, for example, the requirement for avoiding simultaneous switching of the input and the output stage in the optimized PWM in Section 7.2.2 or performance constraints in self-oscillating modulators in Section 7.3) plus additional voltage ΔV_2 for compensating voltage drops throughout the switches, transformer and output filter parasitics::

$$V_{2,max} = \frac{V_{o,pk}}{M_{max}} + \Delta V_2 \tag{6.72}$$

On the primary side, the minimum voltage on the DC-bus is:

$$V_{dc,min} = \sqrt{2} \cdot V_{in,min} - \Delta V_{dc} \tag{6.73}$$

where $V_{in,min}$ is the minimum RMS input voltage and ΔV_{dc} is the allowed voltage drop on the DC-bus at maximum output power.

Due to the half-bridge topology of the input stage, only half of that DC-bus voltage is applied across the primary winding, resulting in:

$$V_{1,min} = \frac{V_{dc,min}}{2} \tag{6.74}$$

The transformer voltage turns ratio n thus becomes:

$$n = \frac{N_1}{N_2} = \frac{V_{1,min}}{V_{2,max}} \tag{6.75}$$

After calculating the load quantities, voltage levels and transformer turns ratio, all SICAM currents can be calculated by going backwards from the filter to the input terminals.

The peak-to-peak filter ripple current flowing through the output filter capacitor can be found by multiplying the slope of the filter ripple current $(V_2 - v_o)/L_f$ by the on-time of the secondary side switches. Taking into account the relation between the output voltage and the duty cycle in (6.26), this gives the following peak value for the filter ripple current of a single-ended amplifier:

$$I_{fr,pk} = \frac{(V_2 - v_o) \cdot DT_s}{2L_f} = \frac{V_2 D(1-D)}{L_f f_{s2}} = \frac{(V_2^2 - v_o^2)}{4V_2 L_f f_{s2}} \tag{6.76}$$

which is depicted in Fig. 6.28, normalized with the peak load current for the specific case, and has maximum for $D = 0.5$ i.e. at zero output voltage $V_o = 0$ as mentioned in [14].

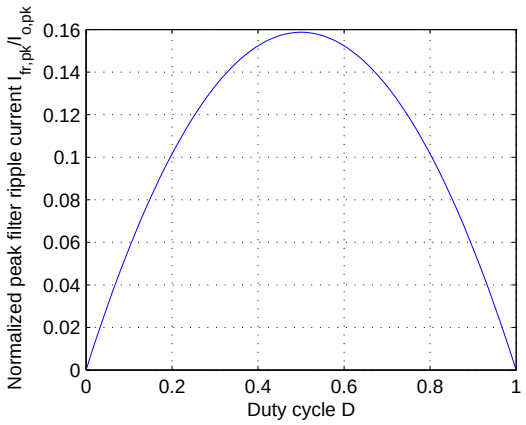

Fig. 6.28. Relationship between the duty cycle and the normalized peak filter ripple current

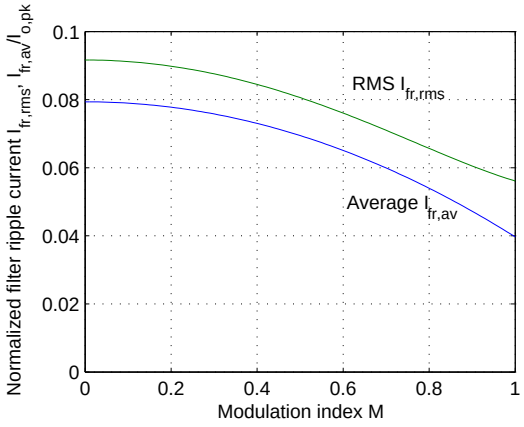

Fig. 6.29. Relationship between the modulation index and the normalized average and RMS filter ripple current

Assuming linear character of the filter ripple current, giving it a triangular form with constant peak value $I_{fr,pk} = const$, its RMS value is:

$$I_{fr,rms} = \frac{I_{fr,pk}}{\sqrt{3}} \tag{6.77}$$

and its average value is:

$$I_{fr,av} = \frac{I_{fr,pk}}{2} \tag{6.78}$$

In the case of sinusoidal output voltage v_o, with modulation index M and modulation angular frequency ω_m given with the following equation:

$$v_o = V_m \sin(\omega_m t) = MV_2 \sin\left(\frac{2\pi}{T_m} t\right) \tag{6.79}$$

the RMS value of the filter ripple current in (6.77) by using (6.76) becomes:

$$\begin{aligned} I_{fr,rms} &= \sqrt{\frac{1}{T_m}\int_0^{T_m} i_{fr,rms}^2 dt} = \sqrt{\frac{1}{T_m}\int_0^{T_m} \frac{I_{fr,pk}^2}{3} dt} = \\ &= \frac{V_2}{4L_f f_{s2}} \sqrt{\frac{1}{T_m}\int_0^{T_m} \frac{[1 - M^2 \sin^2(\omega_m t)]^2}{3} dt} = \\ &= \frac{V_2}{4L_f f_{s2}} \sqrt{\frac{1}{T_m}\int_0^{T_m} \frac{[1 - \frac{M^2}{2} + \frac{M^2}{2}\cos(2\omega_m t)]^2}{3} dt} = \frac{V_2}{4L_f f_{s2}} \sqrt{\frac{1 - M^2}{3} + \frac{M^4}{8}} \end{aligned}$$

(6.80)

and its average value is:

$$I_{fr,av} = \frac{1}{T_m}\int_0^{T_m} i_{fr,av}dt = \frac{1}{T_m}\int_0^{T_m} \frac{I_{fr,pk}}{2}dt = \frac{V_2}{8T_m L_f f_{s2}}\int_0^{T_m}[1 - M^2\sin^2(\omega_m t)]dt =$$
$$= \frac{V_2}{8T_m L_f f_{s2}}\int_0^{T_m}\left[\left(1 - \frac{M^2}{2}\right) + \frac{M^2}{2}\cos(2\omega_m t)\right]dt = \frac{(2 - M^2)V_2}{16L_f f_{s2}} \tag{6.81}$$

After calculating the filter ripple current RMS and average value, the RMS and average values of the secondary-side transformer current and output stage switch current can be calculated by adding together the corresponding values of the load and output filter current. Output stage switch current is:

$$I_{sw2,rms} = I_{2,rms} = \sqrt{I_{o,rms}^2 + I_{fr,rms}^2} \tag{6.82}$$

and its average value is:

$$I_{sw2,av} = I_{2,av} = I_{out,av} + I_{fr,av} \tag{6.83}$$

The RMS value of the reflected load and filter ripple current $I_{1,rms}$ is therefore:

$$I_{1,rms} = \frac{I_{2,rms}}{n} \tag{6.84}$$

and the average primary current is:

$$I_{1,av} = \frac{I_{2,av}}{n} \tag{6.85}$$

The RMS value of the magnetizing current $I_{m,rms}$, assuming linear magnetization, is:

$$I_{m,rms} = \frac{I_{m,pk}}{\sqrt{3}} \tag{6.86}$$

and its average value is:

$$I_{m,av} = \frac{I_{m,pk}}{2} \tag{6.87}$$

where the peak value of the magnetizing current $I_{m,pk}$ is:

$$I_{m,pk} = \frac{\Phi_{max}}{L_m} = \frac{V_{1,max} \cdot DT_s}{2L_m} \tag{6.88}$$

Current flowing through the input stage switches represents a sum of the reflected load and filter ripple current and the transformer magnetizing current. Thus, the input stage switch RMS current is:

$$I_{sw1,rms}^2 = I_{1,rms}^2 + I_{m,rms}^2 \tag{6.89}$$

and its average value is:

$$I_{sw1,av} = I_{1,av} + I_{m,av} \tag{6.90}$$

All these quantities will be used for calculating the power losses in the SICAM stages and overall efficiency.

6.4.2 Power losses in SICAM components and stages

Mains rectifier and input energy storage capacitors

The calculation of power losses in the mains rectifier and the input energy storage capacitor is rather straightforward when knowing the characteristics of the components and the corresponding current levels, determined in Section 3.1.

The losses in the full-bridge mains-rectifier are calculated by multiplying the diode forward voltage drop V_{fd} with the average charging current of the input energy storage capacitors I_{dc}:

$$P_{Cin} = 2V_{fd}I_{dc} \tag{6.91}$$

where the average charging current of the input energy storage capacitors I_{dc} is:

$$I_{dc} = i_{chg}t_c\frac{2}{T_{ac}} \tag{6.92}$$

and i_{chg} is given by (3.6).

The losses in the input energy storage capacitors C_{in} are dissipated in the internal equivalent series resistance (ESR) of the electrolytic capacitors when the capacitor ripple current I_{Cin} flows through them:

$$P_{Cin} = 2(ESR)I^2_{Cin,rms} \tag{6.93}$$

where the RMS value of I_{Cin} is given in (3.8) with the RMS capacitor charging current $I_{chg,rms}$ given in (3.7) and RMS capacitor discharging current equal to the input stage switch RMS current $I_{dis,rms} = I_{sw1,rms}$ from (6.89). Factor 2 in (6.93) stands for the two capacitors in the half-bridge input stage configuration.

Input stage

As already mentioned before, input stage is the primary-side switching part of a SICAM with non-modulated transformer voltages, which operates with constant duty cycle equal to $D = 0.5$.

Looking closely at the input stage conduction losses, two cases from all possible current conduction situations are very simple:

1. Primary current has the same direction throughout one switching period - assuming that the load current keeps the same direction, this corresponds to the situation where the output stage is not performing any switching for load current commutation during that interval; and
2. Primary current reverses after D=0.5 - switching of the input stage happens simultaneously with the switching of the output stage, therefore the reflected load current changes the direction on the primary side.

All other cases fall in between these two limit cases.

In the first case, if the primary current is conducted through the upper MOSFET in the input stage switching leg during $0 < t < DT_s$, for $DT_s < t < T_s$ the same primary current is conducted by the lower freewheeling diode. In the second case, if for $0 < t < DT_s$ primary current is flowing through the upper MOSFET then for $DT_s < t < T_s$ current is flowing through the lower MOSFET, or if for $0 < t < DT_s$ primary current is flowing through the lower freewheeling diode then for $DT_s < t < T_s$ current is flowing through the upper freewheeling diode. These latter two cases are probably two extremes in terms of

power dissipation in the switching components of the input stage and neither is dominant, so only the first case with constant direction of the primary current will be discussed.

The conduction loss in a single MOSFET, conducting the primary current for a half of the switching interval is:

$$P_{con1,T} = \frac{1}{2} R_{DS} I_{sw1,rms}^2 \tag{6.94}$$

and in the diode for the same time:

$$P_{con1,D} = \frac{1}{2} V_F I_{sw1,av} \tag{6.95}$$

where R_{DS} is the on-resistance of the MOSFET and V_F is the forward voltage drop of the MOSFET body diode (or discrete diode, if used) at current of $I_{sw1,av}$.

Total conduction losses in the input stage represent sum of (6.94) and (6.95):

$$P_{con1} = P_{con1,T} + P_{con1,D} = \frac{1}{2} R_{DS} I_{sw1,rms}^2 + \frac{1}{2} V_F I_{sw1,av} \tag{6.96}$$

Switching losses in the input stage at high switching frequencies and with the voltage levels in excess of several hundreds of Volts can be quite high. MOSFETs' switching waveforms and power losses are dependent on several nonlinear parameters at the same time: the output and input parasitic capacitance of the MOSFETs, Miller charge, inserted dead time, as well as the magnetizing and reflected load current. The same problem can be solved in an approximative way, if the losses associated with the non-zero voltage and current during transition are separated from the losses arising from the finite parasitic output capacitance.

First the switching transitions will be analyzed and all relevant time intervals given in Fig. 6.30 will be determined, for the case where the gate drive v_g of both MOSFETs continuously changes between 0 V and $+V_G$ using some semiconductor MOSFET driver. Because of the specified positive current direction, when switching off the upper MOSFET load current I commutates to the lower freewheeling diode. This leads to time intervals equations similar to those given in [14].

The time delay before rise t_{dr} is found by solving the following exponential equation:

$$\begin{aligned} &v_g = -V_G e^{-\frac{t}{R_G C_{iss}}} + V_G \\ &t = t_{dr} \implies v_g = V_{GS,th} + \frac{I}{g_{fs}} \end{aligned} \tag{6.97}$$

which results in:

$$t_{dr} = R_G C_{iss} \ln \frac{V_G}{V_G - V_{GS,th} - \frac{I}{g_{fs}}} \tag{6.98}$$

The time delay before fall t_{df} is found by solving the following exponential equation:

$$\begin{aligned} &v_g = V_G e^{-\frac{t}{R_G C_{iss}}} \\ &t = t_{df} \implies v_g = V_{GS,th} + \frac{I}{g_{fs}} \end{aligned} \tag{6.99}$$

which results in:

$$t_{df} = R_G C_{iss} \ln \frac{V_G}{V_{GS,th} + \frac{I}{g_{fs}}} \tag{6.100}$$

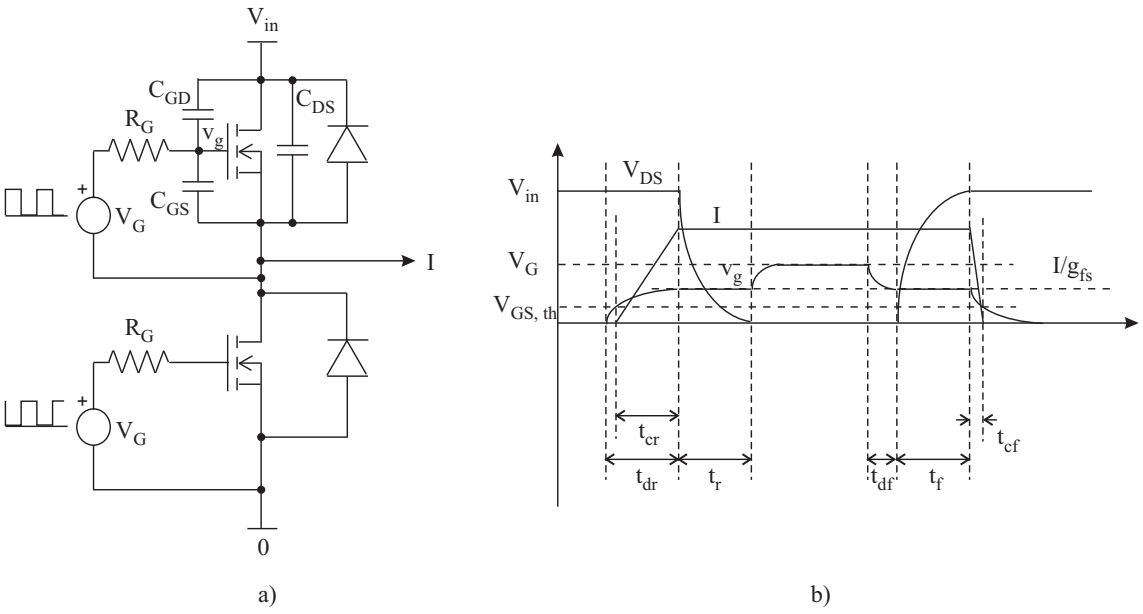

Fig. 6.30. Switching transitions of the upper MOSFET in a switching leg driven with $0, V_G$: a) schematic and b) waveforms

t_{dr} and t_{df} represent the time delays from the moment the transition is initiated until the moment the corresponding transition is actually started and is visible as a change in the MOSFET voltage. It is clear from the equations that these times depend on the electrical characteristics of the MOSFET ($C_{iss},\ V_{GS,th},\ g_{fs}$), current I being switched, as well as the driving circuitry ($V_G,\ R_G$).

The rise time t_r and the fall time t_f on the other hand represent the time needed to accomplish the desired transition of the switch drain-source voltage and are equal to the time the gate driver current $([V_G, 0] - v_g)/R_G$ needs to charge/discharge the Miller capacitance C_{GD}:

$$\begin{aligned} t_r &= \frac{Q_{GD} R_G}{V_G - V_{GS,th} - \frac{I}{g_{fs}}} \\ t_f &= \frac{Q_{GD} R_G}{V_{GS,th} + \frac{I}{g_{fs}}} \end{aligned} \tag{6.101}$$

t_{cr} and t_{cf} represent the time intervals for the switch current to rise/fall from 0/I to I/0 correspondingly. The current rise time interval t_{cr} is found by solving the following exponential equation:

$$\begin{aligned} &v_g = (-V_G + V_{GS,th}) e^{-\frac{t}{R_G C_{iss}}} + V_G \\ &t = t_{cr} \implies v_g = V_{GS,th} + \frac{I}{g_{fs}} \end{aligned} \tag{6.102}$$

which results in:

$$t_{cr} = R_G C_{iss} \ln \frac{V_G - V_{GS,th}}{V_G - V_{GS,th} - \frac{I}{g_{fs}}} \tag{6.103}$$

The current fall time interval t_{cf} is found by solving the following exponential equation:

$$\begin{aligned} &v_g = (V_{GS,th} + \frac{I}{g_{fs}}) e^{-\frac{t}{R_G C_{iss}}} \\ &t = t_{cf} \implies v_g = V_{GS,th} \end{aligned} \tag{6.104}$$

which results in:

$$t_{cf} = R_G C_{iss} \ln \frac{V_{GS,th} + \frac{I}{g_{fs}}}{V_{GS,th}} \tag{6.105}$$

In one slightly different case, pulse transformers are used to transfer the driving pulses to the gates of the MOSFETs and the gate drive voltage continuously changes the sign $\pm V_G$. This leads to different equations for the switching time intervals from those presented above and given in [14]. However, it should be noticed that due to the parasitic resistance and leakage inductance of the pulse transformer and the tracks used to connect it with the associated gate resistor and gate/source pins of the MOSFET, real switching time intervals are likely to be somewhat larger. Therefore, calculations made here tend to be approximative to a certain degree. The switching waveforms are given in Fig. 6.31.

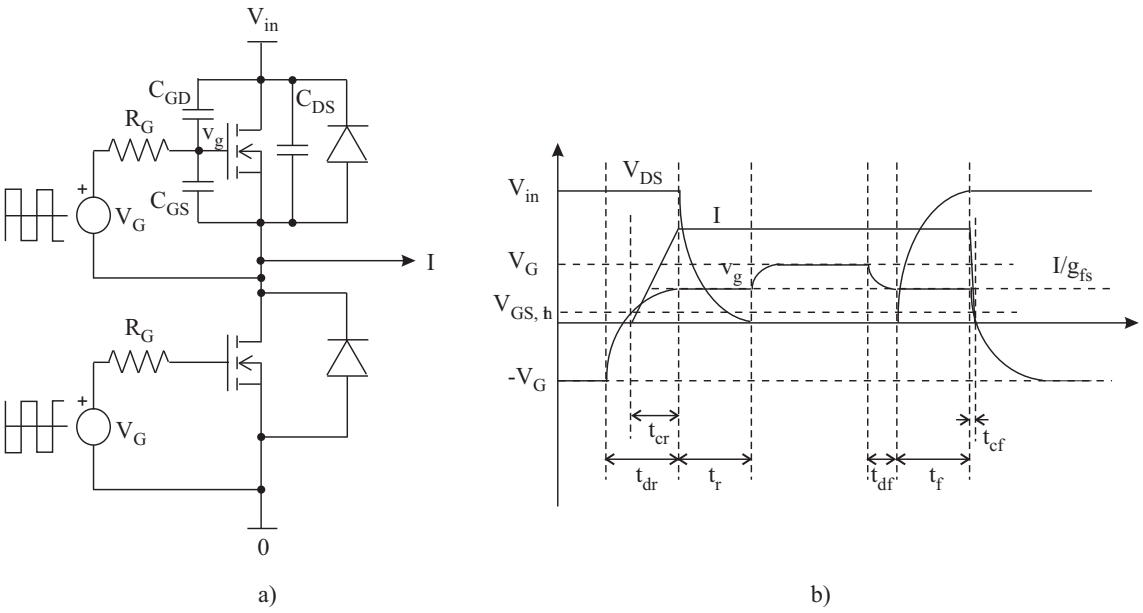

Fig. 6.31. Switching transitions of the upper MOSFET in a switching leg driven with $\pm V_G$: a) schematic and b) waveforms

The time delay before rise t_{dr} is found by solving the following exponential equation:

$$\begin{aligned} v_g &= -2V_G e^{-\frac{t}{R_G C_{iss}}} + V_G \\ t = t_{dr} &\implies v_g = V_{GS,th} + \frac{I}{g_{fs}} \end{aligned} \tag{6.106}$$

which results in:

$$t_{dr} = R_G C_{iss} \ln \frac{2V_G}{V_G - V_{GS,th} - \frac{I}{g_{fs}}} \tag{6.107}$$

The time delay before fall t_{df} is found by solving the following exponential equation:

$$\begin{aligned} v_g &= 2V_G e^{-\frac{t}{R_G C_{iss}}} - V_G \\ t = t_{df} &\implies v_g = V_{GS,th} + \frac{I}{g_{fs}} \end{aligned} \tag{6.108}$$

which results in:

$$t_{df} = R_G C_{iss} \ln \frac{2V_G}{V_G + V_{GS,th} + \frac{I}{g_{fs}}} \tag{6.109}$$

The rise time t_r and the fall time t_f on the other hand represent the time needed to accomplish the desired transition of the switch voltage and are equal to the time the gate driver current $(\pm V_G - v_g)/R_G$ needs to charge/discharge the Miller capacitance C_{GD}:

$$\begin{aligned} t_r &= \frac{Q_{GD} R_G}{V_G - V_{GS,th} - \frac{I}{g_{fs}}} \\ t_f &= \frac{Q_{GD} R_G}{V_G + V_{GS,th} + \frac{I}{g_{fs}}} \end{aligned} \tag{6.110}$$

The current rise time interval t_{cr} is found by solving the following exponential equation:

$$\begin{aligned} &v_g = (-V_G + V_{GS,th}) e^{-\frac{t}{R_G C_{iss}}} + V_G \\ &t = t_{cr} \implies v_g = V_{GS,th} + \frac{I}{g_{fs}} \end{aligned} \tag{6.111}$$

which results in:

$$t_{cr} = R_G C_{iss} \ln \frac{V_G - V_{GS,th}}{V_G - V_{GS,th} - \frac{I}{g_{fs}}} \tag{6.112}$$

The current fall time interval t_{df} is found by solving the following exponential equation:

$$\begin{aligned} &v_g = (V_G + V_{GS,th} + \frac{I}{g_{fs}}) e^{-\frac{t}{R_G C_{iss}}} - V_G \\ &t = t_{cf} \implies v_g = V_{GS,th} \end{aligned} \tag{6.113}$$

which results in:

$$t_{cf} = R_G C_{iss} \ln \frac{V_G + V_{GS,th} + \frac{I}{g_{fs}}}{V_G + V_{GS,th}} \tag{6.114}$$

As already mentioned, switching losses are result of two effects: the first effect is the finite voltage and current rise and fall time intervals associated with real switching elements, and the second one is the charging effect of the parasitic and nonlinear drain-to-source capacitance C_{DS} of the MOSFETs. Assuming sinusoidal load current, switch average value $I_{sw1,av}$ can be used to calculate the switching loss during one period of the modulating signal.

When the reflected load current to the primary side is positive, from the topology of the half-bridge in the input stage it is clear that there will be one hard turn-on and turn-off for the upper MOSFET and one soft and lossless (ZVS) turn-on and turn-off of the lower MOSFET, due to the clamping action of the freewheeling diode. Hard switchings will cause switching loss, since the voltage across the switch and current through the switch are nonzero for a short time interval $(t_r + t_{cr})$ during rise and $(t_f + t_{cf})$ during fall. The switching losses due to the finite time transitions of the MOSFETs are found by multiplying the area under the curve $v_{sw} \cdot i_{sw}$ (triangle within a linear approximation) representing the switching loss per cycle with the switching frequency f_{s1} of the half-bridge:

$$P_{sw1,tr} = \frac{1}{2} f_{s1} V_{in,max} I_{sw1,av} (t_r + t_{cr} + t_f + t_{cf}) \tag{6.115}$$

The second term of the switching losses corresponding to the parasitic drain-to-source capacitance C_{DS} can be found by noticing that every switching period each of the MOSFETs' parasitic output capacitances has been charged and discharged. Taking into account the nonlinear nature of the output capacitance $C_{DC}(V_{DS})$ with changing drain-source voltage V_{DS}, the energy lost during these transitions in an ordinary MOSFET is given by the following equation [73]:

$$E = \frac{2}{3} C_{oss} V_{oss}^{\frac{1}{2}} V_{DS}^{\frac{3}{2}} \tag{6.116}$$

However, due to the altered structure of some newer Power MOSFET structures like, for example, the p/n column structure of CoolMOS, the resulting output capacitance C_{DS} is even more nonlinear i.e. starting from a significantly higher value at $V_{DS} = 0$ V, breaking at around $V_{DS} = 50$ V and going much lower at higher voltages than compared to the ordinary technologies. In these cases the output capacitance cannot be approximated simply as $C_{DS} = C_{oss}\sqrt{V_{oss}/V_{DS}}$, so some other way of calculating the stored energy in the output parasitic capacitance must be found. Fortunately, the manufacturer is providing a fixed energy related output capacitance $C_{o,er}$, which eventually gives the same stored energy for charging to 80% of the maximum reverse voltage as the variable output capacitance C_{oss}. This energy related output capacitance can be used for calculating the switching losses:

$$E = \frac{1}{2} C_{o,er} V_{DS}^2 \tag{6.117}$$

The associated switching losses due to the finite parasitic output capacitance of the MOSFETs in the case of a half-bridge input stage are:

$$P_{sw1,cds} = 2 f_{s1} E_1 = f_{s1} C_{o,er} V_{DS}^2 \tag{6.118}$$

Total switching losses in the input stage are simply the sum of (6.115) and (6.118):

$$P_{sw1} = P_{sw1,tr} + P_{sw1,cds} \tag{6.119}$$

Total losses in the input stage are found by summing the conduction and switching losses in (6.96) and (6.119):

$$P_{tot1} = P_{con1} + P_{sw1} \tag{6.120}$$

Transformer design and losses

Transformer design is performed at the switching frequency of the input stage f_{s1}. Some of the transformer quantities have been already determined in the previous sections:

- transfer (turns) ratio $n = V_1/V_2 = N_1/N_2$
- primary RMS current (6.84): $I_{1,rms}$
- output stage RMS current (6.82): $I_{sw2,rms}$
- secondary winding RMS current from (6.82): $I_{2,rms} = I_{sw2,rms}/\sqrt{2}$

There are several different methods for design of magnetic components, like those based on the area product A_p, core geometry K_g and maximum flux density ΔB_{max} (saturation-limited design), but only the design based on the minimum of total loss $P_{cu} + P_{fe}$ yields the most efficient transformer.

The design of the transformer according to the minimum of total loss approach starts by selecting the magnetic core based on the expected transformer losses in amount of, for

example, 1% of the total transformed power and for simplicity neglecting the losses in the output stage and in the output filter:

$$P_{TR,exp} = 0.01 P_{out} \tag{6.121}$$

When choosing the appropriate magnetic core, one should reconsider the power capacity which the transformer wound on that core can handle, which is in fact dependant on its thermal resistance R_{th} as a quantity expressing the capability of the magnetic core to exchange the heat with the ambient and the allowed temperature rise ΔT over the ambient temperature, which depends primarily on the magnetic material properties.

In order to determine the number of primary turns N_1, magnetic core losses P_{fe} and copper losses P_{cu} are calculated as a function of N_1 and their sum is subsequently optimized.

Core losses P_{fe} at certain frequency are given by the following equation [60]:

$$P_{fe} = k_{fe}(\Delta B)^{\beta} A_e l_m = k_{fe}(\Delta B)^{\beta} V_m = p_{fe} V_m \tag{6.122}$$

where coefficients k_{fe} and β are properties of the magnetic material, ΔB is the magnetic induction (flux density) swing, A_e is the equivalent cross area of the core perpendicular to the direction of the magnetic field, l_m is the mean magnetic path length, p_{fe} is the characteristic core loss (core losses per unit volume) and V_m is the magnetic core volume.

Magnetic induction swing can be determined by noting that during the on-time of the upper MOSFET switch in the half-bridge input stage, the magnetic induction B increases twice the value of the magnetic inductance swing ΔB:

$$\Delta B = \frac{\lambda}{2 N_1 A_e} = \frac{V_1 D T_s}{2 N_1 A_e} \tag{6.123}$$

where λ is flux linkage and N_1 is the number of primary turns.

Equation (6.123) is put into (6.122) to obtain:

$$P_{fe} = k_{fe} \left(\frac{V_1 D T_s}{2 N_1 A_e} \right)^{\beta} V_m \tag{6.124}$$

Coefficients k_{fe} and β are determined from the diagram of the specific power losses $p_{fe} = p_{fe}(f, \Delta B)$ for the corresponding magnetic material at the desired switching frequency, by taking two points with different flux density swing ΔB and fitting the curve (6.124). This procedure results in the following equations for the coefficients:

$$\begin{aligned} \beta &= \frac{\ln\left[(p_{fe}^{\Delta B_2})/(p_{fe}^{\Delta B_1})\right]}{\ln\left[(\Delta B_2)/(\Delta B_1)\right]} \\ k_{fe} &= \frac{p_{fe}^{\Delta B_1}}{\Delta B_1^{\beta}} \end{aligned} \tag{6.125}$$

If the temperature of the core in operation is not known in advance because of, for example, ambient temperature variations, it makes sense to average the results of k_{fe} and β for two different temperatures commonly given in the datasheet.

Copper losses are easily calculated using [60]:

$$P_{cu} = k_{ac} \frac{\rho (MLT) N_1^2 I_{tot}^2}{W_a k_u} \tag{6.126}$$

where k_{ac} is the lumped increase of the DC resistance due to skin and proximity effect (the primary and the secondary side together), $\rho = 23 \cdot 10^{-9} \Omega m$ is the characteristic resistance of copper, (MLT) is the mean length of a turn, W_a is the core window area, $I_{tot} = \sum N_j I_j / N_1$ is the total current referred to the primary, k_u is the filling factor of the core window area. Since the AC resistance factor k_{ac} strongly depends on the actual arrangement of windings, it can be initially set to $k_{ac} = 3$ in the provisional calculation for selecting the primary number of windings N_1, to account for extra resistance when the copper winding is exposed to an alternating electromagnetic field. Filling factor is usually chosen to be around $k_u = 0.5$, due to the additional insulation layers between the windings to fulfil the safety requirements. The actual values for the AC-resistance of the particular windings k_{ac1} and k_{ac2} can be determined after the initial transformer design is done and the calculation of copper losses in (6.126) can be refined for the next round of the design process.

Total transformer losses P_{TR} equal to:

$$P_{TR} = P_{fe} + P_{cu} = P_{fe} + P_{cu1} + P_{cu2} \tag{6.127}$$

Building a center-tapped transformer presents some unique challenges in determining the allowed volume for the primary winding and each of the secondaries windings, which eventually affects the distribution of the copper losses. Using the results of the copper loss optimization in [60], the recommended winding area is:

$$\begin{aligned} \alpha_1 &= \frac{N_1 I_1}{N_1 I_1 + 2 N_2 I_2} = \frac{N_1 I_1}{N_1 I_1 + 2 N_1 I_1 \frac{1}{\sqrt{2}}} = \frac{\sqrt{2}}{\sqrt{2}+2} \approx 0.41 \\ \alpha_2 &= \frac{N_2 I_2}{N_1 I_1 + 2 N_2 I_2} = \frac{N_2 I_2}{N_2 I_2 \sqrt{2} + 2 N_1 I_1 \frac{1}{\sqrt{2}}} = \frac{1}{\sqrt{2}+2} \approx 0.29 \end{aligned} \tag{6.128}$$

The result in (6.128) is logical, since both secondary windings in average conduct current for half of the time and optimally each of them should occupy less volume then the continuously conducting primary winding. On the other hand, the RMS value of the current in each of the secondaries is lower than the output stage current only for a factor of $\sqrt{2}$, so both secondaries must occupy a little bit more space than the single primary winding.

Graph of the transformer power losses, like the one given in Fig. 6.32, can be used to select the optimal number of primary turns N_1.

Primary number of turns N_1 can be chosen slightly away from the optimal number of turns, just to obtain secondary windings with an integer number of turns N_2 or to account for some additional copper or core losses.

After the number of turns in both windings have been determined, it is decided about the actual arrangement of the windings in a way that reduces proximity losses and stray fields, usually by interleaving the windings and maybe even using Litz wire. Afterwards it is possible to determine the AC resistance factor $k_{ac} = R_{ac}/R_{dc}$ using the Dowell's curves for eddy current and proximity losses in [82], [60] to calculate copper losses in the primary and secondary windings:

$$\begin{aligned} P_{cu1} &= 4 k_{ac1} \frac{\rho (MLT) N_1}{\pi d_1^2} I_{1,rms}^2 \\ P_{cu2} &= 4 k_{ac2} \frac{\rho (MLT) N_2}{\pi d_2^2} I_{2,rms}^2 \end{aligned} \tag{6.129}$$

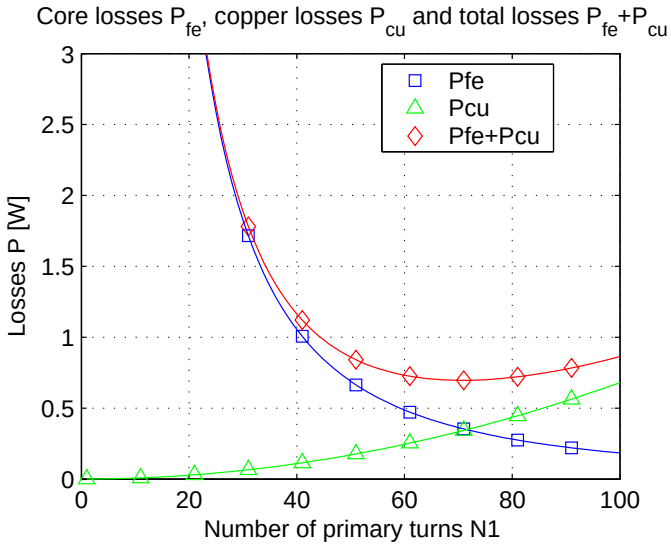

Fig. 6.32. Core losses P_{fe}, copper losses P_{cu} and total losses P_{TR} as a function of the primary number of turns N_1

Output stage

To simplify the output stage analysis, positive direction of the load current throughout the switching period will be adopted, like in the case of the input stage. One pair of series-connected common-source MOSFETs is conducting for half of the period followed by conduction of the other pair of series MOSFETs supporting the same load current direction for the other half period.

When the load current direction is fixed during one switching period, in the bidirectional switch one MOSFET is conducting the load current in the forward direction and the other one is conducting the current in reverse direction, either through the MOSFET channel or through the parasitic diode. Therefore it is difficult to calculate exactly the conduction losses, but analysis can be simplified by looking at the voltage drop across the reverse conducting MOSFET during one half-period of the audio output voltage at maximum output power and neglect the switching action, as shown in Fig. 6.33.

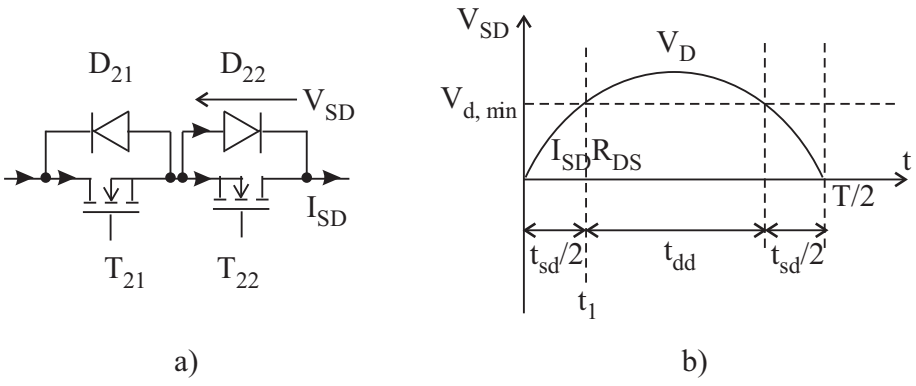

Fig. 6.33. a) Bidirectional switch and b) Voltage drop across the reverse conducting MOSFET

Commutation of the load current from the N channel of the MOSFET to the PN junction of the parasitic diode occurs at some minimum current level $I_{SD,min}$, when the corresponding diode voltage drop is $V_{d,min}$ as shown in Fig. 6.33:

$$V_{d,min} = R_{DS} I_{SD,min} \tag{6.130}$$

Through inspection of the V-I curves of the MOSFET parasitic diode (or an antiparallel discrete diode) and knowing the on-resistance of the MOSFET N channel, the minimum current $I_{SD,min}$ can be found.

Time intervals t_{sd} and t_{dd} corresponding to the conduction intervals of the N channel of the MOSFET and the parasitic diode can be found by noting that t_1 is the time instant when the load current reaches $I_o = I_{SD,min}$:

$$\begin{aligned} I_{SD,min} &= I_{o,pk} \sin(\omega_m t_1) \\ t_1 &= \frac{1}{2\pi f} \arcsin \frac{I_{SD,min}}{I_{o,pk}} \end{aligned} \tag{6.131}$$

The corresponding duty cycles of the N channel of the MOSFET D_{sd} and of the parasitic diode D_{dd} are:

$$\begin{aligned} D_{sd} &= \frac{2t_{sd}}{T} = \frac{4t_1}{T} \\ D_{dd} &= \frac{2t_{dd}}{T} = \frac{2(\frac{T}{2} - 2t_1)}{T} \end{aligned} \tag{6.132}$$

The conduction losses in the MOSFETs are therefore calculated as a sum of fixed losses in the forward conducting MOSFET as well as the losses in the other MOSFET distributed between the N channel and the PN-junction of the parasitic diode (neglecting dynamic resistance R_D):

$$\begin{aligned} P_{con2} &= R_{DS} I_{sw2,rms}^2 + \left(R_{DS} I_{sw2,rms}^2 D_{sd} + V_F I_{sw2,av} D_{dd}\right) = \\ &= R_{DS} I_{sw2,rms}^2 (1 + D_{sd}) + V_F I_{sw2,av} D_{dd} \end{aligned} \tag{6.133}$$

Switching losses in SICAMs with load clamps

While the mechanism of creating conduction losses is the same in both the SICAM with safe-commutation switching strategy and the SICAM with load clamp, switching losses are very different because of the essential differences in the switching methods. Therefore, they will be analyzed separately in the aforementioned two cases.

On the other hand, it will be assumed that the leakage inductances of the secondary side transformer windings can be neglected, so the energy stored in them is very small. This is very important, since whenever there is hard switching of the output stage with an abrupt interruption of the load current path through the bidirectional switch, the energy stored in the leakage inductances must be released in some way, which is usually done by some violent oscillatory actions between the leakage inductance and parasitic capacitance of the MOSFETs, creating losses on the resistive elements in the circuit or through avalanching of the MOSFETs, if the voltage blocking rating of the active devices is inadequate. This emphasizes the need for reducing the secondary-side leakage inductance of the transformer through interleaving of windings and selecting transformer magnetic cores with higher winding windows, choosing control methods which guarantee soft-switching of the output stage for most of the time or control methods where the load current continues to flow through another secondary winding in the SICAMs with central-tapped transformer secondary and tightly coupling these two secondary windings to reduce their leakage inductances. In practical implementations, in most of the cases there will be special *RC*-snubbers across the transformer secondary to handle the stored magnetic energy in the leakage inductance during the switching instants.

Switching of the bidirectional switches in the output stage of a SICAM with load clamps represents hard-switching, where a blanking (dead) time is inserted between the outgoing and the incoming switch during which load current is diverted into the clamp.

Similar to the input stage, during the switching of the output stage there are two lossy mechanisms: one corresponds to the finite transition times during which both current and voltage are non-zero and the other one is the energy stored in the parasitic output capacitances of the MOSFETs, which is eventually dissipated when the MOSFETs are turned on.

The switching process in the output stage is also similar to the one described for the input section, with several minor differences:

- Both gate driving circuits for the upper and lower bidirectional switch are driving two input gate capacitances C_{iss} in parallel, giving a resultant gate capacitance of $2C_{iss}$. This eventually result in longer delays t_{dr}, t_{df} and longer current rise/fall time intervals t_{cr}, t_{cf};
- In a bidirectional switch with two common-source connected MOSFETs, one of the MOSFETs always has a forward biased parasitic diode, so there are no losses associated with the switching of that particular MOSFET neither due to the switching transition nor due to the stored charge in the output capacitance;
- Regarding the previous remark, gate driving circuitry should only discharge or charge a single Miller capacitance Q_{GD} of the MOSFET doing the voltage blocking, i.e. the voltage rise/fall time intervals t_r, t_f for a 4QSW stay eventually the same as for a single MOSFET.

It should be noted, however, that the aforementioned characteristics are pertinent to the bidirectional switch with common-source connection of the individual MOSFETs. These conclusions and the calculation presented below are likely to be different for every other combination of switches, but the development will always follow the same lines.

The switching losses due to finite time transitions $P_{sw2,tr}$ of two 4QSWs, with blocking voltage in excess of $2V_{2,max}$ will amount to:

$$P_{sw2,tr} = 2 \cdot \frac{1}{2} f_{s2}(2V_2) I_{sw2,av}(t_r + t_{cr} + t_f + t_{cf}) = 2 f_{s2} V_2 I_{sw2,av}(t_r + t_{cr} + t_f + t_{cf}) \quad (6.134)$$

where the switching time intervals are given with the same equations like for the input stage section, with two times larger input capacitance C_{iss} and $I = I_{sw2,av}$.

The switching loss mechanism regarding the stored charge in the finite parasitic output capacitances of the MOSFETs C_{DS} becomes more complex in the case of the bidirectional bridge in the output stage. These losses are created in two ways:

- When the output stage switches, which is similar to the case of conventional Class D audio power amplifiers operating from a DC power supply, and
- When the input stage switches, which causes reversal of voltage polarity across the HF-link and thus reversal of the voltage across the blocking pair of MOSFETs.

The latter effect results in additional switching losses associated with discharging one and charging the other parasitic output capacitance C_{DS} of the MOSFETs in the same blocking bidirectional switch when the input stage has switched.

When looking at the switching losses in the output stage of a SICAM with a load clamp and caused by the switching of the output stage itself, these additional switching losses due to parasitic output capacitance of the bidirectional switches (4QSWs) are observed during the dead time periods when the voltage across the load and the output filter i.e. the bridge voltage is clamped to the capacitive clamp voltage. The polarity of the bridge

voltage v_{br} depends on the load current i_o direction and for example in Fig. 6.19 for $i_o > 0$ it is $v_{br} = -V_{cl}$ and for $i_o < 0$ it is $v_{br} = V_{cl}$. Due to this, when one of the 4QSWs is turned on and has zero voltage across it, the other one has $2V_{2,max}$ across it; but as soon as both 4QSWs are turned off and bridge voltage is clamped to $\pm V_{cl}$, the blocked voltages of 4QSWs will become $V_{DS} = V_{cl} \pm V_2$ during the whole dead time, if the load current keeps the same direction. One possible switching sequence of the output stage in a SICAM with load clamp, together with the drain-source voltage V_{DS} of the blocking MOSFET for $v_{HF} = +V_2$ and $V_{cl} > V_2$ (as proposed in SICAMs with active capacitive load voltage clamps) is given in Table 6.4.

Table 6.4. One possible switching sequence of the output stage in SICAM with load clamp with $v_{HF} = +V_2$

$T_{21} - T_{22}$ on	$V_{DS} = 0$	before switching off $T_{21} - T_{22}$
$T_{23} - T_{24}$ off	$V_{DS} = 2V_2$	
$T_{21} - T_{22}$ off	$V_{DS} = V_{cl} + V_2$	$i_o > 0$
$T_{23} - T_{24}$ off	$V_{DS} = V_{cl} - V_2$	
$T_{21} - T_{22}$ off	$V_{DS} = V_{cl} - V_2$	$i_o < 0$
$T_{23} - T_{24}$ off	$V_{DS} = V_{cl} + V_2$	
$T_{21} - T_{22}$ off	$V_{DS} = 2V_2$	after switching on $T_{23} - T_{24}$
$T_{23} - T_{24}$ on	$V_{DS} = 0$	

From Table 6.4 it becomes clear that with certain load current direction and HF-link voltage polarity, one of the bidirectional switches experiences maximum blocking voltage of $V_{DS} = 2V_2$ and the other one $V_{DS} = V_{cl} + V_2$. Due to the symmetrical modulating wave and symmetrical HF-link voltage, these blocking voltages change between the bidirectional switches on a regular basis to average and equalize these switching losses between them.

The maximum energy which is stored in the parasitic capacitance of a single MOSFET of a bidirectional switch during switching of the output stage of a SICAM with load clamp at drain-source voltage of $V_{DS} = V_{cl} + V_2$ can be found using (6.116):

$$E_{22,max} = \frac{2}{3} C_{oss} V_{oss}^{\frac{1}{2}} (V_{cl} + V_2)^{\frac{3}{2}} \tag{6.135}$$

and the minimum stored energy at drain-source voltage of $V_{DS} = 2V_2$ is similarly:

$$E_{22,min} = \frac{2}{3} C_{oss} V_{oss}^{\frac{1}{2}} (2V_2)^{\frac{3}{2}} \tag{6.136}$$

As mentioned earlier, switching losses due to the parasitic output capacitances of 4QSWs in the output stage of a SICAM are created also as a result of the switching of the input stage which changes the polarity of the HF-link voltage. The amount of energy stored in C_{DS} during these changes of the HF-link polarity are given with the same equation (6.136):

$$E_{21} = \frac{2}{3} C_{oss} V_{oss}^{\frac{1}{2}} (2V_2)^{\frac{3}{2}} \tag{6.137}$$

The switching loss in the output section, caused by switching of both the input and the output section $P_{sw2,cds}$ is obtained in the following way:

$$P_{sw2,cds} = 2 f_{s1} E_{21} + f_{s2} (E_{22,min} + E_{22,max}) \tag{6.138}$$

Total switching losses in the output stage are simply the sum of (6.134) and (6.138):

$$P_{sw2} = P_{sw2,tr} + P_{sw2,cds} \tag{6.139}$$

Switching losses in SICAMs with safe-commutation switching strategy

As already shown in Table 6.3, switching of the bidirectional switches in the output stage of a SICAM with safe-commutation switching strategy is much more complicated than in the case of a SICAM with load clamp. Commutation of the load current can be forced and thus lossy, or natural and therefore lossless, but it depends on the duration of the natural commutation Δt_{nc} in (6.34) and the allowed commutation delay Δt_d.

Similar to the output stage of SICAM with load clamp, during the switching of the output stage there are two lossy mechanisms: one corresponds to the finite transition times during which both current and voltage are non-zero and the other one is the energy stored in the parasitic output capacitances of the MOSFETs, which is eventually dissipated when the bidirectional switches are turned on or when input stage changes the polarity of the HF-link voltage. There is, however, one important difference: the gate driving circuits for the upper and lower bidirectional switch are now driving each of the individual MOSFETs separately i.e all input gate capacitances C_{iss} are driven independently via separate gate resistors.

In the case when the commutation delay Δt_d between different steps in the commutation process is longer than the natural commutation time interval Δt_{nc}, there is enough time for the load current to commutate from the outgoing switch to the incoming switch, so there is just one lossy turn-off (from the forced commutation) and one almost ZCS and lossless turn-on (from the natural commutation) during a switching period. In the case when the commutation delay Δt_d is smaller than the natural commutation time interval Δt_{nc}, there is one lossy turn-off (from the forced commutation) and one almost ZCS and lossless turn-on, followed by partially lossy turn-off (from the natural commutation) with the rest of the load current which was naturally commutating.

The only problem when calculating the switching losses caused by the naturally commutating load current is that, in contrast with the switching waveforms in Fig. 6.30 and Fig. 6.31, the switch current limited by the leakage inductance continues increasing or decreasing during the intervals t_r and t_f when the drain-source voltage decreases or increases. This leads to the following energy loss in the naturally commutating incoming switch at turn-on:

$$\begin{aligned} E_{nc,on} &= \int_0^{t_r} v_{ds}(t) i_{sw}(t) dt = \int_0^{t_r} \big(1 - \frac{t}{t_r}\big) V \cdot \frac{t}{t_r} I_{in,nc} dt = \\ &= V I_{in,nc} \int_0^{t_r} \big(\frac{t}{t_r} - \frac{t^2}{t_r^2}\big) dt = \frac{1}{6} V I_{in,nc} t_r \end{aligned} \tag{6.140}$$

where the current in the naturally commutating incoming switch $i_{in,nc}$ is limited by the secondary-side leakage inductance and is increasing linearly to its final value $I_{sw2,av}$, so that its value at the end of the rise time t_r is:

$$I_{in,nc} = \frac{t_r}{\Delta t_{nc}} I_{sw2,av} \tag{6.141}$$

Similarly, the energy loss in the naturally commutating outgoing switch with not completely commutated switch current $I_{out,nc}$ at turn-off is:

$$E_{nc,off} = \frac{1}{6} V \Delta I_{out,nc} t_f + \frac{1}{2} V (I_{out,nc} - \Delta I_{out,nc})(t_f + t_{cf}) \tag{6.142}$$

where $\Delta I_{out,nc}$ is the decrease of the naturally commutating current in the outgoing switch during the fall time t_f:

$$\Delta I_{out,nc} = \begin{cases} 0 & , \Delta t_d > \Delta t_{nc} \\ \dfrac{t_f}{\Delta t_{nc}} I_{sw2,av} & , \Delta t_d < \Delta t_{nc} \end{cases} \tag{6.143}$$

and the current in the hard-switched outgoing switch $I_{out,nc}$ with partially naturally commutated current is:

$$I_{out,nc} = \begin{cases} 0 & , \Delta t_d > \Delta t_{nc} \\ \left(1 - \dfrac{\Delta t_d}{\Delta t_{nc}}\right) I_{sw2,av} & , \Delta t_d < \Delta t_{nc} \end{cases} \tag{6.144}$$

leading to the final expression for the energy loss in the naturally commutating outgoing switch:

$$E_{nc,off} = \frac{1}{6} V \frac{t_f}{\Delta t_{nc}} I_{sw2,av} t_f + \frac{1}{2} V (I_{out,nc} - \frac{t_f}{\Delta t_{nc}} I_{sw2,av})(t_f + t_{cf}) \tag{6.145}$$

It should be noted that because of the definition of the outgoing switch currents in (6.143) and (6.144), the energy loss at turn-off in (6.145) can be zero if the load current has naturally commutated to the incoming switch before the outgoing switch has been turned off.

The two situations with commutation delay Δt_d longer or shorter than the natural commutation interval Δt_{nc} can be therefore represented with the same equation:

$$\begin{aligned} P_{sw2,tr} &= \frac{1}{2} f_{s2}(2V_2) I_{sw2,av}(t_f + t_{cf}) + \frac{1}{6} f_{s2}(2V_2) I_{in,nc} t_r + \\ &+ \frac{1}{6} f_{s2}(2V_2) \Delta I_{out,nc} t_f + \frac{1}{2} f_{s2}(2V_2)(I_{out,nc} - \Delta I_{out,nc})(t_f + t_{cf}) = \\ &= f_{s2} V_2 I_{sw2,av}(t_f + t_{cf}) + \frac{1}{3} f_{s2} V_2 I_{in,nc} t_r + \\ &+ \frac{1}{3} f_{s2} V_2 \Delta I_{out,nc} t_f + f_{s2} V_2 (I_{out,nc} - \Delta I_{out,nc})(t_f + t_{cf}) \end{aligned} \tag{6.146}$$

where the switching time intervals are given with the same equations like for the input stage section.

It should be noted that in the theoretical case when there is no leakage inductance on the secondary side, natural commutation happens immediately $\Delta t_{nc} = 0$ and there will be switching loss only at turn-on of the incoming switch, while turn-off of the outgoing switch will be lossless:

$$\begin{aligned} P_{sw2,tr} &= \frac{1}{2} f_{s2}(2V_2) I_{sw2,av}(t_f + t_{cf}) + \frac{1}{2} f_{s2}(2V_2) I_{sw2,av}(t_r + t_{cr}) = \\ &= f_{s2} V_2 I_{sw2,av}(t_f + t_{cf} + t_r + t_{cr}) \end{aligned} \tag{6.147}$$

When looking at the switching losses due to parasitic output capacitance of the bidirectional switches (4QSWs) in the output stage of a SICAM with safe-commutation switching strategy and caused by the switching of the output stage itself, there is one important difference when compared to the SICAM with load clamp.

In the output stage of a SICAM with load clamp, bidirectional switches are operated with dead time and afterwards both MOSFETs in one of the bidirectional switches are turned on, thus creating a path for capacitive inrush current which is immediately discharging the MOSFET which was performing the whole blocking. There is no specific

mechanism for decreasing these switching losses, because during the dead time load current is diverted into the clamp due to nonexistence of freewheeling current path through the bidirectional switches.

On the other hand, in SICAMs where the load current is commutated using a safe-commutation switching strategy, MOSFETs in the bidirectional switches are turned on and off independently in a way that assures there is no short circuit on the transformer secondary during switching, which essentially leaves some spaces for the load current to perform lossless charging/discharging of the parasitic output capacitances. If the load current is insufficient to perform this function and there is no natural commutation, then the turn-on of the second MOSFET in the incoming bidirectional switch will cause the aforementioned capacitive inrush current to immediately charge the output capacitances of the MOSFETs being switched-off previously.

Calculating the switching losses due to the finite parasitic output capacitances of the bidirectional switches due to the switching of the output stage will be facilitated by the diagram in Fig. 6.34. It represents the time waveform of the energy stored in the parasitic output capacitance given by (6.137) as being constant, since constant peak HF-link voltage has been assumed, while the energy stored in the leakage inductance of the transformer secondary follows the shape of the sinusoidal load current. The filter ripple current is also a part of the secondary-side transformer current, but it has been neglected in order to simplify the mathematical development. The instant t_1 at which these energies are equal is the first moment when there will be no switching losses due to the latter effect:

$$\frac{2}{3}C_{oss}V_{oss}^{\frac{1}{2}}(2V_2)^{\frac{3}{2}} = \frac{1}{2}L_{sl}M^2I_{o,pk}^2\sin^2(\omega_m t_1) \tag{6.148}$$

leading to:

$$t_1 = \frac{1}{4\pi f_m}\arccos\left[1 - \frac{8}{3L_{sl}M^2I_{o,pk}^2}C_{oss}V_{oss}^{\frac{1}{2}}(2V_2)^{\frac{3}{2}}\right] \tag{6.149}$$

Average switching losses due to the finite parasitic output capacitance of the bidirectional switches in the output stage of a SICAM with safe-commutation switching strategy as a result of the switching of the output stage are given by the following integral:

$$\begin{aligned} E_{22} &= \frac{4}{T_m}\int_0^{t_1}\left[\frac{2}{3}C_{oss}V_{oss}^{\frac{1}{2}}(2V_2)^{\frac{3}{2}} - \frac{1}{2}L_{sl}M^2I_{o,pk}^2\sin^2(\omega_m t)\right]dt = \\ &= \frac{4}{T_m}\frac{2}{3}C_{oss}V_{oss}^{\frac{1}{2}}(2V_2)^{\frac{3}{2}}t_1 - \frac{t_1}{T_m}L_{sl}M^2I_{o,pk}^2 + \frac{1}{T_m}L_{sl}M^2I_{o,pk}^2\int_0^{t_1}\cos(2\omega_m t)dt = \\ &= \frac{4}{T_m}\frac{2}{3}C_{oss}V_{oss}^{\frac{1}{2}}(2V_2)^{\frac{3}{2}}t_1 - \frac{t_1}{T_m}L_{sl}M^2I_{o,pk}^2 + \frac{1}{4\pi}L_{sl}M^2I_{o,pk}^2\sin(2\omega_m t_1) \end{aligned} \tag{6.150}$$

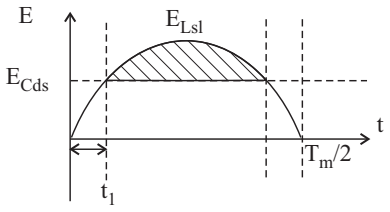

Fig. 6.34. Energy stored in the parasitic output capacitance E_{Cds} and energy stored in the transformer secondary leakage inductance E_{Lsl}

Switching losses due to the parasitic output capacitances of 4QSWs in the output stage of a SICAM with safe-commutation switching strategy as a result of the alternating HF-link voltage are created in a same way like in the SICAM with load clamp, so they are expressed with the following relation:

$$E_{21} = \frac{2}{3} C_{oss} V_{oss}^{\frac{1}{2}} (2V_2)^{\frac{3}{2}} \tag{6.151}$$

The switching loss in the output section, caused by switching of both the input and the output section $P_{sw2,cds}$ is obtained in the following way:

$$P_{sw2,cds} = 2f_{s1}E_{21} + 2f_{s2}E_{22} \tag{6.152}$$

Total switching losses in the output stage are simply the sum of (6.146) and (6.152):

$$P_{sw2} = P_{sw2,tr} + P_{sw2,cds} \tag{6.153}$$

Total losses in the output stage are found by summing the conduction and switching losses in (6.133) and (6.139) or (6.153):

$$P_{tot2} = P_{con2} + P_{sw2} \tag{6.154}$$

Output filter design and calculation of losses

The output filter starts with the analysis of a half circuit output filter, with half of the load impedance (resistance R_h), like shown in Fig. 6.35a. The transfer function $H_h(s)$ of this half circuit is:

$$H_h(s) = \frac{(R_h || \frac{1}{sC_h})}{sL_h + R_h || \frac{1}{sC_h}} = \frac{\frac{R_h}{sC_h}}{sR_hL_h + \frac{L_h}{C_h} + \frac{R_h}{sC_h}} = \frac{1}{s^2C_hL_h + s\frac{L_h}{R_h} + 1} \tag{6.155}$$

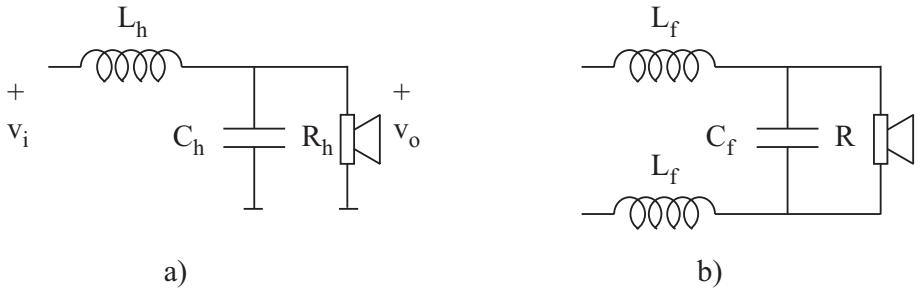

Fig. 6.35. Output filter: a) half circuit and b) full circuit

There are different possibilities for choosing the output filter type, but the most common are:

- Butterworth filter (2nd order):

$$H_{h,But}(s) = \frac{1}{\frac{s^2}{\omega_c^2} + \sqrt{2}\frac{s}{\omega_c} + 1} \tag{6.156}$$

where $\omega_c = \omega_{-3dB}$ is the filter cut-off angular frequency (-3 dB).

- Bessel filter (2nd order):

$$H_{h,Bes}(s) = \frac{1}{\frac{1}{3}\frac{s^2}{\omega_c^2} + \frac{s}{\omega_c} + 1} \tag{6.157}$$

where $\omega_c = \omega_{-3dB}/1.36165$ is the filter characteristic angular frequency, which needs to be scaled by 1.36165 to arrive at the cut-off angular frequency ω_{-3dB} (-3 dB).

Like stated in [83], Butterworth design is characterized by maximally flat magnitude response in the frequency pass-band, and the attenuation in the transition frequency band is better than Bessel. However, in time domain Butterworth filter step response experiences some overshoot and ringing and therefore Bessel filter is generally preferred.

Comparing (6.155) with (6.157) leads to the following results:

$$\begin{aligned} \frac{L_h}{R_h} &= \frac{1}{\omega_c} \quad \Longrightarrow \; L_h = \frac{R_h}{\omega_c} = \frac{R_h}{2\pi f_c} \\ C_h L_h &= \frac{1}{3\omega_c^2} \; \Longrightarrow \; C_h = \frac{1}{6\pi f_c R_h} \end{aligned} \tag{6.158}$$

The final values for the inductors L_f and the capacitor C_f of the full circuit output filter shown in figure 6.35 are found by recognizing that $R = 2R_h$, $C_f = C_h/2$ and $L_f = L_h$:

$$\begin{aligned} L_f &= \frac{R}{2\omega_c} = \frac{R}{4\pi f_c} \\ C_f &= \frac{1}{3\omega_c} = \frac{1}{6\pi f_c R} \end{aligned} \tag{6.159}$$

The characteristic Bessel frequency f_c is connected with the the cut-off frequency f_{-3dB} in the following way:

$$f_c = \frac{f_{-3dB}}{1.361654} \tag{6.160}$$

Copper losses in the output filter inductor are found by multiplying the winding resistance R_L with the square of the secondary switch current RMS value $I_{sw2,rms}^2$, comprising of load and filter ripple current:

$$P_{cu,L_f} = R_{L_f} I_{sw2,rms} = N \frac{4\rho(MLT)}{\pi d_f^2} I_{sw2,rms}^2 \tag{6.161}$$

To simplify the investigation of the core losses, zero modulation is assumed and thus zero output power, resulting in maximum ripple current $I_{fr,max}$. This means that rectangular voltage with magnitude V_2 and duty cycle $D = 0.5$ is applied to the filter inductor L, resulting in magnetic induction swing:

$$\Delta B = \frac{\lambda}{2NA_e} = \frac{V_2 D T_s}{2NA_e} = \frac{V_{out,max}}{4N f_{s2} A_e} \tag{6.162}$$

After the magnetic induction swing ΔB has been determined, one can proceed to the core loss tables to determine the corresponding specific core loss p_{fe}. Then the total core loss is obtained by multiplying the specific core losses p_{fe} with the core volume V_m:

$$P_{fe,L_f} = p_{fe} V_m \tag{6.163}$$

With the most usual designs of output filter inductors on powdered iron toroids with low permeability, the core losses are only a small fraction of the losses in the winding.

However, it is a common practice to tolerate even 20%/80% distribution between the copper and core losses, since in the inductors wound on toroidal iron powder cores, the heat removal is far more easier from a single layer winding than from the inner parts of the core itself.

The total losses in the output filter inductor are obtained by summing up the copper and core losses in equations (6.163) and (6.161):

$$P_{L_f} = P_{cu,L_f} + P_{fe,L_f} \tag{6.164}$$

Calculation of the losses dissipated in the output capacitor equivalent series resistance (ESR) is very hard without making assumptions, like assuming that the whole HF ripple current $I_{fr,rms}$ is flowing entirely through the capacitor, leaving the LF modulated current flow through the load. The ESR can be found using the tangent of loss angle $\tan\delta$ supplied by the manufacturer:

$$ESR = \tan\delta \cdot X_C = \frac{\tan\delta}{2\pi f C} \tag{6.165}$$

The losses in the capacitor ESR due to the filter ripple current $I_{fr,rms}$ are thus:

$$P_{C_f} = (ESR) \cdot I_{fr,rms}^2 \tag{6.166}$$

Total losses in the output filter represent a sum of the losses in the filter inductor (6.164) and filter capacitor (6.166):

$$P_{tot,f} = P_{L_f} + P_{C_f} \tag{6.167}$$

Losses in gate drivers

The losses in a combined high-side/low-side gate driver can be divided into high voltage and low voltage static and dynamic losses [84].

The static driver losses are result of the flow of quiescent current or leakage currents through the different power supplies or level shifting stages of the driver IC and are generally very low, in the order of few mW and therefore can be neglected.

Low voltage (LV) dynamic losses in the MOSFET gate resistance in both the driving IC and the external gate resistor in the input and the output stage are function of the switching frequency f_{s1}, f_{s2}, gate voltage levels V_{G1}, V_{G2}, as well as the MOSFET gate charge Q_{G1}, Q_{G2} in the input and the output stage, respectively:

$$\begin{aligned} P_{dr1,LV} &= 2 f_{s1} V_{G1} Q_{G1} \\ P_{dr2,LV} &= 4 f_{s2} V_{G2} Q_{G2} \end{aligned} \tag{6.168}$$

where the difference in this two equation is from the fact that the output stage has two bidirectional switches with two MOSFETs each. Another low voltage dynamic losses are due to the switching of the internal CMOS circuitry and amount to few tens of mW, so they can be neglected too.

High voltage (HV) dynamic losses happen in high-side gate driver ICs in the input stage. These are created as power is dissipated in the level shifter to transfer the driving signal from ground referenced control circuitry to the floating driver on the upper rail, or with the cyclical charging and discharging of the parasitic well capacitance between the substrate and the floating driver, which amount to:

$$\begin{aligned} P_{dr1,HVls} &= f_{s1}(V_{dc} + V_{G1}) Q_p \\ P_{dr1,HVwell} &= f_{s1} V_{dc} Q_w \end{aligned} \tag{6.169}$$

where V_{dc} is the voltage of the upper rail, Q_p is the charge absorbed by the level shifter and Q_w is the well charge, usually both in a range of few nC.

Losses in the active load voltage clamp

Losses in the active load voltage clamp can be calculated in the same way like in the conventional SMPS, by paying attention to the amount of charge dumped in the clamp capacitor during the operation of the SICAM and its transfer to the primary side to maintain charge balance. For completeness, some guidelines will be given in this section.

Conduction losses in the clamp rectifier depend on the average value of the clamp current $I_{cl,av}$ in (6.46) and diode voltage drop at that current level V_F:

$$P_{rect,cl} = 2V_F I_{cl,av} \tag{6.170}$$

The losses in the clamp capacitor due to its ESR can be calculated by using the RMS clamp capacitor current $I_{Ccl,rms}$ from (6.54) in the following way:

$$P_{Ccl} = (ESR) \cdot I_{Ccl,rms}^2 \tag{6.171}$$

Conduction losses in the active switch are found using, for example, equation (6.94) for a single switch and taking the flyback converter RMS current $I_{fb,rms}$ into account:

$$P_{con,fb} = R_{DS} I_{fb,rms}^2 \tag{6.172}$$

and the flyback converter RMS current is equal to the discharging current of the clamp capacitor $I_{fb,rms} = I_{dis,rms}$ from (6.54).

Switching losses due to switching transitions of the voltage and current in the active switch are found using, for example, equation (6.115):

$$P_{sw,fb,tr} = \frac{1}{2} f_{sfb} V_{cl} I_{fb,av} (t_r + t_{cr} + t_f + t_{cf}) \tag{6.173}$$

where f_{sfb} is the switching frequency of the flyback converter, $I_{fb,av}$ is the average value of the flyback converter current and the switching times are the same as for the input stage.

Switching loss due to the stored energy in the parasitic output capacitance C_{oss} of the active switch is found in a similar way as the one presented in the input stage. The only difference is in the number of switches which are affected, and in the case of a flyback converter it is only one:

$$P_{sw,fb,cds} = f_{sfb} E_{fb} = \frac{2}{3} f_{sfb} C_{oss} V_{oss}^{\frac{1}{2}} V_{cl}^{\frac{3}{2}} \tag{6.174}$$

Total switching losses in the flyback converter are simply sum of (6.173) and (6.174):

$$P_{sw1,fb} = P_{sw1,fb,tr} + P_{sw1,fb,cds} \tag{6.175}$$

Total losses in the active switch are found as a sum of the conduction losses in (6.172) and switching losses in (6.175):

$$P_{as,fb} = P_{con1,fb} + P_{sw1,fb} \tag{6.176}$$

Core losses in the flyback transformer are found in a similar way like in Section 6.4.2, using (6.122) and (6.123) for calculating the core loss:

$$P_{fe,fb} = k_{fe} (\Delta B)^{\beta} V_m = k_{fe} \left(\frac{V_{cl} D_{fb} T_{s,fb}}{2 N_1 A_e} \right)^{\beta} V_m \tag{6.177}$$

and (6.129) for copper losses:

$$P_{cu,fb} = P_{cu1,fb} + P_{cu2,fb} = 4k_{ac1}\frac{\rho(MLT)N_1}{\pi d_1^2}I_{fb1,rms}^2 + 4k_{ac2}\frac{\rho(MLT)N_2}{\pi d_2^2}I_{fb2,rms}^2 \quad (6.178)$$

to give the total transformer losses $P_{TR,fb}$ equal to:

$$P_{TR,fb} = P_{fe,fb} + P_{cu,fb} \quad (6.179)$$

Finally, conduction losses in the output rectifier are calculated using the average value of the flyback converter current on the secondary side $I_{fb2,av}$ and the corresponding diode voltage drop V_{F2}:

$$P_{rect2,cl} = V_{F2}I_{fb2,av} \quad (6.180)$$

Total losses in the active load voltage clamp are sum of (6.170), (6.171), (6.176), (6.179), (6.180) and amount to:

$$P_{cl} = P_{rect,cl} + P_{C,cl} + P_{as,fb} + P_{TR,fb} + P_{rect2,cl} \quad (6.181)$$

6.5 Conclusion

This chapter reviewed several different topologies of SICAM input and output stages and compared their advantages and drawbacks.

On the input side, resonant converters were found inappropriate for building SICAM input stage because of their relatively higher output impedance and large output voltage perturbations they experience when connected directly to audio power amplifiers with bidirectional power flow. ZVS PWM full-bridge inverters were also found less attractive when supplying power directly to SICAM output stage without any rectification and intermediate energy storage on the secondary side, beside of requiring a full-bridge input stage which is not economically appealing for lower output powers. Hard-switched DC-AC inverters with rectangular output voltage are reconsidered as the most suitable choice and best performer for SICAM input stage with the output power levels and switching frequencies considered in this case.

One of the disadvantages of HF-link conversion with regard to the conventional solution with isolated SMPS and Class D audio power amplifier is the need for overdimensioning the input stage, since it is required to handle both the active and reactive load power flow.

For the SICAM output stage, the commutation of the load current was pointed out as the main problem when building the amplifier with bidirectional switches. Similarities with the three-phase matrix converters were used to develop safe-commutation switching strategies, which lead to reliable operation of the output stage without any additional power components, but on behalf of more complex control requirements. On the other hand, it was shown that adding a load clamp can simplify the control of the SICAM output stage and make it similar to the Class D audio power amplifier, where blanking time is added when moving from the outgoing to the incoming switch.

Thorough analysis of the power losses in all SICAM components and stages was presented in this chapter, and will be used in the subsequent chapters for benchmarking different topologies and control methods.

7

Control methods for isolated SICAMs

"I consider that I understand an equation when I can predict the properties of its solutions, without actually solving it."

- Paul Dirac

As mentioned in the introductory Chapter 1, SICAMs need centralized control methods which are capable of operating both the input and the output stage in a way that makes possible to harness the advantages of the high level of dedication pertinent to SICAM definition. Chapter 6 showed that this control methods are very important in providing basic conditions for performing safe commutation of the load current in the SICAM output stage, like avoiding simultaneous switching in both stages. At the same time, control methods should provide simple means for reducing switching losses through decreasing the switching frequency of the output stage, without any adverse effects on the audio quality and control bandwidth. Ultimately, new and advanced control methods for SICAMs can combine the advantages of the best performing self-oscillating modulators from conventional Class D audio power amplifiers with the compact SICAM topologies presented in previous chapters, to get the best from both worlds.

All control methods presented in this chapter assume that the input stage on the primary side of the HF transformer operates with 50% duty cycle, creating non-modulated rectangular voltage on the HF-link. One possible division of these control methods is whether the operation of the input and the output stage is synchronized by locking their switching frequencies or not.

SICAMs with load voltage clamps can use many different control methods, since they do not rely on the control method to provide conditions for safe load current commutation, but have the load voltage clamp to perform this important function. On the other hand, SICAMs with safe-controlled switching strategies must be used in conjunction with smart control techniques that guarantee non-simultaneous switching of the stages, in order to keep the polarity of the HF-link voltage the same during the whole transition process of the output stage. Therefore in this section the main focus will be put predominantly on special control methods for SICAMs with safe-commutation switching strategy, but it goes without saying that SICAMs with load voltage clamps can use all of the presented methods as well, maybe with slight modifications in order to remove the unnecessary feature of non-simultaneous switching of the stages.

At the end, several closed-loop control schemes suitable for SICAM implementation are discussed.

7.1 Unsynchronized control of both stages in isolated SICAMs

7.1.1 Simple PWM modulator for unsynchronized operation

The simplest PWM modulator for HF-link converters and SICAMs in Fig. 7.1 resembles in its structure the PWM modulator with externally generated triangular carrier for common power converters with DC-bus. It uses the same double-sided triangular carrier

with a constant carrier frequency f_{c2} and amplitude V_c, introducing almost constant gain $K_{PWM} = 1/V_c$ up to the carrier frequency. The only difference is that in SICAMs, HF-link voltage is alternating and therefore the output of the comparator cannot be send directly to the gates of the bidirectional switches, but instead it needs some further processing. This is done by additional logical gates to obtain the correct gate signals, according to the instantaneous HF-link polarity, which changes with the switching frequency of the inverter stage f_{s1} i.e. the frequency of the HF-link f_{HF}. Therefore, the actual switching frequency of the bidirectional bridge f_{s2} is:

$$f_{s2} = f_{s1} + f_{c2} \tag{7.1}$$

which means that the switching frequency of the bidirectional bridge does not depend solely on the triangular carrier frequency f_{c2}, like in the conventional PWM modulators for Class D audio power amplifiers, but also on the HF-link frequency f_{HF}.

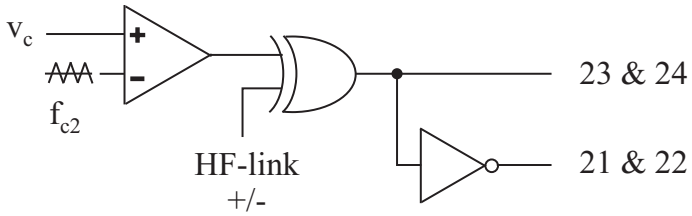

Fig. 7.1. Modified PWM modulator for SICAM

Modifications of the proposed PWM method in Fig. 7.1 are possible, which guarantee that the switching frequency of the output stage is the same as the PWM triangular carrier frequency $f_{s2} = f_{c2}$ and therefore lower switching losses than the present one, but on behalf of slightly more complex modulator scheme [85] presented in Section 7.2.2.

In this open-loop PWM control method, the switching frequency of the primary-side input stage is not related to the one of the output stage in any way, which makes this method essentially unsynchronized. However, switching of the input stage is immediately followed by switching of the output stage, to reconstruct the desired voltage polarity across the load. The biggest advantage of such unsynchronized operation of the stages is that the switching frequencies can be selected independently one from another. For the input stage, the switching frequency f_{s1} can be selected in a way that optimizes the amount of power losses and minimizes the size of the transformer, according to the available thermal interface, i.e. heat sink. On the other hand, the switching frequency of the output stage f_{s2} is usually chosen to obtain the desired control bandwidth with the minimum switching losses. Another significant advantage of the unsynchronized control is the much easier start-up of the SICAM, since both stages can start operating independently one from another. Due to the necessary level of isolation between the primary i.e. the utility grid side and the secondary i.e. the user side, usually the input stage will be the one to start first and then supply the necessary power for the control and gate driving functions of the output stage.

However, it was discovered in the practical implementations of the presented control method that unsynchronized operation gives rise to audio distortion due to idling (spurious) tones as intermodulation products of the input and the output stage switching frequencies, which are constantly shifting in the frequency domain as the device gets heated and changes slightly its characteristics. As an example, measured FFT of output noise with no input and THD+N at three different output levels of a SICAM with active capacitive voltage clamp and simple unsynchronized PWM control is given in Fig. 7.2. On

the diagrams on the left-hand side the switching frequencies of the stages were slightly different than the desired values, while on the right-hand side a tight adjustment of the switching frequencies was performed to simulate synchronized control. It is clear that when the switching frequencies of the stages are left unsynchronized, they will start crawling around their desired values and will start to create spurious components within the audio band which will eventually reduce performance. Therefore, synchronized operation of SICAM input and output stage is preferred, despite of the aforementioned increased design flexibility of the unsynchronized control method.

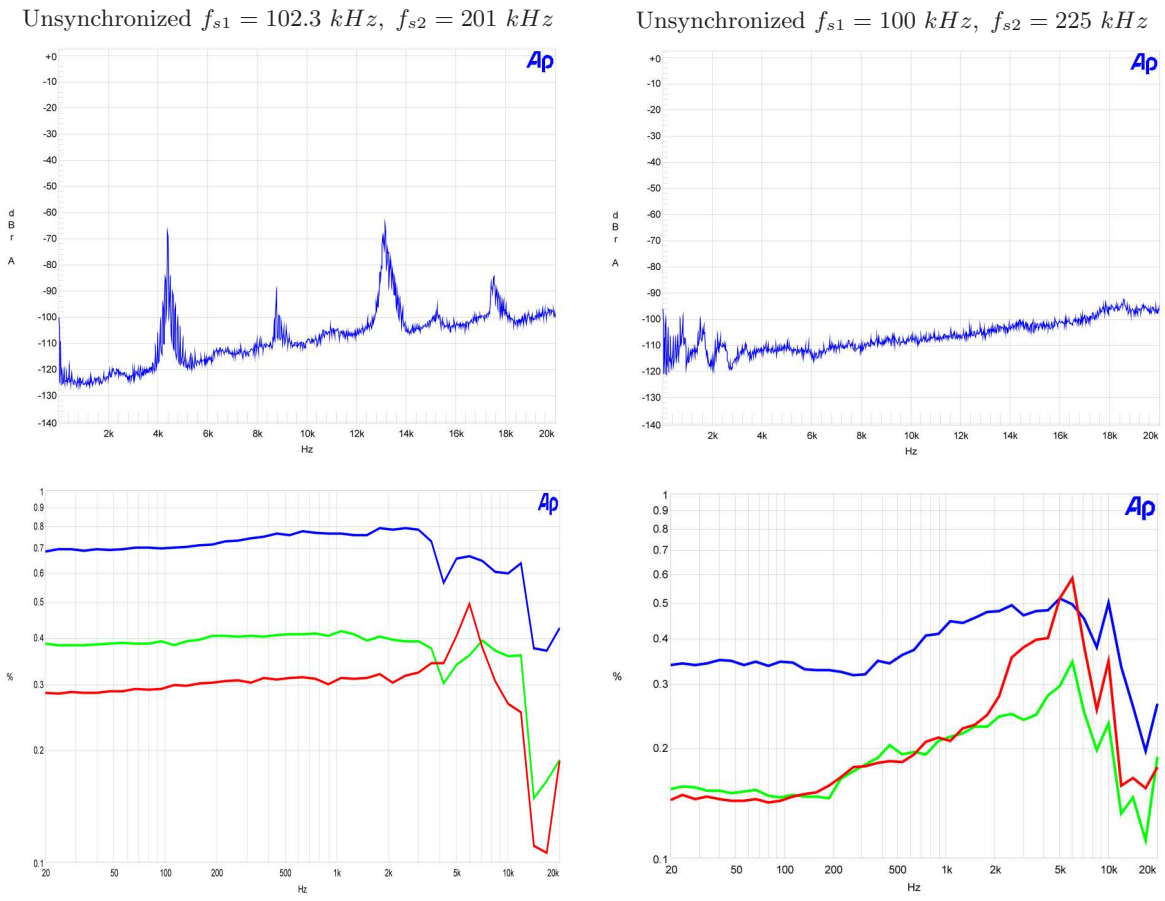

Fig. 7.2. FFT (top) and THD+N (bottom) of two unsynchronized SICAMs with and without tight control of switching frequencies

7.1.2 Master/Slave operation of the input/output stage to accomplish output stage safe commutation

One of the main problems with unsynchronized control of the input and the output stage is finding a way to guarantee non-simultaneous switching, which is necessary to undertake load current commutation with the presented voltage-controlled safe commutation switching sequence in Section 6.2.1. This problem is nonexistent in the SICAMs with load clamps, where during output stage switching the load current is diverted into the clamp.

The simplest approach for avoiding simultaneous switching of the input and the output stage with unsynchronized control is the Master/Slave operation of the input/output stage.

The premises for master/slave operation of this compound input/output stage are like follows:

1. Each of the stages can be either a master or a slave,
2. Both stages can not be masters in the same moment,
3. It is possible for both stages to reside in a slave mode at the same time,
4. Transition of one stage from slave to master is done only if the other stage is in slave mode,
5. Transition back from master to slave of one stage does not depend on the internal events in the other stage, but it allows the latter to transfer from slave to master, if it was waiting for permit.

The block diagram of the proposed master/slave control of isolated SICAMs to achieve safe commutation of the load current is depicted in Fig. 7.3. The input and the output stage in SICAM are sharing the same single logic "master/slave" line, which can have two possible states. If it is implemented with positive logic, than logic one ("1") means that one of the stages is in master mode and logic zero ("0") means that both stages are slaves. Each of the stages becomes a master, if premise 4 is satisfied and a command is issued from the control unit of the corresponding stage to make a transition: for the input stage it means that the voltage across the transformer primary is to be reversed and for the output stage it means that a commutation of the bidirectional bridge is to be undertaken in order to accommodate the audio reference. Whenever a transition is to be made and the master/slave line is idling at "0", the corresponding stage is pulling the master/slave line up to "1" occupying it for the time of its transition. Master/slave line will be released as soon as the transition has ended, but according to premise 5 this is done without any regards to the other slave stage. In this way, the "master" stage can take all the time needed to finish the transition safely. This is, however, done on expense of increased distortion, sacrificing some performance. Due to the premise 1, both stages can not be in master mode at the same time, so transitions in both stages can not occur simultaneously, thus effectively avoiding any possible dangerous commutation.

When implementing the aforementioned master/slave control algorithm, the only thing the output stage control unit still needs to know is the polarity of the HF-link voltage i.e. the primary side inverter state, so that each of the commutation commands proceeds according to the safe commutation switching pattern in Table 6.3. This is done by using a single unidirectional logic-level line from the input to the output stage, or by directly sensing the transformer voltage polarity.

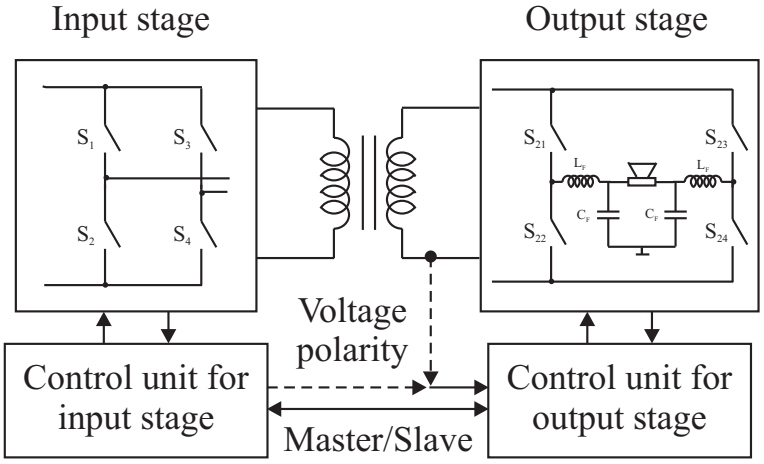

Fig. 7.3. Master/slave control of isolated SICAM with safe commutation switching strategy

By using the HF-link voltage-controlled safe-commutation sequence in Table 6.3, the use of expensive or noisy current and/or voltage sensors, which are otherwise needed in all of the other commutation methods, is avoided, but on behalf of little performance degradation. In the case of the input stage, if the transition is needed and the output stage is already making the load current commutation, thus being a master, prolonged voltage pulse will be applied which can cause increased flux in the transformer magnetic core, maybe even causing saturation if there is only a minor safety margin. In order to avoid any imbalance in the applied Volt-seconds, the control algorithm should be supplemented with a possibility to apply an equally large pulse of opposite polarity for balancing purposes, otherwise the applied DC offset will emerge across the DC blocking capacitor, causing a difference in the HF-link voltage during the positive and negative half-cycles. On the other hand, when talking about the output stage, any delay in the transition command will cause output voltage distortion, which should be subsequently compensated by the feedback control loop. Therefore, it is of prime interest to keep the transition or commutation delay times low, thus effectively avoiding larger performance degradation.

7.2 Synchronized control of both stages in isolated SICAMs

Safe-commutation sequence in Table 6.3 alone is not enough to guarantee proper operation of the amplifier at all times, since HF-link voltage is changing very fast during the switching of the input stage and can cause malfunctioning of the algorithm. Therefore it is important that the switching of the input and output stage is not done simultaneously, and this condition is taken care of in the open-loop control design.

To avoid simultaneous switching of both stages, unsynchronized switching can be combined with master-slave operation from the previous section and [53] that prohibits the slave stage to switch when the master stage is already performing transition. However, it was already mentioned that due to the non-ideality of the switching stages, unsynchronized operation can give rise to intermodulation harmonics that fall into the audio band and spoil performance.

When the operation of the stages is synchronized, the switching frequency of the output stage f_{s2} is an integer multiple of the switching frequency of the input stage f_{s1}:

$$f_{s2} = n f_{s1} \tag{7.2}$$

where $n \in \mathbf{Z}^+$, i.e. there is switching frequency locking between the stages. Beside the improved audio performance, synchronization makes it easier to avoid simultaneous switching of both stages, by performing transitions of the primary stage only at the peak or the valley of the triangular carrier in the PWM modulator and switching the output stage anywhere else by essentially limiting the modulation index of the audio signal.

The aim of the proposed synchronized PWM methods is therefore twofold: on one hand, the triangular carrier is used in the PWM modulator to compare to the reference voltage and decide the switching instants of the output stage, while on the other hand, the triangular carrier governs the transition of the input stage and HF-link voltage change, in a way that secures switching does not overlap. Furthermore, it is desirable to decrease the switching frequency of the output stage and make it ideally equal to the frequency of the triangular carrier used in the PWM modulator, which is also appealing for the SICAM with load clamp.

In the following sections, the PWM methods will be derived and thoroughly analyzed in a case when the PWM modulator triangular carrier frequency f_{c2} is two times higher than the switching frequency of the input stage f_{s1}. The characteristics of any other configuration can be determined by following the same approach.

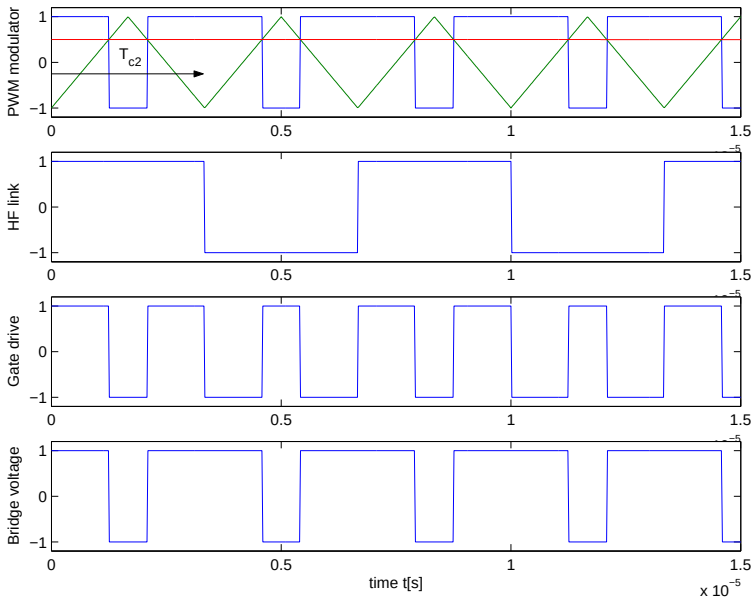

Fig. 7.4. PWM method with 3 switchings during one carrier period T_{c2}

7.2.1 Simple synchronized PWM method

Synchronized operation of the SICAM with non-modulated transformer voltages in Fig. 5.14, is shown in Fig. 7.4 in the case of $f_{c2} = 2f_{s1}$. The switching frequency of the input stage is $f_{s1} = 150$ kHz and the PWM modulator triangular carrier frequency is $f_{c2} = 300$ kHz. With this modulation scheme, output stage is switched in a way that the bridge voltage applied across the output filter and the loudspeaker resembles the PWM modulator output ideally. For this purpose, the output stage switch gate drive must be a product of the PWM modulator output F_{NADD} in (5.5) and the rectangular waveform F_r in (5.6), so the effective switching frequency of the output stage is $f_{s2} = f_{s1} + f_{c2}$ instead of just $f_{s2} = f_{c2}$, as one would normally expect. In Fig. 7.4, this PWM method results in three switchings of the output stage during one period of the carrier T_{c2}, which increases the switching losses in the output stage and reduces efficiency. On the other hand, the input stage is driven only by the synchronized rectangular waveform F_r and the switching of both stages can happen simultaneously, if it is not intentionally delayed. It can be therefore concluded that this straightforward approach complicates the SICAM design and results in number of disadvantages.

The structure of the PWM modulator is essentially the same like in Fig. 7.1, with a remark that the switching of the input stage and thus HF-link voltage changes occur simultaneously with the triangular carrier peak and/or valley.

7.2.2 Optimized PWM method with synchronization and lower output stage switching frequency

The switching frequency of the output stage f_{s2} can be made equal to the carrier frequency f_{c2} and therefore result in only two switchings per carrier period T_{c2} by giving up on the desire to exactly restore the PWM modulator output in the bridge voltage across the output filter and instead choosing a switching waveform that will give the same average value of the bridge output voltage, like the original PWM modulator waveform. This means that the switching of the output stage is not performed as soon as the HF-link changes polarity, but the switching time instants are readjusted. Looking at Fig. 7.5, this means that the average values of the bridge output voltage in the first two carrier periods

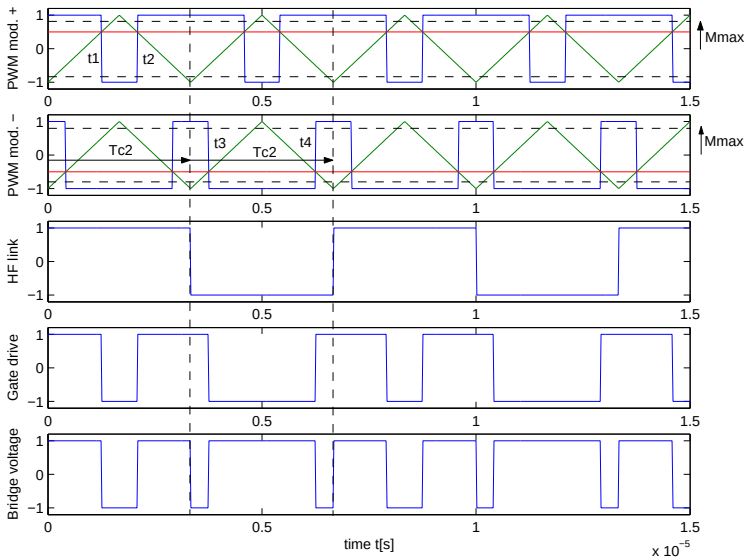

Fig. 7.5. Proposed PWM method with 2 switchings during one carrier period T_{c2}

are the same, despite the fact that the exact waveform is different. Time instants t_1 and t_2 during the half-period with positive HF-link voltage are given by:

$$\begin{aligned} t_1 &= \frac{T_{c2}}{4}\left(1 + \frac{2v_{ref}}{V_{cmax}}\right) \\ t_2 &= \frac{T_{c2}}{4}\left(3 - \frac{2v_{ref}}{V_{cmax}}\right) \end{aligned} \tag{7.3}$$

where v_{ref} is the reference voltage and V_{cmax} is the maximum carrier voltage. From (7.3), the time interval Δt_- during which negative bridge voltage is applied across the output filter while the HF-link voltage is positive is:

$$\Delta t_- = t_2 - t_1 = \frac{T_{c2}}{2}\left(1 - \frac{2v_{ref}}{V_{cmax}}\right) \tag{7.4}$$

During the second period T_{c2} when the HF-link voltage is negative, negative bridge voltage is symmetrically applied at both ends of the carrier period and in order to have the same average output voltage like in the first period T_{c2}, the time instants t_3 and t_4 must be equal to:

$$\begin{aligned} t_3 &= \frac{\Delta t_-}{2} = \frac{T_{c2}}{4}\left(1 + \frac{-2v_{ref}}{V_{cmax}}\right) \\ t_4 &= T_{c2} - \frac{\Delta t_-}{2} = \frac{T_{c2}}{4}\left(3 - \frac{-2v_{ref}}{V_{cmax}}\right) \end{aligned} \tag{7.5}$$

From (7.5) it becomes apparent that the average voltage during either polarity of the HF-link voltage in Fig. 7.5 will be equal, if the actual reference voltage is used in the PWM modulator during positive HF-link voltages and negative reference voltage is used in the PWM modulator during negative HF-link voltages, with the same form of the carrier. As long as the frequency of the reference voltage waveform is much lower than the frequency of the carrier, there will be no output voltage distortion originating from this signal manipulation. The proposed optimized PWM modulator is depicted in Fig. 7.6.

To make possible the safe-commutation of the output stage, the modulation index is limited to $M_{max} < 1$ in Fig. 7.5, so that the maximum reference voltage is slightly lower

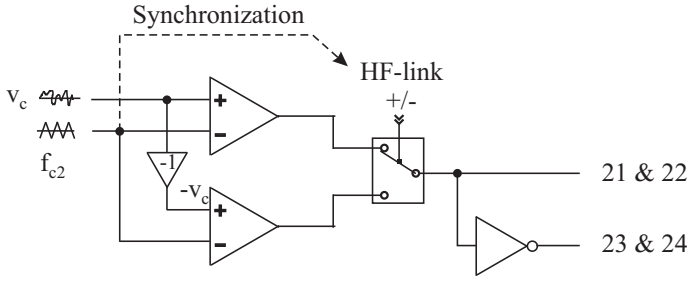

Fig. 7.6. Optimized PWM modulator for SICAM

than the peak value of the carrier voltage V_{cmax}. In this way the switching of the input stage, which is always happening at the peak or the valley of the carrier waveform, cannot be simultaneous with the switching of the output stage. The maximum modulation index M_{max} is chosen taking into account the propagation time delay Δt_1 from the secondary-to-primary-side synchronization signal is given to the moment the HF-link voltage changes, propagation time delay Δt_{2s} from the PWM modulator output to the start of the bidirectional bridge switching sequence and propagation time delay Δt_{2f} from the PWM modulator output to the finish of the same sequence, according to the following equation:

$$M_{max} = \inf\{1 - 4f_{c2}(\Delta t_1 - \Delta t_{2s}), 1 - 4f_{c2}(\Delta t_{2f} - \Delta t_1)\} \tag{7.6}$$

Frequency spectrum of the new PWM method in the case of $f_{c2} = 2f_{s1}$

It is rather interesting to compare the frequency spectrum of the bridge voltage of the conventional PWM method shown in Fig. 7.4, which is equal to F_{NADD} in (5.5), with the frequency spectrum of the bridge voltage in the case of the proposed PWM method in Fig. 7.5. The analysis will focus on the case where the carrier frequency in the PWM modulator is two times the input stage switching frequency. Thorough mathematical development of the PWM waveforms is given in Appendix E.1.

The frequency spectrum of the proposed PWM method in Fig. 7.5 can be found by breaking the PWM pulse train into two separate groups of pulses that correspond to the periods with positive and negative HF-link voltage, correspondingly, as shown in Fig. 7.7. These separate PWM trains are result of the same PWM process $F_{NADD,xh}$ with every second pulse skipped, where for the first pulse train the actual reference voltage and for the second pulse train the negative reference voltage with subsequent reversal of the PWM pulses polarity due to the negative HF-link voltage is being used. At the end, the frequency spectra of the two PWM pulse trains are summed together to give the final one F_{NPWM}. The approach will be explained in the following paragraphs.

The double Fourier series of a two-level, double-sided PWM with every second pulse skipped and pulses only in the odd half-periods is developed in Appendix E.1.3 and is repeated here:

$$\begin{aligned} F_{NADD,1h}(t,\varphi) &= 4kM\cos(\omega_m t + \varphi) + \\ &+ 2\sum_{m=1}^{\infty}\left[\frac{2\cos(2\pi mk - \frac{\pi}{2})}{m\pi}J_0(2\pi mkM) + \frac{\cos(4\pi mk + \frac{\pi}{2})}{m\pi}\right]\cdot\cos(m\omega_{HF}t) + \\ &+ 4\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\infty}\frac{\cos(2\pi mk + \frac{(n-1)\pi}{2} - n\varphi)}{m\pi}\cdot J_n(2\pi mkM)\cos(m\omega_{HF}t + n\omega_m t + n\varphi) \end{aligned} \tag{7.7}$$

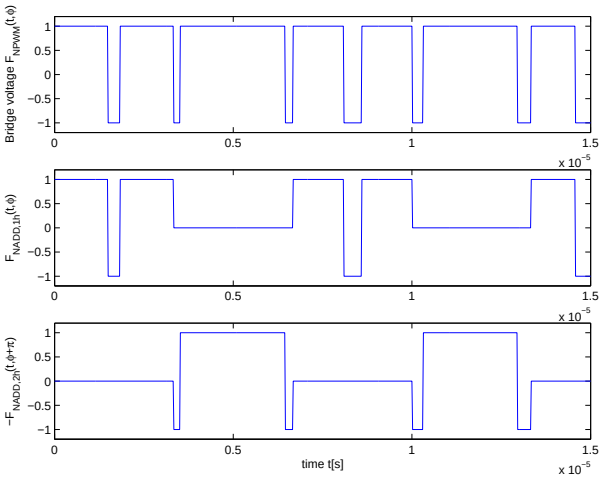

Fig. 7.7. The new PWM pulse train (top) and its two constitutive parts (below)

where ω_m and φ are the angular frequency and the phase of the modulating signal, ω_{HF} is the angular frequency of the triangular carrier and $k = T_{c2}/(4 \cdot T_{HF})$ is a ratio of the carrier and input stage switching period, equal to $k = 0.125$ for the case with two times higher carrier frequency then the input stage switching frequency.

The double Fourier series of a two-level, double-sided PWM with every second pulse skipped and pulses only in the even half-periods is developed in Appendix E.1.4 and is given by the following expression:

$$\begin{aligned} F_{NADD,2h}(t,\varphi) &= 4kM\cos(\omega_m t+\varphi)- \\ &-2\sum_{m=1}^{\infty}\left[\frac{2\cos(6\pi mk-\frac{\pi}{2})}{m\pi}J_0(2\pi mkM)+\right. \\ &\left.\frac{\cos(4\pi mk+\frac{\pi}{2})+\cos(8\pi mk+\frac{\pi}{2})}{m\pi}\right]\cdot\cos(m\omega_{HF}t)- \\ &-4\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\infty}\frac{\cos(6\pi mk+\frac{(n-1)\pi}{2}-n(\varphi+\pi))}{m\pi}\cdot J_n(2\pi mkM)\cos(m\omega_{HF}t+n\omega_m t+n\varphi) \end{aligned} \tag{7.8}$$

From Fig. 7.7 it can be noticed that the pulse train $F_{NADD,2h}$ can be obtained from $F_{NADD,1h}$ by simple pulse train shifting by $-0.5 \cdot (2\pi)/\omega_{HF}$, i.e.:

$$F_{NADD,2h}(t,\varphi) = F_{NADD,1h}(t-0.5\frac{2\pi}{\omega_{HF}},\varphi) \tag{7.9}$$

which can simplify calculation of the Fourier series of the resultant pulse trains.

The double Fourier series given in the equations (7.7) and (7.8) can be used as constitutive parts to calculate the double Fourier series of the conventional two-level double-sided PWM bridge voltage shown at the bottom diagram in Fig. 7.4, as follows:

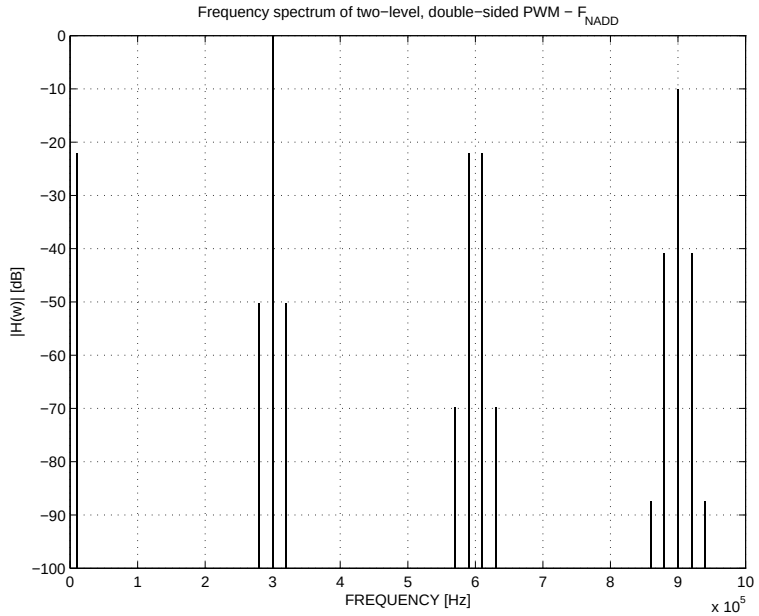

Fig. 7.8. Frequency spectrum of the conventional PWM method F_{NADD} with $M = 0.1$, $f_m = 10$ kHz, $f_{s1} = 150$ kHz, $f_{c2} = 300$ kHz

$$
\begin{aligned}
F_{NADD}(t,\varphi) &= F_{NADD,1h}(t,\varphi) + F_{NADD,2h}(t,\varphi) = 8kM\cos(\omega_m t+\varphi) - \\
&- 2\sum_{m=1}^{\infty}\left[\frac{4\sin(4\pi mk-\frac{\pi}{2})\sin(2\pi mk)}{m\pi}J_0(2\pi mkM)+\frac{\cos(8\pi mk+\frac{\pi}{2})}{m\pi}\right]\cdot\cos(m\omega_{HF}t) - \\
&- 8\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\infty}\frac{\sin(4\pi mk+\frac{(n-1)\pi}{2}-n(\varphi+\frac{\pi}{2}))}{m\pi}\cdot \\
&\quad\cdot\sin(2\pi mk+\frac{n\pi}{2})J_n(2\pi mkM)\cos(m\omega_{HF}t+n\omega_m t+n\varphi)
\end{aligned}
\tag{7.10}
$$

The magnitude diagram of the frequency spectrum of the conventional PWM bridge voltage F_{NADD} with modulation index equal to $M = 0.1$, modulation frequency $f_m = 10$ kHz, input stage switching frequency $f_{s1} = 150$ kHz and carrier frequency $f_{c2} = 300$ kHz is shown in Fig. 7.8.

For calculating the double Fourier series of the newly proposed PWM method for the SICAM bridge voltage F_{NPWM} shown at the bottom diagram in Fig. 7.5, previously developed equations (7.7) and (7.8) are summed in the following way:

$$
\begin{aligned}
F_{NPWM}(t,\varphi) &= F_{NADD,1h}(t,\varphi) - F_{NADD,2h}(t,\varphi+\pi) = 8kM\cos(\omega_m t+\varphi) + \\
&+ 2\sum_{m=1}^{\infty}\left[\frac{4\cos(4\pi mk-\frac{\pi}{2})\cos(2\pi mk)}{m\pi}J_0(2\pi mkM)+\right. \\
&\quad\left.+\frac{2\cos(4\pi mk+\frac{\pi}{2})+\cos(8\pi mk+\frac{\pi}{2})}{m\pi}\right]\cdot\cos(m\omega_{HF}t)+ \\
&+ 8\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\infty}\frac{\cos(4\pi mk+\frac{(n-1)\pi}{2}-n\varphi)}{m\pi}\cdot \\
&\quad\cdot\cos(2\pi mk)J_n(2\pi mkM)\cos(m\omega_{HF}t+n\omega_m t+n\varphi)
\end{aligned}
\tag{7.11}
$$

The magnitude diagram of the frequency spectrum of the new PWM bridge voltage F_{NPWM} with modulation index of $M = 0.1$, $f_m = 10$ kHz, $f_{s1} = 150$ kHz and $f_{c2} = 300$ kHz is shown in Fig. 7.9.

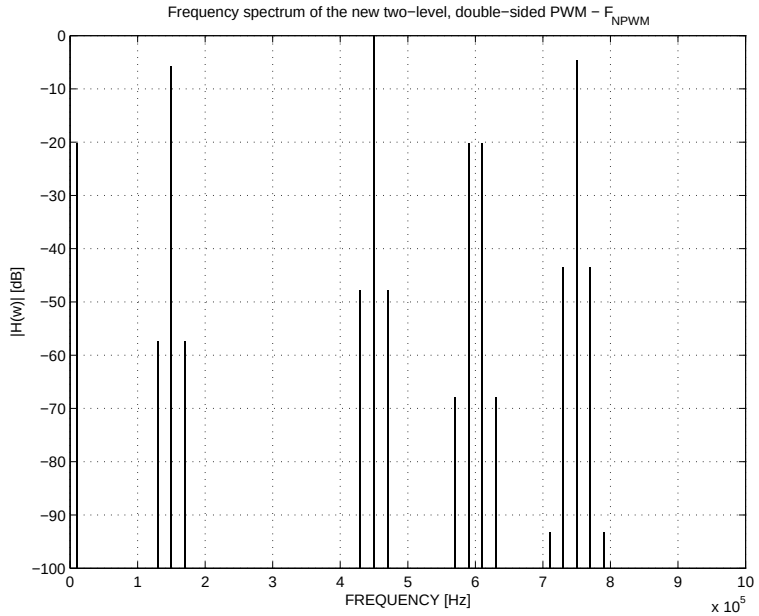

Fig. 7.9. Frequency spectrum of the new PWM method F_{NPWM} with $M = 0.1$, $f_m = 10$ kHz, $f_{s1} = 150$ kHz, $f_{c2} = 300$ kHz

It becomes apparent from Fig. 7.8 that the frequency spectrum of the conventional PWM method F_{NADD} in Fig. 7.4 comprises only of the modulating signal baseband, switching harmonics at multiples of the carrier frequency and their sidebands as intermodulation product of the modulation baseband with the switching harmonics, like suggested in the more compact form of F_{NADD} (5.5). As long as the PWM modulator triangular carrier frequency is substantially higher than the maximum modulating frequency $\omega_c \gg \omega_{m,max}$, there are no switching frequency sidebands interfering with the audio baseband, and the modulation process is essentially linear. The switching harmonics amplitudes at the loudspeaker are suppressed by the output low-pass filter attenuation at those specific frequencies.

On the other hand, by closely inspecting Fig. 7.9 one can notice that the frequency spectrum of the proposed PWM for SICAMs F_{NPWM} has intermodulation sidebands at the multiples of the input stage switching frequency i.e. HF-link frequency, which are not present in the conventional PWM F_{NADD}, while some of the harmonics and sidebands associated with the PWM modulator carrier frequency have disappeared. Since the frequency of the HF-link is usually selected lower than the carrier frequency, these components are likely to cause larger ripple voltage across the loudspeaker, since the low-pass output filter is less effective at the HF-link frequency. Fortunately, the magnitude of the first harmonic of the HF-link voltage at the loudspeaker terminal is lower than the third harmonic, which the output filter can attenuate more effectively. The magnitudes of the first 9 switching harmonics as function of the modulation index are given in Fig. 7.10.

7.2.3 Frequency spectrum of the new optimized PWM method in general case

The double Fourier series (7.7) of the two-level double-sided PWM signal in the beginning of the switching interval can be used to develop the double Fourier series of the new PWM with the desired even integer ratio r of the triangular carrier f_{c2} and the HF-link frequency f_{HF}, $f_{c2} = r \cdot f_{HF}$:

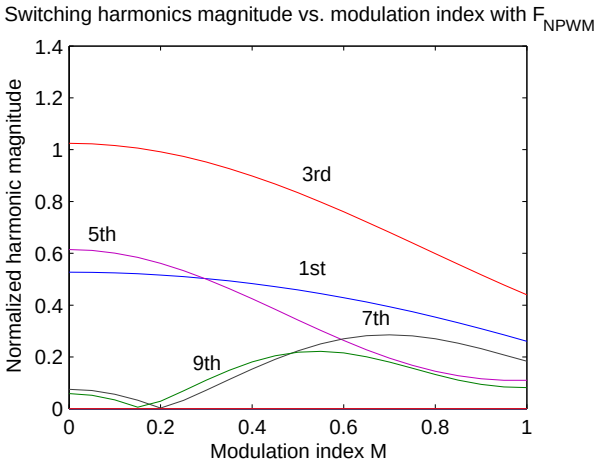

Fig. 7.10. Magnitudes of the switching harmonics in F_{NPWM} with varying modulation index

$$F_{NPWM}(t,\varphi) = \sum_{i=1}^{r/2} F_{NADD,1h}[t-(i-1)\frac{2\pi}{r\omega_{HF}},\varphi] - \sum_{i=r/2+1}^{r} F_{NADD,1h}[t-(i-1)\frac{2\pi}{r\omega_{HF}},-\varphi] \tag{7.12}$$

7.3 Self-oscillating modulators for isolated SICAMs - SOHF

7.3.1 Application and limitations

The most common modulator for direct conversion audio power amplifiers, i.e. SICAMs [3], [9], [53], [54], [85], has up till now been the PWM modulator with externally generated carrier. Reasons for this are mainly twofold and arise from the fact that self-oscillating modulators have variable switching frequency which decreases with increasing modulation index and the inability to predict and steer switching instants, due to the hysteretic-type control. On one hand, when using self-oscillating modulators in SICAMs with PWM modulated transformer voltages [3], variable switching frequency causes the transformer design to be suboptimal and its dimensions must be chosen to bare the largest magnetic flux at lowest switching frequency without going into saturation. On the other hand, when PWM modulation is used only on the secondary side of the transformer in conjunction with some safe-commutation principle in Section 6.2.1 and [85], random switching of the self-oscillating modulator makes it very difficult to synchronize the operation of the input stage to the output stage. However, this does not mean that self-oscillating modulators are completely useless in SICAMs, but rather that they are applicable just with certain SICAM topologies and usually with active [54] or dissipative clamps [9], or conditionally with safe-commutation strategies [85] as means for commutating the load current in the output bidirectional bridge.

In the next sections, the use of self-oscillating modulators will be analyzed with respect to SICAMs with non-modulated transformer voltages [85], [86], where the input inverter stage on the primary side of the transformer is operated with 50% duty cycle to create rectangular transformer voltage with maximum width. The operation of the input stage is not synchronized to any control signal from the secondary side, and therefore the operation of the input stage is referred as free-running. The proposed solution is named SOHF - Self-Oscilating High Frequency-link converters.

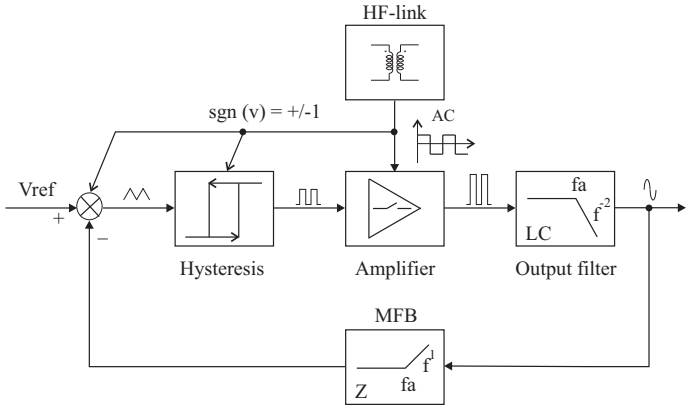

Fig. 7.11. GLIM SOHF

7.3.2 Operation fundamentals

Self-oscillating modulators can be roughly divided into two groups: current mode and voltage mode modulators [15]. There is not bigger difference in their principal operation, except that the measured inductor current in the former group is used directly in the modulator, while in the latter group the measured bridge voltage must be first integrated or processed in some way in the control section [87] or in both control section and power stage [88], [89].

One other possible division of self-oscillating modulators is according to the way self-sustained oscillation is created. In one group of self-oscillating modulators the limit cycling is created by hysteresis window [89], [90], [91], usually made from the amplifier output to improve the PSRR. In another group of self-oscillating modulators, the necessary loop gain of 0 dB at phase-shift of 180° at the switching frequency is created by active and passive phase-shift control with RC-networks in the feedforward and feedback path [88], [92].

The approach presented in the following few paragraphs can be used to modify particular self-oscillating modulator for SICAM operation in a straightforward manner. Without loss of generality, the discussion will deal just with the Global Loop Integrating Modulator (GLIM) [89], where the integrating transfer function from the bridge voltage to the input of the hysteresis block is obtained by combining the poles of the output filter in the power stage with the zero in the modulator feedback block (MFB) at the output filter cut-off frequency. The hysteresis block itself is created from the power stage bridge voltage using a resistive divider, as an input to the comparator.

In all self-oscillating modulators, the polarity of the bridge voltage which is being applied across the output filter and loudspeaker is determined solely by the state of the comparator i.e. the output from the hysteresis block, since the power supply voltage has constant polarity. In SICAMs, bridge voltage essentially represents a product of the HF-link voltage and the state of the comparator. Changing the HF-link polarity causes immediate change in the bridge voltage and hysteresis window polarity bound to it, which will surely bring the power stage into stall due to the ill-posed hysteresis limits. Therefore, any change in the HF-link voltage polarity must be followed by corresponding change in the direction of integration, which essentially means that the polarity of the feedforward and feedback signals entering the comparator must be reversed. The block diagram of the proposed GLIM self-oscillating SICAM is given in Fig. 7.11. For comparison purposes, diagrams of practical implementations of GLIM modulators for Class D audio power amplifier and SICAM are given in Fig. 7.12. The actual circuit schematic of a GLIM modulator for Class D audio power amplifier is depicted in Fig 7.13.

Since the operation of the proposed self-oscillating modulator for SICAMs seems to be determined by the quantities characteristic for the basic self-oscillating modulator intended for operation with Class D audio power amplifiers, quantities associated with the latter will be called basic quantities and will be given asterisk "*" as superscript. Notice that most of these quantities are severely affected and altered when the SICAM HF-link is included in the modulator.

The operation of the self-oscillating modulator for SICAMs depends on the modulation index M of the reference voltage signal at the input of the modulator. Let M^*_{lim} denote the modulation index limit at which the frequency of the basic self-oscillating modulator, equal to the output stage switching frequency f^*_{s2} is two times the switching frequency of the free-running input stage f_{s1}:

$$f^*_{s2}(M^*_{lim}) = 2 \cdot f_{s1} \tag{7.13}$$

For modulation indexes smaller than the modulation index limit $M < M^*_{lim}$ operation of the self-oscillating modulator is called normal operation and for $M \geq M^*_{lim}$ it is referred as locked operation. These notions will be explained in detail in the following sections.

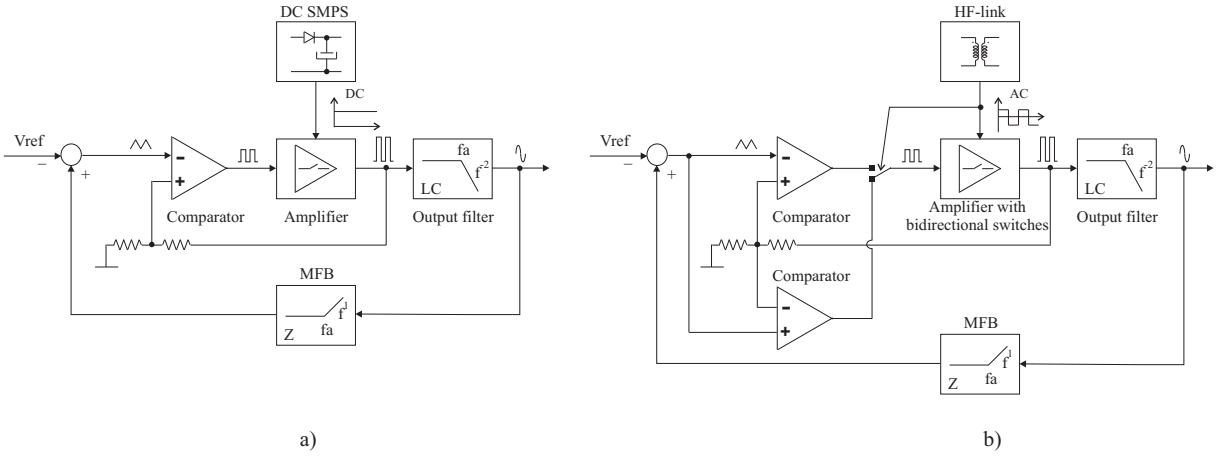

Fig. 7.12. Practical implementation of GLIM modulator for: a) Class D audio power amplifier and b) SOHF

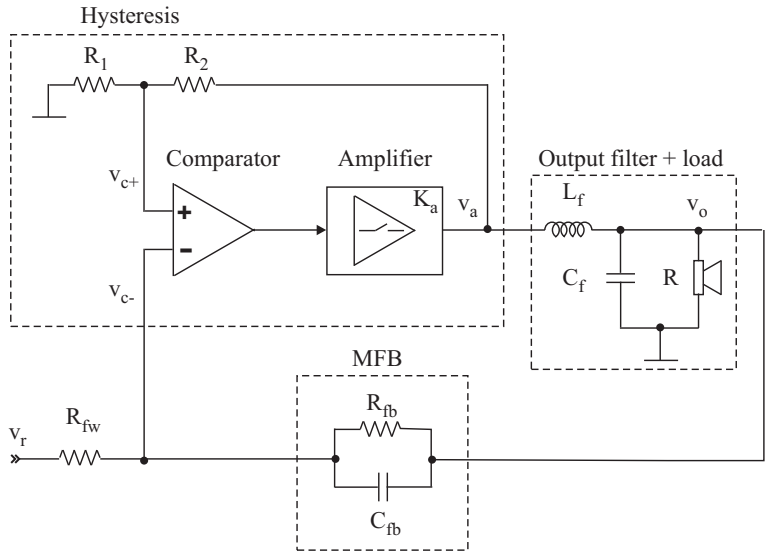

Fig. 7.13. Schematic of GLIM for Class D audio power amplifier

7.3.3 Normal operation with $M < M^*_{lim}$

Normal operation of the self-oscillating modulator in Fig. 7.11, which occurs for modulation indexes $M < M^*_{lim}$ is shown in Fig. 7.14. The operation is called normal since it resembles very much the operation of a conventional Class D audio power amplifier with self-oscillating modulator. With low modulation indexes $M < M^*_{lim}$, the slopes of both the rising portion and the falling portion of the carrier are steep and the output stage performs several switchings within each period of the HF-link voltage v_{HF}. The nature of the operation makes it very difficult to determine the exact switching frequency of the output stage, since it depends not only on the feedback quantities but also on the instants when HF-link changes its polarity. It can be, however, assumed that with sufficient level of accuracy the average switching frequency of the output stage f_{s2} is equal to the switching frequency of the basic self-oscillating modulator f^*_{s2}, developed in Appendix E.2:

$$f_{s2}(M) = f^*_{s2}(M) = \frac{V_s}{4}\frac{1-M^2}{\tau_{int}V_h + t_d V_s}\bigg|_{M<M^*_{lim}} \tag{7.14}$$

where $V_s = |v_{HF}|$ is the absolute value of the HF-link voltage, V_h is the hysteresis window width, t_d is the modulator loop delay and τ_{int} is the integrator time constant which is equal to the output filter cut-off frequency in the GLIM case. In all practical implementations, the hysteresis window is formed using the HF-link voltage:

$$V_h = k_h \cdot V_s \tag{7.15}$$

and MFB in Fig. 7.11 features attenuation equal to the gain of the SICAM amplifier k_a, leading to switching frequency of the output stage f_{s2} which is independent of the supply voltage V_s and significantly improving the PSRR:

$$f_{s2}(M) = f^*_{s2}(M) = \frac{1}{4}\frac{1-M^2}{\tau_{int}k_h k_a + t_d}\bigg|_{M<M^*_{lim}} \tag{7.16}$$

The idling switching frequency with $M = 0$ is:

$$f_{s2,0} = \frac{1}{4}\frac{1}{\tau_{int}k_h k_a + t_d} \tag{7.17}$$

Transition from normal to locked mode of operation happens when the modulation index M is equal to M^*_{lim}, which in the case of the GLIM modulator is obtained by combining equations (7.13) and (7.16) and becomes:

$$M^*_{lim} = \sqrt{1 - 8f_{s1}(\tau_{int}k_h k_a + t_d)} \tag{7.18}$$

7.3.4 Locked operation with $M \geq M^*_{lim}$

The real difference in the operation between the conventional self-oscillating modulator for Class D audio power amplifiers and the one for use with SICAMs is observed with modulation indexes larger than the modulation index limit $M \geq M^*_{lim}$. As shown in Fig. 7.15, the bridge voltage of the self-oscillating SICAMs with $M \geq M^*_{lim}$ turns into 2-level phase-shifted PWM with constant frequency two times the HF-link frequency:

$$f_{br} = 2 \cdot f_{s1} \tag{7.19}$$

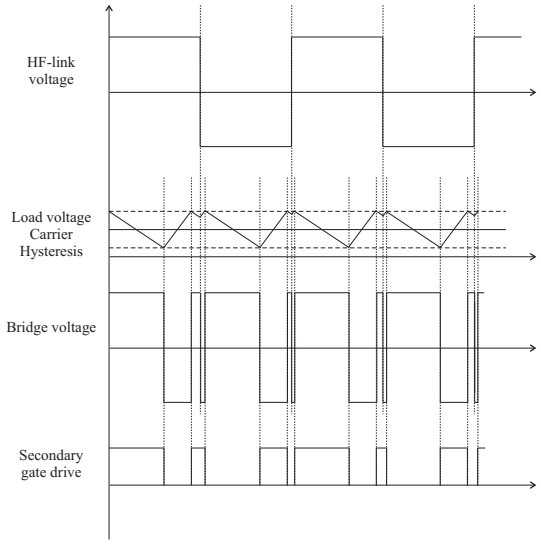

Fig. 7.14. Normal operation with $M < M^*_{lim}$

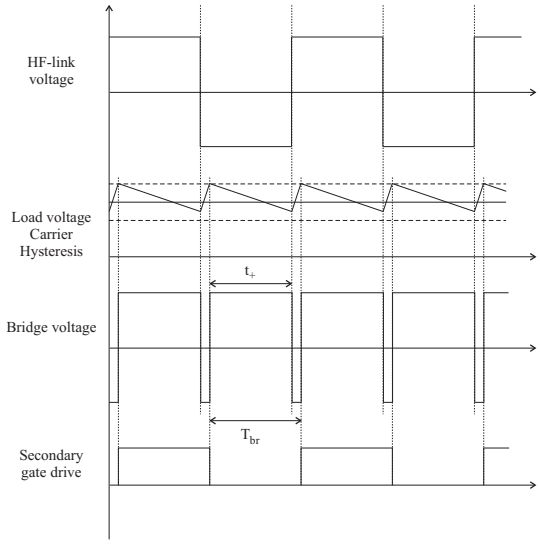

Fig. 7.15. Locked operation with $M \geq M^*_{lim}$

while the output stage switching frequency is exactly equal to the input stage switching frequency i.e. the HF-link frequency:

$$f_{s2}(M) = f_{s1}\Big|_{M \geq M^*_{lim}} \tag{7.20}$$

With the duty cycle D defined as ratio between the time interval with high voltage on the bridge output t_+ and its period T_{br}, equal to half the HF-link period:

$$D = \frac{t_+}{T_{br}} = 2t_+ f_{s1} \tag{7.21}$$

the SICAM output voltage is calculated to be:

$$v_o = DV_s - (1-D)V_s = (2D-1)V_s \tag{7.22}$$

and the duty cycle dependance on the modulation index:

$$D = \frac{1 \pm M}{2} \tag{7.23}$$

where "+" sign is used for positive and "-" sign is used for negative reference voltages v_{ref}.

As implied in equations (7.19) and (7.20), the frequency of quantities associated with the secondary stage becomes locked to the primary side and the HF-link, since the slope of either the rising portion or the falling portion of the carrier has reduced as a result of the large modulation index $M \geq M^*_{lim}$. In this situation, the regular changes in the HF-link polarity interrupt the slower slope of one of the carrier portions before it hits the other wall of the hysteresis block, causing a sort of carrier reset. The time interval between the phase-shifted waveforms created by the switching of the output stage and the subsequent switching of the HF-link is essentially equal to the time interval with positive bridge voltage t_+ and its dependance on the modulation index is:

$$t_+ = DT_{br} = \frac{1 \pm M}{4f_{s1}} \tag{7.24}$$

The phase locking property of the self-oscillating SICAM can be shown to be asymptotically stable. When disturbance voltage Δv is added to the carrier voltage, causing

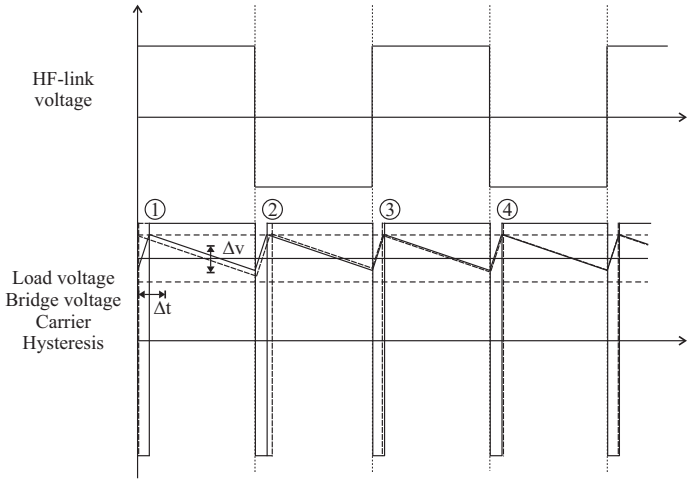

Fig. 7.16. Asymptotic stability of the locked operation

corresponding timing error Δt at the first switching of the output stage, like shown in Fig. 7.16, then the following equations for the subsequent errors are valid:

$$\begin{aligned}
\Delta t_1 &= \Delta t & \Delta v_1 &= \Delta v \\
\Delta t_2 &= \left(\tfrac{1-M}{1+M}\right)\Delta t & \Delta v_2 &= \left(\tfrac{1-M}{1+M}\right)\Delta v \\
\Delta t_3 &= \left(\tfrac{1-M}{1+M}\right)^2\Delta t & \Delta v_3 &= \left(\tfrac{1-M}{1+M}\right)^2\Delta v \\
&\ldots & &\ldots \\
\Delta t_{n+1} &= \left(\tfrac{1-M}{1+M}\right)^n\Delta t & \Delta v_{n+1} &= \left(\tfrac{1-M}{1+M}\right)^n\Delta v
\end{aligned} \tag{7.25}$$

Because of the fact that:

$$\frac{1-M}{1+M} < 1 \tag{7.26}$$

the asymptotic stability of the timing interval t_+ for the phase-shifted PWM is proven:

$$\begin{aligned}
\Delta t_{n+1} &= \left(\tfrac{1-M}{1+M}\right)^n\Delta t \overset{n\to\infty}{\longrightarrow} 0 \\
\Delta v_{n+1} &= \left(\tfrac{1-M}{1+M}\right)^n\Delta v \overset{n\to\infty}{\longrightarrow} 0
\end{aligned} \tag{7.27}$$

With maximum modulation index M_{max}=1, the time interval t_+ of the phase shifted PWM approaches T_{br} and 0 with positive and negative voltages respectively, which means that at one instant close to the maximum modulation the switching of the input and output stage will start to overlap and the resultant bridge voltage will have switching frequency equal to the HF-link voltage $f_{br} = f_{s1} = f_{s2}$.

It is interesting to notice that, if the self-oscillating modulator is designed to have basic idling switching frequency lower than two times the HF-link frequency $f^*_{s2,0} < 2 \cdot f_{HF}$, i.e. $M^*_{lim} \equiv 0$, then the corresponding self-oscillating SICAM will be in locked operation all the time. Even more, if the maximum modulation index is limited to value less than unity $M_{max} < 1$, then the switching of both stages is not simultaneous. This means that many other SICAM topologies which utilize safe-commutation strategies, presented in Section 6.2.1 and in [53], [85] can be used in conjunction with the proposed self-oscillating modulator because of the natural synchronization between the stages during locked operation. This saves some power components on behalf of slightly more complex control circuitry for implementing the safe-commutation switching sequence.

7.3.5 Output stage switching frequency

To summarize, the switching frequency of the output stage f_{s2} in the self-oscillating SICAM differs when operating in normal or locked mode and can be described with the following equation:

$$f_{s2} = \begin{cases} \dfrac{1}{4}\dfrac{1-M^2}{\tau_{int} k_h k_a + t_d} & , M < M^*_{lim} \\ f_{s1} & , M \geq M^*_{lim} \end{cases} \tag{7.28}$$

and represents a discontinuous function, shown in Fig. 7.17. The same figure shows the transferred charge to the clamp and its power in the case of a SICAM with active capacitive voltage clamp from Section 6.2.3, operated with the modified GLIM self-oscillating modulator for SICAMs.

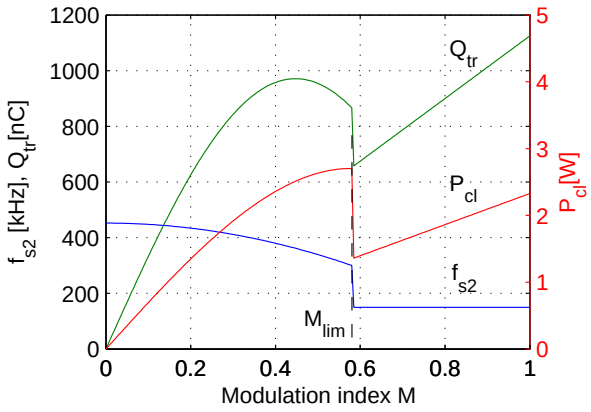

Fig. 7.17. Output stage switching frequency, transferred charge and clamp power (in SICAMs with load voltage clamp)

7.3.6 Audio distortion of self-oscillating SICAM

THD of SICAMs depends predominantly on the used topology and it was already calculated for the two most common SICAM output stages using safe-commutation switching sequence and active capacitive voltage clamp in Sections 6.2.3 and 6.2.1, correspondingly. However, in both cases the switching frequency of the output stage was selected as constant, like using some of the aforementioned synchronized or unsynchronized PWM methods from the previous sections.

THD of the SICAM with active capacitive voltage clamp with self-oscillating GLIM modulator, operating in open loop control with modulation signal of $f_m = 1$ kHz is shown in Fig. 7.18. In the simulation secondary-side voltage is $V_s = 59$ V, clamp voltage is $V_{cl} = 65$ V, maximum modulation index is $M_{max} = 0.8$, modulator loop delay is $t_d = 150$ ns, blanking time is $t_{bl} = 75$ s, modulator window is $k_h = 1/151$ and amplifier gain is $k_a = 20$. THD gradually decreases with higher modulation indexes as the result of the falling switching frequency and the increased switching period T_{s2}, while the blanking time t_{bl} stays essentially the same.

7.4 Closed-loop control schemes

As shown in the previous sections, in every switching-mode audio power amplifier noticeable distortion within the audio band is introduced as a result of the nonlinearities in the

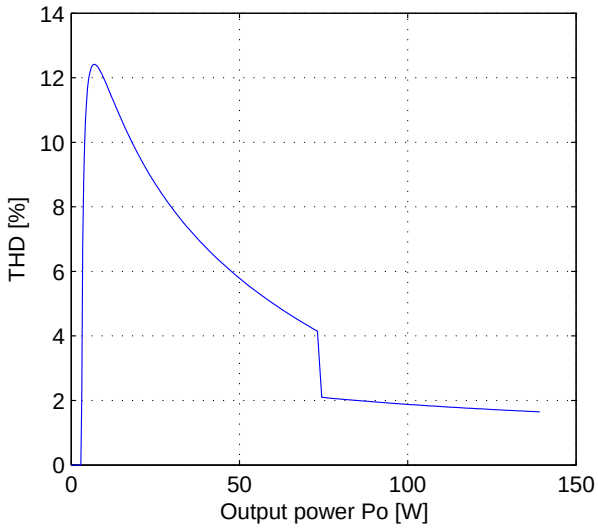

Fig. 7.18. THD of SICAM with active capacitive voltage clamp

power stage. Therefore, various kinds of closed loop control are utilized to diminish the effects of power supply variations, noise and error sources, parameter variations, as well as to decrease the amplifier output impedance. In control systems with negative feedback all the aforementioned negative effects are decreased by the amount of gain in the open loop transfer function L [60]:

$$v_o = \frac{L}{1+L}\frac{1}{H_v}v_{ref} + \frac{G_{vg}}{1+L}v_g - \frac{Z_o}{1+L}i_o \tag{7.29}$$

where v_o is the output voltage, v_{ref} is the reference voltage, v_g is the amplifier input voltage, i_o is the load current, H_v is the voltage feedback coefficient, G_{vg} is the transfer function from the input voltage v_g to the output voltage v_o and Z_o is the amplifier output impedance.

The demand for high open loop gain within the audio bandwidth, known also as power bandwidth, coincides with the demand for having much higher control bandwidth f_c, defined as a frequency at which the open loop transfer function L has a gain of one. This is however not easy to achieve because of the 180° phase shift introduced by the output filter, that spoils the phase margin and threatens stability.

The selection of control approach usually represents a trade-off between simplicity and performance. The block diagram of simple output voltage control through single closed feedback loop is presented in Fig. 7.19. The presence of the output filter double poles makes it very difficult to achieve simultaneously proper phase margin and high control bandwidth i.e. the loop gain within the desired power bandwidth must be kept to reasonable values for robust and reliable operation.

Other options are also possible, like cascade control with fast inner current loop and slower outer voltage loop. The inner current loop can be based on the real load current measurement or load current estimator, like shown in Fig. 7.20, with the parameters explained in Table 7.1. What the inner current loop effectively does is that it eliminates the pole associated with the output filter inductor from the open loop transfer function up to the bandwidth of the inner current loop, thus making it much easier to close the outer voltage feedback loop and provide sufficient gain through integrating action. Since the simplicity of the solution is of utmost interest, complex, expensive and dissipative inductor current sensing through current sense resistors can be replaced with simple inductor current estimator.

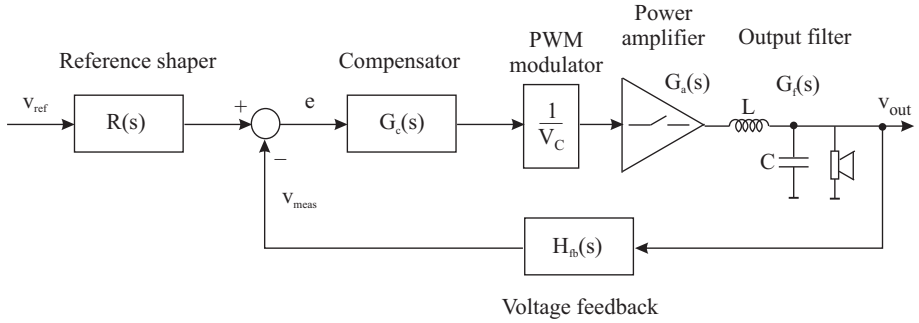

Fig. 7.19. Block diagram of simple output voltage control

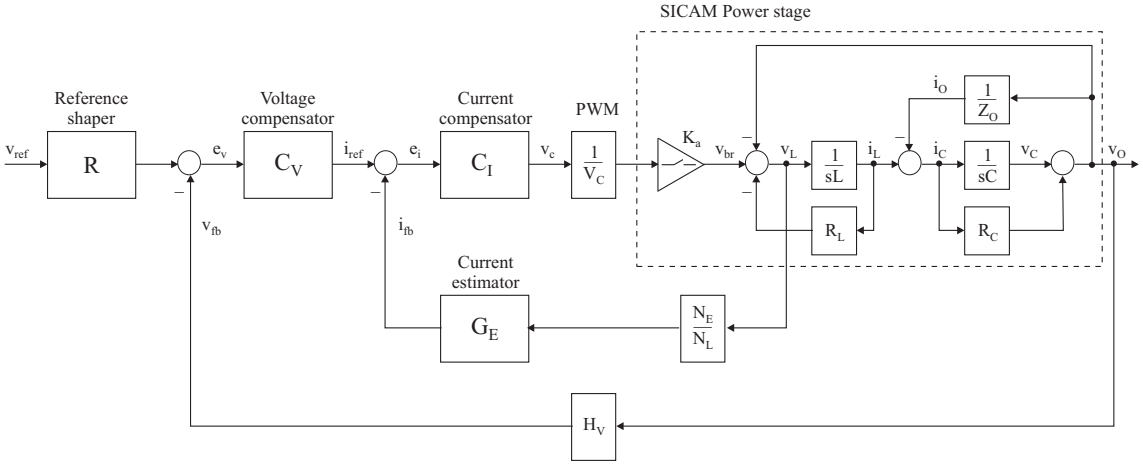

Fig. 7.20. Control block diagram of cascade control

Inductor current estimator is built with additional winding put on the inductor core and sensing the inductor voltage v_L, which bears information about the inductor current i_L:

$$i_L = \frac{1}{L}\int_0^t v_L(\tau)d\tau \tag{7.30}$$

Unfortunately, due to the voltage offsets of the common operational amplifiers it is impossible to build an ideal integrator, which will not saturate when put in a real noisy circuit. In order to alleviate these problems, integrator is replaced with a low pass filter, which has a finite gain at DC and therefore does not saturate, except maybe for some DC offset in the output voltage. The transfer function of the inductor current estimator is:

$$G_{i,est} = \frac{N_e}{N_L}\frac{k_{i,est}}{1 + s\tau_{i,est}} \tag{7.31}$$

Selection of estimator bandwidth is trade-off between the size of the low pass filter and cut-off frequency of the output filter. If the main purpose of closing the inner feedback loop is to dampen the resonance of the output filter by removing the pole associated with the inductor to higher frequencies, then this can be achieved with inductor current estimator which does not reproduce the low frequency content of the inductor current very well, but still captures the high frequency content around the filter resonance very accurately.

7.5 Conclusion

This chapter presented several open-loop and closed-loop control methods for achieving reliable and safe operation of different SICAM topologies presented in the previous chap-

Table 7.1. Explanation of the parameters in Fig. 7.20

Parameter	Description	Comment
R	Reference shaper	Limits the bandwidth of the input signal
C_V	Voltage compensator	With its PI-element characteristics reduces the errors in the outer loop
C_I	Current compensator	With its PI-element characteristics reduces the errors in the inner loop
V_C	Carrier amplitude	External triangular carrier generator with fixed frequency is used
K_a	Amplifier gain	Proportional to the secondary-side voltage
L, C	Output filter components	The output filter has low-pass filter characteristics
R_L, R_C	Output filter parasitics	Resistance of the inductor wire and ESR of the capacitor
Z_o	Amplifier output impedance	At higher frequencies is dominated by the output filter inductor
N_L, N_E	Number of turns on the inductor	The inductor has one operational and one estimator winding
G_E	Current estimator transfer function	Integrates or low-pass filters the inductor voltage
H_v	Voltage feedback coefficient	Reciprocal of the closed-loop system gain

ter. It was emphasized that although unsynchronized control methods give some extra flexibility in selecting independently the switching frequencies of the input and the output stage, they give rise to intermodulation harmonics in the audio band and therefore result in lower performance. At the same time, optimized PWM control methods with synchronization can provide lower switching frequency of the output stage and therefore lower switching losses, as well as the required non-simultaneous switching of the stages for safe commutation of the load current in the output stage.

SICAMs can be also controlled by self-oscillating modulators commonly found in Class D audio power amplifiers, by doing some simple modifications in their structure to account for the alternating polarity of the HF-link voltage. Thus, the radically new and compact way of building isolated audio power amplifiers through HF-link converters is combined with the state-of-the-art self-oscillating modulators for Class D audio power amplifiers to create high-performance audio power amplifiers with smaller form factors.

At the end, several simple closed-loop control methods suitable for SICAMs are presented, capable of suppressing the adverse effects of variable HF-link voltage and nonidealities of the power stage, rejecting undesired perturbances in the output voltage as well as reducing the output impedance.

8

Prototypes of isolated SICAMs with non-modulated transformer voltages

"I hope that posterity will judge me kindly, not only as to the things which I have explained, but also to those which I have intentionally omitted so as to leave to others the pleasure of discovery. "

- René Descartes

In this chapter, several prototypes of isolated SICAMs with non-modulated transformer voltages will be presented. They will represent a mixture of different SICAM topologies from Chapter 6 and different control principles from Chapter 7.

8.1 Isolated SICAM with master/slave operation for achieving safe commutation

One of the first prototypes in the project was the 100 W @ 8 Ω isolated SICAM with master/slave operation to enable reliable safe commutation of the output stage, shown in Fig. 8.1. Its circuit schematics can be found in Appendix F.1. The output stage has a full-bridge configuration and consists of bidirectional switches as antiparallel connection of two voltage 2QSW, as depicted in Fig. 6.12. The implemented voltage-controlled safe-commutation switching sequence is given in Table 6.2 and was implemented with simple digital logic, where all commutation delays were implemented as resistor-capacitor-diode (RCD) combinations. Therefore the implementation of the safe-commutation switching sequence was not flexible and changing the commutation delays required substantial re-work. The primary switching frequency was selected to be $f_{s1} = 100$ kHz to optimize the transformer weight vs. losses, while the secondary-side PWM triangular carrier was chosen to be $f_{c2} = 200$ kHz. The implemented PWM has simple structure described in Section 7.1.1. No frequency locking and synchronization between the input and the output stage existed, thus substantial amount of intermodulation harmonics within the audio band could be expected due to slight variations in the switching frequency of the stages.

Detailed operation of the master/slave SICAM is shown in Fig. 8.2. Both stages share a common M/S digital line, which represents enabling signal for the latches corresponding to the gate drivers of the switches in the input and the output stage. In this way, whenever one of the stages pulls the M/S line low and performs transition, the other stage cannot switch due to lack of enabling signal. Each switching of the input stage causes reversal of the HF-link voltage polarity and thus immediate switching of the output stage, since the operation of the PWM modulator is not optimized. These two events are clearly visible in traces 1 and 2 in Fig. 8.2.

The driving signals for the MOSFETs 1&6, 2&5, 3&8 and 4&7 in the output stage shown in Fig. 6.12 are given in Fig. 8.3. This transition occurs due to change of the HF-link voltage polarity from positive to negative (upper rail negative), according to Table 6.2 and starting from 1,6&3,8 turned on.

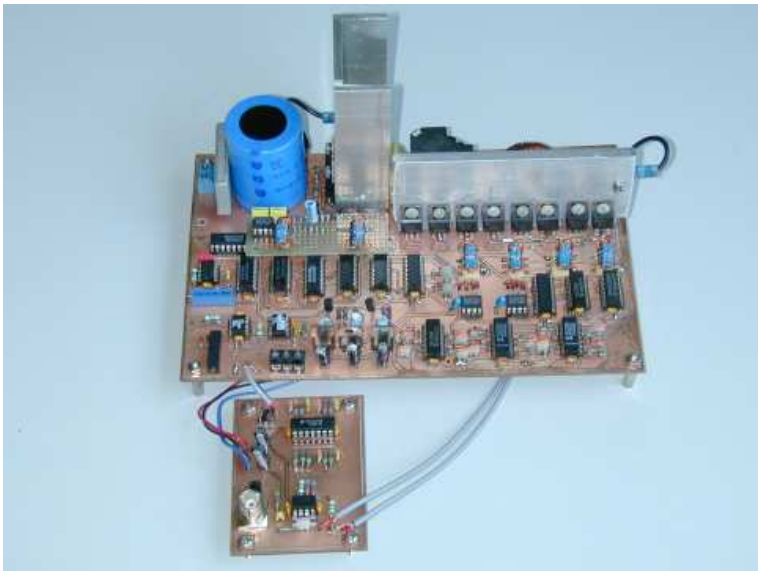

Fig. 8.1. Photograph of the prototype master/slave-operated SICAM

Fig. 8.4 depicts open-loop operation of the M/S SICAM, while Fig. 8.5, Fig. 8.6 and Fig. 8.7 show the closed-loop operation with different output power levels. The FFT of the output voltage is given on the same diagrams. Looking at the waveforms of output voltage and its FFT at different power levels, it is clearly visible that there is significant amount of distortion. This is likely due to many different issues, like noise problems, relatively low ratio of switching frequency to modulating frequency, PWM modulator nonlinearity and distorted triangular carrier in closed loop operation by fedback switching noise. No further measurements were made for audio performance and conversion efficiency.

8.2 Isolated SICAM with simple PWM modulator and active capacitive load voltage clamp

In order to test the feasibility of the proposed approach, a 100 W prototype of the isolated SICAM with active capacitive voltage clamp was constructed, as shown in Fig. 8.8. Its circuit schematics can be found in Appendix F.2. The primary switching frequency was selected to be $f_{s1} = 100$ kHz to optimize the transformer weight vs. losses, while the secondary-side PWM triangular carrier was chosen to be $f_{c2} = 225$ kHz, in order to avoid having too many primary-secondary intermodulation harmonics within the audio range. Independent primary and secondary switching frequencies lead to simpler design with much easier start-up circuitry and possibility to optimize the losses and dimensions of both the input stage and the transformer, but from purely audio perspective frequency locking and synchronizing the operation of the input and the output stage is necessary to improve the audio performance by avoiding intermodulation cross-products.

Operation of the SICAM with active capacitive voltage clamp with more and less detail is shown in Fig. 8.9 and Fig. 8.10 respectively. Notice that the HF-link voltage has rectangular waveform with duty cycle of 50%, while the bridge voltage applied across the combination of the output filter and loudspeaker is chopped from the HF-link voltage in a PWM manner.

The THD+N vs. frequency measurement in Fig. 8.11, THD+N vs. power measurement in Fig. 8.12, intermodulation distortion in Fig. 8.13 and FFT measurement in Fig. 8.14 show the promising audio performance of the prototype.

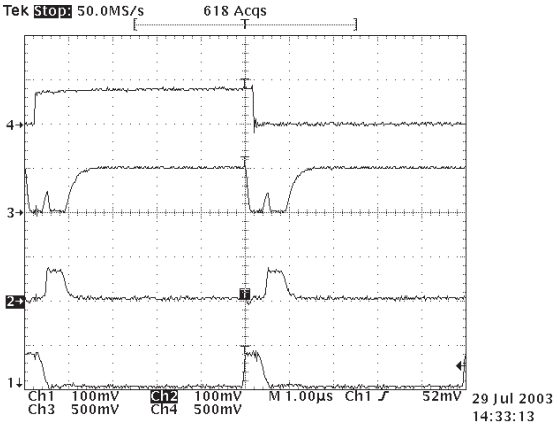

Fig. 8.2. Detailed master/slave SICAM operation: 1) Input stage M/S line driver base voltage, 2) output stage M/S line driver base voltage, 3) M/S line voltage, and 4) input stage voltage polarity (T_1/T_4 driving signal) (all probes 10x)

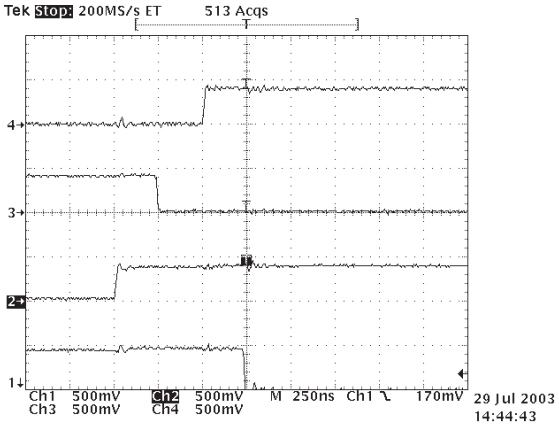

Fig. 8.3. Safe-commutation switching sequence: 1) MOSFETs 1&6 driving signal, 2) MOSFETs 2&5 driving signal, 3) MOSFETs 3&8 driving signal, and 4) MOSFETs 4&7 driving signal for negative rail voltage (all probes 10x)

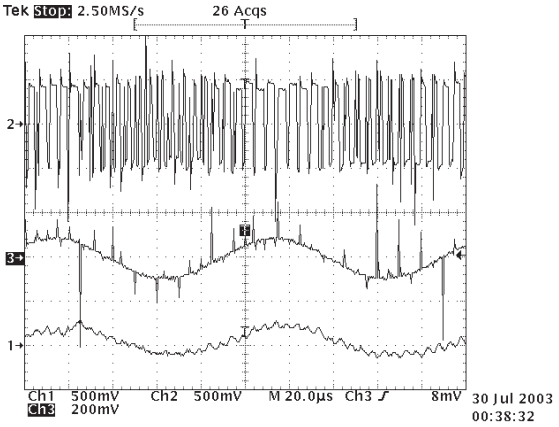

Fig. 8.4. Open-loop operation with 10 kHz reference: 1) load voltage, 2) bridge voltage, and 3) reference signal (probes 1 and 2 - 50x, 3 - 10x)

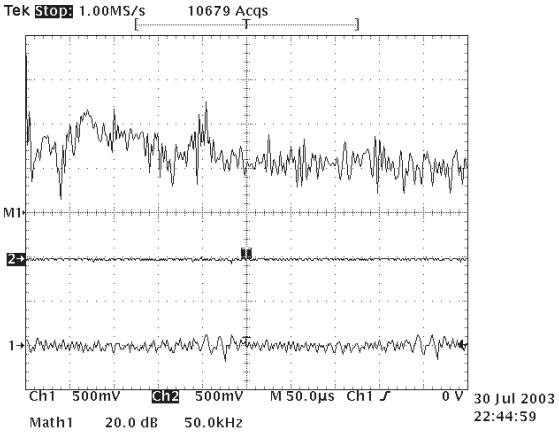

Fig. 8.5. Closed loop operation at P_{out}=0 W with 10 kHz reference: 1) load voltage, 2) reference signal, and M1) FFT (probe 1 - 50x, probe 2 - 10x)

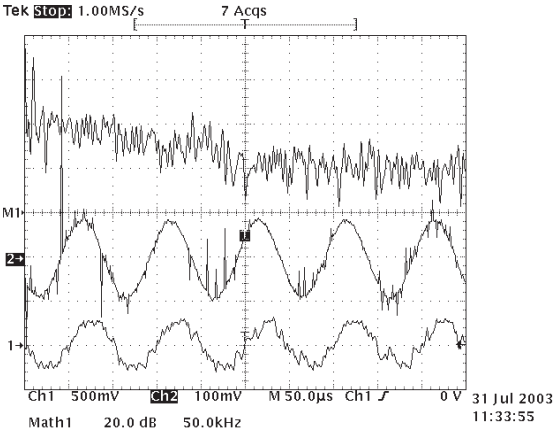

Fig. 8.6. Closed loop operation at P_{out}=1 W with 10 kHz reference: 1) load voltage, 2) reference signal, and M1) FFT (probe 1 - 50x, probe 2 - 10x)

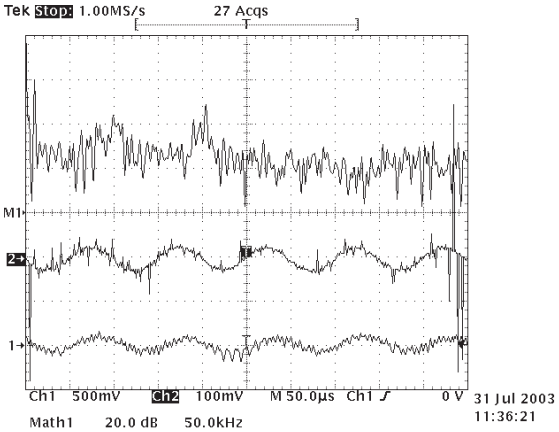

Fig. 8.7. Closed loop operation at P_{out}=10 W with 10 kHz reference: 1) load voltage, 2) reference signal, and M1) FFT (probe 1 - 50x, probe 2 - 10x)

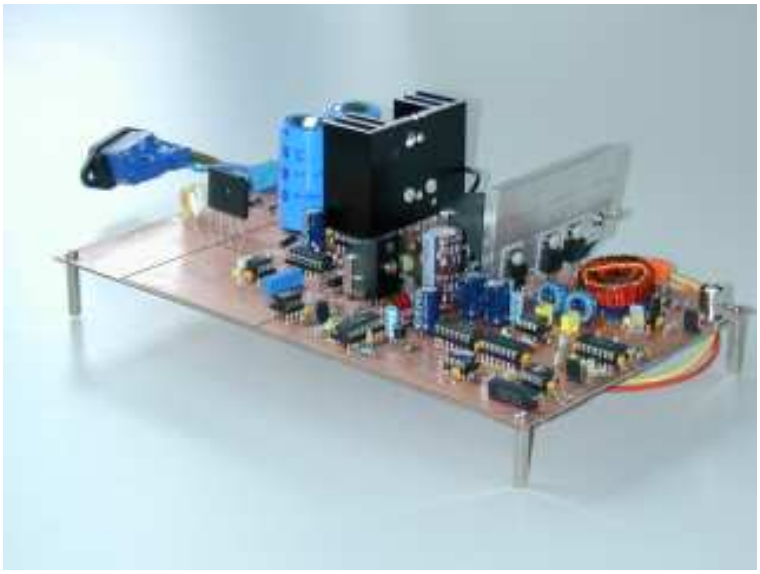

Fig. 8.8. Photograph of the prototype SICAM with active capacitive voltage clamp

The distribution of power losses in the prototype SICAM components and stages and its efficiency are calculated based on the theory presented in Section 6.4 and are presented in Fig. 8.15 and Fig. 8.16. Measured efficiency of the prototype is given in Fig. 8.17. The theoretical efficiency curve in Fig. 8.16 does not account for the power losses in the auxiliary power supplies and the control biasing i.e. the idling losses are not included. This explains the difference in the theoretically calculated efficiency and the measured, together with some neglected loss contributors.

8.3 Isolated SICAM with optimized PWM modulator and safe-commutation switching sequence

To test the SICAM approach with the proposed safe-commutation strategy and the new PWM method, a 100 W @ 8 Ω laboratory prototype according to Fig. 6.13 was built and measured. Its circuit schematics can be found in Appendix F.3. The final primary switching frequency was selected to be $f_{s1} = 150$ kHz and the secondary switching frequency is two times higher i.e. $f_{s2} = 300$ kHz. Some of the first measurements were made with primary switching frequency of $f_{s1} = 100$ kHz and the secondary switching frequency of $f_{s2} = 200$ kHz. The safe-commutation switching sequence in Table 6.3 is programmed into a programmable logic device (PLD), together with the part of the PWM modulator which selects the correct PWM sequence according to the polarity of the HF-link and the input stage switching frequency prescaler. The safe-commutation state machine in Fig. 6.15 is implemented as synchronous with the clock at frequency of $f_{clk} = 20$ MHz, so the commutation delay is $\Delta t_d = 50$ ns. Both the synchronization signal between the stages and the gate signals to the bidirectional switches are transferred using fast optocouplers. The main transformer is used for both energy transfer to the output stage as well as deriving control power supplies and isolated gate drive supplies on the secondary side. Sensing the inductor voltage for the current estimator is done with additional isolated winding on the inductor core, thus very effectively avoiding the problems with signal referencing and conditioning. The prototype is shown in Fig. 8.18.

Fig. 8.19 and Fig. 8.20 show the safe-commutation switching sequence from Table 6.3 into action with more and less detail. Commutation delay is set here to $\Delta t_d = 100$ ns to clearly separate each switching transition in the figure.

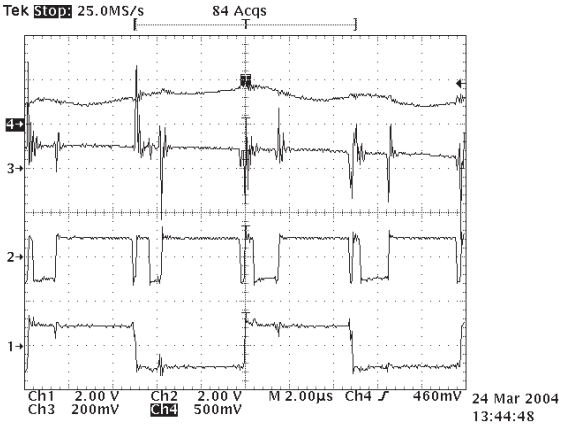

Fig. 8.9. Detailed SICAM operation: 1) HF-link voltage (100V/div), 2) bridge voltage (100V/div), 3) voltage reference (2V/div), 4) output voltage (5V/div) with 10 kHz reference

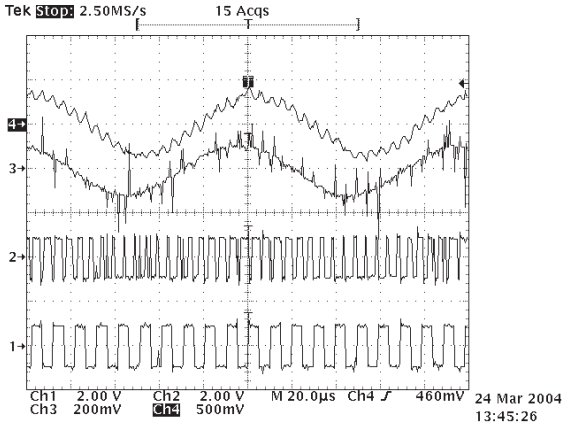

Fig. 8.10. SICAM operation: 1) HF-link voltage (100V/div), 2) bridge voltage (100V/div), 3) voltage reference (2V/div), 4) output voltage (5V/div) with 10 kHz reference

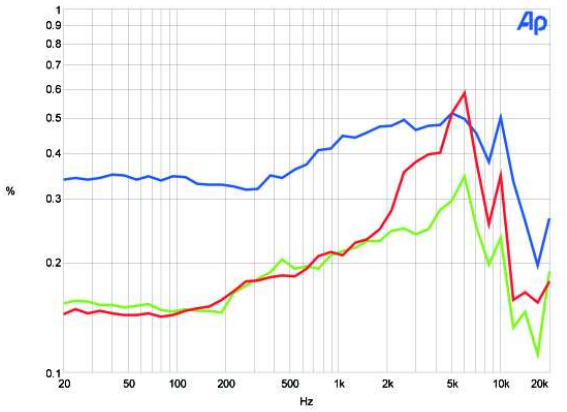

Fig. 8.11. THD+N versus frequency (BW=22kHz and AES17 filter): top - 10 W, bottom - 50 W, middle - 75 W

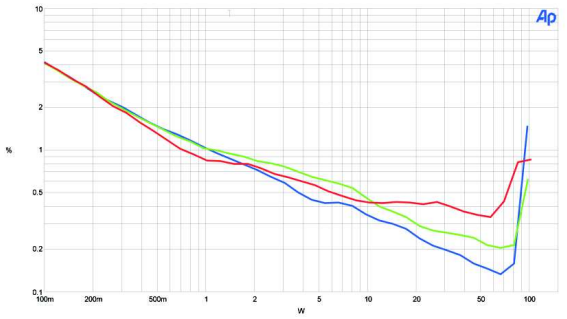

Fig. 8.12. THD+N versus power (BW=22kHz and AES17 filter): bottom - 100 Hz, middle - 1 kHz, top - 6.67 kHz

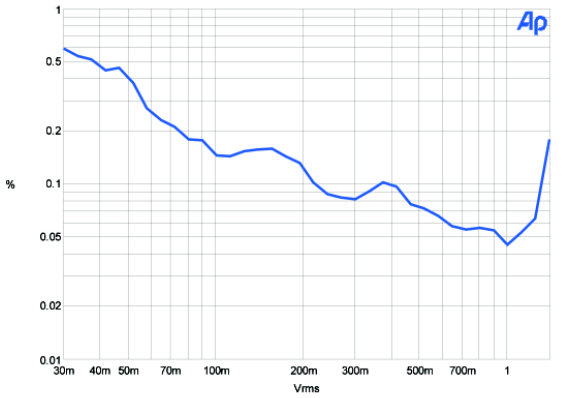

Fig. 8.13. Intermodulation distortion

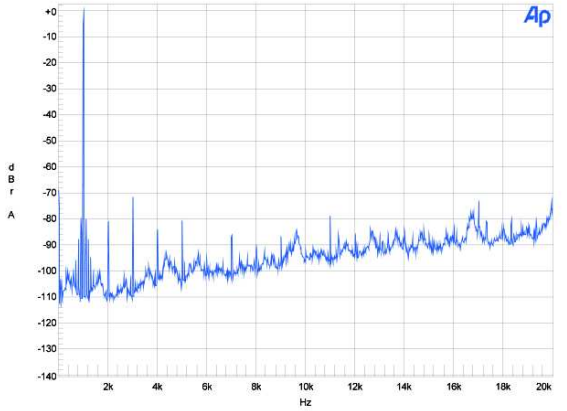

Fig. 8.14. FFT at 50 W with a signal of 1 kHz

The selection of different PWM modulators according to the polarity of the HF-link voltage, as described in Section 7.2.2 is depicted in Fig. 8.21. This multiplexing of the PWM modulator outputs can be also observed in Fig. 8.22, together with the synchronization of the HF-link voltage changes with the valleys of the triangular carrier.

All previous measurements were made with switching frequency of 100 kHz for the input stage and 200 kHz for the output stage.

The SICAM waveforms with reference voltage of 1 kHz at P_o=25 W with more and less detail are shown in Fig. 8.23 and Fig. 8.24 respectively.

The total harmonic distortion plus noise (THD+N) measurement of the SICAM vs. frequency for output power of 10 W and 40 W is given in Fig. 8.25.

The THD+N vs. power measurement of the SICAM at 100 Hz, 1 kHz and 6.67 kHz is given in Fig. 8.26.

Finally, the intermodulation distortion of the SICAM is given in Fig. 8.27.

The FFT of the output voltage at output power of P_o=25 W, with a reference set to 100 W is given in Fig. 8.28.

The distribution of power losses in the components and stages of the prototype SICAM and its efficiency are calculated based on the theory presented in Section 6.4 and are shown in Fig. 8.29 and Fig. 8.30. It can be seen that, at least theoretically, the efficiency at full power is supposed to be higher than the targeted one, but the theoretical calculations do not take into consideration the power losses in the auxiliary power supplies and the control biasing i.e. the idling losses. The measured efficiency of the prototype is given in Fig. 8.31 and is significantly lower than the calculated efficiency in Fig. 8.30, which is likely due to some neglected loss contributors, parasitic ringing/oscillations and possible shoot-through conditions.

All presented results show that the proposed SICAM approach is capable of reproducing audio with a sufficient level of fidelity, which makes it an attractive solution for the lower end of the market. The efficiency is somewhat lower than expected, but this is likely to be improved in future.

8.4 Isolated self-oscillating SICAM with GLIM modulator

The 100 W @ 8 Ω laboratory prototype of isolated self-oscillating SICAM with GLIM modulator according to Fig. 7.12b was built to tryout the proposed self-oscillating modulators for SICAMs in Section 7.3. Its circuit schematics can be found in Appendix F.4. The switching frequency of the free-running input stage was selected to be $f_{s1} = 150$ kHz. Multiplexing the outputs of the two comparators for positive and negative HF-link voltages is implemented in the digital logic of the PLD. The latter also houses the safe-commutation switching sequence from Table 6.3 in locked operation mode and the blanking time generation for the output stage when active clamp is used in combined normal and locked operation mode. The safe-commutation state machine on Fig. 6.15 is implemented as synchronous with the clock at frequency of $f_{clk} = 20$ MHz, so either the commutation delay or the blanking time is equal to 50 ns. All measurements in this section were made in combined normal and locked operation mode with the usage of the active clamp. Clamp voltage is set to $V_{cl} = 65$ VS. The prototype is shown in Fig. 8.32.

The detailed self-oscillating SICAM waveforms with 0 V and 10 V output voltage are shown in Fig. 8.33 and Fig. 8.33. The ringing in the bridge voltage due to the switch parasitics and nonzero output impedance of the input stage, as well as its clamping to the voltage of the clamp capacitor are clearly visible.

The operation of the self-oscillating SICAM with sinusoidal references of 1 kHz and 10 kHz are shown on a larger time scale in Fig. 8.35, Fig. 8.36 and Fig. 8.37. The output voltage is inverted due to the specific GLIM design and the reduced number of used operational amplifiers. Again the clamping action of the active clamp is clearly visible.

The total harmonic distortion plus noise (THD+N) measurement of the SICAM vs. frequency for output power of 6 W is given in Fig. 8.38. No further audio and efficiency measurements were performed.

In conclusion, the audio performance of the prototype is low and total harmonic distortion and noise is excessive. However this is characteristic of the test prototype itself and is likely due to unresolved noise issues, so it is by no means a general conclusion. The presented waveforms show the viability of the self-oscillating approach for SICAMs.

8.5 Conclusion

The prototypes presented in this chapter combined the load current commutation techniques presented in Chapter 6 with some of the control methods described in Chapter 7. The design process for these SICAM prototypes turned to be an involved task, since behind the simple and low component count power topologies shown on the previous figures lie hidden plenty of construction details. The resulting prototypes were functional and operated as expected, as shown in the numerous oscillograms.

The measured audio performance and efficiency of the prototypes were found to be less than the targeted ones in the project description. Somewhat lower efficiency of the SICAM approach can be explained with the increased component voltage and current stress of the proposed single-stage audio amplification topologies. This problem seems to be very similar to the lower efficiency of single-stage PFC rectifiers when compared to their two-stage counterparts. It is believed, however, that the measured results are prototype specific and can be by all means improved in future with more careful design and selection of better components. Introduction of soft-switching techniques (ZVS and ZCS) through alternative input stage topologies like those reviewed in the beginning sections of Chapter 6 and using switch snubbers and clamps can give those extra efficiency points needed to make SICAM even more attractive.

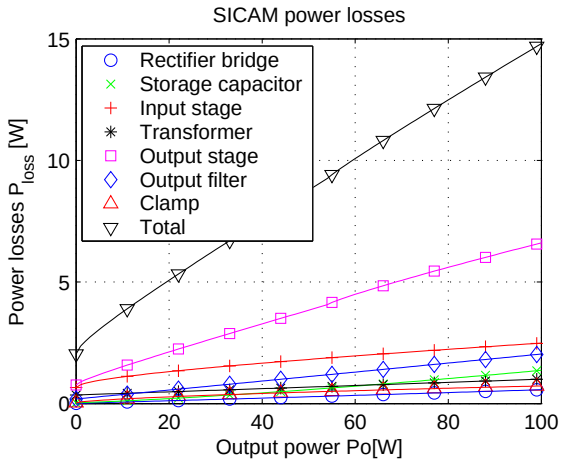

Fig. 8.15. Distribution of power losses in prototype SICAM with active clamp

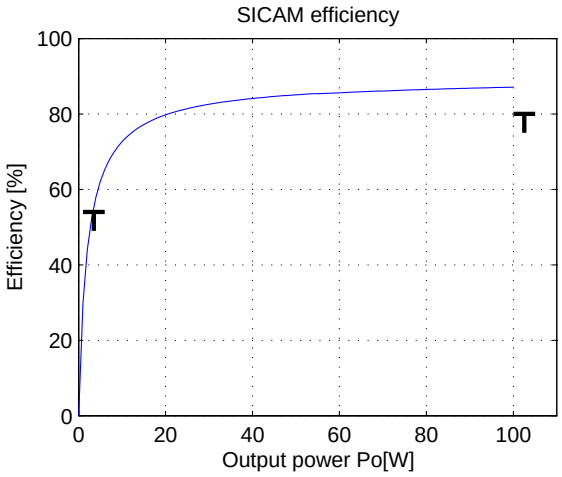

Fig. 8.16. Theoretical efficiency of the prototype SICAM with active clamp ("T"-shaped markings represent the targeted minimum efficiency)

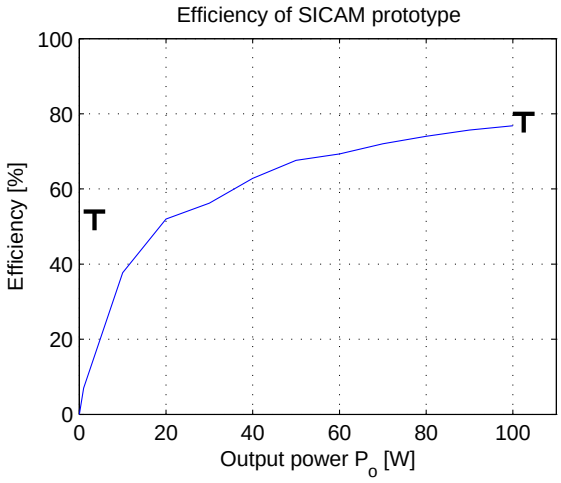

Fig. 8.17. Measure efficiency of the SICAM prototype with active clamp ("T"-shaped markings represent the targeted minimum efficiency)

Fig. 8.18. Photo of the prototype SICAM with safe-commutation switching sequence

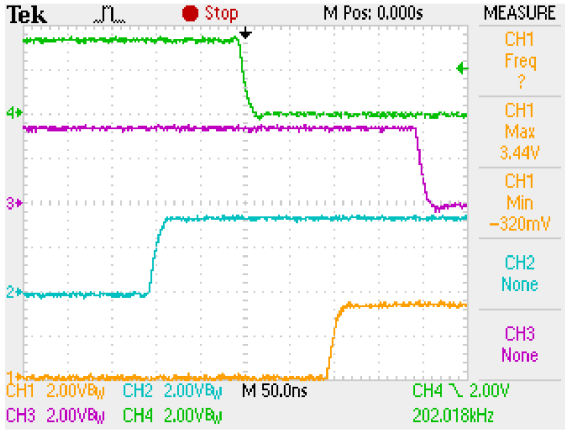

Fig. 8.19. SICAM safe-commutation switching sequence with $v_{HF} > 0$: 1) SW21, 2) SW22, 3) SW23, 4) SW24

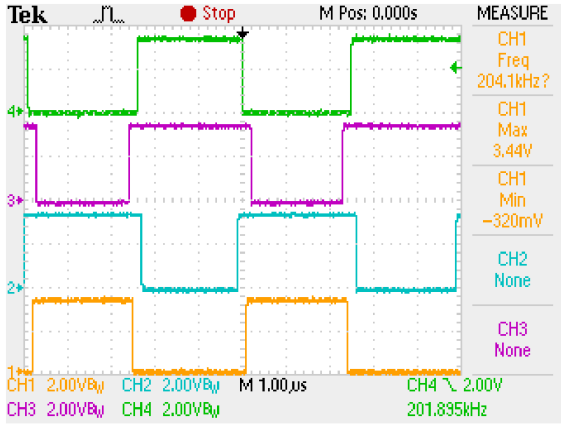

Fig. 8.20. SICAM safe-commutation switching sequence with $v_{HF} > 0$: 1) SW21, 2) SW22, 3) SW23, 4) SW24

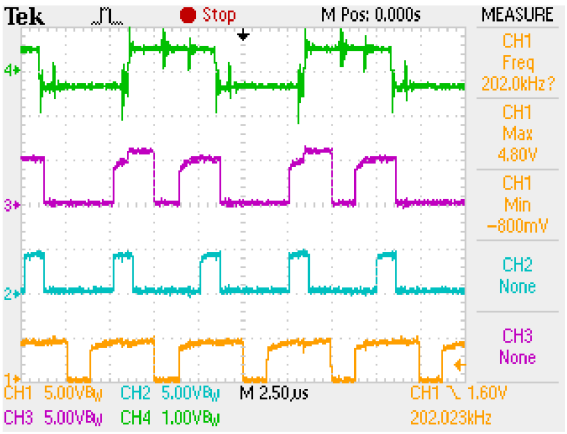

Fig. 8.21. Optimized PWM method for SICAMs: 1) PWM with positive signal, 2) PWM with negative signal, 3) resultant PWM, 4) HF-link voltage

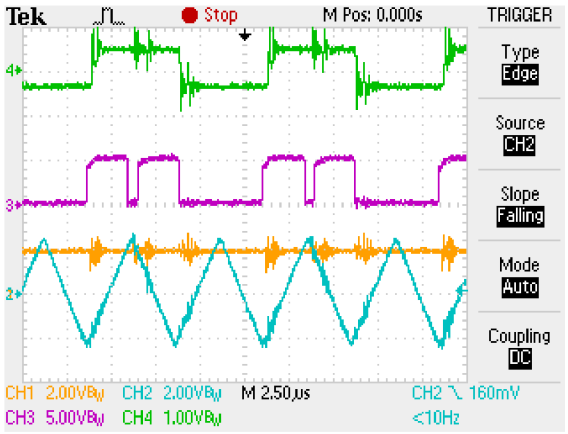

Fig. 8.22. SICAM safe-commutation switching sequence with $v_{HF} > 0$: 1) reference voltage, 2) triangular carrier, 3) bridge voltage, 4) HF-link voltage

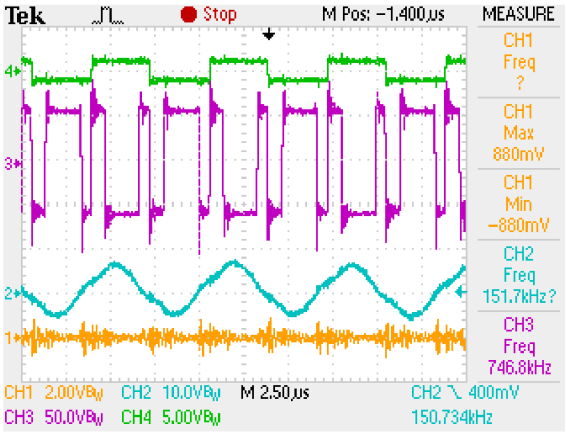

Fig. 8.23. SICAM waveforms at P_o=25 W: 1) reference voltage, 2) output voltage 3) bridge voltage, 4) HF-link voltage(50x)

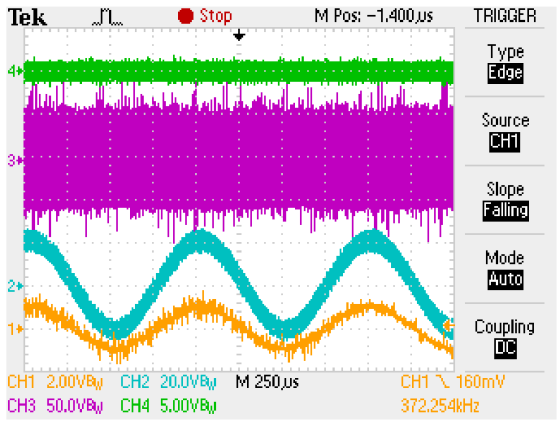

Fig. 8.24. SICAM waveforms at P_o=25 W: 1) ref. voltage, 2) out. voltage 3) bridge voltage, 4) HF-link voltage(50x)

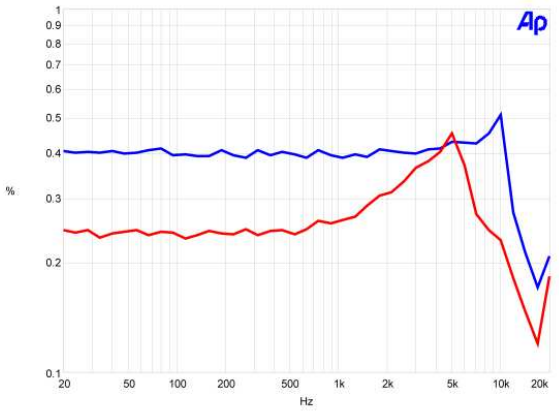

Fig. 8.25. THD+N vs. frequency at P_o=10 W (top) and P_o=40 W (bottom)

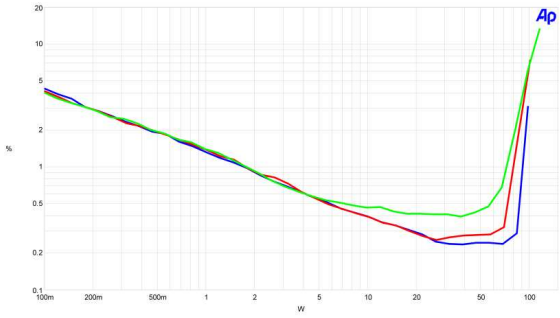

Fig. 8.26. THD+N vs. output power at f_o=100 Hz (bottom), f_o=1 kHz (middle) and f_o=6.67 kHz (top)

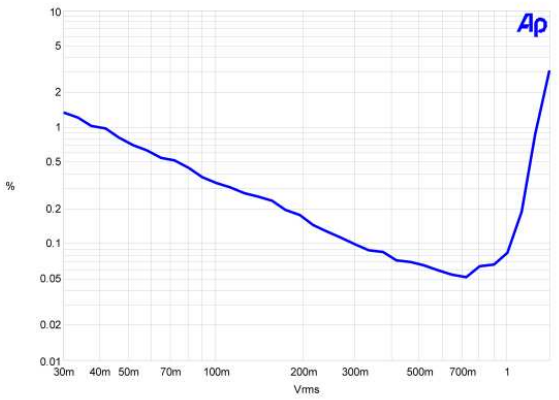

Fig. 8.27. Intermodulation distortion

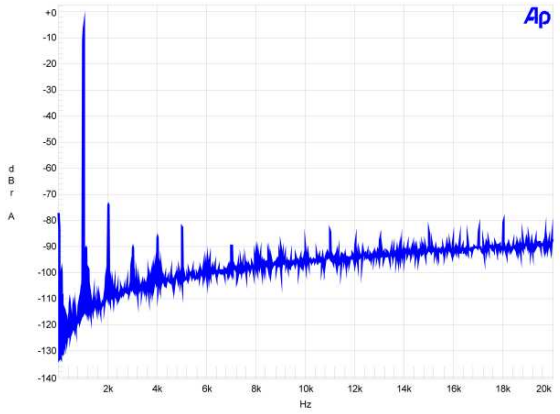

Fig. 8.28. FFT of the output voltage at P_o=25 W (100 W reference)

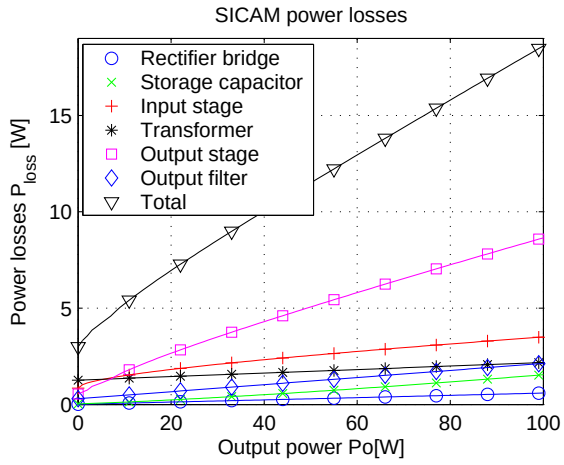

Fig. 8.29. Distribution of power losses in prototype SICAM with safe-commutation switching sequence

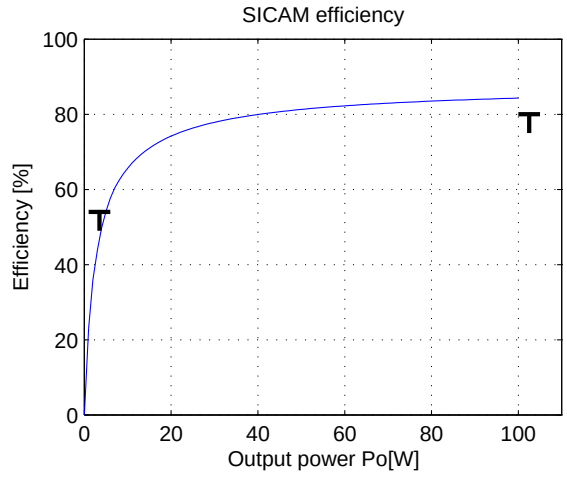

Fig. 8.30. Theoretical efficiency of the prototype SICAM with safe-commutation switching sequence ("T"-shaped markings represent the targeted minimum efficiency)

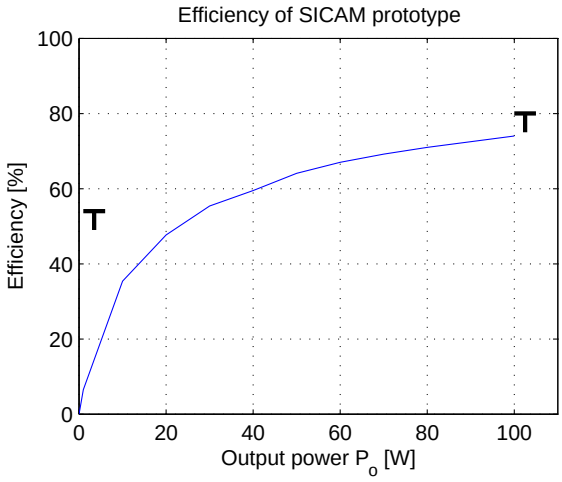

Fig. 8.31. Measured efficiency of the SICAM prototype with safe-commutation switching sequence ("T"-shaped markings represent the targeted minimum efficiency)

Fig. 8.32. Photo of the prototype self-oscillating SICAM with GLIM modulator

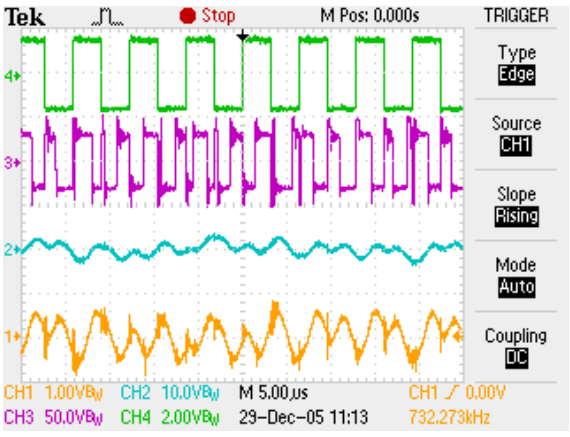

Fig. 8.33. Self-oscillating SICAM waveforms with zero reference: 1) carrier, 2) out. voltage 3) bridge voltage, 4) HF-link voltage(50x)

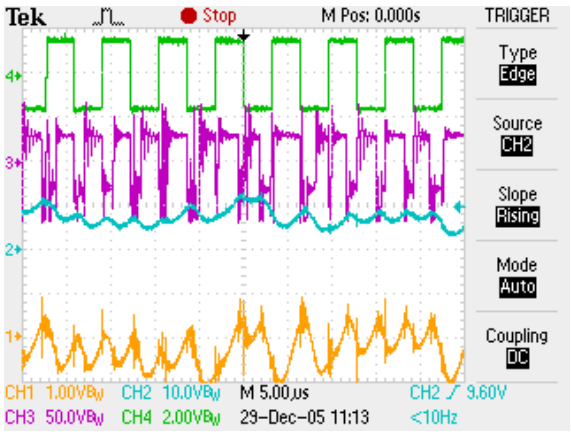

Fig. 8.34. Self-oscillating SICAM waveforms at $V_o = 10$ V: 1) carrier, 2) out. voltage 3) bridge voltage, 4) HF-link voltage(50x)

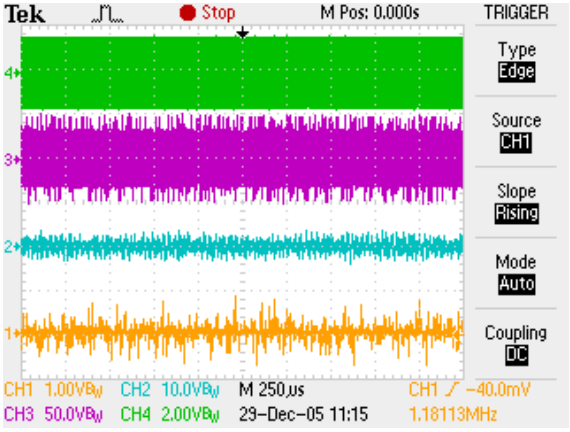

Fig. 8.35. Self-oscillating SICAM waveforms with zero reference: 1) ref. voltage, 2) out. voltage 3) bridge voltage, 4) HF-link voltage(50x)

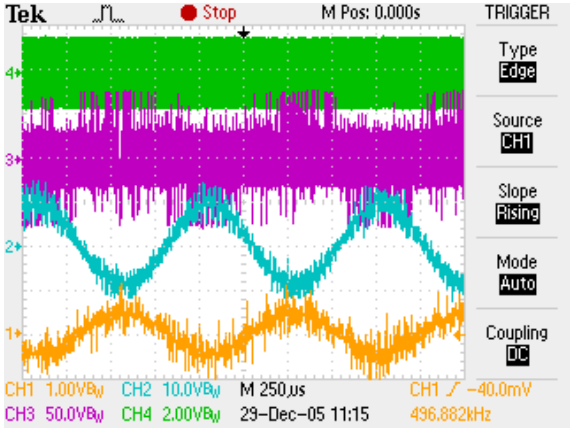

Fig. 8.36. Self-oscillating SICAM waveforms at P_o = 6 W with 1 kHz reference: 1) ref. voltage, 2) out. voltage 3) bridge voltage, 4) HF-link voltage(50x)

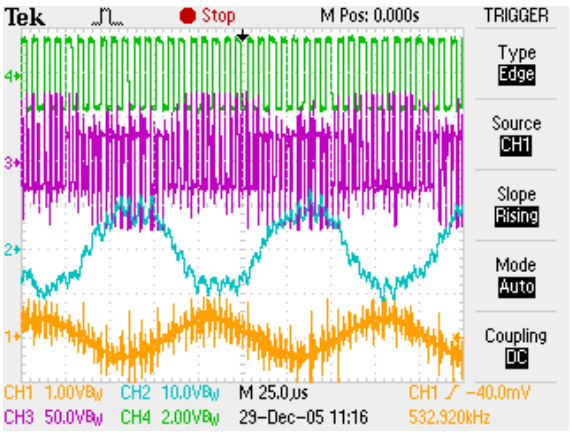

Fig. 8.37. Self-oscillating SICAM waveforms at P_o = 6 W with 10 kHz reference: 1) ref. voltage, 2) out. voltage 3) bridge voltage, 4) HF-link voltage(50x)

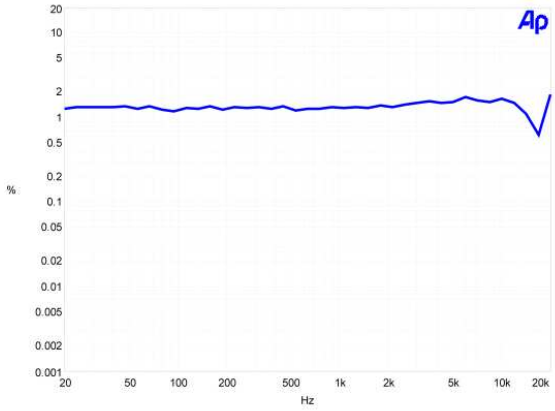

Fig. 8.38. THD+N vs. frequency at P_o=6 W

9

4Q flyback SICAM with modulated transformer voltages

"Science is a differential equation. Religion is a boundary condition."

- Alan Turing

Flyback converter presents the simplest isolated power supply topology, where the filtering inductor is actually integrated into the isolation transformer and represents means of transferring the energy from the primary-side voltage source to the secondary-side load. Consequently, the flyback converter saves the designer one magnetic component, but it increases the size and the stress exerted upon the other components, like the output capacitor that is to supply the whole load current for the periods when the main switch is turned on. On the other hand, there is just single-order filtering of the current switching harmonics at the output, performed solely by the output capacitor, which leads to substantial voltage ripple on the output. Therefore this topology is used only at lower power levels, when its benefits are most pronounced.

4Q flyback SICAM is a representative of the isolated SICAMs with modulated transformer voltages, which means that the primary side switches perform all the audio modulation of the voltages/currents, while the secondary side switches represent kind of synchronous rectifiers and perform the demodulation on the load side.

9.1 Operation and design of 4Q flyback SICAM

The two-switch four-quadrant (4Q) flyback SICAM is shown in Fig. 9.1. It is derived from the two-switch flyback converter by using the principles for developing SICAMs from conventional isolated SMPS topologies laid in Section 5.4 and depicted in Fig. 5.15. The secondary side consists of two windings and two bidirectional switches: $T_{21} - T_{22}$ with antiparallel diodes $D_{21} - D_{22}$ and $T_{23} - T_{24}$ with antiparallel diodes $D_{23} - D_{24}$, while the primary side stays essentially the same like in the two-switch flyback SMPS.

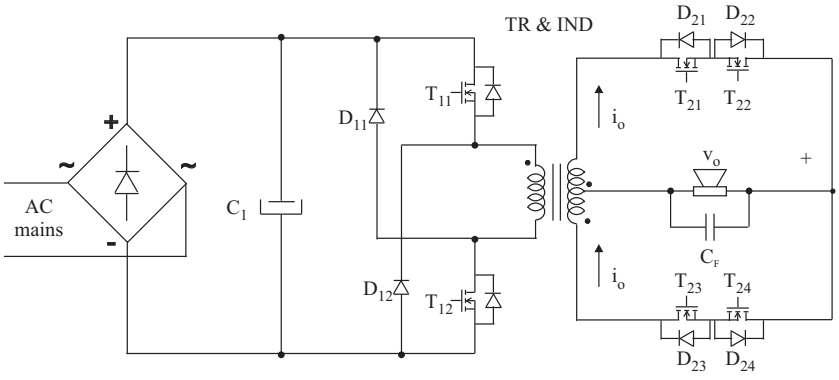

Fig. 9.1. Two-switch 4Q flyback SICAM

The amplifier is operated in a way that the primary side switches are turned on until enough energy has been stored in the magnetizing inductance of the flyback transformer, which is afterwards released either through $T_{21} - T_{22}$ or $T_{23} - T_{24}$ to charge the output capacitor to the desired voltage across the load. When the energy has been delivered to the load the current is allowed to reverse so that part of the capacitor charge is delivered back to the magnetizing inductance and returned to the primary side during the on-time of the main switches. This allows the flyback converter to operate in continuous conduction mode like a "rocking chair", where first the energy is delivered to the load side and then maybe it is partly returned back to the primary side. Current through the primary-side switches i_1, currents through the secondary-side switches i_{21}, i_{22}, output voltage v_o, control voltage v_c, state of the 1-bit quantizer Q and reference current i_{ref} of the 4Q flyback SICAM are all given in Fig. 9.2.

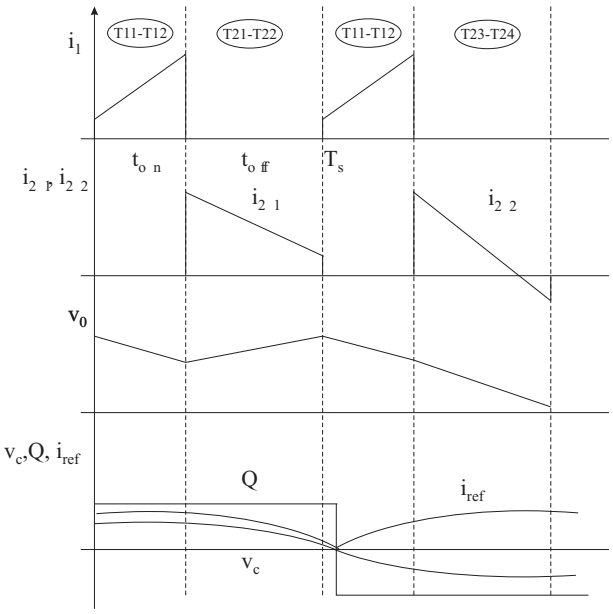

Fig. 9.2. Waveforms of the 4Q flyback SICAM

The 4Q flyback SICAM can be constructed as either single-switch or two-switch. In the practical implementations of single-switch DC-DC flyback converters, it is necessary to use a clamp on the primary side of the transformer to dissipate the energy stored in the primary-side leakage inductance. However, the voltage across the transformer during the off-time of the main switch can have either polarity and therefore the primary side clamp can be charged from the load side whenever the output voltage reflected to the primary side is higher than the clamp voltage. The two-switch 4Q flyback SICAM does not experience the same problem, since the transformer primary side during the off-time of the main switch is clamped to the rectified input voltage by using the two freewheeling diodes D_{11} and D_{12}. This voltage is always bigger than the reflected load voltage since it is limited by the design i.e. the duty cycle is less than 50%. Because of the same reason, the primary side switches do not need to have bidirectional voltage blocking capability, but must have bidirectional current capability (ex. MOSFETs) to allow continuous current-mode operation. Taking into account the additional benefit that the two-switch flyback converter requires switches with just half the voltage blocking capability of the one-switch flyback converter, it can be concluded that the two-switch topology represents a very feasible choice for bidirectional converters from cost and implementation perspective.

The disadvantages of the flyback converter with regard to the large output capacitance needed for filtering the switching harmonics of the inductor current become even more pronounced in its bidirectional implementation. The output capacitor is supplying the whole load current during the on-period of the main switches, therefore the demands set upon it are very stringent. Due to the bipolar nature of the output voltage, the unipolar aluminium electrolytic type capacitors found in conventional switching-mode power supplies cannot be used and the size of the output section is inevitably increased. Therefore, the flyback topology for SICAMs is limited to low power levels.

The most difficult part of the design of the 4Q flyback SICAM power section is the selection of the output capacitor and the flyback transformer magnetizing inductance. The minimum output capacitor is determined by the desired maximum output voltage ripple:

$$C_{min} = \frac{Q}{\Delta V_{max}} = \frac{I_{o,max} D_{max}}{\Delta V_{max} f_s} \tag{9.1}$$

where $I_{o,max}$ is the maximum load current, D_{max} is the maximum duty cycle, ΔV_{max} is the maximum voltage ripple and f_s is the switching frequency.

Although C_{min} is the minimum output capacitance needed with regard to the output voltage ripple limit, it is also the optimal since increasing that value significantly over C_{min} will result in slower response. It will be shown in the next section that the actual output voltage ripple can also depend on the bandwidth of the outer voltage loop, with the proposed control methods.

Choosing the optimal value of the inductance represents slightly greater challenge. One way of choosing the magnetizing inductance is by determining the maximum slope of the average output current $i_o = I_o \sin(2\pi f t)$ and associated average inductor current $i_L = i_o/(1-D)$:

$$\begin{aligned} S_{I_o,max} &= 2\pi f_{max} I_o \cos(2\pi f_{max} t)|_{t=0} = 2\pi f_{max} I_o \\ S_{I_L,max} &= \frac{S_{I_o,max}}{1 - D_{max}} \end{aligned} \tag{9.2}$$

and choosing the instantaneous rising slope of the inductor current V_g/L to be at least 20 times higher than the average inductor current slope $S_{I_L,max}$.

The other preferred way of selecting the magnetizing inductance is by noting that it is limiting the minimum frequency of the right-half plane zero f_{RHPZ} [60]:

$$f_{RHPZ,min} = \frac{D'^2_{min} R}{2\pi D_{max} L_{max}} = 0.5 \frac{R}{2\pi L_{max}} \tag{9.3}$$

It is known that the maximum usable control bandwidth of a system is limited to approximately one third of the frequency of the right half-plane zero [93] and one tenth of the switching frequency f_s. This leads for example to the following selection rule:

$$L_{max} = 0.5 \frac{R}{2\pi \cdot f_{RHPZ,min}} = 0.5 \frac{R}{2\pi \cdot 0.3 f_s} \tag{9.4}$$

Slightly different 4Q flyback converter has been presented in [94], where it is built around a dedicated chipset for ring generators. Its operation principles differ from the proposed simple solution, since during the off-time of the main switch, the secondary side switches are operated in a PWM manner and energy is transferred to the primary side via a separate winding with series rectifier. Another difference is that the secondary side switches can block both voltage polarities, but the current can only be unidirectional and the flyback converter operates in discontinuous conduction mode without the aforementioned "rocking chair" effect.

9.2 Control of 4Q flyback SICAM

The selection of the control algorithm for the 4Q flyback SICAM represents a trade-off among many different objectives, like stability, low distortion and simplicity of implementation.

The simplest way of control is single loop output voltage control, where the only feedback is taken from the load voltage and is used afterwards to derive the main switch duty cycle. The main disadvantages with this approach are the involved second order transfer function with the continuous mode operation, which makes it very difficult to make satisfactory control synthesis, as well as the inability to correct for input line perturbations until changes are observed in the output voltage.

Much better performance can be achieved with current-mode control, where the inner current loop and the outer voltage loop are simultaneously used to derive the duty cycle of the main switch. While the voltage loop is always taken from the load, the selection of current for closing the inner current loop can ask for careful consideration. In the buck derived topologies, where the second order LC output filter is placed across the load, the inductor current is essentially the load current and by controlling directly the inductor current, the dynamics of the load current is being governed too. On the other hand, the flyback output current is different than the inductor current by a factor which depends on the duty cycle and it can be disputed which of these two is to be controlled. However, if the goal of the current selection is to simplify the control synthesis of the outer voltage loop, then by controlling the inductor current the pole associated with the inductor is moved to higher frequencies. Even more, sensing inductor current is sometimes easier due to its continuity and can be done in many different ways, some being more simple than the others. Therefore, in the following sections will be dealt only with inductor current control in the inner loop.

There are many different ways to implement current-mode control, among which the peak and average current-mode control are probably the most applicable ones. They have some distinct advantages and pitfalls, which define their specific application areas. They can be both used in 4Q flyback SICAMs and their implementation is subject of the next few sections.

9.2.1 Peak current-mode control

The block scheme of the control section of the 4Q flyback SICAM with peak current-mode control is given in Fig. 9.3. As shown, it is a cascade system where the inner loop sets the inductor current and the outer loop controls the output voltage. The absolute value of the control voltage v_c gives the reference current i_{ref}, while its sign given by the comparator i.e. 1-bit quantizer Q determines which secondary-side bidirectional switch will be turned on during the off-time of the primary side switches. The reference current i_{ref} is subsequently compared with the instantaneous value of the switch current to determine the switching-off instant, resulting in peak current-mode control. Beside the aforementioned simplification of the transfer function, the peak current-mode control yields a simple solution with fast response, high rejection ratio of the input voltage perturbations and cycle-by-cycle current limiting.

In order to avoid output voltage zero-crossing distortion i.e. crossover distortion, there must be some minimum inductor current delivered to the output even at idle. During this idling time, the 1-bit quantizer is likely to be stuck in a certain state of the output stage, which means that the output voltage will continue to increase in one direction. With other words, 4Q flyback SICAM does not have any stable equilibrium state corresponding to

idle, which represents a strong contrast to the conventional Class D audio power amplifier, where operation with duty cycle of 50% assures zero average output voltage with certain predetermined and limited output filter ripple. In the 4Q flyback SICAM it is up to the outer voltage loop to sense this excessive voltage ripple at idle and prohibit it by changing the sign of the control voltage v_c and the associated output stage state. Therefore, in this implementation it is very important to have shorter time delays within the control loop and provide high control bandwidth, by increasing the gain of the phase compensator $G_v(s)$. The highest possible gain of the compensator at the switching frequency, which does not cause instability is determined by matching the up-slope of the increasing inductor current and the down-slope of the falling output voltage, like shown in Fig. 9.4:

$$\begin{aligned} R_{CS}\frac{V_g}{L} &= A\frac{v_o}{RC} \\ A_{max} &= \frac{R_{CS}\cdot R\cdot C\cdot V_{g,min}}{L\cdot V_{o,max}} \end{aligned} \tag{9.5}$$

where R_{CS} is the current sense resistor, V_g is the DC source voltage, R is the load resistance and A is the gain from the output voltage to the input of the current controller at f_s.

Design of the phase compensator $G_v(s)$ is performed by shaping the overall loop transfer function L so that both sufficient gain throughout the desired signal frequency range and high bandwidth are obtained. The plotting of the loop transfer function is alleviated by assuming that the inner current loop operates ideally and the inductor current i_L is following the reference current i_{ref} with a high degree of accuracy, although this essentially depends on the level of inductor current ripple Δi_L. The loop gain L and its constitutive parts are:

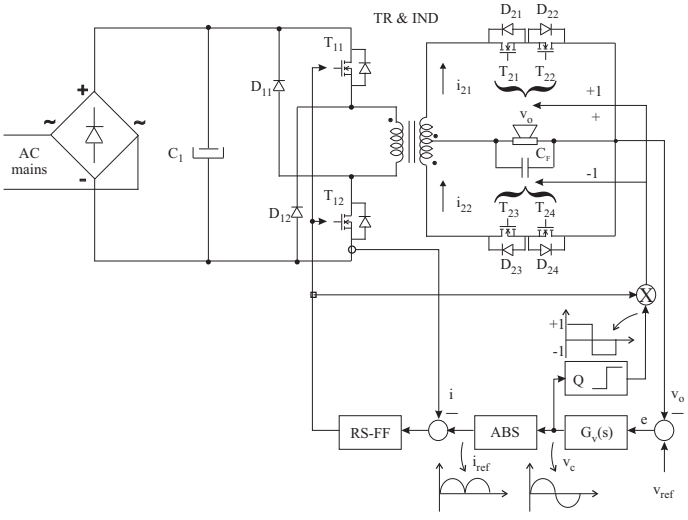

Fig. 9.3. Peak current-mode control

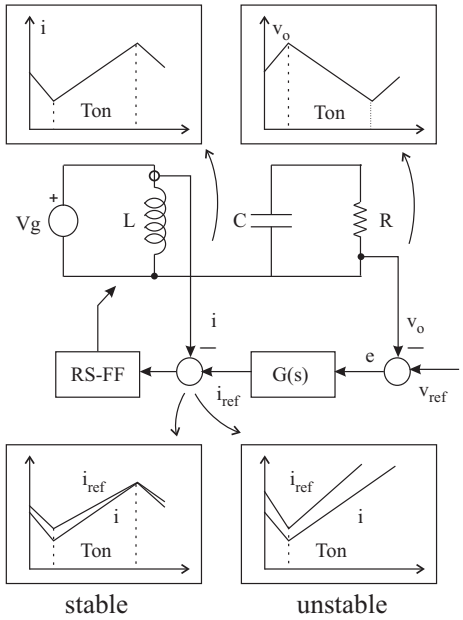

Fig. 9.4. Slope matching

$$
\begin{aligned}
L(s) &= G_v(s)G_{i_Lc}(s)G_{oi_L}(s)G_{opto}(s)H_v(s) \\
G_v(s) &= K(1+\frac{1}{s\tau_i}) \\
G_{i_Lc}(s) &= \frac{1}{nR_{CS}K_{CS}} \\
G_{oi_L}(s) &= \frac{R}{1+sRC} \\
G_{opto}(s) &= K_i \\
H_v(s) &= \frac{1}{K_v}
\end{aligned}
\tag{9.6}
$$

where G_v is the transfer function of the PI voltage phase compensator, G_{i_Lc} is the transfer function from the reference current to the inductor current, G_{oi_L} is the transfer function from the inductor current to the output voltage, G_{opto} is the gain of the linear optocoupler transferring the current reference from the primary to the secondary side and H_v is the gain f the voltage feedback. Control block diagram of the 4Q flyback SICAM with peak current-mode control is given in Fig. 9.5.

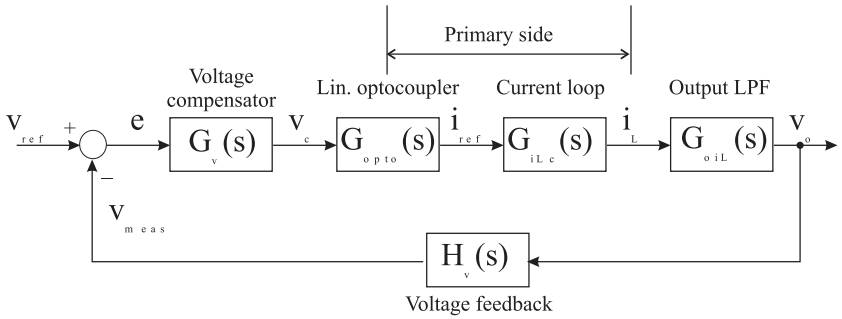

Fig. 9.5. Peak current-mode control block diagram

It is interesting to note that, although the 4Q flyback converter has much simpler power section than the Class D amplifier with separate power supply, the control section shown in Fig. 9.3 tends to be involved and is further aggravated by the need for crossing the isolation barrier. The way this is usually done in a conventional flyback SMPS is to transfer the current reference using a simple optocoupler, which often has a highly nonlinear current transfer ratio (CTR) when looked in a large signal sense. On the other hand, the operation of a 4Q flyback SICAM involves largely varying control signals and the current reference i_{ref} must be transferred to the isolated primary side with high degree of accuracy to avoid excessive distortion. The easiest way to do that is to use a linear optocoupler with servo loop built around it for linearizing its CTR. This results in a combined primary and secondary side control, where the phase compensator of the outer voltage loop resides on the secondary side and the phase compensator of the inner current loop is implemented on the primary side together with the sensing of the switch current. As an option, switch current can be sensed and transferred to the secondary side with a current transformer, so that all the control is located on the secondary side. However, the gate drive signals for the primary side switches still need to be transferred back with a separate pulse transformer, thus complicating this option even further.

9.2.2 Average current-mode control

Beside the aforementioned advantages of the peak current-mode control with regard to its simplicity, speed and cycle-by-cycle current limiting, there are also some serious drawbacks. The most important drawback is the fact that controlling the peak value of the inductor current does not necessarily mean that the average inductor current value follows the current reference, which becomes especially pronounced in the continuous mode operation with large ripple current and even more in the discontinuous mode. For example, if the peak inductor current follows perfectly the sinewave current reference of the audio amplifier, the actual average inductor current is likely to be much different than the reference, depending on the amount of current ripple. As a side effect of this problem, the low frequency gain of the peak current-mode controller is limited and does not guarantee high performance throughout the whole power bandwidth.

Operation of the 4Q flyback SICAM with large inductor ripple current is desired for at least two reasons. Firstly, large ripple is a result of low flyback transformer inductance which allows for much smaller size of the magnetics. On the other hand, low inductance is also a must, since for proper operation of the audio power amplifier the current level must be changed sufficiently fast to achieve the desired dynamics of the converter. This means that correct control of the average inductor current with low distortion will be nearly impossible with peak current-mode control.

In order to reduce the distortion, average current-mode control can be implemented and optimized by slope matching for achieving optimal speed of the response [95], comparable to peak current-mode control. By proper design of the phase compensator in the inner current loop, sufficient gain can be provided even at low frequencies where peak current-mode control is unable to deliver the same performance when large inductor current ripple is present.

Average current-mode control also enables use of non-dissipative techniques for inductor current sensing, in contrast to the usual current sense resistor technique. The inductor current can be estimated by putting additional winding on the flyback transformer and ideally integrating the transformer voltage with electronic components. In this case all the control can be done on the secondary side, and it is just the main switches gate drive that needs to be transferred to the primary side. In practice, integration of the transformer voltage is impossible due to the non-zero offset of operational amplifiers, and what is usually done is low pass filtering to derive exactly the high frequency content of the inductor current. This essentially means that the DC value of the inductor current with this method can not be recovered. Thus the low frequency performance of the control circuit is left to the outer voltage loop. The control block diagram of the 4Q flyback SICAM with average current-mode control is given in Fig. 9.6 and the complete schematic is given in Fig. 9.7. Inductor current estimator transfer function is:

$$G_{i,est}(s) = K_{i,est} \cdot \frac{N_e}{N_l} \cdot \frac{1}{1 + s\tau_{i,est}} \tag{9.7}$$

where $K_{i,est}$ and $\tau_{i,est}$ represent the estimator gain and time constant, and N_e and N_l are the estimator and inductor number of turns respectively.

9.3 Measurements on a 4Q flyback SICAM prototype with average current-mode control

To test the feasibility of the proposed simple approach to building isolated SICAMs with modulated transformer voltages, an 80 W into 8 Ω two-switch 4Q flyback subwoofer

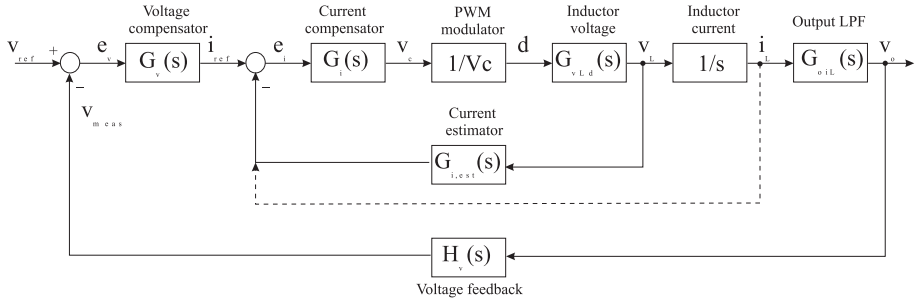

Fig. 9.6. Average current-mode control block diagram

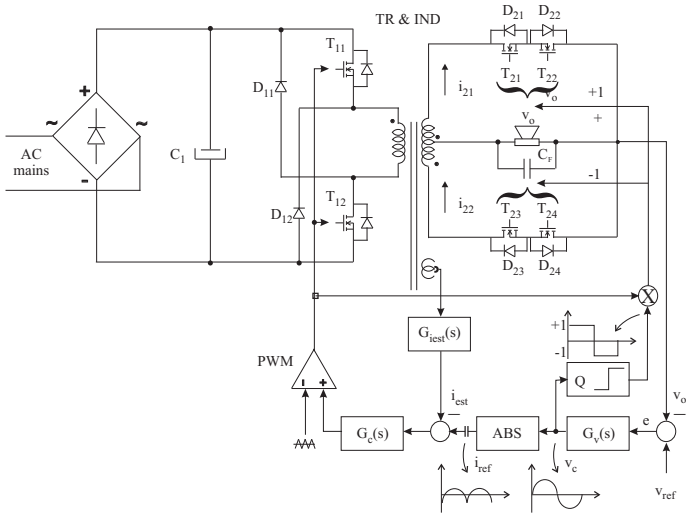

Fig. 9.7. Average current-mode control

SICAM prototype with average current-mode control was constructed and its photo is shown in Fig. 9.8. Its circuit schematics can be found in Appendix F.5. The switching frequency is set to $f_s = 150$ kHz. The prototype resembles the structure shown in Fig. 9.7. It also incorporates integrated magnetics structure for deriving all the auxiliary voltages on the secondary side as explained in Section 10.2 and depicted in Fig. 10.5.

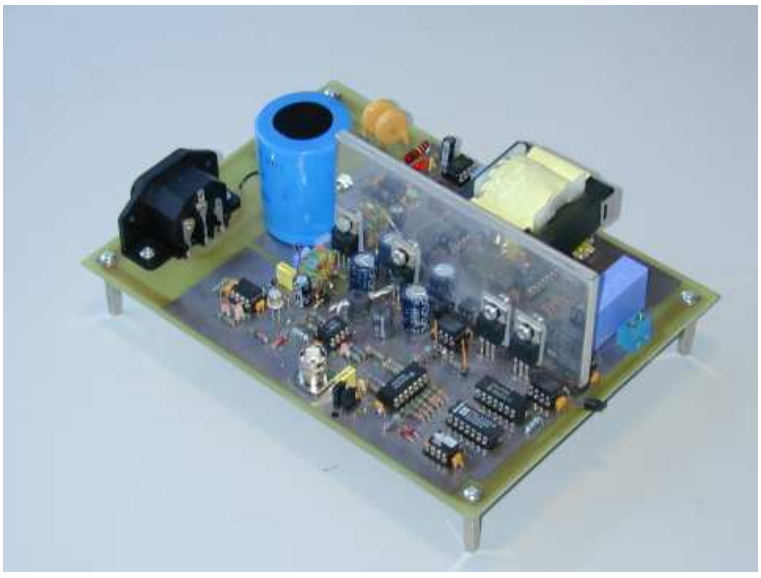

Fig. 9.8. 4Q flyback SICAM prototype

Fig. 9.9 shows in detail the operation of the 4Q flyback SICAM with zero reference. The short on-periods of the primary side switches represent some minimum allowed on-time being intentionally inserted even with no error voltage on the input of the controller, just to avoid zero-crossing distortion of the output voltage. The state of the one-bit quantizer Q determines the secondary side bidirectional switch, which will be turned on right after the primary side switches seize conducting. The selected bidirectional switch is turned on for the rest of the time until the primary side switches conduct again, although the state of the one-bit quantizer Q maybe has changed in the meantime. Due to the fast outer voltage loop even this small ripple in the output voltage is sensed and is causing an immediate change in the control voltage sign, so that the selected bidirectional output switch alternates each period to yield minimum ripple voltage. Making the outer voltage loop slow will cause the output voltage ripple to be large, since the guaranteed minimum inductor current with the same output switch turned on during few periods will continue charging the output capacitor to large values.

Fig. 9.10 depicts the operation of the 4Q flyback SICAM with constant DC-reference, leading to output voltage of around V_o=16 V at output power of P_o=32 W. It can be seen that the width of the gate-drive pulses on the primary side has increased compared to the idling width in Fig. 9.9, to deliver the necessary power to the load side.

Fig. 9.11 shows the operation of the 4Q flyback SICAM at output power of P_o=50 W with 200 Hz reference voltage. The shape of the output voltage looks very good, but a measurement with audio equipment revealed THD+N of few percents in the whole audio range, which is not very close to the desired levels for the application.

The efficiency of the prototype η as function of the output power P_o is given in Fig. 9.12 and the idling losses are approximately P_{idle} =9 W. This particular realization of SICAM has lower efficiency than the targeted one according to the project description, which is not very strange for flyback implementation where the components are extremely stressed. However, it is believed that a major part in the lower efficiency of the prototype itself is played by poor synchronization of the primary and secondary switches, which leads to certain short shoot-through events, as well as the relatively high idling power losses.

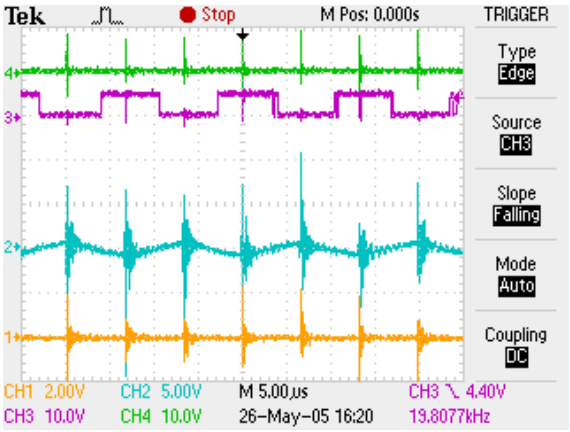

Fig. 9.9. Waveforms with zero reference: 1) ref. voltage v_{ref}, 2) output voltage v_o, 3) comparator Q output, 4) primary gate drive

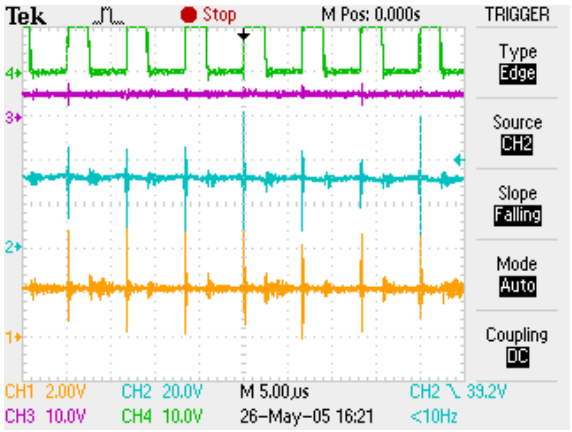

Fig. 9.10. Waveforms with DC-reference: 1) ref. voltage v_{ref}, 2) output voltage v_o, 3) comparator Q output, 4) primary gate drive

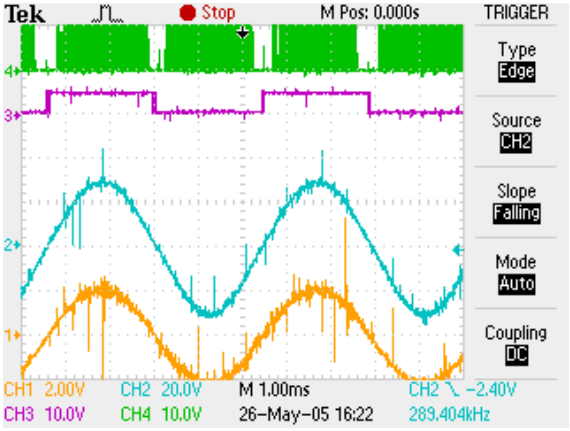

Fig. 9.11. Waveforms at P_o=50 W with 200 Hz reference: 1) ref. voltage v_{ref}, 2) output voltage v_o, 3) comparator Q output, 4) primary gate drive

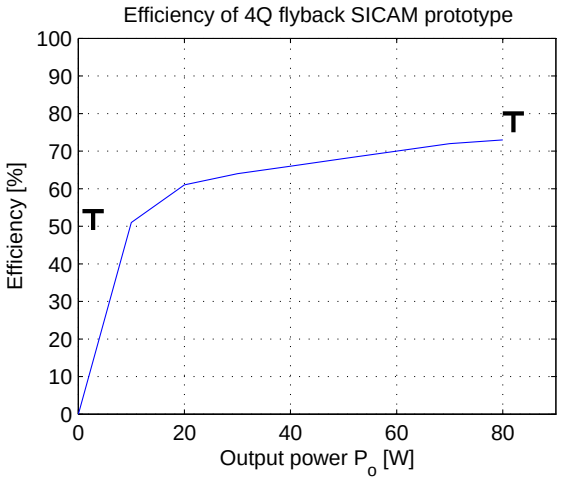

Fig. 9.12. Efficiency of the 4Q flyback SICAM prototype ("T"-shaped markings represent the targeted minimum efficiency)

9.4 Conclusion

4Q flyback SICAM is the simplest isolated SICAM topology with modulated transformer voltages, where the inductor is integrated in the main transformer and filter capacitor is the only discrete filtering component at the output. It operates in a similar way to the common flyback SMPS topology, except that the secondary-side winding has a central tap and two bidirectional switches to redirect the magnetizing current to the either end of the load. The operation of the primary and secondary switches, described as "rocking chair" to symbolize the flow of energy in both directions, must be fairly synchronized in order to avoid significant flow of energy in the primary-side clamp or back to the grid.

Although 4Q flyback represents a very simple topology, the output filtering capacitor is bulky and is subject to high component stress, since it supplies the whole load current during the periods when the primary-side switches are turned on. Because of the same reason, output voltage ripple is also high. One additional problem is created by the right-half plane zero pertinent to the flyback topology, which significantly limits the highest achievable control bandwidth.

Two control methods being extensions of the common current mode control are presented: simple peak current mode control, which lacks low frequency gain and average current mode control, which is desirable also for the possibility of easily integrating inductor current estimator in the control scheme.

The presented measurement results of a prototype prove the feasibility of the 4Q flyback SICAM for audio power amplification. Its application is intended for lower output power levels and lower audio frequency range with limited performance requirements i.e. for not very high-demanding application, like for example subwoofer applications.

10

Integrated magnetics for isolated SICAMs

"He who loves practice without theory is like the sailor who boards ship without a rudder and compass and never knows where he may cast."

- Leonardo Da Vinci

This chapter presents a new integrated magnetics design for HF-link converters, which can significantly improve the compactness and reduce component count by placing the magnetic components from the auxiliary power supply or having some design-specific functions on the same magnetic core with the main transformer. The proposed integrated magnetics can be built around all standard three-leg cores used in power electronics, which have the possibility for putting bobbins on each of the legs. The only additional burden is the somewhat increased winding, manufacturing and assembling complexity, as well as a possible requirement for slightly increasing the volume of the original magnetic core.

The main difference of the proposed solution when compared with other integrated magnetics designs for switching-mode power supplies [96], is that the windings of the corresponding structures do not belong to the same voltage loop and do not share the same voltage waveforms, which opens some new application areas.

The proposed integrated magnetics concept is very similar to patent [97] citing some possible SMPS applications, but it was developed totally independently from it and with having just the SICAM applications in mind.

10.1 Analysis of the integrated magnetics

In order to develop the proposed integrated magnetics design for HF-link converters, it is important to analyze the three-winding transformer, shown in Fig. 10.1. By having three transformer legs, the equivalent electrical circuit introduces two loops i.e. contours, characterized by two independent fluxes Φ' and Φ''. These fluxes are functions of the magnetomotive forces (MMF) F_i in the corresponding contours and are used to calculate the fluxes Φ_i:

$$\begin{aligned}
\Phi_1 &= \frac{(R_2+R_3)F_1 - R_3F_2 - R_2F_3}{R_1R_2 + R_3(R_1+R_2)} \\
\Phi_2 &= \frac{-R_3F_1 + (R_1+R_3)F_2 - R_1F_3}{R_1R_2 + R_3(R_1+R_2)} \\
\Phi_3 &= \frac{-R_2F_1 - R_1F_2 + (R_1+R_2)F_3}{R_1R_2 + R_3(R_1+R_2)}
\end{aligned} \tag{10.1}$$

Beside the general case in Fig. 10.1, especially interesting is one specific transformer design depicted in Fig. 10.2. As a result of the equal number of turns in the outer windings and their series connection, the magnetomotive forces F_1 and F_3 are equal by amplitude and with opposite signs $F_1 = -F_3 = F_l$. The central leg magnetomotive force is likely to be different $F_2 = F_c$. It is also assumed that the transformer core is ideally symmetrical, which means that the magnetic reluctances of the outer legs are equal $R_1 = R_3 = R_l$ and

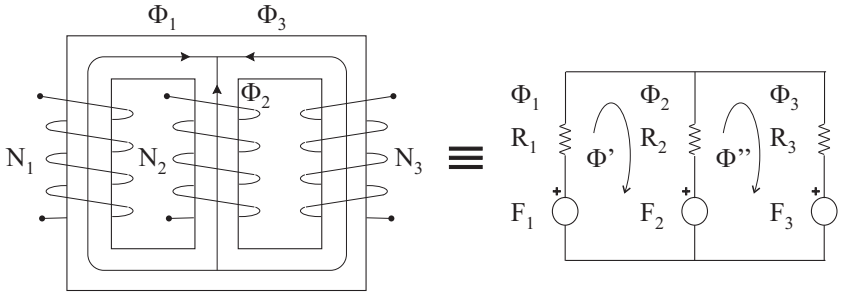

Fig. 10.1. Three-winding transformer and its equivalent electrical circuit

different from the reluctance of the central leg $R_2 = R_c$, resembling many of the standard ferrite cores. In this case the leg fluxes become:

$$\begin{aligned}
\Phi_1 &= \frac{(R_l + 2R_c)F_l - R_l F_c}{R_l(R_l + 2R_c)} \\
\Phi_2 &= \frac{2F_c}{R_l + 2R_c} \\
\Phi_3 &= \frac{-(R_l + 2R_c)F_l - R_l F_c}{R_l(R_l + 2R_c)}
\end{aligned} \tag{10.2}$$

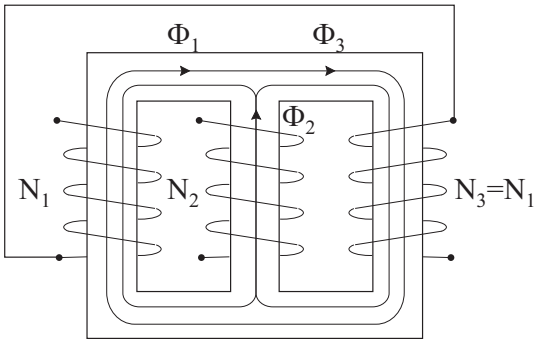

Fig. 10.2. Special design of the three-winding transformer

From (10.2) it is clear that under ideally symmetrical conditions, the center leg flux Φ_2 is not affected by the magnetomotive forces F_l in the outer legs. Even more, the induced voltage in the two series outer windings does not have any component associated with the center leg flux:

$$v_i = N_1 \frac{d\Phi_1}{dt} - N_3 \frac{d\Phi_3}{dt} = N_1 \frac{d}{dt}\left(\frac{F_l}{R_l}\right) \tag{10.3}$$

Simulation of the MMFs and the induced voltages in the central leg and outer legs windings of an E42/21/15 core under ideally symmetrical conditions is given in Fig. 10.3.

In reality, it is very difficult to achieve total symmetry due to manufacturing and assembling tolerances, so it is interesting to challenge the above conclusions. Assuming that there is a slight difference between the magnetic reluctances of the outer legs in excess of $2\Delta R$ due to, for example, slightly different core dimensions or non-equal air-gapes, leg fluxes become:

$$\begin{aligned}\Phi_1 &= \frac{(2R_c + R_l - \Delta R)F_l - (R_l - \Delta R)F_c}{(R_l + \Delta R)R_c + (R_l - \Delta R)(R_l + \Delta R + R_c)} \\ \Phi_2 &= \frac{2\Delta R F_l + 2R_l F_c}{(R_l + \Delta R)R_c + (R_l - \Delta R)(R_l + \Delta R + R_c)} \\ \Phi_3 &= \frac{-(2R_c + R_l + \Delta R)F_l - (R_l + \Delta R)F_c}{(R_l + \Delta R)R_c + (R_l - \Delta R)(R_l + \Delta R + R_c)}\end{aligned} \tag{10.4}$$

The relationships in (10.4) for the non-ideal case show that when $\Delta R \ll R_l$, the center leg flux is still affected only by the center leg magnetomotive force F_c. The resultant induced voltage in the series windings of the outer legs is equal to the derivative of the outer fluxes sum:

$$v_i = \frac{d}{dt}(\Phi_1 + \Phi_3) = \frac{d}{dt}\left[\frac{2N_1(2R_c + R_l)F_l + 2N_1\Delta R F_c}{(R_l + \Delta R)R_c + (R_l - \Delta R)(R_l + \Delta R + R_c)}\right] \tag{10.5}$$

which is not significantly affected by the central leg MMF if $\Delta R \ll 2R_c + R_l$. The aforementioned conditions in practice are not too difficult to obey and do not represent a limiting factor. Simulation of the MMFs and the induced voltages in the central leg and outer legs windings under asymmetrical conditions with $\Delta R = 10\%$ is given in Fig. 10.4, showing just a slight induced voltage modulation.

It is of ultimate importance to carefully design the proposed integrated magnetics with regard to saturation, since the resultant flux $\Phi_2 \pm \Phi_1/2$ in the outer rim can easily saturate the outer legs, which usually have only half of the effective cross-section area of the center leg. Another important issue is to limit the integrated magnetics operation to only the linear part of the magnetization characteristics, since operating it on the saturated part will introduce cross-coupling effects among the fluxes in the respective legs.

10.2 Application to HF-link converters

The block scheme of the direct energy conversion switching-mode audio power amplifier with HF-link shown, i.e. a SICAM in Fig. 5.2 introduces much simpler power conversion topology than the conventional approach in Fig. 5.1 comprising of a separate switching-mode power supply and a Class D audio power amplifier connected to its DC-link. However, what is not immediately clear from these simplified block diagrams is that SICAM requires many magnetic components with different functions:

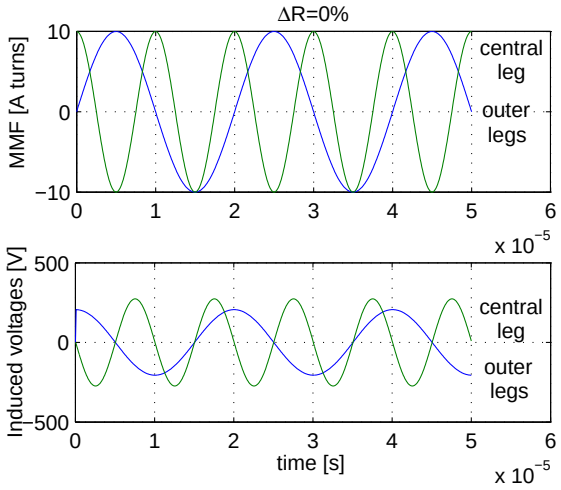

Fig. 10.3. MMFs and induced voltages under symmetrical conditions $\Delta R = 0\%$

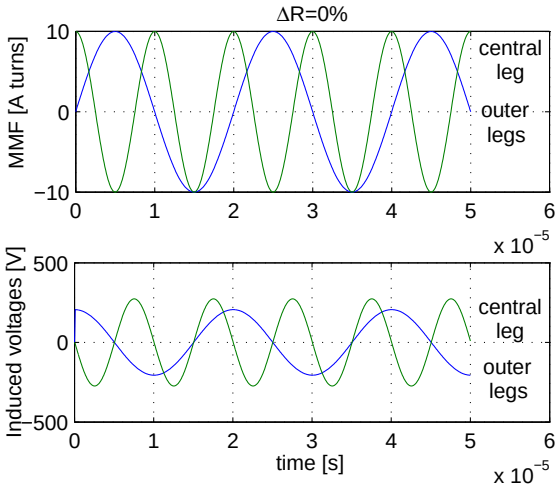

Fig. 10.4. MMFs and induced voltages under asymmetrical conditions $\Delta R = 10\%$

- main power transformer - with all topologies,
- auxiliary power transformer - for control biasing and maybe for isolated gate drives, especially in SICAMs with modulated transformer voltages,
- output filter inductor - with all topologies,
- signal transformers - for transfer of signals between the input and the output stage,
- impulse transformers for bidirectional switch gate drive, and
- power transformer for the active clamp circuit - with certain SICAM topologies.

In one implementation of SICAM with modulated transformer voltage [3], transformer voltages are PWM modulated by the input switching stage according to the reference signal. This means that the transformer flux and subsequently the power flow to any secondary winding are dependent on the reference signal and are far from constant. This makes it impossible to put any auxiliary windings on the transformer central leg for providing control biasing and/or isolated gate drive supplies. However, by using the proposed integrated magnetics and a simple switching converter on the primary, many symmetrical windings can be fitted on the outer legs to derive auxiliary voltages. This is shown in Fig. 10.5, in the case of a 2-switch four-quadrant flyback audio power amplifier, whose transformer voltages are modulated by the reference.

In order to improve the efficiency of SICAMs with dissipative clamp for commutating the load current in the output stage [9], SICAM with active capacitive voltage clamp from Section 6.2.3 which returns the clamped energy from the secondary side back to the primary side capacitor can be implemented by using a simple single-switch isolated converter. With the proposed integrated magnetics, the active clamp converter can be implemented on the same core with the main transformer, as shown in Fig. 10.6.

All isolated SICAMs have two switching stages and their operation usually is synchronized in order to avoid any possible intermodulation products in the output voltage or to achieve safe commutation of the load current in the output stage, as already described in Section 7.2.2. In most of the cases, switching instants of the primary stage are derived from the triangular carrier of the PWM modulator placed in the secondary side controller. Instead of using additional optocouplers or signal transformers for transferring the switching command to the primary, the latter can be achieved simply by putting two sets of symmetrical windings on the power transformer outer legs, as shown in Fig. 10.7.

As an ultimate task of magnetic integration, the output filter inductor can be integrated in the HF-link transformer. Since the inductor necessitates substantial gapping of the ferrite core in order to be able to store enough magnetic energy, it is appropriate to fit the inductor on the center leg and the transformer on the outer legs, as depicted in Fig. 10.8. This is likely to necessitate larger core to accommodate both fluxes and fit both windings, but on the other hand it is a single magnetic component.

10.2.1 Practical investigation of the proposed integrated magnetics

The proposed integrated magnetics was implemented in several isolated SICAM prototypes with different topologies and with different goals for the integration, like presented above. In this section, some measurement results of the integrated magnetics within the 4Q flyback SICAM prototype from Section 9.3 will be presented.

Fig. 10.9 shows the voltage waveforms across the auxiliary power supply secondary-side winding and main secondary-side winding, in the case when only the auxiliary power supply primary-side winding is driven with rectangular voltage. It can be observed that this has almost no effect on the voltage induced in the main secondary-side winding, except for some oscillations which are likely minor resonance of the main winding leakage inductance with the oscilloscope probe parasitic capacitance.

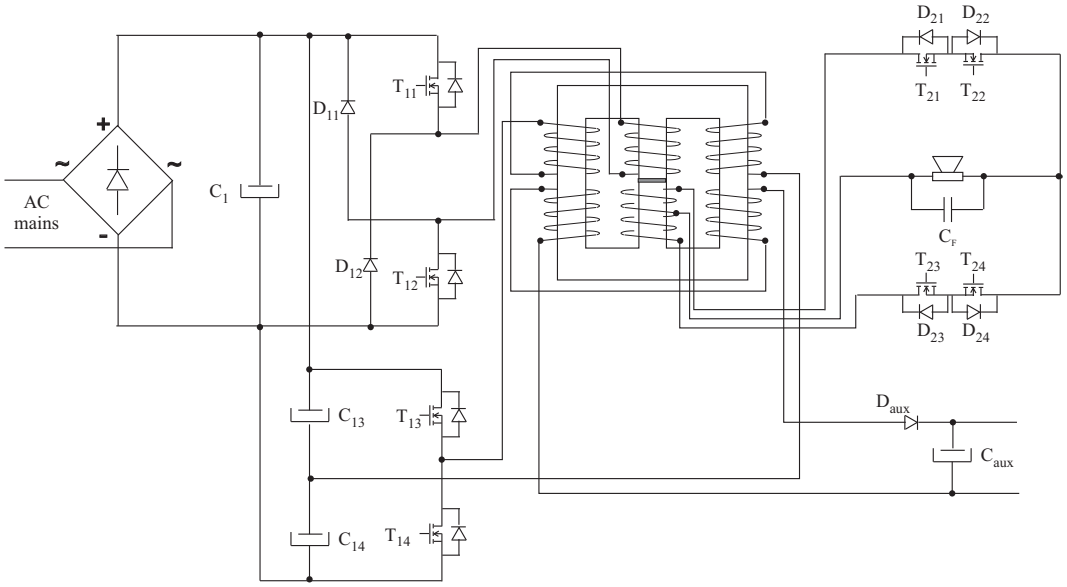

Fig. 10.5. 2-switch 4Q flyback SICAM with integrated magnetics for auxiliary power supplies

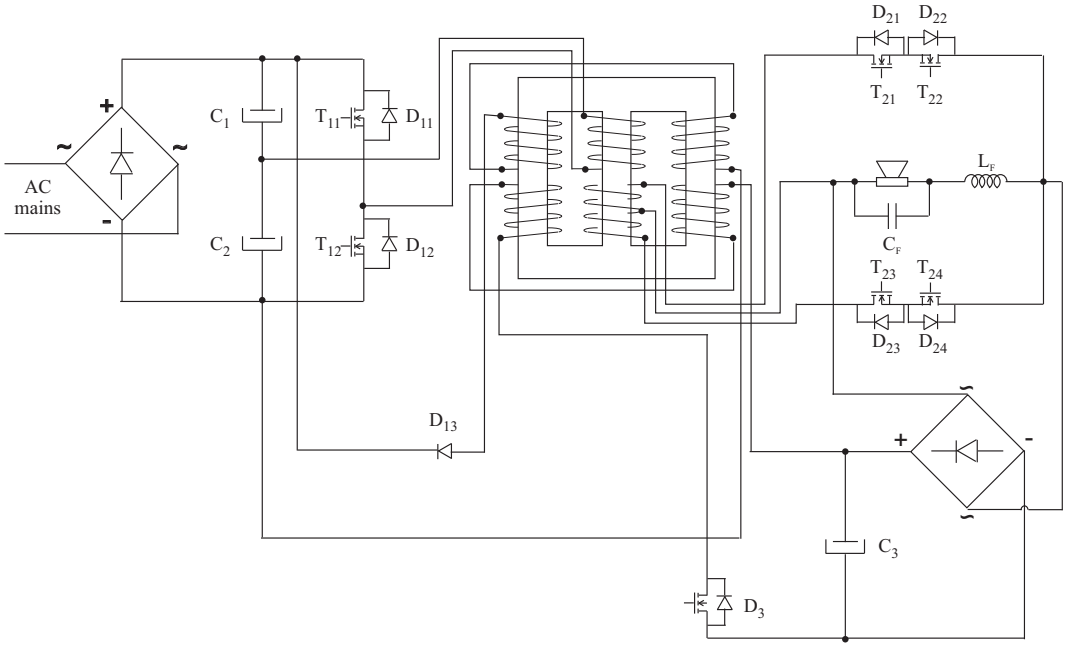

Fig. 10.6. SICAM with active capacitive voltage clamp using integrated magnetics

Fig. 10.10 shows the voltage waveforms across the auxiliary power supply secondary-side winding and main secondary-side winding, in the case when both the main primary-side winding and auxiliary power supply primary-side winding are driven with rectangular voltage. It is clear that now the operation of the main primary-side winding can be sensed in the slightly distorted rectangular voltage of the auxiliary power supply secondary-side winding, but nonetheless the operation of the auxiliary power supply is not being adversely affected.

10.3 Conclusion

In this chapter a new integrated magnetics design was proposed for SICAMs, where both magnetic components placed on a common three-leg core are entirely independent and do not share the same voltage waveforms. It is shown that decoupling of the integrated

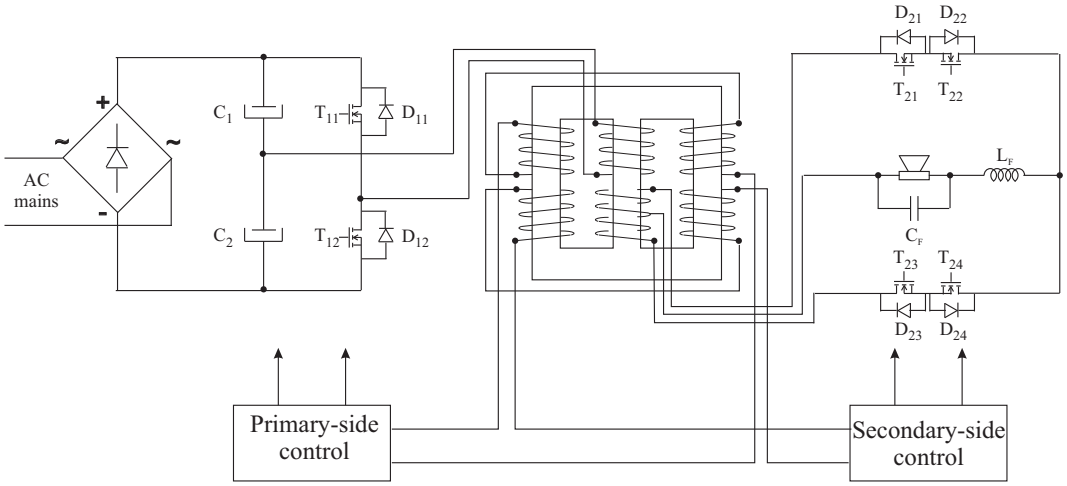

Fig. 10.7. SICAM with safe commutation and synchronization through integrated magnetics

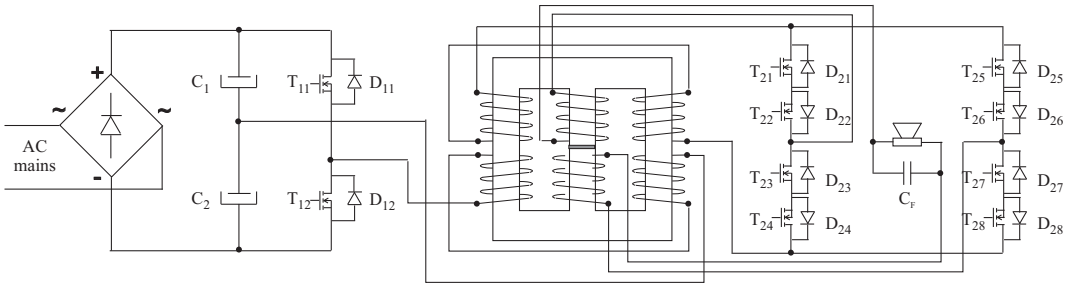

Fig. 10.8. SICAM with output filter inductor integrated on the main transformer

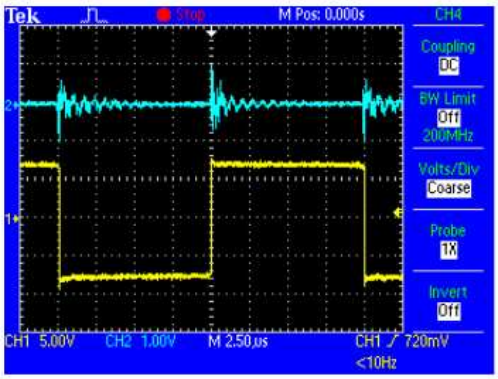

Fig. 10.9. Voltage waveforms across: 1) auxiliary power supply secondary-side winding (5 V/div), and 2) main secondary-side winding (1 V/div)

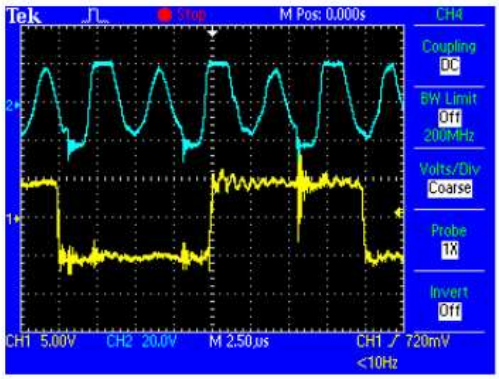

Fig. 10.10. Voltage waveforms across: 1) auxiliary power supply secondary-side winding (5 V/div), and 2) main secondary-side winding (20 V/div)

magnetic components is satisfactory even in the case of slight imbalance due to manufacturing and material tolerances, as long as the magnetic reluctances of the legs and the intentional air gaps are larger than the assembly asymmetries. SICAMs are complex power conversion systems which need many magnetic components for proper operation and they can significantly benefit from the proposed integrated magnetics concept.

11

General conclusion about SICAMs

This Ph.D. thesis defined the notion of SICAM - SIngle Converter stage AMplifier as a single-stage approach to building isolated and non-isolated audio power amplifiers. They strive for as direct energy conversion from the mains to the audio output as possible, by dedicating the operation and functions of the constitutive parts one to another. This in turn results in significant simplifications of the whole power conversion chain and topologies with lower reactive component count, but on behalf of using more fully controlled silicon components and complex control methods. This evolvement of the audio power amplification technology is justified by the ever increasing performance of the silicon power components, while the reactive components have reached the flat end of their development curve due to the natural limits of the dielectric and magnetic materials today.

The challenges in building both isolated and non-isolated SICAMs were clearly emphasized on several occasions.

In the non-isolated mains-connected case, the most natural way to follow is to use a simple full-bridge rectifier with a bulky energy storage capacitor to create a stiff DC-bus, and then use a high voltage Class D audio power amplifier. While this approach exhales in simplicity, the high input voltage creates several problems like decreased audio performance and using suboptimal switching power components with much higher blocking voltage than the output voltage. Therefore, the most interesting approach for the non-isolated mains-connected SICAMs is to use a voltage-step-down PFC front end, or even incorporating the step-down PFC functions as part of the full-bridge Class D amplifier by using the presented advanced control techniques.

In the non-isolated SICAMs for portable applications powered by batteries, the main challenge is to provide output voltage levels that are higher and lower, respectively, than the battery voltage, which is changing in a large range during the typical discharge cycle. It was concluded that in order to maintain the single-stage approach, it is necessary to build a buck-boost-type audio power amplifier with strongly nonlinear output characteristics. The presented digital precompensation control techniques provide a neat way for partial linearization of the aforementioned output characteristic even in open loop operation.

The most challenging task was however the development of isolated SICAMs, which are equally applicable to single and multichannel audio systems and feature high enough level of simplicity and innovation. For this application inspiration was found in HF-link power converters, well known from converters for alternative energy sources and uninterruptible power supplies (UPSs). Two main classes of isolated SICAMs were identified: isolated SICAMs with modulated and non-modulated transformer voltages. In the former, the PWM modulation of the transformer voltage is done with regard to one audio reference and therefore building a multichannel audio system requires using separate SICAM for each channel. Despite of some advantages like the much simplified load current commutation in the output stage, this approach was not investigated herein, partly due to the

large amount of patents in the area. SICAMs with non-modulated transformer voltages have the problem of reliable load current commutation in the output stage, but they are much more appealing for multichannel audio systems, where each additional channel can reuse the same input stage and transformer, thus adding to the product just the cost of a new output stage and slight overdimensioning of the preceding stages.

The main problem with the isolated SICAMs with non-modulated transformer voltages is the commutation of the load current in the output stage. This can be done either by using advanced safe-commutation switching sequences which turn on and off the bidirectional switches in the output stage in a prescribed manner, or by using dissipative and active clamping techniques. Both techniques have their own pros and cons which were clearly presented in the text. The safe-commutation switching technique is however preferred because there are no additional power components needed for performing the load current commutation. Several advanced control techniques for isolated SICAMs were presented as an improvement of the simplest PWM control technique, which take into consideration the specifics of the HF-link power conversion or even enable the use of safe-commutation switching techniques.

The simplest isolated SICAM can be obtained by reworking the simplest isolated DC power supply i.e. the flyback converter, by increasing its control bandwidth and adding bidirectional power capability. The obtained SICAM is essentially characterized by modulated transformer voltages, and all the filtering at the output is done with single capacitor. Due to the high component stress, the 4Q flyback SICAM is intended just for low-end and low power amplifiers.

Further simplifications in the practical implementation of the isolated SICAMs can be obtained by introducing integrated magnetics, which makes it possible to integrate two independent magnetic components on the same three-leg magnetic core. Several possible applications have been proposed in the thesis.

When compared to the conventional solution with separate SMPS and Class D amplifier, the proposed compact direct energy conversion switching-mode audio power amplifier i.e. SICAM introduces much simpler and much more compact power topology. Together with the promises of higher efficiency, less heatsinking material, less volume and board space, reduced number of reactive components and prospects for high-level integration, leading subsequently to lower cost, SICAM represents a highly competitive technology for the lower-end and cost-driven segment of the audio market.

A

Analysis of matrix SICAM

A.1 Time domain analysis of the two load combinations

During the operation of a matrix SICAM with LC-network there are two possible load combinations $L\|R$ and $C\|R$, shown in Fig. A.1b and c. The circuit combination where the LC-network is unloaded is not interesting, since it is characterized with large voltage and current stress of the resonant network.

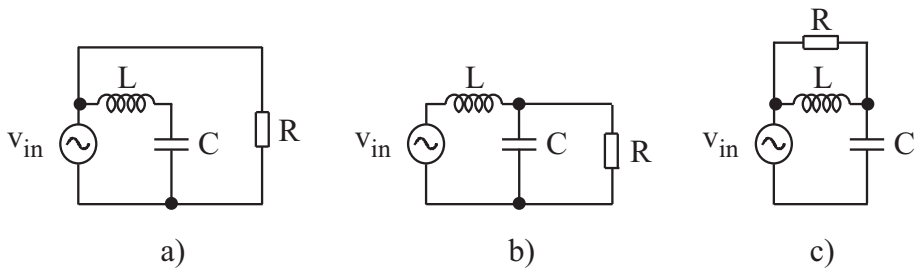

Fig. A.1. General topologies: a) $v_{in}\|R$, b) $L\|R$ and c) $C\|R$ (same as Fig. 2.25)

In the following the two aforementioned load combinations will be analyzed in time domain.

A.1.1 Time domain analysis of $C\|R$ combination

Voltage across the inductor L is given by:

$$v_L = L\frac{di_L}{dt} = v_{in} - v_C \tag{A.1}$$

which leads to the following expression for the inductor current first derivative:

$$\frac{di_L}{dt} = -\frac{1}{L}v_C + \frac{1}{L}v_{in} \tag{A.2}$$

Current through the capacitor C is given by:

$$i_C = C\frac{dv_C}{dt} = i_L - i_R = i_L - \frac{1}{R}v_C \tag{A.3}$$

which leads to the following expression for the capacitor voltage first derivative:

$$\frac{dv_C}{dt} = \frac{1}{C}i_L - \frac{1}{RC}v_C \tag{A.4}$$

After making another time derivation of (A.4):

$$\frac{d^2v_C}{dt^2} = \frac{1}{C}\frac{di_L}{dt} - \frac{1}{RC}\frac{dv_C}{dt} \tag{A.5}$$

and substituting the equation (A.2) for the first derivative of inductor current, the following second order differential equation is obtained:

$$\frac{d^2v_C}{dt^2} + \frac{1}{RC}\frac{dv_C}{dt} + \frac{1}{LC}v_C = \frac{1}{LC}v_{in} \tag{A.6}$$

Define the following angular frequencies:

$$\begin{aligned} \omega_R &= \tfrac{1}{RC} \\ \omega_L &= \tfrac{1}{\sqrt{LC}} \end{aligned} \tag{A.7}$$

Now the differential equation for the $C\|R$ case can be rewritten as following:

$$\frac{d^2v_C}{dt^2} + \omega_R\frac{dv_C}{dt} + \omega_L^2 v_C = \omega_L^2 v_{in} \tag{A.8}$$

Solution to the differential equation (A.8) can be found as a linear combination of the homogenous solution $v_{Ch} = v_{Ch}(t)$ when $v_{in}(t) \equiv 0$ and one particular solution $v_{Cp} = v_{Cp}(t)$ (for the sake of simplicity the time variable t is omitted):

$$v_C = v_{Ch} + v_{Cp} \tag{A.9}$$

Homogenous differential equation has the form:

$$\frac{d^2v_{Ch}}{dt^2} + \omega_R\frac{dv_{Ch}}{dt} + \omega_L^2 v_{Ch} = 0 \tag{A.10}$$

Using the Euler substitution of form $v_{Ch} = e^{st}$ the following quadratic equation is obtained:

$$s^2 + \omega_R s + \omega_L^2 = 0 \tag{A.11}$$

with solutions:

$$s_{1,2} = \frac{-\omega_R \pm \sqrt{\omega_R^2 - 4\omega_L^2}}{2} \tag{A.12}$$

and the time constants being:

$$\tau_{1,2} = \frac{1}{s_{1,2}} \tag{A.13}$$

Finally, homogenous solution has the form:

$$v_{Ch}(t) = A_C e^{s_1 t} + B_C e^{s_2 t} = A_C e^{\frac{t}{\tau_1}} + B_C e^{\frac{t}{\tau_2}} \tag{A.14}$$

where A_C and B_C represent constants, which can be determined from the differential equationś initial conditions. Index letter C in the constants is used to represent the $C\|R$ configuration.

Particular solution $v_{Cp} = v_{Cp}(t)$ is a solution to the following differential equation:

$$\frac{d^2v_{Cp}}{dt^2} + \omega_R\frac{dv_{Cp}}{dt} + \omega_L^2 v_{Cp} = \omega_L^2 v_{in} \tag{A.15}$$

Since the input has the form of a sine function:

$$v_{in}(t) = V_{in}\sin\omega_{in}t \tag{A.16}$$

the particular solution consists of both sine and cosine functions:

$$\begin{aligned} v_{Cp} &= D_C\sin\omega_{in}t + E_C\cos\omega_{in}t \\ \frac{dv_{Cp}}{dt} &= -\omega_{in}E_C\sin\omega_{in}t + \omega_{in}D_C\cos\omega_{in}t \\ \frac{d^2v_{Cp}}{dt^2} &= -\omega_{in}^2D_C\sin\omega_{in}t - \omega_{in}^2E_C\cos\omega_{in}t \end{aligned} \tag{A.17}$$

Substituting the v_{Ch} and its first two derivatives from (A.17) to (A.15) the following equation is obtained:

$$\begin{aligned} &(-\omega_{in}^2D_C - \omega_R\omega_{in}E_C + \omega_L^2D_C)\sin\omega_{in}t + (-\omega_{in}^2E_C + \omega_R\omega_{in}D_C + \omega_L^2E_C)\cos\omega_{in}t = \\ &\quad = \omega_L^2V_{in}\sin\omega_{in}t \end{aligned} \tag{A.18}$$

Comparing both sides of the equation (A.18), the following system of two equations for determining the unknown constants is obtained:

$$\begin{aligned} (\omega_L^2 - \omega_{in}^2)D_C - \omega_R\omega_{in}E_C &= \omega_L^2V_{in} \\ \omega_R\omega_{in}D_C + (\omega_L^2 - \omega_{in}^2)E_C &= 0 \end{aligned} \tag{A.19}$$

After expressing E_C from the second equation and substituting it in the first equation for determining D_C, the following expressions for the constants are obtained:

$$\begin{aligned} D_C &= \frac{\omega_L^2(\omega_L^2 - \omega_{in}^2)}{(\omega_L^2 - \omega_{in}^2)^2 + (\omega_R\omega_{in})^2}V_{in} \\ E_C &= -\frac{\omega_R\omega_L^2\omega_{in}}{(\omega_L^2 - \omega_{in}^2)^2 + (\omega_R\omega_{in})^2}V_{in} \end{aligned} \tag{A.20}$$

Complete solution (A.9) is like the following:

$$v_C(t) = A_Ce^{s_1t} + B_Ce^{s_2t} + D_C\sin\omega_{in}t + E_C\cos\omega_{in}t \tag{A.21}$$

Using the following initial conditions for the moment $t = 0$:

$$\begin{aligned} v_C(0) &= v_{C0} \\ \frac{dv_C(0)}{dt} &= \frac{dv_{C0}}{dt} \end{aligned} \tag{A.22}$$

the following linear system with two unknown constants A_C and B_C is obtained:

$$\begin{aligned} v_{C0} &= A_C + B_C + E_C \\ \frac{dv_{C0}}{dt} &= A_Cs_1 + B_Cs_2 + D_C\omega_{in} \end{aligned} \tag{A.23}$$

After expressing B_C from the first equation and substituting it in the second equation to determine A_C, the following expressions for the constants are obtained:

$$\begin{aligned} A_C &= \frac{-\frac{dv_{C0}}{dt} + v_{C0}s_2 - E_C s_1 + \omega_{in} D_C}{s_2 - s_1} \\ B_C &= \frac{\frac{dv_{C0}}{dt} - v_{C0}s_1 + E_C s_2 - \omega_{in} D_C}{s_2 - s_1} \end{aligned} \tag{A.24}$$

In the case of resonance $\omega_L = \omega_{in} = 1/\sqrt{LC}$ constants D_C and E_C become:

$$\begin{aligned} D_C &= 0 \\ E_C &= -\frac{\omega_{in}}{\omega_R} V_{in} \end{aligned} \tag{A.25}$$

A.1.2 Time domain analysis of $L\|R$ combination

Time domain analysis of $L\|R$ general topology follows the same path as in the $C\|R$ case.

Voltage across the inductor L is given by:

$$v_L = L\frac{di_L}{dt} = v_{in} - v_C \tag{A.26}$$

which leads to the following expression for the inductor current first derivative:

$$\frac{di_L}{dt} = -\frac{1}{L}v_C + \frac{1}{L}v_{in} \tag{A.27}$$

Current through the capacitor C is given by:

$$i_C = C\frac{dv_C}{dt} = i_L + i_R = i_L + \frac{1}{R}(v_{in} - v_C) \tag{A.28}$$

which leads to the following expression for the capacitor voltage first derivative:

$$\frac{dv_C}{dt} = \frac{1}{C}i_L - \frac{1}{RC}v_C + \frac{1}{RC}v_{in} \tag{A.29}$$

After making another time derivation of (A.29):

$$\frac{d^2v_C}{dt^2} = \frac{1}{C}\frac{di_L}{dt} - \frac{1}{RC}\frac{dv_C}{dt} + \frac{1}{RC}\frac{dv_{in}}{dt} \tag{A.30}$$

and substituting the equation (A.27) for the first derivative of inductor current, the following is obtained:

$$\frac{d^2v_C}{dt^2} + \frac{1}{RC}\frac{dv_C}{dt} + \frac{1}{LC}v_C = \frac{1}{LC}v_{in} + \frac{1}{RC}\frac{dv_{in}}{dt} \tag{A.31}$$

Using the angular frequencies defined in (A.7) the differential equation for the $L\|R$ case can be rewritten as following:

$$\frac{d^2v_C}{dt^2} + \omega_R\frac{dv_C}{dt} + \omega_L^2 v_C = \omega_L^2 v_{in} + \omega_R\frac{dv_{in}}{dt} \tag{A.32}$$

Solution to the differential equation (A.32) can be found as a linear combination of the homogenous solution $v_{Ch} = v_{Ch}(t)$ when $v_{in} \equiv 0$ and one particular solution $v_{Cp} = v_{Cp}(t)$ (for the sake of simplicity the time variable t is omitted):

$$v_C = v_{Ch} + v_{Cp} \tag{A.33}$$

Homogenous differential equation has the same form as in the $C\|R$ case:

$$\frac{d^2v_{Ch}}{dt^2} + \omega_R\frac{dv_{Ch}}{dt} + \omega_L^2 v_{Ch} = 0 \tag{A.34}$$

Using the Euler substitution of form $v_{Ch} = e^{st}$ the following quadratic equation is obtained:

$$s^2 + \omega_R s + \omega_L^2 = 0 \tag{A.35}$$

with the same solutions as in the $C\|R$ case:

$$s_{1,2} = \frac{-\omega_R \pm \sqrt{\omega_R^2 - 4\omega_L^2}}{2} \tag{A.36}$$

and the time constants being also the same:

$$\tau_{1,2} = \frac{1}{s_{1,2}} \tag{A.37}$$

Finally, homogenous solution has the form:

$$v_{Ch}(t) = A_L e^{s_1 t} + B_L e^{s_2 t} = A_L e^{\frac{t}{\tau_1}} + B_L e^{\frac{t}{\tau_2}} \tag{A.38}$$

where A_L and B_L represent constants, which can be determined from the differential equationś initial conditions. Index letter L in the constants is used to represent the $L\|R$ configuration.

Particular solution $v_{Cp} = v_{Cp}(t)$ is a solution to the following differential equation:

$$\frac{d^2v_{Cp}}{dt^2} + \omega_R\frac{dv_{Cp}}{dt} + \omega_L^2 v_{Cp} = \omega_L^2 v_{in} + \frac{1}{RC}\frac{dv_{in}}{dt} \tag{A.39}$$

Since the input has the form of a sine function and its first derivative as cosine function:

$$\begin{aligned} v_{in}(t) &= V_{in}\sin\omega_{in}t \\ \frac{dv_{in}(t)}{dt} &= \omega_{in}V_{in}\cos\omega_{in}t \end{aligned} \tag{A.40}$$

the particular solution is a combination of sine and cosine functions:

$$\begin{aligned} v_{Cp} &= D_L\sin\omega_{in}t + E_L\cos\omega_{in}t \\ \frac{dv_{Cp}}{dt} &= -\omega_{in}E_L\sin\omega_{in}t + \omega_{in}D_L\cos\omega_{in}t \\ \frac{d^2v_{Cp}}{dt^2} &= -\omega_{in}^2D_L\sin\omega_{in}t - \omega_{in}^2E_L\cos\omega_{in}t \end{aligned} \tag{A.41}$$

Substituting the v_{Ch} and its first two derivatives from (A.41) to (A.39) the following equation is obtained:

$$\begin{aligned} &(-\omega_{in}^2D_L - \omega_R\omega_{in}E_L + \omega_L^2D_L)\sin\omega_{in}t + (-\omega_{in}^2E_L + \omega_R\omega_{in}D_L + \omega_L^2E_L)\cos\omega_{in}t = \\ &= \omega_L^2V_{in}\sin\omega_{in}t + \omega_R\omega_{in}V_{in}\cos\omega_{in}t \end{aligned} \tag{A.42}$$

Comparing both sides of the equation (A.42), the following system of two equations for determining the unknown constants is obtained:

$$\begin{aligned}(\omega_L^2-\omega_{in}^2)D_L-\omega_R\omega_{in}E_L&=\omega_L^2V_{in}\\ \omega_R\omega_{in}D_L+(\omega_L^2-\omega_{in}^2)E_L&=\omega_R\omega_{in}V_{in}\end{aligned}\tag{A.43}$$

After expressing E_L from the second equation and substituting it in the first equation for determining D_L, the following expressions for the constants are obtained:

$$\begin{aligned}D_L&=\frac{\omega_L^2(\omega_L^2-\omega_{in}^2)+(\omega_R\omega_{in})^2}{(\omega_L^2-\omega_{in}^2)^2+(\omega_R\omega_{in})^2}V_{in}\\ E_L&=-\frac{\omega_R\omega_{in}^3}{(\omega_L^2-\omega_{in}^2)^2+(\omega_R\omega_{in})^2}V_{in}\end{aligned}\tag{A.44}$$

Complete solution (A.33) is like the following:

$$v_C(t)=A_Le^{s_1t}+B_Le^{s_2t}+D_L\sin\omega_{in}t+E_L\cos\omega_{in}t\tag{A.45}$$

Using the following initial conditions for the moment $t=0$:

$$\begin{aligned}v_C(0)&=v_{C0}\\ \frac{dv_C(0)}{dt}&=\frac{dv_{C0}}{dt}\end{aligned}\tag{A.46}$$

the following linear system with two unknown constants A_L and B_L is obtained:

$$\begin{aligned}v_{C0}&=A_L+B_L+E_L\\ \frac{dv_{C0}}{dt}&=A_Ls_1+B_Ls_2+D_L\omega_{in}\end{aligned}\tag{A.47}$$

After expressing B_L from the first equation and substituting it in the second equation to determine A_L, the following expressions for the constants are obtained:

$$\begin{aligned}A_L&=\frac{-\frac{dv_{C0}}{dt}+v_{C0}s_2-E_Ls_1+\omega_{in}D_L}{s_2-s_1}\\ B_L&=\frac{\frac{dv_{C0}}{dt}-v_{C0}s_1+E_Ls_2-\omega_{in}D_L}{s_2-s_1}\end{aligned}\tag{A.48}$$

In the case of resonance $\omega_L=\omega_{in}=1/\sqrt{LC}$ constants D_L and E_L become:

$$\begin{aligned}D_L&=V_{in}\\ E_L&=-\tfrac{\omega_{in}}{\omega_R}V_{in}\end{aligned}\tag{A.49}$$

A.2 State-space model of matrix SICAM

One can pursue a state-space approach to characterize each of the different possible configurations/topologies of the MC-based SICAM using an LC-network. Inductor current i_L and capacitor voltage v_C are chosen as state variables and output voltage v_{out} and input current i_{in} as output variables. The general form of state-space equations is:

$$\begin{aligned}\frac{d\mathbf{x}}{dt}&=\mathbf{A_i}\mathbf{x}+\mathbf{b_i}v_{in}\\ \mathbf{y}&=\mathbf{C_i}\mathbf{x}+\mathbf{d_i}v_{in}\end{aligned}\tag{A.50}$$

where $\mathbf{x}=[i_L\ v_C]^T$ is the state vector, $\mathbf{y}=[v_{out}\ i_{in}]^T$ is the output vector, $\mathbf{A_i}, \mathbf{b_i}, \mathbf{C_i}$ and $\mathbf{d_i}$ are the system matrix, the input vector, the output matrix and the input-to-output vector, i=2, -2, 1-2 or 2-1.

State-space equations

Exact equations for each of the cases are presented herein.

- $\boxed{2}$ corresponding to duty cycle d_2

$$\begin{aligned} L\frac{di_L}{dt} &= v_{in} - v_C \\ C\frac{dv_C}{dt} &= i_L - i_{out} = i_L - \frac{v_C}{R} \\ v_{out} &= v_C \\ i_{in} &= i_L \end{aligned} \tag{A.51}$$

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_C}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_{in} \tag{A.52}$$

$$\begin{bmatrix} v_{out} \\ i_{in} \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_{in} \tag{A.53}$$

So the system matrix $\mathbf{A_2}$, input vector $\mathbf{b_2}$, output matrix $\mathbf{C_2}$ and input-to-output vector $\mathbf{d_2}$ are:

$$\begin{aligned} \mathbf{A_2} &= \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \\ \mathbf{b_2} &= \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \\ \mathbf{C_2} &= \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \\ \mathbf{d_2} &= \begin{bmatrix} 0 \\ 0 \end{bmatrix} \end{aligned} \tag{A.54}$$

- $\boxed{\text{-}2}$ corresponding to duty cycle d_{-2}

$$\begin{aligned} L\frac{di_L}{dt} &= v_{in} - v_C \\ C\frac{dv_C}{dt} &= i_L + i_{out} = i_L - \frac{v_C}{R} \\ v_{out} &= -v_C \\ i_{in} &= i_L \end{aligned} \tag{A.55}$$

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_C}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_{in} \tag{A.56}$$

$$\begin{bmatrix} v_{out} \\ i_{in} \end{bmatrix} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_{in} \tag{A.57}$$

So the system matrix $\mathbf{A_{-2}}$, input vector $\mathbf{b_{-2}}$, output matrix $\mathbf{C_{-2}}$ and input-to-output vector $\mathbf{d_{-2}}$ are:

$$\begin{aligned}
\mathbf{A_{-2}} &= \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \\
\mathbf{b_{-2}} &= \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \\
\mathbf{C_{-2}} &= \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \\
\mathbf{d_{-2}} &= \begin{bmatrix} 0 \\ 0 \end{bmatrix}
\end{aligned} \tag{A.58}$$

- 1-2 corresponding to duty cycle d_{1-2}

$$\begin{aligned}
L\frac{di_L}{dt} &= v_{in} - v_C \\
C\frac{dv_C}{dt} &= i_L + i_{out} = i_L - \frac{v_C}{R} + \frac{v_{in}}{R} \\
v_{out} &= v_{in} - v_C \\
i_{in} &= i_L + i_{out} = i_L - \frac{v_C}{R} + \frac{v_{in}}{R}
\end{aligned} \tag{A.59}$$

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_C}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ \frac{1}{RC} \end{bmatrix} v_{in} \tag{A.60}$$

$$\begin{bmatrix} v_{out} \\ i_{in} \end{bmatrix} = \begin{bmatrix} 0 & -1 \\ 1 & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} 1 \\ \frac{1}{R} \end{bmatrix} v_{in} \tag{A.61}$$

So the system matrix $\mathbf{A_{1-2}}$, input vector $\mathbf{b_{1-2}}$, output matrix $\mathbf{C_{1-2}}$ and input-to-output vector $\mathbf{d_{1-2}}$ are:

$$\begin{aligned}
\mathbf{A_{1-2}} &= \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \\
\mathbf{b_{1-2}} &= \begin{bmatrix} \frac{1}{L} \\ \frac{1}{RC} \end{bmatrix} \\
\mathbf{C_{1-2}} &= \begin{bmatrix} 0 & -1 \\ 1 & -\frac{1}{R} \end{bmatrix} \\
\mathbf{d_{1-2}} &= \begin{bmatrix} 1 \\ \frac{1}{R} \end{bmatrix}
\end{aligned} \tag{A.62}$$

- 2-1 corresponding to duty cycle d_{2-1}

$$\begin{aligned}
L\frac{di_L}{dt} &= v_{in} - v_C \\
C\frac{dv_C}{dt} &= i_L - i_{out} = i_L - \frac{v_C}{R} + \frac{v_{in}}{R} \\
v_{out} &= v_C - v_{in} \\
i_{in} &= i_L - i_{out} = i_L - \frac{v_C}{R} + \frac{v_{in}}{R}
\end{aligned} \tag{A.63}$$

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_C}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ \frac{1}{RC} \end{bmatrix} v_{in} \tag{A.64}$$

$$\begin{bmatrix} v_{out} \\ i_{in} \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} -1 \\ \frac{1}{R} \end{bmatrix} v_{in} \tag{A.65}$$

So the system matrix $\mathbf{A_{2-1}}$, input vector $\mathbf{b_{2-1}}$, output matrix $\mathbf{C_{2-1}}$ and input-to-output vector $\mathbf{d_{2-1}}$ are:

$$\begin{aligned} \mathbf{A_{2-1}} &= \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \\ \mathbf{b_{1-2}} &= \begin{bmatrix} \frac{1}{L} \\ \frac{1}{RC} \end{bmatrix} \\ \mathbf{C_{2-1}} &= \begin{bmatrix} 0 & -1 \\ 1 & -\frac{1}{R} \end{bmatrix} \\ \mathbf{d_{2-1}} &= \begin{bmatrix} 1 \\ \frac{1}{R} \end{bmatrix} \end{aligned} \tag{A.66}$$

State-space averaging

Averaging of the state-space equations presented in the previous section during one switching interval T_s leads to filtering of the switching frequency harmonics [60]. Since the switching interval T_s is very small compared to the AC-mains voltage period $T_s \ll T_{in} = 1/50Hz = 20ms$, AC-mains input voltage v_{in} remains unaffected.

Averaged state-space equations can be written like the following:

$$\begin{aligned} \frac{d\mathbf{x}}{dt} &= (d_2\mathbf{A_2} + d_{-2}\mathbf{A_{-2}} + d_{1-2}\mathbf{A_{1-2}} + d_{2-1}\mathbf{A_{2-1}})\mathbf{x} \\ &\quad +(d_2\mathbf{b_2} + d_{-2}\mathbf{b_{-2}} + d_{1-2}\mathbf{b_{1-2}} + d_{2-1}\mathbf{b_{2-1}})v_{in} \\ \mathbf{y} &= (d_2\mathbf{C_2} + d_{-2}\mathbf{C_{-2}} + d_{1-2}\mathbf{C_{1-2}} + d_{2-1}\mathbf{C_{2-1}})\mathbf{x} \\ &\quad +(d_2\mathbf{d_2} + d_{-2}\mathbf{d_{-2}} + d_{1-2}\mathbf{d_{1-2}} + d_{2-1}\mathbf{d_{2-1}})v_{in} \end{aligned} \tag{A.67}$$

The averaged system matrix $\mathbf{A}$, the averaged input vector $\mathbf{b}$, the averaged output matrix $\mathbf{C}$ and the averaged input-to-output vector $\mathbf{d}$ are:

$$\begin{aligned} \mathbf{A} &= d_2\mathbf{A_2} + d_{-2}\mathbf{A_{-2}} + d_{1-2}\mathbf{A_{1-2}} + d_{2-1}\mathbf{A_{2-1}} \\ \mathbf{b} &= d_2\mathbf{b_2} + d_{-2}\mathbf{b_{-2}} + d_{1-2}\mathbf{b_{1-2}} + d_{2-1}\mathbf{b_{2-1}} \\ \mathbf{C} &= d_2\mathbf{C_2} + d_{-2}\mathbf{C_{-2}} + d_{1-2}\mathbf{C_{1-2}} + d_{2-1}\mathbf{C_{2-1}} \\ \mathbf{d} &= d_2\mathbf{d_2} + d_{-2}\mathbf{d_{-2}} + d_{1-2}\mathbf{d_{1-2}} + d_{2-1}\mathbf{d_{2-1}} \end{aligned} \tag{A.68}$$

Next step is to introduce small perturbations in all of the time variable quantities:

$$\begin{aligned} \mathbf{x} &= \bar{\mathbf{x}} + \tilde{\mathbf{x}} \\ \mathbf{y} &= \bar{\mathbf{y}} + \tilde{\mathbf{y}} \\ v_{in} &= \bar{v}_{in} + \tilde{v}_{in} \\ d_2 &= \bar{d}_2 + \tilde{d}_2 \\ d_{-2} &= \bar{d}_{-2} + \tilde{d}_{-2} \\ d_{1-2} &= \bar{d}_{1-2} + \tilde{d}_{1-2} \\ d_{2-1} &= \bar{d}_{2-1} + \tilde{d}_{2-1} \end{aligned} \tag{A.69}$$

where the bar ($^{-}$) over the quantities represents their stationary, operating point values and the tilde ($\tilde{}$) represents their perturbations.

It is worth pointing out that the operating point value of the input voltage $\bar{v}_{in}$ differs from one to another switching interval, but because of the high switching frequency it can be approximated with a constant value during a single switching interval T_s ($\bar{v}_{in}^k = V_{in} \sin(\omega_{in} k T_s)$ for the k-th switching interval).

When small perturbations are introduced in all of the quantities and all of the second order products of small perturbations are neglected, it is arrived at the following DC operating point mathematical model:

$$\begin{aligned} 0 &= \mathbf{A}\bar{\mathbf{x}} + \mathbf{b}\bar{v}_{in} \\ \bar{\mathbf{y}} &= \mathbf{C}\bar{\mathbf{x}} + \mathbf{d}\bar{v}_{in} \end{aligned} \tag{A.70}$$

and the following linearized AC small signal mathematical model:

$$\begin{aligned} \frac{d\tilde{\mathbf{x}}}{dt} &= \mathbf{A}\tilde{\mathbf{x}} + \mathbf{b}\tilde{v}_{in} + (\tilde{d}_2\mathbf{A_2} + \tilde{d}_{-2}\mathbf{A_{-2}} + \tilde{d}_{1-2}\mathbf{A_{1-2}} + \tilde{d}_{2-1}\mathbf{A_{2-1}})\bar{\mathbf{x}} + \\ &\quad + (\tilde{d}_2\mathbf{b_2} + \tilde{d}_{-2}\mathbf{b_{-2}} + \tilde{d}_{1-2}\mathbf{b_{1-2}} + \tilde{d}_{2-1}\mathbf{b_{2-1}})\bar{v}_{in} \\ \tilde{\mathbf{y}} &= \mathbf{C}\tilde{\mathbf{x}} + \mathbf{d}\tilde{v}_{in} + (\tilde{d}_2\mathbf{C_2} + \tilde{d}_{-2}\mathbf{C_{-2}} + \tilde{d}_{1-2}\mathbf{C_{1-2}} + \tilde{d}_{2-1}\mathbf{C_{2-1}})\bar{\mathbf{x}} + \\ &\quad + (\tilde{d}_2\mathbf{d_2} + \tilde{d}_{-2}\mathbf{d_{-2}} + \tilde{d}_{1-2}\mathbf{d_{1-2}} + \tilde{d}_{2-1}\tilde{\mathbf{d}}_{\mathbf{2-1}})\bar{v}_{in} \end{aligned} \tag{A.71}$$

Although this state-space averaging technique will not be investigated in detail any further and will not be used for developing the MC-based SICAM transfer functions, it is important for providing insight in the creation of the audio band output voltage. Even more, since the averaging is made in a short time interval T_s and the sine wave quantities with frequency equal to the AC-mains input voltage frequency remain intact, this averaging principle can be further extended to the sine waves maximum (max), root mean square (rms) and average (av) values.

B

Analysis of combined mains-connected Class D audio power amplifier and PFC

B.1 Analysis of combined Class D audio power amplifier and boost PFC

The analysis of operation of the combined Class D audio power amplifier with boost PFC front-end in Continuous Conduction Mode (CCM) through state-space averaging will be presented in this section. The four different connections in the operation of the combined Class D audio power amplifier and boost PFC are shown in Fig. B.1. Stepping through the different possible connections is performed according to the sign of the output voltage, and is shown in Fig. B.1 with the plus and minus sign.

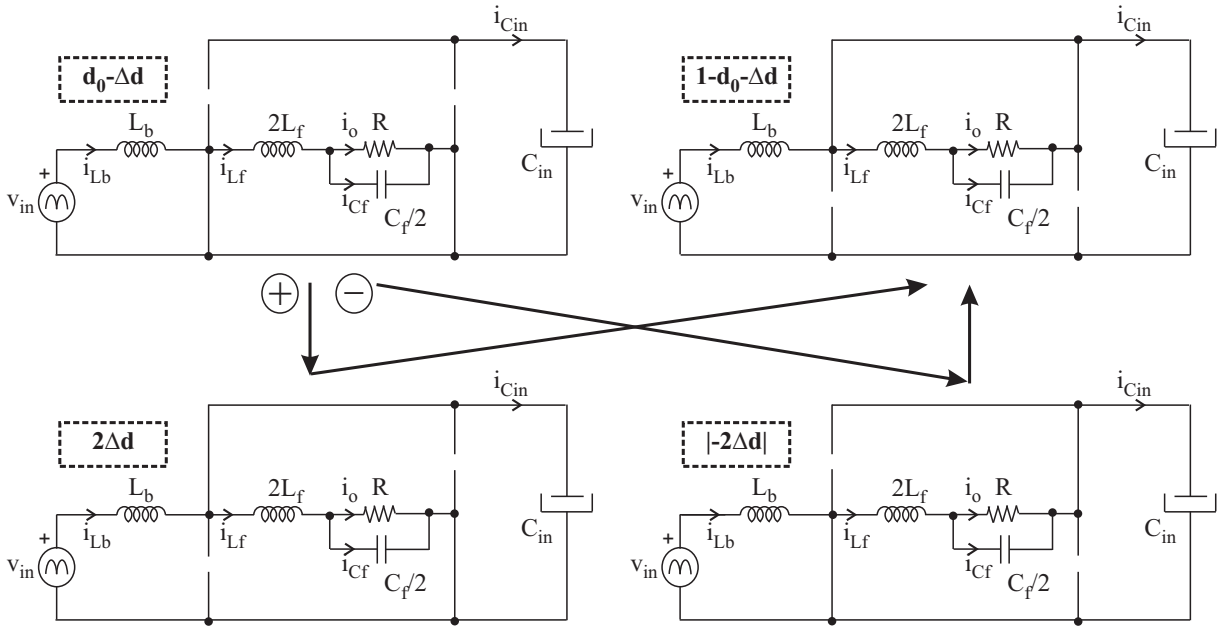

Fig. B.1. Possible connections in the combined Class D audio power amplifier and boost PFC (same as Fig. 3.9)

For positive output voltages:

- during interval $d_0 - \Delta d$:

$$\begin{aligned} L_b\frac{di_{Lb}}{dt} &= v_{in} \\ 2L_f\frac{di_{Lf}}{dt} &= -v_o \\ C_{in}\frac{dv_{Cin}}{dt} &= 0 \\ \frac{C_f}{2}\frac{dv_{Cf}}{dt} &= i_{Lf} - \frac{v_o}{R} \end{aligned} \tag{B.1}$$

i.e.:

$$\begin{aligned} \dot{i}_{Lb} &= \frac{1}{L_b}v_{in} \\ \dot{i}_{Lf} &= -\frac{1}{2L_f}v_o \\ \dot{v}_{Cin} &= 0 \\ \dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R}) \end{aligned} \tag{B.2}$$

- during interval $2\Delta d$:

$$\begin{aligned} L_b\frac{di_{Lb}}{dt} &= v_{in} - v_{Cin} \\ 2L_f\frac{di_{Lf}}{dt} &= v_{Cin} - v_o \\ C_{in}\frac{dv_{Cin}}{dt} &= i_{Lb} - i_{Lf} \\ \frac{C_f}{2}\frac{dv_{Cf}}{dt} &= i_{Lf} - \frac{v_o}{R} \end{aligned} \tag{B.3}$$

i.e.:

$$\begin{aligned} \dot{i}_{Lb} &= \frac{1}{L_b}(v_{in} - v_{Cin}) \\ \dot{i}_{Lf} &= \frac{1}{2L_f}(v_{Cin} - v_o) \\ \dot{v}_{Cin} &= \frac{1}{C_{in}}(i_{Lb} - i_{Lf}) \\ \dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R}) \end{aligned} \tag{B.4}$$

- during interval $1 - d_0 - \Delta d$:

$$\begin{aligned} L_b\frac{di_{Lb}}{dt} &= v_{in} - v_{Cin} \\ 2L_f\frac{di_{Lf}}{dt} &= -v_o \\ C_{in}\frac{dv_{Cin}}{dt} &= i_{Lb} \\ \frac{C_f}{2}\frac{dv_{Cf}}{dt} &= i_{Lf} - \frac{v_o}{R} \end{aligned} \tag{B.5}$$

i.e.:

$$\begin{aligned}
\dot{i}_{Lb} &= \frac{1}{L_b}(v_{in} - v_{Cin}) \\
\dot{i}_{Lf} &= -\frac{1}{2L_f}v_o \\
\dot{v}_{Cin} &= \frac{1}{C_{in}}i_{Lb} \\
\dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R})
\end{aligned} \tag{B.6}$$

For negative output voltages, only the time interval in the middle is different from the positive output voltage:

- during interval $|-2\Delta d|$:

$$\begin{aligned}
L_b\frac{di_{Lb}}{dt} &= v_{in} \\
2L_f\frac{di_{Lf}}{dt} &= -v_{Cin} - v_o \\
C_{in}\frac{dv_{Cin}}{dt} &= i_{Lf} \\
\frac{C_f}{2}\frac{dv_{Cf}}{dt} &= i_{Lf} - \frac{v_o}{R}
\end{aligned} \tag{B.7}$$

i.e.:

$$\begin{aligned}
\dot{i}_{Lb} &= \frac{1}{L_b}v_{in} \\
\dot{i}_{Lf} &= -\frac{1}{2L_f}(v_{Cin} + v_o) \\
\dot{v}_{Cin} &= \frac{1}{C_{in}}i_{Lf} \\
\dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R})
\end{aligned} \tag{B.8}$$

In the next step, averaging of the state-space equations is performed to remove the switching harmonics present in the waveforms and reveal the low frequency content. For the positive output voltages this corresponds to summing up equations (B.2), (B.4) and (B.6) weighted by their respective duty cycles:

$$\begin{aligned}
\dot{i}_{Lb} &= \frac{v_{in}}{L_b} - (1 - d_0 + \Delta d)\frac{v_{Cin}}{L_b} \\
\dot{i}_{Lf} &= -\frac{v_o}{2L_f} + \frac{2\Delta d v_{Cin}}{2L_f} \\
\dot{v}_{Cin} &= (1 - d_o + \Delta d)\frac{i_{Lb}}{C_{in}} - \frac{2\Delta d i_{Lf}}{C_{in}} \\
\dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R})
\end{aligned} \tag{B.9}$$

where all the states are represented by their average values.

For the negative output voltages averaging corresponds to summing up equations (B.2), (B.8) and (B.6) weighted by their respective duty cycles:

$$\begin{aligned}
\dot{i}_{Lb} &= \frac{v_{in}}{L_b} - (1 - d_0 - \Delta d)\frac{v_{Cin}}{L_b} \\
\dot{i}_{Lf} &= -\frac{v_o}{2L_f} - \frac{2\Delta d v_{Cin}}{2L_f} \\
\dot{v}_{Cin} &= (1 - d_o - \Delta d)\frac{i_{Lb}}{C_{in}} + \frac{2\Delta d i_{Lf}}{C_{in}} \\
\dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R})
\end{aligned} \tag{B.10}$$

where all the states are again represented by their average values.

Perturbations are subsequently added to each state to perform linearization of the model around the operating point, so that each of the states become $X + \tilde{x}$, where X represents the operating point and $\tilde{x}$ is a small perturbation around the operating point. It is assumed that all cross-products of the perturbation are so small, so they can be easily neglected without significant adverse impact on the accuracy.

For positive output voltages, the perturbed average model becomes:

$$\begin{aligned}
\dot{\tilde{i}}_{Lb} &= \big[\frac{V_{in}}{L_b} - (1 - D_0 + \Delta D)\frac{V_{Cin}}{L_b}\big] + \big[\frac{\tilde{v}_{in}}{L_b} - \frac{(1 - D_0 + \Delta D)\tilde{v}_{Cin} - (\tilde{d}_0 - \Delta\tilde{d})V_{Cin}}{L_b}\big] \\
\dot{\tilde{i}}_{Lf} &= \big[-\frac{V_o}{2L_f} + \frac{2\Delta D V_{Cin}}{2L_f}\big] + \big[-\frac{\tilde{v}_o}{2L_f} + \frac{2\Delta D\tilde{v}_{Cin} + 2\Delta\tilde{d}V_{Cin}}{2L_f}\big] \\
\dot{\tilde{v}}_{Cin} &= \big[(1 - D_o + \Delta D)\frac{I_{Lb}}{C_{in}} - \frac{2\Delta D I_{Lf}}{C_{in}}\big] + \\
&\quad + \big[\frac{(1 - D_0 + \Delta D)\tilde{i}_{Lb} - (\tilde{d}_0 - \Delta\tilde{d})I_{Lb}}{C_{in}} - \frac{2\Delta D\tilde{i}_{Lf} + 2\Delta\tilde{d}I_{Lf}}{C_{in}}\big] \\
\dot{\tilde{v}}_{Cf} &= \big[\frac{2}{C_f}(I_{Lf} - \frac{V_o}{R})\big] + \big[\frac{2}{C_f}(\tilde{i}_{Lf} - \frac{\tilde{v}_o}{R})\big]
\end{aligned} \tag{B.11}$$

and for negative output voltages:

$$\begin{aligned}
\dot{\tilde{i}}_{Lb} &= \big[\frac{V_{in}}{L_b} - (1 - D_0 - \Delta D)\frac{V_{Cin}}{L_b}\big] + \big[\frac{\tilde{v}_{in}}{L_b} - \frac{(1 - D_0 - \Delta D)\tilde{v}_{Cin} - (\tilde{d}_0 + \Delta\tilde{d})V_{Cin}}{L_b}\big] \\
\dot{\tilde{i}}_{Lf} &= \big[-\frac{V_o}{2L_f} - \frac{2\Delta D V_{Cin}}{2L_f}\big] + \big[-\frac{\tilde{v}_o}{2L_f} - \frac{2\Delta D\tilde{v}_{Cin} + 2\Delta\tilde{d}V_{Cin}}{2L_f}\big] \\
\dot{\tilde{v}}_{Cin} &= \big[(1 - D_o - \Delta D)\frac{I_{Lb}}{C_{in}} + \frac{2\Delta D I_{Lf}}{C_{in}}\big] + \\
&\quad + \big[\frac{(1 - D_0 - \Delta D)\tilde{i}_{Lb} - (\tilde{d}_0 + \Delta\tilde{d})I_{Lb}}{C_{in}} + \frac{2\Delta D\tilde{i}_{Lf} + 2\Delta\tilde{d}I_{Lf}}{C_{in}}\big] \\
\dot{\tilde{v}}_{Cf} &= \big[\frac{2}{C_f}(I_{Lf} - \frac{V_o}{R})\big] + \big[\frac{2}{C_f}(\tilde{i}_{Lf} - \frac{\tilde{v}_o}{R})\big]
\end{aligned} \tag{B.12}$$

DC-model of the combined Class D audio power amplifier and boost PFC is obtained by equating the DC quantities on both sides of (B.11) for positive output voltages:

$$\begin{aligned}
0 &= V_{in} - (1 - D_0 + \Delta D)V_{Cin} && \Rightarrow && V_{Cin} = \frac{V_{in}}{1 - D_0 + \Delta D} \\
0 &= -V_o + 2\Delta D V_{Cin} && \Rightarrow && V_o = 2\Delta D V_{Cin} \\
0 &= (1 - D_0 + \Delta D)I_{Lb} - 2\Delta D I_{Lf} && \Rightarrow && I_{Lb} = \frac{2\Delta D I_{Lf}}{1 - D_0 + \Delta D} \\
0 &= I_{Lf} - \frac{V_o}{R} && \Rightarrow && I_{Lf} = \frac{V_o}{R} = I_o
\end{aligned} \tag{B.13}$$

and (B.11) for negative output voltages:

$$\begin{aligned}
0 &= V_{in} - (1 - D_0 - \Delta D)V_{Cin} && \Rightarrow && V_{Cin} = \frac{V_{in}}{1 - D_0 - \Delta D} \\
0 &= V_o + 2\Delta D V_{Cin} && \Rightarrow && V_o = -2\Delta D V_{Cin} \\
0 &= (1 - D_0 - \Delta D)I_{Lb} + 2\Delta D I_{Lf} && \Rightarrow && I_{Lb} = -\frac{2\Delta D I_{Lf}}{1 - D_0 - \Delta D} \\
0 &= I_{Lf} - \frac{V_o}{R} && \Rightarrow && I_{Lf} = \frac{V_o}{R} = I_o
\end{aligned} \tag{B.14}$$

AC-model of the combined Class D audio power amplifier and boost PFC is obtained by equating the AC quantities on both sides of (B.11) for positive output voltages:

$$\begin{aligned}
\dot{i}_{Lb} &= \frac{v_{in}}{L_b} - \frac{(1 - D_0 + \Delta D)v_{Cin} - (d_0 - \Delta d)V_{Cin}}{L_b} \\
\dot{i}_{Lf} &= -\frac{v_o}{2L_f} + \frac{2\Delta D v_{Cin} + 2\Delta d V_{Cin}}{2L_f} \\
\dot{v}_{Cin} &= \frac{(1 - D_0 + \Delta D)i_{Lb} - (d_0 - \Delta d)I_{Lb}}{C_{in}} - \frac{2\Delta D i_{Lf} + 2\Delta d I_{Lf}}{C_{in}} \\
\dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R})
\end{aligned} \tag{B.15}$$

and (B.11) for negative output voltages:

$$\begin{aligned}
\dot{i}_{Lb} &= \frac{v_{in}}{L_b} - \frac{(1 - D_0 - \Delta D)v_{Cin} - (d_0 + \Delta d)V_{Cin}}{L_b} \\
\dot{i}_{Lf} &= -\frac{v_o}{2L_f} - \frac{2\Delta D v_{Cin} + 2\Delta d V_{Cin}}{2L_f} \\
\dot{v}_{Cin} &= \frac{(1 - D_0 - \Delta D)i_{Lb} - (d_0 + \Delta d)I_{Lb}}{C_{in}} + \frac{2\Delta D i_{Lf} + 2\Delta d I_{Lf}}{C_{in}} \\
\dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R})
\end{aligned} \tag{B.16}$$

where $\sim$ is omitted for brevity.

AC small-signal model for positive output voltages (B.15) can be rewritten in the following state-space form:

$$\frac{d}{dt}\begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\dfrac{1-D_0+\Delta D}{L_b} & 0 \\ 0 & 0 & \dfrac{\Delta D}{L_f} & -\dfrac{1}{2L_f} \\ \dfrac{1-D_0+\Delta D}{C_{in}} & -\dfrac{2\Delta D}{C_{in}} & 0 & 0 \\ 0 & \dfrac{2}{C_f} & 0 & -\dfrac{2}{RC_f} \end{bmatrix} \cdot \begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} +$$

$$+ \begin{bmatrix} \dfrac{1}{L_b} & \dfrac{V_{Cin}}{L_b} & -\dfrac{V_{Cin}}{L_b} \\ 0 & 0 & \dfrac{V_{Cin}}{L_f} \\ 0 & -\dfrac{I_{Lb}}{C_{in}} & \dfrac{I_{Lb}-2I_{Lf}}{C_{in}} \\ 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ d_0 \\ \Delta d \end{bmatrix}$$

$$\begin{bmatrix} i_{in} \\ v_{Cin} \\ v_o \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} + 0 \cdot \begin{bmatrix} v_{in} \\ d_0 \\ \Delta d \end{bmatrix} \tag{B.17}$$

So the system matrix $\mathbf{A_{b+}}$, input matrix $\mathbf{B_{b+}}$, output matrix $\mathbf{C_{b+}}$ and input-to-output matrix $\mathbf{D_{b+}}$ are:

$$\mathbf{A_{b+}} = \begin{bmatrix} 0 & 0 & -\dfrac{1-D_0+\Delta D}{L_b} & 0 \\ 0 & 0 & \dfrac{\Delta D}{L_f} & -\dfrac{1}{2L_f} \\ \dfrac{1-D_0+\Delta D}{C_{in}} & -\dfrac{2\Delta D}{C_{in}} & 0 & 0 \\ 0 & \dfrac{2}{C_f} & 0 & -\dfrac{2}{RC_f} \end{bmatrix}$$

$$\mathbf{B_{b+}} = \begin{bmatrix} \dfrac{1}{L_b} & \dfrac{V_{Cin}}{L_b} & -\dfrac{V_{Cin}}{L_b} \\ 0 & 0 & \dfrac{V_{Cin}}{L_f} \\ 0 & -\dfrac{I_{Lb}}{C_{in}} & \dfrac{I_{Lb}-2I_{Lf}}{C_{in}} \\ 0 & 0 & 0 \end{bmatrix} \tag{B.18}$$

$$\mathbf{C_{b+}} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

$$\mathbf{D_{b+}} = 0$$

The desired output quantities for the state-space representation are the input current i_{in}, DC-bus capacitor voltage v_{Cin} and output voltage v_o, being equal to the boost inductor current i_{Lf}, DC-bus capacitor voltage v_{Cin} and filter capacitor voltage v_{Cf} as system states, correspondingly.

AC small-signal model for negative output voltages (B.16) can be rewritten in the following state-space form:

$$\begin{aligned}
\frac{d}{dt}\begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} &= \begin{bmatrix} 0 & 0 & -\dfrac{1-D_0-\Delta D}{L_b} & 0 \\ 0 & 0 & -\dfrac{\Delta D}{L_f} & -\dfrac{1}{2L_f} \\ \dfrac{1-D_0-\Delta D}{C_{in}} & \dfrac{2\Delta D}{C_{in}} & 0 & 0 \\ 0 & \dfrac{2}{C_f} & 0 & -\dfrac{2}{RC_f} \end{bmatrix} \cdot \begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} + \\
&+ \begin{bmatrix} \dfrac{1}{L_b} & \dfrac{V_{Cin}}{L_b} & -\dfrac{V_{Cin}}{L_b} \\ 0 & 0 & -\dfrac{V_{Cin}}{L_f} \\ 0 & -\dfrac{I_{Lb}}{C_{in}} & \dfrac{2I_{Lf}-I_{Lb}}{C_{in}} \\ 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ d_0 \\ \Delta d \end{bmatrix} \\
\begin{bmatrix} i_{in} \\ v_{Cin} \\ v_o \end{bmatrix} &= \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} + 0 \cdot \begin{bmatrix} v_{in} \\ d_0 \\ \Delta d \end{bmatrix}
\end{aligned} \tag{B.19}$$

So the system matrix $\mathbf{A_{b-}}$, input matrix $\mathbf{B_{b-}}$, output matrix $\mathbf{C_{b-}}$ and input-to-output matrix $\mathbf{D_{b-}}$ are:

$$\begin{aligned}
\mathbf{A_{b-}} &= \begin{bmatrix} 0 & 0 & -\dfrac{1-D_0-\Delta D}{L_b} & 0 \\ 0 & 0 & -\dfrac{\Delta D}{L_f} & -\dfrac{1}{2L_f} \\ \dfrac{1-D_0-\Delta D}{C_{in}} & \dfrac{2\Delta D}{C_{in}} & 0 & 0 \\ 0 & \dfrac{2}{C_f} & 0 & -\dfrac{2}{RC_f} \end{bmatrix} \\
\mathbf{B_{b-}} &= \begin{bmatrix} \dfrac{1}{L_b} & \dfrac{V_{Cin}}{L_b} & -\dfrac{V_{Cin}}{L_b} \\ 0 & 0 & -\dfrac{V_{Cin}}{L_f} \\ 0 & -\dfrac{I_{Lb}}{C_{in}} & \dfrac{2I_{Lf}-I_{Lb}}{C_{in}} \\ 0 & 0 & 0 \end{bmatrix} \\
\mathbf{C_{b-}} &= \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \\
\mathbf{D_{b-}} &= 0
\end{aligned} \tag{B.20}$$

System matrices in (B.18) and (B.20) can be used to develop small-signal transfer functions for positive and negative output voltages by recognizing that:

$$\begin{bmatrix} i_{in} \\ v_{Cin} \\ v_o \end{bmatrix} = \left[\mathbf{C_{b+}}(s\mathbf{I} - \mathbf{A_{b+}})^{-1}\mathbf{B_{b+}} + \mathbf{D_{b+}}\right] \cdot \begin{bmatrix} v_{in} \\ d_0 \\ \Delta d \end{bmatrix} = \\ = \begin{bmatrix} G_{i_{in}v_{in},b+}(s) & G_{i_{in}d_0,b+}(s) & G_{i_{in}\Delta d,b+}(s) \\ G_{v_{Cin}v_{in},b+}(s) & G_{v_{Cin}d_0,b+}(s) & G_{v_{Cin}\Delta d,b+}(s) \\ G_{v_ov_{in},b+}(s) & G_{v_od_0,b+}(s) & G_{v_o\Delta d,b+}(s) \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ d_0 \\ \Delta d \end{bmatrix} \tag{B.21}$$

and:

$$\begin{bmatrix} i_{in} \\ v_{Cin} \\ v_o \end{bmatrix} = \left[\mathbf{C_{b-}}(s\mathbf{I} - \mathbf{A_{b-}})^{-1}\mathbf{B_{b-}} + \mathbf{D_{b-}}\right] \cdot \begin{bmatrix} v_{in} \\ d_0 \\ \Delta d \end{bmatrix} = \\ = \begin{bmatrix} G_{i_{in}v_{in},b-}(s) & G_{i_{in}d_0,b-}(s) & G_{i_{in}\Delta d,b-}(s) \\ G_{v_{Cin}v_{in},b-}(s) & G_{v_{Cin}d_0,b-}(s) & G_{v_{Cin}\Delta d,b-}(s) \\ G_{v_ov_{in},b-}(s) & G_{v_od_0,b-}(s) & G_{v_o\Delta d,b-}(s) \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ d_0 \\ \Delta d \end{bmatrix} \tag{B.22}$$

B.2 Analysis of the synchronous operation of the combined Class D audio power amplifier and buck-boost PFC

The analysis of the synchronous operation of combined Class D audio power amplifier and buck-boost PFC front-end in CCM through state-space averaging will be presented in this section. The four different connections in the operation of the combined Class D audio power amplifier and buck-boost PFC are shown in Fig. B.2. Stepping through the different possible connections is performed according to the sign of the output voltage, and is shown in Fig. B.2 with the plus and minus sign.

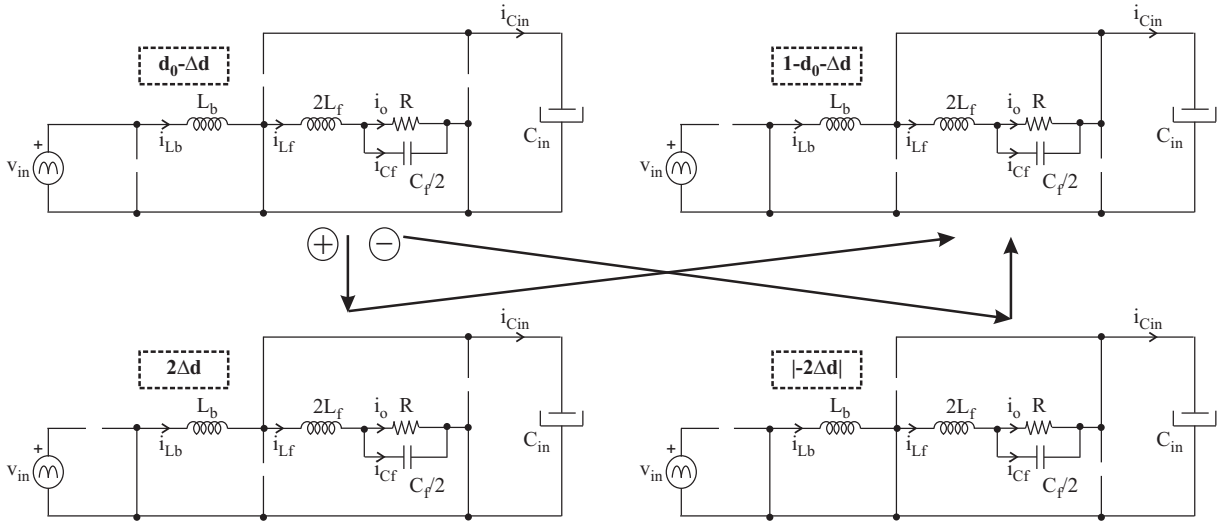

Fig. B.2. Possible connections in the synchronously-operated combined Class D audio power amplifier and buck-boost PFC (same as Fig. 3.14)

For positive output voltages:

- during interval $d_0 - \Delta d$:

$$\begin{aligned} L_b\frac{di_{Lb}}{dt} &= v_{in} \\ 2L_f\frac{di_{Lf}}{dt} &= -v_o \\ C_{in}\frac{dv_{Cin}}{dt} &= 0 \\ \frac{C_f}{2}\frac{dv_{Cf}}{dt} &= i_{Lf} - \frac{v_o}{R} \end{aligned} \tag{B.23}$$

i.e.:

$$\begin{aligned} \dot{i}_{Lb} &= \frac{1}{L_b}v_{in} \\ \dot{i}_{Lf} &= -\frac{1}{2L_f}v_o \\ \dot{v}_{Cin} &= 0 \\ \dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R}) \end{aligned} \tag{B.24}$$

- during interval $2\Delta d$:

$$\begin{aligned} L_b\frac{di_{Lb}}{dt} &= -v_{Cin} \\ 2L_f\frac{di_{Lf}}{dt} &= v_{Cin} - v_o \\ C_{in}\frac{dv_{Cin}}{dt} &= i_{Lb} - i_{Lf} \\ \frac{C_f}{2}\frac{dv_{Cf}}{dt} &= i_{Lf} - \frac{v_o}{R} \end{aligned} \tag{B.25}$$

i.e.:

$$\begin{aligned} \dot{i}_{Lb} &= -\frac{1}{L_b}v_{Cin} \\ \dot{i}_{Lf} &= \frac{1}{2L_f}(v_{Cin} - v_o) \\ \dot{v}_{Cin} &= \frac{1}{C_{in}}(i_{Lb} - i_{Lf}) \\ \dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R}) \end{aligned} \tag{B.26}$$

- during interval $1 - d_0 - \Delta d$:

$$\begin{aligned} L_b\frac{di_{Lb}}{dt} &= -v_{Cin} \\ 2L_f\frac{di_{Lf}}{dt} &= -v_o \\ C_{in}\frac{dv_{Cin}}{dt} &= i_{Lb} \\ \frac{C_f}{2}\frac{dv_{Cf}}{dt} &= i_{Lf} - \frac{v_o}{R} \end{aligned} \tag{B.27}$$

i.e.:

$$\begin{aligned}
\dot{i}_{Lb} &= -\frac{1}{L_b} v_{Cin} \\
\dot{i}_{Lf} &= -\frac{1}{2L_f} v_o \\
\dot{v}_{Cin} &= \frac{1}{C_{in}} i_{Lb} \\
\dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R})
\end{aligned} \tag{B.28}$$

For negative output voltages, only the time interval in the middle is different from the positive output voltage:

- during interval $|-2\Delta d|$:

$$\begin{aligned}
L_b \frac{di_{Lb}}{dt} &= 0 \\
2L_f \frac{di_{Lf}}{dt} &= -v_{Cin} - v_o \\
C_{in} \frac{dv_{Cin}}{dt} &= i_{Lf} \\
\frac{C_f}{2} \frac{dv_{Cf}}{dt} &= i_{Lf} - \frac{v_o}{R}
\end{aligned} \tag{B.29}$$

i.e.:

$$\begin{aligned}
\dot{i}_{Lb} &= 0 \\
\dot{i}_{Lf} &= -\frac{1}{2L_f}(v_{Cin} + v_o) \\
\dot{v}_{Cin} &= \frac{1}{C_{in}} i_{Lf} \\
\dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R})
\end{aligned} \tag{B.30}$$

In the next step, averaging of the state-space equations is performed to remove the switching harmonics present in the waveforms and reveal the low frequency content. For the positive output voltages this corresponds to summing up equations (B.24), (B.26) and (B.28) weighted by their respective duty cycles:

$$\begin{aligned}
\dot{i}_{Lb} &= (d_0 - \Delta d)\frac{v_{in}}{L_b} - (1 - d_0 + \Delta d)\frac{v_{Cin}}{L_b} \\
\dot{i}_{Lf} &= -\frac{v_o}{2L_f} + \frac{2\Delta d v_{Cin}}{2L_f} \\
\dot{v}_{Cin} &= (1 - d_o + \Delta d)\frac{i_{Lb}}{C_{in}} - \frac{2\Delta d i_{Lf}}{C_{in}} \\
\dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R})
\end{aligned} \tag{B.31}$$

where all the states are represented by their average values.

For the negative output voltages averaging corresponds to summing up equations (B.24), (B.30) and (B.28) weighted by their respective duty cycles:

$$\begin{aligned}
\dot{i}_{Lb} &= (d_0 - \Delta d)\frac{v_{in}}{L_b} - (1 - d_0 - \Delta d)\frac{v_{Cin}}{L_b} \\
\dot{i}_{Lf} &= -\frac{v_o}{2L_f} - \frac{2\Delta d v_{Cin}}{2L_f} \\
\dot{v}_{Cin} &= (1 - d_o - \Delta d)\frac{i_{Lb}}{C_{in}} + \frac{2\Delta d i_{Lf}}{C_{in}} \\
\dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R})
\end{aligned} \tag{B.32}$$

where all the states are again represented by their average values.

Perturbations are subsequently added to each state to perform linearization of the model around the operating point, so that each of the states become $X + \tilde{x}$, where X represents the operating point and $\tilde{x}$ is a small perturbation around the operating point. It is assumed that all cross-products of the perturbation are so small, so they can be easily neglected without significant adverse impact on the accuracy.

For positive output voltages, the perturbed average model becomes:

$$\begin{aligned}
\dot{\tilde{i}}_{Lb} &= \big[\frac{(D_0 - \Delta D)V_{in}}{L_b} - (1 - D_0 + \Delta D)\frac{V_{Cin}}{L_b}\big] + \\
&\quad + \big[\frac{(D_0 - \Delta D)\tilde{v}_{in} + (\tilde{d}_0 - \Delta\tilde{d})V_{in}}{L_b} - \frac{(1 - D_0 + \Delta D)\tilde{v}_{Cin} - (\tilde{d}_0 - \Delta\tilde{d})V_{Cin}}{L_b}\big] \\
\dot{\tilde{i}}_{Lf} &= \big[-\frac{V_o}{2L_f} + \frac{2\Delta D V_{Cin}}{2L_f}\big] + \big[-\frac{\tilde{v}_o}{2L_f} + \frac{2\Delta D\tilde{v}_{Cin} + 2\Delta\tilde{d}V_{Cin}}{2L_f}\big] \\
\dot{\tilde{v}}_{Cin} &= \big[(1 - D_o + \Delta D)\frac{I_{Lb}}{C_{in}} - \frac{2\Delta D I_{Lf}}{C_{in}}\big] + \\
&\quad + \big[\frac{(1 - D_0 + \Delta D)\tilde{i}_{Lb} - (\tilde{d}_0 - \Delta\tilde{d})I_{Lb}}{C_{in}} - \frac{2\Delta D\tilde{i}_{Lf} + 2\Delta\tilde{d}I_{Lf}}{C_{in}}\big] \\
\dot{\tilde{v}}_{Cf} &= \big[\frac{2}{C_f}(I_{Lf} - \frac{V_o}{R})\big] + \big[\frac{2}{C_f}(\tilde{i}_{Lf} - \frac{\tilde{v}_o}{R})\big]
\end{aligned} \tag{B.33}$$

and for negative output voltages:

$$\begin{aligned}
\dot{\tilde{i}}_{Lb} &= \big[(D_0 - \Delta D)\frac{V_{in}}{L_b} - (1 - D_0 - \Delta D)\frac{V_{Cin}}{L_b}\big] + \\
&\quad + \big[\frac{(D_0 - \Delta D)\tilde{v}_{in} + (\tilde{d}_0 - \Delta\tilde{d})V_{in}}{L_b} - \frac{(1 - D_0 - \Delta D)\tilde{v}_{Cin} - (\tilde{d}_0 + \Delta\tilde{d})V_{Cin}}{L_b}\big] \\
\dot{\tilde{i}}_{Lf} &= \big[-\frac{V_o}{2L_f} - \frac{2\Delta D V_{Cin}}{2L_f}\big] + \big[-\frac{\tilde{v}_o}{2L_f} - \frac{2\Delta D\tilde{v}_{Cin} + 2\Delta\tilde{d}V_{Cin}}{2L_f}\big] \\
\dot{\tilde{v}}_{Cin} &= \big[(1 - D_o - \Delta D)\frac{I_{Lb}}{C_{in}} + \frac{2\Delta D I_{Lf}}{C_{in}}\big] + \\
&\quad + \big[\frac{(1 - D_0 - \Delta D)\tilde{i}_{Lb} - (\tilde{d}_0 - \Delta\tilde{d})I_{Lb}}{C_{in}} + \frac{2\Delta D\tilde{i}_{Lf} + 2\Delta\tilde{d}I_{Lf}}{C_{in}}\big] \\
\dot{\tilde{v}}_{Cf} &= \big[\frac{2}{C_f}(I_{Lf} - \frac{V_o}{R})\big] + \big[\frac{2}{C_f}(\tilde{i}_{Lf} - \frac{\tilde{v}_o}{R})\big]
\end{aligned} \tag{B.34}$$

DC-model of the combined Class D audio power amplifier and buck-boost PFC is obtained by equating the DC quantities on both sides of (B.33) for positive output voltages:

$$\begin{aligned}
0 &= (D_0 - \Delta D)V_{in} - (1 - D_0 + \Delta D)V_{Cin} \quad &\Rightarrow \quad V_{Cin} &= \frac{(D_0 - \Delta D)V_{in}}{1 - D_0 + \Delta D} \\
0 &= -V_o + 2\Delta D V_{Cin} \quad &\Rightarrow \quad V_o &= 2\Delta D V_{Cin} \\
0 &= (1 - D_0 + \Delta D)I_{Lb} - 2\Delta D I_{Lf} \quad &\Rightarrow \quad I_{Lb} &= \frac{2\Delta D I_{Lf}}{1 - D_0 + \Delta D} \\
0 &= I_{Lf} - \frac{V_o}{R} \quad &\Rightarrow \quad I_{Lf} &= \frac{V_o}{R} = I_o
\end{aligned} \tag{B.35}$$

and (B.11) for negative output voltages:

$$\begin{aligned}
0 &= (D_0 - \Delta D)V_{in} - (1 - D_0 - \Delta D)V_{Cin} \quad &\Rightarrow \quad V_{Cin} &= \frac{(D_0 - \Delta D)V_{in}}{1 - D_0 - \Delta D} \\
0 &= V_o + 2\Delta D V_{Cin} \quad &\Rightarrow \quad V_o &= -2\Delta D V_{in} \\
0 &= (1 - D_0 - \Delta D)I_{Lb} + 2\Delta D I_{Lf} \quad &\Rightarrow \quad I_{Lb} &= -\frac{2\Delta D I_{Lf}}{1 - D_0 - \Delta D} \\
0 &= I_{Lf} - \frac{V_o}{R} \quad &\Rightarrow \quad I_{Lf} &= \frac{V_o}{R} = I_o
\end{aligned} \tag{B.36}$$

AC-model of the combined Class D audio power amplifier and buck-boost PFC is obtained by equating the AC quantities on both sides of (B.33) for positive output voltages:

$$\begin{aligned}
\dot{i}_{Lb} &= \frac{(D_0 - \Delta D)v_{in} + (d_0 - \Delta d)V_{in}}{L_b} - \frac{(1 - D_0 + \Delta D)v_{Cin} - (d_0 - \Delta d)V_{Cin}}{L_b} \\
\dot{i}_{Lf} &= -\frac{v_o}{2L_f} + \frac{2\Delta D v_{Cin} + 2\Delta d V_{Cin}}{2L_f} \\
\dot{v}_{Cin} &= \frac{(1 - D_0 + \Delta D)i_{Lb} - (d_0 - \Delta d)I_{Lb}}{C_{in}} - \frac{2\Delta D i_{Lf} + 2\Delta d I_{Lf}}{C_{in}} \\
\dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R})
\end{aligned} \tag{B.37}$$

and (B.33) for negative output voltages:

$$\begin{aligned}
\dot{i}_{Lb} &= \frac{(D_0 - \Delta D)v_{in} + (d_0 - \Delta d)V_{in}}{L_b} - \frac{(1 - D_0 - \Delta D)v_{Cin} - (d_0 + \Delta d)V_{Cin}}{L_b} \\
\dot{i}_{Lf} &= -\frac{v_o}{2L_f} - \frac{2\Delta D v_{Cin} + 2\Delta d V_{Cin}}{2L_f} \\
\dot{v}_{Cin} &= \frac{(1 - D_0 - \Delta D)i_{Lb} - (d_0 - \Delta d)I_{Lb}}{C_{in}} + \frac{2\Delta D i_{Lf} + 2\Delta d I_{Lf}}{C_{in}} \\
\dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R})
\end{aligned} \tag{B.38}$$

where $\sim$ is omitted for brevity.

The desired output quantities for the state-space representation are the input current i_{in}, DC-bus capacitor voltage v_{Cin} and output voltage v_o, where v_{Cin} and v_o are readily available and are equal to the state quantities v_{Cin} and v_{Cf}, while the DC and AC value of the input current are:

$$I_{in} = (D_0 - \Delta D)I_{Lb} \tag{B.39}$$

and

$$i_{in} = (D_0 - \Delta D)i_{Lb} + (d_0 - \Delta d)I_{Lb} \tag{B.40}$$

AC small-signal model for positive output voltages (B.37) can be rewritten in the following state-space form:

$$\frac{d}{dt}\begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\dfrac{1-D_0+\Delta D}{L_b} & 0 \\ 0 & 0 & \dfrac{\Delta D}{L_f} & -\dfrac{1}{2L_f} \\ \dfrac{1-D_0+\Delta D}{C_{in}} & -\dfrac{2\Delta D}{C_{in}} & 0 & 0 \\ 0 & \dfrac{2}{C_f} & 0 & -\dfrac{2}{RC_f} \end{bmatrix} \cdot \begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} +$$

$$+ \begin{bmatrix} \dfrac{D_0-\Delta D}{L_b} & \dfrac{V_{in}+V_{Cin}}{L_b} & -\dfrac{V_{in}+V_{Cin}}{L_b} \\ 0 & 0 & \dfrac{V_{Cin}}{L_f} \\ 0 & -\dfrac{I_{Lb}}{C_{in}} & \dfrac{I_{Lb}-2I_{Lf}}{C_{in}} \\ 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ d_0 \\ \Delta d \end{bmatrix}$$

$$\begin{bmatrix} i_{in} \\ v_{Cin} \\ v_o \end{bmatrix} = \begin{bmatrix} (D_0-\Delta D) & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} +$$

$$+ \begin{bmatrix} 0 & I_{Lb} & -I_{Lb} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ d_0 \\ \Delta d \end{bmatrix} \tag{B.41}$$

So the system matrix $\mathbf{A_{bb+}}$, input matrix $\mathbf{B_{bb+}}$, output matrix $\mathbf{C_{bb+}}$ and input-to-output matrix $\mathbf{D_{bb+}}$ are:

$$\begin{aligned}
\mathbf{A_{bb+}} &= \begin{bmatrix} 0 & 0 & -\dfrac{1-D_0+\Delta D}{L_b} & 0 \\ 0 & 0 & \dfrac{\Delta D}{L_f} & -\dfrac{1}{2L_f} \\ \dfrac{1-D_0+\Delta D}{C_{in}} & -\dfrac{2\Delta D}{C_{in}} & 0 & 0 \\ 0 & \dfrac{2}{C_f} & 0 & -\dfrac{2}{RC_f} \end{bmatrix} \\
\mathbf{B_{bb+}} &= \begin{bmatrix} \dfrac{D_0-\Delta D}{L_b} & \dfrac{V_{in}+V_{Cin}}{L_b} & -\dfrac{V_{in}+V_{Cin}}{L_b} \\ 0 & 0 & \dfrac{V_{Cin}}{L_f} \\ 0 & -\dfrac{I_{Lb}}{C_{in}} & \dfrac{I_{Lb}-2I_{Lf}}{C_{in}} \\ 0 & 0 & 0 \end{bmatrix} \\
\mathbf{C_{bb+}} &= \begin{bmatrix} (D_0-\Delta D) & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \\
\mathbf{D_{bb+}} &= \begin{bmatrix} 0 & I_{Lb} & -I_{Lb} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}
\end{aligned} \tag{B.42}$$

AC small-signal model for negative output voltages (B.38) can be rewritten in the following state-space form:

$$\begin{aligned}
\frac{d}{dt}\begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} &= \begin{bmatrix} 0 & 0 & -\dfrac{1-D_0-\Delta D}{L_b} & 0 \\ 0 & 0 & -\dfrac{\Delta D}{L_f} & -\dfrac{1}{2L_f} \\ \dfrac{1-D_0-\Delta D}{C_{in}} & \dfrac{2\Delta D}{C_{in}} & 0 & 0 \\ 0 & \dfrac{2}{C_f} & 0 & -\dfrac{2}{RC_f} \end{bmatrix} \cdot \begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} + \\
&+ \begin{bmatrix} \dfrac{D_0-\Delta D}{L_b} & \dfrac{V_{in}+V_{Cin}}{L_b} & -\dfrac{V_{in}+V_{Cin}}{L_b} \\ 0 & 0 & -\dfrac{V_{Cin}}{L_f} \\ 0 & -\dfrac{I_{Lb}}{C_{in}} & \dfrac{I_{Lb}+2I_{Lf}}{C_{in}} \\ 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ d_0 \\ \Delta d \end{bmatrix} \\
\begin{bmatrix} i_{in} \\ v_{Cin} \\ v_o \end{bmatrix} &= \begin{bmatrix} (D_0-\Delta D) & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} + \\
&+ \begin{bmatrix} 0 & I_{Lb} & -I_{Lb} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ d_0 \\ \Delta d \end{bmatrix}
\end{aligned} \tag{B.43}$$

So the system matrix $\mathbf{A_{bb-}}$, input matrix $\mathbf{B_{bb-}}$, output matrix $\mathbf{C_{bb-}}$ and input-to-output matrix $\mathbf{D_{bb-}}$ are:

$$\begin{aligned}
\mathbf{A_{bb-}} &= \begin{bmatrix} 0 & 0 & -\dfrac{1-D_0-\Delta D}{L_b} & 0 \\ 0 & 0 & -\dfrac{\Delta D}{L_f} & -\dfrac{1}{2L_f} \\ \dfrac{1-D_0-\Delta D}{C_{in}} & \dfrac{2\Delta D}{C_{in}} & 0 & 0 \\ 0 & \dfrac{2}{C_f} & 0 & -\dfrac{2}{RC_f} \end{bmatrix} \\
\mathbf{B_{bb-}} &= \begin{bmatrix} \dfrac{D_0-\Delta D}{L_b} & \dfrac{V_{in}+V_{Cin}}{L_b} & -\dfrac{V_{in}+V_{Cin}}{L_b} \\ 0 & 0 & -\dfrac{V_{Cin}}{L_f} \\ 0 & -\dfrac{I_{Lb}}{C_{in}} & \dfrac{I_{Lb}+2I_{Lf}}{C_{in}} \\ 0 & 0 & 0 \end{bmatrix} \\
\mathbf{C_{bb-}} &= \begin{bmatrix} (D_0-\Delta D) & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \\
\mathbf{D_{bb-}} &= \begin{bmatrix} 0 & I_{Lb} & -I_{Lb} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}
\end{aligned} \tag{B.44}$$

The differences in the models for positive and negative output voltages stem from the fact that the buck-boost PFC is asymmetrical in regard with the full-bridge Class D audio power amplifier and this translates to slight changes in the models. Like in the case of a combined Class D audio power amplifier and boost PFC, this asymmetry can be alleviated by having two buck-boost inductors, connected to the middle points of the switching totem poles.

System matrices in (B.42) and (B.44) can be used to develop small-signal transfer functions for positive and negative output voltages by recognizing that:

$$\begin{aligned}
\begin{bmatrix} i_{in} \\ v_{Cin} \\ v_o \end{bmatrix} &= \left[\mathbf{C_{bb+}}(s\mathbf{I}-\mathbf{A_{bb+}})^{-1}\mathbf{B_{bb+}}+\mathbf{D_{bb+}}\right]\cdot\begin{bmatrix} v_{in} \\ d_0 \\ \Delta d \end{bmatrix} = \\
&= \begin{bmatrix} G_{i_{in}v_{in},bb+}(s) & G_{i_{in}d_0,bb+}(s) & G_{i_{in}\Delta d,bb+}(s) \\ G_{v_{Cin}v_{in},bb+}(s) & G_{v_{Cin}d_0,bb+}(s) & G_{v_{Cin}\Delta d,bb+}(s) \\ G_{v_ov_{in},bb+}(s) & G_{v_od_0,bb+}(s) & G_{v_o\Delta d,bb+}(s) \end{bmatrix}\cdot\begin{bmatrix} v_{in} \\ d_0 \\ \Delta d \end{bmatrix}
\end{aligned} \tag{B.45}$$

and:

$$\begin{aligned}
\begin{bmatrix} i_{in} \\ v_{Cin} \\ v_o \end{bmatrix} &= \left[\mathbf{C_{bb-}}(s\mathbf{I}-\mathbf{A_{bb-}})^{-1}\mathbf{B_{bb-}}+\mathbf{D_{bb-}}\right]\cdot\begin{bmatrix} v_{in} \\ d_0 \\ \Delta d \end{bmatrix} = \\
&= \begin{bmatrix} G_{i_{in}v_{in},bb-}(s) & G_{i_{in}d_0,bb-}(s) & G_{i_{in}\Delta d,bb-}(s) \\ G_{v_{Cin}v_{in},bb-}(s) & G_{v_{Cin}d_0,bb-}(s) & G_{v_{Cin}\Delta d,bb-}(s) \\ G_{v_ov_{in},bb-}(s) & G_{v_od_0,bb-}(s) & G_{v_o\Delta d,bb-}(s) \end{bmatrix}\cdot\begin{bmatrix} v_{in} \\ d_0 \\ \Delta d \end{bmatrix}
\end{aligned} \tag{B.46}$$

B.3 Analysis of the asynchronous operation of the combined Class D audio power amplifier and buck-boost PFC

The analysis of the asynchronous operation of combined Class D audio power amplifier and buck-boost PFC front-end in CCM through state-space averaging will be performed using the connection diagrams in Fig. B.3. In this mode of operation there is one additional degree of freedom in the freely selectable duty cycle of the active rectifier d_a. Depending on the duration of this duty cycle d_a compared to the corresponding duty cycles of the Class D audio power amplifier, there are six possible switching sequences, three for each polarity of the output voltage. These are explained in Table B.1, where the duration of each switching combination from Fig. B.3 is given in parenthesis.

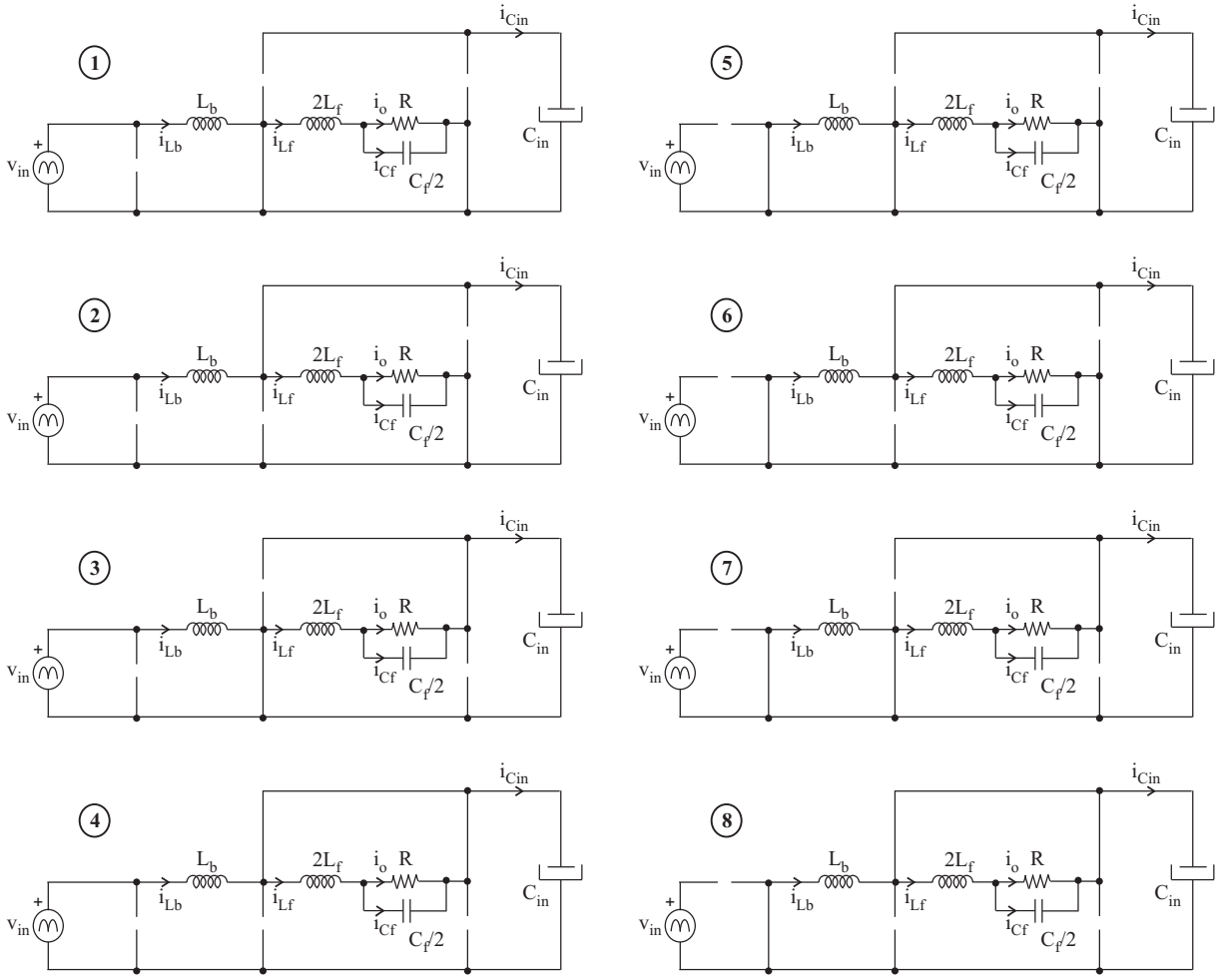

Fig. B.3. Possible connections in the asynchronously-operated combined Class D audio power amplifier and buck-boost PFC (same as Fig. 3.15)

The state-space equations for each of the switching combinations in Fig. 3.15 are:

- combination 1:

Positive output voltage				
$I = d_a < (d_0 - \Delta d)$	**1** (d_a)	**5** $(d_0 - \Delta d - d_a)$	**6** $(2\Delta d)$	**8** $(1 - d_0 - \Delta d)$
$II = (d_0 - \Delta d) < d_a < (d_0 + \Delta d)$	**1** $(d_0 - \Delta d)$	**2** $(d_a - d_0 + \Delta d)$	**6** $(d_0 + \Delta d - d_a)$	**8** $(1 - d_0 - \Delta d)$
$III = (d_0 + \Delta d) < d_a < 1$	**1** $(d_0 - \Delta d)$	**2** $(2\Delta d)$	**4** $(d_a - d_0 - \Delta d)$	**8** $(1 - d_a)$
Negative output voltage				
$IV = d_a < (d_0 - \Delta d)$	**1** (d_a)	**5** $(d_0 - \Delta d - d_a)$	**7** $(2\Delta d)$	**8** $(1 - d_0 - \Delta d)$
$V = (d_0 - \Delta d) < d_a < (d_0 + \Delta d)$	**1** $(d_0 - \Delta d)$	**3** $(d_a - d_0 + \Delta d)$	**7** $(d_0 + \Delta d - d_a)$	**8** $(1 - d_0 - \Delta d)$
$VI = (d_0 + \Delta d) < d_a < 1$	**1** $(d_0 - \Delta d)$	**3** $(2\Delta d)$	**4** $(d_a - d_0 - \Delta d)$	**8** $(1 - d_a)$

Table B.1. Switching sequences of the asynchronously-operated combined Class D audio power amplifier and buck-boost PFC

$$\begin{aligned} \dot{i}_{Lb} &= \frac{1}{L_b} v_{in} \\ \dot{i}_{Lf} &= -\frac{1}{2L_f} v_o \\ \dot{v}_{Cin} &= 0 \\ \dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R}) \end{aligned} \tag{B.47}$$

- combination 2:

$$\begin{aligned} \dot{i}_{Lb} &= \frac{1}{L_b}(v_{in} - v_{Cin}) \\ \dot{i}_{Lf} &= \frac{1}{2L_f}(v_{Cin} - v_o) \\ \dot{v}_{Cin} &= \frac{1}{C_{in}}(i_{Lb} - i_{Lf}) \\ \dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R}) \end{aligned} \tag{B.48}$$

- combination 3:

$$\begin{aligned} \dot{i}_{Lb} &= \frac{1}{L_b}(v_{in} - v_{Cin}) \\ \dot{i}_{Lf} &= -\frac{1}{2L_f}(v_{Cin} + v_o) \\ \dot{v}_{Cin} &= \frac{1}{C_{in}} i_{Lf} \\ \dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R}) \end{aligned} \tag{B.49}$$

- combination 4:

$$\begin{aligned} \dot{i}_{Lb} &= \frac{1}{L_b}(v_{in} - v_{Cin}) \\ \dot{i}_{Lf} &= -\frac{1}{2L_f} v_o \\ \dot{v}_{Cin} &= \frac{1}{C_{in}} i_{Lb} \\ \dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R}) \end{aligned} \tag{B.50}$$

- combination 5:

$$\begin{aligned}
\dot{i}_{Lb} &= 0 \\
\dot{i}_{Lf} &= -\frac{1}{2L_f} v_o \\
\dot{v}_{Cin} &= 0 \\
\dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R})
\end{aligned} \tag{B.51}$$

- combination 6:

$$\begin{aligned}
\dot{i}_{Lb} &= -\frac{1}{L_b} v_{Cin} \\
\dot{i}_{Lf} &= \frac{1}{2L_f}(v_{Cin} - v_o) \\
\dot{v}_{Cin} &= \frac{1}{C_{in}}(i_{Lb} - i_{Lf}) \\
\dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R})
\end{aligned} \tag{B.52}$$

- combination 7:

$$\begin{aligned}
\dot{i}_{Lb} &= 0 \\
\dot{i}_{Lf} &= -\frac{1}{2L_f}(v_{Cin} + v_o) \\
\dot{v}_{Cin} &= \frac{1}{C_{in}} i_{Lf} \\
\dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R})
\end{aligned} \tag{B.53}$$

- combination 8:

$$\begin{aligned}
\dot{i}_{Lb} &= -\frac{1}{L_b} v_{Cin} \\
\dot{i}_{Lf} &= -\frac{1}{2L_f} v_o \\
\dot{v}_{Cin} &= \frac{1}{C_{in}} i_{Lb} \\
\dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R})
\end{aligned} \tag{B.54}$$

In the next step, averaging of the state-space equations is performed to remove the switching harmonics present in the waveforms and reveal the low frequency content. This is done by taking into account the duration of each of the switching combinations 1-8 in the switching sequences $I - VI$ given in Table B.1:

- sequence I:

$$\begin{aligned}
\dot{i}_{Lb} &= d_a \frac{v_{in}}{L_b} - (1 - d_0 + \Delta d)\frac{v_{Cin}}{L_b} \\
\dot{i}_{Lf} &= -\frac{v_o}{2L_f} + \frac{2\Delta d v_{Cin}}{2L_f} \\
\dot{v}_{Cin} &= (1 - d_o + \Delta d)\frac{i_{Lb}}{C_{in}} - \frac{2\Delta d i_{Lf}}{C_{in}} \\
\dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R})
\end{aligned} \tag{B.55}$$

- sequence II:

$$\begin{aligned}
\dot{i}_{Lb} &= d_a\frac{v_{in}}{L_b} - (1 - d_0 + \Delta d)\frac{v_{Cin}}{L_b} \\
\dot{i}_{Lf} &= -\frac{v_o}{2L_f} + \frac{2\Delta d v_{Cin}}{2L_f} \\
\dot{v}_{Cin} &= (1 - d_o + \Delta d)\frac{i_{Lb}}{C_{in}} - \frac{2\Delta d i_{Lf}}{C_{in}} \\
\dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R})
\end{aligned} \tag{B.56}$$

- sequence III:

$$\begin{aligned}
\dot{i}_{Lb} &= d_a\frac{v_{in}}{L_b} - (1 - d_0 + \Delta d)\frac{v_{Cin}}{L_b} \\
\dot{i}_{Lf} &= -\frac{v_o}{2L_f} + \frac{2\Delta d v_{Cin}}{2L_f} \\
\dot{v}_{Cin} &= (1 - d_o + \Delta d)\frac{i_{Lb}}{C_{in}} - \frac{2\Delta d i_{Lf}}{C_{in}} \\
\dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R})
\end{aligned} \tag{B.57}$$

- sequence IV:

$$\begin{aligned}
\dot{i}_{Lb} &= d_a\frac{v_{in}}{L_b} - (1 - d_0 - \Delta d)\frac{v_{Cin}}{L_b} \\
\dot{i}_{Lf} &= -\frac{v_o}{2L_f} - \frac{2\Delta d v_{Cin}}{2L_f} \\
\dot{v}_{Cin} &= (1 - d_o - \Delta d)\frac{i_{Lb}}{C_{in}} + \frac{2\Delta d i_{Lf}}{C_{in}} \\
\dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R})
\end{aligned} \tag{B.58}$$

- sequence V:

$$\begin{aligned}
\dot{i}_{Lb} &= d_a\frac{v_{in}}{L_b} - (1 + d_a - 2d_0)\frac{v_{Cin}}{L_b} \\
\dot{i}_{Lf} &= -\frac{v_o}{2L_f} - \frac{2\Delta d v_{Cin}}{2L_f} \\
\dot{v}_{Cin} &= (1 - d_o - \Delta d)\frac{i_{Lb}}{C_{in}} + \frac{2\Delta d i_{Lf}}{C_{in}} \\
\dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R})
\end{aligned} \tag{B.59}$$

- sequence VI:

$$\begin{aligned}
\dot{i}_{Lb} &= d_a\frac{v_{in}}{L_b} - (1 - d_0 + \Delta d)\frac{v_{Cin}}{L_b} \\
\dot{i}_{Lf} &= -\frac{v_o}{2L_f} - \frac{2\Delta d v_{Cin}}{2L_f} \\
\dot{v}_{Cin} &= (1 - d_o - \Delta d)\frac{i_{Lb}}{C_{in}} + \frac{2\Delta d i_{Lf}}{C_{in}} \\
\dot{v}_{Cf} &= \frac{2}{C_f}(i_{Lf} - \frac{v_o}{R})
\end{aligned} \tag{B.60}$$

where all the states are represented by their average values.

Perturbations are subsequently added to each state to perform linearization of the model around the operating point, so that each of the states become $X + \tilde{x}$, where X represents the operating point and $\tilde{x}$ is a small perturbation around the operating point. It is assumed that all cross-products of the perturbation are so small, so they can be easily neglected without significant adverse impact on the accuracy.

The perturbed average models for the six switching combinations are given with the following differential equations:

- sequence I:

$$\begin{aligned}
\dot{\tilde{i}}_{Lb} &= \big[\frac{D_a V_{in}}{L_b} - (1 - D_0 + \Delta D)\frac{V_{Cin}}{L_b}\big] + \\
&\quad + \big[\frac{D_a \tilde{v}_{in} + \tilde{d}_a V_{in}}{L_b} - \frac{(1 - D_0 + \Delta D)\tilde{v}_{Cin} - (\tilde{d}_0 - \Delta\tilde{d})V_{Cin}}{L_b}\big] \\
\dot{\tilde{i}}_{Lf} &= \big[-\frac{V_o}{2L_f} + \frac{2\Delta D V_{Cin}}{2L_f}\big] + \big[-\frac{\tilde{v}_o}{2L_f} + \frac{2\Delta D\tilde{v}_{Cin} + 2\Delta\tilde{d}V_{Cin}}{2L_f}\big] \\
\dot{\tilde{v}}_{Cin} &= \big[(1 - D_0 + \Delta D)\frac{I_{Lb}}{C_{in}} - \frac{2\Delta D I_{Lf}}{C_{in}}\big] + \\
&\quad + \big[\frac{(1 - D_0 + \Delta D)\tilde{i}_{Lb} - (\tilde{d}_0 - \Delta\tilde{d})I_{Lb}}{C_{in}} - \frac{2\Delta D\tilde{i}_{Lf} + 2\Delta\tilde{d}I_{Lf}}{C_{in}}\big] \\
\dot{\tilde{v}}_{Cf} &= \big[\frac{2}{C_f}(I_{Lf} - \frac{V_o}{R})\big] + \big[\frac{2}{C_f}(\tilde{i}_{Lf} - \frac{\tilde{v}_o}{R})\big]
\end{aligned} \tag{B.61}$$

- sequence II:

$$\begin{aligned}
\dot{\tilde{i}}_{Lb} &= \big[\frac{D_a V_{in}}{L_b} - (1 - D_0 + \Delta D)\frac{V_{Cin}}{L_b}\big] + \\
&\quad + \big[\frac{D_a \tilde{v}_{in} + \tilde{d}_a V_{in}}{L_b} - \frac{(1 - D_0 + \Delta D)\tilde{v}_{Cin} - (\tilde{d}_0 - \Delta\tilde{d})V_{Cin}}{L_b}\big] \\
\dot{\tilde{i}}_{Lf} &= \big[-\frac{V_o}{2L_f} + \frac{2\Delta D V_{Cin}}{2L_f}\big] + \big[-\frac{\tilde{v}_o}{2L_f} + \frac{2\Delta D\tilde{v}_{Cin} + 2\Delta\tilde{d}V_{Cin}}{2L_f}\big] \\
\dot{\tilde{v}}_{Cin} &= \big[(1 - D_0 + \Delta D)\frac{I_{Lb}}{C_{in}} - \frac{2\Delta D I_{Lf}}{C_{in}}\big] + \\
&\quad + \big[\frac{(1 - D_0 + \Delta D)\tilde{i}_{Lb} - (\tilde{d}_0 - \Delta\tilde{d})I_{Lb}}{C_{in}} - \frac{2\Delta D\tilde{i}_{Lf} + 2\Delta\tilde{d}I_{Lf}}{C_{in}}\big] \\
\dot{\tilde{v}}_{Cf} &= \big[\frac{2}{C_f}(I_{Lf} - \frac{V_o}{R})\big] + \big[\frac{2}{C_f}(\tilde{i}_{Lf} - \frac{\tilde{v}_o}{R})\big]
\end{aligned} \tag{B.62}$$

- sequence III:

$$\begin{aligned}
\dot{\tilde{i}}_{Lb} &= \Big[\frac{D_a V_{in}}{L_b} - (1 - D_0 + \Delta D)\frac{V_{Cin}}{L_b}\Big] + \\
&\quad + \Big[\frac{D_a \tilde{v}_{in} + \tilde{d}_a V_{in}}{L_b} - \frac{(1 - D_0 + \Delta D)\tilde{v}_{Cin} - (\tilde{d}_0 - \Delta\tilde{d})V_{Cin}}{L_b}\Big] \\
\dot{\tilde{i}}_{Lf} &= \Big[-\frac{V_o}{2L_f} + \frac{2\Delta D V_{Cin}}{2L_f}\Big] + \Big[-\frac{\tilde{v}_o}{2L_f} + \frac{2\Delta D\tilde{v}_{Cin} + 2\Delta\tilde{d}V_{Cin}}{2L_f}\Big] \\
\dot{\tilde{v}}_{Cin} &= \Big[(1 - D_0 + \Delta D)\frac{I_{Lb}}{C_{in}} - \frac{2\Delta D I_{Lf}}{C_{in}}\Big] + \\
&\quad + \Big[\frac{(1 - D_0 + \Delta D)\tilde{i}_{Lb} - (\tilde{d}_0 - \Delta\tilde{d})I_{Lb}}{C_{in}} - \frac{2\Delta D\tilde{i}_{Lf} + 2\Delta\tilde{d}I_{Lf}}{C_{in}}\Big] \\
\dot{\tilde{v}}_{Cf} &= \Big[\frac{2}{C_f}(I_{Lf} - \frac{V_o}{R})\Big] + \Big[\frac{2}{C_f}(\tilde{i}_{Lf} - \frac{\tilde{v}_o}{R})\Big]
\end{aligned} \tag{B.63}$$

- sequence IV:

$$\begin{aligned}
\dot{\tilde{i}}_{Lb} &= \Big[\frac{D_a V_{in}}{L_b} - (1 - D_0 - \Delta D)\frac{V_{Cin}}{L_b}\Big] + \\
&\quad + \Big[\frac{D_a \tilde{v}_{in} + \tilde{d}_a V_{in}}{L_b} - \frac{(1 - D_0 - \Delta D)\tilde{v}_{Cin} + (\tilde{d}_0 + \Delta\tilde{d})V_{Cin}}{L_b}\Big] \\
\dot{\tilde{i}}_{Lf} &= -\Big[\frac{V_o}{2L_f} + \frac{2\Delta D V_{Cin}}{2L_f}\Big] - \Big[\frac{\tilde{v}_o}{2L_f} + \frac{2\Delta D\tilde{v}_{Cin} + 2\Delta\tilde{d}V_{Cin}}{2L_f}\Big] \\
\dot{\tilde{v}}_{Cin} &= \Big[(1 - D_0 - \Delta D)\frac{I_{Lb}}{C_{in}} + \frac{2\Delta D I_{Lf}}{C_{in}}\Big] + \\
&\quad + \Big[\frac{(1 - D_0 - \Delta D)\tilde{i}_{Lb} - (\tilde{d}_0 + \Delta\tilde{d})I_{Lb}}{C_{in}} + \frac{2\Delta D\tilde{i}_{Lf} + 2\Delta\tilde{d}I_{Lf}}{C_{in}}\Big] \\
\dot{\tilde{v}}_{Cf} &= \Big[\frac{2}{C_f}(I_{Lf} - \frac{V_o}{R})\Big] + \Big[\frac{2}{C_f}(\tilde{i}_{Lf} - \frac{\tilde{v}_o}{R})\Big]
\end{aligned} \tag{B.64}$$

- sequence V:

$$\begin{aligned}
\dot{\tilde{i}}_{Lb} &= \Big[\frac{D_a V_{in}}{L_b} - (1 - D_a - 2D_0)\frac{V_{Cin}}{L_b}\Big] + \\
&\quad + \Big[\frac{D_a \tilde{v}_{in} + \tilde{d}_a V_{in}}{L_b} - \frac{(1 - D_a - 2D_0)\tilde{v}_{Cin} + (\tilde{d}_a - 2\tilde{d}_0)V_{Cin}}{L_b}\Big] \\
\dot{\tilde{i}}_{Lf} &= -\Big[\frac{V_o}{2L_f} + \frac{2\Delta D V_{Cin}}{2L_f}\Big] - \Big[\frac{\tilde{v}_o}{2L_f} + \frac{2\Delta D\tilde{v}_{Cin} + 2\Delta\tilde{d}V_{Cin}}{2L_f}\Big] \\
\dot{\tilde{v}}_{Cin} &= \Big[(1 - D_0 - \Delta D)\frac{I_{Lb}}{C_{in}} + \frac{2\Delta D I_{Lf}}{C_{in}}\Big] + \\
&\quad + \Big[\frac{(1 - D_0 - \Delta D)\tilde{i}_{Lb} - (\tilde{d}_0 + \Delta\tilde{d})I_{Lb}}{C_{in}} + \frac{2\Delta D\tilde{i}_{Lf} + 2\Delta\tilde{d}I_{Lf}}{C_{in}}\Big] \\
\dot{\tilde{v}}_{Cf} &= \Big[\frac{2}{C_f}(I_{Lf} - \frac{V_o}{R})\Big] + \Big[\frac{2}{C_f}(\tilde{i}_{Lf} - \frac{\tilde{v}_o}{R})\Big]
\end{aligned} \tag{B.65}$$

- sequence VI:

$$\begin{aligned}
\dot{\tilde{i}}_{Lb} &= \Big[\frac{D_a V_{in}}{L_b} - (1 - D_a + D_0)\frac{V_{Cin}}{L_b}\Big] + \\
&\quad + \Big[\frac{D_a \tilde{v}_{in} + \tilde{d}_a V_{in}}{L_b} - \frac{(1 - D_a + D_0)\tilde{v}_{Cin} + (\tilde{d}_a - 2\tilde{d}_0)V_{Cin}}{L_b}\Big] \\
\dot{\tilde{i}}_{Lf} &= -\Big[\frac{V_o}{2L_f} + \frac{2\Delta D V_{Cin}}{2L_f}\Big] - \Big[\frac{\tilde{v}_o}{2L_f} + \frac{2\Delta D\tilde{v}_{Cin} + 2\Delta\tilde{d}V_{Cin}}{2L_f}\Big] \\
\dot{\tilde{v}}_{Cin} &= \Big[(1 - D_0 - \Delta D)\frac{I_{Lb}}{C_{in}} + \frac{2\Delta D I_{Lf}}{C_{in}}\Big] + \\
&\quad + \Big[\frac{(1 - D_0 - \Delta D)\tilde{i}_{Lb} - (\tilde{d}_0 + \Delta\tilde{d})I_{Lb}}{C_{in}} + \frac{2\Delta D\tilde{i}_{Lf} + 2\Delta\tilde{d}I_{Lf}}{C_{in}}\Big] \\
\dot{\tilde{v}}_{Cf} &= \Big[\frac{2}{C_f}(I_{Lf} - \frac{V_o}{R})\Big] + \Big[\frac{2}{C_f}(\tilde{i}_{Lf} - \frac{\tilde{v}_o}{R})\Big]
\end{aligned} \tag{B.66}$$

DC-model of the combined Class D audio power amplifier and buck-boost PFC in asynchronous operation is obtained by equating the DC quantities on both sides of the perturbed equations (B.61)-(B.66):

- sequence I:

$$\begin{aligned}
0 &= D_a V_{in} - (1 - D_0 + \Delta D)V_{Cin} \quad &\Rightarrow \quad V_{Cin} &= \frac{D_a V_{in}}{1 - D_0 + \Delta D} \\
0 &= -V_o + 2\Delta D V_{Cin} \quad &\Rightarrow \quad V_o &= 2\Delta D V_{Cin} \\
0 &= (1 - D_0 + \Delta D)I_{Lb} - 2\Delta D I_{Lf} \quad &\Rightarrow \quad I_{Lb} &= \frac{2\Delta D I_{Lf}}{1 - D_0 + \Delta D} \\
0 &= I_{Lf} - \tfrac{V_o}{R} \quad &\Rightarrow \quad I_{Lf} &= \frac{V_o}{R} = I_o
\end{aligned} \tag{B.67}$$

- sequence II:

$$\begin{aligned}
0 &= D_a V_{in} - (1 - D_0 + \Delta D)V_{Cin} \quad &\Rightarrow \quad V_{Cin} &= \frac{D_a V_{in}}{1 - D_0 + \Delta D} \\
0 &= -V_o + 2\Delta D V_{Cin} \quad &\Rightarrow \quad V_o &= 2\Delta D V_{Cin} \\
0 &= (1 - D_0 + \Delta D)I_{Lb} - 2\Delta D I_{Lf} \quad &\Rightarrow \quad I_{Lb} &= \frac{2\Delta D I_{Lf}}{1 - D_0 + \Delta D} \\
0 &= I_{Lf} - \tfrac{V_o}{R} \quad &\Rightarrow \quad I_{Lf} &= \frac{V_o}{R} = I_o
\end{aligned} \tag{B.68}$$

- sequence III:

$$\begin{aligned}
0 &= D_a V_{in} - (1 - D_0 + \Delta D)V_{Cin} \quad &\Rightarrow \quad V_{Cin} &= \frac{D_a V_{in}}{1 - D_0 + \Delta D} \\
0 &= -V_o + 2\Delta D V_{Cin} \quad &\Rightarrow \quad V_o &= 2\Delta D V_{Cin} \\
0 &= (1 - D_0 + \Delta D)I_{Lb} - 2\Delta D I_{Lf} \quad &\Rightarrow \quad I_{Lb} &= \frac{2\Delta D I_{Lf}}{1 - D_0 + \Delta D} \\
0 &= I_{Lf} - \tfrac{V_o}{R} \quad &\Rightarrow \quad I_{Lf} &= \frac{V_o}{R} = I_o
\end{aligned} \tag{B.69}$$

- sequence IV:

$$\begin{aligned}
0 &= D_a V_{in} - (1 - D_0 - \Delta D) V_{Cin} \quad &\Rightarrow \quad V_{Cin} &= \frac{D_a V_{in}}{1 - D_0 - \Delta D} \\
0 &= V_o + 2\Delta D V_{Cin} \quad &\Rightarrow \quad V_o &= -2\Delta D V_{Cin} \\
0 &= (1 - D_0 - \Delta D) I_{Lb} + 2\Delta D I_{Lf} \quad &\Rightarrow \quad I_{Lb} &= -\frac{2\Delta D I_{Lf}}{1 - D_0 - \Delta D} \\
0 &= I_{Lf} - \tfrac{V_o}{R} \quad &\Rightarrow \quad I_{Lf} &= \frac{V_o}{R} = I_o
\end{aligned} \tag{B.70}$$

- sequence V:

$$\begin{aligned}
0 &= D_a V_{in} - (1 - D_a - 2D_0) V_{Cin} \quad &\Rightarrow \quad V_{Cin} &= \frac{D_a V_{in}}{1 - D_a - 2D_0} \\
0 &= V_o + 2\Delta D V_{Cin} \quad &\Rightarrow \quad V_o &= -2\Delta D V_{Cin} \\
0 &= (1 - D_0 - \Delta D) I_{Lb} + 2\Delta D I_{Lf} \quad &\Rightarrow \quad I_{Lb} &= -\frac{2\Delta D I_{Lf}}{1 - D_0 - \Delta D} \\
0 &= I_{Lf} - \tfrac{V_o}{R} \quad &\Rightarrow \quad I_{Lf} &= \frac{V_o}{R} = I_o
\end{aligned} \tag{B.71}$$

- sequence VI:

$$\begin{aligned}
0 &= D_a V_{in} - (1 - D_0 + \Delta D) V_{Cin} \quad &\Rightarrow \quad V_{Cin} &= \frac{D_a V_{in}}{1 - D_0 + \Delta D} \\
0 &= V_o + 2\Delta D V_{Cin} \quad &\Rightarrow \quad V_o &= -2\Delta D V_{Cin} \\
0 &= (1 - D_0 - \Delta D) I_{Lb} + 2\Delta D I_{Lf} \quad &\Rightarrow \quad I_{Lb} &= -\frac{2\Delta D I_{Lf}}{1 - D_0 - \Delta D} \\
0 &= I_{Lf} - \tfrac{V_o}{R} \quad &\Rightarrow \quad I_{Lf} &= \frac{V_o}{R} = I_o
\end{aligned} \tag{B.72}$$

Small-signal AC-model of the combined Class D audio power amplifier and buck-boost PFC in asynchronous mode of operation is obtained by equating the AC quantities on both sides of the perturbed equations (B.61)-(B.66):

- sequence I:

$$\begin{aligned}
\dot{\tilde{i}}_{Lb} &= \frac{D_a \tilde{v}_{in} + \tilde{d}_a V_{in}}{L_b} - \frac{(1 - D_0 + \Delta D)\tilde{v}_{Cin} - (\tilde{d}_0 - \Delta\tilde{d}) V_{Cin}}{L_b} \\
\dot{\tilde{i}}_{Lf} &= -\frac{\tilde{v}_o}{2L_f} + \frac{2\Delta D \tilde{v}_{Cin} + 2\Delta\tilde{d} V_{Cin}}{2L_f} \\
\dot{\tilde{v}}_{Cin} &= \frac{(1 - D_0 + \Delta D)\tilde{i}_{Lb} - (\tilde{d}_0 - \Delta\tilde{d}) I_{Lb}}{C_{in}} - \frac{2\Delta D \tilde{i}_{Lf} + 2\Delta\tilde{d} I_{Lf}}{C_{in}} \\
\dot{\tilde{v}}_{Cf} &= \frac{2}{C_f}(\tilde{i}_{Lf} - \frac{\tilde{v}_o}{R})
\end{aligned} \tag{B.73}$$

- sequence II:

$$\begin{aligned}
\dot{\tilde{i}}_{Lb} &= \frac{D_a \tilde{v}_{in} + \tilde{d}_a V_{in}}{L_b} - \frac{(1 - D_0 + \Delta D)\tilde{v}_{Cin} - (\tilde{d}_0 - \Delta\tilde{d}) V_{Cin}}{L_b} \\
\dot{\tilde{i}}_{Lf} &= -\frac{\tilde{v}_o}{2L_f} + \frac{2\Delta D \tilde{v}_{Cin} + 2\Delta\tilde{d} V_{Cin}}{2L_f} \\
\dot{\tilde{v}}_{Cin} &= \frac{(1 - D_0 + \Delta D)\tilde{i}_{Lb} - (\tilde{d}_0 - \Delta\tilde{d}) I_{Lb}}{C_{in}} - \frac{2\Delta D \tilde{i}_{Lf} + 2\Delta\tilde{d} I_{Lf}}{C_{in}} \\
\dot{\tilde{v}}_{Cf} &= \frac{2}{C_f}(\tilde{i}_{Lf} - \frac{\tilde{v}_o}{R})
\end{aligned} \tag{B.74}$$

- sequence III:

$$\begin{aligned}
\dot{\tilde{i}}_{Lb} &= \frac{D_a\tilde{v}_{in} + \tilde{d}_a V_{in}}{L_b} - \frac{(1 - D_0 + \Delta D)\tilde{v}_{Cin} - (\tilde{d}_0 - \Delta\tilde{d})V_{Cin}}{L_b} \\
\dot{\tilde{i}}_{Lf} &= -\frac{\tilde{v}_o}{2L_f} + \frac{2\Delta D\tilde{v}_{Cin} + 2\Delta\tilde{d}V_{Cin}}{2L_f} \\
\dot{\tilde{v}}_{Cin} &= \frac{(1 - D_0 + \Delta D)\tilde{i}_{Lb} - (\tilde{d}_0 - \Delta\tilde{d})I_{Lb}}{C_{in}} - \frac{2\Delta D\tilde{i}_{Lf} + 2\Delta\tilde{d}I_{Lf}}{C_{in}} \\
\dot{\tilde{v}}_{Cf} &= \frac{2}{C_f}(\tilde{i}_{Lf} - \frac{\tilde{v}_o}{R})
\end{aligned} \tag{B.75}$$

- sequence IV:

$$\begin{aligned}
\dot{\tilde{i}}_{Lb} &= \frac{D_a\tilde{v}_{in} + \tilde{d}_a V_{in}}{L_b} - \frac{(1 - D_0 - \Delta D)\tilde{v}_{Cin} + (\tilde{d}_0 + \Delta\tilde{d})V_{Cin}}{L_b} \\
\dot{\tilde{i}}_{Lf} &= \frac{\tilde{v}_o}{2L_f} + \frac{2\Delta D\tilde{v}_{Cin} + 2\Delta\tilde{d}V_{Cin}}{2L_f} \\
\dot{\tilde{v}}_{Cin} &= \frac{(1 - D_0 - \Delta D)\tilde{i}_{Lb} - (\tilde{d}_0 + \Delta\tilde{d})I_{Lb}}{C_{in}} + \frac{2\Delta D\tilde{i}_{Lf} + 2\Delta\tilde{d}I_{Lf}}{C_{in}} \\
\dot{\tilde{v}}_{Cf} &= \frac{2}{C_f}(\tilde{i}_{Lf} - \frac{\tilde{v}_o}{R})
\end{aligned} \tag{B.76}$$

- sequence V:

$$\begin{aligned}
\dot{\tilde{i}}_{Lb} &= \frac{D_a\tilde{v}_{in} + \tilde{d}_a V_{in}}{L_b} - \frac{(1 - D_a - 2D_0)\tilde{v}_{Cin} + (\tilde{d}_a - 2\tilde{d}_0)V_{Cin}}{L_b} \\
\dot{\tilde{i}}_{Lf} &= \frac{\tilde{v}_o}{2L_f} + \frac{2\Delta D\tilde{v}_{Cin} + 2\Delta\tilde{d}V_{Cin}}{2L_f} \\
\dot{\tilde{v}}_{Cin} &= \frac{(1 - D_0 - \Delta D)\tilde{i}_{Lb} - (\tilde{d}_0 + \Delta\tilde{d})I_{Lb}}{C_{in}} + \frac{2\Delta D\tilde{i}_{Lf} + 2\Delta\tilde{d}I_{Lf}}{C_{in}} \\
\dot{\tilde{v}}_{Cf} &= \frac{2}{C_f}(\tilde{i}_{Lf} - \frac{\tilde{v}_o}{R})
\end{aligned} \tag{B.77}$$

- sequence VI:

$$\begin{aligned}
\dot{\tilde{i}}_{Lb} &= \frac{D_a\tilde{v}_{in} + \tilde{d}_a V_{in}}{L_b} - \frac{(1 - D_a + D_0)\tilde{v}_{Cin} + (\tilde{d}_a - 2\tilde{d}_0)V_{Cin}}{L_b} \\
\dot{\tilde{i}}_{Lf} &= \frac{\tilde{v}_o}{2L_f} + \frac{2\Delta D\tilde{v}_{Cin} + 2\Delta\tilde{d}V_{Cin}}{2L_f} \\
\dot{\tilde{v}}_{Cin} &= \frac{(1 - D_0 - \Delta D)\tilde{i}_{Lb} - (\tilde{d}_0 + \Delta\tilde{d})I_{Lb}}{C_{in}} + \frac{2\Delta D\tilde{i}_{Lf} + 2\Delta\tilde{d}I_{Lf}}{C_{in}} \\
\dot{\tilde{v}}_{Cf} &= \frac{2}{C_f}(\tilde{i}_{Lf} - \frac{\tilde{v}_o}{R})
\end{aligned} \tag{B.78}$$

where $\sim$ is omitted for brevity.

The desired output quantities for the state-space representation are the input current i_{in}, DC-bus capacitor voltage v_{Cin} and output voltage v_o, where v_{Cin} and v_o are readily available and are equal to the state quantities v_{Cin} and v_{Cf}, while the DC and AC value of the input current are:

$$I_{in} = D_a I_{Lb} \tag{B.79}$$

and

$$i_{in} = D_a i_{Lb} + d_a I_{Lb} \tag{B.80}$$

AC small-signal models (B.73)-(B.78) can be rewritten in the following state-space forms:

- sequence I:

$$\begin{aligned}
\frac{d}{dt}\begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} &= \begin{bmatrix} 0 & 0 & -\dfrac{1-D_0+\Delta D}{L_b} & 0 \\ 0 & 0 & \dfrac{\Delta D}{L_f} & -\dfrac{1}{2L_f} \\ \dfrac{1-D_0+\Delta D}{C_{in}} & -\dfrac{2\Delta D}{C_{in}} & 0 & 0 \\ 0 & \dfrac{2}{C_f} & 0 & -\dfrac{2}{RC_f} \end{bmatrix} \cdot \begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} + \\
&+ \begin{bmatrix} \dfrac{D_a}{L_b} & \dfrac{V_{in}}{L_b} & \dfrac{V_{Cin}}{L_b} & -\dfrac{V_{Cin}}{L_b} \\ 0 & 0 & 0 & \dfrac{V_{Cin}}{L_f} \\ 0 & 0 & -\dfrac{I_{Lb}}{C_{in}} & \dfrac{I_{Lb}-2I_{Lf}}{C_{in}} \\ 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ d_a \\ d_0 \\ \Delta d \end{bmatrix} \\
\begin{bmatrix} i_{in} \\ v_{Cin} \\ v_o \end{bmatrix} &= \begin{bmatrix} D_a & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} + \\
&+ \begin{bmatrix} 0 & I_{Lb} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ d_a \\ d_0 \\ \Delta d \end{bmatrix}
\end{aligned} \tag{B.81}$$

So the system matrix $\mathbf{A_{bbI}}$, input matrix $\mathbf{B_{bbI}}$, output matrix $\mathbf{C_{bbI}}$ and input-to-output matrix $\mathbf{D_{bbI}}$ are:

$$\mathbf{A_{bbI}} = \begin{bmatrix} 0 & 0 & -\dfrac{1-D_0+\Delta D}{L_b} & 0 \\ 0 & 0 & \dfrac{\Delta D}{L_f} & -\dfrac{1}{2L_f} \\ \dfrac{1-D_0+\Delta D}{C_{in}} & -\dfrac{2\Delta D}{C_{in}} & 0 & 0 \\ 0 & \dfrac{2}{C_f} & 0 & -\dfrac{2}{RC_f} \end{bmatrix}$$

$$\mathbf{B_{bbI}} = \begin{bmatrix} \dfrac{D_a}{L_b} & \dfrac{V_{in}}{L_b} & \dfrac{V_{Cin}}{L_b} & -\dfrac{V_{Cin}}{L_b} \\ 0 & 0 & 0 & \dfrac{V_{Cin}}{L_f} \\ 0 & 0 & -\dfrac{I_{Lb}}{C_{in}} & \dfrac{I_{Lb}-2I_{Lf}}{C_{in}} \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{B.82}$$

$$\mathbf{C_{bbI}} = \begin{bmatrix} D_a & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

$$\mathbf{D_{bbI}} = \begin{bmatrix} 0 & I_{Lb} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$$

- sequence II:

$$\frac{d}{dt}\begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\dfrac{1-D_0+\Delta D}{L_b} & 0 \\ 0 & 0 & \dfrac{\Delta D}{L_f} & -\dfrac{1}{2L_f} \\ \dfrac{1-D_0+\Delta D}{C_{in}} & -\dfrac{2\Delta D}{C_{in}} & 0 & 0 \\ 0 & \dfrac{2}{C_f} & 0 & -\dfrac{2}{RC_f} \end{bmatrix} \cdot \begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} +$$

$$+ \begin{bmatrix} \dfrac{D_a}{L_b} & \dfrac{V_{in}}{L_b} & \dfrac{V_{Cin}}{L_b} & -\dfrac{V_{Cin}}{L_b} \\ 0 & 0 & 0 & \dfrac{V_{Cin}}{L_f} \\ 0 & 0 & -\dfrac{I_{Lb}}{C_{in}} & \dfrac{I_{Lb}-2I_{Lf}}{C_{in}} \\ 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ d_a \\ d_0 \\ \Delta d \end{bmatrix}$$

$$\begin{bmatrix} i_{in} \\ v_{Cin} \\ v_o \end{bmatrix} = \begin{bmatrix} D_a & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} +$$

$$+ \begin{bmatrix} 0 & I_{Lb} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ d_a \\ d_0 \\ \Delta d \end{bmatrix} \tag{B.83}$$

So the system matrix $\mathbf{A_{bbII}}$, input matrix $\mathbf{B_{bbII}}$, output matrix $\mathbf{C_{bbII}}$ and input-to-output matrix $\mathbf{D_{bbII}}$ are:

$$
\begin{aligned}
\mathbf{A_{bbII}} &= \begin{bmatrix} 0 & 0 & -\dfrac{1-D_0+\Delta D}{L_b} & 0 \\ 0 & 0 & \dfrac{\Delta D}{L_f} & -\dfrac{1}{2L_f} \\ \dfrac{1-D_0+\Delta D}{C_{in}} & -\dfrac{2\Delta D}{C_{in}} & 0 & 0 \\ 0 & \dfrac{2}{C_f} & 0 & -\dfrac{2}{RC_f} \end{bmatrix} \\
\mathbf{B_{bbII}} &= \begin{bmatrix} \dfrac{D_a}{L_b} & \dfrac{V_{in}}{L_b} & \dfrac{V_{Cin}}{L_b} & -\dfrac{V_{Cin}}{L_b} \\ 0 & 0 & 0 & \dfrac{V_{Cin}}{L_f} \\ 0 & 0 & -\dfrac{I_{Lb}}{C_{in}} & \dfrac{I_{Lb}-2I_{Lf}}{C_{in}} \\ 0 & 0 & 0 & 0 \end{bmatrix} \\
\mathbf{C_{bbII}} &= \begin{bmatrix} D_a & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \\
\mathbf{D_{bbII}} &= \begin{bmatrix} 0 & I_{Lb} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}
\end{aligned}
\tag{B.84}
$$

- sequence III:

$$\frac{d}{dt}\begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\dfrac{1-D_0+\Delta D}{L_b} & 0 \\ 0 & 0 & \dfrac{\Delta D}{L_f} & -\dfrac{1}{2L_f} \\ \dfrac{1-D_0+\Delta D}{C_{in}} & -\dfrac{2\Delta D}{C_{in}} & 0 & 0 \\ 0 & \dfrac{2}{C_f} & 0 & -\dfrac{2}{RC_f} \end{bmatrix} \cdot \begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} +$$

$$+ \begin{bmatrix} \dfrac{D_a}{L_b} & \dfrac{V_{in}}{L_b} & \dfrac{V_{Cin}}{L_b} & -\dfrac{V_{Cin}}{L_b} \\ 0 & 0 & 0 & \dfrac{V_{Cin}}{L_f} \\ 0 & 0 & -\dfrac{I_{Lb}}{C_{in}} & \dfrac{I_{Lb}-2I_{Lf}}{C_{in}} \\ 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ d_a \\ d_0 \\ \Delta d \end{bmatrix}$$

$$\begin{bmatrix} i_{in} \\ v_{Cin} \\ v_o \end{bmatrix} = \begin{bmatrix} D_a & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} +$$

$$+ \begin{bmatrix} 0 & I_{Lb} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ d_a \\ d_0 \\ \Delta d \end{bmatrix} \tag{B.85}$$

So the system matrix $\mathbf{A_{bbIII}}$, input matrix $\mathbf{B_{bbIII}}$, output matrix $\mathbf{C_{bbIII}}$ and input-to-output matrix $\mathbf{D_{bbIII}}$ are:

$$\begin{aligned}
\mathbf{A_{bbIII}} &= \begin{bmatrix} 0 & 0 & -\dfrac{1-D_0+\Delta D}{L_b} & 0 \\ 0 & 0 & \dfrac{\Delta D}{L_f} & -\dfrac{1}{2L_f} \\ \dfrac{1-D_0+\Delta D}{C_{in}} & -\dfrac{2\Delta D}{C_{in}} & 0 & 0 \\ 0 & \dfrac{2}{C_f} & 0 & -\dfrac{2}{RC_f} \end{bmatrix} \\
\mathbf{B_{bbIII}} &= \begin{bmatrix} \dfrac{D_a}{L_b} & \dfrac{V_{in}}{L_b} & \dfrac{V_{Cin}}{L_b} & -\dfrac{V_{Cin}}{L_b} \\ 0 & 0 & 0 & \dfrac{V_{Cin}}{L_f} \\ 0 & 0 & -\dfrac{I_{Lb}}{C_{in}} & \dfrac{I_{Lb}-2I_{Lf}}{C_{in}} \\ 0 & 0 & 0 & 0 \end{bmatrix} \\
\mathbf{C_{bbIII}} &= \begin{bmatrix} D_a & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \\
\mathbf{D_{bbIII}} &= \begin{bmatrix} 0 & I_{Lb} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}
\end{aligned} \tag{B.86}$$

- sequence IV:

$$\begin{aligned}
\frac{d}{dt}\begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} &= \begin{bmatrix} 0 & 0 & -\dfrac{1-D_0-\Delta D}{L_b} & 0 \\ 0 & 0 & -\dfrac{\Delta D}{L_f} & -\dfrac{1}{2L_f} \\ \dfrac{1-D_0-\Delta D}{C_{in}} & \dfrac{2\Delta D}{C_{in}} & 0 & 0 \\ 0 & \dfrac{2}{C_f} & 0 & -\dfrac{2}{RC_f} \end{bmatrix} \cdot \begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} + \\
&+ \begin{bmatrix} \dfrac{D_a}{L_b} & \dfrac{V_{in}}{L_b} & \dfrac{V_{Cin}}{L_b} & \dfrac{V_{Cin}}{L_b} \\ 0 & 0 & 0 & -\dfrac{V_{Cin}}{L_f} \\ 0 & 0 & -\dfrac{I_{Lb}}{C_{in}} & -\dfrac{I_{Lb}-2I_{Lf}}{C_{in}} \\ 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ d_a \\ d_0 \\ \Delta d \end{bmatrix} \\
\begin{bmatrix} i_{in} \\ v_{Cin} \\ v_o \end{bmatrix} &= \begin{bmatrix} D_a & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} + \\
&+ \begin{bmatrix} 0 & I_{Lb} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ d_a \\ d_0 \\ \Delta d \end{bmatrix}
\end{aligned} \tag{B.87}$$

So the system matrix $\mathbf{A_{bbIV}}$, input matrix $\mathbf{B_{bbIV}}$, output matrix $\mathbf{C_{bbIV}}$ and input-to-output matrix $\mathbf{D_{bbIV}}$ are:

$$\mathbf{A_{bbIV}} = \begin{bmatrix} 0 & 0 & -\dfrac{1-D_0-\Delta D}{L_b} & 0 \\ 0 & 0 & -\dfrac{\Delta D}{L_f} & -\dfrac{1}{2L_f} \\ \dfrac{1-D_0-\Delta D}{C_{in}} & \dfrac{2\Delta D}{C_{in}} & 0 & 0 \\ 0 & \dfrac{2}{C_f} & 0 & -\dfrac{2}{RC_f} \end{bmatrix}$$

$$\mathbf{B_{bbIV}} = \begin{bmatrix} \dfrac{D_a}{L_b} & \dfrac{V_{in}}{L_b} & \dfrac{V_{Cin}}{L_b} & \dfrac{V_{Cin}}{L_b} \\ 0 & 0 & 0 & -\dfrac{V_{Cin}}{L_f} \\ 0 & 0 & -\dfrac{I_{Lb}}{C_{in}} & -\dfrac{I_{Lb}-2I_{Lf}}{C_{in}} \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{B.88}$$

$$\mathbf{C_{bbIV}} = \begin{bmatrix} D_a & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

$$\mathbf{D_{bbIV}} = \begin{bmatrix} 0 & I_{Lb} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$$

- sequence V:

$$\frac{d}{dt}\begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\dfrac{1-D_a-2D_0}{L_b} & 0 \\ 0 & 0 & -\dfrac{\Delta D}{L_f} & -\dfrac{1}{2L_f} \\ \dfrac{1-D_0-\Delta D}{C_{in}} & \dfrac{2\Delta D}{C_{in}} & 0 & 0 \\ 0 & \dfrac{2}{C_f} & 0 & -\dfrac{2}{RC_f} \end{bmatrix} \cdot \begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} +$$

$$+ \begin{bmatrix} \dfrac{D_a}{L_b} & \dfrac{V_{in}-V_{Cin}}{L_b} & \dfrac{2V_{Cin}}{L_b} & 0 \\ 0 & 0 & 0 & -\dfrac{V_{Cin}}{L_f} \\ 0 & 0 & -\dfrac{I_{Lb}}{C_{in}} & -\dfrac{I_{Lb}-2I_{Lf}}{C_{in}} \\ 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ d_a \\ d_0 \\ \Delta d \end{bmatrix}$$

$$\begin{bmatrix} i_{in} \\ v_{Cin} \\ v_o \end{bmatrix} = \begin{bmatrix} D_a & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} +$$

$$+ \begin{bmatrix} 0 & I_{Lb} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ d_a \\ d_0 \\ \Delta d \end{bmatrix} \tag{B.89}$$

So the system matrix $\mathbf{A_{bbV}}$, input matrix $\mathbf{B_{bbV}}$, output matrix $\mathbf{C_{bbV}}$ and input-to-output matrix $\mathbf{D_{bbV}}$ are:

$$
\begin{aligned}
\mathbf{A_{bbV}} &= \begin{bmatrix} 0 & 0 & -\dfrac{1-D_a-2D_0}{L_b} & 0 \\ 0 & 0 & -\dfrac{\Delta D}{L_f} & -\dfrac{1}{2L_f} \\ \dfrac{1-D_0-\Delta D}{C_{in}} & \dfrac{2\Delta D}{C_{in}} & 0 & 0 \\ 0 & \dfrac{2}{C_f} & 0 & -\dfrac{2}{RC_f} \end{bmatrix} \\
\mathbf{B_{bbV}} &= \begin{bmatrix} \dfrac{D_a}{L_b} & \dfrac{V_{in}-V_{Cin}}{L_b} & \dfrac{2V_{Cin}}{L_b} & 0 \\ 0 & 0 & 0 & -\dfrac{V_{Cin}}{L_f} \\ 0 & 0 & -\dfrac{I_{Lb}}{C_{in}} & -\dfrac{I_{Lb}-2I_{Lf}}{C_{in}} \\ 0 & 0 & 0 & 0 \end{bmatrix} \\
\mathbf{C_{bbV}} &= \begin{bmatrix} D_a & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \\
\mathbf{D_{bbV}} &= \begin{bmatrix} 0 & I_{Lb} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}
\end{aligned}
\tag{B.90}
$$

- sequence VI:

$$\begin{aligned}
\frac{d}{dt}\begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} &= \begin{bmatrix} 0 & 0 & -\dfrac{1-D_0+\Delta D}{L_b} & 0 \\ 0 & 0 & -\dfrac{\Delta D}{L_f} & -\dfrac{1}{2L_f} \\ \dfrac{1-D_0-\Delta D}{C_{in}} & \dfrac{2\Delta D}{C_{in}} & 0 & 0 \\ 0 & \dfrac{2}{C_f} & 0 & -\dfrac{2}{RC_f} \end{bmatrix} \cdot \begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} + \\
&+ \begin{bmatrix} \dfrac{D_a}{L_b} & \dfrac{V_{in}}{L_b} & \dfrac{V_{Cin}}{L_b} & -\dfrac{V_{Cin}}{L_b} \\ 0 & 0 & 0 & -\dfrac{V_{Cin}}{L_f} \\ 0 & 0 & -\dfrac{I_{Lb}}{C_{in}} & -\dfrac{I_{Lb}-2I_{Lf}}{C_{in}} \\ 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ d_a \\ d_0 \\ \Delta d \end{bmatrix} \\
\begin{bmatrix} i_{in} \\ v_{Cin} \\ v_o \end{bmatrix} &= \begin{bmatrix} D_a & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} i_{Lb} \\ i_{Lf} \\ v_{Cin} \\ v_{Cf} \end{bmatrix} + \\
&+ \begin{bmatrix} 0 & I_{Lb} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_{in} \\ d_a \\ d_0 \\ \Delta d \end{bmatrix}
\end{aligned} \tag{B.91}$$

So the system matrix $\mathbf{A_{bbVI}}$, input matrix $\mathbf{B_{bbVI}}$, output matrix $\mathbf{C_{bbVI}}$ and input-to-output matrix $\mathbf{D_{bbVI}}$ are:

$$\begin{aligned}
\mathbf{A_{bbVI}} &= \begin{bmatrix} 0 & 0 & -\dfrac{1-D_0+\Delta D}{L_b} & 0 \\ 0 & 0 & -\dfrac{\Delta D}{L_f} & -\dfrac{1}{2L_f} \\ \dfrac{1-D_0-\Delta D}{C_{in}} & \dfrac{2\Delta D}{C_{in}} & 0 & 0 \\ 0 & \dfrac{2}{C_f} & 0 & -\dfrac{2}{RC_f} \end{bmatrix} \\
\mathbf{B_{bbVI}} &= \begin{bmatrix} \dfrac{D_a}{L_b} & \dfrac{V_{in}}{L_b} & \dfrac{V_{Cin}}{L_b} & -\dfrac{V_{Cin}}{L_b} \\ 0 & 0 & 0 & -\dfrac{V_{Cin}}{L_f} \\ 0 & 0 & -\dfrac{I_{Lb}}{C_{in}} & -\dfrac{I_{Lb}-2I_{Lf}}{C_{in}} \\ 0 & 0 & 0 & 0 \end{bmatrix} \\
\mathbf{C_{bbVI}} &= \begin{bmatrix} D_a & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \\
\mathbf{D_{bbVI}} &= \begin{bmatrix} 0 & I_{Lb} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}
\end{aligned} \tag{B.92}$$

System matrices in (B.82)-(B.92) can be used to develop small-signal transfer functions for each of the switching sequences:

$$\begin{aligned}
\begin{bmatrix} i_{in} \\ v_{Cin} \\ v_o \end{bmatrix} &= \left[\mathbf{C_{bb+}}(s\mathbf{I}-\mathbf{A_{bb+}})^{-1}\mathbf{B_{bb+}}+\mathbf{D_{bb+}}\right]\cdot\begin{bmatrix} v_{in} \\ d_a \\ d_0 \\ \Delta d \end{bmatrix} = \\
&= \begin{bmatrix} G_{i_{in}v_{in},bbK}(s) & G_{i_{in}d_a,bbK}(s) & G_{i_{in}d_0,bbK}(s) & G_{i_{in}\Delta d,bbK}(s) \\ G_{v_{Cin}v_{in},bbK}(s) & G_{v_{Cin}d_a,bbK}(s) & G_{v_{Cin}d_0,bbK}(s) & G_{v_{Cin}\Delta d,bbK}(s) \\ G_{v_ov_{in},bbK}(s) & G_{v_od_a,bbK}(s) & G_{v_od_0,bbK}(s) & G_{v_o\Delta d,bbK}(s) \end{bmatrix}\cdot\begin{bmatrix} v_{in} \\ d_a \\ d_0 \\ \Delta d \end{bmatrix}
\end{aligned} \tag{B.93}$$

where K represents one of the switching sequences $I-VI$.

It is interesting to note that switching sequences I, II and III corresponding to positive output voltages have the same DC and AC models.

C

Analysis of double-boost SICAM for portable applications

The analysis of the double-boost SICAM operation will be performed on the set of four different switch connections shown in Fig. C.1. Stepping through the different possible connections is performed according to the sign of the output voltage, and is shown in Fig. C.1 with the plus and minus sign.

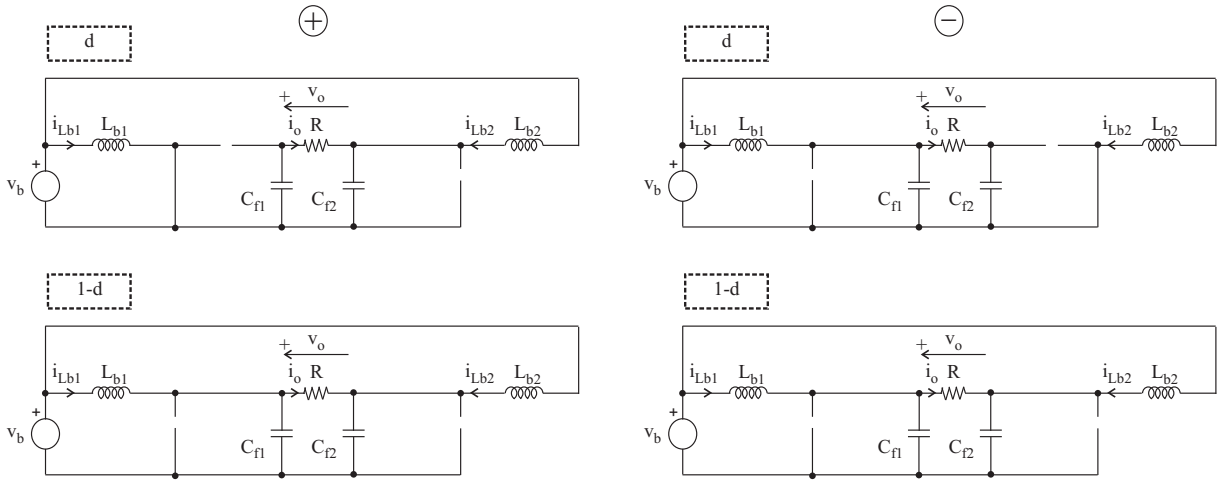

Fig. C.1. Possible connections in the double-boost SICAM (same as Fig. 4.2)

For positive output voltages:

- during interval d:

$$\begin{aligned} L_{b1}\frac{di_{Lb1}}{dt} &= v_b \\ L_{b2}\frac{di_{Lb2}}{dt} &= v_b - v_{Cf2} \\ C_{f1}\frac{dv_{Cf1}}{dt} &= -i_o = -\frac{v_{Cf1}-v_{Cf2}}{R} \\ C_{f2}\frac{dv_{Cf2}}{dt} &= i_o + i_{Lb2} = \frac{v_{Cf1}-v_{Cf2}}{R} + i_{Lb2} \end{aligned} \tag{C.1}$$

i.e.:

$$\begin{aligned}
\frac{di_{Lb1}}{dt} &= \frac{1}{L_{Lb1}} v_b \\
\frac{di_{Lb2}}{dt} &= \frac{1}{L_{Lb2}} (v_b - v_{Cf2}) \\
\frac{dv_{Cf1}}{dt} &= -\frac{v_{Cf1} - v_{Cf2}}{RC_{f1}} \\
\frac{dv_{Cf2}}{dt} &= \frac{v_{Cf1} - v_{Cf2}}{RC_{f2}} + \frac{1}{C_{f2}} i_{Lb2}
\end{aligned} \tag{C.2}$$

- during interval $1 - d$:

$$\begin{aligned}
L_{b1} \frac{di_{Lb1}}{dt} &= v_b - v_{Cf1} \\
L_{b2} \frac{di_{Lb2}}{dt} &= v_b - v_{Cf2} \\
C_{f1} \frac{dv_{Cf1}}{dt} &= -i_o + i_{Lb1} = -\frac{v_{Cf1} - v_{Cf2}}{R} + i_{Lb1} \\
C_{f2} \frac{dv_{Cf2}}{dt} &= i_o + i_{Lb2} = \frac{v_{Cf1} - v_{Cf2}}{R} + i_{Lb2}
\end{aligned} \tag{C.3}$$

i.e.:

$$\begin{aligned}
\frac{di_{Lb1}}{dt} &= \frac{1}{L_{Lb1}} (v_b - v_{Cf1}) \\
\frac{di_{Lb2}}{dt} &= \frac{1}{L_{Lb2}} (v_b - v_{Cf2}) \\
\frac{dv_{Cf1}}{dt} &= -\frac{v_{Cf1} - v_{Cf2}}{RC_{f1}} + \frac{1}{C_{f1}} i_{Lb1} \\
\frac{dv_{Cf2}}{dt} &= \frac{v_{Cf1} - v_{Cf2}}{RC_{f2}} + \frac{1}{C_{f2}} i_{Lb2}
\end{aligned} \tag{C.4}$$

For negative output voltages:

- during interval d:

$$\begin{aligned}
L_{b1} \frac{di_{Lb1}}{dt} &= v_b - v_{Cf1} \\
L_{b2} \frac{di_{Lb2}}{dt} &= v_b \\
C_{f1} \frac{dv_{Cf1}}{dt} &= i_{Lb1} - i_o = i_{Lb1} - \frac{v_{Cf1} - v_{Cf2}}{R} \\
C_{f2} \frac{dv_{Cf2}}{dt} &= i_o = \frac{v_{Cf1} - v_{Cf2}}{R}
\end{aligned} \tag{C.5}$$

i.e.:

$$\begin{aligned}
\frac{di_{Lb1}}{dt} &= \frac{1}{L_{Lb1}} (v_b - v_{Cf1}) \\
\frac{di_{Lb2}}{dt} &= \frac{1}{L_{Lb2}} v_b \\
\frac{dv_{Cf1}}{dt} &= \frac{1}{C_{f1}} i_{Lb1} - \frac{v_{Cf1} - v_{Cf2}}{RC_{f1}} \\
\frac{dv_{Cf2}}{dt} &= \frac{v_{Cf1} - v_{Cf2}}{RC_{f2}}
\end{aligned} \tag{C.6}$$

- during interval $1-d$:

$$\begin{aligned} L_{b1}\frac{di_{Lb1}}{dt} &= v_b - v_{Cf1} \\ L_{b2}\frac{di_{Lb2}}{dt} &= v_b - v_{Cf2} \\ C_{f1}\frac{dv_{Cf1}}{dt} &= -i_o + i_{Lb1} = -\frac{v_{Cf1}-v_{Cf2}}{R} + i_{Lb1} \\ C_{f2}\frac{dv_{Cf2}}{dt} &= i_o + i_{Lb2} = \frac{v_{Cf1}-v_{Cf2}}{R} + i_{Lb2} \end{aligned} \tag{C.7}$$

i.e.:

$$\begin{aligned} \frac{di_{Lb1}}{dt} &= \frac{1}{L_{Lb1}}(v_b - v_{Cf1}) \\ \frac{di_{Lb2}}{dt} &= \frac{1}{L_{Lb2}}(v_b - v_{Cf2}) \\ \frac{dv_{Cf1}}{dt} &= -\frac{v_{Cf1}-v_{Cf2}}{RC_{f1}} + \frac{1}{C_{f1}}i_{Lb1} \\ \frac{dv_{Cf2}}{dt} &= \frac{v_{Cf1}-v_{Cf2}}{RC_{f2}} + \frac{1}{C_{f2}}i_{Lb2} \end{aligned} \tag{C.8}$$

In the next step, averaging of the state-space equations is performed to remove the switching harmonics present in the waveforms and reveal the low frequency content. For the positive output voltages this corresponds to summing up equations (C.2) and (C.4) weighted by their respective duty cycles:

$$\begin{aligned} \dot{i}_{Lb1} &= \frac{v_b}{L_b1} - (1-d)\frac{v_{Cf1}}{L_b1} \\ \dot{i}_{Lb2} &= \frac{v_b - v_{Cf2}}{L_{b2}} \\ \dot{v}_{Cf1} &= -\frac{v_{Cf1}-v_{Cf2}}{RC_{f1}} + (1-d)\frac{i_{Lb1}}{C_{f1}} \\ \dot{v}_{Cf2} &= \frac{v_{Cf1}-v_{Cf2}}{RC_{f2}} + \frac{i_{Lb2}}{C_{f2}} \end{aligned} \tag{C.9}$$

where all the states are represented by their average values.

For the negative output voltages averaging corresponds to summing up equations (C.6) and (C.8) weighted by their respective duty cycles:

$$\begin{aligned} \dot{i}_{Lb1} &= \frac{v_b - v_{Cf1}}{L_{b1}} \\ \dot{i}_{Lb2} &= \frac{v_b}{L_b2} - (1-d)\frac{v_{Cf2}}{L_b2} \\ \dot{v}_{Cf1} &= -\frac{v_{Cf1}-v_{Cf2}}{RC_{f1}} + \frac{i_{Lb1}}{C_{f1}} \\ \dot{v}_{Cf2} &= \frac{v_{Cf1}-v_{Cf2}}{RC_{f2}} + (1-d)\frac{i_{Lb2}}{C_{f2}} \end{aligned} \tag{C.10}$$

where all the states are again represented by their average values.

Perturbations are subsequently added to each state to perform linearization of the model around the operating point, so that each of the states become $X + \tilde{x}$, where X represents the operating point and $\tilde{x}$ is a small perturbation around the operating point.

It is assumed that all cross-products of the perturbation are so small, so they can be easily neglected without significant adverse impact on the accuracy.

For positive output voltages, the perturbed average model becomes:

$$\begin{aligned}
\dot{\tilde{i}}_{Lb1} &= \Big[\frac{V_b}{L_{b1}} - \frac{(1-D)V_{Cf1}}{L_{b1}}\Big] + \Big[\frac{\tilde{v}_b}{L_{b1}} - \frac{(1-D)\tilde{v}_{Cf1} - \tilde{d}V_{Cf1}}{L_{b1}}\Big] \\
\dot{\tilde{i}}_{Lb2} &= \Big[\frac{V_b - V_{Cf2}}{L_{b2}}\Big] + \Big[\frac{\tilde{v}_b - \tilde{v}_{Cf2}}{L_{b2}}\Big] \\
\dot{\tilde{v}}_{Cf1} &= \Big[-\frac{V_{Cf1} - V_{Cf2}}{RC_{f1}} + \frac{(1-D)I_{Lb1}}{C_{f1}}\Big] + \Big[-\frac{\tilde{v}_{Cf1} - \tilde{v}_{Cf2}}{RC_{f1}} + \frac{(1-D)\tilde{i}_{Lb1} - \tilde{d}I_{Lb1}}{C_{f1}}\Big] \\
\dot{\tilde{v}}_{Cf2} &= \Big[\frac{V_{Cf1} - V_{Cf2}}{RC_{f2}} + \frac{I_{Lb2}}{C_{f2}}\Big] + \Big[\frac{\tilde{v}_{Cf1} - \tilde{v}_{Cf2}}{RC_{f2}} + \frac{\tilde{i}_{Lb2}}{C_{f2}}\Big]
\end{aligned} \tag{C.11}$$

and for negative output voltages:

$$\begin{aligned}
\dot{\tilde{i}}_{Lb1} &= \Big[\frac{V_b - V_{Cf1}}{L_{b1}}\Big] + \Big[\frac{\tilde{v}_b - \tilde{v}_{Cf1}}{L_{b1}}\Big] \\
\dot{\tilde{i}}_{Lb2} &= \Big[\frac{V_b}{L_{b2}} - \frac{(1-D)V_{Cf2}}{L_{b2}}\Big] + \Big[\frac{\tilde{v}_b}{L_{b2}} - \frac{(1-D)\tilde{v}_{Cf2} - \tilde{d}V_{Cf2}}{L_{b2}}\Big] \\
\dot{\tilde{v}}_{Cf1} &= \Big[-\frac{V_{Cf1} - V_{Cf2}}{RC_{f1}} + \frac{I_{Lb1}}{C_{f1}}\Big] + \Big[-\frac{\tilde{v}_{Cf1} - \tilde{v}_{Cf2}}{RC_{f1}} + \frac{\tilde{i}_{Lb1}}{C_{f1}}\Big] \\
\dot{\tilde{v}}_{Cf2} &= \Big[\frac{V_{Cf1} - V_{Cf2}}{RC_{f2}} + \frac{(1-D)I_{Lb2}}{C_{f2}}\Big] + \Big[\frac{\tilde{v}_{Cf1} - \tilde{v}_{Cf2}}{RC_{f2}} + \frac{(1-D)\tilde{i}_{Lb2} - \tilde{d}I_{Lb2}}{C_{f2}}\Big]
\end{aligned} \tag{C.12}$$

DC-model of the double-boost SICAM is obtained by equating the DC quantities on both sides of (C.11) for positive output voltages:

$$\begin{aligned}
0 &= V_b - (1-D)V_{Cf1} \quad &\Rightarrow \quad V_{Cf1} &= \frac{V_b}{1-D} \\
0 &= V_b - V_{Cf2} \quad &\Rightarrow \quad V_{Cf2} &= V_b \\
0 &= -\frac{V_{Cf1} - V_{Cf2}}{R} + (1-D)I_{Lb1} \quad &\Rightarrow \quad I_{Lb1} &= \frac{V_{Cf1} - V_{Cf2}}{(1-D)R} \\
0 &= \frac{V_{Cf1} - V_{Cf2}}{R} + I_{Lb2} \quad &\Rightarrow \quad I_{Lb2} &= -\frac{V_{Cf1} - V_{Cf2}}{R}
\end{aligned} \tag{C.13}$$

and (C.11) for negative output voltages:

$$\begin{aligned}
0 &= V_b - V_{Cf1} \quad &\Rightarrow \quad V_{Cf1} &= V_b \\
0 &= V_b - (1-D)V_{Cf2} \quad &\Rightarrow \quad V_{Cf2} &= \frac{V_b}{1-D} \\
0 &= -\frac{V_{Cf1} - V_{Cf2}}{R} + I_{Lb1} \quad &\Rightarrow \quad I_{Lb1} &= \frac{V_{Cf1} - V_{Cf2}}{R} \\
0 &= \frac{V_{Cf1} - V_{Cf2}}{R} + (1-D)I_{Lb2} \quad &\Rightarrow \quad I_{Lb2} &= -\frac{V_{Cf1} - V_{Cf2}}{(1-D)R}
\end{aligned} \tag{C.14}$$

AC-model of the double boost SICAM is obtained by equating the AC quantities on both sides of (C.11) for positive output voltages:

$$\begin{aligned}
\dot{i}_{Lb1} &= \frac{v_b}{L_{b1}} - \frac{(1-D)v_{Cf1} - dV_{Cf1}}{L_{b1}} \\
\dot{i}_{Lb2} &= \frac{v_b - v_{Cf2}}{L_{b2}} \\
\dot{v}_{Cf1} &= -\frac{v_{Cf1} - v_{Cf2}}{RC_{f1}} + \frac{(1-D)i_{Lb1} - dI_{Lb1}}{C_{f1}} \\
\dot{v}_{Cf2} &= \frac{v_{Cf1} - v_{Cf2}}{RC_{f2}} + \frac{i_{Lb2}}{C_{f2}}
\end{aligned} \tag{C.15}$$

and (B.33) for negative output voltages:

$$\begin{aligned}
\dot{i}_{Lb1} &= \frac{v_b - v_{Cf1}}{L_{b1}} \\
\dot{i}_{Lb2} &= \frac{v_b}{L_{b2}} - \frac{(1-D)v_{Cf2} - dV_{Cf2}}{L_{b2}} \\
\dot{v}_{Cf1} &= -\frac{v_{Cf1} - v_{Cf2}}{RC_{f1}} + \frac{i_{Lb1}}{C_{f1}} \\
\dot{v}_{Cf2} &= \frac{v_{Cf1} - v_{Cf2}}{RC_{f2}} + \frac{(1-D)i_{Lb2} - dI_{Lb2}}{C_{f2}}
\end{aligned} \tag{C.16}$$

where $\sim$ is omitted for brevity.

AC small-signal model for positive output voltages (C.15) can be rewritten in the following state-space form:

$$\begin{aligned}
\frac{d}{dt}\begin{bmatrix} i_{Lb1} \\ i_{Lb2} \\ v_{Cf1} \\ v_{Cf2} \end{bmatrix} &= \begin{bmatrix} 0 & 0 & -\frac{1-D}{L_{b1}} & 0 \\ 0 & 0 & 0 & -\frac{1}{L_{b2}} \\ \frac{1-D}{C_{f1}} & 0 & -\frac{1}{RC_{f1}} & \frac{1}{RC_{f1}} \\ 0 & \frac{1}{C_{f2}} & \frac{1}{RC_{f2}} & -\frac{1}{RC_{f2}} \end{bmatrix} \cdot \begin{bmatrix} i_{Lb1} \\ i_{Lb2} \\ v_{Cf1} \\ v_{Cf2} \end{bmatrix} + \\
&+ \begin{bmatrix} \frac{1}{L_{b1}} & \frac{V_{Cf1}}{L_{b1}} \\ \frac{1}{L_{b2}} & 0 \\ 0 & -\frac{I_{Lb1}}{C_{f1}} \\ 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_b \\ d \end{bmatrix} \\
\begin{bmatrix} v_o \\ i_b \end{bmatrix} &= \begin{bmatrix} 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_{Lb1} \\ i_{Lb2} \\ v_{Cf1} \\ v_{Cf2} \end{bmatrix} + 0 \cdot \begin{bmatrix} v_b \\ d \end{bmatrix}
\end{aligned} \tag{C.17}$$

So the system matrix $\mathbf{A_{db+}}$, input matrix $\mathbf{B_{db+}}$, output matrix $\mathbf{C_{db+}}$ and input-to-output matrix $\mathbf{D_{db+}}$ are:

$$
\begin{aligned}
\mathbf{A_{db+}} &= \begin{bmatrix} 0 & 0 & -\dfrac{1-D}{L_{b1}} & 0 \\ 0 & 0 & 0 & -\dfrac{1}{L_{b2}} \\ \dfrac{1-D}{C_{f1}} & 0 & -\dfrac{1}{RC_{f1}} & \dfrac{1}{RC_{f1}} \\ 0 & \dfrac{1}{C_{f2}} & \dfrac{1}{RC_{f2}} & -\dfrac{1}{RC_{f2}} \end{bmatrix} \\
\mathbf{B_{db+}} &= \begin{bmatrix} \dfrac{1}{L_{b1}} & \dfrac{V_{Cf1}}{L_{b1}} \\ \dfrac{1}{L_{b2}} & 0 \\ 0 & -\dfrac{I_{Lb1}}{C_{f1}} \\ 0 & 0 \end{bmatrix} \\
\mathbf{C_{db+}} &= \begin{bmatrix} 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \end{bmatrix} \\
\mathbf{D_{db+}} &= 0
\end{aligned}
\tag{C.18}
$$

AC small-signal model for negative output voltages (C.16) can be rewritten in the following state-space form:

$$
\begin{aligned}
\frac{d}{dt}\begin{bmatrix} i_{Lb1} \\ i_{Lb2} \\ v_{Cf1} \\ v_{Cf2} \end{bmatrix} &= \begin{bmatrix} 0 & 0 & -\dfrac{1}{L_{b1}} & 0 \\ 0 & 0 & 0 & -\dfrac{1-D}{L_{b2}} \\ \dfrac{1}{C_{f1}} & 0 & -\dfrac{1}{RC_{f1}} & \dfrac{1}{RC_{f1}} \\ 0 & \dfrac{1-D}{C_{f2}} & \dfrac{1}{RC_{f2}} & -\dfrac{1}{RC_{f2}} \end{bmatrix} \cdot \begin{bmatrix} i_{Lb1} \\ i_{Lb2} \\ v_{Cf1} \\ v_{Cf2} \end{bmatrix} + \\
&+ \begin{bmatrix} \dfrac{1}{L_{b1}} & 0 \\ \dfrac{1}{L_{b2}} & \dfrac{V_{Cf2}}{L_{b2}} \\ 0 & 0 \\ 0 & -\dfrac{I_{Lb2}}{C_{f2}} \end{bmatrix} \cdot \begin{bmatrix} v_b \\ d \end{bmatrix} \\
\begin{bmatrix} v_o \\ i_b \end{bmatrix} &= \begin{bmatrix} 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_{Lb1} \\ i_{Lb2} \\ v_{Cf1} \\ v_{Cf2} \end{bmatrix} + 0 \cdot \begin{bmatrix} v_b \\ d \end{bmatrix}
\end{aligned}
\tag{C.19}
$$

So the system matrix $\mathbf{A_{db-}}$, input matrix $\mathbf{B_{db-}}$, output matrix $\mathbf{C_{db-}}$ and input-to-output matrix $\mathbf{D_{db-}}$ are:

$$
\begin{aligned}
\mathbf{A_{db-}} &= \begin{bmatrix} 0 & 0 & -\dfrac{1}{L_{b1}} & 0 \\ 0 & 0 & 0 & -\dfrac{1-D}{L_{b2}} \\ \dfrac{1}{C_{f1}} & 0 & -\dfrac{1}{RC_{f1}} & \dfrac{1}{RC_{f1}} \\ 0 & \dfrac{1-D}{C_{f2}} & \dfrac{1}{RC_{f2}} & -\dfrac{1}{RC_{f2}} \end{bmatrix} \\
\mathbf{B_{db-}} &= \begin{bmatrix} \dfrac{1}{L_{b1}} & 0 \\ \dfrac{1}{L_{b2}} & \dfrac{V_{Cf2}}{L_{b2}} \\ 0 & 0 \\ 0 & -\dfrac{I_{Lb2}}{C_{f2}} \end{bmatrix} \\
\mathbf{C_{db-}} &= \begin{bmatrix} 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \end{bmatrix} \\
\mathbf{D_{db-}} &= 0
\end{aligned}
\tag{C.20}
$$

System matrices in (C.18) and (C.20) can be used to develop small-signal transfer functions for positive and negative output voltages by recognizing that:

$$
\begin{aligned}
\begin{bmatrix} v_o \\ i_b \end{bmatrix} &= \left[\mathbf{C_{db+}}(s\mathbf{I} - \mathbf{A_{db+}})^{-1}\mathbf{B_{db+}} + \mathbf{D_{db+}}\right] \cdot \begin{bmatrix} v_b \\ d \end{bmatrix} = \\
&= \begin{bmatrix} G_{v_o v_b,db+}(s) & G_{v_o d,db+}(s) \\ G_{i_b v_b,db+}(s) & G_{i_b d,db+}(s) \end{bmatrix} \cdot \begin{bmatrix} v_b \\ d \end{bmatrix}
\end{aligned}
\tag{C.21}
$$

and:

$$
\begin{aligned}
\begin{bmatrix} v_o \\ i_b \end{bmatrix} &= \left[\mathbf{C_{db-}}(s\mathbf{I} - \mathbf{A_{db-}})^{-1}\mathbf{B_{db-}} + \mathbf{D_{db-}}\right] \cdot \begin{bmatrix} v_b \\ d \end{bmatrix} = \\
&= \begin{bmatrix} G_{v_o v_b,db-}(s) & G_{v_o d,db-}(s) \\ G_{i_b v_b,db-}(s) & G_{i_b d,db-}(s) \end{bmatrix} \cdot \begin{bmatrix} v_b \\ d \end{bmatrix}
\end{aligned}
\tag{C.22}
$$

D

Analysis of flyback auxiliary converter for SICAM with active capacitive voltage clamp

D.1 Analysis of CCM flyback auxiliary converter

The state-space analysis of the CCM flyback auxiliary converter will be performed using the circuit diagram in Fig. D.1.

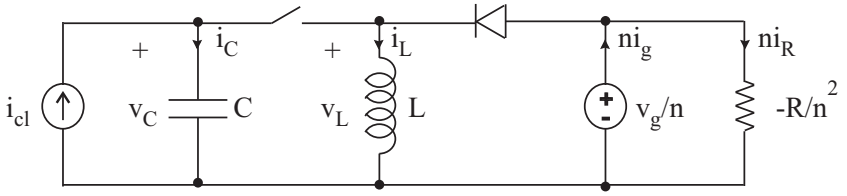

Fig. D.1. Buck-boost auxiliary converter (same as Fig. 6.21)

The differential equations for the CCM flyback auxiliary converter are:

- during interval t_{on} i.e. d:

$$\begin{aligned} L\frac{di_L}{dt} &= v_C \\ C\frac{dv_C}{dt} &= -i_L + i_{cl} \\ ni_g = ni_R &= -\frac{nv_g}{R} \end{aligned} \tag{D.1}$$

- during interval t_{off} i.e. $d' = 1 - d$:

$$\begin{aligned} L\frac{di_L}{dt} &= \frac{v_g}{n} \\ C\frac{dv_C}{dt} &= i_{cl} \\ ni_g = i_L + ni_R &= i_L - \frac{nv_g}{R} \end{aligned} \tag{D.2}$$

In the next step, averaging of the state-space equations is performed to remove the switching harmonics present in the waveforms and reveal the low frequency content. This corresponds to summing up equations (D.1) and (D.2) weighted by their respective duty cycles:

$$\begin{aligned} L\frac{di_L}{dt} &= dv_C + d'\frac{v_g}{n} \\ C\frac{dv_C}{dt} &= -di_L + i_{cl} \\ ni_g = ni_R &= d'i_L - \frac{nv_g}{R} \end{aligned} \tag{D.3}$$

where all the states are represented by their average values.

Perturbations are subsequently added to each state to perform linearization of the model around the operating point, so that each of the states become $X + \tilde{x}$, where X represents the operating point and $\tilde{x}$ is a small perturbation around the operating point. It is assumed that all cross-products of the perturbation are so small, so they can be easily neglected without significant adverse impact on the accuracy. It should be noted that the perturbation on the complementary duty cycle d' is $\Delta d' = -\Delta d$.

The perturbed average model of (D.3) becomes:

$$\begin{aligned} L\frac{d\tilde{i}_L}{dt} &= (DV_c + D'\frac{V_g}{n}) + (D\tilde{v}_C + V_C\tilde{d} + D'\frac{\tilde{v}_g}{n} - \frac{V_g}{n}\tilde{d}) \\ C\frac{d\tilde{v}_C}{dt} &= (-DI_L + I_{cl}) + (-D\tilde{i}_L - I_L\tilde{d} + \tilde{i}_{cl}) \\ n(I_g + \tilde{i}_g) &= (D'I_L - \frac{nV_g}{R}) + (D'\tilde{i}_L - I_L\tilde{d} - \frac{n\tilde{v}_g}{R}) \end{aligned} \tag{D.4}$$

DC-model of the CCM flyback auxiliary converter is obtained by equating the DC quantities on both sides of (D.4):

$$\begin{aligned} 0 = DV_c + D'\frac{V_g}{n} \quad &\Rightarrow \quad V_C = -\frac{D'}{Dn}V_g \\ 0 = -DI_L + I_{cl} \quad &\Rightarrow \quad I_L = \frac{I_{cl}}{D} \\ nI_g = D'I_L - \frac{nV_g}{R} \quad &\Rightarrow \quad I_g = \frac{D'}{nD}I_{cl} - \frac{V_g}{R} \end{aligned} \tag{D.5}$$

AC-model of the CCM flyback auxiliary converter is obtained by equating the AC quantities on both sides of (D.4):

$$\begin{aligned} L\frac{di_L}{dt} &= Dv_C + V_C d + D'\frac{v_g}{n} - \frac{V_g}{n}d \\ C\frac{dv_C}{dt} &= -Di_L - I_L d + i_{cl} \\ ni_g &= D'i_L - I_L d - \tfrac{nv_g}{R} \end{aligned} \tag{D.6}$$

where $\sim$ is omitted for brevity.

The small-signal AC model (D.6) is simply rewritten in the Laplace domain of complex variable s:

$$\begin{aligned} sLi_L(s) &= Dv_C(s) + (V_C - \frac{V_g}{n})d(s) + D'\frac{v_g(s)}{n} \\ sCv_C(s) &= -Di_L(s) - I_L d(s) + i_{cl}(s) \\ ni_g(s) &= D'i_L(s) - I_L d(s) - \tfrac{nv_g(s)}{R} \end{aligned} \tag{D.7}$$

The transfer function G_{vcd} from the duty cycle d to the capacitor voltage v_C is of utmost interest:

$$G_{vcd} = \left.\frac{v_c}{d}\right|_{v_g = i_{cl} = 0} \tag{D.8}$$

By setting $v_g = i_{cl} = 0$, the inductor current i_L can be expressed from the second equation in (D.7):

$$i_L = -\frac{sCv_c - I_L d}{D} \tag{D.9}$$

By replacing (D.9) in the first equation from (D.7), the following control-to-clamp-voltage control function for the CCM flyback auxiliary converter is obtained:

$$G_{vcd,ccm} = \left.\frac{v_c}{d}\right|_{v_g=i_{cl}=0} = \frac{V_g}{nD^2} \cdot \frac{1 - \frac{snLI_{cl}}{DV_g}}{1 + \frac{s^2LC}{D^2}} \tag{D.10}$$

D.2 Analysis of DCM flyback auxiliary converter

The state-space analysis of the DCM flyback auxiliary converter will be performed using its averaged switch model [60], shown with the circuit diagram in Fig. D.2. As a result of the discontinuous conduction mode, there are three different time intervals during each switching period T_s: on-time of the main switch during which the inductor current ramps up ($d_1 = d$), off-time of the main switch with decreasing inductor current (d_2) and off-time of the main switch with zero inductor current ($d_3 = 1 - d - d_2$).

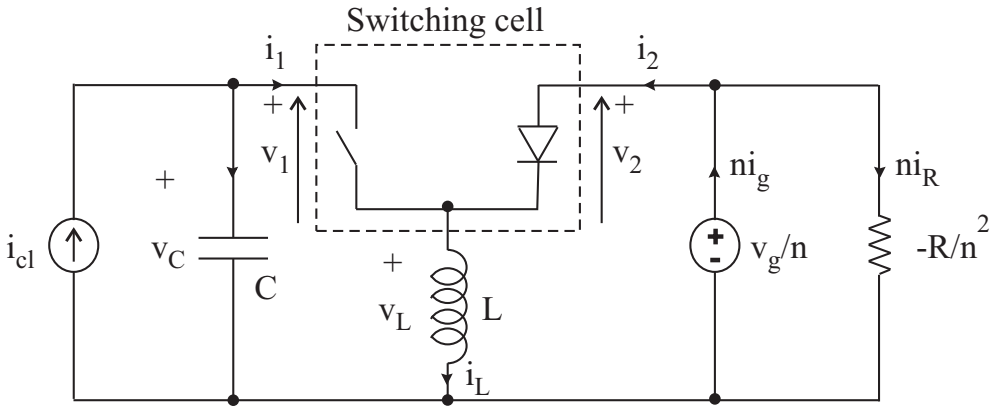

Fig. D.2. Averaged switch model of the DCM flyback auxiliary converter (same as Fig. 6.22)

The voltage equations for the switching cell of the DCM flyback auxiliary converter are:

- during interval t_{on} i.e. $d_1 = d$:

$$\begin{aligned} v_1 &= 0 \\ v_2 &= v_C - \frac{v_g}{n} \end{aligned} \tag{D.11}$$

- during interval t_{off1} i.e. d_2:

$$\begin{aligned} v_1 &= v_C - \frac{v_g}{n} \\ v_2 &= 0 \end{aligned} \tag{D.12}$$

- during interval t_{off2} i.e. $d_3 = 1 - d - d_2$:

$$\begin{aligned} v_1 &= v_C \\ v_2 &= -\frac{v_g}{n} \end{aligned} \tag{D.13}$$

In the next step, averaging of the state-space equations is performed to remove the switching harmonics present in the voltage waveforms and reveal the low frequency content. This corresponds to summing up equations (D.11), (D.12) and (D.13) weighted by their respective duty cycles:

$$\begin{aligned} v_1 &= (1-d)v_C - d_2\frac{v_g}{n} \\ v_2 &= dv_c - (1-d_2)\frac{v_g}{n} \end{aligned} \tag{D.14}$$

where all voltages are represented by their average values.

The average values of the switch currents i_1 and i_2 are calculated in the following way:

$$\begin{aligned} i_1 &= \frac{1}{T_s}\int_t^{t+T_s} i_1 d\tau = \frac{q_1}{T_s} = \frac{dT_s}{2T_s} i_{pk} = \frac{d}{2}\frac{dT_s v_c}{L} = \frac{d^2 T_s}{2L} v_c \\ i_2 &= \frac{1}{T_s}\int_t^{t+T_s} i_2 d\tau = \frac{q_2}{T_s} = \frac{d_2 T_s}{2T_s} i_{pk} = \frac{d_2}{2}\frac{dT_s v_c}{L} = \frac{d d_2 T_s}{2L} v_c \end{aligned} \tag{D.15}$$

Duty cycle d_2 is found by averaging inductor current waveform i_L:

$$i_L = \frac{1}{2} i_{pk}(d+d_2) = \frac{d(d+d_2)T_s}{2L} v_c \tag{D.16}$$

and expressing d_2:

$$d_2 = \frac{2Li_L}{dT_s v_C} - d = \left(\frac{R_e i_L}{v_C} - 1\right) d \tag{D.17}$$

where $R_e = (2L)/d^2 T_s$ represents the equivalent resistance of the lossless input port, which transfers the absorbed power to the output port.

Using the expression (D.17) for the duty cycle d_2, voltage v_1 and current i_2 can be written as:

$$\begin{aligned} v_1 &= (1-d)v_C + d\frac{v_g}{n} - \frac{2Li_L v_g}{ndT_s v_C} = \gamma_1(v_g, v_C, i_L, d) = k_g v_g + k_C v_C + r_1 i_L + f_1 d \\ i_2 &= i_L - \frac{d^2 T_s v_c}{2L} = \gamma_2(v_C, i_L, d) = g_C v_C + h_2 i_L + j_2 d \end{aligned} \tag{D.18}$$

where the coefficients are obtained by differentiating the input voltage v_1 and the output current i_2 of the averaged switch network in (D.18) and are given with the following expressions:

$$\begin{aligned} k_g &= \left.\frac{\partial \gamma_1(v_g, V_C, I_L, D)}{\partial v_g}\right|_{v_g = V_g} = \frac{D}{n} - \frac{2LI_L}{nDT_s V_C} \\ k_C &= \left.\frac{\partial \gamma_1(V_g, v_C, I_L, D)}{\partial v_C}\right|_{v_C = V_C} = (1-D) + \frac{2LI_L V_g}{nDT_s V_C^2} \\ r_1 &= \left.\frac{\partial \gamma_1(V_g, V_C, i_L, D)}{\partial i_L}\right|_{i_L = I_L} = -\frac{2LV_g}{nDT_s V_C} \\ f_1 &= \left.\frac{\partial \gamma_1(V_g, V_C, I_L, d)}{\partial d}\right|_{d=D} = -V_C + \frac{V_g}{n} + \frac{2LI_L V_g}{nD^2 T_s V_C} \end{aligned} \tag{D.19}$$

and:

$$
\begin{aligned}
g_C &= \left.\frac{\partial \gamma_2(v_C, I_L, D)}{\partial v_C}\right|_{v_c=V_C} = -\frac{D^2 T_s}{2L} \\
h_2 &= \left.\frac{\partial \gamma_2(V_C, i_L, D)}{\partial i_L}\right|_{i_L=I_L} = 1 \\
j_2 &= \left.\frac{\partial \gamma_2(V_C, I_L, d)}{\partial d}\right|_{d=D} = -\frac{DT_s V_C}{L}
\end{aligned}
\tag{D.20}
$$

The small-signal equivalent model of the DCM flyback auxiliary converter is depicted in Fig. D.3.

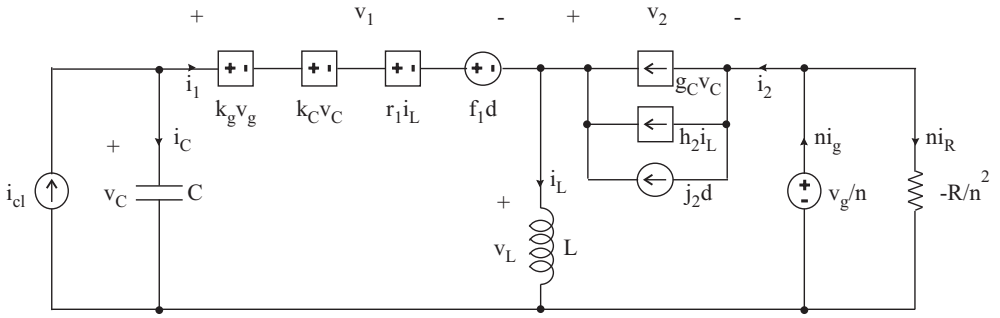

Fig. D.3. Small-signal AC model of DCM flyback auxiliary converter (same as Fig. 6.23)

In order to calculate the control-to-clamp-voltage transfer function of the DCM flyback auxiliary transformer $G_{vcd,dcm}$, it will be again assumed that $v_g = i_{cl} = 0$. From the equivalent circuit diagram in Fig. 6.23, capacitor voltage v_C can be represented as:

$$v_C = k_C v_C + r_1 i_L + f_1 d + sLi_L \tag{D.21}$$

where the inductor current i_L is to be eliminated.

Inductor current from the same diagram can be represented as:

$$
\begin{aligned}
i_L &= -sCv_C + g_C v_C + h_2 i_L + j_2 d \\
i_L &= \frac{-sCv_C + g_C v_C + j_2 d}{1 - h_2}
\end{aligned}
\tag{D.22}
$$

After replacing the inductor current i_L from (D.22) in (D.21), the following control-to-clamp-voltage control function for the DCM flyback auxiliary converter is obtained:

$$G_{vcd,dcm} = \left.\frac{v_c}{d}\right|_{v_g=i_{cl}=0} = \frac{f_1(1-h_2) + j_2(r_1 + sL)}{(1-k_C)(1-h_2) - (r_1 + sL)(g_c - sC)} \tag{D.23}$$

E

Analysis of control methods for SICAMs

E.1 Frequency spectrum of different PWM waveforms in isolated SICAMs

Double Fourier Series (DFS) of a periodical signal $F(x, y)$ being a function of two variables $x = \omega_c t$ and $y = \omega_m t$, where ω_c and ω_m are the carrier and modulating angular frequency, can be represented with the following equation [33]:

$$\begin{aligned} F(x,y) = \frac{1}{2}A_{00} &+ \sum_{n=1}^{\infty}\left[A_{0n}\cos(ny) + B_{0n}\sin(ny)\right] + \\ &+ \sum_{m=1}^{\infty}\left[A_{m0}\cos(mx) + B_{m0}\sin(mx)\right] + \\ &+ \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty}\left[A_{mn}\cos(mx+ny) + B_{mn}\sin(mx+ny)\right] \end{aligned} \tag{E.1}$$

where the Fourier coefficients are given with the expressions:

$$\begin{aligned} A_{00} &= \frac{1}{2\pi^2}\int_0^{2\pi}\int_0^{2\pi} F(x,y)dxdy \\ A_{0n} + iB_{0n} &= \frac{1}{2\pi^2}\int_0^{2\pi}\int_0^{2\pi} e^{iny}F(x,y)dxdy \\ A_{m0} + iB_{m0} &= \frac{1}{2\pi^2}\int_0^{2\pi}\int_0^{2\pi} e^{imx}F(x,y)dxdy \\ A_{mn} + iB_{mn} &= \frac{1}{2\pi^2}\int_0^{2\pi}\int_0^{2\pi} e^{i(mx+ny)}F(x,y)dxdy \end{aligned} \tag{E.2}$$

E.1.1 Double Fourier Series of $F_{NADS,1h}$

The main building block for developing all other PWM waveforms through time-scale inversion and phase-shifting is the two-level single-sided PWM waveform F_{NADS} [33]. In the case of HF-link converters where the frequency of the triangular carrier f_{c2} is two times the HF-link frequency f_{HF}, $f_{c2} = 2f_{HF}$, a modification of the same waveform is required, where each second PWM pulse is skipped $F_{NADS,1h}$. It is essentially a three-level waveform, where just two levels are used in the active intervals, while in the skipped intervals zero is inserted. Its graphical derivation is depicted in Fig. E.1. The coefficient $k = T_{c2}/(4 \cdot T_{HF})$ in fact defines the maximum duty cycle D_{max} of the PWM waveform and for the particular case $f_{c2} = 2f_{HF}$ is $k = 0.125$.

Fourier coefficient A_{00} of $F_{NADS,1h}$ is:

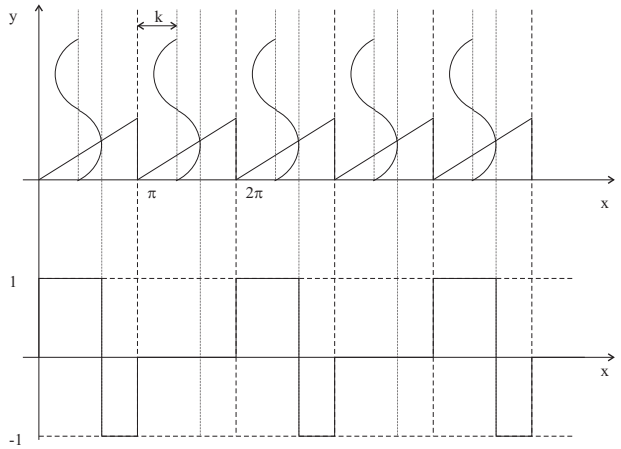

Fig. E.1. Diagram of $F_{NADS,1h}$ for developing its DFS

$$\begin{aligned} A_{00} &= \frac{1}{2\pi^2}\int_0^{2\pi}\left[\int_0^{2\pi k+2\pi kM\cos y} dx - \int_{2\pi k+2\pi kM\cos y}^{4\pi k} dx\right]dy = \\ &= \frac{1}{\pi}\Big[4\pi kM\cos y\Big] = 4kM\cos y \end{aligned} \tag{E.3}$$

Fourier coefficients A_{0n} and B_{0n} of $F_{NADS,1h}$ are:

$$\begin{aligned} A_{0n} + iB_{0n} &= \frac{1}{2\pi^2}\int_0^{2\pi}\left[\int_0^{2\pi k+2\pi kM\cos y} e^{iny}dx - \int_{2\pi k+2\pi kM\cos y}^{4\pi k} e^{iny}dx\right]dy = \\ &= \frac{1}{2\pi^2}\int_0^{2\pi} 4\pi kM\cos y e^{iny}dy = 0 \end{aligned} \tag{E.4}$$

Fourier coefficients A_{m0} and B_{m0} of $F_{NADS,1h}$ are:

$$\begin{aligned} A_{m0} + iB_{m0} &= \frac{1}{2\pi^2}\int_0^{2\pi}\left[\int_0^{2\pi k+2\pi kM\cos y} e^{imx}dx - \int_{2\pi k+2\pi kM\cos y}^{4\pi k} e^{imx}dx\right]dy = \\ &= -\frac{i}{2\pi^2 m}\int_0^{2\pi}\Big[2e^{i(2\pi mk+2\pi mkM\cos y)} - 1 - e^{i4\pi mk}\Big]dy = \\ &= -\frac{i}{\pi^2 m}e^{i(2\pi mk)}\int_0^{2\pi} e^{i(2\pi mkM\cos y)}dy + \frac{i}{\pi m}\Big(1 + e^{i4\pi mk}\Big) = \\ &= \frac{2e^{i(2\pi mk-\frac{\pi}{2})}}{m\pi}J_0(2\pi mkM) + \frac{e^{i\frac{\pi}{2}}}{m\pi} + \frac{e^{i(4\pi mk+\frac{\pi}{2})}}{m\pi} = \\ &= \left[\frac{2\cos(2\pi mk-\frac{\pi}{2})}{m\pi}J_0(2\pi mkM) + \frac{\cos(4\pi mk+\frac{\pi}{2})}{m\pi}\right] + \\ &+ i\left[\frac{2\sin(2\pi mk-\frac{\pi}{2})}{m\pi}J_0(2\pi mkM) + \frac{1+\sin(4\pi mk+\frac{\pi}{2})}{m\pi}\right] \end{aligned} \tag{E.5}$$

Fourier coefficients A_{mn} and B_{mn} of $F_{NADS,1h}$ are:

$$
\begin{aligned}
A_{mn}+iB_{mn} &= \frac{1}{2\pi^2}\int_0^{2\pi}\left[\int_0^{2\pi k+2\pi kM\cos y} e^{i(mx+ny)}dx - \int_{2\pi k+2\pi kM\cos y}^{4\pi k} e^{i(mx+ny)}dx\right]dy = \\
&= -\frac{i}{2\pi^2 m}\int_0^{2\pi}\left[2e^{i(2\pi mk+2\pi mkM\cos y)}e^{iny} - e^{iny} - e^{i4\pi mk}e^{iny}\right]dy = \\
&= -\frac{i}{\pi^2 m}e^{i(2\pi mk)}\int_0^{2\pi} e^{i(2\pi mkM\cos y)}e^{iny}dy = \frac{2}{\pi m}e^{i(2\pi mk+\frac{(n-1)\pi}{2})}J_n(2\pi mkM) = \\
&= \left[\frac{2\cos(2\pi mk+\frac{(n-1)\pi}{2})}{m\pi}J_n(2\pi mkM)\right]+ \\
&+ i\left[\frac{2\sin(2\pi mk+\frac{(n-1)\pi}{2})}{m\pi}J_n(2\pi mkM)\right]
\end{aligned}
\tag{E.6}
$$

E.1.2 Double Fourier Series of $F_{NADS,2h}$

$F_{NADS,2h}$ essentially represents the same waveform $F_{NADS,1h}$ shown in Fig. E.1, but is shifted for π rad. Therefore, the DFS of $F_{NADS,2h}$ can be calculated by starting from the DFS of $F_{NADS,1h}$ and shifting it appropriately in the time domain. It can also be developed in a thorough mathematical way like already done for $F_{NADS,1h}$ in the previous section, and this method will be shown below.

Fourier coefficient A_{00} of $F_{NADS,2h}$ is:

$$
\begin{aligned}
A_{00} &= \frac{1}{2\pi^2}\int_0^{2\pi}\left[\int_{4\pi k}^{6\pi k+2\pi kM\cos y} dx - \int_{6\pi k+2\pi kM\cos y}^{8\pi k} dx\right]dy = \\
&= \frac{1}{\pi}\left[4\pi kM\cos y\right] = 4kM\cos y
\end{aligned}
\tag{E.7}
$$

Fourier coefficients A_{0n} and B_{0n} of $F_{NADS,2h}$ are:

$$
\begin{aligned}
A_{0n}+iB_{0n} &= \frac{1}{2\pi^2}\int_0^{2\pi}\left[\int_{4\pi k}^{6\pi k+2\pi kM\cos y} e^{iny}dx - \int_{6\pi k+2\pi kM\cos y}^{8\pi k} e^{iny}dx\right]dy = \\
&= \frac{1}{2\pi^2}\int_0^{2\pi} 4\pi kM\cos y e^{iny}dy = 0
\end{aligned}
\tag{E.8}
$$

Fourier coefficients A_{m0} and B_{m0} of $F_{NADS,2h}$ are:

$$
\begin{aligned}
A_{m0}+iB_{m0} &= \frac{1}{2\pi^2}\int_0^{2\pi}\left[\int_{4\pi k}^{6\pi k+2\pi kM\cos y} e^{imx}dx - \int_{6\pi k+2\pi kM\cos y}^{8\pi k} e^{imx}dx\right]dy = \\
&= -\frac{i}{2\pi^2 m}\int_0^{2\pi}\left[2e^{i(6\pi mk+2\pi mkM\cos y)} - e^{i4\pi mk} - e^{i8\pi mk}\right]dy = \\
&= -\frac{i}{\pi^2 m}e^{i(6\pi mk)}\int_0^{2\pi} e^{i(2\pi mkM\cos y)}dy + \frac{i}{\pi m}\left(e^{i4\pi mk}+e^{i8\pi mk}\right) = \\
&= \frac{2e^{i(6\pi mk-\frac{\pi}{2})}}{m\pi}J_0(2\pi mkM) + \frac{e^{i\frac{\pi}{2}}}{m\pi}\left(e^{i4\pi mk}+e^{i8\pi mk}\right) = \\
&= \left[\frac{2\cos(6\pi mk-\frac{\pi}{2})}{m\pi}J_0(2\pi mkM) + \frac{\cos(4\pi mk+\frac{\pi}{2})}{m\pi} + \frac{\cos(8\pi mk+\frac{\pi}{2})}{m\pi}\right]+ \\
&+ i\left[\frac{2\sin(6\pi mk-\frac{\pi}{2})}{m\pi}J_0(2\pi mkM) + \frac{\sin(4\pi mk+\frac{\pi}{2})+\sin(8\pi mk+\frac{\pi}{2})}{m\pi}\right]
\end{aligned}
\tag{E.9}
$$

Fourier coefficients A_{mn} and B_{mn} of $F_{NADS,2h}$ are:

$$
\begin{aligned}
A_{mn} + iB_{mn} &= \frac{1}{2\pi^2}\int_0^{2\pi}\left[\int_{4\pi k}^{6\pi k+2\pi kM\cos y} e^{i(mx+ny)}dx - \int_{6\pi k+2\pi kM\cos y}^{8\pi k} e^{i(mx+ny)}dx\right]dy = \\
&= -\frac{i}{2\pi^2 m}\int_0^{2\pi}\left[2e^{i(6\pi mk+2\pi mkM\cos y)}e^{iny} - e^{i4\pi mk}e^{iny} - e^{i8\pi mk}e^{iny}\right]dy = \\
&= -\frac{i}{\pi^2 m}e^{i(6\pi mk)}\int_0^{2\pi} e^{i(2\pi mkM\cos y)}e^{iny}dy = \frac{2}{\pi m}e^{i(6\pi mk+\frac{(n-1)\pi}{2})}J_n(2\pi mkM) = \\
&= \left[\frac{2\cos(6\pi mk+\frac{(n-1)\pi}{2})}{m\pi}J_n(2\pi mkM)\right]+ \\
&+ i\left[\frac{2\sin(6\pi mk+\frac{(n-1)\pi}{2})}{m\pi}J_n(2\pi mkM)\right]
\end{aligned}
\tag{E.10}
$$

E.1.3 Double Fourier Series of $F_{NADD,1h}$

$F_{NADD,1h}$ is a two-level double-sided PWM waveform with a value of zero in the even half-periods. Since the changes in the PWM waveform correspond to the intersections of the sinusoidal reference signal with a double-sided triangular carrier, $F_{NADD,1h}$ is actually constituted from two $F_{NADS,1h}$ waveforms, where the second one has inverted time scale. Taking into consideration the coefficients of $F_{NADS,1h}$ in (E.3)-(E.6), DFS of $F_{NADD,1h}$ becomes:

$$
\begin{aligned}
F_{NADD,1h}(t,\varphi) &= F_{NADS,1h}(t,\varphi) + F_{NADS,1h}(-t,\varphi) = \\
&= 4kM\cos(y+\varphi)+ \\
&+ 2\sum_{m=1}^{\infty}\left[\frac{2\cos(2\pi mk-\frac{\pi}{2})}{m\pi}J_0(2\pi mkM) + \frac{\cos(4\pi mk+\frac{\pi}{2})}{m\pi}\right]\cos(mx)+ \\
&+ 2\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\left[\frac{2\cos(2\pi mk+\frac{(n-1)\pi}{2})}{m\pi}J_n(2\pi mkM)\cos(mx+ny)\cos(n\varphi)+\right. \\
&\quad \left.+\frac{2\sin(2\pi mk+\frac{(n-1)\pi}{2})}{m\pi}J_n(2\pi mkM)\sin(mx+ny)\sin(n\varphi)\right] = \\
&= 4kM\cos(y+\varphi)+ \\
&+ 2\sum_{m=1}^{\infty}\left[\frac{2\cos(2\pi mk-\frac{\pi}{2})}{m\pi}J_0(2\pi mkM) + \frac{\cos(4\pi mk+\frac{\pi}{2})}{m\pi}\right]\cos(mx)+ \\
&+ 4\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\frac{\cos(2\pi mk+\frac{(n-1)\pi}{2}-n\varphi)}{m\pi}J_n(2\pi mkM)\cos(mx+ny+n\varphi)
\end{aligned}
\tag{E.11}
$$

E.1.4 Double Fourier Series of $F_{NADD,2h}$

$F_{NADD,2h}$ is a two-level double-sided PWM waveform with a value of zero in the odd half-periods and represents a time-shifted version of $F_{NADD,1h}$. Its DFS can be obtained either by shifting the DFS of $F_{NADD,1h}$ in (E.11) or by calculating it from the coefficients of $F_{NADS,2h}$ in (E.7)-(E.10). The latter approach is shown below:

$$
\begin{aligned}
F_{NADD,2h}(t,\varphi) &= -\big[F_{NADS,2h}(t,\varphi+\pi)+F_{NADS,2h}(-t,\varphi+\pi)\big]= \\
&= -4kM\cos(y+\varphi+\pi)- \\
&-2\sum_{m=1}^{\infty}\left[\frac{2\cos(6\pi mk-\frac{\pi}{2})}{m\pi}J_0(2\pi mkM)+\frac{\cos(4\pi mk+\frac{\pi}{2})+\cos(8\pi mk+\frac{\pi}{2})}{m\pi}\right]\cos(mx)- \\
&-2\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\left[\frac{2\cos(6\pi mk+\frac{(n-1)\pi}{2})}{m\pi}J_n(2\pi mkM)\cos(mx+ny)\cos(n\varphi+n\pi)+\right. \\
&\quad\left.+\frac{2\sin(6\pi mk+\frac{(n-1)\pi}{2})}{m\pi}J_n(2\pi mkM)\sin(mx+ny)\sin(n\varphi+n\pi)\right]= \\
&= 4kM\cos(y+\varphi)- \\
&-2\sum_{m=1}^{\infty}\left[\frac{2\cos(6\pi mk-\frac{\pi}{2})}{m\pi}J_0(2\pi mkM)+\frac{\cos(4\pi mk+\frac{\pi}{2})+\cos(8\pi mk+\frac{\pi}{2})}{m\pi}\right]\cos(mx)- \\
&-4\sum_{m=1}^{\infty}\sum_{n=\pm1}^{\pm\infty}\frac{\cos(6\pi mk+\frac{(n-1)\pi}{2}-n(\varphi+\pi))}{m\pi}J_n(2\pi mkM)\cos(mx+ny+n\varphi)
\end{aligned}
\tag{E.12}
$$

It should be noted that the minus sign in the first row of (E.12) is result of the fact that the PWM waveform is inverted during the even half-periods because of the negative voltage of the HF-link. On the other hand, the phase of the sinusoidal reference signal is $\varphi+\pi$ because the input to the PWM modulator during the half-periods with negative HF-link voltage is inverted, as explained in Section 7.2.2.

E.2 Switching frequency of GLIM self-oscillating modulator

Switching frequency of the GLIM self-oscillating modulator will be calculated using the waveform in Fig. E.2.

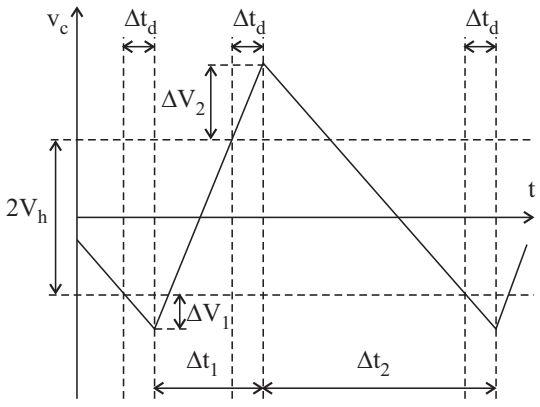

Fig. E.2. GLIM carrier

Due to the delay t_d in the modulator loop, carrier voltage v_c overshoots the hysteresis window $2V_h$ in amount of:

$$
\begin{aligned}
\Delta V_1 &= \frac{V_s(1-M)}{\tau k_a}\Delta t_d \\
\Delta V_2 &= \frac{V_s(1+M)}{\tau k_a}\Delta t_d
\end{aligned}
\tag{E.13}
$$

where V_s is the supply voltage, M is the modulation index, $\tau = 1/(2\pi\sqrt{L_f C_f})$ is the integration constant found also in the MFB block, k_a is the amplifier gain and Δt_d is the modulator loop delay.

Time intervals Δt_1 and Δt_2 corresponding to the rising and falling intervals of the carrier waveform v_c can be determined with the following equations:

$$\begin{aligned} \Delta t_1 &= \frac{(2V_h + \Delta V_1 + \Delta V_2)\tau k_a}{V_s(1+M)} \\ \Delta t_2 &= \frac{(2V_h + \Delta V_1 + \Delta V_2)\tau k_a}{V_s(1-M)} \end{aligned} \tag{E.14}$$

Switching frequency of the GLIM modulator is:

$$\begin{aligned} f_s &= \frac{1}{\Delta t_1 + \Delta t_2} = \frac{V_s(1-M^2)}{2(2V_h + \Delta V_1 + \Delta V_2)\tau k_a} = \\ &= \frac{V_s}{4}\frac{(1-M^2)}{V_h \tau k_a + V_s \Delta t_d} \end{aligned} \tag{E.15}$$

In order to improve the power supply rejection ratio and make the switching frequency independent of the supply voltage, the hysteresis window is usually chosen to be linear function of the supply voltage:

$$V_h = k_h V_s \tag{E.16}$$

In this case, the switching frequency from (E.15) becomes:

$$f_s = \frac{1}{4}\frac{(1-M^2)}{\tau k_h k_a + \Delta t_d} \tag{E.17}$$

F

Prototype schematics

F.1 Schematics of isolated SICAM with master/slave operation

Circuit schematics of the isolated SICAM with master/slave operation are given in Fig. F.1, Fig. F.2 and Fig. F.3.

F.2 Schematics of isolated SICAM with active capacitive load voltage clamp

Circuit schematics of the isolated SICAM with active capacitive load voltage clamp are given in Fig. F.4 and Fig. F.5.

F.3 Schematics of isolated SICAM with optimized PWM modulator and safe-commutation switching sequence

Circuit schematics of the isolated SICAM with optimized PWM modulator and safe-commutation switching sequence are given in Fig. F.6 and Fig. F.7.

F.4 Schematics of isolated self-oscillating SICAM with GLIM modulator

Circuit schematics of the isolated self-oscillating SICAM with GLIM modulator are given in Fig. F.8 and Fig. F.9.

F.5 Schematics of 4Q flyback SICAM

Circuit schematics of the 4Q flyback SICAM are given in Fig. F.10 and Fig. F.11.

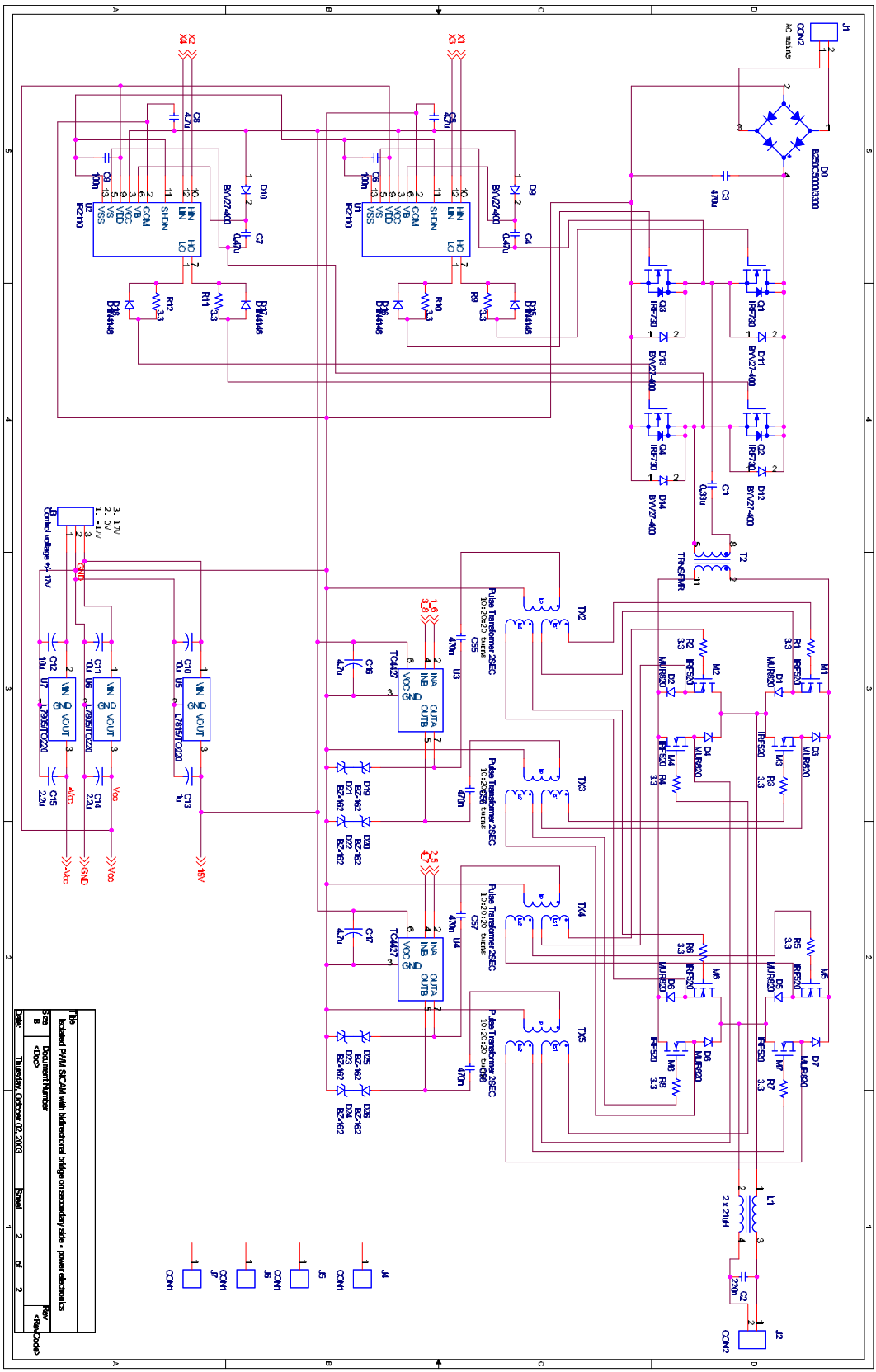

Fig. F.1. Power circuit schematic of the isolated SICAM with master/slave operation

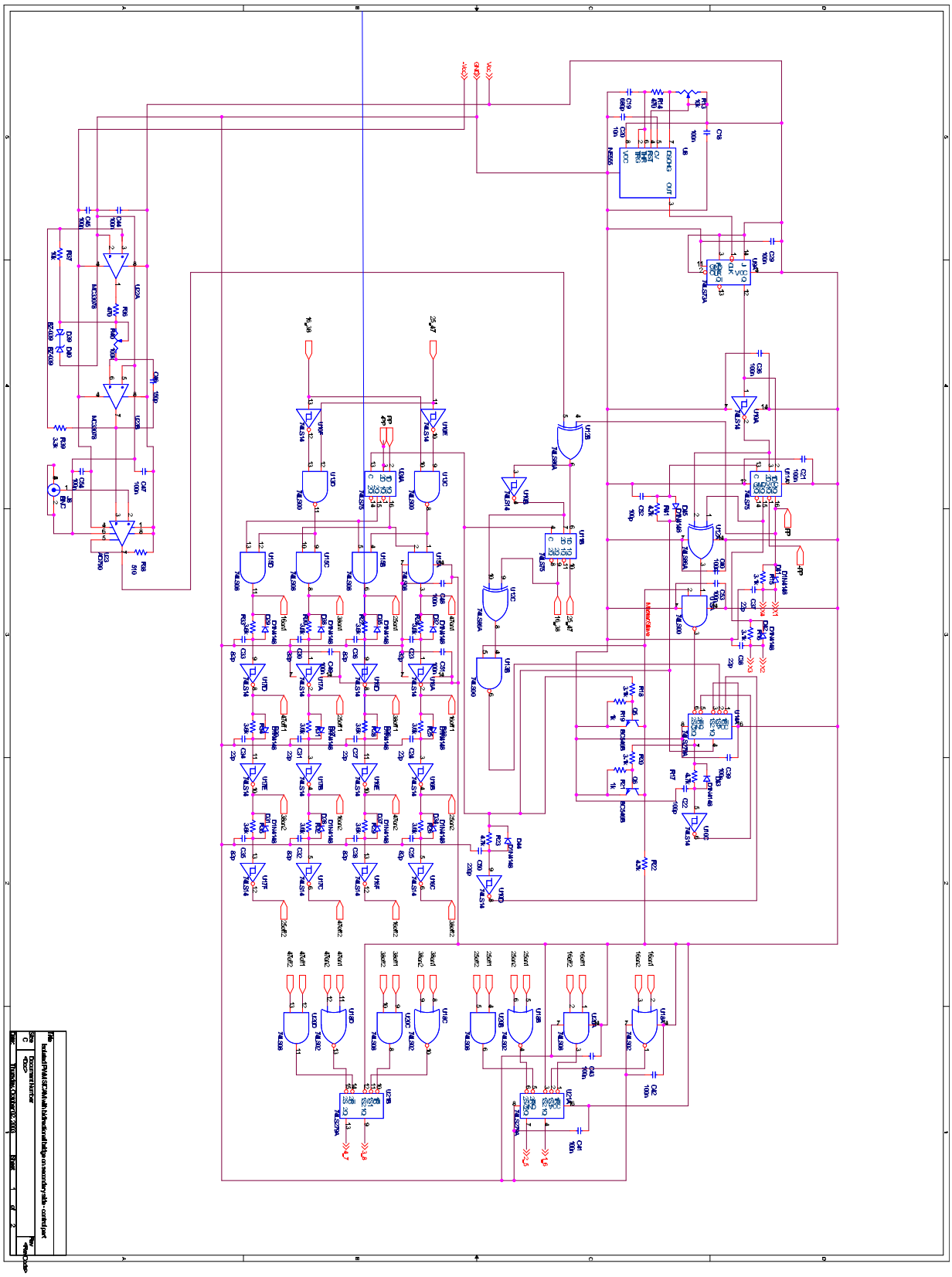

Fig. F.2. Open-loop control circuit schematic of the isolated SICAM with master/slave operation

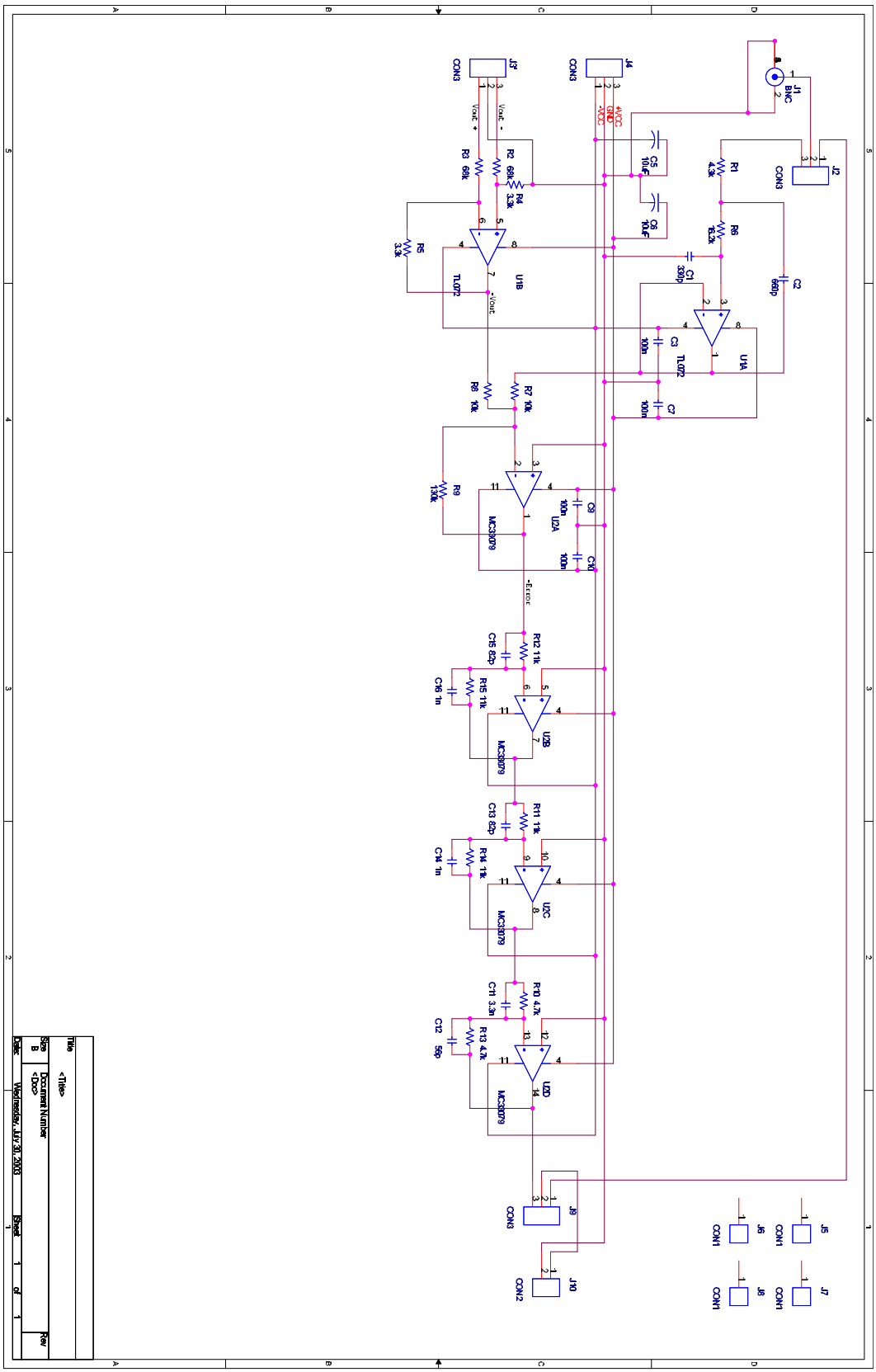

Fig. F.3. Closed-loop control circuit schematic of the isolated SICAM with master/slave operation

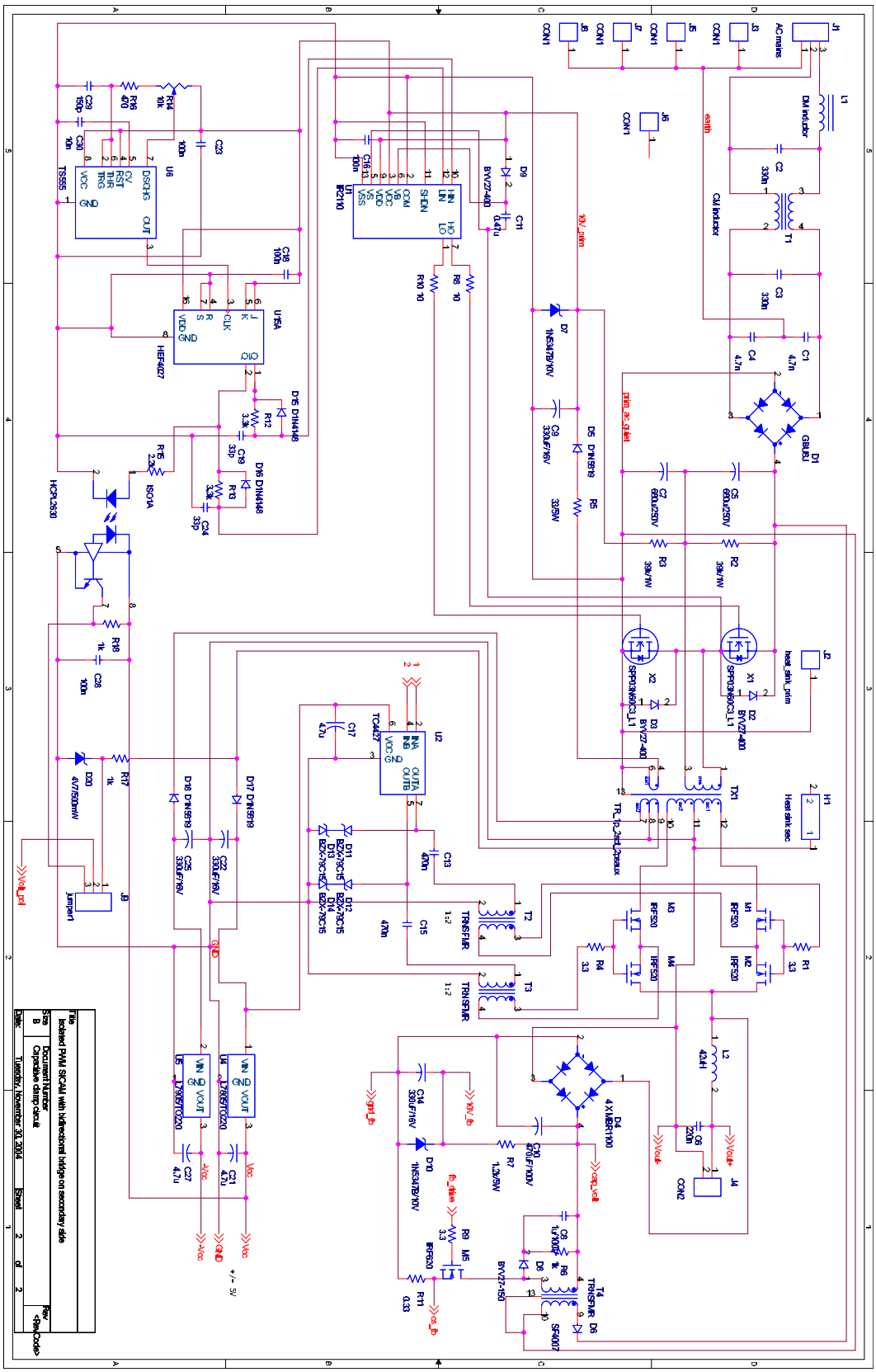

Fig. F.4. Power circuit schematic of the isolated SICAM with active capacitive load voltage clamp

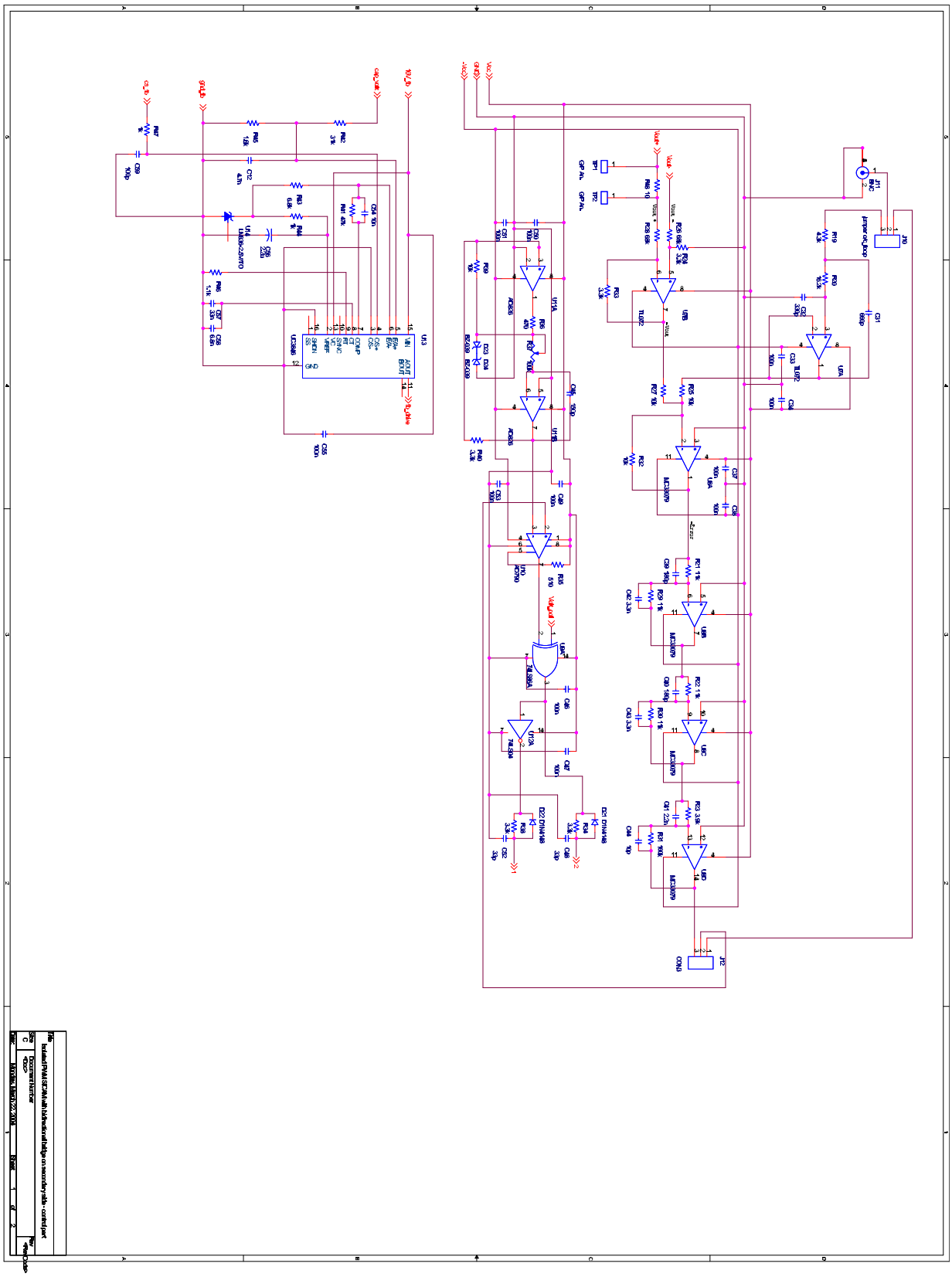

Fig. F.5. Control circuit schematic of the isolated SICAM with active capacitive load voltage clamp

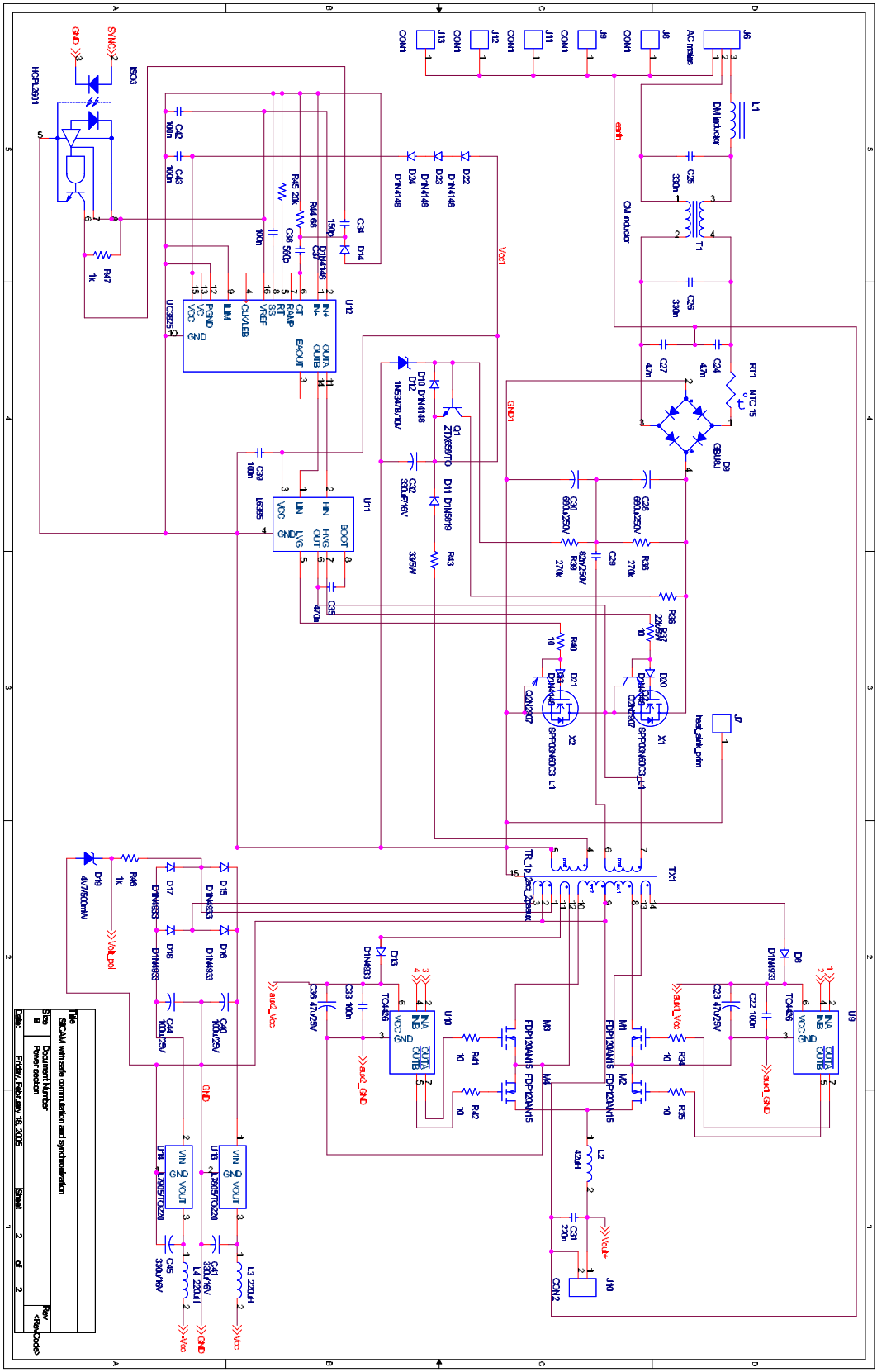

Fig. F.6. Power circuit schematic of the isolated SICAM with optimized PWM modulator and safe-commutation switching sequence

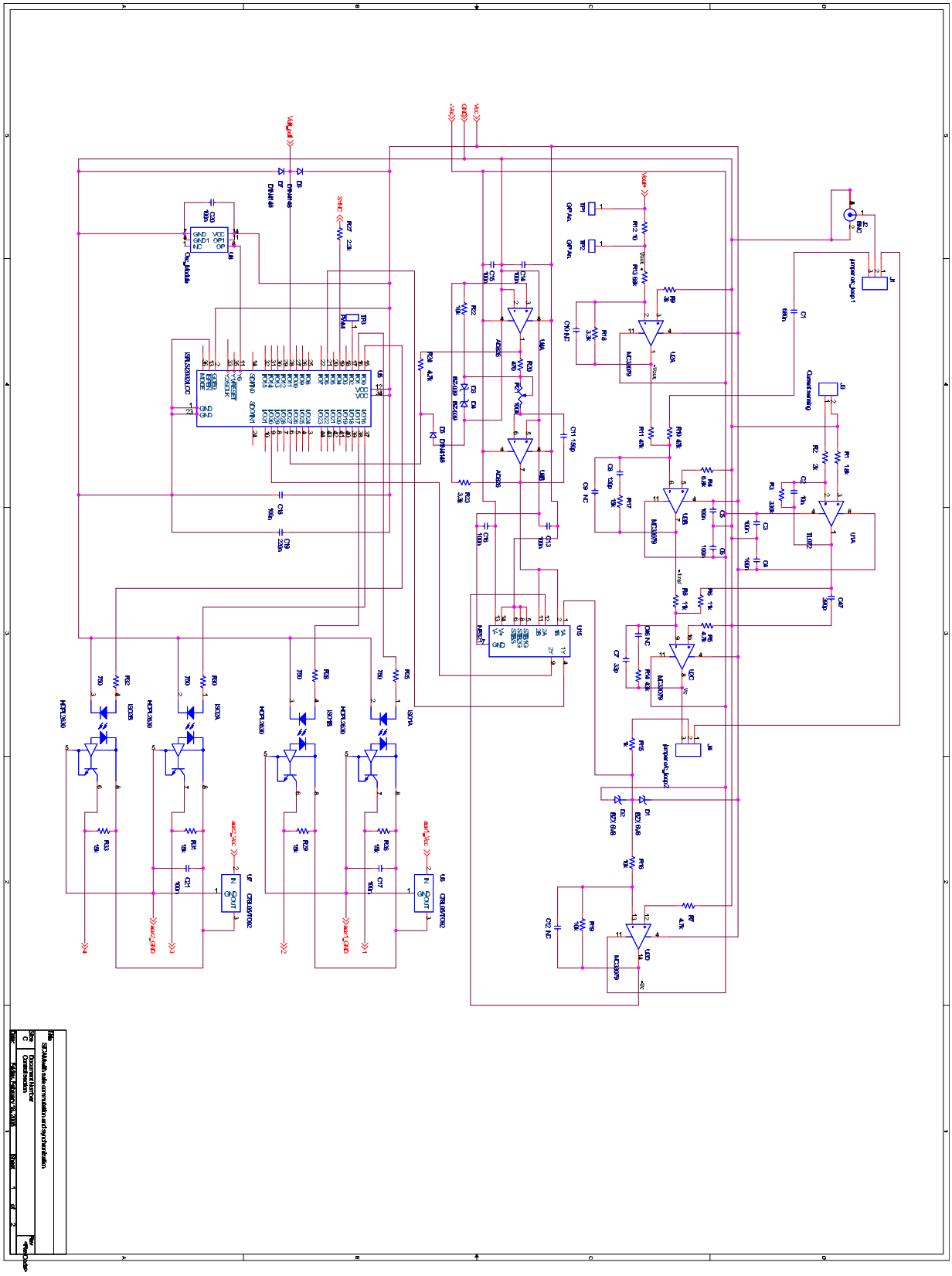

Fig. F.7. Control circuit schematic of the isolated SICAM with optimized PWM modulator and safe-commutation switching sequence

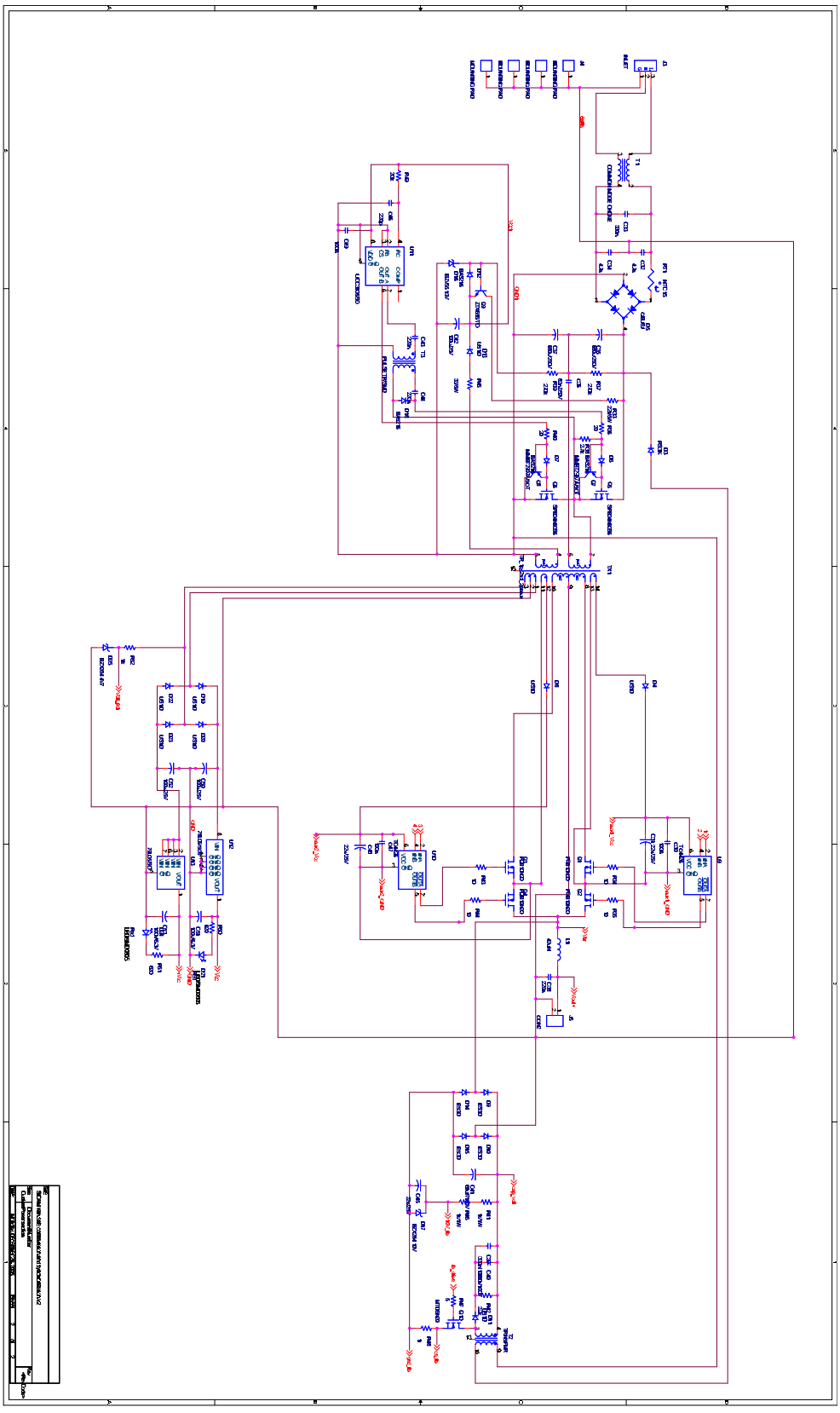

Fig. F.8. Power circuit schematic of the isolated self-oscillating SICAM with GLIM modulator

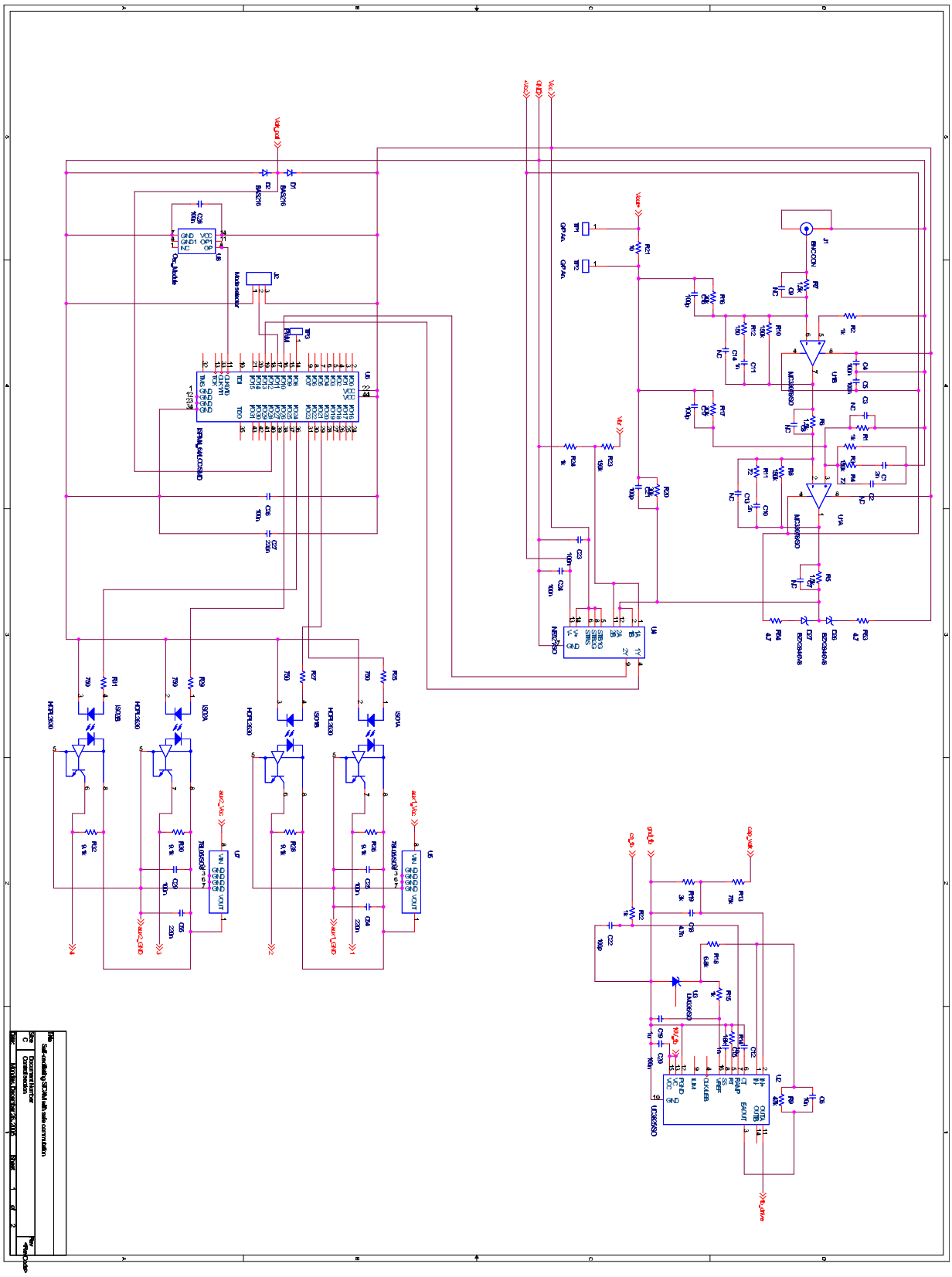

Fig. F.9. Control circuit schematic of the isolated self-oscillating SICAM with GLIM modulator

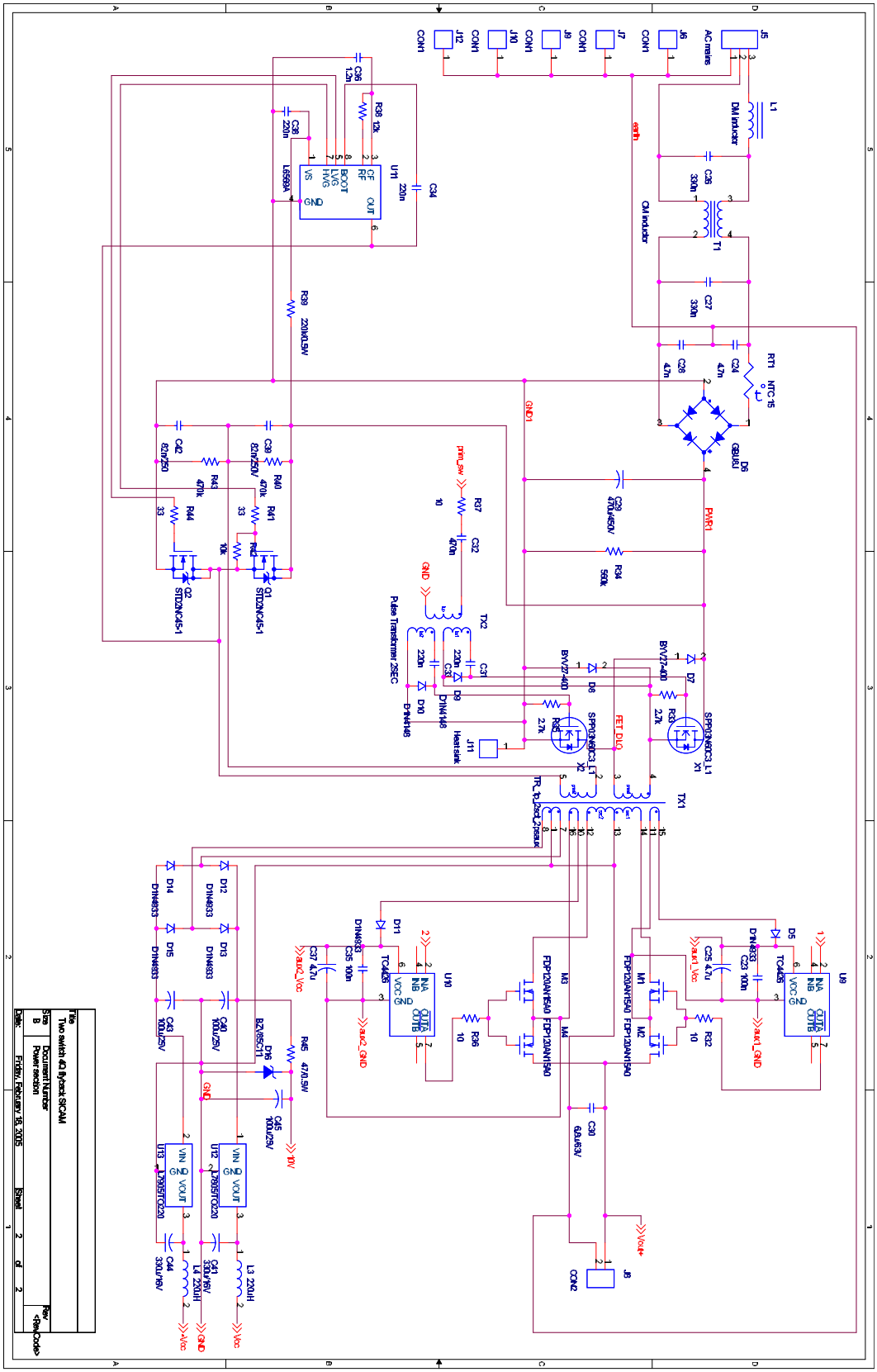

Fig. F.10. Power circuit schematic of the 4Q flyback SICAM

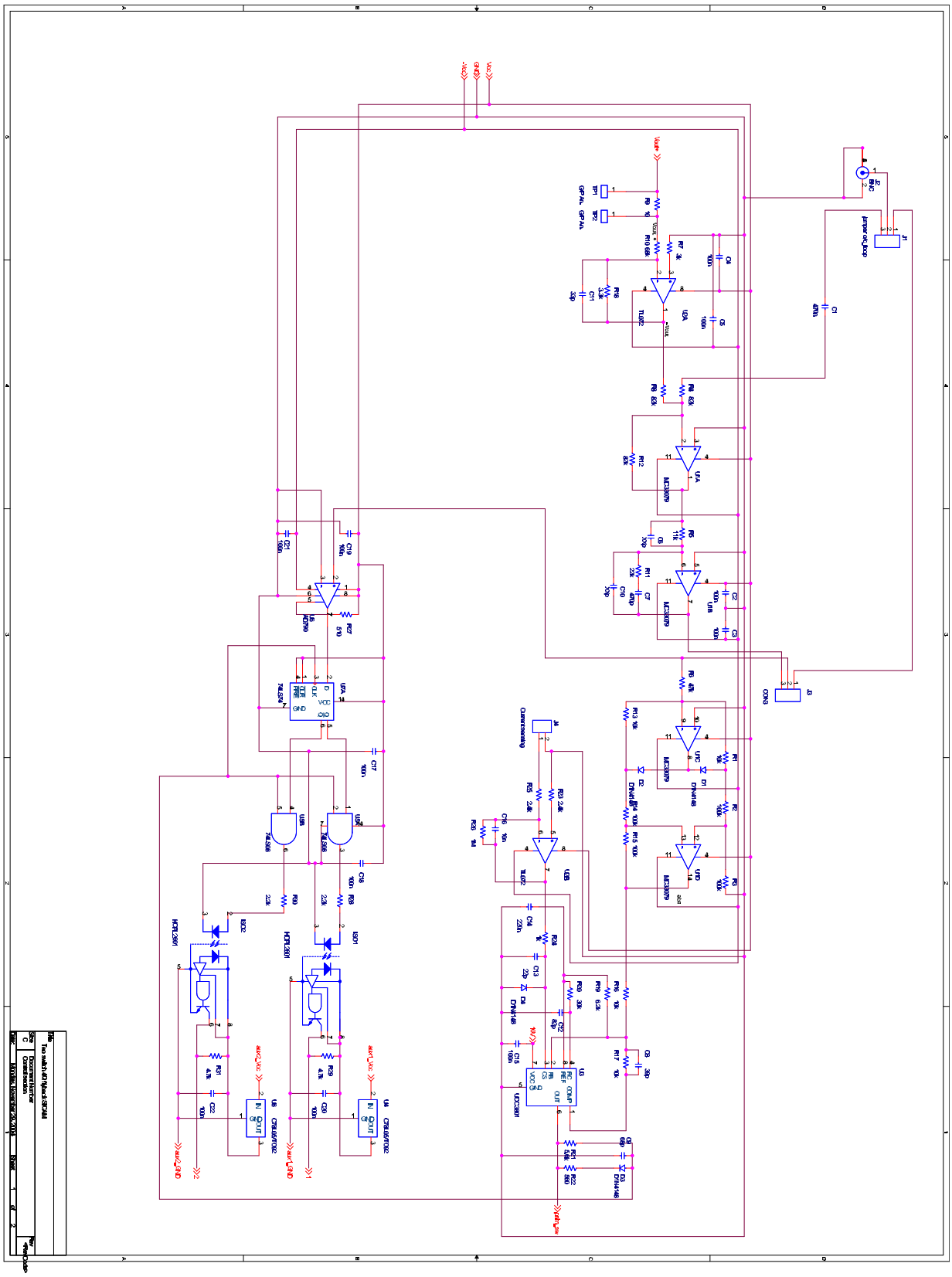

Fig. F.11. Control circuit schematic of the 4Q flyback SICAM

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