Piezoresistivity in Microsystems

Richter, Jacob; Hansen, Ole; Thomsen, Erik Vilain; Christensen, Carsten

Publication date:
2008

Document Version
Publisher's PDF, also known as Version of record

Piezoresistivity in Microsystems

PhD Thesis

Jacob Richter

January 1st 2008

DTU Nanotech - Department of Micro and Nanotechnology
Technical University of Denmark

Abstract

This thesis is a contribution to the research in piezoresistive micro electro mechanical system (MEMS) sensors. Today, a wide range of piezoresistive silicon sensors are commercially available. This thesis focuses on experimental characterization of piezoresistive materials all based on silicon micro and nanotechnology fabrication techniques. With a basis in the characterization of silicon, the piezoresistive properties of other materials are explored in order to search for materials for use in highly sensitive sensors. The piezoresistive properties of silicon are described by the three piezocoefficients, π_{11}, π_{12}, and π_{44}. In this thesis the fundamental theory of piezoresistivity is explained and different experimental piezoresistance characterization structures are suggested.

In order to realize the experimental characterization a four point bending fixture is designed and fabricated. The setup includes heaters embedded in the housing and thermocouples in order to allow for precise temperature control. The setup applies a uniaxial stress to the inserted chip and provides a high precision measurement of π_{44} in p-type silicon with an uncertainty of 1.8%.

By using the four point bending setup the piezocoefficients of n-type silicon are experimentally determined as a function of doping concentration N_D and temperature T: $\pi_{11} = -97 \cdot 10^{-11}$ Pa^{-1}, $\pi_{12} = 43 \cdot 10^{-11}$ Pa^{-1}, and $\pi_{44} = -12 \cdot 10^{-11}$ Pa^{-1} ($N_D = 5.1 \cdot 10^{17}$ cm^{-3}, $T = 30$°C). In p-type silicon the experimental characterization gives: $\pi_{44} = 118 \cdot 10^{-11}$ Pa^{-1} at a doping concentration of $N_A = 1.5 \cdot 10^{17}$ cm^{-3} and $T = 30$°C. The temperature dependency of the piezocoefficients decreases for increasing doping concentration . A theoretical model is developed in order to describe how π_{44} in p-type silicon depends on the temperature and doping concentration, since this piezocoefficient has a very large technological relevance. A simple analytical fit has been applied to this model. The fit is intended to be used by experimentalists when the performance of a designed piezoresistive MEMS device is to be predicted.

In the search for highly sensitive piezoresistive materials biaxially pre-strained silicon and silicon germanium grown by molecular beam epitaxy are characterized experimentally. The results show that the strain of the crystal lattice indeed influence the piezoresistive properties. By compressively straining silicon germanium π_{66}, which is equivalent to π_{44} in silicon, increases up to 36% compared to π_{44} in silicon, and in biaxially tensile strained silicon π_{66} is decreased by 25% compared to π_{44} in silicon. The temperature dependency of the piezocoefficients is highly influenced by the strain and the experiments show that the temperature dependency of the piezocoefficient in strained silicon, $\frac{1}{\pi_{66}}\frac{\partial \pi_{66}}{\partial T} = 0.1\%/°\text{C}$, is much smaller than that of bulk silicon, $\frac{1}{\pi_{44}}\frac{\partial \pi_{44}}{\partial T} = 0.35\%/°\text{C}$.

Silicon nanowires are characterized experimentally and the decrease in size has a large impact on the piezoresistance properties. An increase in the piezocoefficient π_{44} of up to approximately

630% compared to that of bulk p-type silicon is observed.

This thesis provides new knowledge to the field of piezoresistive MEMS and NEMS and improves the understanding of piezoresistivity in general. The results obtained in this thesis proof that it is possible to obtain highly sensitive piezoresistive materials by manipulating the crystal structure of silicon or by decreasing the component size. The results from this thesis is to be used as building blocks towards a new MEMS and NEMS generation of highly sensitive piezoresistive sensors.

Resumé (in Danish)

Denne afhandling er et bidrag til forskningen indenfor piezoresistive mikro elektro mekaniske system (MEMS) sensorer. Der findes i dag en bred vifte af kommercielle piezoresistive silicium sensorer. Denne afhandling fokuserer på den eksperimentelle karakterisering af piezoresistive materialer, som er fremstillet ved silicium baseret mikro- og nanoteknologiske fabrikationsteknikker. Med udgangspunkt i karakterisering af silicium er de piezoresistive egenskaber i andre materialer undersøgt med fokus på at finde materialer der kan bruges til sensorer med høj følsomhed. De piezoresistive egenskaber i silicium er beskrevet ved de tre piezokoefficienter π_{11}, π_{12} og π_{44}. I denne afhandling beskrives den fundamentale teori omhandlende piezoresistivitet og der foreslås forskellige piezoresistive karakteriseringsstrukturer.

En fire punkts bøjning forsøgsopstilling er designet og fabrikeret for at kunne udføre de eksperimentelle karakteriseringer. I opstillingen er der inkluderet varmeelementer og temperaturmålere for at kunne udføre præcise målinger ved forskellige temperaturer. Opstillingen påfører en uniaksial mekanisk spænding til den indsatte chip og måler med høj præcision piezokoefficienten π_{44} i p-type silicium med en usikkerhed på 1.8%.

Ved brug af fire punkts bøjning opstillingen bestemmes piezokoefficienterne i n-type silicium som en funktion af doping koncentration N_D og temperatur T: $\pi_{11} = -97 \cdot 10^{-11}$ Pa^{-1}, $\pi_{12} = 43 \cdot 10^{-11}$ Pa^{-1} og $\pi_{44} = -12 \cdot 10^{-11}$ Pa^{-1} ($N_D = 5.1 \cdot 10^{17}$ cm^{-3}, $T = 30$°C). I p-type silicium giver den eksperimentelle karakterisering følgende resultat: $\pi_{44} = 118 \cdot 10^{-11}$ Pa^{-1} for en doping koncentration på $N_A = 1.5 \cdot 10^{17}$ cm^{-3} ved $T = 30$°C. For p-type silicium er der yderligere udviklet en teoretisk model som beskriver π_{44} som funktion af temperatur og doping koncentration. Da π_{44} har en stor teknologisk relevans er der til denne model udviklet et simpelt analytisk fit. Dette fit er tiltænkt eksperimentalister til brug når følsomheden af en designet piezoresistiv MEMS sensor skal estimeres.

I søgen efter højt følsomme piezoresistive materialer karakteriseres prøver med biaksialt strakt silicium og biaksialt sammentrukket silicium germanium krystaller. Disse lag er fabrikeret ved hjælp af metoden molekylær stråle epitaxy. I sammentrukket silicium germanium opnås en forstørrelse af π_{66}, som er direkte sammenlignelig med π_{44} i silicium, på 36% i forhold til π_{44} for ustrakt silicium. Yderligere, ses en formindskelse på 25% af π_{66} for strakt silicium sammenlignet med π_{44} for silicium. Temperatur afhængigheden af piezokoefficienterne er ændret for de strakte materialer i forhold til ustrakt silicium. I strakt silicium observeres en temperatur afhængighed af piezokoefficienten på $\frac{1}{\pi_{66}} \frac{\partial \pi_{66}}{\partial T} = 0.1\%/°\text{C}$, som er en forbedring i forhold til den målte temperatur afhængighed af piezokoefficienten i ustrakt silicium på $\frac{1}{\pi_{44}} \frac{\partial \pi_{44}}{\partial T} = 0.35\%/°\text{C}$.

Silicium komponenter i nanostørrelse karakteriseres eksperimentelt og det observeres at en

formindskelse af komponentens størrelse har en stor indflydelse på de piezoresistive egenskaber. De eksperimentelle målinger for p-type silicium viser en forøgelse af piezokoefficienten på omkring 630% i komponenter i nanostørrelse i forhold til piezokoefficienten i silicium komponenter med mikrometer størrelse.

Denne afhandling bidrager med ny viden til forskning af piezoresistive MEMS og NEMS sensorer og giver en solid forståelse for piezoresistivitet generelt. De resultater der er præsenteret i denne afhandling beviser at det er muligt at opnå piezoresistive sensorer med høj følsomhed ved enten at manipulere krystal strukturen eller ved at formindske størrelsen på komponenterne. Resultaterne fra denne afhandling kan direkte bruges som fundament til en ny generation af piezoresistive MEMS of NEMS sensorer med høj følsomhed.

Preface

This thesis is submitted in partial fulfillment of the requirement for obtaining the Doctor of Philosophy (Ph.D.) degree in engineering at the *Technical University of Denmark* (DTU). The project has been carried out at the *Department of Micro and Nanotechnology* (MIC) under the supervision of Prof. Erik V. Thomsen and Associate Prof. Ole Hansen. The Danish company Grundfos A/S has financially contributed to the project and Ph.D. Carsten Christensen has been the supervisor and contact person to Grundfos A/S throughout the project.

The thesis ”Piezoresistivity in microsystems" covers a study of three years from January 2005 to January 2008.

There is a lot of people who has contributed to this thesis and I appreciate their help and guidance throughout the entire project. Firstly, I would like to thank my main supervisor Prof. Erik V. Thomsen. Since I attended my first course at MIC in 2000 (*Solid state physics and microtechnology*) where Erik V. Thomsen was the teacher, he has been a great inspiration to me, both academically but certainly also in his way of appreciating life and always turning what seemed to be a negative message into a positive challenge. I would like to thank Associate Professor Ole Hansen for never giving up on an analytical challenge before its solved. He keeps on surprising me with his excellent problem solving methods and has always had time for discussions and advice.

I have had the privilege of co-supervising two MSc. projects, Morten Berg Arnoldus and Kasper Reck. These two projects has in particular contributed to my project. Additionally, I would like to thank the students whose bachelor projects I have supervised, Esben Krauthammer, Mikkel Olesen, Tobias Hedegaard, Martin Filskov Laursen, Kasper Reck, Jesper K. Olsen, Anders Greve and the many students who have attended special courses under my supervision. The group members of the MEMS-Applied Sensors group deserve a special thank for many inspiring discussions during group meetings. There is always a friendly and helpful atmosphere in the group. A special thanks to Thomas Pedersen for proof-reading the thesis. Also thanks to the cleanroom personal at Danchip for always being friendly and helpful when discussing possible fabrication processes.

I would also like to thank Dr. Prof. Oliver Paul from IMTEK, Freiburg. As a part of this project I have had the privilege of being a part of his group during a two months research stay in Freiburg. I was inspired by the work in his group and Dr. Prof. Paul and I have had many fruitful discussions. From IMTEK, I would also like to thank Dr. Patrick Ruther for supervising me on a daily basis and keeping the spirit high during my research stay in Freiburg. Additionally, I would like to thank all the members of the group of Dr. Prof. Paul at IMTEK for making my stay in wonderful Freiburg a memorable one, especially thanks to Dr. Joao Gaspar, Pascal Gieschke, Sebastian Kisban and Joseph Joos.

From Grundfos A/S I would like to thank Carsten Christensen for guidance and helpful discussions during the project.

I would like to give a special thank to Anders Hyldgård who has been a co-student and a good friend throughout my study at DTU. We have had many interesting discussions and Anders Hyldgård has provided a solid and important help throughout this project.

Finally, I would like to thank my wonderful family, in particular my girlfriend Mette, who has supported me 100% and has been a solid foundation in my private life throughout this project.

Kgs. Lyngby, Denmark, January 1st, 2008

Jacob Richter
MIC - Department of Micro and Nanotechnology
Ørsteds Plads, Building 345 East
Technical University of Denmark
DK-2800 Kgs. Lyngby, Denmark

Contents

CHAPTER

1 Introduction

Today, numerous components and devices applied in our daily lives are fabricated with the use of microtechnology. These components are included in the computer at work, the mobile phone, the radio, the calculator, etc. This development of microelectronics has ensured a mature fabrication technology. High expertise manufacturers of computer components such as Intel are now fabricating transistors with 45 nm gate lengths [1].

Pure electronics components are not the only devices that with advantage can be fabricated using microtechnology. A microsystem can have almost any purpose or application and perform many functions such as sensing, actuation, signal processing, control, and display.

The main subject of this thesis is mechanical sensing and in particular piezoresistive sensing. This chapter serves partly as an introduction to mechanical and piezoresistive sensing and partly as a presentation of the main topics dealt with in this thesis. The introduction to mechanical sensing includes three examples of realized piezoresistive sensors. The brief introduction leads to the presentation of the thesis focus. Subsequently, an introduction to piezoresistivity in general and in particular in silicon is given. A historical overview of the experimental research is given and a theoretical model is presented in order to describe the main contributions to the piezoresistive effect. This is followed by a presentation of the materials which piezoresistive properties have been characterized during this project. Finally, the characterization setup is introduced.

1.1 MEMS

Micro electro mechanical systems (MEMS) include both moving and non-moving devices of which mechanical, thermal, fluidic, magnetic, optical, and chemical properties are just a few of many properties, the systems explore. In 1962 Tufte and Chapman [2] demonstrated a pressure sensor using diffused silicon piezoresistors on a membrane. The pressure sensor was one of the first MEMS devices to be commercialized and has also been one of the most successful devices measured by production number. Other MEMS success stories include electrostatic projection displays [3], gyroscopes [4] and accelerometers [5].

A large part of conventional MEMS devices detect and sense physical parameters in the surroundings where the above mentioned pressure sensor and accelerometer are some well known examples. Biochemical sensors used to detect specific molecules have also been commercialized [6] and the size of the MEMS devices now enables in-the-body analysis [7, 8]. The need to sense gradually smaller and smaller objects or variations in physical parameters challenges the industry and academia to develop highly sensitive sensors. The sensing principle differs between devices,

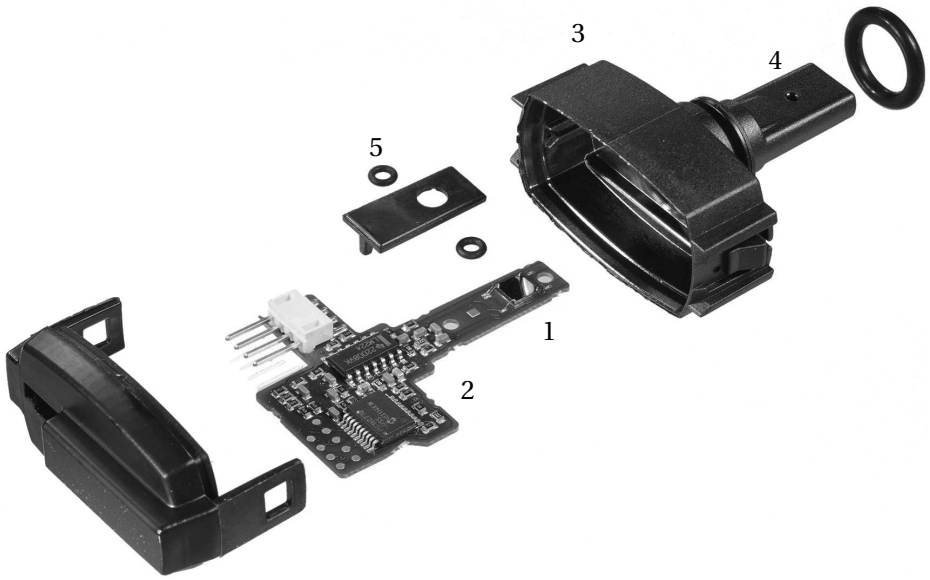


Figure 1.1: Pressure sensor concept developed by Grundfos A/S [15]. The packaged system consists of a silicon chip (1), interface electronics (2), and housing (3). The silicon chip is exposed directly to the media by a through hole (4) in the housing and o-rings (5) are used for sealing.

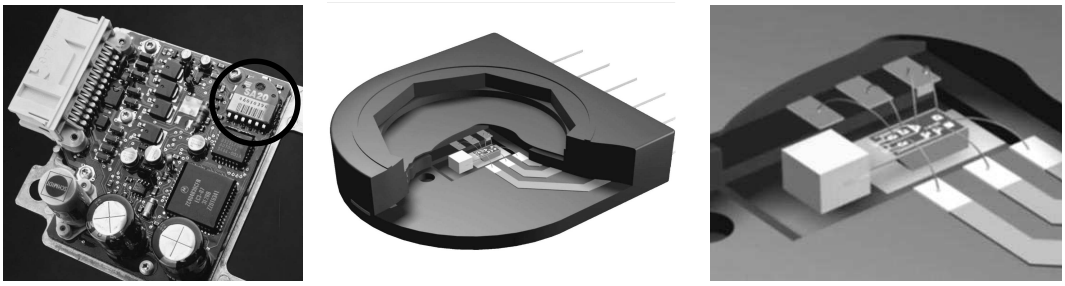
depending on what to detect and the needed accuracy. Among sensing principles that rely on mechanical properties are piezoresistive [9, 10, 11], capacitive [12], piezoelectric [13], and resonance frequency sensing [14]. A large number of commercialized MEMS utilize the piezoresistive properties of silicon. Three examples of realized devices are given below.

1.1.1 Pressure sensor

A pressure sensor can be realized using a silicon chip with a thin membrane. A pressure difference between frontside and backside of the membrane causes the membrane to bend. By placing small piezoresistive resistors on the membrane the deformation is detected electrically. An example of a commercial available pressure sensor is shown in Fig. 1.1. The pressure sensor which is fabricated by Grundfos A/S [15] is an integrated part of a pump control concept that is used to pump water in pipes of a heating system. The device measures the pressure difference over the pump and this allows for a better regulation of the pump speed which saves energy.

1.1.2 Accelerometer

Piezoresistive silicon accelerometers are used as airbag sensors. The chip consists of a silicon beam with a proof mass at the end of the beam. If a car decelerates the proof mass bends the beam and this bend is detected with the small piezoresistive resistors which are placed on the beam. An example of a commercial airbag sensor is shown in Fig. 1.2. The accelerometer is fabricated by SensoNor and is mounted in over 35 million cars. The sensor is protected by a polymer housing which is filled with a silicone oil to provide damping of the accelerometer.



(a) (b) (c)

Figure 1.2: An airbag sensor. (a) The SA 20 accelerometer mounted on a printed circuit board. (b) and (c) Zoom in on the sensor and package. The accelerometer is protected by an epoxy packaging. The sensor consists of a silicon chip and includes a silicon beam with a proof mass. Pictures from [16, 17].

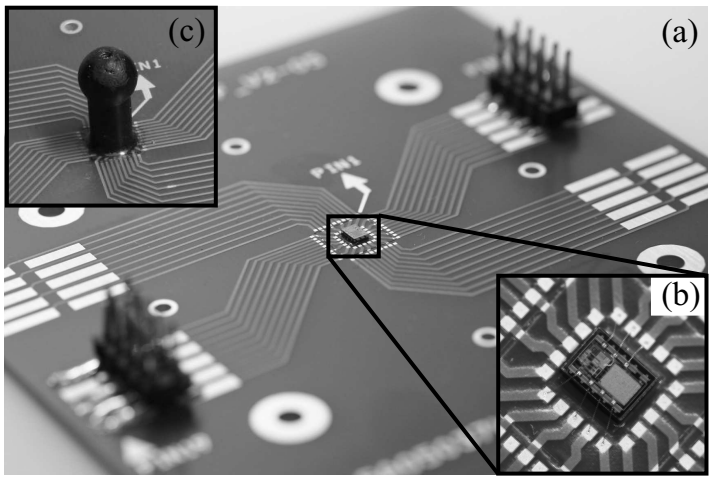
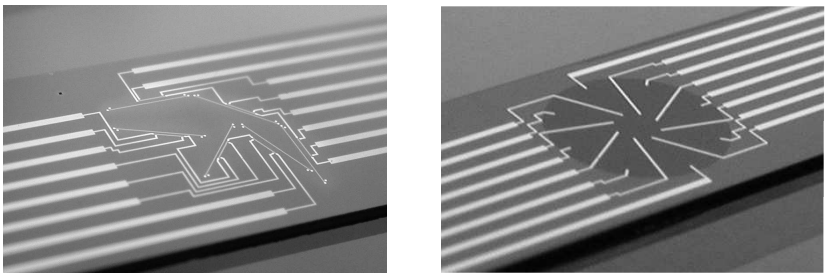


Figure 1.3: Solid state joystick. The stress sensor chip developed at IMTEK, University of Freiburg is glued on to a printed circuit board and wirebonded (a) and (b). The joystick is fabricated in epoxy by vacuum casting (c).

1.1.3 Solid state joystick

A four-degree-of-freedom solid state joystick can be realized by using a piezoresistive stress sensor developed at IMTEK, University of Freiburg. The joystick was designed and fabricated as a part of this project during a research stay in the group of Dr. Prof. Paul at IMTEK and is described in more detail in [18]. The stress sensor system was first demonstrated with a smart bracket system [19]. The joystick consists of an integrated CMOS stress sensor chip molded into a rigid polymer cylinder with a spherical dome, see Fig. 1.3. The device may be used in microrobotics and for biomechanical measurements [20] and it can be used as an input device for various electronic devices since it can steer an object on a screen with 4 degrees of freedom, i.e., 2D position, orientation, and magnification.

In the first examples, the pressure sensor and the accelerometer, simple unidirectional resistors



(a) (b)

Figure 1.4: Photographs of characterization chips with a close up on piezoresistor area. (a) The chip with six unidirectional piezoresistors in different directions is used to determine accurate values of the piezocoefficients. This design has been used in order to obtain the main results of this thesis. (b) The chip with one circular piezoresistor can be used to compare the piezoresistance properties of different materials. This chip is discussed in detail in Chap. 6.

are used in order to measure a unidirectional stress applied to the chip. The stress is applied either by a pressure difference on the front and back side of the silicon membrane or by an acceleration of the proof mass on the silicon beam, respectively. In the last example the current density vector can be changed in the resistor by using a method called current spinning, and a more complex stress distribution is measured. In this thesis the main results are obtained by using unidirectional resistors. However, the current spinning method is used to develop a device that enables comparison of the piezoresistance properties of different materials and that potentially allows for complex realtime stress measurements.

1.2 Thesis focus

This thesis is a contribution to the research in piezoresistive MEMS sensors. In this thesis a thorough description of piezoresistive MEMS devices is given and the theoretical background needed in order to develop and design these devices is presented. During the project chips for piezoresistance characterization, see Fig. 1.4, have been fabricated and several materials have been characterized:

- Silicon. The piezoresistance properties of both p- and n-type silicon are determined experimentally. Today, silicon is the most commonly used material in commercial MEMS devices.

- Strained crystals. Biaxially pre-strained tensile silicon and compressive strained $Si_{0.9}Ge_{0.1}$ piezoresistors are characterized experimentally in the search for materials that have a larger piezoresistance effect than silicon.

- Silicon nanowires. The piezoresistance in silicon nanowires is characterized experimentally as dimensions of the resistors are decreased. This characterization is performed as a part of the search for materials or structures where the piezoresistance effect is larger than the piezoresistance effect in bulk silicon.

A characterization setup is designed and fabricated as a part of this project in order to determine the piezoresistance properties of the above materials.

A theoretical model describing the piezoresistive properties of p-type silicon is developed. The model is intended to present a simple analytical expression that can be used by experimentalists in order to obtain a reliable temperature and doping concentration dependency of the piezoresistive properties. The model serves as the main building block in the future theoretical studies of strained crystals and nanowires.

1.3 Piezoresistivity in semiconductors

In the three examples of the piezoresistive MEMS devices the electrical output changes when the sensor material is deformed. The deformation of the material is defined as the strain. Now, consider a piezoresistor which is strained along the length of the resistor ϵ_L. The relative change in resistance $\frac{\Delta R}{R}$ is then written as

$$\frac{\Delta R}{R} = (1+2\nu)\epsilon_L + \frac{\Delta\rho}{\rho}, \tag{1.1}$$

where ν is Poisson's ratio and the first term is due to a change in geometry of the resistor and the second term is due to a change in the resistivity ρ of the material. In semiconductors, the contribution from the change in resistivity is most often much larger than the contribution from the change in geometry, thus the geometry contribution will be neglected in the following. The strain in the material is due to an applied stress and these are related via Hooke's law. The change in resistance caused by the strain or stress in the resistor is called the piezoresistance effect and in semiconductors this effect is thus described by a change in the resistivity tensor. Both the resistivity tensor and the stress tensor are tensors of second order. The piezoresistive properties are described by a fourth order piezoresistivity tensor $\boldsymbol{\pi}$ which relates the resistivity tensor to the stress tensor

$$\frac{\boldsymbol{\Delta\rho}}{\rho_0} = \boldsymbol{\pi}\boldsymbol{\sigma_\epsilon}, \tag{1.2}$$

where the change in resistivity is $\boldsymbol{\Delta\rho}$, the scalar resistivity at zero stress (no deformation) is ρ_0, and $\boldsymbol{\sigma_\epsilon}$ is the stress tensor. Using Einstein notation this can be written as

$$\frac{\Delta\rho_{ij}}{\rho_0} = -\frac{\Delta\sigma_{ij}}{\sigma_0} = \pi_{ijkl}\sigma_{\epsilon,kl}. \tag{1.3}$$

where $\frac{\Delta\sigma_{ij}}{\sigma_0}$, which is the relative change of the conductivity tensor $\boldsymbol{\sigma}$, is included and the indices (i,j,k,l) each varies from 1 to 3. The fourth order piezotensor includes $3^4 = 81$ independent coefficients. The above equation can be simplified significantly due to the symmetry of the resistivity and stress tensor. In order to apply this symmetry six-vector notation is often used. In this notation Eq. (1.3) is written as

$$\frac{\Delta\rho_\kappa}{\rho_0} = -\frac{\Delta\sigma_\kappa}{\sigma_0} = \pi_{\kappa\lambda}\sigma_{\epsilon,\lambda}, \tag{1.4}$$

where the indices (κ,λ) now each varies from 1 to 6, and the piezoresistivity tensor is reduced to include only 36 independent piezocoefficients. The piezocoefficients depend on sample material, temperature, doping concentration, and dopant.

1.4 Piezoresistance in silicon

Since the pioneering work of Smith in 1954 [21] piezoresistivity of silicon has attracted attention from both academia and industry. The continued academic interest is partly due to the scarcity of

Type	Material	Resistivity	π_{11}	π_{12}	π_{44}
		Ωcm	10^{-11} Pa^{-1}	10^{-11} Pa^{-1}	10^{-11} Pa^{-1}
n	Si	11.7	-102.2	+53.4	-13.6
p	Si	7.8	+6.6	-1.1	+138.1
n	Ge	1.5	-2.3	-3.3	-138.1
p	Ge	1.1	-3.7	+3.2	+96.7

Table 1.1: Piezocoefficients in bulk n- and p-type silicon and germanium with low doping concentrations at room temperature [21].

reliable measurements and partly due to a discrepancy between theoretical models and available measurements especially for p-type silicon.

The piezoresistive tensor for silicon reduces significantly to include only three independent coefficients due to the symmetry of the silicon crystal. The tensor is often written in six vector notation as

$$\boldsymbol{\pi} = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix}, \tag{1.5}$$

where π_{11}, π_{12}, and π_{44} are the piezocoefficients of silicon. The piezocoefficients have different values depending on the dopant type, i.e. p-type or n-type, see Table 1.1. The most commonly used dopant in p-type silicon is boron and the most commonly used dopant in n-type silicon is phosphorus. These dopants are referred to when n-type and p-type silicon are discussed in this thesis.

Boron doped silicon is the preferred piezoresistive material in commercial MEMS due to the large magnitude of the piezocoefficient π_{44} and the very low values of the two other piezocoefficients π_{11} and π_{12}. When the piezoresistors are directed along certain crystal directions, the <110> directions, and placed in a Wheatstone bridge configuration these piezocoefficients result in a high sensitivity of the MEMS device. In this particular configuration the effective longitudinal and transversal piezocoefficients (which are linear combinations of π_{11}, π_{12}, and π_{44}) are large and almost matched in magnitude but with opposite sign. The noise in a piezoresistor is mostly due to $1/f$ noise which decreases with increasing doping concentration [22]. For increasing doping concentration the piezoresistive effect and the temperature dependency is decreased. Thus, the piezoresistive effect as a function of doping concentration and temperature is a very important information for MEMS system designers.

1.4.1 Experimental approach

The experimental approach to determine the piezocoefficients is to fabricate a sample with piezoresistors and measure the change in resistance as a function of applied stress, according to Eq. (1.1) and Eq. (1.3). Today, the experimental values of the piezocoefficients measured by Smith in 1954 for lightly doped silicon and germanium, see Table 1.1, are still used as reference values. The piezoresistance coefficients of more heavily doped silicon were later experimentally estimated by other research groups [25, 26, 27]. However, the experimental results vary significantly as seen in

Ref.	Dop. conc.	π_{44}	dev.
	10^{18} cm^{-3}	10^{-11} Pa^{-1}	%
[21]	0.002	138.1	
[23]	0.02	93.1	7.5
[24]	0.03	113.5	6
[25]	0.8	105	8-12
[26]	1.5	87	6.5
[27]	3	111	
[25]	8.2	95	8-12
[27]	9	98	
[27]	50	78	
[27]	300	60	
[27]	500	48	
[27]	2000	35	

Table 1.2: Experimentally obtained values of the piezocoefficient π_{44} at T = 300 K in p-type silicon and standard deviations of the measurements. The obtained values are plotted in Fig. 1.5.

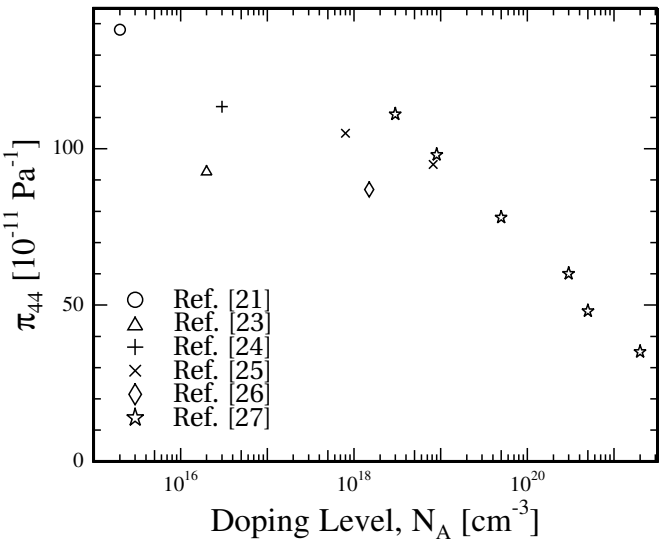


Figure 1.5: Graphical presentation of the experimental results of the piezocoefficient π_{44} in p-type silicon at room temperature as a function of doping concentration as listed in Table 1.2. The figure shows that there is a large difference in the obtained values.

Table 1.2 which lists the piezocoefficient π_{44} determined by different research groups. Fig. 1.5 plots the results.

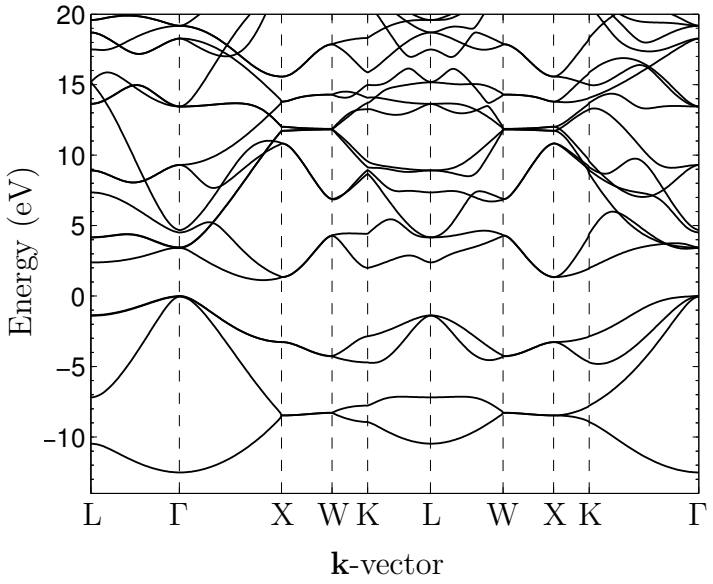


Figure 1.6: (a) Band structure of silicon calculated with a tight binding method in the **k**-domain. The symmetry points in silicon in **k**-space are listed on the **k**-vector axis. The point of interest is especially the Γ point where the valence band has its maximum value.

1.4.2 Theoretical approach

A theoretical model has been developed during this project in order to describe how π_{44} depends on temperature and doping concentration in p-type silicon. The model is described in detail in App. B.1 and this section gives a short summary of the methods and conclusions presented.

The theoretical approach to determine the piezocoefficients is to consider how the components in the conductivity tensor change according to strain. The conductivity tensor may be calculated using the Boltzmann transport equation in the relaxation time approximation [28]

$$\sigma_{ij} = -\frac{e^2}{4\pi^3\hbar^2}\sum_{n=1}^{3}\int \tau_{\mathbf{m}}(\mathbf{k},T)\frac{\partial\xi_n(\mathbf{k})}{\partial k_i}\frac{\partial\xi_n(\mathbf{k})}{\partial k_j}\frac{\partial f_0}{\partial\xi}\mathrm{d}\mathbf{k}, \tag{1.6}$$

given the dispersion relation $\xi_n(\mathbf{k})$, where ξ_n is the hole energy as a function of the wavevector $\mathbf{k}$. The subscript n refers to the valence band index, and the sum extends over the three valence bands, i.e. the heavy hole band, the light hole band, and the split-off band. The equilibrium distribution function for the holes is denoted f_0 and $\tau_{\mathbf{m}}$ is the momentum relaxation time. The approximations applied to the band structure $\xi_n(\mathbf{k})$ and the relaxation time $\tau_{\mathbf{m}}$ are outlined below.

1.4.2.1 Silicon band structure

The band structure of silicon in k-space is shown in Fig. 1.6. This band structure can be calculated by different methods. The band structure calculations have been performed by two different methods, the tight-binding method and the $\mathbf{k}\cdot\mathbf{p}$ method. The results from the $\mathbf{k}\cdot\mathbf{p}$ method showed to be in good agreement with experimental data, thus this model is used to calculate the band structure below. The Hamiltonian $\mathbf{H}$ is composed of three terms

$$\mathbf{H}\left(\mathbf{k},\epsilon_{ij}\right) = \mathbf{H}_{\mathbf{k}\cdot\mathbf{p}}\left(\mathbf{k}\right) + \mathbf{H}_{\mathrm{so}} + \mathbf{H}_{\epsilon}\left(\mathbf{k},\epsilon_{ij}\right). \tag{1.7}$$

The first term is a doubly degenerate three band Hamiltonian matrix, $\mathbf{H}_{\mathbf{k}\cdot\mathbf{p}}(\mathbf{k})$, calculated using the $\mathbf{k}\cdot\mathbf{p}$ method. The three band structure parameters adjust the Hamiltonian to fit experimental band structure data [29]. The second term is a constant spin-orbit perturbation Hamiltonian matrix, $\mathbf{H}_{\text{so}}$, with a single parameter which is the spin-orbit splitting energy Δ_{so}. The final term is a strain perturbation Hamiltonian matrix, $\mathbf{H}_{\epsilon}(\mathbf{k},\boldsymbol{\epsilon})$, which is a function of both wavevector and strain tensor $\boldsymbol{\epsilon}$. The strain perturbation Hamiltonian from Ref. [30] is tuned to match experimental data. The total Hamiltonian is diagonalized at each k-point at a prescribed strain and six pair-wise identical eigenvalues are determined. These eigenvalues form the three valence bands $\xi_n(\mathbf{k})$.

1.4.2.2 Relaxation time

The momentum relaxation time $\tau_{\mathbf{m}}$ depends on the dominant scattering mechanisms which near room temperature are non-polar optical phonon scattering, acoustical phonon scattering, and ionized impurity scattering. The microscopic scattering rates add, thus the momentum relaxation time is written as

$$\frac{1}{\tau_{\mathbf{m}}(\mathbf{k},T)} = \frac{1}{\tau_{\text{ap}}(\mathbf{k},T)} + \frac{1}{\tau_{\text{op}}(\mathbf{k},T)} + \frac{1}{\tau_{\text{I}}(\mathbf{k},T)}, \tag{1.8}$$

where $1/\tau_{\text{ap}}$, $1/\tau_{\text{op}}$, and $1/\tau_{\text{I}}$ are the scattering rates due to acoustic phonons, non-polar optical phonons, and ionized impurities, respectively.

This method of including all important scattering mechanisms is completely new, since the relaxation time is most commonly modelled via a simple power law,

$$\tau_{\mathbf{m}} = \tau_0 \left(\frac{\xi_n(\mathbf{k}) - \xi_n^{(0)}}{k_B T_0} \right)^s, \tag{1.9}$$

where $\xi_n^{(0)}$ is the band minimum, $T_0 = 300$ K, and the parameter $s \in \{-1/2, 0, 3/2\}$. The $s = -1/2$ model corresponds to scattering dominated by acoustic phonons and is employed by Kanda [31] which is the commonly used model, the $s = 0$ model assumes a constant relaxation time, and $s = 3/2$ corresponds to scattering dominated by ionized impurities. The simple power law model is insufficient for several reasons. Firstly, it is a very poor model for non-polar optical phonon scattering, which is important in silicon near room temperature. Secondly, the different scattering mechanisms emphasize transport in regions of the band structure rendered insignificant by other scattering mechanisms, and thus the final real transport properties can not be deduced from individual conductivities evaluated using this model.

1.4.2.3 The piezocoefficient π_{44}

The calculated band structures and relaxation times are applied to Eq. (1.6) for a shear strain ϵ_{xy} in order to directly extract the piezocoefficient π_{44}. This is done by applying Eq. (1.1), Eq. (1.3), and Eq. (1.5) in six vector notation and isolate π_{44}

$$\pi_{44} = -\frac{1}{\sigma_{\epsilon,6}} \frac{\Delta\sigma_6}{\sigma_0} = -\frac{S_{44}}{\epsilon_6} \frac{\Delta\sigma_6}{\sigma_0}, \tag{1.10}$$

where the compliance tensor is written in six-vector notation, $S_{\eta\mu}$, and has the same structure as the piezoresistivity tensor $\pi_{\eta\mu}$ and describes the linear relation between stress and strain, i.e. $\epsilon_\eta = S_{\eta\mu}\sigma_{\epsilon,\mu}$. From Eq. (1.10) the piezocoefficient π_{44} may be calculated from the calculated shear conductance values σ_6 at given values of the shear strain ϵ_6. The results are shown in Fig. 1.7 where experimental data is included in order to compare the results.

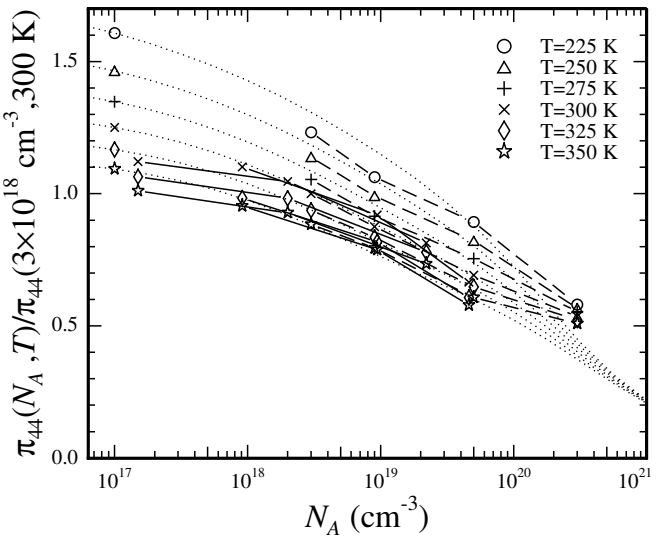


Figure 1.7: Experimental and calculated values of the normalized piezocoefficient π_{44} as a function of doping level with temperature as parameter. The piezocoefficients are normalized to π_{44} at $T = 300$ K and $N_A = 3.0 \cdot 10^{18}$ cm^{-3}. The dashed lines are experimental data from Tufte and Stelzer [27] and the solid lines are experimental data obtained during this project (uniformly doped piezoresistors with doping concentrations $N_A = 1.5 \cdot 10^{17}$ cm^{-3}, $2.0 \cdot 10^{18}$ cm^{-3}, $2.2 \cdot 10^{19}$ cm^{-3}, and piezoresistors with a Gaussian doping profile with peak doping concentrations of $N_A = 9.1 \cdot 10^{17}$ cm^{-3}, $9.4 \cdot 10^{18}$ cm^{-3}, $4.6 \cdot 10^{19}$ cm^{-3}). Notice, the full lines connects the actual experimental points and are thus just guides to the eye. The dotted lines represent the model calculations. The temperature and doping concentration dependency for doping concentrations between 10^{18} cm^{-3} and 10^{20} cm^{-3}, which is the technological relevant doping range, is in good agreement with experimental results.

1.4.2.4 Piezoresistive fitting function

In order to provide experimentalists with a simple function that can be used to predict how π_{44} depends on doping concentration and temperature a fit to the theoretical model is performed. The fitting function is

$$P(N_A, \Theta) = \Theta^{-\vartheta}\left[1 + \left(\frac{N_A}{N_b}\right)^{\alpha}\Theta^{-\beta} + \left(\frac{N_A}{N_c}\right)^{\gamma}\Theta^{-\eta}\right]^{-1}, \tag{1.11}$$

where $P(N_A, \Theta)$ is the normalized piezocoefficient to the lowest acceptor density value at $T_0 = 300$ K, $\Theta = T/T_0$, and N_b and N_c are fitting parameters and ϑ, α, β, γ, and η are correction powers listed in Table 1.3. The fit is shown in Fig. 1.8. For more information about the above model the reader is referred to App. B.1.

1.5 Biaxial strained Si and SiGe

The piezoresistive effect of a material depends on the crystal structure. In this thesis it is investigated how the piezoresistive effect depends on a pre-strain of the crystal. A pre-strained material can be obtained by forcing a crystal compression/(expansion) in one plane of the crystal and

Parameter	Value
N_b	6×10^{19} cm^{-3}
N_c	7×10^{20} cm^{-3}
ϑ	0.9
α	0.43
β	0.1
γ	1.6
η	3

Table 1.3: Fitting parameters to the expression in Eq. (1.11).

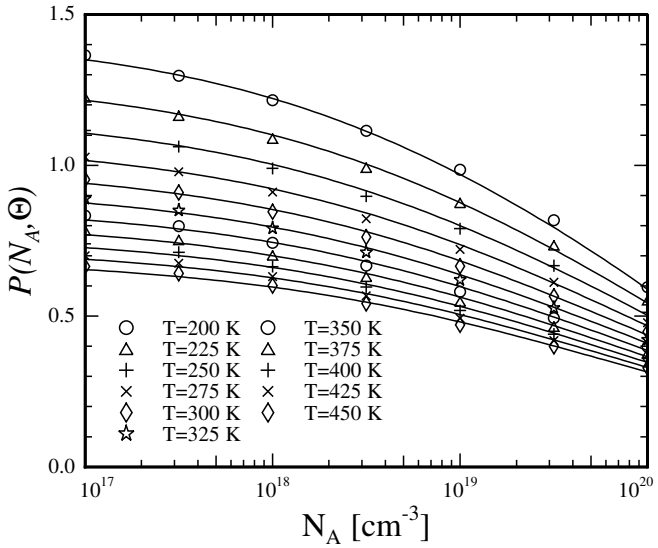


Figure 1.8: Fitted correction factor $P(N_A,\Theta)$ for π_{44} as a function of carrier density and temperature. The fit (solid) is described by Eq. (1.11) and the fitting parameters are listed in Table 1.3.

to compensate for this a lattice expansion/(compression) occurs in the direction normal to that plane.

The crystal symmetry originally present in silicon and germanium is reduced in biaxial tensile and compressive pre-strained materials, and the piezotensor is now (in six-vector notation)

$$\boldsymbol{\pi} = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{13} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{13} & 0 & 0 & 0 \\ \pi_{13} & \pi_{13} & \pi_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{66} \end{bmatrix}. \tag{1.12}$$

The work in this thesis employs existing technology to obtain these pre-strained crystals by molecular beam epitaxy (MBE). By growing $Si_{1-x}Ge_x$, where x is the percentage composition of germa-

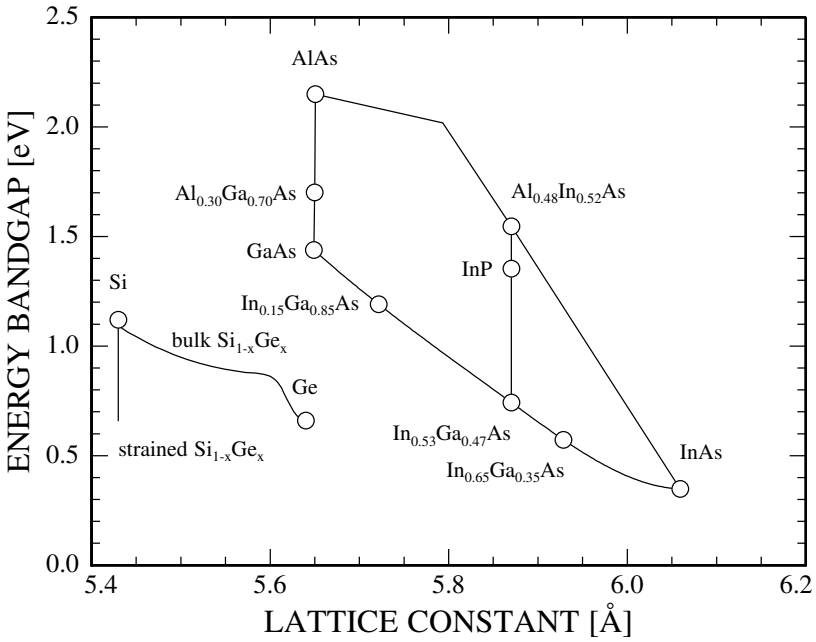


Figure 1.9: A mapping of the energy bandgap and lattice constant of different semiconductors and possible compounds. The line between two points, illustrates the path from one material to the other. The figure is reproduced from [32].

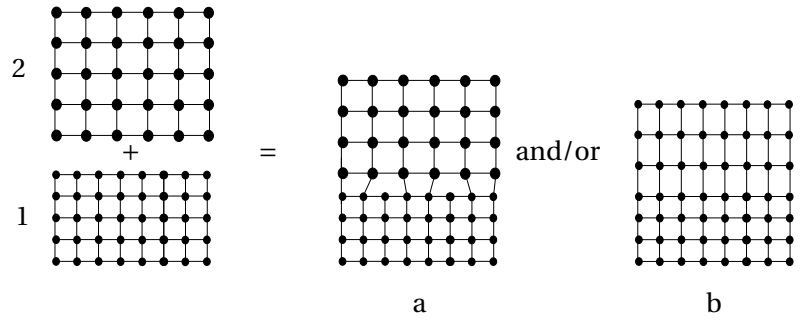


Figure 1.10: Schematic diagram in 2D of possible locally outcome of MBE growth. The deposited material will either (a) generate dislocations and defects near the interface and obtain its bulk crystal structure, and/or the material will (b) adjust its crystal arrangement in order to fit into the crystal lattice of the substrate.

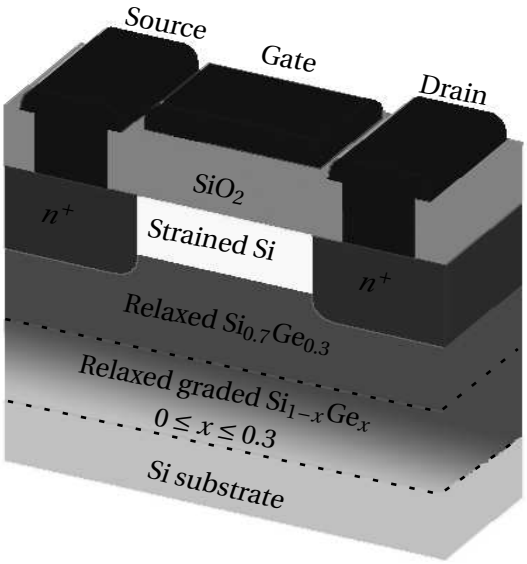


Figure 1.11: Schematic illustration of a strained silicon n-channel MOSFET. The electrons in the strained silicon layer has a higher mobility than the electrons in a relaxed silicon crystal thus the device can operate at higher frequencies.

nium, on top of a silicon substrate a compressive strained material is obtained, since bulk $Si_{1-x}Ge_x$ has a larger lattice constant than silicon, see Fig. 1.9. On the other hand, tensile strained silicon is obtained by growing silicon directly on top of a $Si_{1-x}Ge_x$ substrate. The $Si_{1-x}Ge_x$ substrate is obtained by gradually increasing the germanium concentration while growing the material on top of a silicon substrate. Using this technique, the grown $Si_{1-x}Ge_x$ layer is relaxed.

If the lattice mismatch of two materials is too large, misfit dislocations appear near the interface and the grown material will obtain its bulk crystal structure. This is illustrated in Fig. 1.10 where material 1 has a smaller lattice constant than material 2. The strained structure becomes thermally unstable at a certain thickness called the critical thickness which depends on the composition of the grown layer. The larger the lattice mismatch is the smaller the critical thickness. Thus, the critical thickness limits the design of devices with epitaxially grown structures.

The strain in the crystal changes the electrical and optical properties [33, 34]. The mobility is enhanced and this is exploited to fabricate high speed micro electronic devices. One example is a metal oxide semiconductor field effect transistor (MOSFET) as illustrated in Fig. 1.11. By applying a voltage to the gate electrode, a channel from the source to the drain is generated. The electron mobility in strained silicon is higher, than that of bulk silicon, thus a faster electron drift is obtained [35], which in turn increases the maximum operating frequency of the device.

1.6 Silicon nanowires

The piezoresistance of top-down fabricated silicon nanowires is investigated in this thesis. Previously published results show a large increase in the piezoresistance effect when lowering the dimensions of the resistors. He and Yang [36] showed measurements with an increase of up to 20

times that of the values obtained by Smith [21] in bulk silicon. The results in Ref. [36] are obtained on bottom up fabricated silicon nanowires and are in good agreement with the theoretical studies in Ref. [37]. The experimental results obtained on top down fabricated nanowires so far by Toriyama [38] shows an increase in the piezoresistance effect of 55%, which is far from the giant increase reported in Ref. [36]. In this thesis experimental results are obtained in order to confirm the increase in the piezoresistance effect in top down fabricated silicon nanowires compared to microscale silicon piezoresistors.

The nanowires are obtained by a top down fabrication technique. Bottom up fabrication of nanowires has so far shown difficulties in wafer scale fabrication and for commercial devices this technology has not yet been fully developed. In contrast, the top down fabrication methods are well established for industrial development. The top down approach in this thesis uses electron beam lithography to define the nanowires on a bulk silicon layer as in Refs. [39, 40]. However, this technique is a very expensive and time consuming process and is not fit for commercial applications. This is an issue that can be overcome by using nanoimprint lithography (NIL) [41, 42] which is a parallel process.

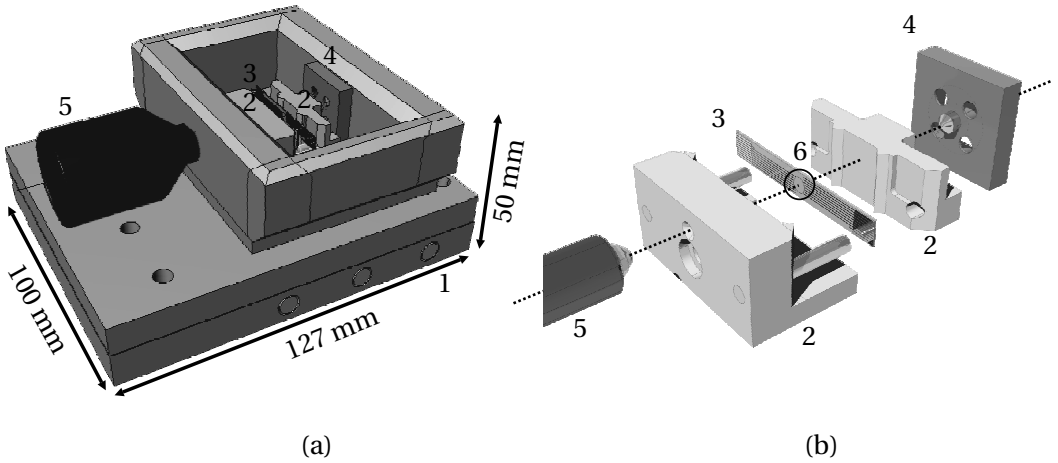
Today, nanowires is a very hot topic in research. As quantum mechanical effects become important the material properties, such as electrical, magnetic, and thermoelectrical properties change drastically. So far, the nanowires have shown their use in many different applications, e.g. chemical [43, 44] and biomedical sensors [45, 46]. The aim of this nanowire study is to investigate if the use of top down fabricated silicon nanowires in mechanical sensors potentially can lead to highly sensitive sensors.

1.7 Experimental setup

The experimental approach is to fabricate samples consisting of piezoresistors of bulk silicon, strained silicon, strained $Si_{1-x}Ge_x$, and silicon nanowires. These piezoresistors are embedded in a silicon substrate that is inserted into a test fixture. The fixture applies a well defined stress to the piezoresistors while the change in resistance is measured. According to Eq. (1.1) and Eq. (1.3) the piezoresistance in the material can then be determined.

In the original experiments by Smith [21] silicon rods were pulled to apply a uniform uniaxial stress. In Ref. [27] a pull force was applied by pins inserted in the through holes of machined pull samples. For microfabricated thin film devices it is more convenient to use a four point bending fixture (4PB) [11, 23, 47]. This type of setup is used in many applications where a uniform and uniaxial stress must be applied to a sample. In Refs. [47, 48] an optical method is used to measure the deflection and curvature of the chip. The stress is applied to the chip using a piezoelectric actuator and a translation stage, respectively. Refs. [23, 49] use simple loads to apply the force and has no external measurement of the applied force. This is a cumbersome and time consuming method, especially for characterization at different temperatures.

The setup developed in this thesis consists of a 4PB fixture where a motorized stepper actuator performs a bending of the chip while the force on the chip is measured with a dedicated force sensor, see Fig. 1.12. With this method the measured force is used directly to calculate the stress. By using this method Young's modulus is not included in the stress calculation which is the case when a deflection is measured. A detailed description of the setup is included in App. B.2.



(a) (b)

Figure 1.12: Schematic of the complete piezoresistance characterization setup. (a) The setup comprises cartridge heaters (1) that are embedded in the bottom plate of the Al housing surrounding the 4PB fixture (2), the chip (3), and the force sensor (4). The actuator motor (5) is placed outside the Al housing to prevent heating of the motor. (b) Exploded view of the setup illustrating the uniaxial force interaction between actuator, 4PB fixture, chip and force sensor. This ensures uniformity of the stress in the center region of the chip, where the piezoresistors are located (6).

1.8 Thesis overview

This thesis summarizes the three year study of piezoresistive properties in microsystems. The work has been focused on obtaining the most accurate measurement of the piezocoefficients of different materials suitable for microsystems. The most accurate measurement is obtained on unidirectional resistors. An example of a chip containing these resistors was shown in Fig. 1.4a. The theory described in Chap. 2 is derived with the focus on unidirectional resistors and these resistors are included in the chip design in Chap. 3. The fabrication processes of the chips are described in Chap. 4 and the characterization results obtained on the unidirectional resistors are presented in Chap. 5. Parallel to the design, fabrication, and characterization of the unidirectional resistors another piezoresistive characterization resistor has been developed. The resistor is circular and consists of several contacts that enable both current injection and voltage measurements. The circular resistor was shown in Fig. 1.4b. The description of the circular resistor and the results obtained using this resistor are individually treated in Chap. 6.

The accepted and submitted journal papers written as a part of this thesis are intended to be included actively during the reading of the thesis. The main results appear in the thesis, however some subjects are only covered in the journal papers and the reader is suggested to consult these papers when further description is needed. This, in particular, concerns two subjects:

- The theoretical model of how the piezocoefficient π_{44} depends on temperature and doping concentration has been introduced in this chapter and will not be discussed further in this thesis. For further details see App. B.1.

- The four point bending setup used in this thesis to characterize the piezoresistive samples has been introduced in this chapter. The setup is described in detail in App. B.2.

The conference proceedings and the journal papers published during this thesis are all listed in App. A.

1.8.1 Outline of chapters

The thesis is structured as follows:

- Chap. 2 introduces the concepts of stress and strain. The focus is on the stress distribution in a chip inserted in a four point bending fixture. Furthermore, the chapter includes the theoretical knowledge and tools needed in order to extract the piezocoefficients by electrical resistance measurements.
- Chap. 3 presents the design of the chip. The piezoresistors located on the chip are designed in the light of the knowledge gained from Chap. 2 with the focus on how to measure the piezocoefficients with the smallest possible uncertainty. The outer dimensions are determined in order for the chip to fit into the four point bending setup.
- Chap. 4 describes the fabrication of the chips. The chips are fabricated in the cleanroom facility at Danchip, DTU. The chip fabrication process includes a large number of specific processes, for example reactive ion etch, molecular beam epitaxy, UV lithography, E-beam lithography, and E-beam evaporation of metal.
- Chap. 5 presents the experimental results obtained in this project by the use of unidirectional piezoresistors. This includes piezoresistance measurements of silicon, biaxial strained silicon and $Si_{1-x}Ge_x$, and crystalline and polycrystalline silicon nanowires. The piezocoefficients of the materials are measured as functions of doping concentration and temperature.
- Chap. 6 presents a piezocoefficient characterization device which includes a circular piezoresistor. The design enables a rotation of the current density vector in the piezoresistor and the chip is suitable for comparison of different materials. Furthermore, preliminary experiments, where the device is used as a stress sensor, are shown.
- Chap. 7 concludes the thesis.

CHAPTER

2 Theory

This chapter introduces the theoretical relations between stress, resistivity, and resistance.

First, a short introduction to stress in general is given. This is an important measure since the stress in the piezoresistor needs to be well defined in order to extract the piezocoefficients. This is followed by a more detailed description of the stress distribution in the setup used, i.e. a four point bending fixture.

When the stress distribution in the chip is well described the next section gives a detailed description of how this stress is related to a measurable value, i.e. the electrical resistance in a resistor. The proportionality constant between the stress and the relative resistance change is the piezocoefficient. Due to the anisotropy of silicon the piezocoefficient depends on the crystal orientation and stress direction. These dependencies are derived and outlined in order to design the chip in the most optimal way.

2.1 Introduction to stress

The force per unit area, or intensity of the forces distributed over a given section, is called the stress on that section. Fig. 2.1 shows a differential volume element with side lengths Δx, Δy, and Δz, and corresponding stress directions for each side. Here, it is assumed that the stress acts uniformly on the surface and not only in one point of the section.

The stresses acting perpendicular on a surface section is called normal stresses, and are denoted by σ_{xx}, σ_{yy}, and σ_{zz}. The stresses acting along a surface is called the shear stresses. For example, σ_{zx} is the shear stress acting on the surface normal to the z direction in the x direction. The stress components acting on a volume element are represented in the second order stress tensor which is invariant to rotations and thus symmetric (i.e. $\sigma_{ij} = \sigma_{ji}$). The stress tensor is written as

$$\boldsymbol{\sigma} = \begin{bmatrix} \sigma_{xx} & \sigma_{xy} & \sigma_{xz} \\ \sigma_{xy} & \sigma_{yy} & \sigma_{yz} \\ \sigma_{xz} & \sigma_{yz} & \sigma_{zz} \end{bmatrix}, \tag{2.1}$$

where the six coefficients in the symmetric stress tensor in full detail describe the stress distribution in a given point in a material.

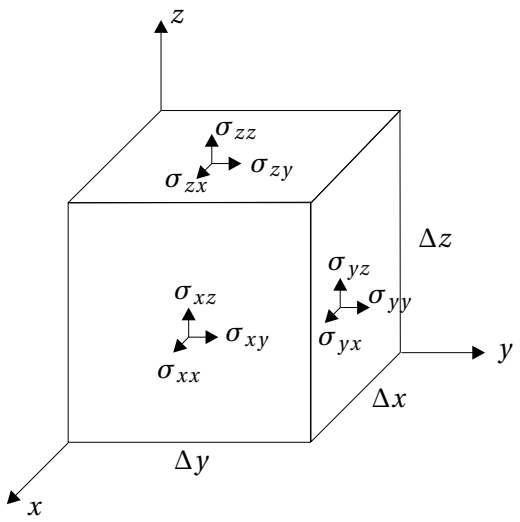


Figure 2.1: Schematic illustration of normal stresses σ_{ii} and shear stresses σ_{ij} acting on a differential volume element with side lengths of Δx, Δy, and Δz.

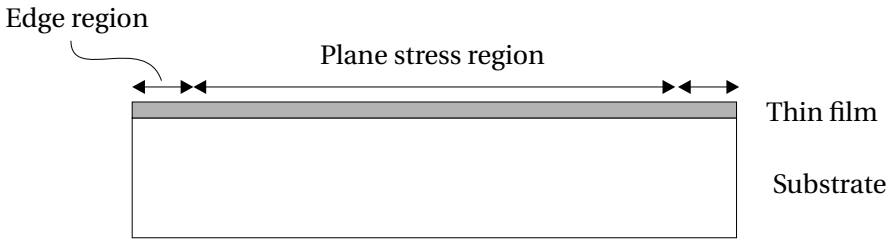


Figure 2.2: A thin film (grey) deposited on a thick rigid substrate (white) is subjected to plane stress a distance of approximately three film thicknesses from the edge.

2.1.1 Plane stress

In many applications the stress distribution is simpler than that illustrated in Fig. 2.1. Plane stress in a material occurs in a thin film deposited on top of a rigid substrate, as the example shown in Fig. 2.2. A distance away from the edge of the film, roughly corresponding to three film thicknesses, the only stress components acting on the film are in the plane of the film [13]. Close to the edge of the film the stress is affected by several boundary effects which result in a more complex situation.

If the xy-plane is the plane of the film, the stress component in the z-direction can be assumed to be zero, since the substrate is much thicker than the film, and the film and substrate surfaces are stress free. Thus, the state of stress in the thin film depends only on the stress components σ_{xx}, σ_{yy}, and σ_{xy}. One can then write the stress tensor as

$$\boldsymbol{\sigma}_{\text{plane stress}} = \begin{bmatrix} \sigma_{11} & \sigma_{12} & 0 \\ \sigma_{12} & \sigma_{22} & 0 \\ 0 & 0 & 0 \end{bmatrix}, \tag{2.2}$$

where the subscripts xyz are exchanged by 123. The xyz notation was used in order to properly introduce the stress tensor in Fig. 2.1. In the following, the stress tensor and other tensors are de-

S_{11}	S_{12}	S_{44}
76.8 GPa	-21.4 GPa	126 GPa

Table 2.1: Compliance coefficients in silicon at room temperature from Ref. [50].

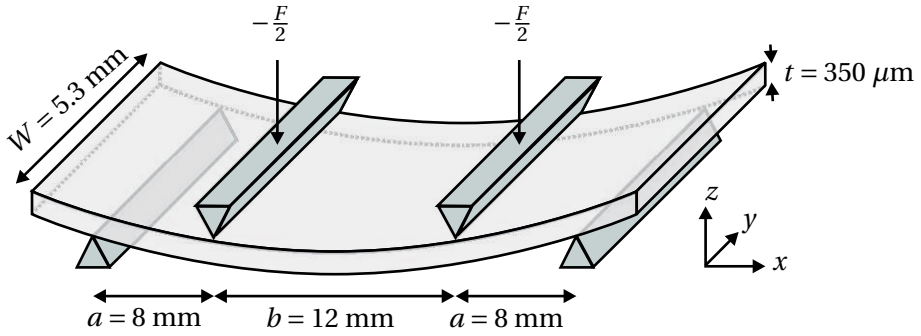


Figure 2.3: Sketch of a four point bending fixture. The piezoresistors are placed in the surface of the rectangular chip and in the center region between the two upper blades since the stress is constant and uniaxial in this area.

scribed with the subscripts 123. The simplified stress tensor in Eq. (2.2) is often valid in microtechnology, because the actual devices are processed in the surface of a much thicker substrate. For example, microfabricated piezoresistors are located in the surface of the chip and have a thickness of approximately 0.5 μm compared to the chip thickness of 350 μm.

2.1.2 Relation between stress and strain

Applying a force to a solid body results in a deformation of the crystal structure. The differential deformation is called the strain. The strain, $\boldsymbol{\varepsilon}$, and stress, $\boldsymbol{\sigma}$, are related through the compliance tensor, $\boldsymbol{S}$, of the material

$$\varepsilon_{ij} = S_{ijkl}\sigma_{kl}. \tag{2.3}$$

The compliance tensor can be reduced significantly in silicon due to symmetry of the silicon crystal to contain only three independent coefficients. Using 6 vector notation the compliance tensor is written as

$$\mathbf{S} = \begin{bmatrix} S_{11} & S_{12} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{11} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{12} & S_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & S_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & S_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & S_{44} \end{bmatrix}, \tag{2.4}$$

where the compliance coefficients are listed in Table 2.1.

2.2 Stress in a four point bending fixture

A uniaxial stress is applied to the sample by the use of a 4PB fixture. The expected stress distribution is described below.

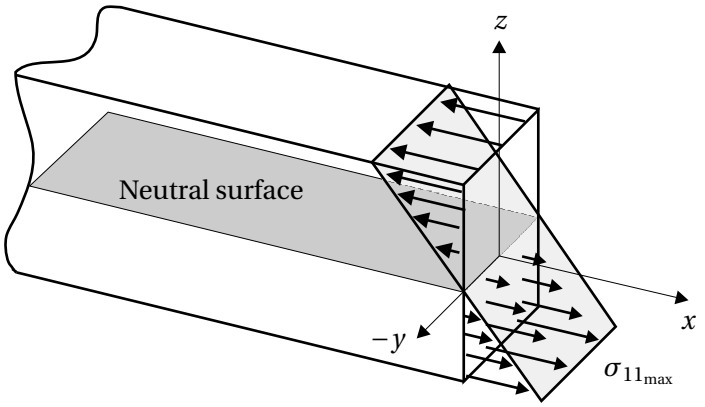


Figure 2.4: Illustration of the stress distribution in a beam subjected to pure bending. The sign of the stress, σ_{11}, changes depending on whether the material is compressed or stretched. In this case the stress is negative at positive z values.

Consider first the test chip in the 4PB set-up, shown in Fig. 2.3, as a beam of width W and thickness t. At the outer knives the beam is simply supported. The two inner knives act on the beam with the forces $-\frac{1}{2}F\hat{\mathbf{z}}$, and due to symmetry and static stability, the outer knives act on the beam with equally large opposite forces $+\frac{1}{2}F\hat{\mathbf{z}}$. In such a configuration the beam is said to be subjected to pure bending. The part of the beam outside the outer knives is free from external forces and moments, thus the shear force in the beam is zero outside the outer knives. Between each pair of outer and inner knives the shear force is constant (magnitude $\frac{1}{2}F$) and it is zero between the inner knives. As a result, the magnitude of the moment increases linearly from zero at the outer knives to $\frac{1}{2}Fa$ at the inner knives, where a is the distance between neighboring inner and outer knives. Between the inner knives the moment is constant with the magnitude $\frac{1}{2}Fa$. This moment makes the beam bend to a circular arc, causing a strain that varies linearly with z, and thus creates uniaxial internal stresses that varies linearly with z as illustrated in Fig. 2.4. These stresses balance the moment. The surfaces normal to the z-axis and the y-axis between the inner blades are free from loads, thus all stresses except σ_{11} vanish. The moment balance yields

$$W\int_{-\frac{t}{2}}^{\frac{t}{2}}\sigma_{11}z\,dz = -W\sigma_{11_{\max}}\int_{-\frac{t}{2}}^{\frac{t}{2}}\frac{2z}{t}z\,dz = -\sigma_{11_{\max}}\frac{Wt^2}{6} = -\frac{1}{2}Fa, \tag{2.5}$$

where $\sigma_{11_{\max}}$ is the magnitude of the maximum value of the stress, and the origin of the z-axis is assumed to be in the middle of the beam on the neutral surface shown in Fig. 2.4. The stress between the inner knives is thus

$$\sigma_{11} = -\frac{2z}{t}\sigma_{11_{\max}} = -\frac{2z}{t}\frac{3Fa}{Wt^2}. \tag{2.6}$$

The piezoresistors are placed in the top surface of the beam, at $z = \frac{t}{2}$, thus the stress acting on the piezoresistors is

$$\sigma_{11} = -\sigma_{11_{\max}} = -\frac{3Fa}{Wt^2}. \tag{2.7}$$

This derivation is simplified significantly, since a correct treatment should be based on plate theory including possible effects of the anisotropic elastic properties of silicon. However, the expression for the stress where the piezoresistors are located is still a very good approximation for the

following reasons. The exact solution for a rectangular plate in pure bending caused by external moments evenly distributed on facing edges of the plate is a uniaxial stress $\sigma_{11} = -2z\sigma_{11_{\max}}/t$ [51], if the stresses causing the external moments are distributed exactly as σ_{11}. The stresses causing the load moments at the inner knives certainly do not fulfil this requirement, but according to the principle of Saint-Venant [51] the exact solution still applies far from the inner knives. The deviations from the exact solution found near the inner knives decays rapidly on a length scale set by the thickness of the piezoresistor test-chip ($t = 350\ \mu$m).

In the exact pure bending solution, the surface becomes an anticlastic surface [51] with the curvature $1/r$ in the $x-z$ plane and the curvature $-\nu/r$ in the $y-z$ plane. The beams are oriented along the [100] and [110] directions, where Poisson's ratio ν in silicon is $\nu = 0.28$ and $\nu = 0.07$, respectively [52]. Thus, in both cases the effect of curvature in the $y-z$ plane is small. However, still this causes the load moment to be unevenly, but symmetrically distributed at the inner knives, which results in deviations from the exact pure bending solution. According to the principle of Saint-Venant the deviations decay rapidly on a length scale equal to half the width of the chip, $W/2$. Taking into account the anisotropic elastic properties of silicon these conclusions are still valid. The exact solution remains essentially the same, as seen if the derivation given in Ref. [51] is redone with the elastic parameters of silicon for a beam oriented along the crystal coordinate system and the [110] direction. For the [110] direction the pertinent rotated tensor elements of the compliance tensor are $S'_{11} = \frac{1}{2}\left(S_{11} + S_{12} + \frac{1}{2}S_{44}\right)$, $S'_{12} = \frac{1}{2}\left(S_{11} + S_{12} - \frac{1}{2}S_{44}\right)$, and $S'_{13} = S_{12}$. The primed symbols are the rotated tensor elements and the unprimed symbols are the tensor elements in the crystal coordinate system listed in Table 2.1. The Poisson's ratio mentioned in the curvature discussion above is related to these tensor elements $\nu = -S_{12}/S_{11}$ and $\nu = -S'_{12}/S'_{11}$ for the [100] and [110] direction, respectively. Thus, analytically the 4PB fixture applies a unidirectional stress given by Eq. (2.6) to the piezoresistors if the chip is thin and if the piezoresistors are placed more than half the width of the chip from the inner knives.

This analytical approach presents how to determine the magnitude of the uniaxial stress which is applied to the chip by the 4PB fixture. The reader is referred to App. B.2 for a thorough description of the 4PB setup used in order to obtain the results in this thesis.

2.3 Piezoresistivity

In this section the relation between the resistance in a resistor and the deformation of the resistor is presented. The resistivity ρ of a material describes the relation between the current density vector $\boldsymbol{J}$ and the electric field vector $\boldsymbol{E}$. This relation is written as

$$E_i = \rho_{ij} J_j, \tag{2.8}$$

where the Einstein summation notation is used above, and in the following, for convenience. In the stress free material each component of the resistivity tensor is constant $\rho_{ii} = \rho^0_{jj}$ and the shear resistivities, $\rho_{ij}, i \neq j$, are all equal to zero. The mean resistivity is found as

$$\bar{\rho} = \rho^0_{ii}. \tag{2.9}$$

The resistivity tensor is symmetric according to the theorem by Onsager [53] which states that a matrix connecting phenomenological coefficients is symmetric when choosing proper "fields" and linearly connected "fluxes". By applying a stress to the material the resistivity will change as a function of the magnitude and the direction of the stress. The relation between the change

in resistivity $\Delta\rho_{ij}$ and the stress is determined by the piezoresistive effect. This relation can be mathematically described by using the series expansion

$$\frac{\Delta\rho_{ij}}{\bar{\rho}} = \pi_{ijkl}\sigma_{kl} + \Lambda_{ijklmn}\sigma_{kl}\sigma_{mn} + ... \tag{2.10}$$

where π_{ijkl} and Λ_{ijklmn} are components in a tensor of fourth and sixth rank, respectively. The tensors consist of 3^N elements, where N denotes the rank. In the low stress linear regime the only contribution to the resistivity is the fourth order tensor $\boldsymbol{\pi}$ which is called the piezotensor. This tensor consists of 81 elements called piezocoefficients.

In this section the above equation is evaluated. Firstly, the symmetry of the silicon crystal is described. The symmetry of the crystal simplifies the piezotensor significantly. Secondly, the relation between the resistance of a resistor and the subjected stress to the resistor is derived. These equations are described for two types of resistances: R, which is the resistance of a resistor found by measurement of the voltage drop parallel to the current density vector, and R_H (called "Hall type"), which is found by measurement of the voltage drop perpendicular to the current density vector.

2.3.1 Symmetry of the silicon crystal

The silicon atoms are organized in a diamond structure and the crystal belongs to the O_h crystal class. This crystal class is highly symmetric, thus the number of independent coefficients in the piezotensor is reduced significantly. The reduction from 81 coefficients to 3 coefficients is thoroughly described in App. C. The simplified piezotensor is visualized as

$$\boldsymbol{\pi} = \left[\begin{array}{ccc}
\begin{pmatrix} \pi_{11} & 0 & 0 \\ 0 & \pi_{12} & 0 \\ 0 & 0 & \pi_{12} \end{pmatrix} & \begin{pmatrix} 0 & \frac{\pi_{44}}{2} & 0 \\ \frac{\pi_{44}}{2} & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} & \begin{pmatrix} 0 & 0 & \frac{\pi_{44}}{2} \\ 0 & 0 & 0 \\ \frac{\pi_{44}}{2} & 0 & 0 \end{pmatrix} \\
\begin{pmatrix} 0 & \frac{\pi_{44}}{2} & 0 \\ \frac{\pi_{44}}{2} & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} & \begin{pmatrix} \pi_{12} & 0 & 0 \\ 0 & \pi_{11} & 0 \\ 0 & 0 & \boxed{\pi_{12}} \end{pmatrix} & \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & \frac{\pi_{44}}{2} \\ 0 & \frac{\pi_{44}}{2} & 0 \end{pmatrix} \\
\begin{pmatrix} 0 & 0 & \frac{\pi_{44}}{2} \\ 0 & 0 & 0 \\ \frac{\pi_{44}}{2} & 0 & 0 \end{pmatrix} & \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & \frac{\pi_{44}}{2} \\ 0 & \frac{\pi_{44}}{2} & 0 \end{pmatrix} & \begin{pmatrix} \pi_{12} & 0 & 0 \\ 0 & \pi_{12} & 0 \\ 0 & 0 & \pi_{11} \end{pmatrix}
\end{array}\right], \tag{2.11}$$

where for example $\pi_{2233} = \pi_{12}$ (outlined box) is the coefficient placed on the 3rd row in the 3rd column in the matrix placed on the 2nd row in the 2nd column.

The piezotensor is often represented in 6 vector notation, where the subscripts are changed ($11 \to 1, 22 \to 2, 33 \to 3, 32 \to 4, 31 \to 5, 12 \to 6$). Thus, including the symmetry of the silicon crystal the piezotensor is normally written as

$$\boldsymbol{\pi} = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix}. \tag{2.12}$$

The crystal symmetry originally present in silicon and germanium is reduced in biaxial tensile and compressive pre-strained materials, such as strained silicon and strained $Si_{1-x}Ge_x$. The crystal

structure now belongs to the tetragonal crystal class D_{4h}. However, due to the remaining symmetry the piezoresistivity tensor of biaxial strained $Si_{1-x}Ge_x$ and strained Si is expected to have 6 linearly independent coefficients π_{11}, π_{12}, π_{13}, π_{33}, π_{44}, and π_{66} while the non-zero elements are found at the same positions in the tensor (in matrix notation) as for silicon [54]. For strained $Si_{1-x}Ge_x$ and strained Si the piezoresistivity tensor thus has the topology

$$\boldsymbol{\pi} = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{13} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{13} & 0 & 0 & 0 \\ \pi_{13} & \pi_{13} & \pi_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{66} \end{bmatrix}. \tag{2.13}$$

The following description is performed by using the piezotensor for silicon in the full representation in Eq. (2.11). The piezotensor for strained Si and $Si_{1-x}Ge_x$ can replace the silicon piezotensor in the derivations below.

2.3.2 Electrical derivation

The transport equations are normally presented in the main crystal coordinate system. However, it is often useful to describe the equations in another coordinate system, the primed coordinate system. This system is rotated by some angle with respect to the main crystal coordinate system.

In this section the stress coordinate system is transformed in order to obtain a simple expression of the stress when a uniaxial stress is applied along any given direction. The electric field vector and current density vector are also transformed in order to apply current and voltage measurements on a resistor oriented along any given direction directly to theory.

The resistor is located in the (001) plane in the calculations below and all transformations are performed in this plane around the z axis, i.e. the [001] direction. (001) silicon substrates are used very often as substrates in MEMS technology due to the favorable anisotropic etching properties. In Fig. 2.5a the transformation of the stress coordinate system is described by the angle ϕ. The current density vector coordinate system is the same as the electric field vector coordinate system which is transformed with an angle θ with respect to the main crystal coordinate system. Recall from Sec. 2.1, that the component subscripts of the symmetric stress tensor of second rank are defined in such a manner, that σ_{ij} describes the stress component acting on the i'th face in the j'th direction. Thus, σ_{ii} corresponds to stresses along the main axes and σ_{ij} corresponds to shear stresses.

At relatively small stress levels only the first term on the right hand side of Eq. (2.10) is contributing to the resistivity. Thus, the resistivity change is linear dependent on the applied stress, and one can write

$$\Delta\rho_{ij} = \bar{\rho}\pi_{ijkl}\sigma_{kl}. \tag{2.14}$$

Each component of the resistivity tensor depends on the resistivity at zero stress and the change caused by an applied stress

$$\rho_{ij} = \rho^0_{ij} + \Delta\rho_{ij} = \rho^0_{ij} + \bar{\rho}\pi_{ijkl}\sigma_{kl}. \tag{2.15}$$

The stress tensor is to be defined in any arbitrary coordinate system. The transformation matrix used is derived in App. D to be

$$M_{ij} = \begin{bmatrix} \cos(\phi) & \sin(\phi) & 0 \\ -\sin(\phi) & \cos(\phi) & 0 \\ 0 & 0 & 1 \end{bmatrix}, \tag{2.16}$$

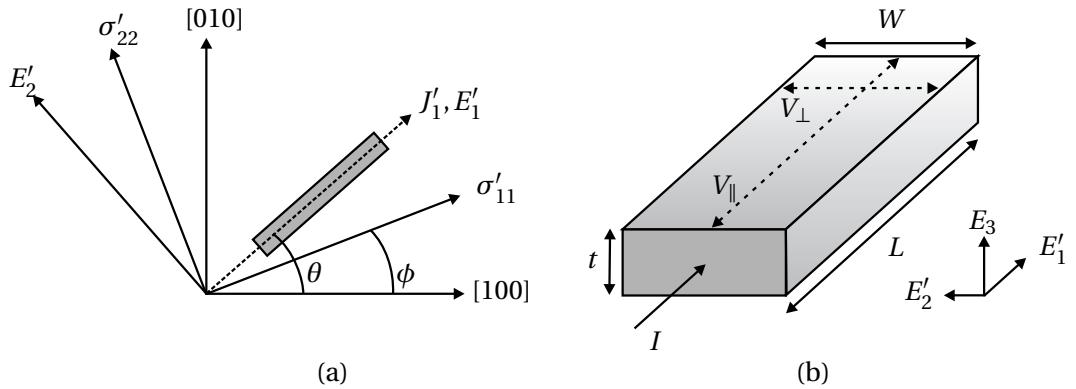


Figure 2.5: (a) In-plane illustration of the piezoresistor (grey) orientation with respect to the crystal direction. The angle θ describes the direction of the current density vector component J'_1 and the electric field vector component E'_1 with respect to the [100] direction. The angle ϕ describes the rotation of the stress coordinate system with respect to the < 100 > coordinate system. (b) Illustration of a simple rectangular resistor where t is the thickness, W is the width, and L is the length. The current I is directed along the electric field vector component E'_1 (which is in the same direction as the current density vector component J'_1). The voltage drop along the resistor i.e. along the current direction $V_\parallel$ and the voltage drop across the resistor i.e. perpendicular to the current direction $V_\perp$ are shown for clarity.

where ϕ is the angle of rotation in the xy plane with respect to the <100> coordinate system on a (001) substrate. The stress tensor is rotated according to this matrix

$$\sigma_{ij} = M^{-1}_{ik} M^{-1}_{jl} \sigma'_{kl}, \tag{2.17}$$

where the primed coordinate system is a new stress coordinate system described by ϕ in the xy plane of a (001) substrate. Thus the resistivity change is

$$\Delta\rho_{ij} = \bar{\rho}\pi_{ijkl} M^{-1}_{km} M^{-1}_{ln} \sigma'_{mn}. \tag{2.18}$$

The electric field is then written as

$$E_i = \rho_{ij} J_j, \tag{2.19}$$

where the current density vector, $\boldsymbol{J}$ is rotated according to

$$J_i = M^{-1}_{ij} J'_j, \tag{2.20}$$

and the transformation matrix includes θ which describes the angle between the new current density coordinate system and the crystal coordinate system. The electric field vector is then rotated with respect to the same angle (θ) as the current density vector

$$E'_i = M_{ij} E_j. \tag{2.21}$$

For a current density vector described as $\boldsymbol{J} = [J'_1, 0, 0]$ in a coordinate system rotated an angle θ with

respect to the crystal directions on a (001) silicon substrate the electric field is thus

$$\boldsymbol{E}' = J_1'\rho_0 \begin{bmatrix} 1+\frac{1}{2}[\pi_{11}+\cos(2\theta)\cos(2\phi)(\pi_{11}-\pi_{12})+\pi_{12}+\sin(2\theta)\sin(2\phi)\pi_{44}]\sigma'_{11} \\ +[-\cos(2\theta)\sin(2\phi)(\pi_{11}-\pi_{12})+\cos(2\phi)\sin(2\theta)\pi_{44}]\sigma'_{12} \\ +\frac{1}{2}[\pi_{11}-\cos(2\theta)\cos(2\phi)(\pi_{11}-\pi_{12})+\pi_{12}-\sin(2\theta)\sin(2\phi)\pi_{44}]\sigma'_{22} \\ +\pi_{12}\sigma'_{33} \\ \frac{1}{2}[\cos(2\phi)\sin(2\theta)(\pi_{11}-\pi_{12})+\cos(2\theta)\sin(2\phi)\pi_{44}]\sigma'_{11} \\ +[\sin(2\theta)\sin(2\phi)(\pi_{11}-\pi_{12})+\cos(2\theta)\cos(2\phi)\pi_{44}]\sigma'_{12} \\ +\frac{1}{2}[\cos(2\phi)\sin(2\theta)(\pi_{11}-\pi_{12})-\cos(2\theta)\sin(2\phi)\pi_{44}]\sigma'_{22} \\ \pi_{44}[\cos(\theta-\phi)\sigma'_{13}+\sin(\theta-\phi)\sigma'_{23}] \end{bmatrix}, \tag{2.22}$$

where ϕ describes the stress coordinate system with respect to the <100> coordinate system. By using $E_0' = \rho_0 J_1'$ the above equation is written as

$$\begin{bmatrix} \frac{E_x'-E_0'}{E_0'} \\ \frac{E_y'}{E_0'} \\ \frac{E_z'}{E_0'} \end{bmatrix} = \begin{bmatrix} \frac{1}{2}[\pi_{11}+\cos(2\theta)\cos(2\phi)(\pi_{11}-\pi_{12})+\pi_{12}+\sin(2\theta)\sin(2\phi)\pi_{44}]\sigma'_{11} \\ +[-\cos(2\theta)\sin(2\phi)(\pi_{11}-\pi_{12})+\cos(2\phi)\sin(2\theta)\pi_{44}]\sigma'_{12} \\ +\frac{1}{2}[\pi_{11}-\cos(2\theta)\cos(2\phi)(\pi_{11}-\pi_{12})+\pi_{12}-\sin(2\theta)\sin(2\phi)\pi_{44}]\sigma'_{22} \\ +\pi_{12}\sigma'_{33} \\ \frac{1}{2}[\cos(2\phi)\sin(2\theta)(\pi_{11}-\pi_{12})+\cos(2\theta)\sin(2\phi)\pi_{44}]\sigma'_{11} \\ +[\sin(2\theta)\sin(2\phi)(\pi_{11}-\pi_{12})+\cos(2\theta)\cos(2\phi)\pi_{44}]\sigma'_{12} \\ +\frac{1}{2}[\cos(2\phi)\sin(2\theta)(\pi_{11}-\pi_{12})-\cos(2\theta)\sin(2\phi)\pi_{44}]\sigma'_{22} \\ \pi_{44}[\cos(\theta-\phi)\sigma'_{13}+\sin(\theta-\phi)\sigma'_{23}] \end{bmatrix}. \tag{2.23}$$

By considering a resistor of uniform doping concentration and confined dimensions as illustrated in Fig. 2.5b the derivation in App. E yields

$$\begin{aligned} \frac{E_x'-E_0'}{E_0'} &= \frac{R-R_0}{R_0} = \frac{\Delta R}{R_0} \\ \frac{E_y'}{E_0'} &= \frac{R_H}{R_\square}, \end{aligned} \tag{2.24}$$

where $\frac{\Delta R}{R_0}$ is the relative resistance change of a resistor $R = \frac{V_\parallel}{I_\parallel}$ with a current density vector $\boldsymbol{J} = [J_1', 0, 0]$, and $R_H = \frac{V_\perp}{I_\parallel}$ is the "Hall type" measurement, where $V_\perp$ is the potential drop (in the xy plane) perpendicular to the current direction described by $I_\parallel$. $R_\square$ is the sheet resistance at zero stress.

By applying a uniaxial stress σ'_{11} to the resistor the equations in Eq. (2.23) and Eq. (2.24) simplify significantly to

$$\begin{aligned} \frac{\Delta R}{R_0} &= \frac{1}{2}[\pi_{11}+\cos(2\theta)\cos(2\phi)(\pi_{11}-\pi_{12})+\pi_{12}+\sin(2\theta)\sin(2\phi)\pi_{44}]\sigma'_{11} \\ \frac{R_H}{R_\square} &= \frac{1}{2}[\cos(2\phi)\sin(2\theta)(\pi_{11}-\pi_{12})+\cos(2\theta)\sin(2\phi)\pi_{44}]\sigma'_{11}. \end{aligned} \tag{2.25}$$

As described in Sec. 2.2 a 4PB fixture is used in this project to characterize the samples. This fixture applies a uniaxial and uniform stress σ'_{11} to the resistor. Thus, when using the 4PB fixture the above equations describe the relation between the change in resistance, the magnitude and direction of the applied stress, the direction of the current density vector, and the three piezocoefficients.

2.4 Application specific examples

The 4PB fixture applies a uniaxial stress in the direction of the chip. Thus, when inserting the chip in the 4PB fixture the stress direction is determined by the orientation of the chip. The chips used in this thesis are cut along two different crystal directions, [100] and [110], respectively.

2.4.1 Stress described in <100>

In this coordinate system $\phi = 0$ and Eq. (2.23) combined with Eq. (2.24) gives

$$\begin{aligned}\frac{\Delta R}{R_0} = &\ \frac{1}{2}[\pi_{11} + \cos(2\theta)(\pi_{11} - \pi_{12}) + \pi_{12}]\sigma_{11} \\ &+ \frac{1}{2}[\pi_{11} - \cos(2\theta)(\pi_{11} - \pi_{12}) + \pi_{12}]\sigma_{22} \\ &+ \sin(2\theta)\pi_{44}\sigma_{12} \\ \frac{R_H}{R_\square} = &\ \frac{1}{2}[\sin(2\theta)(\pi_{11} - \pi_{12})]\sigma_{11} \\ &- \frac{1}{2}[\sin(2\theta)(\pi_{11} - \pi_{12})]\sigma_{22} \\ &+ \cos(2\theta)\pi_{44}\sigma_{12},\end{aligned} \tag{2.26}$$

where σ_{ij} is presented in the main crystal coordinate system and is thus not primed.

2.4.1.1 Uniaxial stress along [100]

When cutting the chip along the main crystal axis, i.e. the [100] direction and applying a uniaxial stress σ_{11} along the direction of the chip the above equation is simplified to

$$\begin{aligned}\frac{\Delta R}{R_0} &= \frac{1}{2}[\pi_{11} + \cos(2\theta)(\pi_{11} - \pi_{12}) + \pi_{12}]\sigma_{11} \\ \frac{R_H}{R_\square} &= \frac{1}{2}[\sin(2\theta)(\pi_{11} - \pi_{12})]\sigma_{11}.\end{aligned} \tag{2.27}$$

From this equation it is seen that π_{11} and π_{12} can be found by placing the resistors along the following crystal directions

$$\begin{aligned}\frac{\Delta R}{R_0}(\theta = 0^\circ) &= \pi_{11}\sigma_{11} \\ \frac{\Delta R}{R_0}(\theta = 90^\circ) &= \pi_{12}\sigma_{11}.\end{aligned} \tag{2.28}$$

When the stress is applied to the chip along the [100] direction the piezocoefficient π_{44} can not be determined since π_{44} is not coupled to σ_{11} in this configuration. The piezocoefficient π_{44} can be found if the stress is applied in the [110] direction.

If the setup applied a pure shear stress σ_{12} to the chip it is seen from Eq. (2.26) that the R_H resistor can be used to determine the piezocoefficient π_{44}

$$\frac{R_H}{R_\square}\left(\theta = 0^\circ\right) = \pi_{44}\sigma_{12}. \tag{2.29}$$

Since the 4PB setup applies a uniaxial normal stress to the resistor this resistor can not be used to determine π_{44}. However, the resistor is used to verify the stress distribution since the resistor enables a measurement of a possible shear stress in the chip.

2.4.2 Stress described in <110>

In the <110> coordinate system $\phi = \frac{\pi}{4}$ and Eq. (2.23) combined with Eq. (2.24) gives

$$\begin{aligned}\frac{\Delta R}{R_0} = &\ \tfrac{1}{2}[\pi_{11}+\pi_{12}+\sin(2\theta)\pi_{44}]\sigma'_{11} \\ &+\tfrac{1}{2}[\pi_{11}+\pi_{12}-\sin(2\theta)\pi_{44}]\sigma'_{22} \\ &-\cos(2\theta)(\pi_{11}-\pi_{12})\sigma'_{12} \\ \frac{R_H}{R_\square} = &\ \tfrac{1}{2}\cos(2\theta)\pi_{44}\sigma'_{11} \\ &-\tfrac{1}{2}\cos(2\theta)\pi_{44}\sigma'_{22} \\ &-\sin(2\theta)(\pi_{11}-\pi_{12})\sigma'_{12},\end{aligned} \tag{2.30}$$

where the primed coordinate system is along the <110> directions and θ is the angle between the resistor direction and the [100] direction.

2.4.2.1 Uniaxial stress along [110]

When applying a uniaxial stress σ'_{11} along the [110] direction the relative resistance change is according to Eq. (2.30)

$$\begin{aligned}\tfrac{\Delta R}{R_0} &= \tfrac{1}{2}[\pi_{11}+\pi_{12}+\sin(2\theta)\pi_{44}]\sigma'_{11} \\ \tfrac{R_H}{R_\square} &= \tfrac{1}{2}\cos(2\theta)\pi_{44}\sigma'_{11}.\end{aligned} \tag{2.31}$$

From this equation it is seen that the piezocoefficient π_{44} can be found using two different approaches. One approach is by measuring the resistance of two (or more) resistors and eliminating π_{11} and π_{12}, for example $R_1(\theta = 45°)$ and $R_2(\theta = 135°)$

$$\frac{\Delta R_1}{R_0}\left(\theta = 45°\right) - \frac{\Delta R_2}{R_0}\left(\theta = 135°\right) = \pi_{44}\sigma'_{11}. \tag{2.32}$$

Another approach is to use one resistor and measure the potential drop across the resistor

$$\frac{R_H}{R_\square}\left(\theta = 0°\right) = \frac{1}{2}\pi_{44}\sigma'_{11}. \tag{2.33}$$

With this resistor orientation the π_{44} piezocoefficient is measured using only one resistor.

2.5 Summary

This chapter introduced the physical stress and strain tensors. This was followed by an analytical description of the setup, the 4PB fixture, used in this project to characterize the piezoresistive properties. It was shown that the setup applies a uniaxial and uniform stress to the center region of the chip surface where the resistors are located.

The relation between the stress and the resistivity of a material is described by the fourth order piezotensor which was simplified in 6 vector notation to contain only 3 independent coefficients, i.e. π_{11}, π_{12}, and π_{44}. The electrical resistance dependency on the resistivity of the material was found for resistors located on a (001) substrate as a function of resistor orientation (described by θ) and stress direction (described by ϕ) with respect to the [100] crystal direction. The three piezocoefficients can be found with many different configurations of stress and resistor orientation. However, in this chapter it was shown that a possible extraction of three piezocoefficients could

involve the use of two chips, one chip to measure π_{11} and π_{12} and one chip to measure π_{44} in the following configurations

$$\begin{gathered}
\frac{\Delta R}{R_0}\left(\theta = 0^\circ, \phi = 0^\circ\right) = \pi_{11}\sigma_{11} \\
\frac{\Delta R}{R_0}\left(\theta = 90^\circ, \phi = 0^\circ\right) = \pi_{12}\sigma_{11} \\
\frac{\Delta R_1}{R_0}\left(\theta = 45^\circ, \phi = 45^\circ\right) - \frac{\Delta R_2}{R_0}\left(\theta = 135^\circ, \phi = 45^\circ\right) = \frac{1}{2}\pi_{44}\sigma'_{11} \\
\frac{R_H}{R_\square}\left(\theta = 0^\circ, \phi = 45^\circ\right) = \frac{1}{2}\pi_{44}\sigma'_{11},
\end{gathered} \tag{2.34}$$

where the unprimed and the primed coordinate systems are in the <100> and <110> crystal coordinate systems, respectively. The next chapter uses the analytical expressions derived in this chapter to determine where to locate the resistors and how to apply the stress in order to obtain the most accurate method to determine the three piezocoefficients. The results leads to a chip design which is presented in the next chapter.

CHAPTER

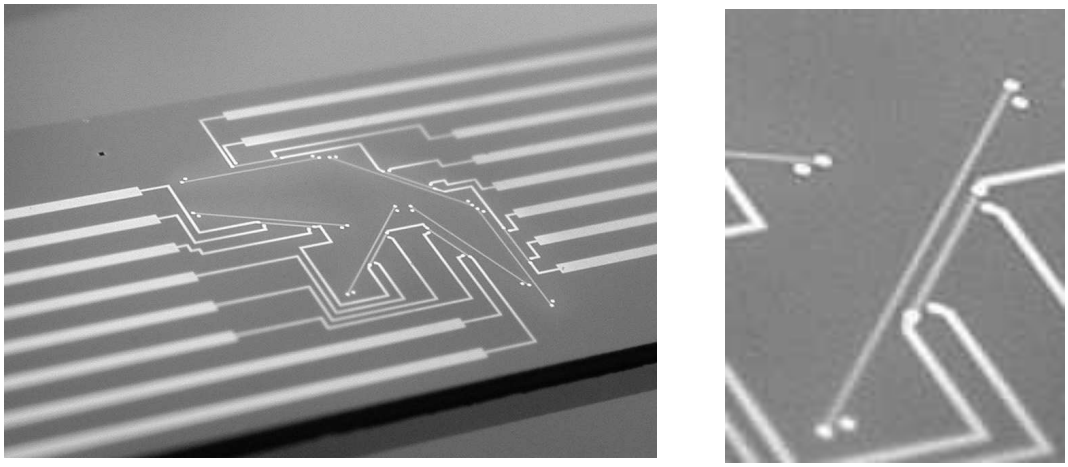
3 Chip design

The theoretical conclusions in the previous chapter are the most important guidelines used in the design of the chips. The chips described in this chapter are used to obtain the three piezocoefficients in silicon π_{11}, π_{12}, and π_{44} with the smallest uncertainty possible. In strained silicon and strained $Si_{1-x}Ge_x$ these coefficients are equivalent to π_{11}, π_{12}, and π_{66}. Furthermore, the design of the chips which are used to determine how the piezocoefficient depends on the width of a nanometer scaled piezoresistor is described. The circular resistor design introduced in Fig. 1.4b on page 4 will be described in Chap. 6.

In the previous chapter it was shown that the relative resistance change in a resistor depends on the orientation of the resistor and the direction of the applied stress. The 4PB fixture applies a uniaxial stress which is perpendicular to the blades in the setup and parallel to the length direction of the chip. In the final design chips from the same wafer are cut in two different crystal directions. One chip is cut along the [100] direction and one chip is cut along the [110] direction in order to apply uniaxial stresses along these two directions, respectively. The design allows for six piezoresistors on each chip. These piezoresistors are oriented along different crystal directions in order to obtain the three piezocoefficients. A zoom-in on the resistor area of a fabricated chip is shown in Fig. 3.1.

This chapter discusses the different chip design possibilities with regards to chip dimension, electrical connection methods, resistor configurations, placement of resistors, and applied stress directions. The conclusions of the discussion leads to the final chip layout.

First, the outer dimensions of the chip are presented. The width and thickness of the chip allow for a practical and simple ”plug and measure" method where the chip is inserted into a standard connector in order to obtain electrical connection. Subsequently, various resistance measurement techniques are discussed in order to apply the most proper method. This is followed by a detailed analysis of the uncertainty caused by a possible misalignment of the resistor orientation and the stress direction with respect to the crystal directions. The analysis is performed for the three piezocoefficients for both p-type and n-type silicon. From this analysis the most accurate determination of the piezocoefficients is found. The above knowledge is used to decide the chip design concerning resistor orientations and stress directions. Finally, the dimensions and design of the individual resistors are presented. In the end of the chapter an overall description of the chip design and wafer layout is given.



(a) (b)

Figure 3.1: Photograph of resistor configuration on a fabricated chip. (a) The chip contains six piezoresistors which are oriented along different angles with respect to the chip direction. The design includes two metal masks which either connect to resistors which have a length to width ratio of 20 (this is the metal mask used in this photograph) or connects to resistors which have a length to width ratio of 80. This variation in length to width ratio is included in the design in order to always obtain resistance values in the kΩ domain for different doping concentrations. (b) A magnified view of one of the piezoresistors.

3.1 Dimensions of the chip

The outer dimensions of the chip are determined by two issues. Firstly, the length to width ratio of the chip has to be large since the theory in Sec. 2.2 assumes a long slender beam. With the use of 4" wafers, there is a natural maximum chip length. In order to efficiently use the whole wafer area, it was decided to find some compromise of large chip length and good exploitation of wafer area. The compromise resulted in a chip length of 4 cm. Secondly, the electrical connection method is non-trivial since the chip must not be mechanically supported anywhere in order not to influence the bending of the chip. This issue is solved by the use of flat flexible cable (FFC) connectors, which are discussed in the following section. The width and thickness of the chip are designed to fit these connectors. The outer dimensions of the chip are

- The chip length is $L = 4$ cm.
- The chip width is $W = 5.3$ mm.
- The chip thickness is $t = 350$ μm.

According to the theory in Sec. 2.2 the 4PB fixture is expected to apply a uniaxial stress to the chip. However, due to the finite dimensions of the chip a transverse stress is also present. This is described in detail in App. B.2. The distance between the inner blades in the fixture is $b = 12$ mm as illustrated in Fig. 2.3 on page 19. The magnitude of the transverse stress varies as a function of the location on the chip and the width of the chip. The transverse stress is zero at the transversal surfaces (i.e. the chip surfaces normal to the transverse stress σ'_{22}) and the confinement caused by the inner blades results in an increasing value of the transverse stress σ'_{22} when approaching the middle of the chip. Along the length of the chip the stress σ'_{22} in the resistors is smallest when the

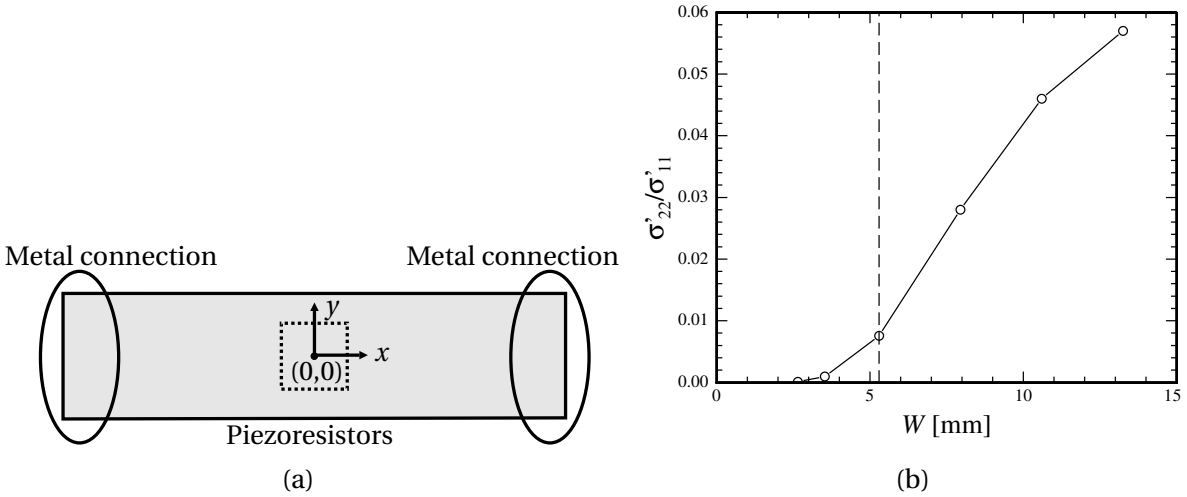


Figure 3.2: (a) Illustration of chip. The piezoresistors are located on the surface in the center of the chip in a 3×3 mm^2 area sketched by the dashed square. The center of the chip is in the coordinate (x, y)=(0,0). (b) FEM simulation of the ratio $\frac{\sigma'_{22}}{\sigma'_{11}}$ as a function of chip width. The distance between the inner blades in the 4PB fixture is $b = 12$ mm and the measurement is performed in the resistor area on the chip surface in the point where the transverse stress has its maximum value $(x, y) = (1.5\text{ mm},0)$. The black dashed line indicates the realized width of the chip, $W = 5.3$ mm. By choosing a width smaller than $W = 3.5$ mm the transverse stress σ'_{22} is smaller than 0.1% of the applied stress σ'_{11}.

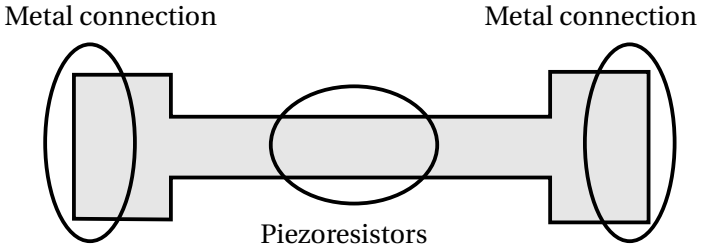
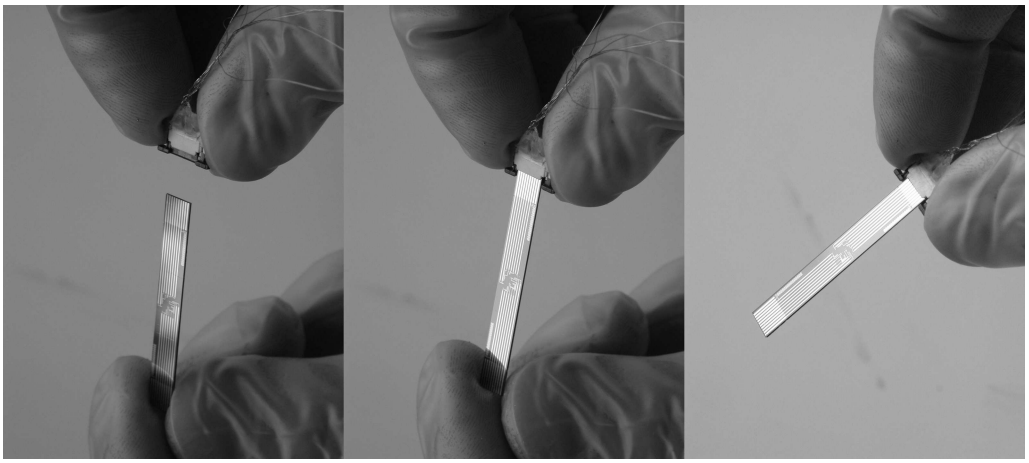


Figure 3.3: Suggested chip shape for future designs. The design enables FFC connection at the ends of the chip, $W = 5.3$ mm and is decreased in width in the region of the chip that is inserted in the 4PB fixture. According to Fig. 3.2b the inner width of the chip needs to be 3.5 mm in order to obtain a transverse stress that is less than 0.1% of σ'_{11}.



(a) (b) (c)

Figure 3.4: Photo sequence of FFC connection to chip. With a calm hand, the chip is inserted into the connector (a). The chip is fastened to the connector (b), and ready to use (c).

resistors are located as far away as possible from the blades, i.e. in the center of the chip, since the chip is placed symmetrically in between the blades. The resistors are placed on the chip surface in a square of 3×3 mm^2 in the center region of the chip. The transverse stress is evaluated where this stress is largest, i.e. 1.5 mm from the center of the chip along the length direction and in the middle of the chip along the transverse direction, i.e. $(x, y) = (1.5\text{ mm}, 0)$ where the xy coordinate system is defined in Fig. 3.2a. In order to investigate this further a simple finite element model (FEM) using *COMSOL* [55] has been developed. From this model the ratio $\frac{\sigma'_{22}}{\sigma'_{11}}$ is plotted as a function of chip width, W, in Fig. 3.2b in the point $(x, y) = (1.5\text{ mm}, 0)$ on the chip surface. It is seen that a maximum transverse stress $\sigma'_{22} = 0.8\%$ of σ'_{11} is present in the chip. It is also seen that by decreasing the width even further a significantly smaller transverse stress is present. Thus, in the light of this analysis the next chip generations could with advantage be fabricated with a smaller width. However, since the ends of the chip need to fit into the FFC connectors, a shape as shown in Fig. 3.3 is suggested for future designs. According to Fig. 3.2b the width of the chip in the resistor area need to be 3.5 mm in order to obtain a transverse stress that is less than 0.1% of σ'_{11}.

The complete new FFC connection method is discussed in the next section.

3.1.1 Electrical connection

Naturally, the electrical connection to the chip is very important. Since the 4PB fixture bends the whole chip it can not be supported by anything that prevents this bend. Furthermore, the connection method must not result in any significant stress distribution in the area of the resistors on the chip. Zero insertion force FFC chip connection is a practical "plug and measure" connection where the chip is plugged directly into the electrical connector. After use the chip is unplugged and another chip can be inserted into the connector. Fig. 3.4 shows the simple connection scheme.

The dimensions of the metal paths on an FFC are adopted onto the chip. The FFC connector has ten connections with a pitch of 0.50 mm. The width of the chip is set to match the width of the FFC, $W = 5.3$ mm. The data sheets for the 0.50 mm pitch FFC connector and the matching FFC are

listed in App. F and App. G, respectively. With the use of both ends of the chip, a total connection of 20 metal paths is possible. This limits the number of resistors on the chip. In order for the chip to fit into the FFC connector the thickness of the chip has to be approximately 0.3 mm, which is the thickness of an FFC. However, a chip with a thickness of $t = 350$ μm (which is the most common thickness of a double side polished 4" wafer) can also be inserted.

The weight of the FFC connector is $m \approx 0.14$ g. The applied stress from the 4PB fixture is several decades larger than the stress associated with the gravitational force resulting from these connectors. Thus, the gravitational force from the connectors does not affect the stress distribution in the chip. Furthermore, resistance measurements have been performed on the chip with and without connector by the use of probes and there is no significantly change in the electrical resistance. Thus, there is no significant stress contribution from the connectors to the resistor area. The contact resistance between FFC connector and chip is measured to be approximately 0.1Ω which is insignificantly small compared to the resistance of the resistors which is in the kΩ domain.

The connector concept is a more reliable and more convenient contact method than what has been previously used. Probes are put directly onto the chip in the region of the resistors in Ref. [23]. This approach seems to lead to some uncertainty, since the probes affect the stress distribution near the resistors. An extended version of this is presented in Ref. [11] where the chip is wire bonded near the resistor location though a hole on a PCB located above the chip. The contribution from the wire bonds to the stress distribution is negligible. In a previous project at MIC heavy wire bonding (performed at Grundfos A/S) to the ends of the chip was used for electrical connection [56]. The bonds are very fragile and furthermore this bonding method is not possible at MIC. A third method is to integrate the electrical connections into the setup such that the upper blades of the 4PB fixture both work as electrical contacts and force actuators. This approach seems promising, however some research needs to be done in order to include correct metal wiring on the PEEK surface (the 4PB fixture is machined in PEEK).

3.2 Resistance measurement method

The electrical resistance is measured by a four terminal measurement. This measurement method is very reliable and it is a simple way of measuring the resistance. A constant current is forced through the resistor between two contacts while a high impedance voltage measurement is performed on two other contacts. The voltage measurement is either performed along the direction of the current i.e. $V_{\parallel}$ to obtain R or perpendicular to the direction of the current i.e. $V_{\perp}$ to obtain R_H. The four terminal measurement measures the true resistance in the resistor and eliminates contact resistances and resistances in the metal wiring.

The four terminal measurement enables a large number of resistors with different orientations on one chip. The resistors are placed in a series connection and the current is forced through several resistors at the same time. In this way, the number of contacts necessary for the measurements is minimized.

By using the FFC connection method presented in the previous section a total number of 20 electrical contacts are available. An example of the chip layout is shown in Fig. 3.5. For practical purposes there is no electrical connection from one end of the chip to the other end of the chip. Each end connects three resistors in a series connection for current injection (contact 1 or 2 to contact 9) while high impedance voltage measurements are performed on each resistor (contact 3 and 4, contact 5 and 6, and contact 7 and 8). The ends of the chip also contains a substrate contact (contact 0) to ensure that the pn junction between substrate and resistor is reverse biased.

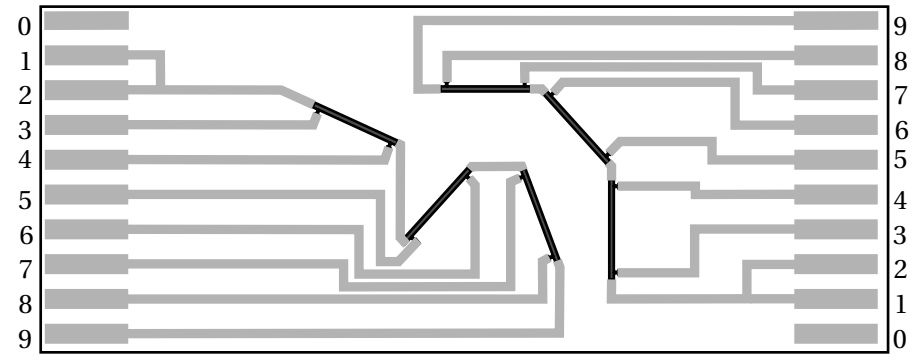


Figure 3.5: Presentation of chip layout. The resistors (dark grey) are series connected by metal wiring (light grey) in order to allow a current through the resistors from contact 1 or 2 to contact 9 while high impedance voltage measurements are performed on contact 3 and 4, contact 5 and 6, and contact 7 and 8. Contact 0 is connected to the substrate.

As described in Sec. 3.1.1 the metal pattern in the two ends of the chip is determined by the FFC connection method.

Recall, from Eq. (2.28) on page 26 that both the π_{11} and the π_{12} piezocoefficient can be found by doing this type of measurement on one resistor for each coefficient. The π_{44} coefficient is found from measurements on two resistors when measuring the potential drop parallel to the current density, Eq. (2.32) on page 27, and only one resistor when $V_\perp$ is measured, Eq. (2.33) on page 27.

A simpler resistance measurement technique that allows for fewer electrical connections is a two terminal resistance measurement. The current is forced through two terminals while the voltage drop is measured across the same two terminals. The major disadvantage with this method is that the parasitic resistances, e.g. contact resistances and metal wire resistances are included in the resistance measurement. Secondly, R_H can not be measured with this method. A third disadvantage, which also applies for the four terminal measurement, is that it is the absolute resistance that is measured and not the resistance change. The resistance change is calculated afterwards, by subtracting the resistance in the unstressed resistor with the resistance in the stressed resistor.

The relative resistance change can be measured directly by placing the piezoresistors in a Wheatstone bridge configuration. If the stress σ'_{11} is applied along the [110] direction, and if two resistors are placed along the stress direction and two resistors are placed perpendicular to the stress direction one obtains the output voltage V_{out}

$$V_{out} \approx \tfrac{1}{2}\pi_{44}\sigma'_{11}V_{in}, \tag{3.1}$$

where V_{in} is the input voltage. This equation is not exact since it is assumed that the contribution from the two piezocoefficients π_{11} and π_{12} is negligible. This is a reasonable assumption in p-type silicon, however in n-type silicon this can not be assumed. A Wheatstone bridge configuration can also be used to extract π_{11} and π_{12} although a number of the resistors need to be placed in a stress-free location. This results in a long distance between the resistors connected in the Wheatstone bridge giving a significant wire resistance which contributes to the output.

The Wheatstone bridge measurement and the two terminal measurement are not included in the chip design. The high impedance four terminal measurement is the method chosen since it offers the most precise resistance measurement of the three methods as discussed above.

A completely different approach is not to use a structure as the above structures, where a unidirectional current is injected in the resistor, but to use a structure that allows for a change of the current density vector direction. In order to obtain this, a circular resistor has been designed and used for piezoresistance characterization. This structure will be described in detail individually in Chap. 6. In the following the design of the unidirectional resistors will be described. The unidirectional resistors have been used in order to obtain the results which will be presented in Chap. 5.

3.3 Uncertainty estimation

This section estimates the precision of the extracted piezocoefficients. The method used to determine the piezocoefficients is to apply a known stress to the resistor, measure the resistance change of the resistor, and then use the theory in Sec. 2.3.2 in order to convert the resistance value to a piezocoefficient value. The measured resistance is a function of the piezocoefficients, the resistor orientation, and the stress direction and magnitude.

For example, from Eq. (2.25) on page 25 the π_{44} piezocoefficient is

$$\begin{aligned}&\pi_{44}(\theta,\phi,\tfrac{\Delta R}{R},\sigma'_{11}) = \\ &\tfrac{2}{\sin(2\theta)\sin(2\phi)}\left\{\tfrac{1}{\sigma'_{11}}\tfrac{\Delta R}{R} - \tfrac{1}{2}[1+\cos(2\theta)\cos(2\phi)]\pi_{11} - \tfrac{1}{2}[1-\cos(2\theta)\cos(2\phi)]\pi_{12}\right\},\end{aligned} \tag{3.2}$$

where σ'_{11} is the stress applied in the direction described by ϕ and θ describes the direction of the resistor, both with respect to the [100] direction. For small variations in the variables the change in π_{44} is written as (assuming that π_{11} and π_{12} are constant)

$$\delta\pi_{44}(\theta,\phi,\frac{\Delta R}{R},\sigma'_{11}) = \frac{\partial\pi_{44}}{\partial\theta}\delta\theta + \frac{\partial\pi_{44}}{\partial\phi}\delta\phi + \frac{\partial\pi_{44}}{\partial\left(\frac{\Delta R}{R}\right)}\delta\left(\frac{\Delta R}{R}\right) + \frac{\partial\pi_{44}}{\partial\sigma'_{11}}\delta\sigma'_{11}, \tag{3.3}$$

where similar equations apply for π_{11} and π_{12} (replace π_{44} with these). The above equation is valid for a uniaxial applied stress σ'_{11}. If the stress is not uniaxial and other stress components are present the uncertainty will naturally also depend on these contributions. Thus, the uncertainty depends on five factors:

- Crystal misalignment of the resistor described by $\delta\theta$.
- Crystal misalignment of the stress direction described by $\delta\phi$.
- Uncertainty of electrical resistance measurement $\delta\left(\frac{\Delta R}{R}\right)$
- Variation of applied stress $\delta\sigma'_{11}$.
- Contributions from stress components other than σ'_{11}.

Each of these contributions to the uncertainty will be discussed in the sections below.

3.3.1 Crystal misalignment

This analysis focuses on the variation of the extracted piezocoefficient due to a misalignment of the resistor orientation and stress direction. The full analysis is carried out for the π_{44} piezocoefficient. The approach to estimate the uncertainty of π_{11} and π_{12} is similar and the results are outlined at the end of the section. The starting point is Eq. (3.3) and only the two first terms are considered in this section. The two last terms are discussed in the following sections.

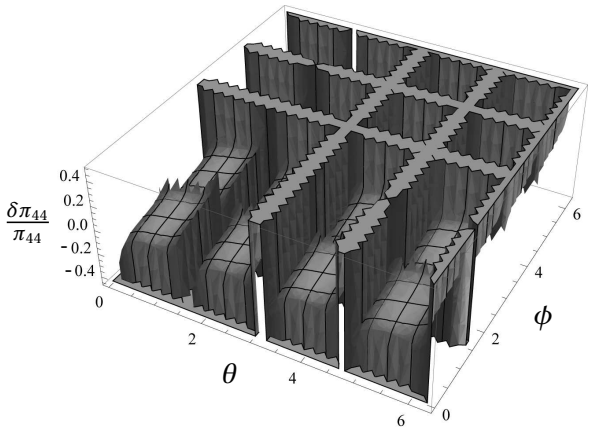


Figure 3.6: 3D plot of the uncertainty of π_{44} in p-type silicon according to Eq. (3.5) as a function of resistor orientation (described by θ) and stress direction (described by ϕ), where $\frac{\Delta R}{R} = 0.05$, $\sigma'_{11} = 70$ MPa, and $\delta\theta = 1°$. The uncertainty is smallest at $\theta, \phi = n\frac{\pi}{4}$ where $n = 1, 3, ...$

The chip direction and resistor orientation are defined with two lithography masks which are aligned to each other in a photolithographic process. Thus, the internal misalignment of the two masks is negligible (a misalignment of 10 μm across the wafer a distance of 8.6 cm from one alignment mark to the other alignment mark results in a misalignment of 0.007°). A misalignment to the crystal direction due to wafer specifications (±2°) is the main contribution to $\delta\theta$ and $\delta\phi$. A crystal alignment process step is included in the fabrication process, which will be described in Sec. 4.1.1, in order to obtain a crystal alignment of $\delta\theta = \delta\phi = 0.1°$. However, this step can not be performed on all wafers, as will be described in Sec. 4.2, thus in the following an uncertainty of $\delta\theta = \delta\phi = 1°$ is assumed. The placement of the chip in the 4PB fixture ensures that the chip is aligned correctly and that the applied stress is directed along the chip direction. Since, θ and ϕ are aligned to each other with a high precision $\delta\theta = \delta\phi$, and Eq. (3.3) is simplified to

$$\delta\pi_{44}(\theta, \phi, \frac{\Delta R}{R}, \sigma'_{11}, \delta\theta) = \left(\frac{\partial\pi_{44}}{\partial\theta} + \frac{\partial\pi_{44}}{\partial\phi}\right)\delta\theta. \tag{3.4}$$

The relative variation is then

$$\frac{\delta\pi_{44}(\theta, \phi, \frac{\Delta R}{R}, \sigma'_{11}, \delta\theta)}{\pi_{44}} = \frac{1}{\pi_{44}}\left(\frac{\partial\pi_{44}}{\partial\theta} + \frac{\partial\pi_{44}}{\partial\phi}\right)\delta\theta. \tag{3.5}$$

This function is plotted in Fig. 3.6 as a function of θ and ϕ for $\delta\theta = 1°$, $\sigma'_{11} = 70$ MPa, and $\frac{\Delta R}{R} = 0.05$ (obtained if $\phi = \theta = \frac{\pi}{4}$). The values of the piezocoefficients are those reported in Ref. [21] listed in Table 1.1 on page 6 and they will be used in the following analysis. It is seen that the smallest relative uncertainty is for $\theta_0, \phi_0 = n\frac{\pi}{4}$ where $n = 1, 3, ...$ Fig. 3.7 shows the function at $\phi = \frac{\pi}{4}$ for different misalignments $\delta\theta = 0.5°, 1°, 5°$. By inserting $\delta\theta = 1°$ in Eq. (3.5) and adjusting $\theta = \theta_0 + \delta\theta$ and $\phi = \phi_0 + \delta\theta$ the uncertainty is $\frac{\delta\pi_{44}}{\pi_{44}} = 0.2\%$. Thus, the π_{44} piezocoefficient in p-type silicon is determined very precisely. Even at a relative large misalignment of $\delta\theta = 1°$ the uncertainty is less than 1%. The large value of the piezocoefficient π_{44} compared to π_{11} and π_{12} results in this small uncertainty. In n-type silicon the piezocoefficients have different magnitudes compared to p-type and this naturally affects the uncertainty calculation. Fig. 3.8 shows the variation of π_{44} as a

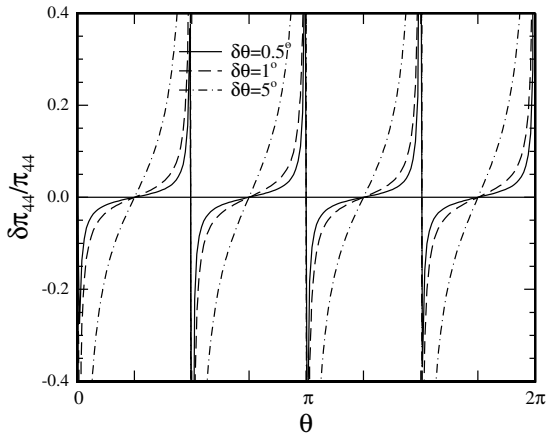


Figure 3.7: The uncertainty of the piezocoefficient π_{44} in p-type silicon according to Eq. (3.5) for different crystal misalignments, $\delta\theta$, as a function of resistor orientation at a stress direction of $\phi = \frac{\pi}{4}$, $\sigma'_{11} = 70$ MPa, and $\frac{\Delta R}{R} = 0.05$. The uncertainty is lowest for resistors oriented longitudinal ($\theta = \frac{\pi}{4}$) and transversal ($\theta = \frac{3\pi}{4}$) to the stress direction.

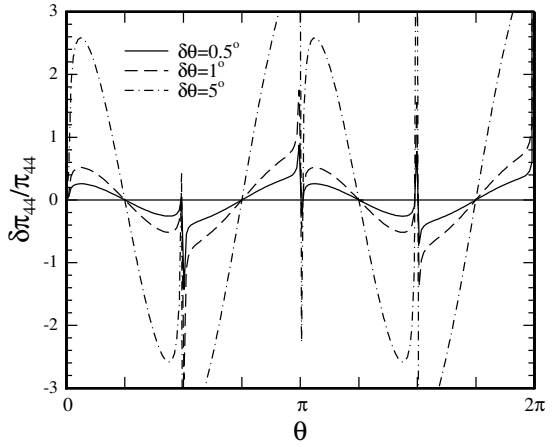


Figure 3.8: The uncertainty of π_{44} in n-type silicon for $\phi = \frac{\pi}{4}$. The uncertainty is smallest at resistor orientations longitudinal and transversal to the stress direction.

function of the resistor orientation at a constant stress ($\sigma'_{11} = 70$ MPa) and $\frac{\Delta R}{R} = -0.02$ (obtained if $\phi = \theta = \frac{\pi}{4}$). Notice the almost ten times larger scale on the $\frac{\delta\pi_{44}}{\pi_{44}}$-axis in Fig. 3.8 compared to Fig. 3.7. The uncertainty is lowest at $\theta_0 = n\frac{\pi}{4}$ where $n = 1, 3, \ldots$. A misalignment of $\delta\theta = 1^\circ$ for $\theta_0, \phi_0 = \frac{\pi}{4}$ results in an estimated uncertainty of 4.4% on π_{44}.

The same analysis is performed on π_{11} and π_{12} for both p-type and n-type silicon in order to find the angles θ_0 and ϕ_0 where the piezocoefficients are determined with the smallest uncertainty. The uncertainties are found with a misalignment of $\delta\theta = 1^\circ$. The results are summarized in Table 3.1 and shows that the large piezocoefficients π_{44} in p-type silicon and π_{11} and π_{12} in n-type silicon can be determined with a very high accuracy. The accuracy of the piezocoefficient π_{12} in

	θ_0	ϕ_0	p-type $\frac{\delta\pi_{ij}}{\pi_{ij}}$	n-type $\frac{\delta\pi_{ij}}{\pi_{ij}}$
π_{11}	0	0	2.5%	0.2%
π_{12}	$\frac{\pi}{2}$	0	15.6%	0.3%
π_{44}	$\frac{\pi}{4}$	$\frac{\pi}{4}$	0.2%	4.4%

Table 3.1: The minimum uncertainty of the extracted piezocoefficients $\frac{\delta\pi_{ij}}{\pi_{ij}}$ with a misalignment angle of $\delta\theta = 1^\circ$ are found at the angle combinations of θ_0 and ϕ_0. If the piezocoefficients are to be determined with the highest possible accuracy it is seen that two chips are needed. One chip in order to determine π_{11} and π_{12}, and one chip on order to determine π_{44}.

p-type silicon is very low due to the very small value of this coefficient compared to π_{44}. It is seen that in order to obtain the highest possible accuracy of all three piezocoefficients a two chip solution is needed, where one chip is used to determine π_{11} and π_{12}, and one chip is used to determine π_{44}.

3.3.2 Stress distribution

The stress distribution in the chip is discussed thoroughly in App. B.2 where the 4PB setup is described. This section summarizes the conclusions.

The uncertainty of the applied stress from Eq. (2.7) on page 20 is described by (taken directly from App. B.2)

$$\frac{\Delta\sigma'_{11}}{\sigma'_{11}} = \sqrt{\left(\frac{\Delta F}{F}\right)^2 + \left(\frac{\Delta a}{a}\right)^2 + 2\left(\frac{\Delta t}{t}\right)^2 + \left(\frac{\Delta W}{W}\right)^2} = 1.5\%, \tag{3.6}$$

where F is the applied force to the 4PB fixture, a is the distance between the inner and outer blades, t is the thickness of the chip, and W is the width of the chip.

Recall, from the discussion in Sec. 3.1 that a maximum transverse stress of 0.8% of σ'_{11} is present in the chip. Since the stresses σ'_{11} and σ'_{22} are coupled in Eq. (2.23) on page 25 as $(\sigma'_{11} + \sigma'_{22})$ or $(\sigma'_{11} - \sigma'_{22})$ the magnitude of the transverse stress is added to the uncertainty of σ'_{11}. Thus the total uncertainty of the estimation of σ'_{11} is

$$\frac{\Delta\sigma'_{11}}{\sigma'_{11}} = \sqrt{(1.5\%)^2 + (0.8\%)^2} = 1.7\%. \tag{3.7}$$

Characterization of the 4PB fixture showed that a large shear stress of maximum 4% of σ'_{11} is present in the chip. This shear stress is caused by a vertical misalignment of the inner blades in the 4PB fixture. The shear stress affects the measurement of the piezocoefficients directly according to Eq. (2.26) on page 26 and Eq. (2.30) on page 27 for the chips stressed along the [100] and [110] crystal direction, respectively. These equations are listed below for $\sigma'_{22} = 0$

$$\begin{aligned} \tfrac{\Delta R}{R_0}|_{\phi=0} &= \tfrac{1}{2}[\pi_{11} + \cos(2\theta)(\pi_{11} - \pi_{12}) + \pi_{12}]\sigma_{11} + \sin(2\theta)\pi_{44}\sigma'_{12} \\ \tfrac{\Delta R}{R_0}|_{\phi=\frac{\pi}{4}} &= \tfrac{1}{2}[\pi_{11} + \pi_{12} + \sin(2\theta)\pi_{44}]\sigma_{11} - \cos(2\theta)(\pi_{11} - \pi_{12})\sigma'_{12} \end{aligned} . \tag{3.8}$$

The uncertainty of the piezocoefficients due to the contribution from the shear stress is obtained by inserting the angles of θ in Eq. (3.8) and estimate the change in $\frac{\Delta R}{R_0}$ caused by the shear stress.

Again, the piezocoefficient values listed in Table 1.1 on page 6 are used. The relative change in $\frac{\Delta R}{R_0}$ is the uncertainty of the measurement and is thus a measure of the uncertainty of the extracted piezocoefficient. The equations show that the contribution from the σ'_{12} component is zero for the angle combinations listed in Table 3.1 thus the shear stress should not contribute to the uncertainty of the piezocoefficients. However, for some angle combinations the shear stress can be significant if a small misalignment is present. This contribution is basically a function of the ratios of the piezocoefficient values. The effect of the extra contribution from the shear stress is listed in Table 3.2 for the angle combinations in Table 3.1. The table concludes that the shear stress is only contributing significantly to the uncertainty of π_{11} (4%) and π_{12} (25%) in p-type silicon. The example below describes how these numbers are calculated.

3.3.2.1 Example

The chip is stressed along the [100] direction, i.e. $\phi = 0$. If $\theta = 0$ Eq. (3.8) is

$$\frac{\Delta R}{R_0} = \pi_{11}\sigma_{11}. \tag{3.9}$$

However, if a misalignment of $\delta\theta = \delta\phi = 1^\circ$ is present, the shear stress contributes to the measurement. From Eq. (2.23) and Eq. (2.24) on page 25 the relative resistance change is

$$\begin{aligned} \frac{\Delta R}{R_0} = \quad & \tfrac{1}{2}[\pi_{11} + \cos(2\theta)\cos(2\phi)(\pi_{11} - \pi_{12}) + \pi_{12} + \sin(2\theta)\sin(2\phi)\pi_{44}]\sigma_{11} \\ & + [-\cos(2\theta)\sin(2\phi)(\pi_{11} - \pi_{12}) + \cos(2\phi)\sin(2\theta)\pi_{44}]\sigma_{12}, \end{aligned} \tag{3.10}$$

where only σ_{11} and σ_{12} are considered. For a shear stress of 4% of σ_{11} and a misalignment of $\delta\theta = \delta\phi = 1^\circ$ this results in an relative resistance change of

$$\begin{aligned} \frac{\Delta R}{R_0} = \quad & \tfrac{1}{2}[\pi_{11} + \cos(2^\circ)\cos(2^\circ)(\pi_{11} - \pi_{12}) + \pi_{12} + \sin(2^\circ)\sin(2^\circ)\pi_{44}]\sigma_{11} \\ & + [-\cos(2^\circ)\sin(2^\circ)(\pi_{11} - \pi_{12}) + \cos(2^\circ)\sin(2^\circ)\pi_{44}] \cdot 0.04\sigma_{11} \\ & \approx \pi_{11} + 0.0006\pi_{44} - 0.0014(\pi_{11} - \pi_{12}) + 0.0014\pi_{44}. \end{aligned} \tag{3.11}$$

The approximate variation of the two results of $\frac{\Delta R}{R}$ is then

$$\frac{\delta\left(\frac{\Delta R}{R}\right)}{\frac{\Delta R}{R}} \approx \frac{0.0006\pi_{44} - 0.0014(\pi_{11} - \pi_{12}) + 0.0014\pi_{44}}{\pi_{11}}. \tag{3.12}$$

By inserting the values of the piezocoefficients in Table 1.1 on page 6 the uncertainties are $\frac{\delta\left(\frac{\Delta R}{R}\right)}{\frac{\Delta R}{R}} \approx$ 4% for p-type and $\frac{\delta\left(\frac{\Delta R}{R}\right)}{\frac{\Delta R}{R}} \approx 0$ for n-type.

3.3.3 Electrical measurement

The electronic instruments used to measure the voltage drop and to inject the current are all high precision instruments. The Keithley 2700 Multimeter with multiplexer which is used for the high impedance voltage measurements has an accuracy below 0.1% at a voltage of 1 V and the Keithley 2400 Sourcemeter which is used for current injection has a current source accuracy of 0.03% at 100 μA.

The instrumentation used to measure the silicon nanowires are also all high precision instruments. The current is injected using a HP 4155B Semiconductor Parameter Analyzer which has

	θ_0	ϕ_0	p-type $\frac{\delta\pi_{ij}}{\pi_{ij}}$	n-type $\frac{\delta\pi_{ij}}{\pi_{ij}}$
π_{11}	0	0	4%	0.2%
π_{12}	$\frac{\pi}{2}$	0	25%	0.4%
π_{44}	$\frac{\pi}{4}$	$\frac{\pi}{4}$	0.5%	0.4%

Table 3.2: Uncertainty of the measurement due to a shear stress contribution of 4% of σ'_{11} for a misalignment angle of $\delta\theta = \delta\phi = 1°$. The shear stress affects the uncertainty of the measurement of π_{11} and π_{12} in p-type silicon, since the shear stress is coupled to the piezocoefficient π_{44} in Eq. (3.10).

an accuracy of $\approx \pm 0.5\%$ if $I = 1$ nA. The resistor potentials are measured by using a Keithley 2182 Nanovoltmeter which has an accuracy below 0.1% at a voltage drop of 100 μV.

The above mentioned uncertainties are significantly smaller than the uncertainties described in the above sections and can thus be neglected.

3.3.4 Summary

In this section the contributions to the uncertainty of the measurements of the piezocoefficients were described and estimated. The angle combinations of θ and ϕ where the uncertainties of the three piezocoefficients are lowest have been analyzed and with an estimated angle misalignment of 1° the uncertainties of the three piezocoefficients were determined (Table 3.1). The stress distribution in the chip was described and uncertainties due to the magnitude of the stress and due to the presence of other stress components were presented (Eq. (3.7) and Table 3.2). The uncertainty of the electrical equipment used is significantly smaller than the uncertainties caused by the other effects listed above.

The uncertainties from Table 3.1 $\left(\frac{\delta\pi_{ij}}{\pi_{ij}} \text{ due to } \delta\theta\right)$, Table 3.2 $\left(\frac{\delta\pi_{ij}}{\pi_{ij}} \text{ due to } \sigma'_{12}\right)$, and Eq. (3.7) $\left(\frac{\delta\pi_{ij}}{\pi_{ij}} \text{ due to } \delta\sigma'_{11}\right)$ results in a total uncertainty of the piezocoefficient written as

$$\frac{\delta\pi_{ij}}{\pi_{ij}} = \sqrt{\left(\left.\frac{\delta\pi_{ij}}{\pi_{ij}}\right|_{\text{due to } \delta\theta}\right)^2 + \left(\left.\frac{\delta\pi_{ij}}{\pi_{ij}}\right|_{\text{due to } \delta\sigma'_{11}}\right)^2 + \left(\left.\frac{\delta\pi_{ij}}{\pi_{ij}}\right|_{\text{due to } \sigma'_{12}}\right)^2}. \tag{3.13}$$

The uncertainties obtained by the above equation is listed in Table 3.3. These uncertainties are the lowest possible uncertainties if a misalignment of $\delta\theta = \delta\phi = 1°$ is present. The piezocoefficients π_{11} and π_{12} in n-type silicon and π_{44} in p-type silicon are determined with a very high accuracy. The uncertainties of the remaining piezocoefficients are significantly larger due to the small numerical values of these piezocoefficients compared to the other piezocoefficients.

3.4 Resistor configuration

The resistors are oriented along different directions with respect to the crystal axes. Four chips have been designed, all shown in Fig. 3.9. The design shown in Fig. 3.9a is used for two chips. These two chips are cut along the [100] and [110] directions, respectively. The length directions of the chips in Fig. 3.9b and Fig. 3.9c are along the [100] and [110] direction, respectively. The relative resistance change of the resistors according to Eq. (2.25) on page 25 is listed in Table 3.4. With

	θ_0	ϕ_0	p-type $\frac{\delta\pi_{ij}}{\pi_{ij}}$	n-type $\frac{\delta\pi_{ij}}{\pi_{ij}}$
π_{11}	0	0	5.0%	1.7%
π_{12}	$\frac{\pi}{2}$	0	29.5%	1.8%
π_{44}	$\frac{\pi}{4}$	$\frac{\pi}{4}$	1.8%	4.8%

Table 3.3: Total uncertainty of the piezocoefficients according to Eq. (3.13) for a misalignment angle of $\delta\theta = 1°$. These uncertainties are estimated as worst case scenario since some of the characterized chips are fabricated with a possible misalignment of $\delta\theta = 0.1°$. The uncertainty is very low for the measurements of π_{44} in p-type silicon and π_{11} and π_{12} in n-type silicon. For π_{12} in p-type silicon the uncertainty is very large due to its very small value compared to π_{44}.

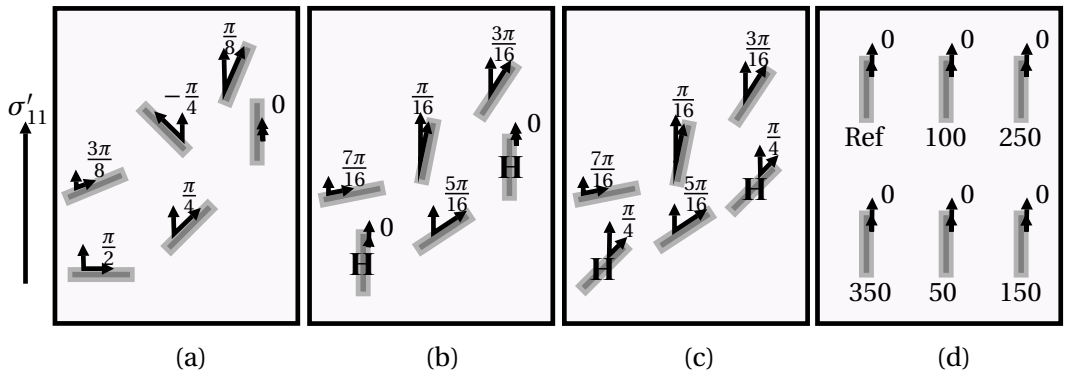


Figure 3.9: Illustration of chip design. For design (a) the length direction of the chip is cut along the [100] direction and the [110] direction. For design (b) and (c) the chip is cut along [100] and [110], respectively. These designs consist of resistors that are directed along different angles with respect to the stress direction and are used for piezoresistance analysis of silicon, strained silicon and strained $Si_{1-x}Ge_x$. The "H" in (b) and (c) indicates that the resistor is a "Hall type" resistor. Design (d) is cut along the [110] direction and consists of five nanowire resistors of different widths (50 nm - 350 nm) and a reference micrometer scale resistor of width 25 μm (ref). The resistors are all directed along the [110] direction and are used to analyze the piezoresistance in silicon nanowires as a function of nanowire width.

this configuration 9 different angles of the resistors with respect to the stress direction is obtained. The measurements from these resistors are used to verify the theory in Sec. 2.3.2 for both silicon and pre-strained silicon samples. However, the most important resistors are the resistors oriented according to Table 3.3 that determines the three piezocoefficients with the lowest uncertainty. All of the resistors listed in Table 3.4 are used for piezoresistive characterization except the resistor listed in the last row. This “Hall type" resistor is used to characterize the shear stress in the chip. The use of this resistor resulted in the conclusions in the shear stress analysis in Sec. 3.3.2. The chip in Fig. 3.9d is cut along the [110] direction and is designed to measure the piezoresistance effect of a resistor directed along the [110] direction as a function of resistor width. The chip consists of six resistors, one reference resistor which has the same size as the resistors in the other designs (micrometer scale) and five nanowire resistors with widths varying from 50 nm to 350 nm.

θ'	$\sigma_{11} \parallel [100]$ $\frac{\Delta R}{R}\frac{1}{\sigma_{11}}$	$\sigma'_{11} \parallel [110]$ $\frac{\Delta R}{R}\frac{1}{\sigma'_{11}}$
0	π_{11}	$\frac{1}{2}(\pi_{11}+\pi_{12}+\pi_{44})$
$\frac{\pi}{16}$	$0.961940\pi_{11}$-$0.038060\pi_{12}$	$\frac{1}{2}(\pi_{11}+\pi_{12}+0.923880\pi_{44})$
$\frac{\pi}{8}$	$0.853553\pi_{11}+0.146447\pi_{12}$	$\frac{1}{2}(\pi_{11}+\pi_{12})+0.353553\pi_{44}$
$\frac{3\pi}{16}$	$0.691342\pi_{11}+0.308658\pi_{12}$	$\frac{1}{2}(\pi_{11}+\pi_{12})+0.382683\pi_{44}$
$\frac{\pi}{4}$	$\frac{1}{2}(\pi_{11}+\pi_{12})$	$\frac{1}{2}(\pi_{11}+\pi_{12})$
$-\frac{\pi}{4}$	$\frac{1}{2}(\pi_{11}+\pi_{12})$	$\frac{1}{2}(\pi_{11}+\pi_{12})$
$\frac{5\pi}{16}$	$0.617317\pi_{11}+0.691342\pi_{12}$	$\frac{1}{2}(\pi_{11}+\pi_{12}-0.382683\pi_{44})$
$\frac{3\pi}{8}$	$0.146447\pi_{11}+0.853553\pi_{12}$	$\frac{1}{2}(\pi_{11}+\pi_{12})-0.351077\pi_{44}$
$\frac{7\pi}{16}$	$0.038060\pi_{11}+0.961940\pi_{12}$	$\frac{1}{2}(\pi_{11}+\pi_{12})-0.923880\pi_{44}$
$\frac{\pi}{2}$	π_{12}	$\frac{1}{2}(\pi_{11}+\pi_{12}-\pi_{44})$
H $\frac{\pi}{4}$		$\frac{1}{2}\pi_{44}$
H 0	$\pi_{44}\sigma_{12}$	

Table 3.4: The linear combination of the piezocoefficients in silicon in each resistor according to Eq. (2.25) on page 25, when the chip is stressed along the [100] and the [110] direction, respectively. θ' is the resistor orientation angle with respect to the stress direction. The two last rows are the equations used for "Hall type" resistors. Notice that R_H of the resistor in the last row is not proportional to the σ_{11} stress but the shear stress σ_{12}. The nanowire resistors are all stressed along [110] and the resistors are directed parallel to the stress direction, i.e. $\theta' = 0$.

3.5 Resistor design

The resistor designs from the chips presented in Fig. 3.9 are described below. The resistors in Fig. 3.9a-c are described first, followed by the nanowire resistors from Fig. 3.9d.

3.5.1 Standard piezoresistors

The chips in Fig. 3.9a-c contain two different resistor layouts. One resistor enables a four terminal measurement of the voltage drop parallel to the current density vector and another resistor is designed for four terminal measurement of the voltage drop perpendicular to the current density vector, i.e. the “Hall type" resistor. The two designs are illustrated in Fig. 3.10a-b and the dimensions are listed in Table 3.5. The length to width ratio of the longitudinal resistor is 20 for low doped resistors and 80 for high doped resistors to keep the resistance of these resistors in the kΩ range for all doping concentrations. There are two noise sources that are expected to contribute to the noise in the piezoresistors [22]. Firstly, the $1/f$ noise $< v_f >$, which normally is the largest noise source in piezoresistors, described by

$$< v_f^2 >= \int_{f_{min}}^{f_{max}} \frac{\alpha V_s^2}{fN} df \;\Rightarrow\; < v_f >= \sqrt{\frac{\alpha V_s^2}{N} \ln\left(\frac{f_{max}}{f_{min}}\right)}, \tag{3.14}$$

where N is the number of carriers in the resistor, i.e. $N = N_A wLh$ where L and w are shown in Fig. 3.10 and h is the height, $f_{min} = 1$ Hz to $f_{max} = 50$ Hz is the frequency range, V_s is the supply voltage, and $\alpha = 4 \cdot 10^{-6}$ is a material parameter. The value of α is experimentally determined in Ref. [22]. The other noise source is the thermal noise or Johnson noise $< v_j >$ [13] described by

$$< v_j^2 >= 4k_b TR\Delta f \Rightarrow < v_j >= \sqrt{4k_b TR\Delta f}, \tag{3.15}$$

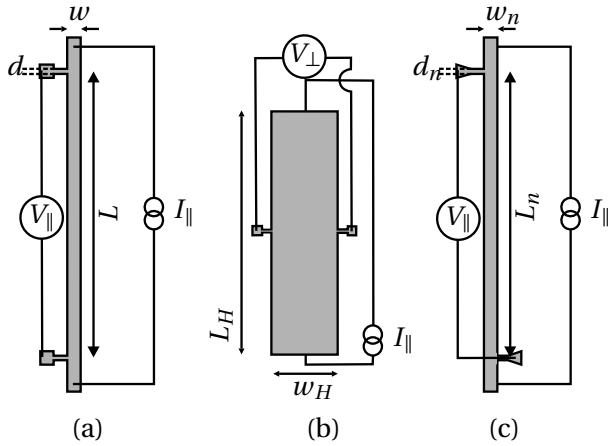


Figure 3.10: Presentation of the designs of the micrometer scale resistors used to perform high impedance voltage measurements parallel (a) and perpendicular (b) to the current density vector. The resistor dimensions are listed in Table 3.5. In the nanowire resistor design (c) the length L_n to width w_n ratio is 20 for all widths shown in Fig. 3.9d and the channel width $d_n = 40$ nm. The illustration are not to scale.

Dimension	d	w	L	w_H	L_H
Low doped resistor	5 μm	25 μm	500 μm	140 μm	320 μm
High doped resistor	5 μm	20 μm	800 μm	140 μm	320 μm

Table 3.5: Dimensions of the two resistors illustrated in Fig. 3.10a-b.

N_A [cm^{-3}]	ρ [Ωcm]	w [μm]	L [μm]	h [μm]	R [kΩ]	I [μA]	V [V]	ΔV [mV]	$< v_j >$ [μV]	$< v_f >$ [nV]
$1.5 \cdot 10^{17}$	0.15	25	500	1	30	20	0.6	12	0.15	0.05
$1 \cdot 10^{20}$	0.0012	20	1800	1	0.9	100	0.1	2	0.03	0.0002

Table 3.6: Calculated Johnson, $< v_j >$, and $1/f$, $< v_f >$, noise contributions for two p-type piezoresistors. The shown doping concentrations represents the minimum and maximum doping concentration. The resistivity is found from the doping concentration using Ref. [57]. The magnitude of the current I in the resistor ensures that there is no significantly self-heating in the resistor, according to App. H. In order to calculate the change in voltage drop ΔV it is assumed that the relative resistance change in the resistor is $\frac{\Delta R}{R} = 2\%$. The contributions from the two noise sources do not change the signal significantly.

where T is the temperature, R is the resistance, and $\Delta f = 50$ Hz is the bandwidth of the signal. The calculated noise signals in the resistors are shown in Table 3.6 for the highest and lowest resistance values. The maximum current allowed in the resistor is found by investigating the self-heating in the resistor. The calculation is included in App. H. Since the supply voltage is low the $1/f$ noise is smaller than the Johnson noise for both resistors. The noise does not contribute significantly to the measured signal.

The contact channel width d in Fig. 3.10a-b is to be as small as possible with respect to the width of the resistor in order to lower the influence of the extra space available to the current in the

N_A [cm^{-3}]	ρ [Ωcm]	w [nm]	L [μm]	h [nm]	R [kΩ]	I [nA]	V [μV]	ΔV [μV]	$< v_j >$ [μV]	$< v_f >$ [μV]
$1.5 \cdot 10^{17}$	0.15	50	1	50	600	1.3	780	16	0.7	.016
$1.2 \cdot 10^{20}$	0.001	50	1	50	4	15	60	1.2	0.06	0.0004

Table 3.7: Calculated Johnson, $< v_j >$, and $1/f$, $< v_f >$, noise contributions for two nanowire resistors. The resistivity is found from the expected minimum and maximum doping concentration in the nanowires using Ref. [57]. The magnitude of the current I in the nanowire is the maximum allowed current in order to ensure that there is no significantly self-heating (below 0.01°C) in the resistor according to FEM. In order to calculate the change in the voltage drop ΔV it is assumed that the relative resistance change in the resistor is $\frac{\Delta R}{R} = 2\%$. The largest noise contribution is from the Johnson noise which is approximately 5% of the signal for both the low doped and the high doped nanowire.

voltage contact channel and resistor interconnection. By using the dimensions listed in Table 3.5 ($d = 5$ μm and $w = 20$ μm) FEM shows that the voltage channel results in an insignificant change in the resistance of 0.1%. The resistance in the channel is large due to its small width, however it is negligible compared to the large input impedance of the multimeter which is in the order of 10 GΩ. The distance from the current contacts to the voltage contacts is larger than the width of the resistor, thus the current is assumed to be uniformly distributed along the width of the resistor between the two voltage contacts for both resistor designs.

3.5.2 Nanowire piezoresistors

The nanowire design is shown in Fig. 3.10c. The length to width ratio is 20 for all resistors, thus the length is changed for each resistor according to the width. The nanowires have large resistances (4 kΩ-600 kΩ), thus more care needs to be taken according to self-heating of the resistor. By using the same method as in App. H but changing the dimensions of the resistor ($L = 1$ μm) and the resistance (600 kΩ) a maximum current of $I_{max} = 260$ nA is allowed. A more detailed FEM analysis, where the change in thermal conductivity as a function of nanowire width [58, 59] and the oxide layer surrounding the nanowire is included in the model, shows that the maximum current in a nanowire (with a width of 50 nm and $R = 600$ kΩ) is $I_{max} = 1.3$ nA in order to keep the self-heating below 0.01°C. Since the FEM analysis is more accurate compared to the approximate method in App. H, FEM is used to define the maximum injected currents in the nanowires. This maximum current is used to calculate the contributions from the two noise sources, Johnson noise and $1/f$ noise, described in the previous section. The contributions are listed in Table 3.7 for the nanowires with lowest and highest doping concentration, respectively. The current used is the maximum allowed current in order to keep the self-heating of the nanowire below 0.01°C according to FEM. In the two nanowires the Johnson noise is the largest noise source of approximately 5% of the expected signal, which is acceptable for the nanowire measurement. It is seen that the $1/f$ noise, as expected from Eq. (3.14), decreases when increasing the doping concentration.

3.6 Chip design

The chips are designed according to the conclusions in the previous sections. Furthermore, two characterization structures are implemented along the edges of the chip. The test structures are

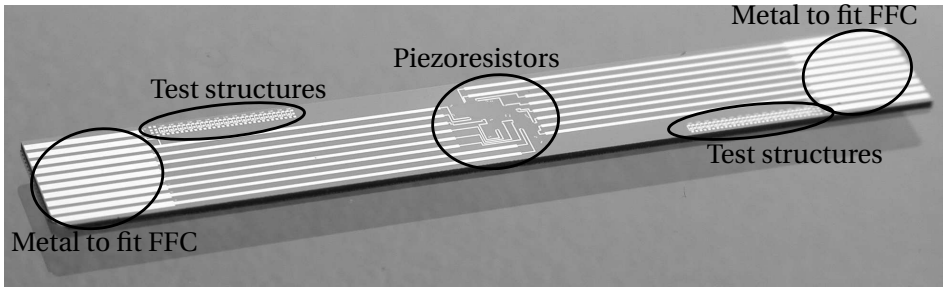


Figure 3.11: Photograph of fabricated chip. The piezoresistors are located in the center region of the chip and test structures are placed along the edges. At the two ends of the chip the metal design fits the electrical connection of FFC connectors.

van der Pauw structures used to measure the sheet resistance and 6 terminal Kelvin structures used to measure the contact resistance. Fig. 3.11 shows a fabricated chip.

For the standard piezoresistors the chips are directed along two crystal directions, i.e. the [100] and the [110] direction, respectively. In addition to this the large dimensions of the chip minimize the number of chips on one wafer. Separate chips containing test structures only are also located on the wafer. These test structures includes square areas (900×900 μm^2) for secondary ion mass spectroscopy (SIMS) measurements additionally to the test structures on the chips with piezoresistors. The full wafer layout is illustrated in Fig. 3.12. The wafer layout for the nanowire piezoresistors consists of chips directed only along the [110] direction, since the study focuses on the change in the piezocoefficent π_{44} as a function of nanowire width.

3.7 Summary

This chapter presented the design of the piezoresistive test chips for both piezoresistors in the micrometer domain and piezoresistive nanowires. By using the FFC connectors to obtain electrical connection to the chip the width (5.3 mm) and height (350 μm) of the chip were determined in order to fit into these connectors. The length of the chip (4 cm) was determined due to a compromise of a large chip length and a large number of chips on one wafer.

The piezoresistance characterization is performed by high impedance four terminal measurements. The designs of the resistors were presented and a thorough uncertainty analysis was performed in order to find the combination of resistor orientation and stress direction that results in the most accurate determination of the three piezocoefficients. This analysis proved that the chips need to be cut along two directions:

[100] in order to determine π_{11} and π_{12} with resistors oriented along [100] and [010], respectively.

[110] in order to determine π_{44} with resistors oriented along [110] and [$\bar{1}$10].

The chips containing the silicon nanowires are cut only along the [110] direction and contains nanowires directed only along the [110] direction, since the study focuses on the change of π_{44} as a function of nanowire width.

The next section presents the fabrication of the chips.

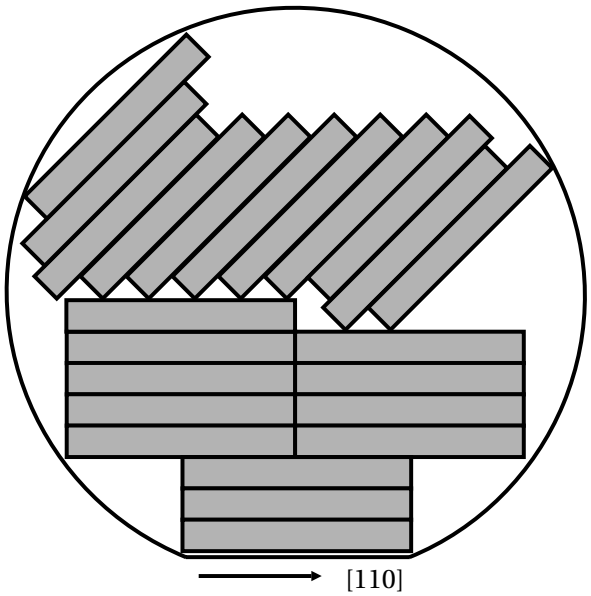


Figure 3.12: Illustration of wafer layout. The chips are directed along two crystal directions, i.e. the [100] and the [110] crystal direction. The rotation of the chips puts a limit to the number of chips on one wafer. Isolated chips including test structures only (for sheet resistance, contact resistance and SIMS characterization) are also located on the wafer. The wafer layout for the nanowire piezoresistors include chips directed along the [110] direction only. The illustration is not to scale.

CHAPTER

4 Chip fabrication

The chip fabrication process is aimed at being as simple as possible but at the same time as flexible as possible. Simplicity is a keyword when planning the process flow. The simpler the process sequence is, the larger the chance of successful fabrication. The majority of the samples characterized in this thesis are fabricated as parts of student projects. This emphasizes the importance of a simple and straightforward fabrication process in order to optimize the process yield. Since the piezoresistance characterization concerns several different materials the process sequence should allow for change of materials and allow for process modifications to enable addition of process steps where needed.

In order to satisfy the need for simplicity and flexibility a general fabrication process has been developed. From this general fabrication process it is possible to add and change fabrication steps when needed. An example of a fabricated chip is shown in Fig. 4.1.

Four different fabrication processes are needed in order to fabricate four different batches. These four fabrication processes all follow the same general process outline but includes dedicated process steps. The four different batches are

- Molecular beam epitaxial (MBE) growth of strained Si and $Si_{0.9}Ge_{0.1}$ piezoresistors.
- Ion implanted silicon piezoresistors.
- Uniformly doped silicon piezoresistors.
- Crystalline and polycrystalline silicon nanowire piezoresistors.

This chapter gives an overview of the general process fabrication scheme and detailed description of important process steps. This is followed by a brief process description of each of the four batches. In these sections only the difference from the general process scheme is described.

4.1 General process

The major process steps in the general process sequence are shown in Fig. 4.2. The general process sequence fits the sequence of a highly doped MBE grown piezoresistor.

The overall process flow can be summarized in the following main processes

- Anisotropic etch in order to determine the crystal orientation.
- Ion implantation in order to obtain an ohmic contact to the substrate.

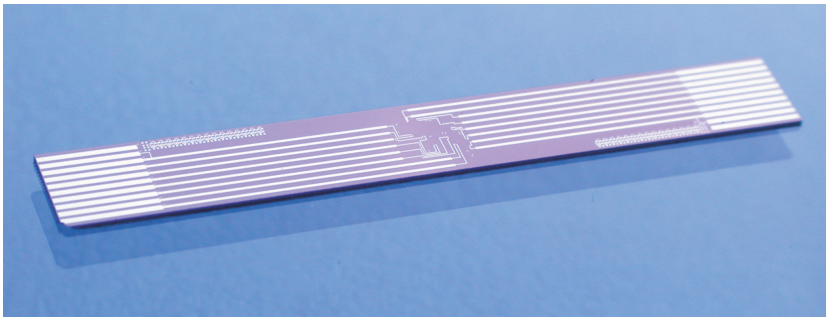


Figure 4.1: Photograph of fabricated chip. This chip contains compressively strained $Si_{0.9}Ge_{0.1}$ piezoresistors grown by MBE on a silicon substrate.

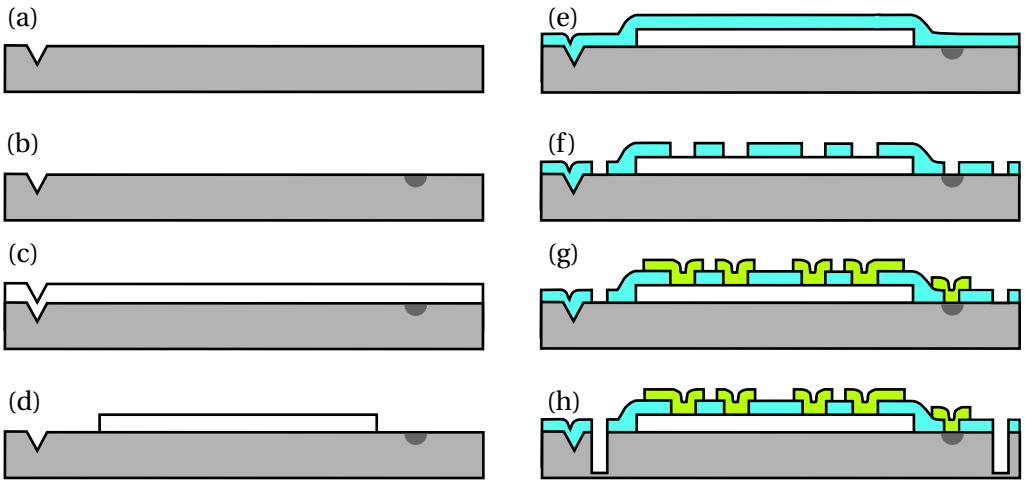


Figure 4.2: Schematic of the general process sequence. The process sequence illustrates the fabrication scheme of a highly doped MBE grown piezoresistor. (a) An anisotropic KOH etch is used to determine the crystal orientation of the substrate (grey). (b) Ion implantation of substrate contact (dark grey) followed by a recrystallization. In the processes where the piezoresistors are made by ion implantation this step is included in step (f). (c) An MBE layer (white) is grown on top of the substrate. In the processes where the piezoresistors are made by ion implantation, this MBE growth is exchanged by an ion implantation of the whole wafer surface. (d) The resistors are defined by RIE. (e) An oxide (blue) is deposited on top of the structures for isolation, and (f) contact holes are etched with the use of BHF. (g) Metal (green) is evaporated and patterned in a lift off process, and finally (h) the chips are diced using DRIE.

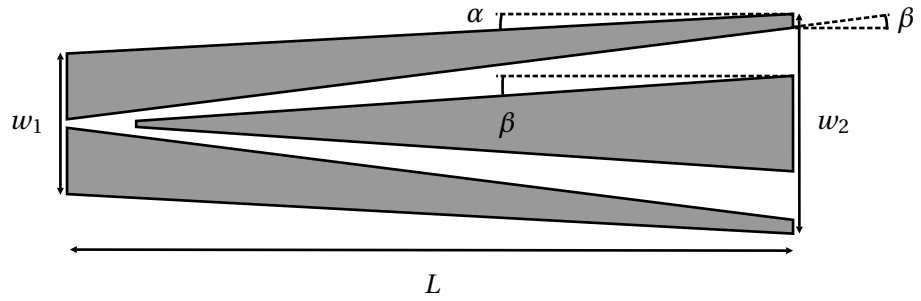


Figure 4.3: Illustration of crystal alignment structure. The structure is symmetric in the center horizontal plane. Dimensions of the structure are $L = 700$ μm, $w_1 = 89.62$ μm, $w_2 = 98.62$ μm, $\alpha = 1.5°$, and $\beta = 3.5°$.

- Implantation or MBE growth of in situ doped piezoresistor layer on the whole wafer surface.
- Reactive ion etch (RIE) in order to define piezoresistor pattern.
- Thermal oxidation or plasma enhanced chemical vapor deposition (PECVD) of oxide in order to isolate the piezoresistors.
- Buffered HF (BHF) in order to open oxide windows for contacts.
- Deposition and anneal of a Ti/Al metal layer in order to obtain proper electrical contact to the piezoresistor.
- Deep RIE (DRIE) in order to dice the chips.

Below, the important processes are described in detail.

4.1.1 Crystal alignment

The first process is the determination of the exact crystal direction. The wafers are guaranteed a crystal alignment to the wafer flat of ±2° to the [110] direction. A 2° misalignment of the resistor and stress direction can result in large uncertainties as explained in Sec. 3.3.1, thus a preliminary step is performed in order to the determine the crystal direction with an uncertainty of ±0.1°.

Inspired by Ref. [60] the crystal direction is found by exposing specifically designed structures on the silicon surface to an anisotropic KOH etch. The KOH etch rate along the {111} planes is significantly smaller than for the {100} and {110} planes [61] and this is exploited in the crystal alignment process. The alignment structure shown in Fig. 4.3 is etched by BHF in a 500 nm thermal oxide on top of the (001) Si substrate. After being exposed to KOH (80°C) in 13 min 30 s. (the experienced etch rate is listed in Table 4.1) the pattern of the etched structure depends on the rotation of the structure with respect to the [110] direction. An *ACES* (etching simulation computer software [62]) simulation is performed in Fig. 4.4 where a perfectly aligned structure and a 1.5° misaligned structure with respect to the [110] direction is exposed to KOH. The structures are inspected visually for two effects caused by crystal misalignment. The first effect is the union of tip and sidewalls on one side of the structure (1 in Fig. 4.4b). The second effect is an asymmetric etch of the upper and lower parts resulting in a difference of how much the (001) plane is etched. This is seen by a difference in the placement of where the sidewalls of each part meet (2 in Fig. 4.4b). The crystal orientation alignment mask contains an array of the structure in Fig. 4.3 in both sides of the

Etchant	Material	Etch rate	Mask
KOH	Si, [110] direction	1.3 μm	500 nm Thermal SiO_2
RIE	Si and $Si_{1-x}Ge_x$	300 nm/min	1.5 μm resist
BHF	PECVD SiO_2	1100 Å/min	2.2 μm resist
BHF	LPCVD (TEOS) SiO_2	1000 Å/min	2.2 μm resist
BHF	Thermal SiO_2	700 Å/min	2.2 μm resist
ASE	Si	6 μm/min	9.5 μm resist

Table 4.1: Etch rates experienced during processing.

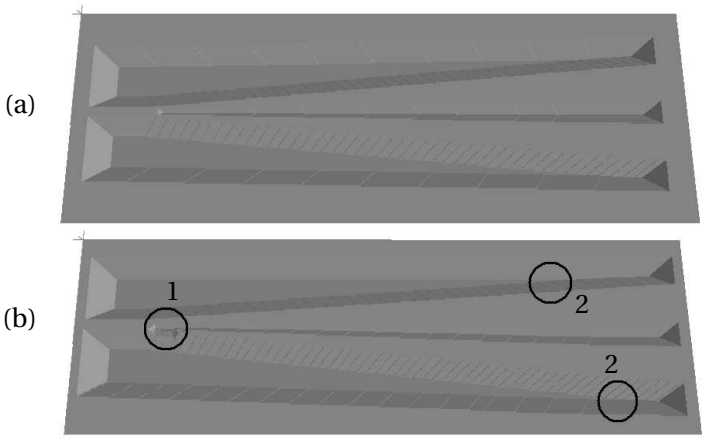


Figure 4.4: *ACES* [62] simulation of crystal alignment structures on a (001) silicon substrate exposed to KOH. (a) A perfect aligned structure to the [110] direction. (b) A 1.5° misaligned structure to the [110] direction. The misalignment can be seen by two effects, (1) the union of tip and sidewall of the lower or upper part, (2) the asymmetry of the two (001) planes created by the etch of the upper and lower parts.

mask. The arrays consist of 40 structures each rotated 0.1° with respect to each other. Each rotated structure includes an alignment mark to be used for the next mask. The 40 structures covers a misalignment of ±2°. The mask is aligned to the wafer flat (the crystal alignment to the [110] flat specification is ±2° guaranteed by the wafer supplier).

Fig. 4.5 shows the etched structures. Both effects are visualized in the structures and it is possible to determine the crystal direction with an uncertainty of ±0.1°. The best aligned structure is marked with 1. The sequence for the KOH crystal alignment process is included in App. I.1.

4.1.2 RIE of piezoresistors

The piezoresistors are defined by reactive ion etch (RIE) in an STS Cluster System C010 SF_6 (32 sccm) and O_2 (8 sccm) plasma with an RF power of 30W (pressure = 80 mTorr). A 1.5 μm photoresist is used as masking layer for the approximately 500 nm silicon etch. The experienced etch rate is listed in Table 4.1.

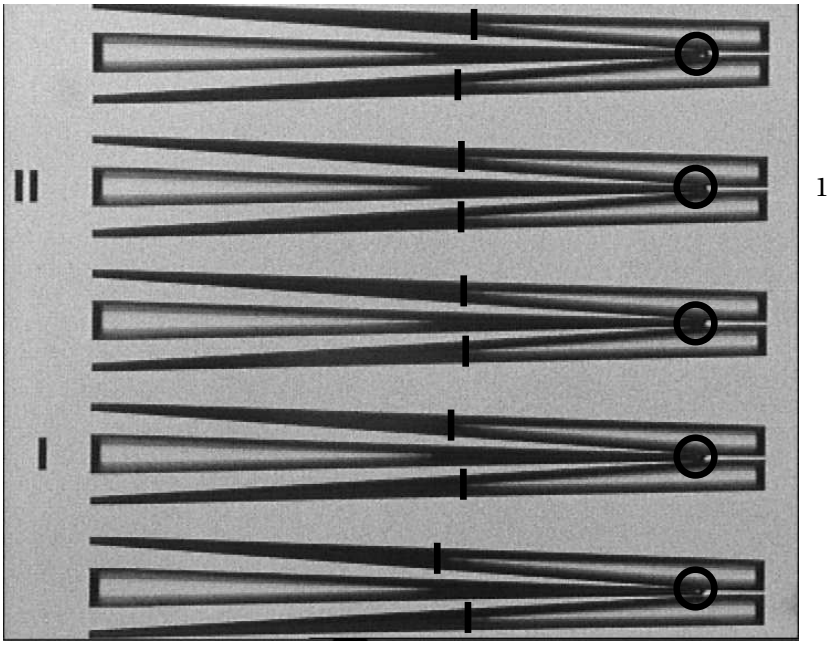


Figure 4.5: Optical image of the crystal alignment structures after being exposed to KOH. The red lines and circles indicate how to inspect the structures. The best aligned structure is marked with 1.

4.1.3 Metal deposition

The metal is deposited in a lift off process with a negative 2.2 μm photoresist as a masking layer. To cover the edges from the RIE of approximately 500 nm the metal layer has a thickness of 700 nm. The metal combination aluminum (600 nm) on titanium (100 nm) has proven to create good ohmic contacts, thus this metal combination is used for all processes. The metal is sputtered by e-beam evaporation in an Alcatel SCM 600 E-beam metal deposition system. After deposition the metal is annealed at $T = 450°C$ for 15 min.

4.1.4 DRIE chip isolation

The outer dimensions of the chips are defined using DRIE. Since the chips are directed along different crystal orientations on a wafer, see Fig. 3.12 on page 46, the use of a saw is a time consuming process and it has shown to decrease the yield significantly on the chips directed along the [100] direction. Furthermore, the use of a photolithographic mask gives a more precise definition of the crystallographic direction of the chip. The DRIE process is performed in an STS MESC Multiplex ICP cluster in an SF_6 (230 sccm) and O_2 (23 sccm) plasma with passivation(etch) cycles of 8(5) seconds. A 9.5 μm photoresist is used as masking layer. The etch rate is listed in Table 4.1. This etch creates trenches to define the chips. The trenches are not etched completely to the backside since the etch is stopped when a trench layer thickness of approximately 50 μm is reached. With this thickness it is possible to break the chips apart after leaving the cleanroom. If the trench thickness is larger than 80 μm the yield is decreased significantly, since it is then very difficult to break the chips along the correct directions.

Material	ε	N_A	t
Si	0	$1.6 \cdot 10^{18}$ cm^{-3}	200 nm
Si	0	$3 \cdot 10^{18}$ cm^{-3}	200 nm
Si	0	$1.7 \cdot 10^{19}$ cm^{-3}	200 nm
Si	0.002	$3 \cdot 10^{18}$ cm^{-3}	200 nm
Si	0.004	$3 \cdot 10^{18}$ cm^{-3}	200 nm
$Si_{0.9}Ge_{0.1}$	-0.004	$1.6 \cdot 10^{18}$ cm^{-3}	200 nm
$Si_{0.9}Ge_{0.1}$	-0.004	$1.7 \cdot 10^{19}$ cm^{-3}	200 nm

Table 4.2: Specifications of the MBE grown materials, strain, ε, boron doping concentration, N_A, and layer thickness, t.

4.2 Individual batch processes

This section includes brief summaries of the fabrication processes of each batch. The main focus is on the added processes and/or the modifications to the general process sequence described above.

4.2.1 Strained MBE piezoresistors

The strained crystal piezoresistors are grown by MBE and in-situ doped with boron. Table 4.2 lists the materials. For strained MBE piezoresistors with $N_A \approx 10^{18}$ cm^{-3} a process step is added before the RIE. In order to obtain a proper electrical contact to the resistor a thin, highly doped layer is grown on top of the piezoresistor layer. The contact areas are defined by etching the highly doped layer to obtain isolated areas of highly doped material in the contact regions. These contacts are not ion implanted since the strained MBE layers are not stable at high temperatures ($T > 800$°C) which is needed in order to activate the dopants. After the etch of the thin highly doped layer the piezoresistors are patterned (Fig. 4.2d) and the process follows the general process in Fig. 4.2. A PECVD oxide is used for isolation between piezoresistor and metal paths in order to keep the temperature budget low. Relaxation of the strained piezoresistor can also be caused by the thickness exceeding the critical thickness of the layer. The chosen thicknesses of the strained MBE layers listed in Table 4.2 ensure stability.

The full process sequence for MBE grown piezoresistors is listed in App. I.2.

4.2.1.1 MBE

The strained layers are grown in a VG80-S MBE system. The deposition temperature is 500°C with a rate of approximately 0.1 nm/s.

Before the actual growth of the strained layers a spacer layer is grown on top of the substrate. This spacer layer is 50 nm thick and lightly n-doped. Defects are present at the interface of the MBE layer and substrate. By growing a spacer layer, these defects are present near the spacer and substrate interface, and are thus not influencing the actual piezoresistive layer.

The compressively strained $Si_{0.9}Ge_{0.1}$ layers are grown by e-beam evaporation of silicon and germanium sources on to the spacer layer. Fig. 4.6 shows a secondary ion mass spectroscopy (SIMS) of the doping concentration profile and germanium content of the piezoresistor. By comparing the boron and silicon dioxide intensities to the intensities from a calibrated sample with a

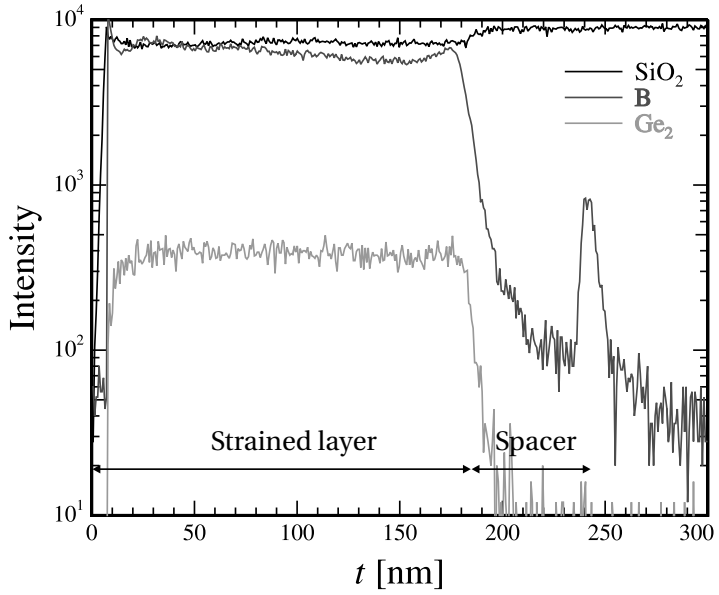


Figure 4.6: SIMS measurement of a wafer containing a strained $Si_{0.9}Ge_{0.1}$ layer with a doping concentration of $N_A = 1.7 \cdot 10^{19}$ cm^{-3}. Intensities of Ge_2 (green), B (red), and SiO_2 (black) are shown as functions of approximate thickness t. The boron doping concentration is found by comparing the intensities with the intensity data from a sample with known boron doping concentration. The MBE layer is approximately 179 nm thick. The interface between the spacer and the substrate is seen at the boron peak. The spacer is approximately 61 nm thick.

known boron concentration the boron concentration in the sample is found. The in-situ doping of boron ensures an almost uniform doping concentration in the resistor.

The tensile strained Si layers are grown on top of relaxed $Si_{0.95}Ge_{0.05}$ and $Si_{0.9}Ge_{0.1}$ layers. The relaxed $Si_{1-x}Ge_x$ layer is grown on a silicon spacer by slowly increasing the amount of germanium in the silicon and germanium evaporation system. In order to obtain a relaxed $Si_{0.9}Ge_{0.1}$ layer the thickness of the layer needs to be approximately 2 μm.

The biaxial strain ϵ listed in Table 4.2 is calculated by using a first order linear relation of the lattice constants. For example, in $Si_{0.9}Ge_{0.1}$ the lattice constant $a(Si_{0.9}Ge_{0.1})$ is expected to be $a(Si_{0.9}Ge_{0.1}) = 0.9 \cdot a(Si) + 0.1 \cdot a(Ge) = 0.9 \cdot 5.43\,\text{Å} + 0.1 \cdot 5.65\,\text{Å} = 5.45\,\text{Å}$ [63]. Thus, if $Si_{0.9}Ge_{0.1}$ is grown directly on top of silicon the biaxial strain in the surface plane is

$$\epsilon = \frac{a(Si_{0.9}Ge_{0.1}) - a(Si)}{a(Si_{0.9}Ge_{0.1})} = \frac{5.45\,\text{Å} - 5.43\,\text{Å}}{5.45\,\text{Å}} = 0.004. \tag{4.1}$$

The biaxial strain is calculated in the same manner for the other materials listed in Table 4.2.

4.2.2 Gaussian doping profile piezoresistors

The fabrication process for Gaussian doping profile ion implanted piezoresistors follows the general process except an extra implantation step is added in order to obtain ohmic contacts to the piezoresistors. Thus, a total of three implantation steps are performed: Piezoresistor, piezoresistor contact, and substrate contact. For this process, the substrate contact implantation is not performed in step b in Fig. 4.2 but is to be included in step f. The piezoresistor layer is implanted

No.	Dopant	Energy	Dose	Simulation		Measurement
				$R_\square$	Peak conc. N_A or N_D	$R_\square$
i1	B	30 keV	$8\cdot10^{15}$ cm^{-2}	18 Ω/□	$4.6\cdot10^{19}$ cm^{-3}	14 Ω/□
i2	B	30 keV	$1\cdot10^{15}$ cm^{-2}	125 Ω/□	$9.4\cdot10^{18}$ cm^{-3}	140 Ω/□
i3	B	30 keV	$8\cdot10^{13}$ cm^{-2}	715 Ω/□	$9\cdot10^{17}$ cm^{-3}	795 Ω/□
i4	P	30 keV	$9\cdot10^{14}$ cm^{-2}	346 Ω/□	$5\cdot10^{18}$ cm^{-3}	275 Ω/□
i5	P	30 keV	$9\cdot10^{14}$ cm^{-2}	346 Ω/□	$5\cdot10^{18}$ cm^{-3}	279 Ω/□
i6	P	30 keV	$8\cdot10^{13}$ cm^{-2}	1250 Ω/□	$5.1\cdot10^{17}$ cm^{-3}	1035 Ω/□
i7	P	30 keV	$8\cdot10^{13}$ cm^{-2}	1250 Ω/□	$5.1\cdot10^{17}$ cm^{-3}	1047 Ω/□

Table 4.3: Ion implantation specifications for both p-type and n-type piezoresistors. Also listed are the measured sheet resistances and the expected sheet resistances and peak doping concentrations (N_A for boron doped wafers and N_D for phosphorus doped wafers) found by simulation [64]. The annealing of the wafers are included in the simulation (boron wafers: Dry thermal oxidation at T = 1100°C for 80 min., and phosphorus wafers: Dry thermal oxidation at T = 1000°C for 160 min. and N_2 atmosphere T = 1000°C for 30 min.). The process of wafer i4 (i for implantation) is the same as the process of wafer i5, which is also seen by the measured sheet resistances. This is also the case for wafer i6 and i7. The realized sheet resistances are approximately 10 – 20% lower than the sheet resistance found by the simulation.

on the whole wafer and the resistors are defined by RIE (Fig. 4.2c-d). This is followed by thermal oxidation and recrystallization. Table 4.3 shows doping specifications and expected (simulated in Silvaco Deckbuild software [64]) and measured sheet resistances. The measured sheet resistances are approximately 10 – 20% lower than what is expected in the simulation. This holds for both dopants. The extracted values from the simulation of the doping concentration is used as an approximate value of the doping concentration in the piezoresistor. The analysis is described in detail in the next section. BHF etching opens the contact holes and the piezoresistor contacts are implanted with a high dose in order to obtain an ohmic contact using the same photoresist mask for both BHF etch and implantation. After this step, the contact holes are opened to the substrate contacts and these are ion implanted. Notice, that this step is included in Fig. 4.2f. The contacts are annealed prior to metal deposition (Fig. 4.2g). The full process sequence for ion implanted piezoresistors is listed in App. I.3 and App. I.4.

4.2.2.1 Process simulation

The Silvaco Deckbuild simulation software uses SIMS verified ion implanted doping profiles to calibrate the simulation models. The ion implantation profile depends on the projected range (the total distance along the axis an ion travel before coming to rest) and straggle (the fluctuations in the projected range) of the dopant [66]. In Fig. 4.7a the simulated Gaussian implantation profiles for wafer no. i2 and i4 in Table 4.3 are plotted. The implantation is performed on a silicon wafer with a 56 nm oxide on the surface in order to avoid channelling of the ions and in order to protect the silicon surface during ion implantation. It is clearly seen that the range and straggle of the phosphorus atoms are much smaller than those of boron. The low range of the phosphorus ions causes the phosphorus peak to be outside the silicon material. This results in a large loss of the implanted dose $D = 9\cdot10^{14}$ cm^{-2} since the realized dose is $D = 1.2\cdot10^{14}$ cm^{-2} according to the simulation, whereas the boron implantation dose of $D = 1\cdot10^{15}$ cm^{-2} decreases by 10% to $D = 9\cdot10^{14}$ cm^{-2}. In future processing it is suggested that the energy of the phosphorus implantation is increased in order to increase the projected range and thus ensure that the doping peak is inside

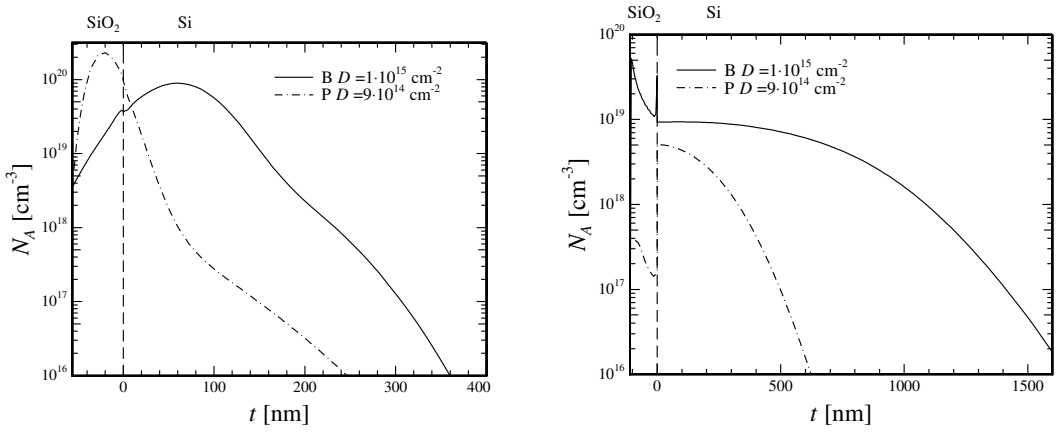


Figure 4.7: Silvaco Deckbuild [64] simulation of the doping profile near the silicon and silicon dioxide interface at $t = 0$ for wafer i2 (solid) and i4 (dashed and dotted) in Table 4.3 before annealing (a) and after annealing (b). (a) The implantation is performed with a 56 nm oxide on top of the silicon wafer. This layer is present in order to avoid channelling of the implanted ions and in order to protect the silicon surface from the ion bombardment during implantation. The range, R_p, and straggle, σ_p, of boron and phosphorus in silicon are different (boron: $R_p = 112.2$ nm and $\sigma_p = 49$ nm, phosphorus: $R_p = 42.9$ nm and $\sigma_p = 18.9$ nm at 30 keV [65]), which is seen in the doping profiles. The phosphorus peak is placed in the silicon dioxide layer. This results in a high loss of the phosphorus dose. (b) The oxide from (a) is etched and a new oxide is grown during the recrystallization process. The two wafers are annealed at different temperatures and times (boron sample: Dry thermal oxidation at $T = 1100$°C for 80 min., and phosphorus sample: Dry thermal oxidation at $T = 1000$°C for 160 min. and N_2 atmosphere $T = 1000$°C for 30 min.). The high oxidation temperature of the boron wafer and the larger straggle of boron atoms in silicon explains why boron is diffused much more than phosphorus. The large dose of boron present in the oxide compared to the amount of phosphorus is a result of the large difference in the segregation coefficients of boron and phosphorus at the silicon and silicon dioxide interface.

the silicon layer. Another suggestion is to remove the oxide or decrease the oxide thickness before implantation.

The simulated Gaussian doping profiles after an annealing step are show in Fig. 4.7b. The annealing is performed in order to recrystallize the lattice and activate the dopants while a thermal oxide is grown on the top of the wafer. In Silvaco Deckbuild the segregation across the interface of two materials that contain a dopant is modelled with a first order kinetic model of the flux near the interface of the two materials, i.e. silicon and oxide. The dopant flux from material 1 (silicon) to material 2 (oxide), F_{12} is written as

$$F_{12} = h_{12}\left(\frac{C_1}{M_{12}} - C_2\right), \tag{4.2}$$

where h_{12} is the interface transport velocity, M_{12} is the segregation coefficient from material 1 to material 2, and C_1 and C_2 are the doping concentrations in material 1 and material 2, respectively. The interface transport velocity is assumed constant and independent on temperature, $h_{12} = 1.66 \cdot 10^{-7}$ cm/s for both boron and phosphorus. However, the segregation coefficient is strongly dependent on the doping type. At a temperature of 1000°C $M_{12} = 30$ for phosphorus and $M_{12} = 0.28$ for boron [64]. Thus, the flux from the silicon material to the oxide is approximately 100

No.	Dose [cm^{-2}]	Simulation $R_\square$ [Ω/□]	Simulation N_A or N_D [cm^{-3}]	Theory $R_{\square,min}$ [Ω/□]	Theory $N_{A,max}$ or $N_{D,max}$ [cm^{-3}]	Measurement $R_\square$ [Ω/□]
u1	B $1.5\cdot10^{15}$	109	$2.2\cdot10^{19}$	72	$3.4\cdot10^{19}$	103
u2	B $1.5\cdot10^{14}$	660	$2.3\cdot10^{18}$	497	$3.4\cdot10^{18}$	462
u3	B $1.5\cdot10^{13}$	2368	$2.3\cdot10^{17}$	1788	$3.4\cdot10^{17}$	1490
u4	P $1.1\cdot10^{15}$	61	$2.5\cdot10^{19}$	61	$2.5\cdot10^{19}$	43

Table 4.4: Specifications of the uniformly doped wafers (u for uniform doping profile), all implanted with an energy of 50 keV followed by a dry thermal oxidation process at T = 1050°C for 180 min. and annealing in a nitrogen atmosphere at T = 1000°C for 30 min. in order to activate contact implantation dopants which were implanted after the dry thermal oxidation process. The measured values are compared to the simulated and theoretical minimum sheet resistance and maximum doping concentration according to Eq. (4.3) using the relation between mobility and the doping concentration from Ref. [64]. In the simulation and the calculation of the minimum sheet resistance and maximum doping concentration a resistor thickness of t = 500 nm is used. The table shows a large discrepancy between measured values and expected values, except for wafer u1 which has a measured sheet resistance which is in agreement with the simulation.

times lower if the dopant is phosphorus compared to boron. This is seen in Fig. 4.7b, where the boron concentration is much larger than the phosphorus concentration in the oxide. During the thermal oxidation the boron dose is decreased from $D = 9\cdot10^{14}$ cm^{-2} to $D = 6.8\cdot10^{14}$ cm^{-2}, whereas the phosphorus ions stays in the silicon material during thermal oxidation, i.e. $D = 1.2\cdot10^{14}$ cm^{-2}. The grown thermal oxide on the two wafers are processed with different process parameters. The thermal oxide on the boron doped wafer is grown in a T = 1100°C dry atmosphere for 80 min. and the thermal oxide on the phosphorus doped wafer is grown at T = 1000°C for 160 min. (followed by an annealing of subsequently highly doped ions at T = 1000°C for 30 min. in order to obtain ohmic contacts). The high temperature thermal oxidation (which results in a high diffusivity) of the boron implanted wafer and the larger straggle of boron results in a much broader doping profile compared to the doping profile of phosphorus.

4.2.3 Uniformly doped piezoresistors

The uniformly doped piezoresistors are fabricated on silicon on insulator (SOI) wafers. The device layer is 2 μm ±0.5 μm. The resistors are isolated from the substrate with the buried oxide layer (thickness 400 nm), thus substrate contact implantation is ignored. Due to the small thickness of the device layer the KOH crystal alignment process can not be used. Thus, step (a) in Fig. 4.2 is ignored and the masks are aligned to the wafer flat. The substrate is not used for KOH crystal alignment since the uncertainty of the device layer and substrate layer alignment is the same as the uncertainty of flat orientation which is ±2°. The device layer is thinned by oxidation thinning to a thickness of 500 nm ±500 nm in order to obtain a RIE step of approximately 500 nm that can be covered by the metallization step. The RIE is stopped by oxide end point detection in order to ensure that the device layer is etched and the resistors are isolated on the majority of the chips. Since, the thickness of the device layer varies with ±500 nm, which means that the device layer is already etched in some places on the wafer after the oxidation thinning process, the end point detection method is not that suitable. In future processing it is suggested to use wafers with a much smaller variation of the device layer thickness in order to avoid this large thickness difference. The device layer is ion implanted according to the specifications in Table 4.4. The implantation is followed

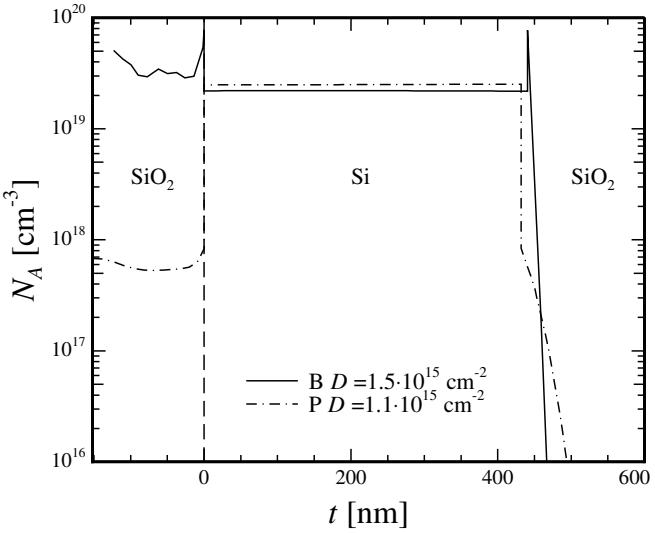


Figure 4.8: Silvaco Deckbuild [64] simulation of doping profile in the uniformly doped wafers u1 and u4 in Table 4.4. The interface between the thermal oxide and silicon is at $t = 0$. As in Fig. 4.7 a large dose of boron is present in the thermally grown oxide compared to the amount of phosphorus. The thermal oxidation process is the same for the two wafers, a dry oxidation process at $T = 1050°$C for 180 min and annealing in a nitrogen atmosphere at $T = 1000°$C for 30 min. The doses in each layer is found by integration of the doping concentration with respect to the thickness of the layer. The results are listed in Table 4.5. The diffusion tail of the dopants in the oxide on the right hand side of silicon shows that in oxide the diffusivity of phosphorus is larger than the diffusivity of boron.

		Simulated doses in layers		
No.	Dose [cm^{-2}]	SiO$_2$ [cm^{-2}]	Si [cm^{-2}]	SiO$_2$ [cm^{-2}]
u1	B $1.5 \cdot 10^{15}$	$4.6 \cdot 10^{14}$	$9.7 \cdot 10^{14}$	$7 \cdot 10^{13}$
u4	P $1.1 \cdot 10^{15}$	$9 \cdot 10^{12}$	$1.1 \cdot 10^{15}$	$1.7 \cdot 10^{12}$

Table 4.5: Simulated doses of boron and phosphorus in an oxide silicon oxide sandwich. The simulation shows that the boron doped wafers loose a large number of dopants to the surrounding oxide contrary to the phosphorus doped wafers where almost all phosphorus dopants stay in the silicon layer. This is in agreement with the discussion in Sec. 4.2.2.1. The simulation is showed in Fig. 4.8. The layers are located from the left to the right as listed in this table.

by diffusion and thermal oxidation to ensure a uniform doping concentration in the piezoresistor and to grow an oxide on top of the resistor surface. After opening of contact holes (Fig. 4.2f) the piezoresistor contacts are implanted with a high dose like the ion implanted piezoresistor contacts in Sec. 4.2.2. The full fabrication process flow of the uniformly doped piezoresistors is listed in App. I.5.

Table 4.4 compares the measured sheet resistances of the device layers to the simulated values obtained by Silvaco Deckbuild [64] and the theoretical expected values. The maximum theoretical value of the doping concentration is $N_A = \frac{D}{t}$ or $N_D = \frac{D}{t}$, where D is the dose and t is the resistor

No.	Dose [cm^{-2}]	Simulation t [μm]	Simulation $R_\square$ [$\Omega/\square$]	Simulation N_A or N_D [cm^{-3}]	Measurement $R_\square$ [$\Omega/\square$]
u2	B $1.5\cdot10^{14}$	0.6	590	$2\cdot10^{18}$	462
u3	B $1.5\cdot10^{13}$	0.8	1894	$1.5\cdot10^{17}$	1490
u4	P $1.1\cdot10^{15}$	1	56	$1.3\cdot10^{19}$	43

Table 4.6: The resistor thickness is varied in the simulation in order to reach a sheet resistance which is within a range of approximately 20% with respect to the measured sheet resistance. The simulation shows that this is reached within the expected resistor layer thickness of t = 500 nm ±500 nm, which is the thickness variation of the device layer. Thus, the resistors on the chips where the sheet resistance is measured are expected to have the thicknesses listed above and these resistors are used in the piezoresistance characterization.

thickness. That is, all dopants are located in the resistor layer. For a boron doped material the sheet resistance is then found as

$$R_\square = \frac{\rho}{t} = \frac{1}{qN_A\mu t} = \frac{1}{qD\mu}, \tag{4.3}$$

where ρ is the resistivity, q is the elementary charge, and μ is the mobility. The relation between mobility and doping concentration used in Ref. [64] is used to obtain the minimum theoretical value of $R_\square$. In the light of the discussion in Sec. 4.2.2.1 the difference in the simulated and theoretical maximum values of the boron doping concentrations in wafer u1, u2, and u3 are explained by the small value of the segregation coefficient, $M_{12} = 0.28$ at the silicon and silicon dioxide interface. For the phosphorus doped wafer u4 the simulation agrees with the maximum doping concentration value as expected from Sec. 4.2.2.1 since $M_{12} = 30$. As an example the simulated doping profiles of wafer u1 and u4 are shown in Fig. 4.8. As in Fig. 4.7b it is clear to see that a much larger number of boron ions compared to phosphorus ions are located in the surrounding oxide layers. Table 4.5 shows the simulated doses in each layer. The dose is found by integration of the doping concentration along the thickness. The table shows that in the boron doped wafer u1 the surrounding oxide contains a dose $D = (4.6+0.7)\cdot10^{14}$ cm^{-2} = $5.3\cdot10^{14}$ cm^{-2} which is approximately half of the dose in the silicon layer $D = 9.7\cdot10^{14}$ cm^{-2}. In the phosphorus doped wafer u4 there is basically no phosphorus in the surrounding oxide layers. The diffusivity of phosphorus in oxide is much larger than the diffusivity of boron in oxide $D_{\text{diff}} = 1.06\cdot10^{-16}$ cm^2/s and $D_{\text{diff}} = 3.36\cdot10^{-18}$ cm^2/s [64], respectively at T = 1000°C. This is clearly seen on the doping concentration tail in the oxide on the right hand side of silicon in Fig. 4.8.

The simulation is used to check if the expected device layer thickness of t = 500 nm is correct. For wafer u1 the measured sheet resistance is in good agreement with the simulated sheet resistance. However, the measured sheet resistances of the three other wafers are not in agreement with the simulation and the variations are not within the 20% variation which was accepted in the previous section. Since the device layer thickness varies ±500 nm the resistor thickness of t = 500 nm (which was used in Table 4.4) may not be the correct thickness. The simulations are run again changing the thickness of the silicon layer (t = 500 nm ±500 nm) in order to obtain a simulated sheet resistance in agreement with measurement (within approximately 20%). The results are shown in Table 4.6 and it is seen that the observed thickness of the resistors are within the expected values $t \leq 1$ μm. In the following chapter, the obtained doping concentrations from these simulations are the doping concentrations that are used.

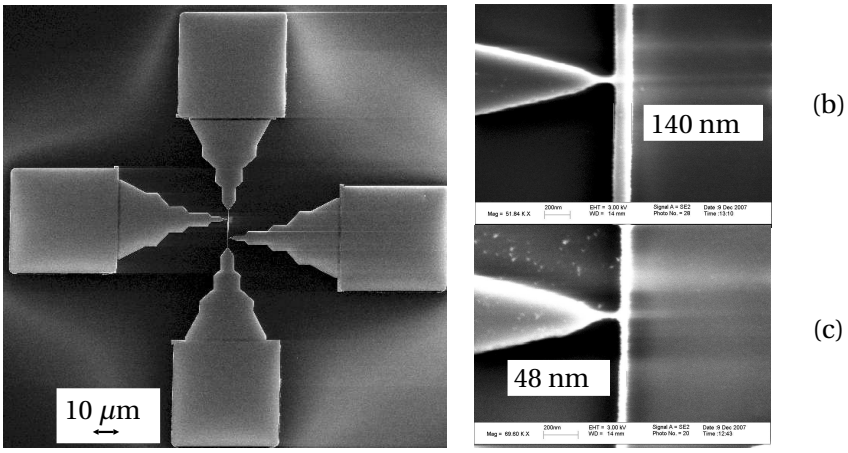


Figure 4.9: SEM image of fabricated nanowires. (a) Full image of nanowire defined by E-beam lithography and contact pads (large squares) defined by UV lithography. (b) zoom in on a 140 nm wide nanowire, and (c) zoom in on a 48 nm wide nanowire.

4.2.4 Si nanowire piezoresistors

The crystalline silicon nanowires are fabricated on SOI wafers with a device layer thickness of 340 nm ±40 nm. The wafers have a thickness of 540 μm. In order to comply with the dimensions of the FFC connectors the first step is to thin the wafers to a thickness of 350 μm. This is done in a KOH etch from the backside with a protecting PECVD nitride layer on the top of the device layer. The substrate contact and the KOH crystal alignment processes are ignored as argued in Sec. 4.2.3.

The polycrystalline silicon nanowires are fabricated in a low pressure chemical vapor deposition (LPCVD) of polysilicon (deposited at 620°C) and in-situ doped with boron on a 1000 nm oxide layer. The crystalline Si nanowire piezoresistors are doped by ion implantation of the device layer (Fig. 4.2c) (Energy 50 keV, and doses $D = 1 \cdot 10^{13}$ cm^{-2} and $D = 1 \cdot 10^{16}$ cm^{-2}). The measured sheet resistances after processing of the resistor layer with these two doses gives doping concentrations of $N_A = 1.5 \cdot 10^{17}$ cm^{-3} and $N_A = 1.2 \cdot 10^{20}$ cm^{-3}, respectively when calculating the resistivity of the layer and using the relation between resistivity and doping concentration in Ref. [57]. The nanowires have shown not to withstand an annealing at $T = 1000$°C. The nanowires broke and disappeared from the oxide surface due to stresses and poor adhesion during annealing. Thus, the piezoresistor contact implantation (for the lowed doped wafers) and annealing of both piezoresistor and contact dopants are pushed forward in the process sequence and are performed prior to the RIE.

In order to minimize the e-beam writing processing time the large test structures and contact areas are defined by UV lithography. Thus, the first step is a UV lithography step where the structures are defined in a 10 nm /60 nm e-beam evaporated Ti/Au lift off process. The nanowire structures are defined with a JEOL JBX9300FS E-beam writer in the positive resist ZEP520A (thickness 150 nm) at a dose of 250μC/cm^2, current $I = 0.2$ nA, and acceleration voltage $E = 100$ keV. This is followed by a second Ti/Au lift off. The metal layer is used as masking layer for the RIE process which isolates the nanowires (Fig. 4.2d). The gold and titanium layers are subsequently removed by potassium iodide and an amoniahydroxide/hydrogenperoxide solution, respectively. Fig. 4.9

shows SEM images of the processed nanowires. The oxide in Fig. 4.2e consists of a thin dry oxide and a 140 nm tetraethoxysilane (TEOS) oxide. The thermal oxidation step is also used to thin the nanowires in both width and thickness by controlled oxidation followed by an oxide etch in BHF.

The full process sequence for silicon nanowires is listed in App. I.6.

4.3 Summary

This section described the general fabrication process of the chips with piezoresistors located on the surface. The piezoresistor layer consists of one of these four layers:

- Compressive $Si_{1-x}Ge_x$ and tensile strained Si.
- Gaussian doping profile ion implanted silicon piezoresistors.
- Uniformly doped silicon piezoresistors.
- Crystalline and polycrystalline silicon nanowires.

The important process steps, such as a developed crystal alignment process, RIE, metal lift-off, and isolation of chips using DRIE were described in detail. Furthermore, the differences in the fabrication processes from the general process were outlined for each type of piezoresistor layer. The complete fabrication processes are shown in App. I.

The results from the piezoresistive characterization of the fabricated chips are presented in the next section.

CHAPTER

5 Results

This chapter presents the major results of the piezoresistance measurements. A brief description of the actual measurement method is presented, followed by a graphical presentation of the measurement results, which are all listed in tabular form in App. J. The section includes results of:

- p-type silicon. The results of boron doped p-type silicon contain both characterization on piezoresistors with a Gaussian doping profile and on piezoresistors with a uniform doping profile.
- n-type silicon. The piezoresistance in phosphorus doped n-type silicon is characterized on piezoresistors with a Gaussian doping profile and on piezoresistors with a uniform doping concentration.
- Tensile strained p-type silicon and compressive strained p-type $Si_{0.9}Ge_{0.1}$. The strained crystal layers are in-situ doped during growth of the layer and contains uniform boron doping profiles.
- Crystalline and polycrystalline p-type silicon nanowires. The characterization of the piezoresistance in silicon nanowires is performed on uniformly doped piezoresistors.

This chapter is to be read as a summary of the results obtained in this thesis, and it includes both published and unpublished results. The results of the investigation of π_{44} in uniformly doped p-type silicon are included in App. B.1 (*p-type silicon revisited*) as a part of the paper describing the theoretical model of the piezoresistance in p-type silicon. The measurements of π_{66} in strained p-type $Si_{0.9}Ge_{0.1}$ and strained p-type silicon are included in App. B.3 (*Piezoresistance of silicon and strained $Si_{0.9}Ge_{0.1}$*) and [67]. The results of the investigation of π_{44} in p-type silicon nanowires are included in Ref. [68]. The experimental setup used in order to obtain these results is thoroughly described in App. B.2 (*Four point bending setup for characterization of semiconductor piezoresistance*).

The first section of this chapter describes the measurement method by showing how the piezocoefficient π_{44} in p-type silicon is measured. After this description, the results are presented.

5.1 Measurement methodology

This section gives an example of how the piezocoefficient π_{44} in uniformly doped p-type silicon is determined. The doping concentration of the piezoresistor is $N_A = 2.2 \cdot 10^{19}$ cm^{-3}. A chip which

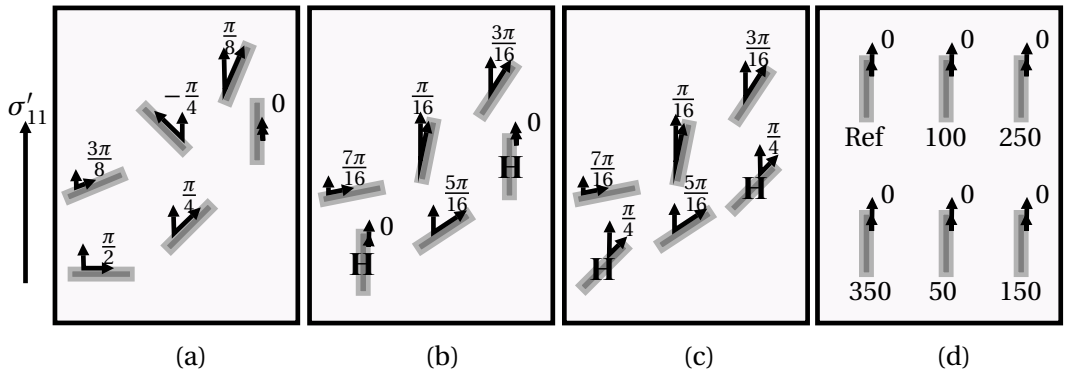


Figure 5.1: Illustration of chip design. For convenience, this figure is a copy of Fig. 3.9 on page 41 since it is referred to several times in this chapter. For design (a) the length direction of the chip is cut along the [100] direction and the [110] direction. For design (b) and (c) the chip is cut along [100] and [110], respectively. These designs consists of resistors that are directed along different angles with respect to the stress direction and is used for piezoresistance analysis of silicon, strained silicon and strained $Si_{1-x}Ge_x$. Design (d) is cut along the [110] direction and consists of five nanowire resistors of different widths (50 nm - 350 nm) and a reference micrometer scale resistor of width 25 μm (Ref). The resistors are all directed along the [110] direction and are used to analyze the piezoresistance in silicon nanowires as a function of nanowire width.

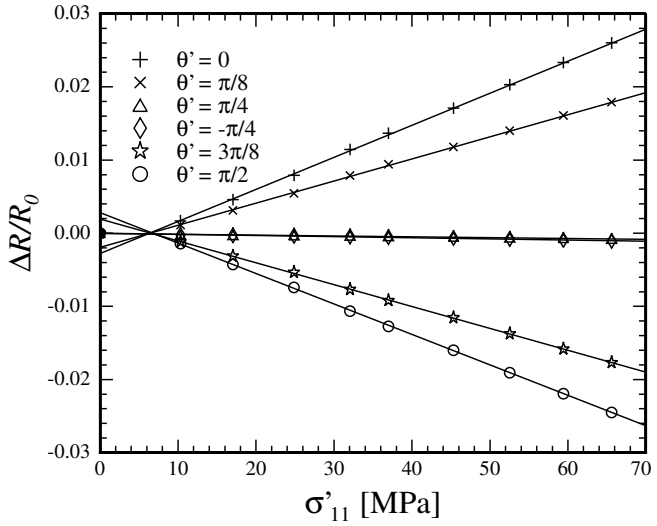


Figure 5.2: The relative change in resistance $\frac{\Delta R}{R}$ for the resistors in Fig. 5.1a as a function of the stress σ'_{11}, which is applied along the [110] direction. θ' is the angle between the resistor direction and the [110] stress direction. The piezoresistors are uniformly doped with a boron doping concentration of $N_A = 2.2 \cdot 10^{19}$ cm^{-3} and the chip is from wafer u1 in Table 4.4 on page 56. The relative resistance change is directly proportional to the applied stress and the slope of the linear fits (solid lines) are used to extract the piezocoefficient π_{44} according to Eq. (5.1). The interception of the linear fits with the σ'_{11} axis is due to a frictional force in the setup, which does not contribute to the slope of the fit.

is cut along [110] is inserted into the 4PB fixture and the fixture applies a uniaxial stress σ'_{11} along the chip, i.e. the [110] direction. The stress is applied by an actuator and a force sensor measures the force applied to the chip via the blades of the 4PB fixture. The stress in the chip is directly proportional to the force and the applied stress is calculated from the measured force. According to Eq. (2.31) on page 27 the relative resistance change $\frac{\Delta R}{R}$ in the piezoresistor depends on the applied stress in the following manner

$$\frac{\Delta R}{R_0} = \frac{1}{2}[\pi_{11} + \pi_{12} + \cos(2\theta')\pi_{44}]\sigma'_{11}, \tag{5.1}$$

where θ' is defined as the angle between the resistor direction and the [110] stress direction (in Sec. 2.3.2 θ is described with respect to the [100] direction). The chip design in Fig. 5.1a is used in this example. Fig. 5.2 shows the measured relative change in resistance of the six resistors as a function of the applied stress. The slopes of the linear fits to the data are used to extract the piezocoefficients. The interception of the linear fits with the σ'_{11} axis is due to a frictional force in the setup. This frictional force does not contribute to the slope of the linear fit. This is discussed in further detail in App. B.2. The relative resistance measurements of the resistors where $\theta' = 0$ and $\theta' = \frac{\pi}{2}$ are used to extract π_{44} since Sec. 3.3.1 concluded that at these resistor orientations π_{44} is found with the smallest uncertainty. The relative resistance measurements of the other resistors shown in Fig. 5.2 do behave according to the theory in Eq. (5.1). According to Eq. (2.32) on page 27, π_{44} can be found as

$$\pi_{44} = \frac{\Delta R}{R_0 \cdot \sigma'_{11}}\left(\theta' = 0\right) - \frac{\Delta R}{R_0 \cdot \sigma'_{11}}\left(\theta' = \frac{\pi}{2}\right) = [43.8 - (-41.6)] \cdot 10^{-11}\ \text{Pa}^{-1} = 85 \cdot 10^{-11}\ \text{Pa}^{-1}. \tag{5.2}$$

where $\frac{\Delta R}{R_0 \cdot \sigma'_{11}}\left(\theta'\right)$ is the slope of the linear fit to the data in Fig. 5.2 for the resistor directed the angle θ' with respect to the [110] stress direction.

The results presented in this chapter have all been obtained by using the above procedure. The piezocoefficient π_{44} is determined by measurements on chips cut along the [110] direction. The resistors used for this analysis are either the two resistors described above in Eq. (5.2) or one "Hall type" resistor described in Sec. 2.4.2.1 where

$$\pi_{44} = 2\frac{R_H}{R_\square \cdot \sigma'_{11}}\left(\theta' = \frac{\pi}{4}\right), \tag{5.3}$$

when using the chip design presented in Fig. 5.1c. The piezocoefficients π_{11} and π_{12} are determined by measurements on chips cut along the [100] direction. According to Eq. (2.28) on page 26

$$\begin{aligned} \pi_{11} &= \frac{\Delta R}{R_0 \cdot \sigma_{11}}\ (\theta = 0) \\ \pi_{12} &= \frac{\Delta R}{R_0 \cdot \sigma_{11}}\left(\theta = \frac{\pi}{2}\right), \end{aligned} \tag{5.4}$$

where the chip design in Fig. 5.1a is used for both measurements and σ_{11} is the applied stress along the [100] direction, and θ is the resistor orientation with respect to the [100] direction.

The uncertainties on the measurements of the three piezocoefficients were derived in Sec. 3.3 and are listed in Table 3.3 on page 41 for both n-type and p-type silicon. The following sections presents the results of the piezoresistance measurements. First, the piezoresistance results of p-type and n-type silicon is presented. This is followed by the piezoresistance results of tensile strained Si and compressive strained $Si_{0.9}Ge_{0.1}$, and finally the piezoresistance results of the silicon nanowires are presented.

5.2 *p*-type Silicon

The measurements on p-type silicon piezoresistors focus on the extraction of π_{44}. The two other piezocoefficients π_{11} and π_{12} are not of technological relevance due to their much smaller values compared to π_{44}. In Sec. 3.3.4 it was shown that these two coefficients could in principle be found with an uncertainty of 5% and 30%, respectively. However, experimental experience has shown that there are some issues that need to be considered and that the values of these coefficients can not be determined with a satisfactory uncertainty. Thus, this section is split into two parts, where one part discusses the measurements of π_{11} and π_{12} and one part concentrates on the extraction of π_{44}.

5.2.1 π_{11} and π_{12}

In order to determine π_{11} and π_{12} the chip design in Fig. 5.1a is used and the chip is cut along the [100] direction. In the derivation in Sec. 2.3.2 the relative resistance change was assumed to be a function of only the change in resistivity and not depending on geometrical changes. This is correct in silicon in most cases since this resistivity change is normally much larger than the contribution from the geometrical change. However in p-type silicon, if π_{44} is not contributing to the resistivity, the relative resistance change depends on both the contribution from the relative resistivity change $\frac{\Delta\rho}{\rho}$ and on the contribution from geometrical changes $(1+2\nu)\epsilon_L$, where ν is Poisson's ratio and ϵ_L is the strain in the direction of the chip. The relative resistance change $\frac{\Delta R}{R}$ is then

$$\frac{\Delta R}{R} = \frac{\Delta\rho}{\rho} + (1+2\nu)\epsilon_L. \tag{5.5}$$

If, for example a stress σ_{11} is applied along the [100] direction to a resistor oriented along the same direction the relation between the two contributions in Eq. (5.5) is

$$\frac{\frac{\Delta\rho}{\rho}}{(1+2\nu)\epsilon_L} = \frac{\pi_{11}\sigma_{11}}{(1+2\nu)\frac{\sigma_{11}}{Y}} = \frac{\pi_{11}Y}{(1+2\nu)} = \frac{6.6\cdot10^{-11}\cdot130\cdot10^{9}}{1+2\cdot0.28} = 5.5, \tag{5.6}$$

where Young's modulus, Y, and ν are taken from Ref. [52] and π_{11} is taken from Ref. [21]. It is seen that the resistive contribution is approximately a factor of five larger than the contribution from the geometry changes and thus the geometry changes are not negligible. Naturally, the ratio of the two contributions is even worse for the piezocoefficient π_{12} which according to Ref. [21] is 6 times smaller than π_{11} resulting in approximately even contributions to the relative resistance change from geometry changes and resistivity changes.

Another contribution to an imprecise measurement of π_{11} and π_{12} is the presence of a shear stress in the chip, which is approximately 4% of the applied stress σ_{11}, as argued in detail in App. B.2. In order to visualize this, Fig. 5.3 shows measurements on p-type silicon piezoresistors oriented according to Fig. 5.1a and stressed along the [100] direction. The polar plot contains measurements from five resistors in the design, where the effective piezocoefficient π_{eff} is defined according to Eq. (2.27) on page 26

$$\pi_{\text{eff}} = \frac{1}{2}[\pi_{11} + \cos(2\theta)(\pi_{11}-\pi_{12}) + \pi_{12}], \tag{5.7}$$

where θ is the angle of the resistor direction with respect to the [100] stress direction and the stress is assumed to be uniaxial. It is clearly seen that the presence of a shear stress of 4% makes the

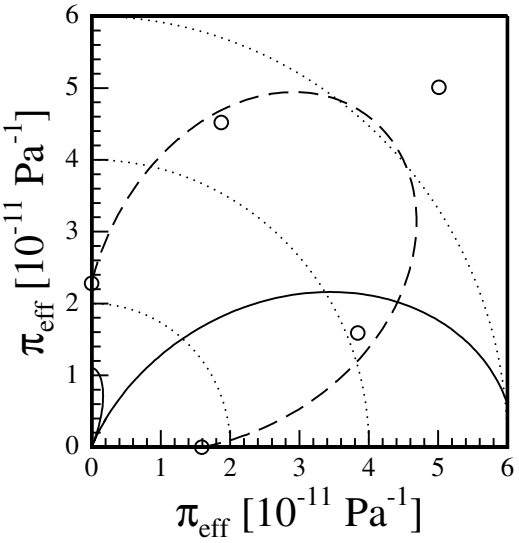


Figure 5.3: Polar plot illustrating the piezoresistive results obtained, when the chips are stressed along the [100] direction for silicon resistors with a doping concentration of $N_A = 1.6 \cdot 10^{18}$ cm^{-3}. The effective piezocoefficient is defined according to Eq. (5.7). The theoretical behavior of silicon is illustrated by the solid line, where it is assumed that there is a uniaxial stress and the values from Ref. [21] are used. The circular symbols show the actual measurements. The contribution from the shear stress, which is 4% of the applied uniaxial stress σ_{11} is added to Eq. (5.7) and the dashed line represents the expected effective piezocoefficient. This effective piezocoefficient is calculated by using Eq. (2.26) on page 26 and the piezocoefficient values obtained in this measurement (i.e. $\pi_{11} = 1.6 \cdot 10^{-11}$Pa^{-1} which is the interception with the x-axis where $\theta = 0$ and $\pi_{12} = 2.3 \cdot 10^{-11}$Pa^{-1} which is the interception with the y-axis where $\theta = \frac{\pi}{2}$, and $\pi_{44} = 103.4 \cdot 10^{-11}$Pa^{-1} determined from another measurement). It is clearly seen that the contribution from the shear stress has a profound influence on the results and explains the obtained measurements.

measured data significantly deviate from the theoretical behavior. Notice, that the numerical values obtained by the measurements of $\pi_{11} = 1.6 \cdot 10^{-11}$ Pa^{-1} and $\pi_{12} = 2.3 \cdot 10^{-11}$ Pa^{-1}, which are the values on the x axis (the resistor is directed along the applied stress direction) and y axis (the resistor is directed perpendicular to the applied stress direction) of the polar plot, respectively do not agree with the values reported in Ref. [21] ($\pi_{11} = 6.6 \cdot 10^{-11}$ Pa^{-1} and $\pi_{12} = -1.1 \cdot 10^{-11}$ Pa^{-1}) listed in Table 1.1 on page 6.

The values of π_{11} and π_{12} in p-type silicon can not be determined with a satisfactory uncertainty. Thus, in this thesis the focus is on the extraction of the value of the piezocoefficient π_{44}. The values of π_{11} and π_{12} are numerically found to be in the same order of magnitude as determined by Smith [21] but the uncertainty on each measurement is too large to extract a reliable value. For all measurements of $(\pi_{11} + \pi_{12})$ a value of approximately $1 \cdot 10^{-11}$ Pa^{-1} to $5 \cdot 10^{-11}$ Pa^{-1} is found.

5.2.2 π_{44}

This section presents the results of π_{44}. The piezocoefficients are extracted from measurements on two resistors (as in Eq. (5.2)) or from measurement on one "Hall type" resistor (as in Eq. (5.3)). The

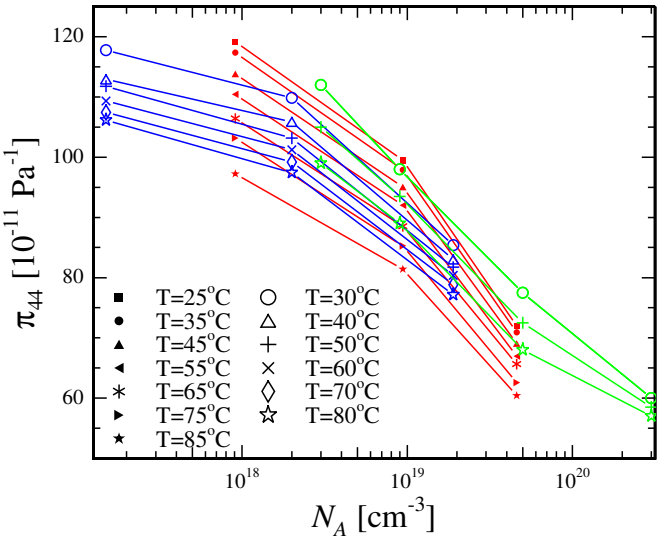


Figure 5.4: The piezocoefficient π_{44} as a function of temperature and doping concentration on uniformly doped piezoresistors (blue), Gaussian doping profile piezoresistors (red) and measurements from Ref. [27] (green). The measurements performed in this thesis show good agreement with previous published results.

measurements of π_{44} include both measurements of piezoresistors with a Gaussian doping profile and piezoresistors with a uniform doping profile. For the Gaussian doping profile piezoresistors the expected peak doping concentration found in the analysis in Sec. 4.2.2 is used as a reference. The results of the piezocoefficient π_{44} are shown in Fig. 5.4. The piezocoefficient π_{44} decreases in magnitude when increasing the doping concentration, for example in a uniformly doped piezoresistor at room temperature π_{44} changes from $118 \cdot 10^{-11}$ Pa^{-1} to $85 \cdot 10^{-11}$ Pa^{-1} when increasing the doping concentration from $1.5 \cdot 10^{17}$ cm^{-3} to $2.2 \cdot 10^{19}$ cm^{-3}. This decrease in the value of π_{44} is in agreement with the previous published results shown in Fig. 1.5 on page 7 and can be explained by considering the occupation of charge carriers in the energy bands. The resistivity depends on the curvature of these bands since the curvature is related to the effective mass, and the curvature is effected by an applied stress. In the outer regions of the energy bands far from the local maximum at $k = 0$ the change in curvature may not be as effective as the curvature change near $k = 0$. At low doping concentrations the carriers are mostly distributed around $k = 0$. Increasing the doping concentration the carriers occupy states further away from the local maximum and these carriers are not affected in the same way as the carriers near $k = 0$. This may explain why π_{44} decreases when increasing the doping concentration.

For all doping concentrations the magnitude of π_{44} is seen to decrease when increasing the temperature. However, the magnitude of this temperature dependency is a function of the doping concentration. The piezocoefficient depends strongly on temperature for low doping concentrations. This temperature dependency is seen to decrease when the doping concentration is increased. This may be explained by the change in the distribution function as a function of temperature. The occupied states are placed in a small area near $k = 0$ when the doping concentration is low. If the distribution function is changed due to a change in temperature the hole distribution may change significantly. On the other hand, if the hole concentration is large the same change in temperature does not have the same large relative influence on the distribution of the holes.

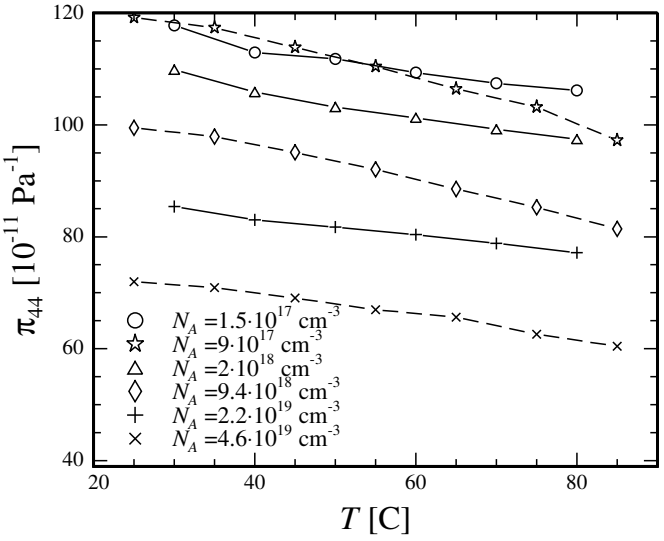


Figure 5.5: The piezocoefficient π_{44} as a function of temperature on uniformly doped piezoresistors (solid lines) and Gaussian doping profile piezoresistors (dashed lines). The temperature dependency is decreased as doping concentration increases. The Gaussian doping profile piezoresistors have a larger temperature dependency than the uniformly doped piezoresistors since in these piezoresistors not only the peak doping concentration (as is used in the legend to identify the resistors) contributes, but also the lower doping concentrations which are present in the piezoresistor.

The piezocoefficient π_{44} is determined in resistors with a Gaussian doping profile and with a uniform doping profile. Since π_{44} depends on the doping concentration the extracted π_{44} values varies depending on the doping profile. The uniform doping profile resistors are expected to give the correct π_{44} value at a given doping concentration. The Gaussian doping profile resistors are expected to give an effective π_{44} which is an weighted average value of π_{44} of the doping concentrations from the peak concentration to the pn-junction intersection at $N_A \approx 10^{15}$ cm^{-3}. Since this effective π_{44} is a weighted average value (which means that lower doping concentrations contribute to the value of π_{44}) the temperature dependency is larger than that of the π_{44} value extracted from the uniformly doped resistors and the magnitude of the effective π_{44} is generally larger than π_{44} extracted from a uniformly doped resistor. These results are also seen in Fig. 5.5 where the temperature dependency of π_{44} is plotted. For example, the value of π_{44} obtained in the Gaussian doping profile piezoresistor with $N_A = 9 \cdot 10^{17}$ decreases from $119 \cdot 10^{-11}$ Pa^{-1} to $97 \cdot 10^{-11}$ Pa^{-1} (which is a decrease of 18%) when the temperature is changed from 25°C to 85°C, whereas π_{44} measured on a piezoresistor with a uniform doping concentration of $N_A = 1.5 \cdot 10^{17}$ decreases from $118 \cdot 10^{-11}$ Pa^{-1} to $106 \cdot 10^{-11}$ Pa^{-1} (which is a decrease of 10%) when the temperature changes from 30°C to 80°C. Thus, the doping profile of the piezoresistor has a large impact on the magnitude of the extracted value of π_{44} and on the temperature dependency of π_{44}.

The obtained values of the piezocoefficient π_{44} all show lower values than the value commonly used, i.e. $\pi_{44} = 138.1 \cdot 10^{-11}$ Pa^{-1} taken from Ref. [21]. The values of π_{44} obtained in this project are all between $60 \cdot 10^{-11}$ Pa^{-1} to $120 \cdot 10^{-11}$ Pa^{-1} for resistors with doping concentrations from $N_A = 1.5 \cdot 10^{17}$ cm^{-3} to $N_A = 4.6 \cdot 10^{19}$ cm^{-3} and in the temperature range from 25°C to 85°C. Thus, for resistors with these properties it is very important not to directly use the values from Ref. [21]

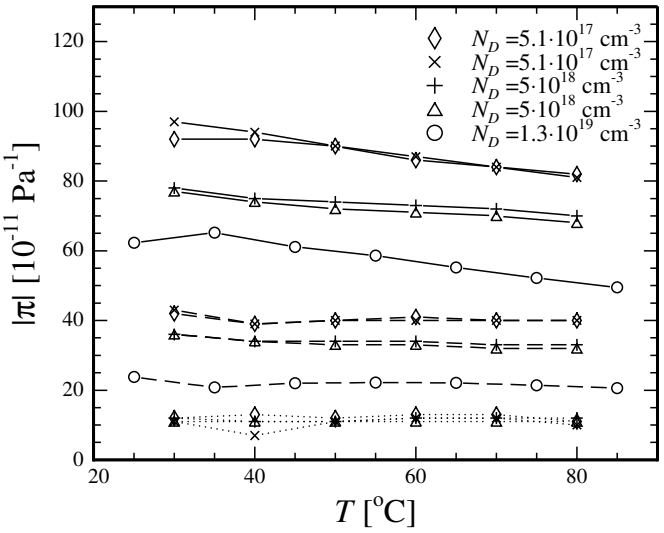


Figure 5.6: The absolute values of the piezocoefficients ($|\pi_{11}|$ - solid lines, π_{12} - dashed lines, and $|\pi_{44}|$ - dotted lines) in ion implanted n-type silicon as functions of temperature for three different doping concentrations. The piezocoefficient π_{11} depends on both doping concentration and temperature, the piezocoefficient π_{12} depends mostly on doping concentration and π_{44} does not change significantly as a function of doping concentration and temperature. The piezoresistors used are i4-i7 and u4 (∘) listed in Table 4.3 on page 54 and Table 4.6 on page 58, respectively.

but to adjust the values according to the values obtained in this thesis. The theoretical model described in App. B.1 focuses on this adjustment and gives an expression of how to determine the piezocoefficient value as a function of doping concentration and temperature. The function, which is also presented in Eq. (1.11) on page 10 can be used by MEMS designers in order to predict the piezoresistive output of a device. The model seems to be in much better agreement with experiments compared to the most commonly used model by Kanda [31]. App. J.1 lists the obtained values of π_{44} in p-type silicon.

5.3 *n*-type silicon

This section presents the piezoresistive measurements performed on n-type silicon. The results are obtained from five wafers, where one is uniformly doped and four have a Gaussian doping profile. The Gaussian doping profile piezoresistors have been implanted with the same dose in pairs, i.e. i4 and i5 have the same peak doping concentration and i6 and i7 have the same peak concentration, all listed in Table 4.3 on page 54. The results of the three piezocoefficients in n-type silicon as a function of temperature are shown in Fig. 5.6. Clearly, the values of the piezocoefficients obtained from the piezoresistors fabricated with the same dose (i.e. same doping concentration) follow the same trends.

The numerical largest piezocoefficient, π_{11}, is highly dependent on doping concentration and temperature. The obtained value numerically decreases from $-97 \cdot 10^{-11}$ Pa^{-1} to $-62 \cdot 10^{-11}$ Pa^{-1} (at $T = 30$°C and $T = 25$°C, respectively) when increasing the doping concentration from $5.1 \cdot 10^{17}$ cm^{-3} to $1.3 \cdot 10^{19}$ cm^{-3}. The temperature dependency decreases as the doping concentration in-

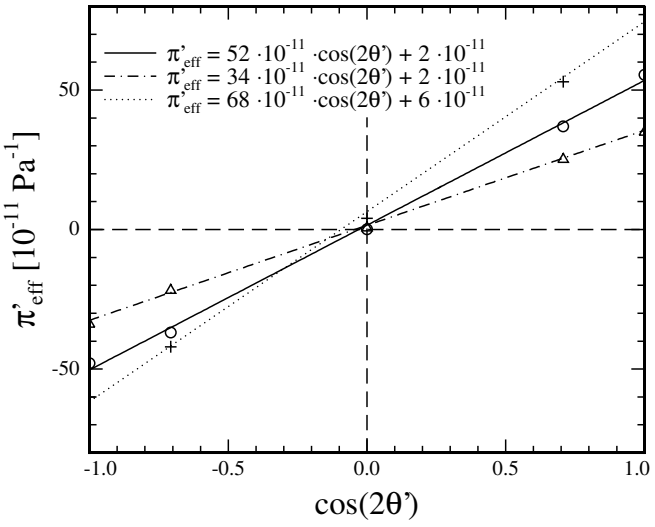


Figure 5.7: The effective piezocoefficient π'_{eff} described by Eq. (5.8) for MBE grown Si (solid line) with $N_A = 1.6 \cdot 10^{18}$ cm^{-3}, tensile strained Si (dashed and dotted line) with $N_A = 3 \cdot 10^{18}$ cm^{-3} ($\epsilon = 0.004$) and compressive strained $Si_{0.9}Ge_{0.1}$ (dotted line) with $N_A = 1.6 \cdot 10^{18}$ cm^{-3} ($\epsilon = -0.004$) at room temperature. The π_{66} piezocoefficient is the slope of the linear fit times two. The intersection with the π'_{eff}-axis is $0.5 \cdot (\pi_{11} + \pi_{12})$.

creases. For example, for the Gaussian doping profile piezoresistors with a peak doping concentration of $N_D = 5.1 \cdot 10^{17}$ cm^{-3} $\pi_{11} = -97 \cdot 10^{-11}$ Pa^{-1} at $T = 30$°C and this value numerically decreases by 16% at $T = 80$°C. With a peak doping concentration of $N_D = 5 \cdot 10^{18}$ cm^{-3} in the piezoresistor $\pi_{11} = -77 \cdot 10^{-11}$ Pa^{-1} at $T = 30$°C and this value decreases by 12% at $T = 80$°C. The doping concentration dependency is also present for the second largest piezocoefficient π_{12}, where $\pi_{12} = 43 \cdot 10^{-11}$ Pa^{-1} ($T = 25$°C) when $N_D = 5.1 \cdot 10^{17}$ cm^{-3} and $\pi_{12} = 24 \cdot 10^{-11}$ Pa^{-1} ($T = 30$°C) when $N_D = 1.3 \cdot 10^{19}$ cm^{-3} and it has is no measurable temperature dependency. Finally, the piezocoefficient π_{44} does not have any significant dependency on temperature nor doping concentration, for example when $N_D = 5.1 \cdot 10^{17}$ cm^{-3} and $T = 25$°C, $\pi_{44} = -12 \cdot 10^{-11}$ Pa^{-1} and when $N_D = 5 \cdot 10^{18}$ cm^{-3} and $T = 80$°C, $\pi_{44} = -11 \cdot 10^{-11}$ Pa^{-1}.

The extracted piezocoefficients at $T = 30$°C for the lowest doping concentration $N_D = 5.1 \cdot 10^{17}$ cm^{-3} ($\pi_{11} = -97 \cdot 10^{-11}$ Pa^{-1}, $\pi_{12} = 43 \cdot 10^{-11}$ Pa^{-1}, and $\pi_{44} = -12 \cdot 10^{-11}$ Pa^{-1}) are comparable with the values obtained by Ref. [21] listed in Table 1.1 on page 6 ($\pi_{11} = -102.2 \cdot 10^{-11}$ Pa^{-1}, $\pi_{12} = 53 \cdot 10^{-11}$ Pa^{-1}, and $\pi_{44} = -13.6 \cdot 10^{-11}$ Pa^{-1}). The obtained piezocoefficients in *n*-type silicon are listed in App. J.2.

5.4 Strained *p*-type silicon

This section presents the piezoresistive results of tensile strained Si ($\epsilon = 0.002, \epsilon = 0.004$) and compressive strained $Si_{0.9}Ge_{0.1}$ ($\epsilon = -0.004$). The tensile strained silicon resistors have a uniform doping concentration of $N_A = 3 \cdot 10^{18}$ cm^{-3} and the compressive strained $Si_{0.9}Ge_{0.1}$ resistors are boron doped with uniform doping concentrations of $N_A = 1.6 \cdot 10^{18}$ cm^{-3} and $N_A = 1.7 \cdot 10^{19}$ cm^{-3}. Fig. 5.7 shows the results for MBE grown silicon (where $\pi_{44} = \pi_{66}$), tensile strained silicon ($\epsilon = 0.004$), and

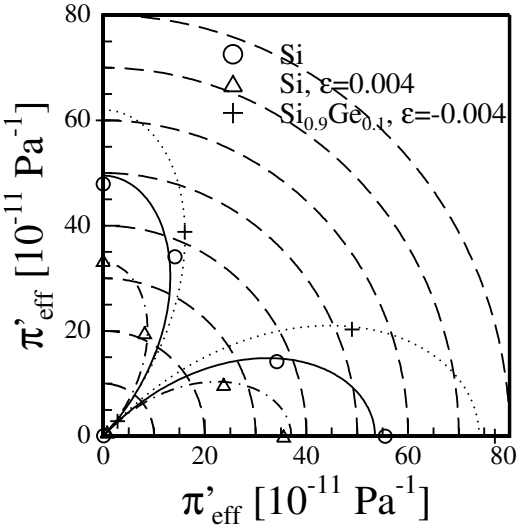


Figure 5.8: A polar plot of the effective piezocoefficient π'_{eff} described by Eq. (5.8) for MBE grown Si (solid line) with $N_A = 1.6 \cdot 10^{18}$ cm^{-3}, tensile strained Si (dashed and dotted line) with $N_A = 3 \cdot 10^{18}$ cm^{-3} ($\epsilon = 0.004$) and compressive strained $Si_{0.9}Ge_{0.1}$ (dotted line) with $N_A = 1.6 \cdot 10^{18}$ cm^{-3} ($\epsilon = -0.004$) at room temperature. The lines are the fits to the data with the extracted slopes ($\frac{1}{2}\pi_{66}$) and offsets ($\frac{1}{2}[\pi_{11} + \pi_{12}]$) from Fig. 5.7.

compressive strained $Si_{0.9}Ge_{0.1}$ ($\epsilon = -0.004$) where the effective piezocoefficient, π'_{eff}, is defined as

$$\pi'_{\text{eff}} = \frac{1}{2}[\pi_{11} + \pi_{12} + \pi_{66}\cos(2\theta')], \tag{5.8}$$

and θ' is the angle between the resistor direction and the [110] stress direction. Notice that the slope of the linear fits in Fig. 5.7 and thus π_{66} changes drastically between the three materials. The slope is proportional to the piezocoefficient π_{66}. The compressively strained $Si_{0.9}Ge_{0.1}$ with $\epsilon = -0.004$ has a piezocoefficient $\pi_{66} = 136 \cdot 10^{-11}$ Pa^{-1} which is 30% larger than the piezocoefficient $\pi_{44} = 103 \cdot 10^{-11}$ Pa^{-1} measured in MBE grown silicon with $N_A = 1.6 \cdot 10^{18}$ cm^{-3}. The tensile strained Si with $\epsilon = 0.004$ has a piezocoefficient $\pi_{66} = 70 \cdot 10^{-11}$ Pa^{-1}. The π_{66} value is decreased by 25% compared to the measured $\pi_{44} = 93 \cdot 10^{-11}$ Pa^{-1} in MBE grown silicon with $N_A = 3 \cdot 10^{18}$ cm^{-3}.

The large increase in the piezocoefficient in $Si_{0.9}Ge_{0.1}$ is not necessarily a result of the compressive strain. The germanium atoms could also introduce some difference in the value of the piezocoefficient. In order to investigate this a first order linear relation between the two material contents and the piezocoefficient is written as $\pi_{66}(Si_{0.9}Ge_{0.1}) = 0.9 \cdot \pi_{44}(Si) + 0.1 \cdot \pi_{44}(Ge)$. According to Table 1.1 on page 6 the piezocoefficient π_{44} in germanium is smaller than π_{44} in silicon, thus if the germanium atoms contribute significantly to the value of π_{66} a value smaller than π_{44} in silicon should be obtained. Thus, it is most possible that the increased piezocoefficient is caused by the strain in the material. This conclusion is verified by the fact that the piezocoefficient π_{66} in strained silicon is also changed drastically.

The offset of the linear fits in Fig. 5.7, i.e. $0.5 \cdot (\pi_{11} + \pi_{12})$, is approximately three times larger for compressive strained $Si_{0.9}Ge_{0.1}$ than for the two other materials. The effective piezocoefficients are plotted in a polar plot in Fig. 5.8, where the extracted slopes and offsets from Fig. 5.7 are used.

N_A cm^{-3}	π_{44} Si 10^{-11} Pa^{-1}	π_{66} $Si_{0.9}Ge_{0.1}$ 10^{-11} Pa^{-1}
$1.6 \cdot 10^{18}$	103	136
$1.7 \cdot 10^{19}$	81	86.8

Table 5.1: Measurements of the piezocoefficient π_{44} in Si and the piezocoefficient π_{66} in compressive strained $Si_{0.9}Ge_{0.1}$ ($\epsilon = -0.004$) for two different doping concentrations. With a doping concentration of $N_A = 1.6 \cdot 10^{18}$ cm^{-3} in the piezoresistor the difference of the measured piezocoefficients is large between silicon and strained $Si_{0.9}Ge_{0.1}$, however this large difference is not present with a doping concentration of $N_A = 1.7 \cdot 10^{19}$ cm^{-3}.

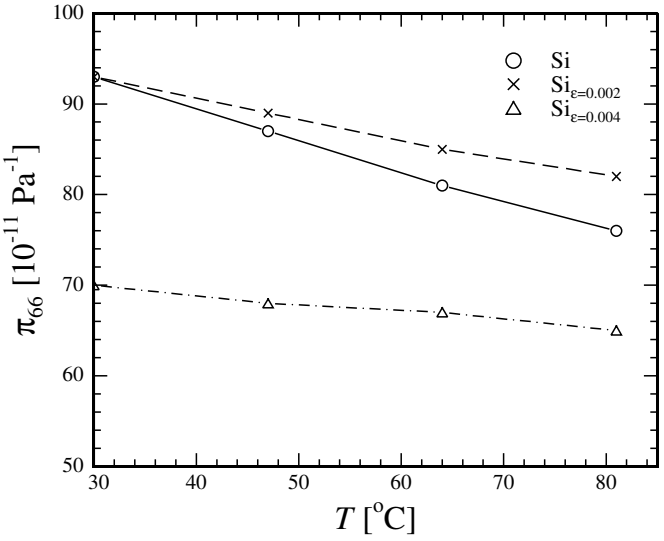


Figure 5.9: The π_{66} piezocoefficient for MBE grown Si (solid line), tensile strained Si, $\epsilon = 0.002$ (dashed line) and $\epsilon = 0.004$ (dashed and dotted line) with doping concentrations of $N_A = 3 \cdot 10^{18}$ cm^{-3} as a function of temperature. The temperature dependency decreases when increasing the strain. For $\epsilon = 0.002$ the magnitude of π_{66} at $T = 30°$ is equal to the magnitude of π_{44} in silicon. For $\epsilon = 0.004$ the magnitude of the piezocoefficient is deceased by 25%. This suggests that the magnitude of π_{66} does not depend linearly on the strain in the crystal.

The shapes of the polar plots confirm that in the strained crystals $\pi_{11} \ll \pi_{66}$ and $\pi_{12} \ll \pi_{66}$ which also applies for silicon.

For compressive strained $Si_{0.9}Ge_{0.1}$ the piezoresistance measurements are performed on resistors with two doping concentrations. The effect of doping concentration for compressive strained $Si_{0.9}Ge_{0.1}$ is shown in Table 5.1 including measurements on MBE grown silicon as reference. It is seen that the piezocoefficients in strained $Si_{0.9}Ge_{0.1}$ depends strongly on doping concentration (decreases by 36% when the doping concentration is decreased from $N_A = 1.6 \cdot 10^{18}$ cm^{-3} to $N_A = 1.7 \cdot 10^{19}$ cm^{-3}). With a doping concentration of $N_A = 1.7 \cdot 10^{19}$ cm^{-3} the piezocoefficient π_{66} is approximately the same as the piezocoefficient π_{44} in silicon. This is to be compared with the large difference of 36% between silicon and strained $Si_{0.9}Ge_{0.1}$ with a doping concentration of $N_A = 1.6 \cdot 10^{18}$ cm^{-3}.

The temperature dependency of the piezocoefficient π_{66} for tensile strained silicon is shown in Fig. 5.9. The temperature dependency decreases when increasing the strain. The magnitude of the piezocoefficient π_{66} for a tensile strain of $\epsilon = 0.002$ is comparable to that of π_{44} for silicon at $T = 30°C$. However, for $\epsilon = 0.004$ the magnitude is decreased by 27%. This may suggest that the magnitude of the piezocoefficient is not linearly dependent on the strain. For MBE grown silicon π_{44} decreases from $93 \cdot 10^{-11}$ Pa^{-1} to $76 \cdot 10^{-11}$ Pa^{-1} (which is a decrease of 18%) when increasing the temperature from 30°C to 81°C, whereas π_{66} in tensile strained silicon, $\epsilon = 0.004$, decreases from $69 \cdot 10^{-11}$ Pa^{-1} to $65 \cdot 10^{-11}$ Pa^{-1} (which is a decrease of 6%) in the same temperature domain. The observed temperature dependency of π_{44} (18% decrease when increasing the temperature from 30°C to 81°C) in the MBE grown silicon sample ($N_A = 3 \cdot 10^{18}$ cm^{-3}) is significantly larger than observed in the uniformly doped resistors presented in Sec. 5.2.2 where π_{44} is decreased by 12% ($N_A = 2 \cdot 10^{18}$ cm^{-3}) in the same temperature range. The larger temperature dependency of the MBE grown resistors may be caused by a poor interface between substrate and resistor. If defects are present near the interface these can result in a larger temperature variation. The uniformly doped resistors presented in Sec. 5.2.2 are fabricated on SOI wafers and are expected to be fully isolated in the full temperature range.

The measurements show that the piezoresistive effect is highly dependent on the strain in the crystal. The piezoresistive effect can be tailored in terms of magnitude and temperature dependency by increasing or decreasing the strain in silicon. A compressive strain increases the piezoresistance while a tensile strain decreases the piezoresistance. Furthermore, the piezocoefficient π_{66} in tensile strained silicon has a smaller temperature dependency compared to π_{44} in silicon. The measured piezocoefficients of the strained crystals are all listed in App. J.3.

5.5 Silicon nanowires

This section presents the measurements of the piezocoefficient π_{44} in p-type silicon nanowires. The piezocoefficient is investigated as a function of nanowire width. The piezocoefficient is found by performing measurements on the resistors presented in Fig. 5.1d. It is assumed that $\pi_{44} \gg \pi_{11}$ and $\pi_{44} \gg \pi_{12}$, thus

$$\frac{\Delta R}{R} = \frac{\sigma'_{11}}{2}(\pi_{11} + \pi_{12} + \pi_{44}) \approx \frac{\sigma'_{11}}{2}\pi_{44}, \tag{5.9}$$

according to Sec. 2.4.2.1 where σ'_{11} is directed along the [110] direction. The widths of the nanowires varies from 50 nm to 350 nm. A micrometer scaled reference piezoresistor is located on each chip in order to compare the results of the nanowires to standard micrometer sized piezoresistors fabricated with the use of UV lithography. Measurements are performed on crystalline silicon nanowires with doping concentrations of approximately $N_A = 1.5 \cdot 10^{17}$ cm^{-3} and $N_A = 1.2 \cdot 10^{20}$ cm^{-3} and on polycrystalline silicon nanowires with resistivity of $\rho = 0.15$ Ωcm. The relation between resistivity and doping concentration in polysilicon depends on the fabrication process and the grain size. It was not possible to determine the doping concentration, thus the resistivity is used as a reference for the polysilicon nanowires.

The extracted values of π_{44} as a function of nanowire width are shown in Fig. 5.10. For the low doped nanowires ($N_A = 1.5 \cdot 10^{17}$ cm^{-3}) the piezocoefficient π_{44} increases when decreasing the width. The largest increase of π_{44} is found in a 140 nm wide nanowire with a thickness of 200 nm. The observed value $\pi_{44} = 910 \cdot 10^{-11}$ Pa^{-1} is approximately 7 times larger (an increase of 630%) than the value of π_{44} of the reference resistor. The increase in the value of π_{44} as a function of decreasing width can not be explained by quantum effects due to the size of the nanowires, but

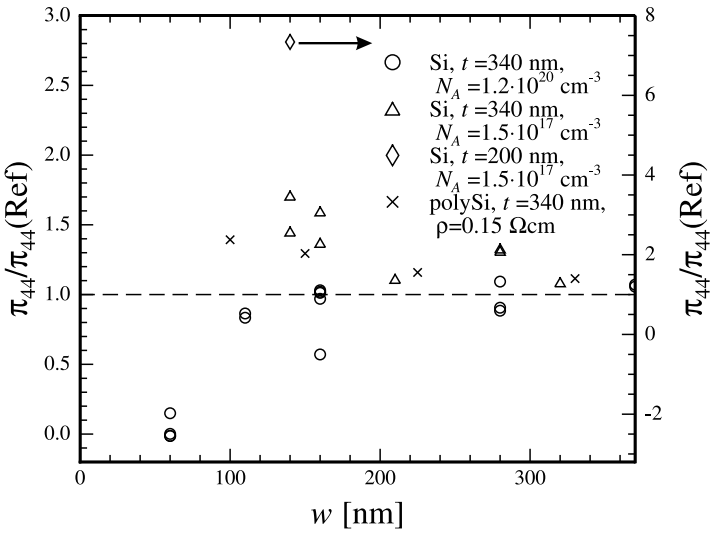


Figure 5.10: The piezocoefficient π_{44} normalized with respect to the piezocoefficient π_{44}(Ref) of the micrometer scaled reference piezoresistor as a function of nanowire width w for p-type silicon nanowires. All resistors have a length to width ratio of approximately 20. The piezocoefficient π_{44} increases significantly when decreasing the width of the nanowires with a low doping concentration. This behavior may be explained by the increasing ratio between number of surface states and number of carriers in the nanowire when decreasing the width. The results show a large variation which may be caused by a large variation in the surface roughness of the individual nanowires. Notice, π_{44} from the nanowire with a thickness of $t = 200$ nm is plotted on the right axis and the results of all of the other nanowires are plotted on the left axis. For polysilicon nanowires π also increases when the width is decreased, however this increase is smaller than in the case of crystalline silicon. For highly doped silicon the piezocoefficient π_{44} does not change as a function of width when the width is larger than 100 nm and π_{44} approaches zero for nanowire widths smaller than 100 nm. This behavior may be explained by surface scattering effects.

may be explained by the presence of surface states at the silicon silicon dioxide interface. The nanowires are surrounded by a thermally grown oxide. The density of surface states is approximately $D_{\text{it}} = 10^{11} - 10^{12}$ cm^{-2}/eV [69] near the silicon silicon dioxide interface. Due to the presence of these surface states in the oxide the same number of states but with opposite sign is present in silicon. In a standard micrometer sized piezoresistor the number of surface states is much smaller than the number of carriers thus the surface states do not contribute significantly to the piezoresistance effect. However, by decreasing the size the number of surface states are approaching the number of carriers. The number of surface states in the nanowire of width 140 nm, thickness 200 nm and length 3 μm can be calculated as $n_{\text{it}} = D_{\text{it}} \cdot (2A_1 + 2A_2) \cdot kT$, where $A_1 = 140 \cdot 10^{-7} \cdot 3 \cdot 10^{-4}$ cm^2 $= 4.2 \cdot 10^{-9}$ cm^2 is the area of the top and bottom of the nanowire and $A_2 = 200 \cdot 10^{-7} \cdot 3 \cdot 10^{-4}$ cm^2 $= 6 \cdot 10^{-9}$ cm^2 is the area of the sidewall of the nanowire, and $kT = 0.0259$ eV is the thermal energy at $T = 27$°C. When assuming a surface state density of $D_{\text{it}} = 5 \cdot 10^{11}$ cm^{-2}/eV the number of states in the nanowire due to surface states is $n_{\text{it}} = 5 \cdot 10^{11}(2 \cdot 4.2 \cdot 10^{-9} + 2 \cdot 6 \cdot 10^{-9}) \cdot 0.0259 = 264$. The doping concentration in the nanowire is measured to be $N_A = 1.5 \cdot 10^{17}$ cm^{-3} and the number of carriers implanted in the nanowire is thus $n_p = N_A \cdot V = 12600$, where $V = 140 \cdot 200 \cdot 3000$ nm^3. Thus, the number of surface states is 2.1% of the number of carriers implanted in the nanowire. The ratio between surface states and implanted carriers increases as nanowire width decreases. When the nanowire is strained the number of surface states change and if this change result in a significant

change in the ratio between surface states and carriers this may effect the piezoresistive properties. This might explain the increase in the piezocoefficient value for decreasing width, which is seen in Fig. 5.10. In future experiments, it is suggested to perform measurements on nanowires with other passivation layers than silicon dioxide, which is used for these measurements, in order to further investigate the effect from the surface states. The large difference in the piezocoefficients obtained for the two nanowires with width 140 nm may be explained by the difference in resistor thickness. The number of surface states is approximately a factor of 1.5 larger for the resistor which has a much larger piezocoefficient compared to the other resistor. The number of surface states is dependent on the roughness of the resistor, and if the resistor of thickness 200 nm has a larger surface roughness this will increase the number of surface states. The variation in the results presented in Fig. 5.10 for all nanowire widths may be due to a variation in the surface roughness of the nanowires.

For the highly doped resistors in Fig. 5.10 the doping concentration is measured to be $N_A = 1.2 \cdot 10^{20}$ cm^{-3}. The ratio between surface states and carriers is thus decreased by a factor of 10^{-3} compared to the nanowires with doping concentration $N_A = 1.5 \cdot 10^{17}$ cm^{-3}. In Fig. 5.10 it is seen that the piezocoefficients of the highly doped nanowires are constant as a function of nanowire width for nanowires larger than 100 nm. This may be a result of the small ratio between surface states and implanted carriers. For these highly doped nanowires the piezocoefficient π_{44} approaches zero when the width is 60 nm. This decrease in the value of the piezocoefficient may be explained by the boundary scattering. The resistivity in the nanowire is considered a function of two contributions: The resistivity in the bulk material and the resistivity in the surface regions where scattering occurs. If the width of the surface scattering region is constant, these regions approaches the center of the nanowire when decreasing the size and overlap at a certain nanowire width. When the surface scattering regions overlap the resistivity depends only on the surface scattering. The resistivity in the surface scattering regions is much larger than the resistivity in the bulk material and is assumed to be independent of stress. Thus, if surface scattering is dominant the resistance of an unstressed nanowire increases significantly, but the change in the bulk resistance due an applied stress is the same as a micrometer sized piezoresistor. This results in a decrease in the piezocoefficient.

The piezocoefficient value in polycrystalline silicon is increased by approximately 40% compared to the reference resistor when decreasing the width. For the reference resistor at room temperature a value of $\pi = 18 \cdot 10^{-11}$ cm^{-3} is obtained and for a 100 nm polysilicon nanowire with the same resistivity $\rho = 0.15$ Ωcm as the reference resistor $\pi = 25 \cdot 10^{-11}$ cm^{-3}. These results are in agreement with the results obtained in Ref. [70].

The piezocoefficients in silicon nanowires are highly dependent on the nanowire width. The measured data showed a maximum increase in the piezocoefficient value of up to 7 times the value of π_{44} in a micrometer scaled reference resistor. The obtained piezocoefficient values of crystalline silicon nanowires and polycrystalline silicon nanowires are listed in App. J.4. These preliminary measurements show that piezoresistive nanowires potentially can be used in highly sensitive MEMS and NEMS sensors. However, other issues such as the temperature dependency of the piezocoefficients and the influence from different passivation layers need to be investigated.

5.6 Summary

This chapter presented the results of the piezoresistance measurements performed on piezoresistors of

- p-type silicon.
- n-type silicon.
- Tensile strained p-type silicon and compressive strained p-type $Si_{0.9}Ge_{0.1}$.
- Crystalline and polycrystalline p-type silicon nanowires.

In general, the results showed that the piezoresistance is highly dependent on temperature when the doping concentration is low. The temperature dependency decreases when increasing the doping concentration. By pre-straining the silicon crystal structure the piezoresistive effect is changed. This can be used to either increase (compressive strained crystal) or decrease (tensile strained crystal) the value of π_{66} which is equivalent to π_{44} in silicon. It was also shown that the temperature dependency of the piezocoefficient π_{66} in a tensile strained Si crystal is smaller than the temperature dependency of π_{44} in silicon. The piezocoefficient π_{44} in silicon nanowires was shown to be highly dependent on the width of the nanowire, where an increase in the piezocoefficient π_{44} of up to 630% was shown. However, it was also found that this large increase is only found for low doped nanowires. The piezocoefficient approaches zero for nanowires with a high doping concentration. The piezocoefficient of polycrystalline silicon nanowires showed also to depend on nanowire width. However, the increase in the piezocoefficient value was 40%, which is significantly smaller than the large change observed in low doped crystalline silicon nanowires.

All of the measurements presented in this chapter was performed on the unidirectional resistors which were described in Sec. 3.5. The next section presents a circular resistor where the current density vector is rotated in the device while potential drops are measured near the center of the resistor. With the use of this device it is possible to obtain polar plots of the piezoresistance properties. These polar plots can be used to compare the piezoresistance properties of different materials.

CHAPTER

6 Circular resistor: A piezocoefficient mapping device and a stress sensor

In this chapter a circular resistor which allows for construction of 360° polar plots of the piezoresistance properties of semiconductors is presented. The novel device, which is inspired by the work in Refs. [11, 19], enables illustrative comparison of the piezoresistance effect of different materials and enables determination of the three piezocoefficients in silicon. This is all performed on one chip and using only one circular resistor.

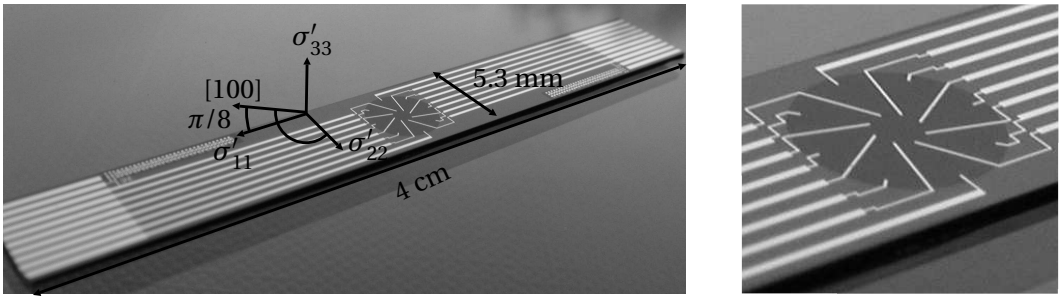
The design of the circular resistor is presented in the first section where the measurement concept is introduced. This is followed by a theoretical analysis which is a continuation of the derived theory in Sec. 2.3.2. The theoretically obtained equations are compared to results of a FEM analysis of the structure and appropriate correction factors are introduced. Finally, the measurements are presented. At the end of the chapter, preliminary results where the circular resistor is used as a stress sensor are shown.

The main focus of this project is to characterize the piezoresistance properties of different semiconductor materials. Comparison of these materials may be difficult and several samples need to be analyzed before drawing any conclusions. The circular resistor presented in this chapter enables this comparison by the use of only one chip and one resistor. The device is shown in Fig. 6.1.

In the end of the chapter it is investigated if this device can be used for packaging induced stress sensing. The last step to commercialization of a MEMS device is often related to packaging in order to protect the device from the surroundings. It is a challenging task to protect the device and not to affect the performance of the device at the same time. The performance of an electrical component can be highly influenced by packaging induced stress. Thus, packaging induced stress sensing is an important topic which draws attention from both academia [11, 71] and industry. The circular resistor can potentially be implemented in any fabrication process and thus operate as a stress sensor in a given packaged chip. This enables on-chip comparison between device performance and stress. The preliminary test experiments of stress sensing using the circular resistor have been introduced in the conference proceedings in Refs. [72, 73] and are presented in the end of the chapter.

6.1 Chip design

In this section a presentation of the chip design and measurement concept is given. The outer dimensions of the chip equal the outer dimensions of the chips presented in Sec. 3.1. In the center region of the chip a circular piezoresistor is located. The piezoresistor is doped with phosphorus by



(a) (b)

Figure 6.1: (a) Photograph of the chip with a circular resistor. The chip is cut along the direction which is rotated by $\frac{\pi}{8}$ with respect to the [100] direction. In the center region of the chip a single circular n-type resistor is located. A current is forced through the resistor by contacts near the perimeter and 8 contacts placed in the center of the resistor measure 4 potential drops. (b) Close up on the circular resistor. The figure shows that a total number of eight contacts are placed near the perimeter of the circular resistor. In the analysis in this chapter only four of these eight contacts are used. For the circular resistor used in this chapter the inner contacts are placed in a radius of 100 μm from the resistor center. This is a photograph of a former design where the inner contacts are placed in a radius of 500 μm from the resistor center.

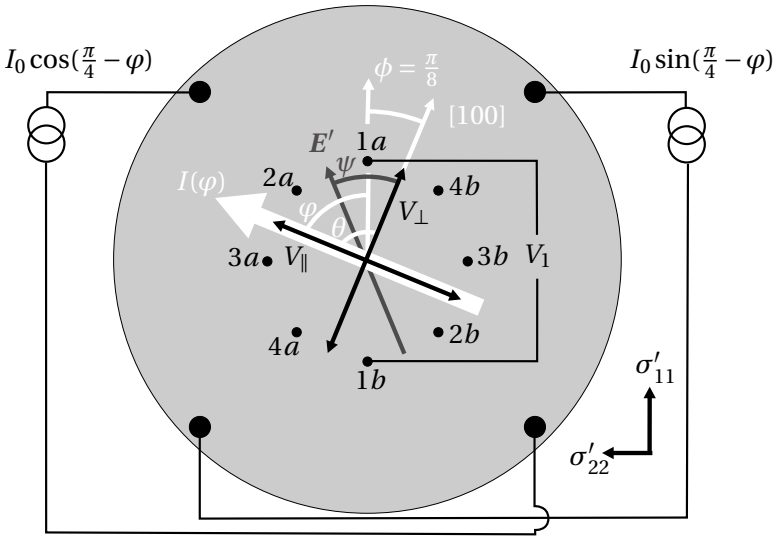


Figure 6.2: Schematic of the circular piezoresistor. The resistor radius is 1800 μm and the inner contacts are placed in a radius of 100 μm from the center. The four outer contacts spin the current $I(\varphi=\theta-\frac{\pi}{8})$ in the center of the resistor. The rotation of the electric field vector $\boldsymbol{E}'$ is described by ψ with respect to the [100] direction. The fictive voltage drops, $V_\parallel$ and $V_\perp$, are linear combinations of all measured potential drops, V_i = $V_{ia}-V_{ib}$ where $i=1,2,3,4$. The potential drop V_1 is shown as an example. The illustration is not to scale.

ion implantation and has a doping concentration of approximately $N_D = 10^{18}$ cm^{-3}, see App. I.7 for the full process sequence. This circular piezoresistor includes eight contacts placed near the perimeter used to inject a current, from which only four are used in the analysis in this chapter, and eight contacts placed near the resistor center used to measure the potential. The diameter of the inner contacts is 3 μm and these contacts are highly doped with phosphorus in order to obtain an Ohmic contact. The resistor diameter is 3600 μm and the eight inner contacts are located in a

radius of 100 μm from the center of the resistor. A conceptual drawing of the resistor is shown in Fig. 6.2. By using two current sources with magnitudes of $I_0\cos(\frac{\pi}{4}-\varphi)$ and $I_0\sin(\frac{\pi}{4}-\varphi)$, respectively, the current density vector in the center region described by the angle φ is rotated 360° in the circular piezoresistor. In this chapter the injected current $I(\varphi)$ is rotated in steps of 5°. This concept is named current spinning and is reported by Refs. [74, 75]. The eight inner contacts measure the potential drops $V_i = V_{ia} - V_{ib}$, where $i = 1,2,3,4$ for each current direction. A linear combination of the four measured potential drops gives the fictive voltage drops $V_\parallel$ and $V_\perp$ seen in Fig. 6.2. In the following section the expected potential drops of V_i, $V_\parallel$ and $V_\perp$ are derived as functions of the direction of the current density vector φ, the stress components and the piezocoefficients.

The chip is cut along the direction which is rotated by $\frac{\pi}{8}$ with respect to the [100] direction. By applying a uniaxial stress to the chip along this direction all three piezocoefficients can be extracted by using only one chip. Recall, the discussion in Sec. 3.3.1 where it was decided to use a two chip solution, one chip to measure π_{44} and one chip to measure π_{11} and π_{12}. The two chip solution was decided because this configuration gives the most accurate results. By using one chip that is rotated by $\frac{\pi}{8}$ with respect to the [100] direction the three piezocoefficients are obtained with a larger uncertainty. However, this rotation opens for other possibilities and the device is useful for comparison of different materials in supplement to the exact extraction of the three piezocoefficients. Furthermore, given a set of measured piezocoefficients complex stress determination is possible.

6.2 Theory

In Eq. (2.23) on page 25 the electric field vector was derived when the electric field vector and the current density vector were described in the same coordinate system. In the circular resistor the current density vector is rotated in the resistor while the contacts for the potential measurements are placed in the same point for all measurements. Thus, it is convenient to describe the two vectors, the electric field vector and the current density vector, in two different coordinate systems. The electric field vector is transformed according to

$$E_i' = M_{ij}E_j, \tag{6.1}$$

where the transformation now is described by the angle ψ, which is the rotation of the electric field vector with respect to the [100] direction in the (001) plane (and not θ which is the angle that describes the rotation of the current density as in Eq. (2.21) on page 24). If ϕ describes the rotation of the stress tensor with respect to the [100] direction (as described in detail in Sec. 2.3.2),

the electric field vector is written as

$$\frac{\boldsymbol{E}'}{J_1'\rho_0} = \begin{bmatrix} \cos(\theta-\psi) \\ +\frac{1}{2}\left[\cos(\theta-\psi)\pi_{11}+\cos(2\phi)\cos(\theta+\psi)\left(\pi_{11}-\pi_{12}\right)+\cos(\theta-\psi)\pi_{12}+\sin(2\phi)\sin(\theta+\psi)\pi_{44}\right]\sigma_{11}' \\ +\frac{1}{2}\left[-2\cos(\theta+\psi)\sin(2\phi)\left(\pi_{11}-\pi_{12}\right)+2\cos(2\phi)\sin(\theta+\psi)\pi_{44}\right]\sigma_{12}' \\ +\frac{1}{2}\left[\cos(\theta-\psi)\pi_{11}-\cos(2\phi)\cos(\theta+\psi)\left(\pi_{11}-\pi_{12}\right)+\cos(\theta-\psi)\pi_{12}-\sin(2\phi)\sin(\theta+\psi)\pi_{44}\right]\sigma_{22}' \\ +\cos(\theta-\psi)\pi_{12}\sigma_{33}' \\ \sin(\theta-\psi) \\ +\frac{1}{2}\left[\sin(\theta-\psi)\pi_{11}-\cos(2\phi)\sin(\theta+\psi)\left(\pi_{11}-\pi_{12}\right)+\sin(\theta-\psi)\pi_{12}+\cos(\theta+\psi)\sin(2\phi)\pi_{44}\right]\sigma_{11}' \\ +\frac{1}{2}\left[2\sin(2\phi)\sin(\theta+\psi)\left(\pi_{11}-\pi_{12}\right)+2\cos(2\phi)\cos(\theta+\psi)\pi_{44}\right]\sigma_{12}' \\ +\frac{1}{2}\left[\sin(\theta-\psi)\pi_{11}+\cos(2\phi)\sin(\theta+\psi)\left(\pi_{11}-\pi_{12}\right)+\sin(\theta-\psi)\pi_{12}-\cos(\theta+\psi)\sin(2\phi)\pi_{44}\right]\sigma_{22}' \\ +\sin(\theta-\psi)\pi_{12}\sigma_{33}' \\ \pi_{44}[\sigma_{13}'\cos(\theta-\phi)+\sigma_{23}'\sin(\theta-\phi)] \end{bmatrix}, \tag{6.2}$$

where the primed components are the components in the transformed coordinate systems.

The electric field vector simplifies significantly for the specific application. The length direction of the chip is cut along the direction which is oriented $\frac{\pi}{8} = 22.5°$ with respect to the [100] direction, thus $\phi = \frac{\pi}{8}$ since the applied stress from the 4PB fixture is directed along the chip. The angle θ is the rotation of the current density vector. In order to describe this vector in the stress coordinate system the angle φ is defined as $\varphi = \theta - \frac{\pi}{8}$ as illustrated in Fig. 6.2[1]. For example, if the electric field vector is rotated such that it is described in the stress coordinate system, i.e. $\psi = \frac{\pi}{8}$ the relative change in the electric field vector is

$$\frac{\boldsymbol{E}'(\psi=\phi=\frac{\pi}{8})-\boldsymbol{E}'(\psi=\phi=\frac{\pi}{8},\sigma_{ij}=0)}{\boldsymbol{E}'(\psi=\phi=\frac{\pi}{8},\sigma_{ij}=0)} = \begin{bmatrix} \frac{\sigma_{11}'}{4}\left[3\pi_{11}+\pi_{12}+\pi_{44}+(-\pi_{11}+\pi_{12}+\pi_{44})\tan(\varphi)\right] \\ +\frac{\sigma_{12}'}{2}\left[-\pi_{11}+\pi_{12}+\pi_{44}+(\pi_{11}-\pi_{12}+\pi_{44})\tan(\varphi)\right] \\ +\frac{\sigma_{22}'}{4}\left[\pi_{11}+3\pi_{12}-\pi_{44}+(\pi_{11}-\pi_{12}-\pi_{44})\tan(\varphi)\right] \\ +\sigma_{33}'\pi_{12} \\ \frac{\sigma_{11}'}{4}\left[\pi_{11}+3\pi_{12}-\pi_{44}+(-\pi_{11}+\pi_{12}+\pi_{44})\cot(\varphi)\right] \\ +\frac{\sigma_{12}'}{2}\left[\pi_{11}-\pi_{12}-\pi_{44}+(\pi_{11}-\pi_{12}+\pi_{44})\cot(\varphi)\right] \\ +\frac{\sigma_{22}'}{4}\left[3\pi_{11}+\pi_{12}+\pi_{44}+(\pi_{11}-\pi_{12}-\pi_{44})\cot(\varphi)\right] \\ +\sigma_{33}'\pi_{12} \\ 0 \end{bmatrix}, \tag{6.3}$$

where $\boldsymbol{E}'(\sigma_{ij}=0)$ is the electric field vector $\boldsymbol{E}'$ at zero stress. The above equation gives the relative change in the electric field vector in the stress coordinate system, when the current density is rotated an angle φ with respect to the stress direction. The first component of the above vector is thus the relative change of the electric field along the applied stress direction. According to Fig. 6.2

[1] Notice the notation: ϕ describes the rotation of the stress coordinate system with respect to the <100> coordinate system in the (001) plane. θ describes the rotation of the current density vector with respect to the <100> coordinate system in the (001) plane. φ describes the rotation of the current density vector with respect to the length direction of the chip. Since the chip is cut along the direction rotated by $\frac{\pi}{8}$ with respect to the <100> coordinate system in the (001) plane $\varphi = \theta - \frac{\pi}{8}$. ψ describes the rotation of the electric field vector with respect to the <100> coordinate system in the (001) plane. The angles are illustrated in Fig. 6.2.

the potential drop V_1 is measured along this direction and V_3 is measured perpendicular to this direction, i.e. the same direction as the second component of the vector above. The electric field is directly related to the potential drop thus

$$\begin{aligned}\frac{V_1 - V_{1,0}}{V_{1,0}} &= \frac{E_1' - E_{1,0}'}{E_{1,0}'} \\ \frac{V_3 - V_{3,0}}{V_{3,0}} &= \frac{E_2' - E_{2,0}'}{E_{2,0}'},\end{aligned} \tag{6.4}$$

where $E_{i,0}$ is the electric field component at zero stress and $\frac{E_i - E_{i,0}}{E_{i,0}}$ is described according to Eq. (6.3). By rotating the electric field vector another $\frac{\pi}{4}$, i.e. $\psi = \frac{\pi}{8} + \frac{\pi}{4}$ the equations of V_2 and V_4 can be found. In order to neglect the contribution from the measured potential drops at the points where the functions (in the case of V_1 and V_3 it is $\tan(\varphi)$ and $\cot(\varphi)$) approaches infinity two potential drops are defined in the current density coordinate system. These potential drops, $V_\parallel$ and $V_\perp$, are parallel to and perpendicular to the current density, respectively, as shown in Fig. 6.2. In terms of the four measurable potential drops these two fictive voltage drops are

$$\begin{aligned}V_\parallel &= \tfrac{1}{2}(\cos(\varphi)\cdot V_1 + \cos(\varphi - \tfrac{\pi}{4})\cdot V_2 + \sin(\varphi)\cdot V_3 + \sin(\varphi - \tfrac{\pi}{4})\cdot V_4) \\ V_\perp &= \tfrac{1}{2}(\sin(\varphi)\cdot V_1 + \sin(\varphi - \tfrac{\pi}{4})\cdot V_2 - \cos(\varphi)\cdot V_3 - \cos(\varphi - \tfrac{\pi}{4})\cdot V_4).\end{aligned} \tag{6.5}$$

By inserting the equations of the four potential drops into the above equation the relative change in the fictive voltage drops due to an applied stress are described by

$$\begin{aligned}\frac{\Delta V_\parallel}{V_{\parallel,0}} = &\left(\sigma_{11}' + \sigma_{22}' + \sigma_{33}'\frac{2\pi_{12}}{\pi_{11}+\pi_{12}}\right)\frac{\pi_{11}+\pi_{12}}{2} \\ &+ \cos(2\varphi)\left[(\sigma_{11}' - \sigma_{22}')\frac{\pi_{11}-\pi_{12}+\pi_{44}}{4} + \sigma_{12}'\frac{-\pi_{11}+\pi_{12}+\pi_{44}}{2}\right] \\ &+ \sin(2\varphi)\left[(\sigma_{11}' - \sigma_{22}')\frac{-\pi_{11}+\pi_{12}+\pi_{44}}{4} + \sigma_{12}'\frac{\pi_{11}-\pi_{12}+\pi_{44}}{2}\right]\end{aligned} \tag{6.6}$$

$$\begin{aligned}\frac{V_\perp}{V_{\parallel,0}} = &\cos(2\varphi)\left[(\sigma_{11}' - \sigma_{22}')\frac{\pi_{11}-\pi_{12}-\pi_{44}}{4} + \sigma_{12}'\frac{-\pi_{11}+\pi_{12}-\pi_{44}}{2}\right] \\ &+ \sin(2\varphi)\left[(\sigma_{11}' - \sigma_{22}')\frac{\pi_{11}-\pi_{12}+\pi_{44}}{4} + \sigma_{12}'\frac{-\pi_{11}+\pi_{12}+\pi_{44}}{2}\right],\end{aligned}$$

where $\Delta V_\parallel = V_\parallel - V_{\parallel,0}$ and $V_\parallel$ and $V_\perp$ are found according to Eq. (6.5) and

$$V_{\parallel,0} = \frac{1}{2}(\cos(\varphi)\cdot V_{1,0} + \cos(\varphi - \frac{\pi}{4})\cdot V_{2,0} + \sin(\varphi)\cdot V_{3,0} + \sin(\varphi - \frac{\pi}{4})\cdot V_{4,0}) \tag{6.7}$$

is the voltage drop $V_\parallel$ at zero stress.

In Eq. (6.6) the three piezocoefficients are coupled by linear combinations. Since, the piezoresistor is doped with phosphorus the difference in absolute magnitude of these coefficients vary from approximately $12\cdot10^{-11}$ Pa^{-1} to $97\cdot10^{-11}$ Pa^{-1} according to the results in Sec. 5.3 and each coefficient contributes to the equation. In boron doped silicon, the absolute magnitude of the coefficients vary much more, as seen in Sec. 5.2 and the piezocoefficient π_{44} dominates the linear combinations of the three piezocoefficients. Thus, if a p-type silicon piezoresistor is used it is not possible to distinguish between a linear combination of the three piezocoefficients and π_{44}. However, the resistor can still be used for comparison of the piezoresistance properties. A phosphorus

doped silicon piezoresistor is used in this chapter to demonstrate the method, since this dopant enables an extraction of all three piezocoefficients.

The equations in Eq. (6.6) are derived when the only contribution to the potential drop is the contribution from the change in resistivity due to the applied stress. However, non-ideal contributions may be present. Previously, the piezocoefficients were derived in a temperature controlled setup, but if the circular resistor is to be used as a stress sensor it is no longer in its controlled environment and thermal and magnetic effects can influence the measurement. These contributions to the measurement are discussed below.

Temperature changes in the resistor can be described by a linear change in the resistivity as $\rho = \rho_0[1+\alpha(T-T_0)]$, where α is the temperature coefficient of resistance, T_0 is the temperature at which the resistivity is ρ_0, and T is the actual temperature. In low doped n-type silicon $\alpha \approx 2500\cdot10^{-6}$ /C° [13]. If this temperature dependency of ρ is taken into account it is found that $V_\parallel$ depends on the temperature $\frac{\Delta V_\parallel}{V_{\parallel,0}}\left(\sigma_{ij},T\right) = \frac{\Delta V_\parallel}{V_{\parallel,0}}\left(\sigma_{ij}\right)+\alpha(T-T_0)$, where $V_{\parallel,0}$ is independent on temperature. The other fictive voltage drop $V_\perp$ is independent of temperature $\frac{V_\perp}{V_{\parallel,0}}\left(\sigma_{ij},T\right) = \frac{V_\perp}{V_{\parallel,0}}\left(\sigma_{ij}\right)$. Thus, if the temperature is not constant throughout the measurement the temperature change will contribute to the measured value of $V_\parallel$. For example, if the temperature is changed by 2°C the contribution from the temperature change is $2\alpha = 0.5\%$. By approximating the contribution from the stress to be $\sigma'_{11}\cdot\pi'_{\text{eff}}$ where $\pi'_{\text{eff}} \approx 100\cdot10^{-11}$ Pa^{-1}, the temperature contribution corresponds to a stress contribution of 5 MPa. Thus, a change in temperature results in a significant contribution to $V_\parallel$. In the above example the temperature dependency of the piezocoefficients is neglected. The results in Sec. 5.3 show that a small change of 2°C does not change the piezocoefficient value significantly. The temperature dependency was found to be largest for π_{11}, which numerically decreased by 16% in the temperature range from 30° to 80° corresponding to a temperature change of 0.32%/°C. With a temperature change of 2°C this results in a change of 0.64%. Thus the temperature dependency of the piezocoefficients is assumed to be negligible in the following and the fictive potential drop $V_\perp$ is considered independent on temperature. However if the potential drop is measured perpendicular to the current density a contribution from a possible magnetic field perpendicular to the resistor surface B_z will be present, $V_{\perp,B} = \mu_n V_\parallel B_z$, where μ_n is the mobility. The contribution from a magnetic field is assumed to be constant since the setup is located at the same place while all the measurements are performed. Thus, by offset compensation of $V_\perp$, i.e. $V_\perp = V_\perp - V_{\perp,0}$, where $V_{\perp,0}$ is measured at zero stress and is ideally zero, the contribution from a possible magnetic field is assumed to be negligible in the following.

6.3 FEM

In this section a 2D finite element model (FEM) in *COMSOL* [55] of the circular resistor structure is described and the results are compared to the analytical expression in Eq. (6.6). The 2D resistivity tensor is rotated by $\frac{\pi}{8}$ in order to comply with the length direction of the chip. This gives the components

$$\begin{aligned}
\rho'_{11} &= \rho_0[1+\tfrac{1}{4}(3\pi_{11}+\pi_{12}+\pi_{44})\sigma'_{11}+\tfrac{1}{4}(\pi_{11}+3\pi_{12}-\pi_{44})\sigma'_{22}+\tfrac{1}{2}(-\pi_{11}+\pi_{12}+\pi_{44})\sigma'_{12}+\pi_{12}\sigma'_{33}]\\
\rho'_{22} &= \rho_0[1+\tfrac{1}{4}(\pi_{11}+3\pi_{12}-\pi_{44})\sigma'_{11}+\tfrac{1}{4}(3\pi_{11}+\pi_{12}+\pi_{44})\sigma'_{22}+\tfrac{1}{2}(\pi_{11}-\pi_{12}-\pi_{44})\sigma'_{12}+\pi_{12}\sigma'_{33}]\\
\rho'_{12} &= \tfrac{\rho_0}{4}[(-\pi_{11}+\pi_{12}+\pi_{44})(\sigma'_{11}-\sigma'_{22})+2(\pi_{11}-\pi_{12}+\pi_{44})\sigma'_{12}].
\end{aligned} \tag{6.8}$$

where ρ_0 is the resistivity at zero stress and the stress components are defined in the coordinate system rotated $\frac{\pi}{8}$ with respect to [100]. The dimensions of the resistor described in Sec. 6.1 are

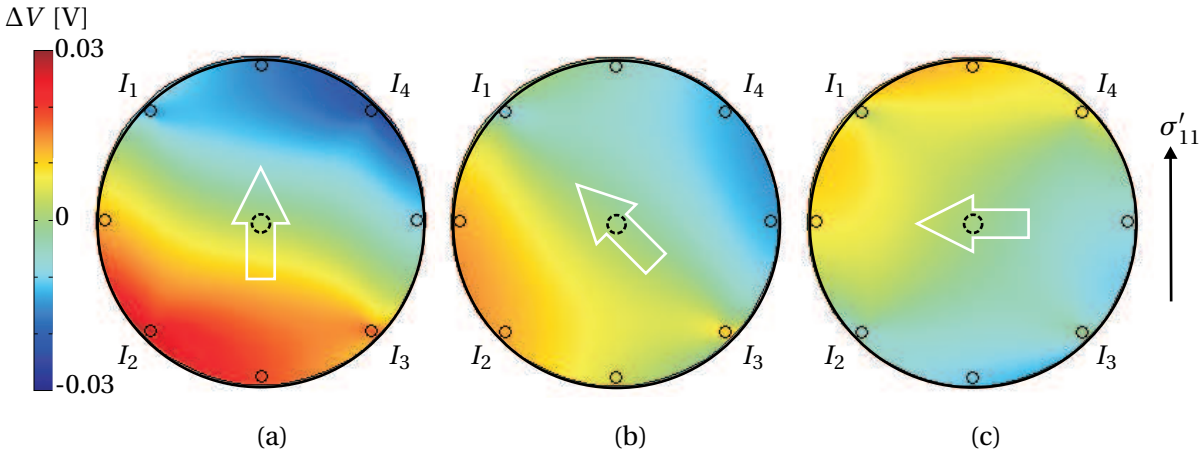


Figure 6.3: FEM of potential difference $\Delta V = V(\sigma'_{ij} = 0) - V(\sigma'_{11} = 50\ \text{MPa})$ in the circular piezoresistor when the current density vector (white arrow) is (a) directed along the stress direction, (b) rotated by $\frac{\pi}{4}$ with respect to the stress direction and (c) rotated by $\frac{\pi}{2}$ with respect to the stress direction. The dashed circles indicate the placement of the inner contacts. The stress direction is described by $\phi = \frac{\pi}{8}$ with respect to the [100] direction. In the 2D simulation the resistivity is defined as written in Eq. (6.8) with $\rho_0 = 1$ and the current is injected from the point sources in units of A/m as $I_3 = -I_1 = \cos(\frac{\pi}{4} - \varphi)$, $I_2 = -I_4 = \sin(\frac{\pi}{4} - \varphi)$. The asymmetry of the potential in the resistor is a result of the anisotropic resistivity tensor.

$CF_{\parallel,0}$	$CF_{\parallel,1}$	$CF_{\parallel,2}$	$CF_{\perp,1}$	$CF_{\perp,2}$
1.00	1.45	0.50	0.50	1.45

Table 6.1: The correction factors defined in Eq. (6.9) determined by FEM. The results from the FEM shows no significant changes when the correction factors are rounded to two decimals.

adopted in the FEM structure. The chosen design of the inner contacts (which have a radius of 3 μm and are placed in a radius of 100 μm from the resistor center) does not contribute significantly to the current density vector. This has been verified in the FEM analysis and in the following the contacts are assumed to be point contacts for simplicity. Fig. 6.3 illustrates the potential difference in the resistor $\Delta V = V(\sigma'_{ij} = 0) - V(\sigma'_{11} = 50\ \text{MPa})$ for different current density directions. The asymmetric behavior confirms the anisotropic properties of the resistivity tensor.

Due to the anisotropic resistivity tensor in Eq. (6.8) the current density vector in the circular resistor does not behave completely as the ideal situation derived in Eq. (6.6) where the current density is unidirectional. Inspired by Ref. [19] correction factors are inserted in the equation in order to compensate for this. These correction factors are found from the FEM analysis. Eq. (6.6)

is thus modified to

$$\begin{aligned}\frac{\Delta V_\parallel}{V_{\parallel,0}} = \quad & CF_{\parallel,0}\left(\sigma'_{11}+\sigma'_{22}+\sigma'_{33}\frac{2\pi_{12}}{\pi_{11}+\pi_{12}}\right)\frac{\pi_{11}+\pi_{12}}{2} \\ & +CF_{\parallel,1}\cos(2\varphi)\left[\left(\sigma'_{11}-\sigma'_{22}\right)\frac{\pi_{11}-\pi_{12}+\pi_{44}}{4}+\sigma'_{12}\frac{-\pi_{11}+\pi_{12}+\pi_{44}}{2}\right] \\ & +CF_{\parallel,2}\sin(2\varphi)\left[\left(\sigma'_{11}-\sigma'_{22}\right)\frac{-\pi_{11}+\pi_{12}+\pi_{44}}{4}+\sigma'_{12}\frac{\pi_{11}-\pi_{12}+\pi_{44}}{2}\right] \qquad (6.9)\end{aligned}$$

$$\begin{aligned}\frac{V_\perp}{V_{\parallel,0}} = \quad & CF_{\perp,1}\cos(2\varphi)\left[\left(\sigma'_{11}-\sigma'_{22}\right)\frac{\pi_{11}-\pi_{12}-\pi_{44}}{4}+\sigma'_{12}\frac{-\pi_{11}+\pi_{12}-\pi_{44}}{2}\right] \\ & CF_{\perp,2}\sin(2\varphi)\left[\left(\sigma'_{11}-\sigma'_{22}\right)\frac{\pi_{11}-\pi_{12}+\pi_{44}}{4}+\sigma'_{12}\frac{-\pi_{11}+\pi_{12}+\pi_{44}}{2}\right],\end{aligned}$$

where $CF_{\parallel,0}$, $CF_{\parallel,1}$, $CF_{\parallel,2}$, $CF_{\perp,1}$, and $CF_{\perp,2}$ are the correction factors. The correction factors determined by FEM are listed in Table 6.1 and have been found using the following approach: In the FEM the piezocoefficients and the stress distribution are defined and the current is rotated in steps of 5° while the four inner potential drops are extracted and $V_\parallel$ and $V_\perp$ are calculated for each current density direction. The results of $\frac{\Delta V_\parallel}{V_{\parallel,0}}$ and $\frac{V_\perp}{V_{\parallel,0}}$ from the FEM analysis are then compared to the expected analytical results from Eq. (6.6). If the current density is varied in steps of 5° the overdetermined linear equation system for $\frac{\Delta V_\parallel}{V_{\parallel,0}}$ is written as

$$\begin{bmatrix} \left.\frac{\Delta V_\parallel}{V_{\parallel,0}}\right|_{\mathrm{FEM}}(\varphi=0°) \\ \left.\frac{\Delta V_\parallel}{V_{\parallel,0}}\right|_{\mathrm{FEM}}(\varphi=5°) \\ \vdots \\ \left.\frac{\Delta V_\parallel}{V_{\parallel,0}}\right|_{\mathrm{FEM}}(\varphi=355°) \end{bmatrix} = \begin{bmatrix} a(\varphi=0°) & b(\varphi=0°) & c(\varphi=0°) \\ a(\varphi=5°) & b(\varphi=5°) & c(\varphi=5°) \\ \vdots & \vdots & \vdots \\ a(\varphi=355°) & b(\varphi=355°) & c(\varphi=355°) \end{bmatrix} \cdot \begin{bmatrix} CF_{\parallel,0} \\ CF_{\parallel,1} \\ CF_{\parallel,2} \end{bmatrix}, \qquad (6.10)$$

where

$$\begin{aligned} a(\varphi)=&\left(\sigma'_{11}+\sigma'_{22}+\sigma'_{33}\frac{2\pi_{12}}{\pi_{11}+\pi_{12}}\right)\frac{\pi_{11}+\pi_{12}}{2} \\ b(\varphi)=&\cos(2\varphi)\left[\left(\sigma'_{11}-\sigma'_{22}\right)\frac{\pi_{11}-\pi_{12}+\pi_{44}}{4}+\sigma'_{12}\frac{-\pi_{11}+\pi_{12}+\pi_{44}}{2}\right] \qquad (6.11) \\ c(\varphi)=&\sin(2\varphi)\left[\left(\sigma'_{11}-\sigma'_{22}\right)\frac{-\pi_{11}+\pi_{12}+\pi_{44}}{4}+\sigma'_{12}\frac{\pi_{11}-\pi_{12}+\pi_{44}}{2}\right]. \end{aligned}$$

The correction factors are determined through a least squares fit of the results from the FEM to the analytical expression. The correction factors for $\frac{V_\perp}{V_{\parallel,0}}$ are found using the same approach. The corrections factors do not change significantly when performing the above analysis for different stress distributions and stress magnitudes in the FEM.

When the correction factors are determined the relation between the piezocoefficients, the stress and the fictive potential drops is known and the device can be used to measure the piezocoefficients when applying a known stress to the device.

6.4 Piezocoefficient mapping device

Once the correction factors have been determined, the circular structure can be used to analyze the piezoresistance properties of the resistor material and to determine all three piezocoefficients

using only one chip. The 4PB fixture described in App. B.2 is used for this purpose. The fixture applies a uniaxial stress σ'_{11} to the chip. By isolating the piezocoefficients in Eq. (6.9) and by applying a uniaxial stress σ'_{11} to the resistor, the fictive potential drops are

$$\begin{aligned}\frac{\Delta V_\parallel}{V_{\parallel,0}} = \quad & \pi_{11}[2\cdot CF_{\parallel,0} + CF_{\parallel,1}\cos(2\varphi) - CF_{\parallel,2}\sin(2\varphi)]\frac{\sigma'_{11}}{4} \\ & \pi_{12}[2\cdot CF_{\parallel,0} - CF_{\parallel,1}\cos(2\varphi) + CF_{\parallel,2}\sin(2\varphi)]\frac{\sigma'_{11}}{4} \\ & \pi_{44}[CF_{\parallel,1}\cos(2\varphi) + CF_{\parallel,2}\sin(2\varphi)]\frac{\sigma'_{11}}{4} \\ \frac{V_\perp}{V_{\parallel,0}} = \quad & (\pi_{11}-\pi_{12})[CF_{\perp,1}\cos(2\varphi) + CF_{\perp,2}\sin(2\varphi)]\frac{\sigma'_{11}}{4} \\ & \pi_{44}[-CF_{\perp,1}\cos(2\varphi) + CF_{\perp,2}\sin(2\varphi)]\frac{\sigma'_{11}}{4}.\end{aligned} \tag{6.12}$$

It is seen that for $\frac{\Delta V_\parallel}{V_{\parallel,0}}$ it is possible to create a linear system with three independent equations, thus all three piezocoefficients can be determined. By using the equations for $\frac{V_\perp}{V_{\parallel,0}}$ only $(\pi_{11}-\pi_{12})$ and π_{44} can be determined. The piezocoefficients are found using the same least squares fit approach as used in the previous section when the correction factors were found. The linear system of $\frac{\Delta V_\parallel}{V_{\parallel,0}}$ is written as

$$\begin{bmatrix} \frac{\Delta V_\parallel}{V_{\parallel,0}}(\varphi=0°) \\ \frac{\Delta V_\parallel}{V_{\parallel,0}}(\varphi=5°) \\ \vdots \\ \frac{\Delta V_\parallel}{V_{\parallel,0}}(\varphi=355°) \end{bmatrix} = \begin{bmatrix} d(\varphi=0°) & e(\varphi=0°) & f(\varphi=0°) \\ d(\varphi=5°) & e(\varphi=5°) & f(\varphi=5°) \\ \vdots & \vdots & \vdots \\ d(\varphi=355°) & e(\varphi=355°) & f(\varphi=355°) \end{bmatrix} \cdot \begin{bmatrix} \pi_{11} \\ \pi_{12} \\ \pi_{44} \end{bmatrix}, \tag{6.13}$$

where $\frac{\Delta V_\parallel}{V_{\parallel,0}}$ are measured values, and

$$\begin{aligned} d(\varphi) &= [2\cdot CF_{\parallel,0} + CF_{\parallel,1}\cos(2\varphi) - CF_{\parallel,2}\sin(2\varphi)]\frac{\sigma'_{11}}{4} \\ e(\varphi) &= [2\cdot CF_{\parallel,0} - CF_{\parallel,1}\cos(2\varphi) + CF_{\parallel,2}\sin(2\varphi)]\frac{\sigma'_{11}}{4} \\ f(\varphi) &= [CF_{\parallel,1}\cos(2\varphi) + CF_{\parallel,2}\sin(2\varphi)]\frac{\sigma'_{11}}{4}. \end{aligned} \tag{6.14}$$

The extracted piezocoefficients are shown in Table 6.2. The doping concentration of the resistor is approximately $N_D = 10^{18}$ cm^{-3} and the values of π_{11}, π_{12}, and π_{44} are in good agreement with the results presented in Fig. 5.6 on page 68, since the values of π_{11} and π_{12} are in between the piezocoefficient values obtained with doping concentrations of $N_D = 5.1\cdot 10^{17}$ cm^{-3} and $N_D = 5\cdot 10^{18}$ cm^{-3} and π_{44} has approximately the same value for all doping concentrations.

In Fig. 6.4 a polar plot of the measurements compared to the results from the FEM is shown. The measurements are in very good agreement with FEM for both $V_\parallel$ and $V_\perp$. The FEM is performed with the measured values of the piezocoefficients in Table 6.2, which have been extracted by the use of Eq. (6.13), and a measured applied uniaxial stress $\sigma'_{11} = 54.7$ MPa. The FEM and the measured values verify that the analytical expression can be corrected by the correction factors in order to obtain the results from the FEM. The polar plots are excellent plots for comparison of different materials and additionally an extraction of all three piezocoefficients is possible. In the future characterization of the piezoresistance properties of materials the extracted piezocoefficients from this structure are to be compared to the more accurate measurements which are performed on two chips as discussed in Sec. 3.3.1.

Since the piezocoefficients have been determined the device can now be used to measure the stress distribution in the chip. In the next section the preliminary work on this approach is described.

π_{11}	π_{12}	π_{44}
$-90\cdot10^{-11}$ Pa^{-1}	$42\cdot10^{-11}$ Pa^{-1}	$-12.5\cdot10^{-11}$ Pa^{-1}

Table 6.2: Measured piezocoefficients in n-type silicon with a doping concentration of $N_D \approx 10^{18}$ cm^{-3} by using one circular piezoresistor. An approximate comparison of these measurements to the results in Sec. 5.3 can be obtained by linear interpolation of the piezocoefficients of the doping concentrations $N_D = 5.1\cdot10^{17}$ cm^{-3} and $N_D = 5\cdot10^{18}$ cm^{-3} at $T = 30$°C. Using this simple approximation the expected piezocoefficient values are: $\pi_{11} \approx \frac{-95-78}{2} \approx -87\cdot10^{-11}$ Pa^{-1}, $\pi_{12} \approx 40\cdot10^{-11}$ Pa^{-1}, and $\pi_{44} \approx -12\cdot10^{-11}$ Pa^{-1}. These interpolated values are in good agreement with the values extracted from the circular resistor.

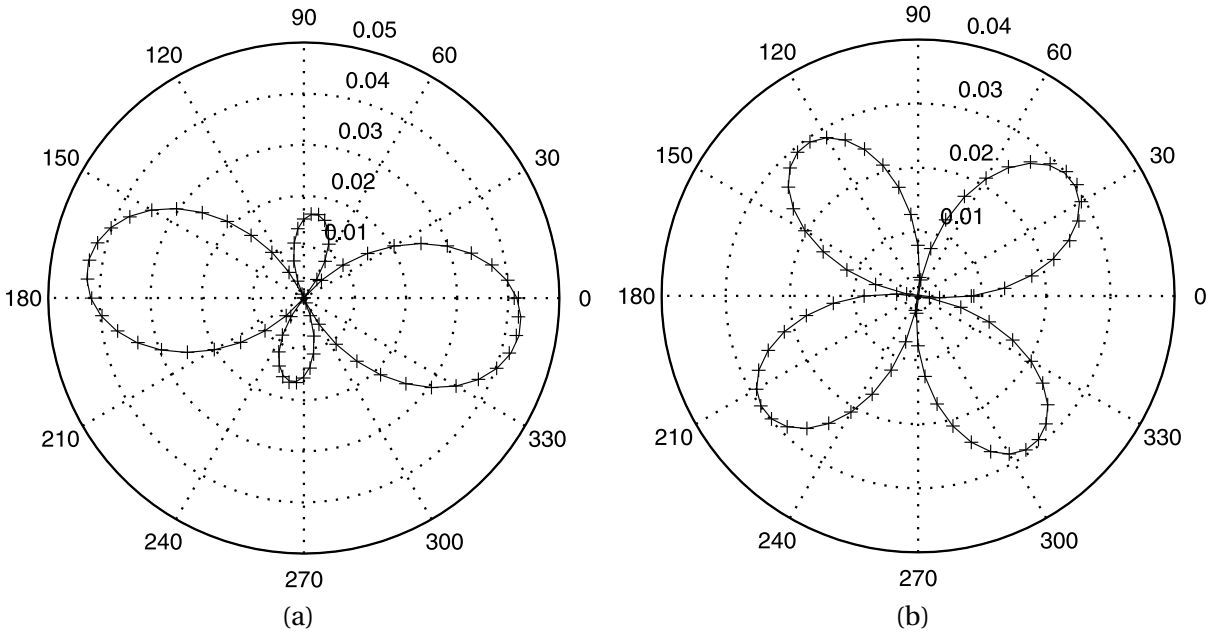


Figure 6.4: Measured values (+ symbols) of (a) $\frac{\Delta V_\parallel}{V_{\parallel,0}}$ and (b) $\frac{V_\perp}{V_{\parallel,0}}$ compared to the expected values from FEM (solid line). In the FEM analysis the extracted piezocoefficients from the measurement presented in Table 6.2 and the measured stress of $\sigma'_{11} = 54.7$ MPa are used. The shape of the polar plots verifies the agreement between the analytical expression when including the extracted values of the correction factors and the FEM.

6.5 Stress measurement

In this section the results of the piezocoefficients from the above measurements are used to determine the stress distribution in the resistor when the resistor is exposed to a multi-directional stress. By using the circular resistor as a stress sensor many applications are possible, of which realtime on-chip stress measurements during the curing of an epoxy packaging will be presented as an example of use in this section. Since the piezocoefficients vary as a function of doping concentration as shown in Sec. 5.3 the piezocoefficient values can vary between different batches. Thus, it is important in terms of the accuracy of the device that the piezocoefficients are measured prior to the determination of the stress. The circular resistor allows for this calibration step which is performed as presented above. In order to measure the stress in the chip, the stress components are

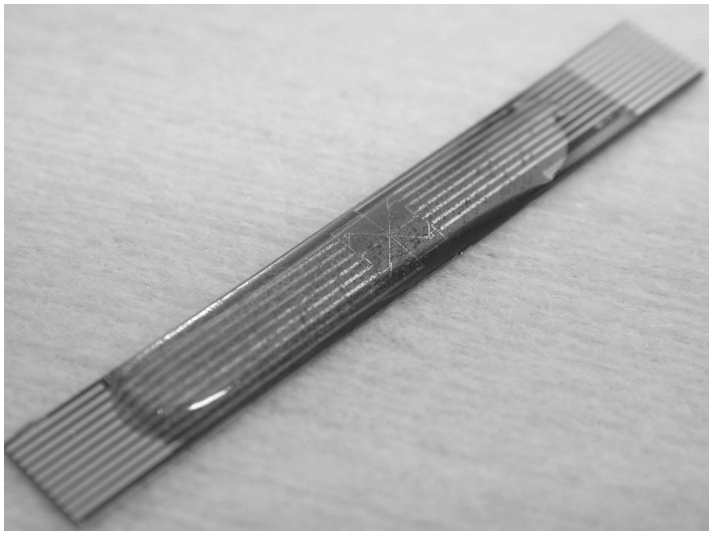


Figure 6.5: Cured two component epoxy on the resistor and chip. As a proof of concept the stress induced by a two component epoxy [76] is measured by the circular resistor during the curing of the epoxy.

isolated in Eq. (6.9) and the obtained linear system is thus

$$\begin{bmatrix} \frac{\Delta V_\parallel}{V_{\parallel,0}}(\varphi=0°) \\ \frac{\Delta V_\parallel}{V_{\parallel,0}}(\varphi=5°) \\ \vdots \\ \frac{\Delta V_\parallel}{V_{\parallel,0}}(\varphi=355°) \end{bmatrix} = \begin{bmatrix} g(\varphi=0°) & h(\varphi=0°) & i(\varphi=0°) \\ g(\varphi=5°) & h(\varphi=5°) & i(\varphi=5°) \\ \vdots & \vdots & \vdots \\ g(\varphi=355°) & h(\varphi=355°) & i(\varphi=355°) \end{bmatrix} \cdot \begin{bmatrix} \left(\sigma'_{11}+\sigma'_{22}+\sigma'_{33}\frac{2\pi_{12}}{\pi_{11}+\pi_{12}}\right) \\ \sigma'_{11}-\sigma'_{22} \\ \sigma'_{12} \end{bmatrix}, \tag{6.15}$$

where $\frac{\Delta V_\parallel}{V_{\parallel,0}}$ are measured values, and

$$\begin{aligned} g(\varphi) &= CF_{\parallel,0}\frac{\pi_{11}+\pi_{12}}{2} \\ h(\varphi) &= CF_{\parallel,1}\cos(2\varphi)\frac{\pi_{11}-\pi_{12}+\pi_{44}}{4} + CF_{\parallel,2}\sin(2\varphi)\frac{-\pi_{11}+\pi_{12}+\pi_{44}}{4} \\ i(\varphi) &= CF_{\parallel,1}\cos(2\varphi)\frac{-\pi_{11}+\pi_{12}+\pi_{44}}{2} + CF_{\parallel,2}\sin(2\varphi)\frac{\pi_{11}-\pi_{12}+\pi_{44}}{2}. \end{aligned} \tag{6.16}$$

Similar equations are obtained for $\frac{V_\perp}{V_{\parallel,0}}$. The overdetermined linear equation system is solved for the three stress combinations in Eq. (6.15), i.e. $\left(\sigma'_{11}+\sigma'_{22}+\sigma'_{33}\frac{2\pi_{12}}{\pi_{11}+\pi_{12}}\right)$, $(\sigma'_{11}-\sigma'_{22})$, and σ'_{12}. If $\sigma'_{33}=0$ the method allows determination of all three in-plane stress components by using the measurements from $\frac{V_\parallel}{V_{\parallel,0}}$. The measurements from $\frac{V_\perp}{V_{\parallel,0}}$ allows for determination of $(\sigma'_{11}-\sigma'_{22})$, and σ'_{12}.

In this proof of concept experiment a two component epoxy [76] is deposited on top of the chip, see Fig. 6.5. The epoxy has a curing time of approximately 24 hours. In order to measure the stress in the resistor during the curing of the epoxy $V_\parallel$ and $V_\perp$ are continuously measured on the resistor until curing is reached. The extracted stress components are shown in Fig. 6.6 when using the measurements from both $\frac{\Delta V_\parallel}{V_{\parallel,0}}$ and $\frac{V_\perp}{V_{\parallel,0}}$. It is seen that the extracted stress components from $\frac{\Delta V_\parallel}{V_{\parallel,0}}$ have a much smaller signal to noise ratio compared to the extracted stress components

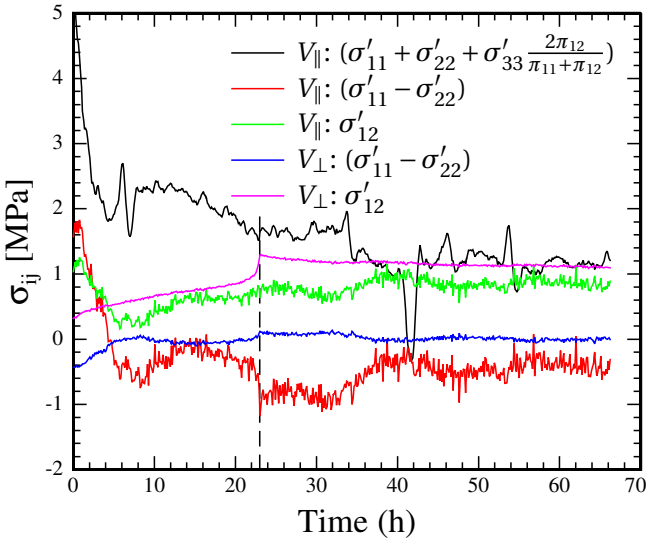


Figure 6.6: Preliminary results of extracted stress components while curing of a two component epoxy [76]. The stress components are extracted from measurements of $\frac{\Delta V_\parallel}{V_{\parallel,0}}$ and $\frac{V_\perp}{V_{\parallel,0}}$. It is seen that the stress components extracted from $\frac{\Delta V_\parallel}{V_{\parallel,0}}$ fluctuate much more than the components extracted from $\frac{V_\perp}{V_{\parallel,0}}$. In the beginning of the measurement the stress components extracted from $\frac{\Delta V_\parallel}{V_{\parallel,0}}$ are much larger than the stress components extracted from $\frac{V_\perp}{V_{\parallel,0}}$. These signals and the larger fluctuations of $\frac{\Delta V_\parallel}{V_{\parallel,0}}$ are most likely caused by temperature variations in the chip. From the measurements of $\frac{V_\perp}{V_{\parallel,0}}$ a curing time of 23 hours is found (indicated by the dashed line). The signal from $\frac{V_\perp}{V_{\parallel,0}}$ is not changing significantly after curing is reached. These preliminary results show that some optimization still need to be performed in order for this device to function properly as a stress sensor.

	$\left(\sigma'_{11}+\sigma'_{22}+\sigma'_{33}\frac{2\pi_{12}}{\pi_{11}+\pi_{12}}\right)$	$\sigma'_{11}-\sigma'_{22}$	σ'_{12}
$\frac{\Delta V_\parallel}{V_{\parallel,0}}$	1.2 MPa ± 0.07 MPa	-0.5 MPa ± 0.4 MPa	0.8 MPa ± 0.2 MPa
$\frac{V_\perp}{V_{\parallel,0}}$	-	0.02 MPa ± 0.08 MPa	1.1 MPa ± 0.04 MPa

Table 6.3: Measured stress components in the resistor with a cured two component epoxy on the top surface. The values obtained from the measurement of $\frac{V_\perp}{V_{\parallel,0}}$ are temperature compensated and are thus considered to be more reliable than the values obtained from $\frac{\Delta V_\parallel}{V_{\parallel,0}}$. The variation of the extracted stress components show that more work need to done in order to obtain a reliable stress measurement with identical results from the two measurements methods.

from $\frac{\Delta V_\perp}{V_{\parallel,0}}$. The fluctuations of the signal is approximately ±150 kPa. If these fluctuations are a result of temperature fluctuations the temperature change is $\Delta T \approx 0.1$°C when the estimated values described in Sec. 6.2 are used. In the setup used for this preliminary experiment such temperature fluctuations are expected. Furthermore it is seen that the stress components measured by $\frac{\Delta V_\parallel}{V_{\parallel,0}}$ are large from the beginning and then decreases with time until an equilibrium is reached. This might also be explained by temperature variation, since only a few degrees of difference between epoxy

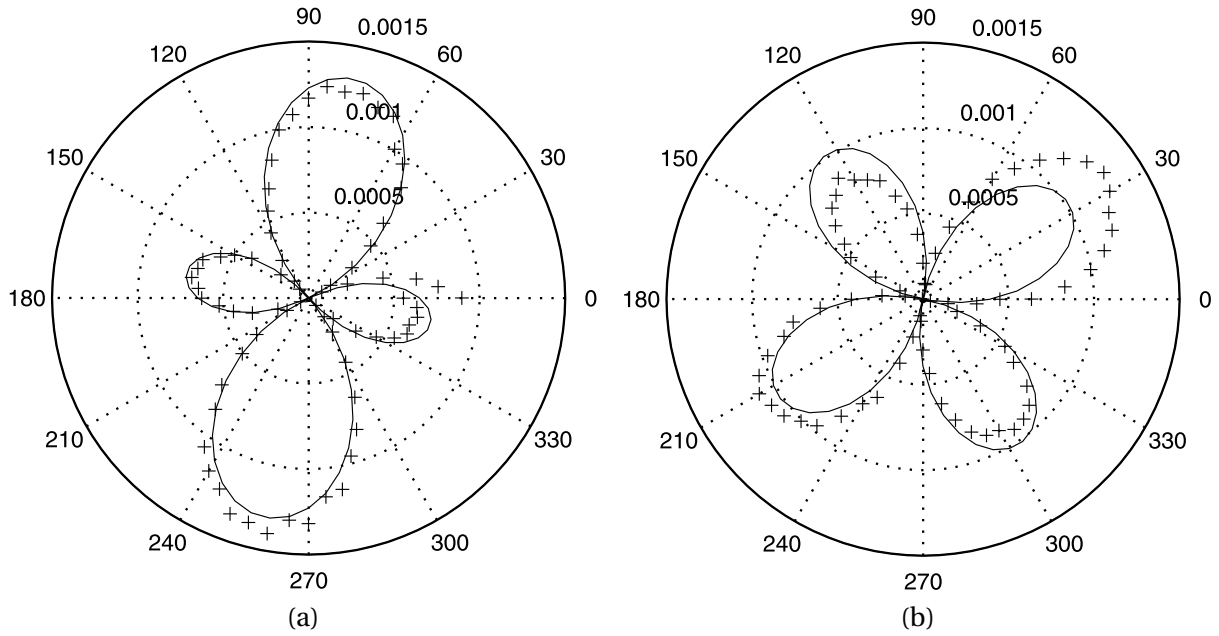


Figure 6.7: Preliminary stress sensing. The measured values (+ symbols) of (a) $\frac{\Delta V_\parallel}{V_{\parallel,0}}$ and (b) $\frac{V_\perp}{V_{\parallel,0}}$ in the resistor after the epoxy is cured. The stress is calculated by Eq. (6.15) and inserted in the FEM. The results from the FEM (solid line) are also shown for comparison. In the FEM the stress values extracted from $\frac{V_\perp}{V_{\parallel,0}}$ are used for σ'_{12} and $\sigma'_{11}-\sigma'_{22}$ and the stress values of $(\sigma'_{11}+\sigma'_{22}+\sigma'_{33}\frac{2\pi_{12}}{\pi_{11}+\pi_{12}})$ are taken from the measurement of $\frac{\Delta V_\parallel}{V_{\parallel,0}}$. The values are listed in Table 6.3. The shape of the curves show that the measurement to some extend agree with FEM.

and chip will cause the curves to behave as shown. Additionally, the epoxy temperature changes during the curing due to the chemical process and this will also effect the measurement. The large stress values obtained in the beginning of the measurement is not observed when the temperature compensated measurement of $\frac{V_\perp}{V_{\parallel,0}}$ is used, and the signal to noise ratio of this measurement is significantly smaller than the measurement of $\frac{\Delta V_\parallel}{V_{\parallel,0}}$. Thus, the measurement of $\frac{\Delta V_\parallel}{V_{\parallel,0}}$ is most likely influenced by temperature variation. From the measurement of $\frac{V_\perp}{V_{\parallel,0}}$ the curing time is determined to be approximately 23 hours, since there is no significant changes in the signals thereafter. The signal changes very slowly after 23 hours which indicates that a slight relaxation might occur. The extracted stress components after curing are listed in Table 6.3. From this table it is seen that depending on which potential drop is used for the measurement different stress values are obtained. The most reliable measurement of the two is considered to be $\frac{V_\perp}{V_{\parallel,0}}$ since this measurement is temperature compensated.

The results from the last measurement are compared with the results from FEM. In the FEM the measured piezocoefficient values from Table 6.2 and the stress values obtained from the measurement listed in Table 6.3 are used. The extracted values of σ'_{12} and $(\sigma'_{11}-\sigma_{22})$ from the measurement of $\frac{V_\perp}{V_{\parallel,0}}$ are used (since this is the measurement that is considered to be the most reliable) and the extracted value of $(\sigma'_{11}+\sigma'_{22}+\sigma'_{33}\frac{2\pi_{12}}{\pi_{11}+\pi_{12}})$ is used from the measurement of $\frac{\Delta V_\parallel}{V_{\parallel,0}}$. The results are shown in Fig. 6.7. The measurements do to some extend agree with FEM, but are far from the excellent results obtained in Fig. 6.4. Fig. 6.6 and Fig. 6.7 show that there are still room for optimization in order for the circular resistor to operate satisfactory. The challenges in the future optimization are

to solve the following issues. Firstly, the measurements from the two fictive voltage drops should ideally extract the same values of σ'_{12} and $(\sigma'_{11} - \sigma'_{22})$. Secondly, The measured values of $\frac{\Delta V_{\parallel}}{V_{\parallel,0}}$ and $\frac{V_{\perp}}{V_{\parallel,0}}$ do not exactly follow the expected curve from FEM. Thirdly, the temperature dependency of $\frac{\Delta V_{\parallel}}{V_{\parallel,0}}$ results in large fluctuations of the extracted stress values.

In order to solve the above issues the following modifications are suggested. One of the issues could be the size of the resistor with respect to the size of the chip. The surface area of the resistor is very large and the resistor perimeter is not far from the chip edge, thus edge effects from the glue are present in the resistor and the stress in the resistor can not be assumed to be uniform. This can be adjusted by decreasing the size of the resistor. Another issue is that this preliminary test experiment applied a very small stress to the resistor. The largest stress component which was measured was σ'_{12} = 1.1 MPa. In the future experiments it is suggested to develop a calibration setup that applies a controlled non-uniaxial stress of minimum 10 MPa to the chip in order to obtain a larger signal to noise ratio. The temperature dependency of the measurement of $\frac{\Delta V_{\parallel}}{V_{\parallel,0}}$ can be accounted for by implementing an on-chip temperature sensor to monitor the temperature continuously. Furthermore, it is suggested that these experiments are performed such that $\sigma'_{33} = 0$ in order to be able to extract the magnitudes of the three in-plane stress components.

Although the experiment needs to be further optimized, this preliminary test shows that the circular resistor can be used for complex realtime stress measurements. The circular resistor can potentially be used on any chip layout after a calibration of the device, either on chip or separately by another chip from the same batch that fits the calibration setup. However, more work is needed in order to obtain satisfactory stress measurements with this device.

6.6 Summary

In this section the circular resistor has been introduced. The design of the chip and resistor was first presented together with a description of the measurement concept. This was followed by a theoretical derivation which was compared to FEM. From this comparison correction factors were implemented in theoretical equations in order for the analytical expression and FEM to agree. The device was then used as a piezocoefficient mapping device where is was subjected to a uniaxial stress and the three piezocoefficients were determined. The polar plots of the measurement were presented together with the expected values from FEM and these were in excellent agreement. The polar plots offer an excellent visual comparison of the piezoresistance properties of different materials. Finally, the circular resistor was used for sensing stress induced by a curing two component epoxy. This preliminary test showed that the circular resistor potentially can be used for stress sensing, however still some work needs to done.

CHAPTER

7 Conclusion

This thesis is a contribution to the research in piezoresistive MEMS sensors. The major goals of this project were:

- To develop an improved theoretical model that describes the piezoresistance effect in p-type silicon.
- To design, fabricate and characterize a new setup for piezoresistance characterization.
- To design a piezoresistance test chip layout which enables comparison of the piezoresistance effect of different materials.
- To characterize the piezoresistance properties of p- and n-type silicon.
- To modify silicon based materials with the aim to find materials that have larger and less temperature sensitive piezoresistance properties than silicon.

The above goals have all been reached during this project.

The theoretically developed model is an improved model compared to the model by Kanda [31] which is commonly used today. The model calculates the bandstructure of the three upper valence bands in silicon by including both a spin-orbit and a strain pertubation Hamiltonian in the total Hamiltonian. It is found that it is very important to include all contributing scattering effects when calculating the relaxation time. The model results are fitted to a function which can be used by experimentalist in order to predict the temperature and doping concentration dependency of the piezoresistive effect.

A four point bending setup has been designed and fabricated in order to perform high precision characterization of the piezoresistance effect. The setup consists of a motorized actuator and a high sensitivity force sensor which measures the force applied on the dedicated chip inserted in the fixture. The compact setup includes heaters embedded in the housing and thermocouples in order to allow for precise temperature control. The setup applies a uniaxial stress to the inserted chip and provides a high precision measurement of π_{44} in p-type silicon with an uncertainty of 1.8%.

Piezoresistance test chips have been designed with the aim to extract the three piezocoefficients in silicon with the lowest possible uncertainty. The piezocoefficient π_{44} is determined with the lowest uncertainty if the uniaxial stress is applied along the [110] direction and the resistors are placed parallel to and perpendicular to [110]. The piezocoefficients π_{11} and π_{12} are determined

with the lowest uncertainty if the uniaxial stress is applied along the [100] crystal direction and the resistors are placed parallel to and perpendicular to the [100] direction, respectively.

A piezocoefficient mapping device has been designed with the main aim to compare the piezoresistance properties of different materials by using only one chip. The chip consists of only one circular resistor and in n-type silicon the chip enables extraction of all three piezocoefficients. The chip can potentially also operate as a stress sensor. Preliminary test results of this use has been presented.

The piezoresistance test chips have been fabricated in the cleanroom facility at Danchip, DTU. For this purpose a general process sequence has been developed. The fabrication of the chips with different test materials follow the general process sequence with few modifications depending on the specific test material properties.

The piezoresistance properties of p- and n-type silicon have been characterized as a function of temperature and doping concentration. In p-type silicon the piezocoefficient π_{44} is determined in piezoresistors with both a uniform doping profile and a Gaussian doping profile. The results show that π_{44} decreases with increasing doping concentration and that the temperature dependency of π_{44} also decreases with increasing doping concentration. In a piezoresistor with a Gaussian profile and peak doping concentration of $N_A = 9 \cdot 10^{17}$ cm^{-3}, $\pi_{44} = 119 \cdot 10^{-11}$ Pa^{-1} at room temperature and π_{44} decreases 18% when the temperature is increased to 85°C. In a uniformly doped piezoresistor with $N_A = 1.5 \cdot 10^{17}$ cm^{-3}, $\pi_{44} = 118 \cdot 10^{-11}$ Pa^{-1} at $T = 30$°C. The obtained values are more than 14% smaller than the value $\pi_{44} = 138.1 \cdot 10^{-11}$ Pa^{-1} which was measured by Smith [21] and is the most commonly used value in literature when the piezoresistive properties of silicon MEMS devices are to be predicted. In the light of the piezoresistance characterization of p-type silicon it is suggested to use the values obtained in the results section in this thesis instead of the larger value obtained by Smith in order to obtain a more reliable prediction of the piezoresistance properties of the MEMS device.

In n-type silicon π_{11}, π_{12}, and π_{44} have been found as functions of doping concentration and temperature. The piezocoefficient π_{11} is highly dependent on both doping concentration and temperature, at room temperature $\pi_{11} = -97 \cdot 10^{-11}$ Pa^{-1} in a Gaussian doping profile piezoresistor with a doping concentration of $N_D = 5.1 \cdot 10^{17}$ cm^{-3}. This value numerically decreases with 16% when the temperature is increased to 80°C. In a piezoresistor with a Gaussian doping profile and a peak doping concentration of $N_D = 5.1 \cdot 10^{17}$ cm^{-3} the piezocoefficient π_{12} at room temperature is determined as $\pi_{12} = 43 \cdot 10^{-11}$ Pa^{-1}. This piezocoefficient decreases with increasing doping concentration but it has a very small temperature dependency. The piezocoefficient $\pi_{44} = -12 \cdot 10^{-11}$ Pa^{-1} showed no measurable dependency on doping concentration and temperature. The extracted piezocoefficients for the lowest doping concentration are in good agreement with the most commonly used values measured by Smith [21].

The piezoresistance properties of molecular beam epitaxially grown tensile strained Si and compressive strained $Si_{0.9}Ge_{0.1}$ have been characterized as functions of temperature and crystal strain. For compressive strained $Si_{0.9}Ge_{0.1}$ ($\epsilon = -0.004$) at room temperature in a piezoresistor with a uniform doping concentration of $N_A = 1.6 \cdot 10^{18}$ cm^{-3} the piezocoefficient π_{66} is found to be $\pi_{66} = 136 \cdot 10^{-11}$ Pa^{-1}, which is an increase of 36% in the piezoresistance properties compared to what is measured in silicon. The piezocoefficient π_{66} in tensile strained Si ($\epsilon = 0.004$) is decreased by 25% compared to the equivalent piezocoefficient π_{44} in silicon. The temperature dependency of π_{66} in tensile strained silicon is smaller than that of π_{44} in silicon. The value of π_{66} in tensile strained Si ($\epsilon = 0.004$) was shown to decrease 6% when increasing the temperature from 30°C to 81°C. In the same temperature range π_{44} in silicon decreased 18%. Finally, it was shown that π_{66}

in compressive strained $Si_{0.9}Ge_{0.1}$ is highly dependent on the doping concentration. The value of π_{66} decreases by 38% when increasing the doping concentration from $N_A = 1.6 \cdot 10^{18}$ cm^{-3} to $N_A = 1.7 \cdot 10^{19}$ cm^{-3}. The increase of the piezoresistance effect in compressive strained silicon can be used to increase the sensitivity of the MEMS device. The decrease in the temperature dependency of π_{66} in tensile strained silicon suggests the use of strained layers in MEMS which are exposed to large temperature variations.

The piezoresistance of p-type crystalline and polycrystalline silicon nanowires have been characterized as a function of doping concentration and nanowire width. The results show that for low doping concentration the piezocoefficient increases when decreasing the width. In a silicon nanowire of width 140 nm (thickness 200 nm) and $N_A = 1.5 \cdot 10^{17}$ cm^{-3} the piezocoefficient π_{44} was measured to be $\pi_{44} = 910 \cdot 10^{-11}$ Pa^{-1}. The large ratio between surface states and carriers in the nanowire is expected to cause this increase. The value of π_{44} is decreased as doping concentration is increased. In silicon nanowires with a very high doping concentration $N_A = 1.2 \cdot 10^{20}$ cm^{-3}, π_{44} is unchanged if the width is larger than 100 nm and π_{44} rapidly decreases and approaches zero if the width is smaller than 100 nm. This effect may be due to boundary scattering in the nanowire. In polycrystalline nanowires the piezocoefficient is seen to increase when decreasing the width. The piezocoefficient in a polysilicon nanowire with a resistivity of $\rho = 0.15$ Ωcm is increased by 40% in a nanowire of width 100 nm compared to a micrometer scaled polysilicon piezoresistor. The measurements on p-type silicon nanowires show that the piezoresistance increases significantly when decreasing the nanowire size. This discovery may be used in future NEMS and MEMS in order to increase the sensitivity significantly. In particular, the highly sensitive nanowires may be used in biomedical sensors where high sensitivity is needed. Furthermore, the increase of 40% in the piezoresistance properties of the polycrystalline silicon nanowires may also be used for biomedical sensing to increase the sensitivity significantly where substrates other than silicon (e.g. cantilevers consisting of silicon nitride films) are used.

This thesis has provided new knowledge to the field of piezoresistive MEMS and NEMS and improved the understanding of piezoresistivity in general. The thesis proofs that it is possible to manipulate crystal structures in order to obtain a larger piezoresistance effect and to decrease the temperature dependency. The results obtained in this thesis may by used as building blocks towards a new MEMS and NEMS generation of highly sensitive piezoresistive sensors.

Bibliography

[1] Intel. www.intel.com. Internet, 2007.

[2] O.N. Tufte and P.W. Chapman. Silicon diffused-element piezoresistive diaphragms. Journal of Applied Physics, 33, 1962.

[3] M.R. Douglas. DMD reliability: a MEMS success story. Proceedings of SPIE - The International Society for Optical Engineering, 4980:1–11, 2003.

[4] S.E. Alper, K. Azgin, and T. Akin. A high-performance silicon-on-insulator MEMS gyroscope operating at atmospheric pressure. Sensors and Actuators A. Physical, 135:34 Ű 42, 2007.

[5] Inc. Silicon Designs. www.silicondesigns.com. Internet, 2007.

[6] Cantion A/S. www.cantion.com. Internet, 2007.

[7] N. Maluf, I. Dale, A. Gee, K.E. Petersen, and G.T.A. Kovacs. Medical applications of MEMS. WESCON/95. Conf. Proc. 'Microelectronics Communications Technology Producing Quality Products Mobile and Portable Power Emerging Technologies', page 300, 1995.

[8] A.C.R. Grayson, R.S. Shawgo, A.M. Johnson, N.T. Flynn, Y. Li, M.J. Cima, and R. Langer. A bioMEMS review: MEMS technology for physiologically integrated devices. Proc. of the IEEE, 92(1):6–21, 2004.

[9] J. Thaysen. Cantilever-based bio-chemical sensor integrated in a microliquid handling system. MEMS 2001. Proceedings of the 14th IEEE International Conference on Micro Electro Mechanical Systems, 1:401–404, 2001.

[10] H. Jung. Design of smart piezoresistive pressure sensor. Science and Technology 2001, 1:202–205, 2001.

[11] J. Bartholomeyczik, S. Brugger, P. Ruther, and O. Paul. Multidimensional cmos in-plane stress sensor. IEEE Sensors Journal, 5:872–882, 2005.

[12] Z. Xiao. Silicon micro-accelerometer with mg resolution, high linearity and large frequency bandwidth fabricated with two mask bulk process. Sensors and Actuators: Physical A, 77:113–119, 1999.

[13] S.D. Senturia. Microsystem Design. Kluwer Academic Publishers, 3 edition, 2001.

[14] G. Abagal. electromechanical model of a resonating nano-cantilever-based sensor for high-resolution and high-sensitivity mass detection. Nanotechnology, 12:100–104, 2001.

[15] Grundfos. www.grundfos.com. Internet, 2007.

[16] Autoliv Inc. www.autoliv.com. Internet, 2007.

[17] Infineon Technologies SensoNor A/S. www.sensonor.no. Internet, 2007.

[18] P. Gieschke, J. Richter, J. Joos, P. Ruther, and O. Paul. Four-degree-of-freedom solid state MEMS joystick. Proc. of the IEEE MEMS, 2008.

[19] J. Bartholomeyczik. Advanced CMOS-Based Stress Sensing. PhD thesis, IMTEK, University of Freiburg, 2006.

[20] P. Valdastri, S. Roccella, L. Beccai, E. Cattin, A. Menciassi, M.C. Carrozza, and P. Dario. Characterization of a novel hybrid silicon three-axial force sensor. Sensors and Actuators A. Physical, 123-124:249–257, 2005.

[21] C.S. Smith. Piezoresistance effect in germanium and silicon. Physical Review, 94:42–49, 1954.

[22] J. Thaysen. Cantilever for Bio-Chemical Sensing Integrated in a Microliquid Handling System. PhD thesis, Mikroelektronik Centret, 2001.

[23] R.E. Beaty and R.C. Jaeger. Evaluation of piezoresistive coefficient variation in silicon stress sensors using a four-point bending test fixture. IEEE Transactions on components, hybrids, and manufacturing technology, 15:904–914, 1992.

[24] R.C. Jaeger and J.C. Suhling. A (100) silicon stress test chip with optimized piezoresistive sensor rosettes. IEEE Electronic Components and Technology Conference, 44:741–749, 1994.

[25] E. Lund. Measurement of the temperature dependency of the piezoresistance coefficients in p-type silicon. Advances in Electronic Packaging, 1:215–218, 1999.

[26] R.C. Jaeger and J.C. Suhling. Off-axis sensor rosettes for measurement of the piezoresistive coefficients of silicon. IEEE Transactions on components, hybrids, and manufacturing technology, 16:925–931, 1993.

[27] O.N. Tufte and E.L. Stelzer. Piezoresistive properties of silicon diffused layers. Journal of Applied Physics, 34, 1963.

[28] B.M. Askerov. Electron transport phenomena in semiconductors. World scientific, 1994.

[29] A. F. Kip G. Dresselhaus and C. Kittel. Cyclotron resonance of electrons and holes in silicon and germanium crystals. Physical Review, 98(2):368–384, 1955.

[30] G. E. Pikus and G. L. Bir. Symmetry and Strain-Induced Effects in Semiconductors. Wiley, New York, 1974.

[31] Y. Kanda. A graphical representation of the piezoresistance coefficients in silicon. IEEE Transactions on Electron Devices, pages 64–70, 1982.

[32] E.V. Thomsen. $Si_{1-x}Ge_x$ strained epitaxial films on Silicon for Heterojunction Bipolar Transistors. PhD thesis, Mikroelektronik Centret, 1998.

[33] T. Manku. Valence energy-band structure for strained group-iv semiconductors. Journal of Applied Physics, 73:1205–1212, 1993.

[34] G. Theodorou. Structural, electronic, and optical properties of strained $si_{1-x}ge_x$ alloys. Physical Review B (Condensed Matter), 50:18355–18359, 1994.

[35] J.L Hoyt and H.M. Nayfeh. Strained silicon mosfet technology. Electron Devices Meeting, 2002. IEDM '02. International, pages 23–26, 2002.

[36] R. He and P. Yang. Giant piezoresistance effect in silicon nanowires. Nature nanotechnology, 1(1):42–46, October 2006.

[37] J.X. Cao, X.G. Gong, and R.Q. Wu. Giant piezoresistance and its origin in si(111) nanowires: First-principles calculations. Physical Review B, 75(23):233302.1–233302.4, June 2007.

[38] T. Toriyama and D. Funai S. Sugiyama. Piezoresistance measurement on single crystal silicon nanowires. J. Appl. Phys., 93(1):561–565, January 2003.

[39] T. Toriyama and S. Sugiyama. Single crystal silicon piezoresistive nano-wire bridge. Sensors and Actuators, 108:244–249, April 2003.

[40] A.T. Tilke, F.C. Simmel, H. Lorenz, R.H. Blick, and J.P. Kotthaus. Quantum interference in a one-dimensional silicon nanowire. Physical Review B, 68:075311.1–075311.6, August 2003.

[41] S.Y. Chou, P.R. Krauss, and P.J. Renstrom. Imprint of sub-25 nm vias and trenches in polymers. Applied Physics Letters, 67(21):3114–3116, November 1995.

[42] S.Y. Chou, P.R. Krauss, W. Zhang, L. Guo, and L. Zhuang. Sub-10 nm imprint lithography and applications. Journal of Vacuum Science and Technology, 15(6):2897–2904, Nov/Dec 1997.

[43] Y. Cui, J. Lauhon, M.S. Gudriksen, and J. Wang. Diameter-controlled synthesis of single-crystal silicon nanowires. Applied Physics Letters, 78(15):2214–2216, April 2001.

[44] X.T. Zhou, J.Q. Hu, C.P. Li, D.D.D. Ma, C.S. Lee, and S.T. Lee. Silicon nanowires as chemical sensors. Chemical Physics Letters, 369:220 Ű 224, 2003.

[45] Z. Gao, A. Agarwal, A.D. Trigg, N. Singh, C. Fang, C.-H. Tung, Y. Fan, and K.D. Buddharajuand J. Kong. Silicon nanowire arrays for label-free detection of DNA. Anal. Chem., 79(9):3291–3297, 2007.

[46] I. Park, Z. Li amd X. Li, A.P. Pisano, and R.S Williams. Towards the silicon nanowire-based sensor for intracellular biochemical detection. Biosensors and Bioelectronics, 22:2065 Ű 2070, 2007.

[47] E. Lund and T.G. Finstad. Design and construction of a four-point bending based set-up for measurement of piezoresistance in semiconductors. Rev. Sci. Instrum., 75:4960–4966, 2004.

[48] V. Weihnacht, W. Brückner, and C.M. Schneider. Apparatus for thin-film measurement with integrated four-point bending equipment: Performance and results on Cu films. Rev. Sci. Instrum., 71:4479–4482, 2000.

[49] J. Richter, O. Hansen, A. Nylandsted Larsen, J. Lundsgaard Hansen, G.F. Eriksen, and E.V. Thomsen. Piezoresistance of silicon and strained $Si_{0.9}Ge_{0.1}$. Sensors and Actuators A. Physical, 123, 2005.

[50] W.P. Mason. Physical acoustics and the properties of solids, volume 1. Van Nostrand, Princeton, New Jersey, 1964.

[51] S.P. Timoshenko and J.N. Goodier. Theory of Elasticity. McGraw-Hill, 3 edition, 1970.

[52] J.J. Wortman and R.A. Evans. Young's modulus, shear modulus, and poisson's ratio in silicon and germanium. Journal of Applied Physics, 36, 1965.

[53] L. Onsager. Reciprocal relations in irreversible processes. i. Physical Review, 37:405–426, 1931.

[54] J.F. Nye. Physical Properties of Crystals. Oxford University Press, 1 edition, 1957.

[55] COMSOL. www.comsol.com. Internet, 2007.

[56] J. Richter and K. Wonsyld. Piezo resisitive effect in silicon. MIC - Department of micro and nanotechnology, 2003.

[57] ASTM Designation F723-88. Standard practice for conversion between resistivity and dopant density for boron-doped and phosphorus-doped silicon, 1995.

[58] N. Mingo. Calculation of Si nanowire thermal conductivity using complete phonon dispertion relations. Physical Review B, 68(11):113308, 2006.

[59] D. Li, Y. Wu, P. Kim, L. Shi, P. Yang, and A. Majumdar. Thermal conductivity of individual silicon nanowires. Appl. Phys. Letters, 83(14):2934–2936, 2003.

[60] M. Vangbo and Y. Bäcklund. Precise mask alignment to the crystallographic orientation of silicon wafers using wet anisotropic etching. J. Micromech. Microeng., 6:279–284, 1996.

[61] M.J. Madou. Fundamentals of Microfabrication: The Science of Miniaturization. CRC, 2 edition, 2002.

[62] ACES. http://galaxy.micro.uiuc.edu/research/completed/aces/pages/home.html. Internet, 2007.

[63] D.A. Neamen. Semiconductor Physics and Devices. McGraw-Hill, 3 edition, 2003.

[64] Silvaco Deckbuild. www.silvaco.com. Internet, 2007.

[65] SRIM The Stopping and Range of Ions in Matter. www.srim.org. Internet, 2007.

[66] S.M Sze. Semiconductor Devices - Physics and Technology. John Wiley and Sons, 1 edition, 1985.

[67] J. Richter, M.B. Arnoldus, J. Lundsgaard Hansen, A. Nylandsted Larsen, O. Hansen, and E.V. Thomsen. Piezoresistance in strained silicon and strained silicon germanium. Materials Research Society Symposium Proceedings, 958:133, 2006.

[68] K. Reck, J. Richter, O. Hansen, and E.V. Thomsen. Piezoresistive effect in top-down fabricated silicon nanowires. Proc. of the IEEE MEMS, 2008.

[69] S. Wolf and R.N. Tauber. Silicon processing, volume 1. Lattice Press, 1986.

[70] T. Toriyama, Y. Tanimoto, and S. Sugiyama. Characteristics of silicon nano wire as piezoresistor for nano electro mechanical systems. Proc. of the IEEE MEMS, pages 305–308, 2001.

[71] A. Mian, J.C. Suhling, and R.C. Jaeger. The van der pauw stress sensor. IEEE Sensors Journal, 6, 2006.

[72] J. Richter, A. Hyldgård, K. Birkelund, O. Hansen, and E.V. Thomsen. Realtime 3d stress measurement in curing epoxy packaging. Proc. of Transducers, 2007.

[73] J. Richter, A. Hyldgård, K. Birkelund, M.B. Arnoldus, O. Hansen, and E.V. Thomsen. Determination of packaging induced 3d stress utilizing a piezocoefficient mapping device. Proc. of the IEEE MEMS, pages 69–72, 2007.

[74] R. Steiner, Ch. Maier, A. Haberli, F.-P Steiner, and H. Baltes. Offset reduction in Hall devices by continuous spinning current method. Sensors and Actuators A: Physical, 66:167–172, 1998.

[75] J. Bartholomeyczik, M. Doelle, P. Ruther, and O. Paul. The continuous spining current (CSC) stress sensor method for the extraction of two stress components in an offset compensated manner. Sensors and Actuators A: Physical, 127:255–260, 2006.

[76] Araldite two component epoxy.

[77] D.A. Bittle and J.C. suhling. Piezoresistive stress sensors for structural analysis of electronic packages. Journal of Electronic Packaging, 113:203–215, 1991.

[78] S.H. Crandall, N.C. Dahl, and T.J. Lardner. An Introduction to Mechanics of Solids. McGraw-Hill, 2 edition, 1978.

[79] S.M. Sze. Semiconductor sensors. John Wiley and Sons Inc., 1 edition, 1994.

[80] R. E. H. Rasmussen. Elementær Måleteori. Jul. Gjellerups Forlag, 4 edition, 1964.

[81] E.V. Thomsen and J. Richter. Piezo resistive MEMS devices. Mikroelektronik Centret DTU, 2003.

[82] R.C. Jaeger and J.C. Suhling. A piezoresistive sensor chip for measurement of stress in electronic packaging. Electronic Components and Technology Conference, 43:686–692, 1993.

[83] Y. Kanda and K. Suzuki. Origin of the shear piezoresistance coefficient π_{44} of n-type silicon. Physical Review B, 43:6754–6756, 1991.

[84] Y. Kanda. Piezoresistance effect of silicon. Sensors and Actuators, A: Physical, 28:83–91, 1991.

[85] J.D. Cressler. Re-engineering silicon: Si-ge heterojunction bipolar technology. IEEE Spectrum, 33:49–57, 1995.

[86] O. Slattery. Predicting thermomechanical stress using mesmeric methodology.

[87] F.P. Beer and Jr. E.R. Johnston. Mechanics of Materials. McGraw-Hill, si metric edition, 1985.

[88] K. Yamada and M. Nishihara. Nonlinearity of the piezoresistance effect of p-type silicon diffused layers. IEEE transactions on electron devices, pages 71–77, 1982.

[89] K. Matsuda. Second-order pieziresistance coefficients of p-type silicon. Japanese Journal of Applied Physics, Part 2 (Letters), 29:1941–1942, 1990.

[90] K. Matsuda and Y. Kanda. Nonlinearity of piezoresistance effect in p- and n-type silicon. Sensors and Actuators, A: Physical, 21:45–48, 1990.

[91] J. Richter and A. Hyldgård. Design of generic testchip - for a multiple project wafer. MIC - Department of micro and nanotechnology, 2002.

[92] J. Bausells. Design handbook - nordic microsystems manufacturing cluster. SensoNor foundry Processes, 1999.

[93] W.P. Mason, J.J. Forst, and L.M. Tornillo. Recent developments in semiconductor strain tranducers. Semiconductor and conventional strain gauges, 1962.

[94] S. Elliott. The Physics and Chemistry of Solids. John Wiley and Sons, 1 edition, 1998.

[95] Webelements. www.webelements.com. Internet, 2004.

[96] D.K. Schroeder. Semiconductor Material and Device Characterization. John Wiley and Sons Inc., 1990.

[97] S.T. Jespersen. Design and packaging concepts for MEMS pressure sensors. Master's thesis, MIC - Department of Micro and Nanotechnology, DTU, 2003.

[98] S.M. Sze and G.S. May. Fundamentals of Semiconductor Fabrication. John Wiley and Sons Inc., 2004.

[99] R.E. Newnham. Properties of materials. Oxford university press, 2005.

[100] C. Pramanik, S. Banerjee, and C.K. Sarkar. Piezoresistivity of silicon quantum well wire. Nanotechnology, 17:3209–3214, 2006.

APPENDIX

A List of publications

- J. Richter, J. Pedersen, M. Brandbyge, O. Hansen and E.V. Thomsen, *Piezoresistance in p-type silicon revisited. Journal of Applied Physics*, Vol. 104, 023715-1-8, 2008.
- J. Richter, M.B. Arnoldus, O. Hansen and E.V. Thomsen, *Four point bending setup for characterization of semiconductor piezoresistance. Review of scientific instruments*, Vol. 79(4), 044703-1-10, 2008.
- K. Reck, J. Richter, O. Hansen and E.V. Thomsen, *Piezoresistive effect in top-down fabricated silicon nanowires.* In *Proceedings of IEEE MEMS 2008*, Tucson, USA, 2008.
- P. Gieschke, J. Richter, J. Joos, P. Ruther, and O. Paul, *Four-degree-of-freedom solid state MEMS joystick.* In *Proceedings of IEEE MEMS 2008*, Tucson, USA, 2008.
- J. Richter, A. Hyldgård, K. Birkelund, O. Hansen and E.V. Thomsen, *Realtime 3D stress measurement in curing epoxy packaging.* In *Proceedings of Transducers 2007*, Lyon, France, 2007.
- J. Richter, A. Hyldgård, K. Birkelund, M.B. Arnoldus, O. Hansen and E.V. Thomsen, *Determination of packaging induced 3D stress utilizing a piezocoefficient mapping device.* In *Proceedings of IEEE MEMS 2007*, p. 69-72, Kyoto, Japan, 2007.
- J. Richter, M.B. Arnoldus, J. Lundsgaard Hansen, A. Nylandsted Larsen, O. Hansen and E.V. Thomsen, *Piezoresistance in strained silicon and strained silicon germanium.* In *2006 Materials Research Society Symposium Proceedings*, Vol. 958, p. 133, Boston, USA, 2006.
- M.B. Arnoldus, T. Hedegaard, M. Olesen, J. Richter and E.V. Thomsen, *Determination of piezoresistive properties of silicon and strained silicon germanium.* In *Technical Digest of Eurosensors XVX*, p. 130-133, Gothenburg, Sweden, 2006.
- J. Richter, O. Hansen, A. Nylandsted Larsen, J.L. Hansen, G.F. Eriksen and E.V. Thomsen, *Piezoresistance of Si and strained $Si_{1-x}Ge_x$. Sensors and Actuators A*, 123-124, p. 388-396, 2006.
- J. Richter, O. Hansen, A. Nylandsted Larsen, J.L. Hansen, G.F. Eriksen and E.V. Thomsen, *Piezoresistance of Si and strained $Si_{1-x}Ge_x$.* In *Technical Digest of Eurosensors XVIII*, p. 961-962, Rome, Italy, 2004.

APPENDIX

B Journal papers

B.1 Journal of Applied Physics

JOURNAL OF APPLIED PHYSICS **104**, 023715 (2008)

Piezoresistance in *p*-type silicon revisited

J. Richter,[1,a)] J. Pedersen,[1] M. Brandbyge,[1] E. V. Thomsen,[1] and O. Hansen[1,2]
[1]*Department of Micro- and Nanotechnology, DTU Nanotech Building 345 East, Technical University of Denmark, DK-2800 Kgs. Lyngby, Denmark*
[2]*Danish National Research Foundation's Center for Individual Nanoparticle Functionality (CINF), Technical University of Denmark, DK-2800 Kgs. Lyngby, Denmark*

(Received 28 January 2008; accepted 28 May 2008; published online 30 July 2008)

We calculate the shear piezocoefficient π_{44} in *p*-type Si with a 6×6 $\mathbf{k}\cdot\mathbf{p}$ Hamiltonian model using the Boltzmann transport equation in the relaxation-time approximation. Furthermore, we fabricate and characterize *p*-type silicon piezoresistors embedded in a (001) silicon substrate. We find that the relaxation-time model needs to include all scattering mechanisms in order to obtain correct temperature and acceptor density dependencies. The $\mathbf{k}\cdot\mathbf{p}$ results are compared to results obtained using a recent tight-binding (TB) model. The magnitude of the π_{44} piezocoefficient obtained from the TB model is a factor of 4 lower than experimental values; however, the temperature and acceptor density dependencies of the normalized values agree with experiments. The 6×6 Hamiltonian model shows good agreement between the absolute value of π_{44} and the temperature and acceptor density dependencies when compared to experiments. Finally, we present a fitting function of temperature and acceptor density to the 6×6 model that can be used to predict the piezoresistance effect in *p*-type silicon. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2960335]

I. INTRODUCTION

Piezoresistance in silicon and germanium was discovered by Smith in 1954.[1] Since then there has been academic and industrial interest in the characterization and exploitation of piezoresistance in silicon and other semiconductor materials. The interest from industry is due to the large piezoresistive response of silicon that favors a large sensitivity of microelectromechanical system (MEMS) sensors.[2] The academic focus is due to scarcity of reliable experimental results and disagreement between measurements and theoretical models, especially in *p*-type silicon. Yet another important issue is that the results from the theoretical models need to be available in a form that is directly usable for experimentalists. By increasing the complexity of materials as technology matures, the need for a reliable theoretical piezoresistive model becomes important. For example, experimental data on strained silicon crystals[3] and silicon nanowires[4] show a significant increase in the piezoresistive effect. In order to understand the effect in the new material structures that nanotechnology provides, a fully developed physical model for bulk material, in particular *p*-type silicon, is needed.

In *p*-type silicon the piezoresistive effect is mainly described by the shear piezocoefficient π_{44}. The shear piezocoefficient is known to be dependent on temperature and doping level.[5] Thus a model is needed in order to predict MEMS device sensitivity. For prediction of the sensitivity, a model from Kanda[6] is most commonly used. Kanda[6] determined a correction factor $P(T,N)$ to describe the effect of temperature T and doping level N on the piezocoefficients. Kanda's[6] analysis was based on repopulation effects due to stress induced shifts of rigid parabolic bands or valleys, assuming a power law energy dependency of the relaxation time. This many-valley model[7] has proven very successful in describing piezoresistivity in *n*-type silicon, where even the predicted relative magnitudes of the piezocoefficients agree well with experiments. In *p*-type silicon, however, the model is not as successful since the piezoresistivity is due to warpage of the energy surfaces while repopulation effects are unimportant, as already pointed out by Adams.[8] In spite of this fact the correction factor $P(T,N)$ is often used and quoted in most textbooks on the subject. It is, however, an experimental fact that it severely underestimates the piezocoefficient π_{44} at high doping levels; this is very important since optimization of piezoresistive sensors for low $1/f$ noise favor the use of high doping levels.[9] Recently, Kozlovskiy *et al.*[10] carried out a detailed analytical study of piezoresistance in *p*-type silicon using analytical valence band models of varying complexity, derived from Pikus and Bir,[11] combined with a power law model for momentum relaxation time, as was also used in previous works.[12–14] Approximations to the valence band structure valid close to the top of the valence band were used in Refs. 13 and 14, while Toriyama and Sugiyama[12] used an approximation valid at larger hole energies.

In this paper we calculate the piezocoefficient π_{44} in silicon based on a 6×6 $\mathbf{k}\cdot\mathbf{p}$ (6×6) model as well as a state-of-the-art tight-binding (TB) model, and fabricate and characterize silicon samples in order to compare theory with experimental results. We calculate the piezoresistance using the Boltzmann transport equation considering different models for the energy-dependent relaxation time. We find that it is vital to include all scattering mechanisms properly in the relaxation time, as also noted by Ohmura.[15] The results from the two models are compared to experimental data obtained on microfabricated boron doped silicon piezoresistors embedded in a silicon substrate, from own experiments and from Tufte and Stelzer.[5] The results from the 6×6 model are used to obtain a fitting function of the piezocoefficient π_{44}

a)Electronic mail:jar@mic.dtu.dk.

dependency on the temperature and the acceptor density. This simple fit can easily be included in commercial software to predict the output of a designed piezoresistive MEMS component.

II. THEORY

A. Piezoresistivity

By applying a tensorial strain ϵ_{ij} or stress X_{ij} to a silicon crystal, the resistivity and conductivity tensors change. These changes are in the low stress linear regime characterized by the fourth order piezoresistance tensor π_{ijkl}. The resistivity ϱ_{ij} and conductivity σ_{ij} tensors are

$$\varrho_{ij} = \varrho_{ij}^{(0)} + \Delta\varrho_{ij} = \varrho_0(\delta_{ij} + \pi_{ijkl}X_{kl}),$$

$$\sigma_{ij} = \sigma_{ij}^{(0)} + \Delta\sigma_{ij} = \sigma_0(\delta_{ij} - \pi_{ijkl}X_{kl}), \tag{1}$$

where $i,j,k,l \in \{1,2,3\}$, δ_{ij} is Kronecker's delta, and $\Delta\varrho_{ij}$ and $\Delta\sigma_{ij}$ are the stress induced resistivity and conductivity changes, respectively. The superscript (0) indicates unstrained condition, and σ_0 and ϱ_0 are the scalar conductivity and resistivity, respectively. By using six-vector notation and by applying the symmetry of the silicon crystal,[16] the piezoresistance tensor is simplified to a 6×6 matrix $\pi_{\eta\mu}$ with only three independent coefficients—π_{11}, π_{12}, and π_{44}. We determine the shear piezocoefficient using

$$\pi_{44} = -\frac{1}{X_6}\frac{\Delta\sigma_6}{\sigma_0} = -\frac{S_{44}}{\epsilon_6}\frac{\Delta\sigma_6}{\sigma_0} = -\frac{S_{44}}{\epsilon_6}\frac{\sigma_6}{\sigma_0}, \tag{2}$$

where the linear relation between stress and strain is used, i.e., $\epsilon_\eta = S_{\eta\mu}X_\mu$, where $\eta,\mu \in \{1,2,3,4,5,6\}$, and the compliance tensor $S_{\eta\mu}$ has the same structure as the piezoresistance tensor $\pi_{\eta\mu}$. Notice that the six-vector to tensor element relations are $\Delta\sigma_6 = \Delta\sigma_{xy}$, $X_6 = X_{xy}$, and $\epsilon_6 = 2\epsilon_{xy}$.[16] From Eq. (2) the shear piezocoefficient π_{44} may be calculated from the calculated shear conductance values σ_6 at given values of the shear strain ϵ_{xy}.

B. Conductivity

Given the dispersion relation $\xi_n(\mathbf{k})$, where ξ_n is the *hole* energy, $\mathbf{k}$ is the wavevector, and n refers to the band index, the electrical conductivity tensor may be calculated using the Boltzmann transport equation in the relaxation-time approximation,[17]

$$\sigma_{ij} = -\frac{e^2}{4\pi^3\hbar^2}\sum_{n=1}^{3}\int \tau_{\mathbf{m}}(\mathbf{k},T)\frac{\partial\xi_n(\mathbf{k})}{\partial k_i}\frac{\partial\xi_n(\mathbf{k})}{\partial k_j}\frac{\partial f_0}{\partial\xi}\mathrm{d}\mathbf{k}, \tag{3}$$

where the sum extends over the three valence bands, and f_0 is the equilibrium distribution function for holes. The relaxation time $\tau_{\mathbf{m}}$ is most commonly modeled via a simple power law,

$$\tau_{\mathbf{m}} \propto \left(\frac{\xi_n(\mathbf{k}) - \xi_n^{(0)}}{k_B T_0}\right)^s, \tag{4}$$

where $\xi_n^{(0)}$ is the band minimum, $T_0 = 300$ K, and the parameter $s \in \{-1/2, 0, 3/2\}$. The $s=-1/2$ model corresponds to scattering dominated by acoustic phonons and is the model employed by Kanda,[6] the $s=0$ model assumes a constant relaxation time, and $s=3/2$ corresponds to scattering dominated by ionized impurities. Such a crude model is insufficient for several reasons. First, it is a very poor model for nonpolar optical phonon scattering, which is important in silicon near room temperature. Second, the different scattering mechanisms emphasize transport in regions of the band structure rendered unimportant by other scattering mechanisms, and thus the final real transport properties cannot be deduced from individual conductivities evaluated using this model. That is, Matthiessen's rule simply cannot be applied to the integrated quantities. We consequently employ a more detailed model of the relaxation time. The important scattering mechanisms near room temperature are nonpolar optical phonon scattering, acoustical phonon scattering, and ionized impurity scattering. The microscopic scattering rates add; thus the momentum relaxation time is taken as

$$\frac{1}{\tau_{\mathbf{m}}(\mathbf{k},T)} = \frac{1}{\tau_{\mathrm{ap}}(\mathbf{k},T)} + \frac{1}{\tau_{\mathrm{op}}(\mathbf{k},T)} + \frac{1}{\tau_I(\mathbf{k},T)}, \tag{5}$$

where $1/\tau_{\mathrm{ap}}$, $1/\tau_{\mathrm{op}}$, and $1/\tau_I$ are the scattering rates due to acoustic phonons, nonpolar optical phonons, and ionized impurities, respectively.

The acoustic phonon scattering rate is[18]

$$\frac{1}{\tau_{\mathrm{ap}}} = \frac{2\pi D_a^2 k_B T}{\hbar\rho v_s^2} g(\xi_{\mathbf{k}}), \tag{6}$$

where D_a is the acoustic deformation potential, ρ is the mass density, v_s is the speed of sound, and $g(\xi_{\mathbf{k}})$ is the density of final states. The high density of states in the heavy hole band makes scattering to this band dominant. Thus, for simplicity we take for all three bands the acoustic scattering rate

$$\frac{1}{\tau_{\mathrm{ap}}(\mathbf{k},T)} = \frac{1}{\tau_{\mathrm{ap0}}}\frac{T}{T_0}\sqrt{\frac{\xi(\mathbf{k}) - \xi_{hh}^{(0)}}{k_B T_0}}, \tag{7}$$

with $\tau_{\mathrm{ap0}} = 5.6\times10^{-13}$ s adjusted to reproduce the rates calculated by Hinckley and Singh.[19] Here $\xi_{hh}^{(0)}$ is the minimum of the heavy hole band. For simplicity we have assumed an overall parabolic band structure for the target heavy hole band, and use the effective mass of the unstrained heavy hole band in the calculation of the density of states of the target band.

The nonpolar optical phonon scattering rate is[18]

$$\frac{1}{\tau_{\mathrm{op}}} = \frac{\pi D_o^2}{\rho\omega_0}[N_q g(\xi_{\mathbf{k}} + \hbar\omega_0) + (N_q + 1)g(\xi_{\mathbf{k}} - \hbar\omega_0)], \tag{8}$$

where the first term is due to absorption and the second term is due to emission of an optical phonon with the energy $\hbar\omega_0$. D_o is the optical deformation potential and $N_q = 1/(\exp\hbar\omega_0/k_B T - 1)$ is the phonon occupation probability. Again, scattering to the heavy hole band is dominant; thus for all three bands we obtain a simplified nonpolar optical scattering rate as

$$\frac{1}{\tau_{\mathrm{op}}(\mathbf{k},T)} = \frac{1}{\tau_{\mathrm{op}0}}\left[N_q \sqrt{\frac{\xi(\mathbf{k}) - \xi_{hh}^{(0)} + \hbar\omega_0}{k_B T_0}} + (N_q + 1)\mathrm{Re}\left(\sqrt{\frac{\xi(\mathbf{k}) - \xi_{hh}^{(0)} - \hbar\omega_0}{k_B T_0}} \right) \right], \quad (9)$$

with $\tau_{\mathrm{op}0} = 10^{-13}$ s, which reproduces the rates calculated by Hinckley and Singh.[19]

By assuming full ionization, the Brooks–Herring screened Coulomb potential scattering rate is[18]

$$\frac{1}{\tau_I} = \frac{\pi N_A e^4}{4\varepsilon^2 \hbar k^4} g(\xi_{\mathbf{k}}) L(2\lambda_D k), \quad (10)$$

where λ_D is the Debye length, ε is the permittivity, and N_A is the acceptor density, and where the function $L(x) = \ln(1+x^2) - x^2/(1+x^2)$ is slowly varying for $x > 1$. Again, scattering to the heavy hole band is dominant; thus, as an approximate model for all three bands, we write

$$\frac{1}{\tau_I} = \frac{1}{\tau_{I0}} \frac{k_0^4}{k^4} \frac{N_A}{N_0} \sqrt{\frac{\xi(\mathbf{k}) - \xi_{hh}^{(0)}}{k_B T_0}} \times L(2\lambda_D k), \quad (11)$$

with the parameters $N_0 = 10^{17}$ cm^{-3}, $k_0 = 1.0$ Å^{-1}, and $\tau_{I0} = 1.8 \times 10^{-7}$ s calculated using the density of states mass for the heavy hole band. The Debye length is the electrostatic screening length obtained in a linearization of Poisson's equation for the semiconductor. Thus

$$\frac{1}{\lambda_D^2} \equiv \frac{e^2}{\varepsilon k_B T} \left| \frac{\partial h}{\partial \xi_F} \right| \simeq \frac{e^2 N_A}{\varepsilon k_B T} \frac{\mathcal{F}_{-1/2}(\xi_F)}{\mathcal{F}_{1/2}(\xi_F)}, \quad (12)$$

where h is the hole density, ξ_F is the Fermi level in units of $k_B T$, and $\mathcal{F}_n(x)$ is the Fermi–Dirac integral of order n. In the approximate expression, an overall parabolic band approximation is assumed.

C. Band structures

We have employed two different methods to calculate the band structure of silicon—a 6×6 $\mathbf{k} \cdot \mathbf{p}$ Hamiltonian model and a recent TB model. The main reason for the comparison is that TB is used extensively to model transport in Si nanostructures and it is thus interesting to access the performance of TB.

For the 6×6 model we closely follow Hinckley and Singh[19] where the total Hamiltonian matrix is composed of three terms, as follows:

$$\mathbf{H}(\mathbf{k}, \epsilon_{ij}) = \mathbf{H}_{\mathbf{k}\cdot\mathbf{p}}(\mathbf{k}) + \mathbf{H}_{\mathrm{so}} + \mathbf{H}_{\epsilon}(\mathbf{k}, \epsilon_{ij}). \quad (13)$$

The first term is a doubly degenerate three band Hamiltonian matrix $\mathbf{H}_{\mathbf{k}\cdot\mathbf{p}}(\mathbf{k})$ calculated using the $\mathbf{k} \cdot \mathbf{p}$ method on the basis of $|x\uparrow\rangle$, $|y\uparrow\rangle$, $|z\uparrow\rangle$, $|x\downarrow\rangle$, $|y\downarrow\rangle$, and $|z\downarrow\rangle$. The three band structure parameters L, M, and N adjust the Hamiltonian to fit experimental band structure data.[20] The second term is a constant spin-orbit perturbation Hamiltonian matrix $\mathbf{H}_{\mathrm{so}}$ with a single parameter which is the spin-orbit splitting energy Δ_{so}. The final term is a strain perturbation Hamiltonian matrix $\mathbf{H}_{\epsilon}(\mathbf{k}, \epsilon_{ij})$, which is a function of both wavevector and strain tensor. The strain perturbation Hamiltonian has three deformation potential parameters a, b, and d (Ref. 11), which are tuned to match experimental data. Since the present work emphasizes the shear piezoresistance coefficient, only the shear deformation potential d is used in this work. The parameter values used are listed in Table I.[21] The total Hamiltonian is diagonalized at each k-point at a prescribed strain and six pair-wise identical eigenvalues are determined. These eigenvalues form the three valence bands.[22]

TABLE I. Parameter values for the 6×6 Hamiltonian (Ref. 21).

L (eV Å^2)	M (eV Å)	N (eV Å)	d (eV)	Δ_{so} (eV)
−21.488	−13.716	−33.259	−5.1	0.044

We base our TB calculation on the recent parametrization by Boykin *et al.* in Ref. 23. We found that earlier TB parameters developed by Jancu *et al.*[24] yield negative values for the piezocoefficient π_{44} due to an erroneous $\pi/2$ rotation of the band structure under pure shear strain. The effect of strain on these parameters is included both via the angular dependencies of the Slater–Koster decompositions, as well as the bond-length dependencies.[25]

D. Numerical method

The conductivity integral in the Boltzmann transport equation of Eq. (3) is calculated numerically using the discrete three-dimensional (3D) dispersion relation obtained using the band structure calculations outlined in the previous section. We assume full ionization so that $h = N_A$, where h is the hole density. The density of holes may be calculated as

$$h = \sum_n \frac{2}{(2\pi)^3} \int f_0(\mathbf{k}, n) d\mathbf{k}, \quad (14)$$

where $f_0(\mathbf{k}, n)$ is the equilibrium distribution function for holes, and a factor of 2 for spin has been included. The sum extends over the three valence bands. By evaluating this integral for several values of the Fermi level ξ_F, we may determine the Fermi level at a given dopant level. To determine the strain dependence of the conductivity we calculate the 3D band structure of the strained material. However, to avoid numerical problems with the evaluation of the Fermi level integral, we do not calculate this for each strain. Instead, we have found it useful to determine the Fermi level of the unstrained structure, and then calculate the dependence of the Fermi level on strain along the desired direction as follows. Since the hole density is assumed to equal the constant N_A independent of strain, we get

$$\frac{dh}{d\epsilon} = \sum_n \int \frac{e^{\xi_F^{(0)} - \xi_{n,\mathbf{k}}}}{(e^{\xi_F^{(0)} - \xi_{n,\mathbf{k}}} + 1)^2} \times \frac{d\xi_{n,\mathbf{k}}}{d\epsilon} d\mathbf{k} + \sum_n \int \frac{e^{\xi_F^{(0)} - \xi_{n,\mathbf{k}}}}{(e^{\xi_F^{(0)} - \xi_{n,\mathbf{k}}} + 1)^2} \times \frac{d\xi_F}{d\epsilon} d\mathbf{k} = 0, \quad (15)$$

where ξ_F and $\xi_{n,\mathbf{k}}$ are in units of kT. From this we calculate the change of Fermi level with strain,

TABLE II. Values of π_{44} in p-type silicon at an acceptor density of $N_A = 10^{14}$ cm^{-3} calculated using the TB model and the 6×6 model.

T (K)	TB π_{44} ($\times10^{-11}$ Pa^{-1})	6×6 π_{44} ($\times10^{-11}$ Pa^{-1})
200	41	180
300	31	122
400	25	94

$$\frac{d\xi_F}{d\epsilon} = \frac{\sum_n \int \frac{e^{\xi_F^{(0)}-\xi_{n,\mathbf{k}}}}{(e^{\xi_F^{(0)}-\xi_{n,\mathbf{k}}}+1)^2} \times \frac{d\xi_{n,\mathbf{k}}}{d\epsilon} d\mathbf{k}}{\sum_n \int \frac{e^{\xi_F^{(0)}-\xi_{n,\mathbf{k}}}}{(e^{\xi_F^{(0)}-\xi_{n,\mathbf{k}}}+1)^2} d\mathbf{k}}, \tag{16}$$

where $\xi_F^{(0)}$ is the Fermi level calculated at zero applied strain. We then calculate the Fermi level at a given strain as

$$\xi_F(h,\epsilon) = \xi_F(h,\epsilon=0) + \frac{d\xi_F}{d\epsilon}\epsilon. \tag{17}$$

Implementation of the model has been carried out in MATLAB.[26] The calculated conductivities have all been converged with respect to the volume of k-space evaluated around the Γ point as well as the k-point resolution. All results presented in this article have been calculated using equidistant k-point sampling along each principal axis. A total of $N=357\,911$ k-points have been sampled. The piezoresistance coefficients are extracted from a linear fit to calculated shear conductivities for four values of the applied shear strain $\epsilon_{xy} \in \{0, 0.0005, 0.001, 0.0015, 0.002\}$; in that strain range the relation between shear conductance and shear strain was almost perfectly linear.

III. MODEL RESULTS

Using the calculated conductivities with and without applied strain, the piezocoefficient π_{44} is calculated from Eq. (2). We shall concentrate on π_{44} due to the technological relevance compared to the other piezocoefficients π_{11} and π_{12}; they could, however, be calculated in a manner similar to π_{44}, as seen from Eq. (1). In the calculation the shear compliance $S_{44}=1.256\times10^{-11}$ Pa^{-1} is used,[27] while the relative temperature coefficient of S_{44} ($\sim97\times10^{-6}$ K^{-1}) is ignored since the numerical value is much smaller than that of π_{44} ($\sim-3\times10^{-3}$ K^{-1}). The relative temperature coefficient of S_{44} is estimated from the relative temperature coefficient of the coefficient of elasticity $C_{44}=1/S_{44}$ ($\sim-97\times10^{-6}$ K^{-1}).[28]

The values of π_{44} at an acceptor density of $N_A=1.0\times10^{14}$ cm^{-3} calculated at temperatures $T=200$, 300, and 400 K using the TB model and the 6×6 model are listed in Table II. Calculations of π_{44} showing the detailed dependency on acceptor dopant density and temperature are shown graphically in Fig. 1 when using the 6×6 model. The two different models result in similar observable trends for the temperature as well as the dopant density dependency. In the temperature range from $T=200$ to 450 K the π_{44} value extracted from the TB model varies from 41×10^{-11} to 22×10^{-11} Pa^{-1} at the dopant density $N_A=1.0\times10^{14}$ cm^{-3}.

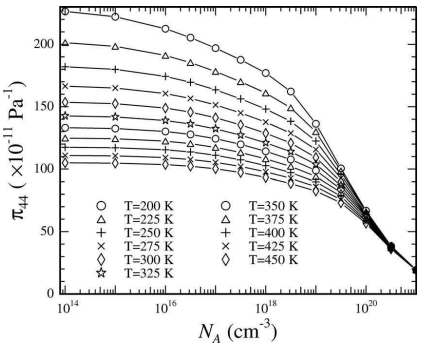


FIG. 1. The piezocoefficient π_{44} as a function of carrier density and temperature calculated using the 6×6 model. The calculated values are in good agreement with the experimental data listed in Table III.

Compared to published experimental data listed in Table III, these values are approximately a factor of 4 too small. Thus, we conclude that the parameters used in the TB model are not yet fully optimized for piezoresistance calculations. In contrast to this large discrepancy, the 6×6 model results in absolute π_{44} values essentially in agreement with experiments.

In Fig. 2 the calculated temperature dependency, for both the 6×6 and TB models, is illustrated by plotting the π_{44} values normalized with the values calculated at $T=300$ K for two different doping levels, $N_A=1.0\times10^{14}$ and 1.0×10^{19} cm^{-3}. The normalized piezocoefficient values are plotted as a function of $1/T$. At low dopant density the piezocoefficients calculated from the 6×6 model closely follow the expected $1/T$ dependency, while the temperature dependency extracted from the TB model is somewhat smaller (by approximately 10%). At the higher dopant density the calculated temperature dependencies from the two models are similar and less than the $1/T$ dependency. The approximate $1/T$ dependencies arise from piezocoefficients approximately inversely proportional to the kinetic energy of the carriers, while the similar dependency observed in n-type silicon is due to repopulation effects.

TABLE III. Experimental values of the piezocoefficient π_{44} in p-type silicon at $T=300$ K. The last column lists standard deviations of the piezocoefficient measurements when available.

Ref.	Dopant density ($\times10^{18}$ cm^{-3})	π_{44} ($\times10^{-11}$ Pa^{-1})	Deviation (%)
[1]	0.002	138.1	
[29]	0.02	93.1	7.5
[30]	0.03	113.5	6
[31]	0.8	105	8–12
[32]	1.5	87	6.5
[5]	3	111	
[31]	8.2	95	8–12
[5]	9	98	
[5]	50	78	
[5]	300	60	
[5]	500	48	
[5]	2000	35	

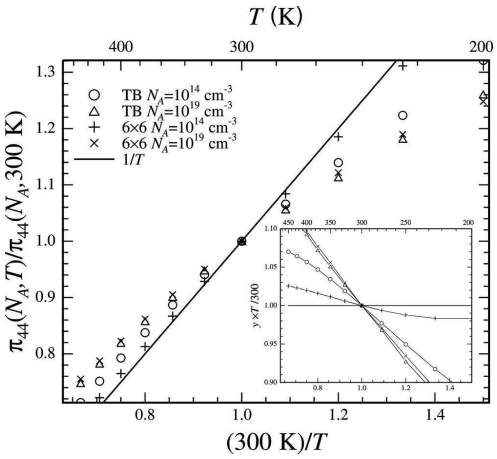


FIG. 2. Temperature dependency of the normalized piezocoefficient $\pi_{44}(T)/\pi_{44}(T_0=300\ \mathrm{K})$ at the dopant densities $N_A=1.0\times10^{14}$ and 1.0×10^{19} cm^{-3} calculated using the TB model and the 6×6 model. The solid line shows a perfect $1/T$ dependency. In the inset the normalized piezocoefficients are multiplied by the factor $T/300$ K to reveal the deviation from the expected $1/T$ dependency. The 6×6 model calculations at low acceptor density ($N_A=1.0\times10^{14}$ cm^{-3}) deviates only a few percent from the $1/T$ dependency.

IV. EXPERIMENTAL

We have designed and fabricated piezoresistance test chips in order to compare the calculated piezocoefficients from the two models with experimental data. A micrograph of the chip is shown in Fig. 3. In the region near the center of the chip, six resistors, oriented along different crystal directions, are defined. The chips are fabricated using conventional microfabrication techniques. The test chips have been fabricated in two different processes. One process includes the use of a silicon on insulator (SOI) substrate with a (001) device layer; the SOI starting material is very useful since it facilitates uniform doping of the piezoresistors. The piezoresistors are defined using reactive ion etching (RIE), and boron doped using ion implantation followed by a thermal oxidation and anneal to ensure activation and uniform doping of the device layer. The uniformly doped piezoresistors have doping concentrations of $N_A=1.5\times10^{17}$, 2.0×10^{18}, and 2.2×10^{19} cm^{-3}. In the other process boron ion implantation on the surface of a (001) silicon substrate followed by RIE, thermal oxidation, and anneal gives piezoresistors a Gaussian doping profile. The peak boron concentrations in the Gaussian doping profile resistors are $N_A=9.1\times10^{17}$, 9.4×10^{18}, and 4.6×10^{19} cm^{-3}. For both processes contact windows are etched using buffered HF and interconnects to the resistors are defined in an e-beam evaporated double layer of Ti/Al. The piezoresistance characterization is done in an automated four point bending fixture. This fixture applies a uniaxial, uniform stress to the resistors in the center region of the chip[33] in steps of approximately 5 to a maximum value of 70 MPa, which corresponds to a strain of $\epsilon_{xx}\approx0.0004$.

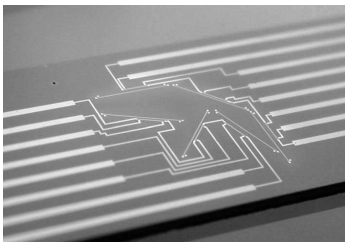


FIG. 3. Close-up micrograph of the fabricated piezoresistance test chip. Six piezoresistors are directed along different directions and located in the center region of the chip. The chip is 4 cm long and 5.3 mm wide.

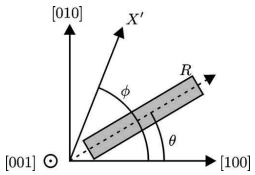


FIG. 4. Schematic showing the orientation of the piezoresistor and the applied uniaxial stress X'. The long axis of the resistor is oriented at the angle θ, while the uniaxial stress is applied at the angle ϕ to the [100] direction on a (001) substrate.

In the experimental approach we use Eq. (1) where the change in resistivity depends on the applied stress X. The relative change in resistivity is equal to the relative change in the resistance of a piezoresistor. Now consider the resistor R on a (001) substrate as shown in Fig. 4. By applying the uniaxial, uniform stress X' to the sample, the relative resistance change is[34]

$$\frac{\Delta R}{R_0}(\phi,\theta)=\frac{X'}{2}[\pi_{11}+\pi_{12}+\cos(2\phi)\cos(2\theta)(\pi_{11}-\pi_{12})+\sin(2\theta)\sin(2\phi)\pi_{44}], \quad (18)$$

where θ is the angle of the resistor orientation with respect to the [100] direction and ϕ is the angle at which the stress X' is directed with respect to the [100] direction. The piezocoefficient π_{44} can then be found by measuring the resistance on two resistors directed according to the equation

$$\pi_{44}=\frac{\Delta R}{R_0}\left(\frac{\pi}{4},\frac{\pi}{4}\right)\frac{1}{X'}-\frac{\Delta R}{R_0}\left(\frac{\pi}{4},\frac{3\pi}{4}\right)\frac{1}{X'}=\pi_l-\pi_t, \quad (19)$$

where π_l and π_t are the longitudinal and transversal piezocoefficients, respectively.

V. DISCUSSION

Using the piezoresistance test chips in the four point bending setup, we have experimentally determined the shear piezocoefficient π_{44} in silicon with the acceptor dopant densities given in Sec. IV at three different temperatures $T=300$, 325, and 350 K. The experimental data are plotted in Fig. 5, where experimental data from Tufte and Stelzer[5] are added to extend the experimental range of dopant densities and temperatures. Our measurements are seen to agree well with the data from literature in the range where the param-

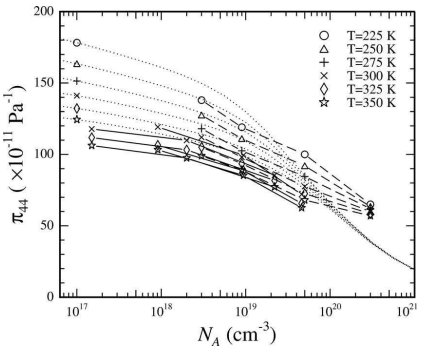


FIG. 5. Experimental and calculated values of the piezocoefficient π_{44} as a function of doping level with temperature as parameter. The dashed lines are experimental data from Tufte and Stelzer (Ref. 5) and the solid lines are experimental data obtained from the piezoresistors described in Sec. IV. Notice that the full lines connect the actual experimental points and are thus just guides to the eye. The dotted lines are model calculations using the 6 $\times$6 model.

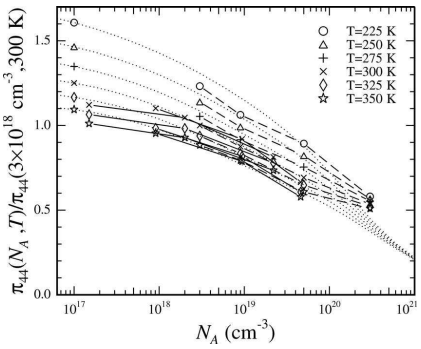


FIG. 7. Experimental and calculated values of the normalized piezocoefficient π_{44} as a function of doping level with temperature as parameter. The piezocoefficients are normalized to π_{44} at T=300 K and N_A=3.0 $\times 10^{18}$ cm^{-3}. The dashed lines are experimental data from Tufte and Stelzer (Ref. 5) and the solid lines are experimental data obtained from the piezoresistors described in Sec. IV. Notice that the full lines connect the actual experimental points and are thus just guides to the eye. The dotted lines are model calculations using the 6$\times$6 model with the scattering rates multiplied by the availability factor $(1-f_0)$.

eters are comparable. In Fig. 5 the experimental data are compared to shear piezocoefficients π_{44} calculated using the 6$\times$6 model. The absolute magnitude of the calculated piezocoefficients are in quite good agreement with the measured values, and any small discrepancy at a given doping level and temperature could be attributed to the value of the shear deformation potential d used, since $\pi_{44} \propto d$.

To focus attention on the temperature and doping level dependency, we plot in Fig. 6 the data of Fig. 5 normalized to π_{44} at T=300 K and $N_A=3.0\times10^{18}$ cm^{-3}. Excellent agreement between experiments and model calculations is seen at dopant densities below 1×10^{19} cm^{-3}. At larger dopant densities the model calculations show a significantly stronger dopant density dependency than experimentally observed. This discrepancy could be due to several reasons related to shortcomings in the model used. First, in the model

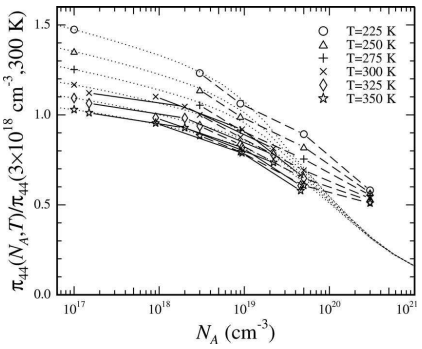


FIG. 6. Experimental and calculated values of the normalized piezocoefficient π_{44} as a function of doping level with temperature as parameter. The piezocoefficients are normalized to π_{44} at T=300 K and N_A=3.0 $\times 10^{18}$ cm^{-3}. The dashed lines are experimental data from Tufte and Stelzer (Ref. 5) and the solid lines are experimental data obtained from the piezoresistors described in Sec. IV. Notice that the full lines connect the actual experimental points and are thus just guides to the eye. The dotted lines are model calculations using the 6$\times$6 model.

of the scattering rates we have ignored the effect of availability of the final states; this is vital at very high doping levels. Second, at very high doping the band structure is modified by band tailing.[35] As a result, the actual Fermi level at high doping will be closer to the band edge than expected from simple theory. This is easily understood if we write the total hole concentration $h=h_{bt}+h_b$,[35] where h_{bt} is the hole concentration in the band tail while h_b is the hole concentration in the remaining unperturbed bands. This change in doping level dependency of the Fermi level will affect the magnitude of the piezocoefficient as well as the temperature dependency, since relatively simple considerations predict a piezocoefficient $\pi_{44} \propto d/\langle E_{kin}\rangle$, where $\langle E_{kin}\rangle$ is the average kinetic energy of the carriers contributing to the conductivity. At low doping levels $\langle E_{kin}\rangle \propto k_B T$ while at very high doping levels only carriers with a kinetic energy close to the Fermi level contribute to the conductivity and $\langle E_{kin}\rangle$ equals the energy difference between the Fermi level and the band edge. Thus the temperature dependency of the piezocoefficient vanishes at high doping levels, as is also seen in the calculations.

To illustrate the effect of availability of final states we adopt a crude model, where the scattering rate Eq. (5) is multiplied by the availability factor $(1-f_0)$, and calculate the resulting piezocoefficients using the 6$\times$6 model. The result of the calculation is shown in Fig. 7 where piezocoefficients normalized to π_{44} at T=300 K and doping level $N_A=3.0\times10^{18}$ cm^{-3} are shown along with the experimental values. The agreement between model calculations and experiments is seen to improve; at dopant densities below 1×10^{20} cm^{-3} the agreement is very good. The remaining disagreement is probably due to the band-tailing effect discussed above. Unfortunately, a simple yet satisfactory model for this effect is not available; therefore we have not been able to do modeling experiments to verify the effect on the piezocoefficients.

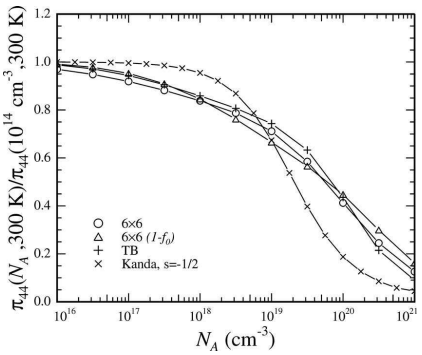


FIG. 8. Calculated piezocoefficients π_{44} at $T=300$ K normalized to π_{44} at low dopant density $N_A=1.0\times10^{14}$ cm^{-3} as a function of acceptor dopant density. Calculations using both the TB and the 6×6 models are shown. For the 6×6 model a calculation using the scattering rate multiplied by the availability factor $(1-f_0)$ is added. Finally, the correction factor due to Kanda (Ref. 6) using $s=-1/2$ is included.

To illustrate the effect of the band structure model and the scattering rate model we plot the calculated normalized piezocoefficients at $T=300$ K resulting from the 6×6 and TB models in Fig. 8, where a calculation for the 6×6 model with the scattering rate multiplied by the availability factor $(1-f_0)$ is also shown. The piezocoefficients are normalized with π_{44} at very low dopant density $N_A=1.0\times10^{14}$ cm^{-3}. Finally, for comparison, the popular correction factor due to Kanda[6] with $s=-1/2$ is added to the graph. The dopant density dependency of all our model calculations differ significantly from Kanda's correction factor. The effect of increased doping density is much more gradual in our calculations. The dopant density dependency predicted from the two band structure models differ only slightly.

The effect of the scattering rate model on the calculated piezocoefficients from the 6×6 model is shown in Fig. 9, where the calculated piezocoefficients at $T=300$ K normalized to π_{44} at very low dopant density $N_A=1.0\times10^{14}$ cm^{-3} are shown for five different models of the scattering rate. The results from using the full scattering rate model Eq. (5) and the same model with a slightly simplified impurity scattering model replacing $L(2\lambda_D k)$ by a constant are shown together with calculations using the power law model Eq. (4) using $s=0$, $-1/2$, and 3/2. Obviously, if all relevant scattering mechanisms are included, a much more gradual reduction in the piezocoefficient with increased doping level is seen as compared to the steep reduction obtained with the power law models. Since the gradual decrease is also seen experimentally (Fig. 5), we conclude that it is essential to use the detailed scattering rate model. The effect of using a less accurate impurity scattering model is quite small though.

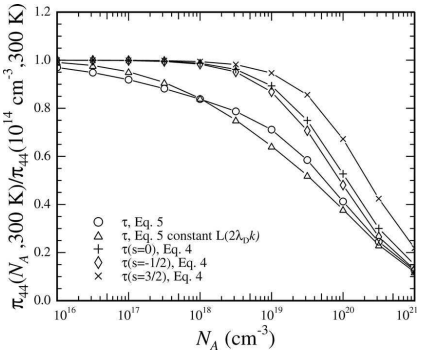


FIG. 9. Piezocoefficients π_{44} at $T=300$ K normalized to π_{44} at low dopant density $N_A=1.0\times10^{14}$ cm^{-3} calculated from the 6×6 model as a function of acceptor dopant density. Five different models for the scattering rates are used. The results from using the full scattering rate model Eq. (5) and the same model with a slightly simplified impurity scattering model replacing $L(2\lambda_D k)$ by a constant are shown together with calculations using the power law model Eq. (4) using $s=0$, $-1/2$, and 3/2.

TABLE IV. Fitting parameters used in Eq. (20).

Parameter	Value
N_b	6×10^{19} cm^{-3}
N_c	7×10^{20} cm^{-3}
ϑ	0.9
α	0.43
β	0.1
γ	1.6
η	3

A. Piezocoefficient fit

In order to produce a more satisfactory correction factor compared to that of Kanda,[6] we fit the normalized piezocoefficient π_{44} as a function of temperature and acceptor density to the results from the 6×6 model calculations with the scattering rate multiplied by the availability factor $(1-f_0)$. We fit the normalized piezocoefficient to the function

$$P(N_A,\Theta)=\Theta^{-\vartheta}\left[1+\left(\frac{N_A}{N_b}\right)^{\alpha}\Theta^{-\beta}+\left(\frac{N_A}{N_c}\right)^{\gamma}\Theta^{-\eta}\right]^{-1}, \quad (20)$$

where $P(N_A,\Theta)$ is the piezocoefficient normalized to the lowest acceptor density value at $T_0=300$ K, $\Theta=T/T_0$, N_b and N_c are fitting parameters, and ϑ, α, β, γ, and η are power coefficients.

The fitting parameters are found by a two-dimensional fit to the surface defined by N_A and Θ. The resulting parameters are listed in Table IV. The first term in the denominator dominates at low acceptor densities while at high acceptor densities both terms are important. The fit is shown in Fig. 10 together with normalized piezocoefficient values calculated using the 6×6 model. The simple fit agrees well with the 6×6 model calculations and can therefore be used to predict the π_{44} dependence on acceptor density and temperature at acceptor densities below 1×10^{20} cm^{-3}. Thus, the fitting function is a simple tool provided to experimentalist and industrial MEMS developers within piezoresistive device research and applications.

VI. CONCLUSION

We have numerically calculated the shear piezocoefficient π_{44} in p-type silicon using a 6×6 $\mathbf{k}\cdot\mathbf{p}$ Hamiltonian

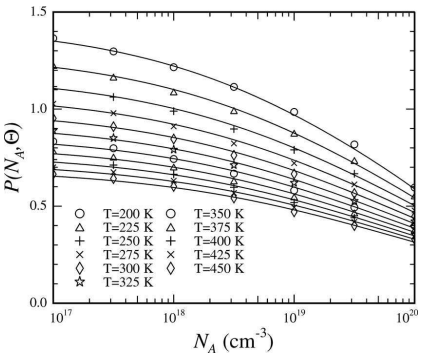


FIG. 10. Fitted correction factor for π_{44} as a function of carrier density and temperature. The fit (solid) is described by Eq. (20) and the fitting parameters are listed in Table IV. The symbols are 6×6 model calculations using the availability corrected scattering rates.

band structure calculation combined with detailed analytical models for the scattering rates. These results have been compared to results obtained with a recent TB model as well as to experimental data. We have measured the shear piezocoefficient π_{44} in *p*-type silicon at several dopant densities and temperatures, using dedicated test chips and a four point bending fixture measurement setup. Band structures calculated from the 6×6 $\mathbf{k}\cdot\mathbf{p}$ Hamiltonian predict piezocoefficients in quite good agreement with experiments at acceptor dopant densities below $N_A=1\times10^{20}$ cm^{-3}. We have found that it is important to include all relevant scattering mechanisms, acoustic phonon, nonpolar optical phonon, and ionized impurity scattering in order to get decent agreement between model calculations and experiments. This is particularly important in order to reproduce the gradual decrease in piezoresistance coefficient with increased dopant density.

Our comparison highlights the importance of an accurate description of the strain dependence of TB parameters. The parameters developed by Boykin *et al.* result in a strained band structure that underestimates the piezocoefficients by a factor of 4 compared to the experiments and the 6×6 $\mathbf{k}\cdot\mathbf{p}$ results. It follows that more work is needed in order to optimize TB parameters for piezoresistance calculations.

The calculations result in a piezoresistance coefficient variation with temperature quite close to $1/T$ dependency at low dopant density. This dependency is caused by the average kinetic energy of the carriers contributing to the conductivity. In *p*-type silicon repopulation effects are insignificant, whereas these are the reason for the similar $1/T$ dependency seen in *n*-type silicon.[7]

Finally, since the piezocoefficient model calculations are in quite good agreement with experiments, we have developed a simple analytical fit to the calculated piezocoefficients; this fit could prove to be a useful tool in device modeling and optimization.

ACKNOWLEDGMENTS

We thank Dr. Chris Bowen (Texas Instrument) for useful comments on the TB parametrizations. Center for Individual Nanoparticle Functionality (CINF) is sponsored by The Danish National Research Foundation.

[1]C. S. Smith, Phys. Rev. **94**, 42 (1954).
[2]O. N. Tufte, P. W. Chapman, and D. Long, J. Appl. Phys. **33**, 3322 (1962).
[3]J. Richter, O. Hansen, A. Nylandsted Larsen, J. Lundsgaard Hansen, G. F. Eriksen, and E. V. Thomsen, Sens. Actuators, A **123–124**, 388 (2005).
[4]R. He and P. Yang, Nanotechnology **1**, 42 (2006).
[5]O. N. Tufte and E. L. Stelzer, J. Appl. Phys. **34**, 313 (1963).
[6]Y. Kanda, IEEE Trans. Electron Devices **29**, 64 (1982).
[7]C. Herring and E. Vogt, Phys. Rev. **101**, 944 (1956).
[8]E. N. Adams, Phys. Rev. **96**, 803 (1954).
[9]J. A. Harley and T. W. Kenny, J. Microelectromech. Syst. **9**, 226 (2000).
[10]S. I. Kozlovskiy, V. V. Nedostup, and I. I. Boiko, Sens. Actuators, A **133**, 72 (2007).
[11]G. E. Pikus and G. L. Bir, *Symmetry and Strain-Induced Effects in Semiconductors* (Wiley, New York, 1974).
[12]T. Toriyama and S. Sugiyama, J. Microelectromech. Syst. **11**, 598 (2002).
[13]K. Suzuki, H. Hasegawa, and Y. Kanda, Jpn. J. Appl. Phys., Part 2 **23**, L871 (1984).
[14]P. Kleimann, B. Semmache, M. Le Berre, and D. Barbier, Phys. Rev. B **57**, 8966 (1998).
[15]Y. Ohmura, J. Phys. Soc. Jpn. **61**, 217 (1992).
[16]J. F. Nye, *Physical Properties of Crystals*, 1st ed. (Oxford University Press, New York, 1957).
[17]B. M. Askerov, *Electron Transport Phenomena in Semiconductors* (World Scientific, Singapore, 1994).
[18]J. Singh, *Physics of Semiconductors and Their Heterostructures* (McGraw-Hill, New York, 1993).
[19]J. M. Hinckley and J. Singh, Phys. Rev. B **41**, 2912 (1990).
[20]G. Dresselhaus, A. F. Kip, and C. Kittel, Phys. Rev. **98**, 368 (1955).
[21]P. Y. Yu and M. Cardona, *Fundamentals of Semiconductors, Physics and Material Properties* (Springer-Verlag, Berlin, 2001).
[22]J. C. Slater and G. F. Koster, Phys. Rev. **94**, 1498 (1954).
[23]T. B. Boykin, G. Klimeck, and F. Oyafuso, Phys. Rev. B **69**, 115201 (2004).
[24]J. M. Jancu, R. Scholz, F. Beltram, and F. Bassani, Phys. Rev. B **57**, 6493 (1998).
[25]The TB model uses a basis set consisting of ten orthogonal valence orbitals ($sp^3d^5s^*$). The bond-length dependencies of the two-center integrals are fitted to generalizations of Harrison's free-electron distance law (Refs. 36 and 37). On-site parameters are shifted due to the displacements of nearest neighbors (Ref. 38). The spin-orbit is taken into account in the model by adding intra-atomic matrix elements using Chadi's approximation (Ref. 39).
[26]MATLAB version 7.0.1.
[27]S. K. Clark and K. D. Wise, IEEE Trans. Electron Devices **26**, 1887 (1979).
[28]H. Metzger and F. R. Kessler, Z. Naturforsch. A **25**, 904 (1970).
[29]R. E. Beaty, R. C. Jaeger, J. C. Suhling, R. W. Johnson, and R. D. Butler, IEEE Trans. Compon., Hybrids, Manuf. Technol. **15**, 904 (1992).
[30]R. C. Jaeger, J. C. Suhling, and A. A. Anderson, *Proceedings of the 44th IEEE Electronic Components and Technology Conference*, p. 741–749 (1994).
[31]E. Lund and T. Finstad, *InterPACK '99: Pacific RIM/ASME International Intersociety Electronics Photonic Packaging Conference*, Advances in Electronic Packaging, p. 215–218 (1999).
[32]R. C. Jaeger, J. C. Suhling, M. T. Carey, and R. W. Johnson, IEEE Trans. Compon., Hybrids, Manuf. Technol. **16**, 925 (1993).
[33]J. Richter, M. B. Arnoldus, O. Hansen, and E. V. Thomsen, Rev. Sci. Instrum. **79**, 044703 (2008).
[34]D. A. Bittle, J. C. Suhling, R. E. Beaty, R. C. Jaeger, and R. W. Johnson, J. Electron. Packag. **113**(3), 203 (1991).
[35]S. Wang, *Fundamentals of Semiconductor Theory and Device Physics* (Prentice-Hall, Englewood Cliffs, NJ, 1989).
[36]W. A. Harrison, *Electronic Structure and Properties of Solids* (Dover, New York, 1989).
[37]T. B. Boykin, N. Kharche, and G. Klimeck, Phys. Rev. B **76**, 035310 (2007).
[38]T. B. Boykin, G. Klimeck, R. C. Bowen, and F. Oyafuso, Phys. Rev. B **66**, 125207 (2002).
[39]D. J. Chadi, Phys. Rev. B **16**, 790 (1977).

B.2 Review of Scientific Instruments

REVIEW OF SCIENTIFIC INSTRUMENTS **79**, 044703 (2008)

Four point bending setup for characterization of semiconductor piezoresistance

J. Richter,[a] M. B. Arnoldus, O. Hansen,[b] and E. V. Thomsen
Department of Micro- and Nanotechnology, Technical University of Denmark, DTU Nanotech Building 345 East, DK-2800 Kongens Lyngby, Denmark

(Received 30 November 2007; accepted 24 March 2008; published online 16 April 2008)

We present a four point bending setup suitable for high precision characterization of piezoresistance in semiconductors. The compact setup has a total size of 635 cm^3. Thermal stability is ensured by an aluminum housing wherein the actual four point bending fixture is located. The four point bending fixture is manufactured in polyetheretherketon and a dedicated silicon chip with embedded piezoresistors fits in the fixture. The fixture is actuated by a microstepper actuator and a high sensitivity force sensor measures the applied force on the fixture and chip. The setup includes heaters embedded in the housing and controlled by a thermocouple feedback loop to ensure characterization at different temperature settings. We present three-dimensional finite element modeling simulations of the fixture and discuss the possible contributions to the uncertainty of the piezoresistance characterization. As a proof of concept, we show measurements of the piezocoefficient π_{44} in *p*-type silicon at three different doping concentrations in the temperature range from $T=30\ ^\circ C$ to $T=80\ ^\circ C$. The extracted piezocoefficients are determined with an uncertainty of 1.8%. © *2008 American Institute of Physics.* [DOI: 10.1063/1.2908428]

I. INTRODUCTION

Since the pioneering work of Smith in 1954,[1] piezoresistivity of silicon has attracted attention from both academia[2–4] and industry.[5,6] Smith experimentally determined the three piezoresistance coefficients of lightly doped silicon. The piezoresistance coefficients for more heavily doped silicon were later experimentally determined by other research groups,[2,3] and still, today, the piezoresistance coefficients of silicon and other materials are topics of interest in both academia[4,7,8] and industry. The continued academic interest is partly due to the scarcity of reliable measurements and partly due to a discrepancy between theoretical models and available measurements especially for *p*-type silicon.[9–12]

Essentially, the piezoresistance effect is a change in the resistivity tensor (second order) caused by an applied stress.[13] The effect is characterized by a fourth order piezoresistivity tensor, which, in the case of silicon due to symmetry, has three independent coefficients.[14] The piezoresistance coefficients are dependent on sample temperature, doping level, and doping type.[2] In order to measure these coefficients and characterize the effect, it is necessary to apply a well controlled stress to the silicon sample with well defined resistors and measure the relative change in resistance of these.

In the original experiments by Smith,[1] silicon rods were pulled to apply a uniform uniaxial stress. Machined pull samples with through holes were used in Ref. 2 and a pull force was applied by pins inserted in the through holes.

For microfabricated thin film devices, it is more convenient to use a four point bending (4PB) fixture.[8,15–19] In Refs. 16 and 18 an optical method is used to measure the deflection and curvature of the chip. The stress is applied to the chip using a piezoelectric actuator and a translation stage, respectively. In Ref. 17, the displacement of the chip is known at the contact points between chip and 4PB fixture and this enables a calculation of the applied stress in the chip. Reference 8 and 15 use simple loads to apply the force and has no external measurement of the applied force. This is a cumbersome and time consuming method, especially for characterization at different temperatures.

We present a four point bending method where a motorized stepper actuator is used to apply a displacement while the force on the chip sample is measured with a dedicated force sensor. With this method, the measured force can be directly applied to calculate the stress. Thus, Young's modulus is not included in the stress calculation as is the case when a deflection is measured. The compact setup has a total volume of 635 cm^2.

The four point bending setup is designed and fabricated to analyze the piezoresistance coefficients of embedded piezoresistors located on a dedicated silicon chip. The main focus is to characterize the piezoresistivity of *p*-type silicon and other related semiconductor materials, e.g., Si under tensile strain[19] and compressively strained SiGe.[8] In this paper, we present measurements of the piezocoefficient π_{44} in *p*-type silicon with several different doping concentrations in the temperature range $T=30–80\ ^\circ C$ as an example of use of the setup. Boron doped silicon is the preferred piezoresistive material in commercial micro electromechanical systems (MEMS) due to the large piezocoefficient π_{44} and the very low values of the two other piezocoefficients π_{11} and π_{12}. When the piezoresistors are directed along certain crystal directions, ⟨110⟩, and placed in a Wheatstone bridge configu-

[a]Electronic mail: jar@mic.dtu.dk.
[b]Also at CINF-Center for Individual Nanoparticle Functionality, Department of Micro- and Nanotechnology, Technical University of Denmark, DTU Nanotech Building 345 East, DK-2800 Kongens Lyngby, Denmark.

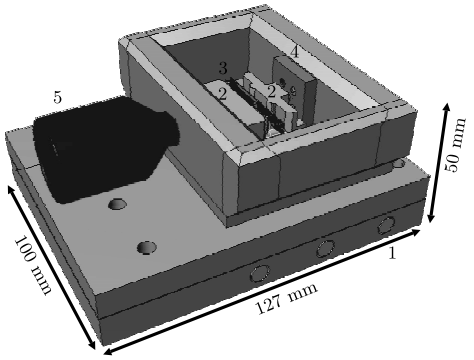


FIG. 1. Schematic of the complete piezoresistance characterization setup. The setup comprises cartridge heaters (1) that are embedded in the bottom plate of the Al housing surrounding the 4PB fixture (2) consisting of base and slider, the chip (3), and the force sensor (4). The actuator motor (5) is placed outside the Al housing to prevent heating of the motor.

ration, these piezocoefficients result in a high sensitivity of the MEMS device, since the effective longitudinal and transverse piezocoefficients are large and almost matched in magnitude but of opposite sign.

We characterize the 4PB setup using analytical expressions, finite element modeling (FEM), calibration measurements, and an application specific stress sensor chip. The stress distribution in a chip in the 4PB setup is thoroughly investigated and this analysis is used to estimate the uncertainties of the measured piezocoefficients.

II. APPARATUS

The piezoresistance characterization setup consists of a 4PB fixture with integrated thermocouples and temperature control. An actuator applies a displacement to the fixture and the force is measured by a force sensor. A schematic of the setup is shown in Fig. 1.

The fixture is placed in an aluminum housing including a metal lid (not shown in the figure) to stabilize temperature and shield off light. The thickness of the aluminum bottom plate and sidewalls are 10 and 20 mm, respectively. Aluminum has a very high thermal conductivity of 239 $\mathrm{W/m\,K^{-1}}$ (Ref. 20) compared to air ($\approx$0.02 $\mathrm{W/m\,K^{-1}}$), ensuring a uniform heat distribution in the aluminum casing.

The 4PB fixture is guided along the axis of the actuator by small rails in the bottom plate of the setup. The contact area between the rails and the 4PB fixture is very small (40 $\mathrm{mm^2}$) which minimizes friction between fixture and bottom plate. The frictional force may be even lower in a vertical design, however, the horizontal design was chosen in order to use gravity to assist alignment of the different parts of the setup and of the sample.

A. Four point bending fixture

An exploded view of the 4PB setup is shown in Fig. 2. It consists of a base part containing two blades separated by a distance of 28 mm and a sliding part where two more blades are formed separated by a distance of 12 mm. The base part slides on two rails formed in the bottom plate of the setup casing. The sliding part is in contact with the base only at two steel pins that ensure good directional control of the force and low frictional force. A dedicated silicon chip is placed in between the sliding part and the base part; the force is applied to the chip by the four blades.

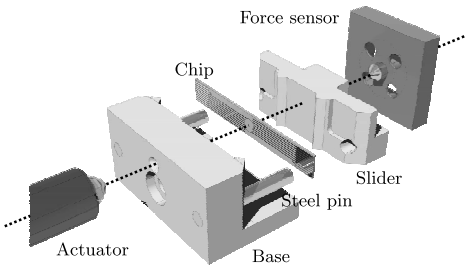


FIG. 2. Exploded view of the setup illustrating the uniaxial force interaction between actuator, 4PB fixture, chip, and force sensor. This ensures uniformity of the stress in the center region of the chip.

The 4PB fixture applies a uniaxial and uniform stress distribution to the center region of the chip. The bending force F is measured using a force sensor. From simple bending beam theory, we obtain the stress σ_{xx} (Ref. 8)

$$\sigma_{xx} = \frac{6Faz}{wh^3}, \tag{1}$$

where h is the thickness of the chip, z is the position of the resistor with respect to the neutral plane of the chip, i.e., $z=h/2$ at the surface, a is the distance between the inner and outer blades of the 4PB fixture, and w is the width of the chip.

The 4PB fixture is made from the thermoplastic material polyetheretherketon (PEEK) which is a semicrystalline material. Young's modulus of PEEK is $Y=3.5$ GPa and the mechanical properties are quite stable in the temperature range from -64 to 250 °C.[21]

The vertical alignment of the chip to the 4PB fixture is ensured by resting the chip on the two steel pins in the setup (see Fig. 2). Horizontal alignment of the chip is done by visual inspection. The stress is considered constant in the area between the two inner blades on the slider. The dimensions of the resistor are much smaller than the 12 mm distance between the two inner blades. Thus, the resistors which are located in the middle region between the two inner blades experience a uniform stress.

B. Force sensor

The force sensor is a Strain Measurement Devices s415 button cell.[22] It consists of a plate with four sputter defined resistors in a Wheatstone bridge configuration. The force sensor is fastened to the setup casing. An input voltage, $V_{\mathrm{in}} = 10$ V, is applied to the bridge. The output voltage of the Wheatstone bridge, V_o, depends linearly on the force F, as described by

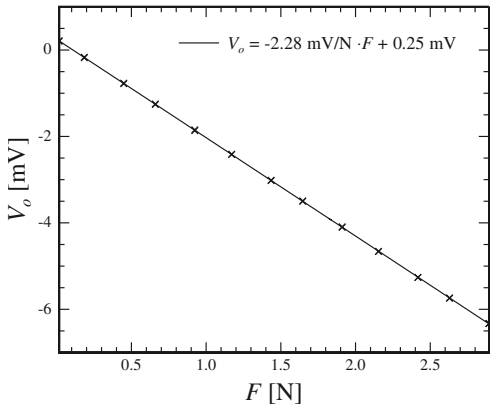


FIG. 3. Force sensor calibration curve at $T=30$ °C. A force F is applied by adding weights to the force sensor with an input voltage $V_{in}=10$ V while the output voltage, V_o of the Wheatstone bridge is measured. The slope and offset of linear fit (solid line) at different temperatures are listed in Table I.

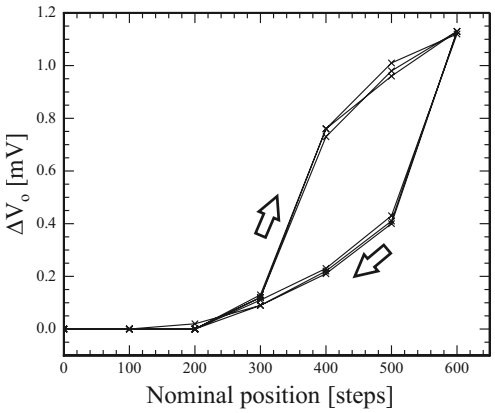


FIG. 4. Actuator position hysteresis. The force sensor output voltage $\Delta V_o = V_o - V_{off}$ as a function of the nominal actuator displacement in three subsequent measurement series. The output voltage depends on the direction of the actuator motion due to a hysteresis in the actual actuator position.

$$F = \frac{1}{\alpha}(V_o - V_{off}), \tag{2}$$

where $1/\alpha$ is the constant of proportionality and V_{off} is the offset voltage.

The constant α is measured in a calibration setup where the force sensor is horizontally placed and well known forces are applied using weights of different masses. The calibration curve at $T=30$ °C is shown in Fig. 3, where the calibration constant, α, is determined as the slope of the linear fit. The force sensor showed a small hysteresis in the output when increasing and decreasing the applied force. The hysteresis is described by a 0.3% change in the calibration constant and this will not significantly contribute to the uncertainty. The force sensor was calibrated at different temperatures (see Table I). The temperature dependence of α is significant and the values in Table I are included in the analysis.

The force sensor offset is a result of imbalance in the thin film Wheatstone bridge and the actual force sensor temperature. This offset has no influence on the measurements since the force sensor is offset compensated before the actual measurement.

C. Actuator

The motorized Newport NSA12 microstep actuator[23] used in the setup has a resolution of 0.3 μm and a maximum loading capacity of 25 N. The actual force on the actuator is of no interest since the force on the chip is measured by an independent force sensor. Characterization of the actuator has shown severe hysteresis during increasing and subsequent decreasing loads. The displacement of the actuator is affected by the force thus the actual position of the actuator is not reliable (see Fig. 4). The actuator is, in turn, increasing the load on the chip and decreasing the load while the output voltage on the force sensor is measured. Since previous characterization in Fig. 3 showed that the force sensor signal linearly depends on the applied force, we conclude that the hysteresis is caused by the actuator. This actuator hysteresis has no influence on the piezoresistance measurements since the force sensor signal (and not the actuator displacement) is used in the characterization.

TABLE I. Force sensor calibration. The table summarizes the slope α and offset V_{off} of the linear fits to experimentally obtained force-voltage curves at four different temperatures with an input voltage of $V_{in}=10$ V.

T (°C)	V_{off} (m V)	α (m V/N)
30	0.25	2.280
47	0.10	2.290
64	−0.05	2.294
81	−0.20	2.312

D. Temperature monitor and control

The setup contains two integrated thermocouples. One thermocouple is placed in air close to the chip and reads the temperature near the chip. The other thermocouple is attached to the aluminum casing. This thermocouple supplies a feedback signal to the temperature controller. The thermocouples have small thermal masses resulting in a fast response time. The temperature is read using a Pico Technologies data logger.[24]

A Watlow series 96 temperature controller is used to control the temperature and a Watlow solid state DIN-A-MITE power relay supplies bias current to three Watlow cartridge heaters embedded in the aluminum plate placed below the setup, as seen in Fig. 1. The actuator has a temperature operating range between 5 and 40 °C, thus cooling of the actuator is necessary. This is done using an ARX Cera Dyne fan and a heat sink on the actuator. A metal shield between the fan and the metal casing prevents significant cooling of the setup casing.

The time to reach a given temperature is measured to be less than $t_{eq}=20$ min. This is done by measuring the temperature inside the Al housing as a function of time at a

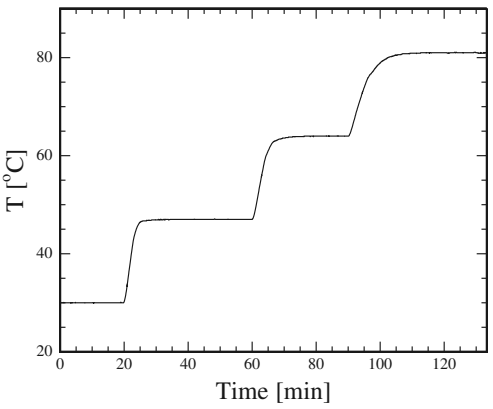


FIG. 5. The temperature readout from the thermocouple placed inside the aluminum housing near the chip as a function of time. The temperature is sequentially set to the values T=30, 47, 64, and 81 °C. The maximum time for equilibrium is t_{eq}=20 min seen when the temperature is increased from 64 to reach 81 °C.

given set temperature. Figure 5 shows the temperature development at set temperatures 30, 47, 64, and 81 °C. The maximum equilibration time is t_{eq}=20 min when increasing the temperature by 17 °C from 64 °C. All measurement series are performed by increasing the temperature in steps of 10 °C, thus thermal equilibrium is reached within less than 20 min.

E. Chip design

The silicon chip to be inserted in the setup is a 4 cm long and 5.3 mm wide beam. The resistors are fabricated on 350 μm (001) silicon on insulator wafers with a device layer of 2 μm. The device layer is thinned down to 500 nm by oxidation thinning. The piezoresistors are formed in the 500 nm thick device layer by boron doping using ion implantation. The implanted doses were $D=1.5\times10^{13}$, 1.5×10^{14}, and 1.5×10^{15} cm^{-2}, respectively, all at an energy of 50 keV. The resulting final doping concentrations in the samples are then $N_A=1.5\times10^{17}$, 2.0×10^{18}, and 2.2×10^{19} cm^{-3}, respectively. The fabrication of the piezoresistors was performed by using a long postoxidation annealing which activates the acceptors and results in an extremely uniform doping profile in the piezoresistors, as verified in a simulation using the SILVACO ATHENA process simulator.[25] The piezoresistors are patterned using UV lithography and reactive ion etching (RIE). Contact windows in the oxide are formed using buffered HF on a photoresist mask. This mask is also used to pattern an additional high dose (5×10^{15} cm^{-2}) boron ion implant to improve the contact resistance. A Ti/Al metal layer is deposited in a lift-off process to form interconnects and electrical contact to the piezoresistors. Finally, the chips are diced in a deep RIE using the Bosch process[26] with an etch angle of 90° ± 1° to accurately define the chip direction with respect to the crystal orientation. A cross sectional schematic of the chip is shown in Fig. 6.

The chip layout is sketched in Fig. 7. This test chip is

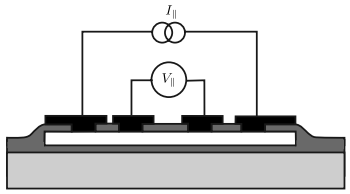


FIG. 6. Schematic cross section of the chip. The silicon piezoresistor (white) is surrounded by silicon dioxide (dark gray) and electrically connected by Al/Ti metal tracks (black) on a silicon substrate (light gray). The electrical resistance measurement is performed by a four terminal high impedance voltage measurement where a current $I_\parallel$ is forced through the resistor from the outer contacts while a voltage drop $V_\parallel$ is measured on the inner contacts.

designed to measure the piezocoefficient π_{44} and the sum of the two other coefficients $\pi_{11}+\pi_{12}$ in p-type silicon. The relative resistance change, $\Delta R/R$, in a resistor with an applied uniaxial stress, σ_{xx}, is given by[8]

$$\frac{\Delta R}{R} = \sigma_{xx}\left[\frac{\pi_{11}+\pi_{12}+\pi_{44}\cos(2\theta)}{2}\right], \tag{3}$$

where $R=V_\parallel/I_\parallel$ is the resistance according to Figs. 6 and 7(b) and θ is the angle of the resistor direction with respect to the σ_{xx} stress direction, i.e., [110] according to Fig. 7(a). By plotting the relative resistance change as a function of the applied stress, we obtain a value of the bracketed piezocoefficient linear combination in Eq. (3) for each resistor. This value is plotted as a function of $\cos(2\theta)$ to determine the piezocoefficient π_{44} as the slope of a linear fit and the sum $(\pi_{11}+\pi_{12})$ as the offset of a linear fit.

F. Electrical measurements

The full electrical setup is sketched in Fig. 8. A thermocouple placed in the Al housing supplies the signal to a feedback loop for the heaters in the bottom of the Al housing through the temperature controller. A Keithley 2400 sourcemeter and a Keithley 2700 multimeter are used for the electrical measurements on the chip with a simple four ter-

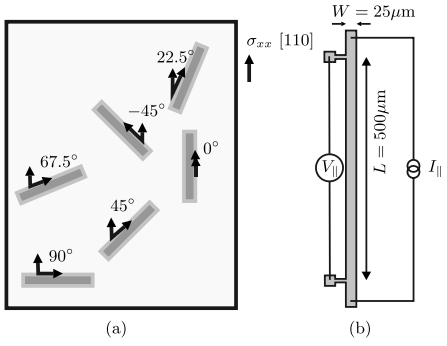


FIG. 7. Chip design for piezoresistance measurements, not to scale. (a) The chip has six resistors all placed in the center region of the chip. The resistors are oriented along the different angles with respect to the [110] stress direction. (b) A close-up of the resistor showing the four terminal electrical resistance measurement used on each resistor.

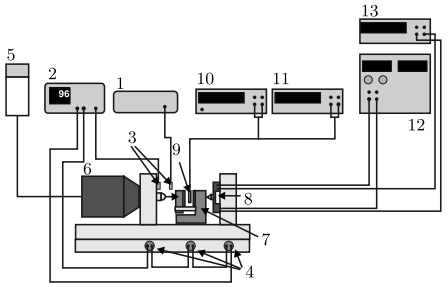


FIG. 8. A schematic of the complete setup. (1) Temperature logger. (2) proportional-integral-derivative temperature controller. (3) Thermocouples. (4) Cartridge heaters. (5) Motion controller. (6) Actuator. (7) 4PB fixture. (8) Force sensor. (9) Chip. (10) Keithley 2700 Multimeter with multiplexer. (11) Keithley 2400 sourcemeter. (12) TTi EL302T triple Power Supply. (13) Keithley 2000 multimeter.

minal measurement, as illustrated in Fig. 6. The force sensor is connected to a power supply and a multimeter. All instruments are controlled via a NATIONAL INSTRUMENTS LABVIEW software interface.

The chip is contacted using zero insertion force flat flexible cable (FFC) connectors [Molex Electronics, part No. 52746-1090 (Ref. 27)], as shown in Fig. 9. The connectors do not influence the stress distribution in the chip and allow for mechanical movement of the chip.

III. ERROR ESTIMATES

The accuracy of the piezoresistance measurements depends on several factors associated with the 4PB fixture. First, the inaccuracy of the intended uniaxial stress caused by force and geometry errors is discussed. Second, deviations from the assumed uniaxial stress distribution caused by model insufficiencies and alignment errors are analyzed using FEM and analytical approaches. Third, we discuss the contribution from errors due to the electronic equipment. Finally, the frictional forces in the setup are outlined and their contribution to the piezoresistance measurement is discussed.

A. Stress uncertainty

The stress at the surface ($z=h/2$) is determined by Eq. (1), thus the relative uncertainty in the applied stress is given by

$$\frac{\Delta\sigma_{xx}}{\sigma_{xx}} = \sqrt{\left(\frac{\Delta F}{F}\right)^2 + \left(\frac{\Delta a}{a}\right)^2 + 2\left(\frac{\Delta h}{h}\right)^2 + \left(\frac{\Delta w}{w}\right)^2}. \quad (4)$$

The uncertainty of the applied force F we obtain from the standard deviation on the calibration factor α and an estimate of the precision of the actual electrical measurement on the force sensor. This gives an uncertainty on the measured force of 0.25%. The distance between the inner and outer blades in the 4PB fixture is $a=8.0$ mm with an uncertainty of $\Delta a=0.1$ mm. The chip thickness is $h=356$ μm with an uncertainty of $\Delta h=2$ μm. The chip dimensions are individually measured. The width of the chip, $w=5.3$ mm, is accurately defined by photolithography, as described in Sec. II E and the uncertainty can be assumed to be negligible compared to the above values. The vertical sidewalls of the chip are obtained from the deep RIE to have an angle of $90° \pm 1°$. This angle results in a negligible difference of the width of 2×6 μm^2 on front side compared to back side of the chip. Thus, the relative uncertainty of the induced stress is

$$\frac{\Delta\sigma_{xx}}{\sigma_{xx}} = \sqrt{(0.0025)^2 + \left(\frac{0.1}{8.0}\right)^2 + 2\left(\frac{2}{356}\right)^2} = 1.5\,\%. \quad (5)$$

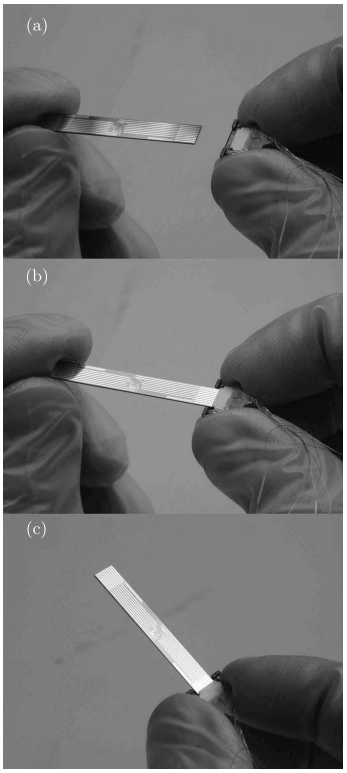


FIG. 9. The chip is electrically interfaced through zero insertion force flat flexible cable (FFC) connectors. The assembly is an easy "plug and measure" method, (a) before insertion of chip in the connector, (b) during insertion, and (c) the chip is connected to the electronic instrumentation.

B. Stress distribution: FEM analysis

The stress distribution in the chip is simulated in COMSOL MULTIPHYSICS 3.3. In the simulation, the inner blades of PEEK are constrained in the z direction on the bottom surface of the PEEK mass. The outer blades each have a distributed force, $F/2$ on the surface plane. The chip is assigned the elastic parameters Young's modulus $Y=170$ GPa and Poisson's ratio $\nu=0.07$ from Ref. 28, since the chip is stressed along the [110] direction. Figure 10(a) shows the stress distribution σ_{xx} in the chip at a force of $F=2.5$ N. The resistor area in the center region of the chip is sketched by the dashed square (3×3 mm^2). The in-plane stress distribu-

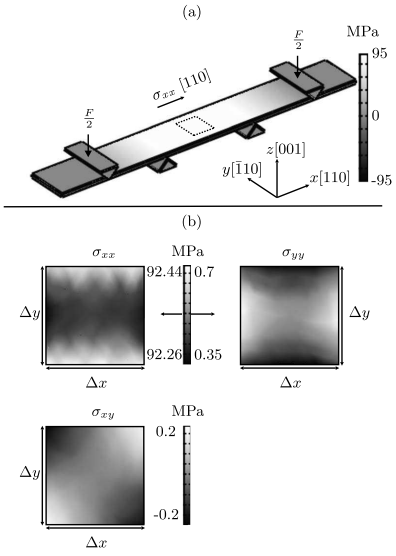


FIG. 10. FEM analysis of the 4PB setup. (a) Gray-scale encoded stress distribution σ_{xx} in the chip placed in the 4PB fixture with an applied force F. The area marked by a dashed square ($\Delta x \times \Delta y = 3 \times 3$ mm^2) indicates the location of the piezoresistors in the surface of the chip center. In (b), a zoom-in on this area shows all in-plane stress distributions, σ_{xx}, σ_{yy}, and σ_{xy}. Notice the different scales, the stress σ_{xx} is more than 100 times larger than σ_{yy} and σ_{xy}.

tions (σ_{xx}, σ_{yy}, and σ_{xy}) in the resistor area are shown in Fig. 10(b).

Since the chip is subjected to pure bending, we expect an exact solution to the problem with σ_{xx} given by Eq. (1) and all other stress components to be zero for a narrow chip. However, due to the rather large width to length ratio, $w/l = 0.13$, the chip is also subjected to a transverse stress. As is seen in Fig. 10(b), this transverse stress is at least a factor 100 less than the stress σ_{xx}.

Ideally, the blades are considered sharp wedges contacting the chip in lines. Real blades will have a finite width in the contact area. FEM analysis shows that even 30 μm wide contact areas causes a change in σ_{xx} less than 0.6% and insignificant changes to σ_{yy} and σ_{xy}. Considering the quality of the milling machine used in the fabrication of the setup, these effects are insignificant.

C. Horizontal blade misalignment: FEM analysis

FEM is used to describe the influence of a possible misalignment of the blades. The simulations are done with a total misalignment of $\phi = \pm 2°$ on each blade in order to analyze the effect (see illustration in Fig. 11). The investigation is summarized in Table II, where the ratio of the stress components are listed for different blade configurations. The ratios listed are the maximum values obtained in the resistor area. To obtain the maximum value of σ_{yy}/σ_{xx}, the (x,y) coordinate is (1.5 mm, 0). The maximum σ_{xy}/σ_{xx} value is found in the coordinate (1.5, 1.5 mm).

TABLE II. Results of a FEM analysis of blade rotation. The blades are rotated with a worst case misalignment of $\phi = 2°$ according to Fig. 11. Column 2: the relative difference in the extracted FEM σ_{xx} and the analytically calculated stress $\sigma_{xx,an}$ in the center of the chip surface. Column 3: σ_{yy}/σ_{xx} at the chip surface in $(x,y) = (1.5\text{ mm}, 0)$. Column 4: σ_{xy}/σ_{xx} at the chip surface in $(x,y) = (1.5, 1.5\text{ mm})$.

Configuration	$\frac{\Delta\sigma_{xx}}{\sigma_{xx,an}}$	$\frac{\sigma_{yy,max}}{\sigma_{xx}}$	$\frac{\sigma_{xy,max}}{\sigma_{xx}}$
A,B,C,D: $\phi = 0°$	0.1%	0.8%	0.3%
B,C,D: $\phi = 0°$; A: $\phi = 2°$	0.2%	0.8%	0.2%
B,C: $\phi = 0°$; A,D: $\phi = 2°$	0.1%	0.8%	0.2%
B,C: $\phi = 0°$; A: $\phi = 2°$; D: $\phi = -2°$	0.2%	0.8%	0.2%
A,C,D: $\phi = 0°$; B: $\phi = 2°$	0.2%	0.8%	1.9%
A,D: $\phi = 0°$; B,C: $\phi = 2°$	0.4%	0.7%	3.5%
A,D: $\phi = 0°$; B: $\phi = 2°$; C: $\phi = -2°$	0.2%	0.7%	0.3%

Notice, that the σ_{xx} stress in all cases varies less than 0.5% with respect to the analytical expression in Eq. (1). It is also seen that the transverse stress, σ_{yy}, does not depend on the blade misalignment. Thus, we assume that this stress is constant and less than 0.8% of the σ_{xx} stress. A misalignment of the outer blades, A and D in Fig. 11 does not have a significant impact on the stress distribution. However, a misalignment of the inner blades does change the shear stress distribution. As listed in Table II, the largest shear stress, $\sigma_{xy}/\sigma_{xx} = 3.5\%$, is obtained with a rotation in the same direction of the two inner blades.

The above values are extracted for a 2° horizontal rotation of the blades. This rotation is very large compared to the realistic value, but it is used in order to illustrate the influence. The milling machine used to fabricate the 4PB fixture has a very high precision (precision of 1 μm), thus, it is not expected that a horizontal misalignment influences the stress distribution in the chip.

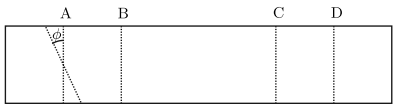


FIG. 11. Top-view schematic of chip and blades (A)–(D). In the FEM analysis, each blade is rotated an angle ϕ. The stress distribution for different configurations of blade rotation is listed in Table II.

D. Vertical blade misalignment

A vertical rotation of the two inner blades as sketched in Fig. 12 results in a pure torsion of the beam. The resulting shear stress in the surface can be described by[29]

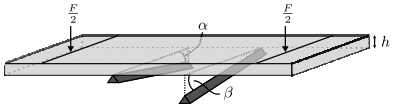


FIG. 12. Schematic of chip exposed to torsion due to vertical misalignment α and β of the inner blades. The outer blades each applies a line force of $F/2$ to the chip of thickness h.

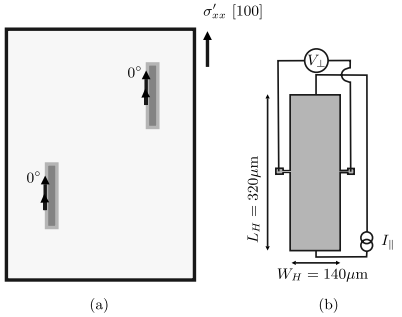


FIG. 13. (a) Schematic showing the design of the dedicated shear stress sensor chip. The chip consists of two resistors each placed in a corner of the 3×3 mm^2 resistor area in the middle of the chip. (b) The current $I_\parallel$ is forced through the resistor and a voltage drop $V_\perp$ is measured perpendicular to the current direction. The illustrations are not to scale.

$$\sigma_{xy} = Gh\frac{\Delta\psi}{\Delta x}, \tag{6}$$

where the elastic shear modulus $G=Y/(2+2\nu)$, $\Delta\psi=\alpha+\beta$ in Fig. 12 measured in radians, and the distance between the two inner blades of the chip $\Delta x=12$ mm. For example, at a misalignment angle of $\Delta\psi=0.1°$, the shear stress component is as large as $\sigma_{xy}=4$ MPa.

E. Shear stress measurement and discussion

In order to investigate the actual shear stress component during measurements, we have fabricated a dedicated shear stress sensor chip with the long axis along [100]. The chip design is shown in Fig. 13 where the primed coordinate system is along the ⟨100⟩ crystal axes. A constant current $I_\parallel$ is forced through the resistor while the potential drop $V_\perp$ perpendicular to the current is measured. The relation between shear stress, σ'_{xy}, and resistance $R_H=V_\perp/I_\parallel$ is

$$\frac{\Delta R_H}{R_\square}[100] = \frac{1}{2}\pi_{44}\sigma'_{xy}, \tag{7}$$

where $R_\square$ is the sheet resistance. The result of this measurement is shown in Fig. 14 and proves that there is a nonideal shear stress distribution in the chip. The figure shows a linear relation between the resistance change and the applied stress σ'_{xx}. Thus, when increasing σ'_{xx}, the shear stress also increases. Inserting a measured value of $\pi_{44}=85\times10^{-11}$ Pa^{-1} (measured at a doping concentration of $N_A=2.2\times10^{19}$ cm^{-3} and $T=30$ °C) in Eq. (7), we obtain $\sigma'_{xy}=3$ MPa and $\sigma'_{xy}=2$ MPa for the two resistors, respectively, at $\sigma'_{xx}=85$ MPa. Thus, we find a shear stress component value which is 3.6% and 2.5% of the σ'_{xx} value. The two resistors are placed in two different corners of the resistor area sketched in Fig. 10, thus, we assume that all resistors experience a shear stress which is in between these two values.

The shear stress is most likely caused by vertical misalignment of the inner blades, since a very small vertical misalignment results in a rather large shear stress component as argued in Eq. (6). In order to accommodate a shear stress of $\sigma'_{xy}=3$ MPa for $\sigma'_{xx}=85$ MPa, the vertical misalignment of the inner blades is $\Delta\psi=0.07°$. A FEM of the shear stress in a chip placed in a 4PB fixture as a function of vertical misalignment of the outer blades is performed in Ref. 30. They report a linear relation between the applied force and shear stress until full contact between the vertically misaligned blades and chip is reached. By further increasing the force, the shear stress contribution approaches a constant value. In Fig. 14, it is seen that the shear stress linearly depends on the applied force in the measured stress interval and taking the results from Ref. 30 into account, we find that the inner blades may be misaligned at a larger angle than $\Delta\psi=0.07°$. The actual misalignment angle can be measured by increasing the stress even further than what is seen in Fig. 14. Thus, if the shear stress is caused by a vertical misalignment of the inner blades, we conclude that the misalignment is at least $\Delta\psi=0.07°$. Another contribution to the shear stress may rise from an in-plane misalignment of the inner blades, as described in Sec. III B. A misalignment of $\phi\approx2°$ of both inner blades need to be present in order to accommodate the measured shear stress and considering the precision of the mechanical equipment used to machine the 4PB (precision $=1$ μm), this is not possible. A third contribution is a rotation of the whole PEEK 4PB fixture. The distance between the guiding rails in the bottom of the aluminum housing is 0.15 mm larger than the width of the 4PB base to accommodate thermal expansion of the two materials. Thus, a rotation of the 4PB fixture is possible. However, due to the very small air gap, the rotation angle is at most 0.3° and this does not significantly contribute to the shear stress. A fourth contribution to the shear stress is a misalignment of the slider and the base. However, since the two steel pins and guiding holes are specifically fabricated to fit each other with a very small air gap, this is not expected to induce a significant shear stress. Thus, we conclude that the present shear stress in the chip is an effect from a vertical rotation of the inner blades in the 4PB fixture.

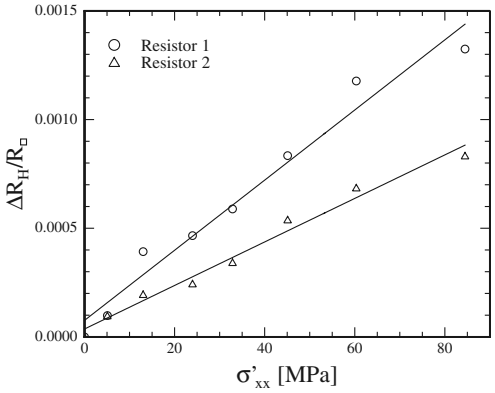


FIG. 14. Plot of the relative resistance change $\Delta R_H/R_\square$ for the two resistors on the shear stress sensor chip at a temperature of 30 °C as a function of applied stress σ'_{xx} along [100]. The resistance change indicates the presence of a shear stress component σ'_{xy} proportional to σ'_{xx}.

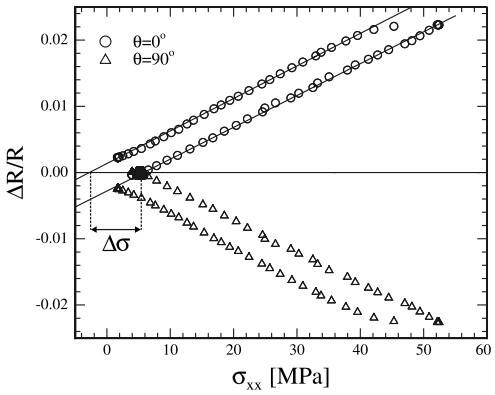


FIG. 15. The relative change in resistance $\Delta R/R$ when increasing and decreasing the load. The measurement data from two resistors, $\theta=0°$ and $\theta=90°$ in Fig. 7(a), are plotted as a function of the applied stress σ_{xx} at $T=30$ °C. The solid lines are linear fits to the data. The lateral distance between the fit lines is a measure of the frictional force described by $\Delta\sigma=2\sigma_f$.

F. Electronic setup

The electronic instruments used to measure the voltage drop and to inject the current are all high precision instruments. The Keithley 2700 multimeter with multiplexer has a resolution of 1 μV at a voltage of 1 V and the Keithley 2400 sourcemeter has a current source accuracy of 0.03% at 100 μA. These uncertainties are significantly smaller than the uncertainties described in Sec. III A.

G. Friction

Frictional forces are expected to be present in the four point bending fixture since it consists of two parts where one is moving (slider) with respect to the other (base). Figure 15 shows a characterization of two resistors during sequential increasing and decreasing loads where the resistance change is measured at each applied load. For both resistors, a hysteresis loop is seen where the measured data are shifted to the right during increasing loads and to the left during decreasing loads. This behavior is explained by the frictional force, F_f, between the slider and the base, while we conclude from the force diagram sketched in Fig. 16 that the frictional force, F_{ch}, between the 4PB base and the aluminum housing does not affect the measurements. The only significant frictional force contribution is from the movement of the slider on the steel pins. The frictional force may be a multivalued

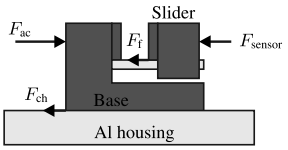


FIG. 16. Force diagram of the 4PB fixture. The actuator applies a force F_{ac} to the 4PB fixture and the force on the force sensor is F_{sensor}. The frictional force, F_{ch}, between base and aluminum housing does not contribute to the frictional force seen in Fig. 15. The only contribution to this is the frictional force between base and slider F_f.

function of the velocity $\mathbf{v}$ in a stick-slip fashion. At rest, the magnitude of the applied force must exceed the static stiction-friction force, F_{f00}, to initiate motion, while in motion, the frictional force may be assumed to have a static and a dynamic component, $\mathbf{F}_f=\mathbf{F}_f(\mathbf{v})=-F_{f0}\mathbf{v}/|\mathbf{v}|-\beta\mathbf{v}$, where $F_{f00}\geqslant F_{f0}$ and β is a viscous friction coefficient. In a steady state sequence of measurement steps in a given direction, the stiction-friction force is unimportant, as is the viscous friction, since the important frictional force is found when motion stops. Thus, we expect the relation, $F_{\mathrm{sensor}}=F_s\pm F_{f0}$, between the force, F_{sensor}, measured on the force sensor and the actual force, F_s, on the sample in the 4PB fixture, where the sign depends on the direction of motion.

The force F_{f0} can be estimated from the width of the hysteresis loop in the stress direction, $\Delta\sigma\simeq 2\sigma_{f0}\simeq 8.2$ MPa, as seen in Fig. 15. This corresponds to a frictional force of $F_{f0}=0.11$ N. If this frictional force is load independent, it does not affect the piezoresistance characterization since only the slopes of the linear fits to the measured resistance change during increasing or decreasing loads are used. We do, however, slightly find different slopes for increasing and decreasing loads, such that they equal the mean slope $\pm 0.6\%$. This uncertainty must be included in the total uncertainty derived in Sec. III A.

H. Discussion

In Eq. (3), only the effect of the stress σ_{xx} was considered. However, if all in-plane stress components are included, we obtain a relative resistance change $\Delta R/R$ of

$$\frac{\Delta R}{R}=\sigma_{xx}\left[\frac{\pi_{11}+\pi_{12}+\pi_{44}\cos(2\theta)}{2}\right]+\sigma_{yy}\left[\frac{\pi_{11}+\pi_{12}-\pi_{44}\cos(2\theta)}{2}\right]+\sigma_{xy}(\pi_{11}-\pi_{12})\sin(2\theta). \quad (8)$$

In p-type silicon, the piezocoefficient π_{44} is much larger than π_{11} and π_{12}, i.e., $|\pi_{11}/\pi_{44}|\approx 0.8\%$ and $|\pi_{12}/\pi_{44}|\approx 4.3\%$.[1] Moreover, the maximum value of the shear stress in the chip was measured to be 3.6% of σ_{xx}. Thus, it follows from Eq. (8) that the shear stress causes an insignificant error.

However, the contribution from the stress σ_{yy} cannot be neglected since its effect is proportional to the large piezocoefficient π_{44} in Eq. (8). From the FEM analysis, we conclude that the contribution from σ_{yy} is approximately 0.8% of the contribution from σ_{xx}. Including this contribution (and the contribution from the uncertainty of the linear fits from Sec. III G) in the uncertainty calculation of the magnitude of σ_{xx} in Sec. III A, we conclude that the piezocoefficient π_{44} is determined with an uncertainty of 1.8%.

IV. SAMPLE CHARACTERIZATION

The chips presented in Sec. II E have been characterized in the 4PB setup. An example of a measurement series at $T=30$ °C on a chip with a doping concentration of $N_A=1.5\times 10^{17}$ cm^{-3} is shown in Fig. 17 for increasing loads. The

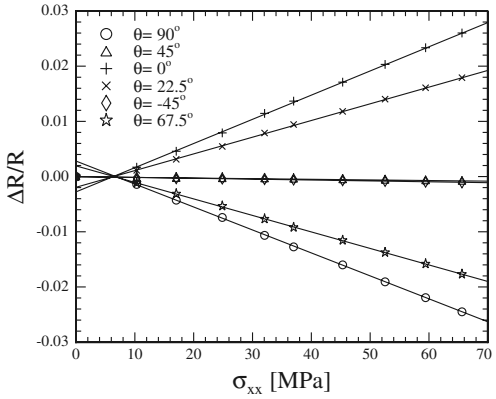


FIG. 17. Relative change in resistance $\Delta R/R$ for the six resistors sketched in Fig. 7(a) as a function of the applied stress. The solid lines are the linear fits to the data series. Notice, the nonzero intercept with the x axis which is due to the frictional force explained in Sec. III G.

figure shows measurements on a chip with six resistors oriented at six different angles, θ, with respect to the stress direction, [110]. The slopes of the linear fits found in Fig. 17 are plotted for each resistor in Fig. 18 as a function of $\cos(2\theta)$ according to Eq. (3). The slope of the linear fit to these data is proportional to the piezocoefficient π_{44}, as seen in Eq. (3).

This analysis has been done for samples with the three doping concentrations given in Sec. II E at temperatures from $T=30$ °C to $T=80$ °C. The results are shown in Fig. 19 where the measured piezocoefficients are plotted as a function of doping density with the measurement temperature as parameter. The data in the figure are in good agreement with the doping concentration and temperature dependence in previous published results.[2] The analysis in Sec. III concluded that errors due to shear stress are negligible, the error contribution from σ_{yy} is at most 0.8%, and the uncertainty in the σ_{xx} value is 1.5%. The slope of the linear fit to the data is found with an uncertainty of 0.6%, thus, the presented 4PB setup allows measurements of the piezocoefficient π_{44} in p-type silicon at different doping concentrations and temperatures with an uncertainty of 1.8%.

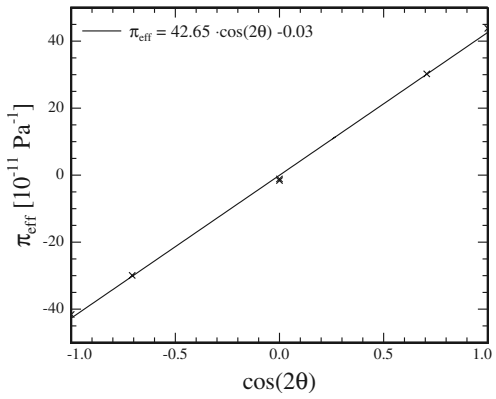


FIG. 18. The slopes of the linear fits in Fig. 17, the effective piezocoefficients π_{eff}, are plotted as a function of $\cos(2\theta)$, where θ is the angle between the resistor direction and the [110] σ_{xx} stress direction. The slope of the linear fit (solid line) is equal to $\pi_{44}/2$.

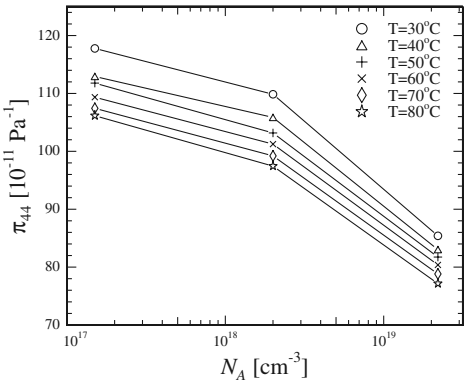


FIG. 19. The measured piezocoefficient π_{44} in p-type silicon as a function of temperature and doping concentration N_A.

ACKNOWLEDGMENTS

Center for Individual Nanoparticle Functionality (CINF) is sponsored by The Danish National Research Foundation. We are grateful for financial support from Grundfos A/S.

[1] C. S. Smith, Phys. Rev. **94**, 42 (1954).
[2] O. N. Tufte and E. L. Stelzer, J. Appl. Phys. **34**, 313 (1963).
[3] R. C. Jaeger and J. C. Suhling, IEEE Trans. Compon., Hybrids, Manuf. Technol. **16**, 925 (1993).
[4] E. Lund and T. Finstad, *Proceedings of the 1999 Advances in Electronic Packaging* (unpublished), Vol. 12, p. 215.
[5] Grundfos A/S (www.grundfos.com).
[6] Infinion Technologies SensoNor A/S (www.sensonor.no).
[7] P. Yang and R. He, Nat. Nanotechnol. **1**, 42 (2006).
[8] J. Richter, O. Hansen, A. Nylandsted Larsen, J. Lundsgaard Hansen, G. F. Eriksen, and E. V. Thomsen, Sens. Actuators, A **123–124**, 388 (2005).
[9] Y. Kanda, IEEE Trans. Electron Devices **ED-29**, 64 (1982).
[10] J. A. Harley and T. W. Kenny, J. Microelectromech. Syst. **9**, 226 (2000).
[11] S. I. Kozlovskiy, V. V. Nedostup, and I. I. Boiko, Sens. Actuators, A **133**, 72 (2007).
[12] T. Toriyama and S. Sugiyama, J. Microelectromech. Syst. **11**, 598 (2002).
[13] C. S. Smith, *Macroscopic Symmetry and Properties of Crystals*, Solid-State Physics Vol. 6 edited by F. Seitz and D. Turnbull (Academic, New York, 1957).
[14] J. Nye, *Physical Properties of Crystals*, 1st ed. (Oxford University Press, Oxford, 1957).
[15] R. E. Beaty and R. C. Jaeger, IEEE Trans. Compon., Hybrids, Manuf. Technol. **15**, 904 (1992).
[16] E. Lund and T. G. Finstad, Rev. Sci. Instrum. **75**, 4960 (2004).
[17] J. Bartholomeyczik, S. Brugger, P. Ruther, and O. Paul, IEEE Sens. J. **5**, 872 (2005).
[18] V. Weihnacht, W. Bruckner, and C. M. Schneider, Rev. Sci. Instrum. **71**, 4479 (2000).
[19] J. Richter, O. Hansen, A. Nylandsted Larsen, J. Lundsgaard Hansen, and E. V. Thomsen, *2006 MRS Fall Meeting*, MRS Symposia Proceedings No. 958 (Materials Research Society, Pittsburgh, 2006) p. 133.
[20] C. J. Smithells, *Smithells Metals Reference Book*, edited by E. A. Brandes and G. B. Brook (Butterworth-Heinemann, Oxford, UK, 1992).
[21] Victrex (www.victrex.com).
[22] Strain Measurement Devices (www.smdsensors.com).

[23] Newport Corporation (www.newport.com).
[24] Pico Technology (www.picotech.com).
[25] Silvaco Deckbuild (www.silvaco.com).
[26] F. Laermer and A. Schilp, U.S. Patent No. 5,501,893 (August 5, 1994).
[27] Molex Electronics (www.molex.com).
[28] J. J. Wortman and R. A. Evans, J. Appl. Phys. **36**, 153 (1965).
[29] S. P. Timoshenko and J. N. Goodier, *Theory of Elasticity* (McGraw-Hill, New York, 1970).
[30] J. Bartholomeyczik, S. Brugger, S. Kibbel, P. Ruther, and O. Paul, Proceedings of the Eurosensors, 2005 (unpublished), Paper No. TB23.

B.3 Sensors and Actuators

Available online at www.sciencedirect.com
SCIENCE DIRECT®
Sensors and Actuators A 123–124 (2005) 388–396
SENSORS AND ACTUATORS A PHYSICAL
www.elsevier.com/locate/sna

Piezoresistance of silicon and strained $Si_{0.9}Ge_{0.1}$

J. Richter [a,*], O. Hansen [a], A. Nylandsted Larsen [b], J. Lundsgaard Hansen [b], G.F. Eriksen [c], E.V. Thomsen [a]

[a] *MIC - Department of Micro and Nanotechnology, Build. 345 East, Technical University of Denmark, DTU, 2800 Kgs. Lyngby, Denmark*
[b] *Institute of Physics and Astronomy, Ny Munkegade Build. 520, University of Aarhus, 8000 Aarhus C, Denmark*
[c] *Grundfos A/S, Poul Due Jensens Vej 7, 8850 Bjerringbro, Denmark*

Received 13 September 2004; received in revised form 7 February 2005; accepted 20 February 2005
Available online 16 April 2005

Abstract

We present experimentally obtained results of the piezoresistive effect in p-type silicon and strained $Si_{0.9}Ge_{0.1}$. Today, strained $Si_{1-x}Ge_x$ is used for high speed electronic devices. This paper investigates if this area of use can be expanded to also cover piezoresistive micro electro mechanical systems (MEMS) devices. The measurements are performed on microfabricated test chips where resistors are defined in layers grown by molecular beam epitaxy on (0 0 1) silicon substrates. A uniaxial stress along the [1 1 0] direction is applied to the chip, with the use of a four point bending fixture. The investigation covers materials with doping levels of $N_A = 10^{18}$ cm^{-3} and $N_A = 10^{19}$ cm^{-3}, respectively. The results show that the π_{66} piezoresistive coefficient in strained $Si_{0.9}Ge_{0.1}$ is approximately 30% larger than the comparable π_{44} piezoresistive coefficient in silicon at a doping level of $N_A = 10^{18}$ cm^{-3}. Thus, strained $Si_{0.9}Ge_{0.1}$ holds promise for use in high sensitivity MEMS devices.

Keywords: Piezoresistance; Silicon; $Si_{1-x}Ge_x$; MEMS; p-Type

1. Introduction

A large part of conventional micro electro mechanical systems, MEMS, are used to detect and sense. The sensing principles differ between devices, depending on what to detect, and the needed accuracy. Among sensing principles that rely on mechanical properties, are capacitive sensing [1], piezoresistive sensing [2–4], and resonance frequency sensing [5]. The focus of this paper is on MEMS sensing, based on the piezoresistive effect of silicon and strained $Si_{0.9}Ge_{0.1}$. The fact that silicon has a relatively large piezoresistive effect has been known since 1954 [6]. Shortly after, within the following 10 years, this effect was used for applications to measure pressure, force and acceleration [7,8]. Today, silicon based technology has a most dominant status for applications in the MEMS industry.

Thin film layers of strained $Si_{1-x}Ge_x$ are used for high speed micro electronic devices [9] due to an enhancement of the carrier mobility and the ability to tailor the intrinsic carrier concentration and the bandgap [10]. Strained layers for use in high mobility devices is currently a hot topic, where not only strained $Si_{1-x}Ge_x$ layers are being investigated [11], but also strained Si thin films [12,13]. These layers can be grown by molecular beam epitaxy, MBE, or chemical vapor deposition, CVD. Since the processing technology already is established it is natural to apply strained $Si_{1-x}Ge_x$ to other areas, e.g. MEMS, in search of a new and more sensitive material for piezoresistive sensor devices. To the best of our knowledge, there has not yet been any experimental results of the piezoresistance in strained $Si_{1-x}Ge_x$.

In this paper, we present experimentally obtained results of the piezoresistive effect in p-type silicon. These results are compared to the generally used values of the piezoresistive coefficients obtained by Smith [6] and values obtained by others [14,15]. Furthermore, we present theoretically and

* Corresponding author. Tel.: +45 4525 5700; fax: +45 4588 7762.
E-mail address: jar@mic.dtu.dk (J. Richter).

0924-4247/$ – see front matter © 2005 Elsevier B.V. All rights reserved.
doi:10.1016/j.sna.2005.02.038

experimentally obtained results of the piezoresistive effect in strained p-type $Si_{0.9}Ge_{0.1}$.

To obtain these results piezoresistive test chips have been fabricated using microtechnology. A four point bending test set-up has been manufactured. The set-up applies a constant uniaxial stress in the center region of the test chips, and allows an investigation of the piezoresistive effect.

2. Theory

The change in resistance caused by an applied stress is the result of both dimensional changes and a change in resistivity. The relation between the relative resistance change in a piezoresistor, $\Delta R/R_0$, subjected to uniaxial stress, is given by

$$\frac{\Delta R}{R_0} = (1 + 2\nu)\varepsilon_{\mathrm{L}} + \frac{\Delta\rho}{\rho_0}, \tag{1}$$

where ν is the Poisson's ratio and ε_{L} the strain along the piezoresistor with resistance, R. The resistance and the resistivity in the unstressed material is denoted by R_0 and ρ_0, respectively. In silicon and germanium the change in the resistivity, $\Delta\rho/\rho_0$, can be quite large compared to the contribution from the first term on the right side of the equation. Thus, one can ignore this term and write

$$\frac{\Delta R}{R_0} = \frac{\Delta\rho}{\rho_0}. \tag{2}$$

To a first order approximation the relative resistivity change in a resistor is proportional to the applied stress. Since, both the stress and the resistivity in anisotropic materials are described by second order tensors, $\boldsymbol{\sigma}$ and $\boldsymbol{\rho}$, respectively, the proportionality factor consists of a fourth order tensor. With the use of the Einstein summation convention this can be written as

$$\frac{\Delta\rho_{ij}}{\rho_0} = \pi_{ijkl}\sigma_{kl}, \tag{3}$$

where the piezoresistive tensor, $\boldsymbol{\pi}$, consists of elements, π_{ijkl}, which are called piezoresistive coefficients. The coefficients of both $\boldsymbol{\rho}$ and $\boldsymbol{\sigma}$ are described in the principle symmetry coordinate system, i.e. the coordinate system along the $\langle 1\,0\,0\rangle$ directions.

2.1. Symmetry considerations

The lattice symmetry of silicon results in a simplification of $\boldsymbol{\pi}$ in Eq. (3). For materials with the same lattice symmetry as silicon, that is they belong to crystal class O_h [6], π consists of only three independent piezoresistive coefficients, π_{11}, π_{12}, and π_{44} [16].

When a strained layer of $Si_{1-x}Ge_x$ is grown on top of a silicon substrate the lattice constant in the surface plane becomes equal to that of silicon. This compression of the crystal is compensated by an extension of the lattice constant in the direction perpendicular to the surface plane [17]. Since the lattice constant of bulk $Si_{1-x}Ge_x$ is larger than the lattice constant of silicon, the crystal symmetry of strained $Si_{0.9}Ge_{0.1}$ is not the same as that of silicon.

The in-plane strain in the grown strained $Si_{0.9}Ge_{0.1}$ layer is approximately $\varepsilon_{||} = -0.004$ due to the lattice mismatch, thus the film has a compressive biaxial in-plane initial stress on the order of $\sigma_{||} \simeq 700$ MPa. Due to the strain most of the symmetry elements originally present in Si or bulk $Si_{1-x}Ge_x$ are destroyed, and as a result the film belongs to the tetragonal crystal class D_{4h}. In this crystal class, the resistivity is anisotropic and the resistivity tensor has two independent non-zero elements, the in-plane resistivity, $\varrho_{||}$, and the resistivity normal to the plane, $\varrho_{\perp}$ [16]. In terms of microscopic transport theory, this is easily understood, since the strain lifts the degeneracy of the heavy and light hole bands. As a result the light hole contribution to the transport in the plane is increased, and at the same time the light hole contribution to the transport normal to the plane decreased. Thus, the in-plane resistivity is lower than the resistivity normal to the plane $\varrho_{||} < \varrho_{\perp}$.

Due to the remaining symmetry the piezoresistivity tensor of biaxially strained $Si_{1-x}Ge_x$ is expected to have six linearly independent coefficients [16] π_{11}, π_{12}, π_{13}, π_{33}, π_{44}, and π_{66}; the non-zero elements are found at the same positions in the tensor (in matrix notation) as for silicon. For strained $Si_{0.9}Ge_{0.1}$ the piezoresistivity tensor thus has the topology

$$\boldsymbol{\pi} = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{13} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{13} & 0 & 0 & 0 \\ \pi_{13} & \pi_{13} & \pi_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{66} \end{bmatrix}. \tag{4}$$

Work trying to relate these coefficients to the bandstructure is currently in progress. On top of the complications caused by the reduced symmetry, also alloy effects due to the random distribution of silicon and germanium atoms on the lattice sites come into play. In order to simplify comparisons between Si and strained $Si_{1-x}Ge_x$, we introduce an effective piezoresistive coefficient, π_{eff}, which is a linear combination of some of the coefficients in the piezoresistivity tensor.

By applying a uniaxial stress, σ_{xx}, to the material, one can obtain π_{eff}, with the use of following relation

$$\frac{\Delta R}{R_0} = \pi_{\mathrm{eff}}\sigma_{xx}. \tag{5}$$

Thus, we can compare the effective piezoresistive coefficients of different materials without knowing the actual values of each piezoresistive coefficient in $\boldsymbol{\pi}$.

2.2. Four point bending

Four point bending is often used in material analysis and have also been used for piezoresistive measurements in refs. [14,15,18].

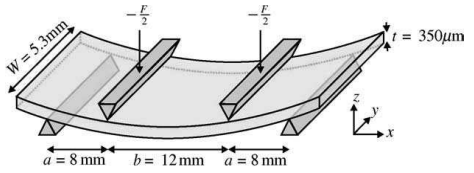


Fig. 1. Sketch of a four point bending fixture. In the surface of the rectangular material, in the region between the two upper blades, the stress is constant and uniaxial.

Consider first the test chip in the four point bending set-up, shown in Fig. 1, as a beam of width W and thickness t. At the outer knives the beam is simply supported. The two inner knives act on the beam with the forces $-\hat{\mathbf{z}}F/2$, and due to symmetry and static stability, the outer knives act on the beam with equally large opposite forces $\hat{\mathbf{z}}F/2$. The part of the beam outside the outer knives is free from external forces and moments, thus the shear in the beam is zero outside the outer knives, constant (magnitude $F/2$) in-between each pair of outer and inner knives, and zero between the inner knives. As a result, the magnitude of the moment increases linearly from zero at the outer knives to $Fa/2$ at the inner knives, where a is the distance between neighboring inner and outer knives. Between the inner knives the moment is constant with the magnitude $Fa/2$. This moment makes the beam bend to a circular arc, causing a strain that varies linearly with z, and thus creates uniaxial internal stresses that varies linearly with z. These stresses balance the moment. Between the inner blades we have the surfaces normal to the z-axis and the y-axis free from loads, thus all stresses except σ_{xx} vanish. The moment balance yields

$$W\int_{-t/2}^{t/2}\sigma_{xx}z\,\mathrm{d}z = -W\sigma_{xx_{\max}}\int_{-t/2}^{t/2}\frac{2z}{t}z\,\mathrm{d}z = -\sigma_{xx_{\max}}\frac{Wt^2}{6} = -\frac{1}{2}Fa, \tag{6}$$

where $\sigma_{xx_{\max}}$ is the magnitude of the maximum value of the stress, and the origin of the z-axis is assumed to be in the middle of the beam. Solving for the stress, we find the stress between the inner knives

$$\sigma_{xx} = -\frac{2z}{t}\sigma_{xx_{\max}} = -\frac{2z}{t}\frac{3Fa}{Wt^2}. \tag{7}$$

The piezoresistors are placed in the top surface of the beam, at $z = t/2$, thus the stress acting on the piezoresistors in the four point beam bending set up is

$$\sigma_{xx} = -\sigma_{xx_{\max}} = -\frac{3Fa}{Wt^2}. \tag{8}$$

This derivation is simplified significantly, since a correct treatment should be based on plate theory including possible effects of the anisotropic elastic properties of silicon and strained $Si_{1-x}Ge_x$. However, the expression for the stress at the piezoresistors is still correct to a very good approximation for the following reasons. The exact solution for a rectangular plate in pure bending caused by external moments evenly distributed on facing edges of the plate is a uniaxial stress $\sigma_{xx} = -2z\sigma_{xx_{\max}}/t$ [19], if the stresses causing the external moments are distributed exactly as σ_{xx}. The stresses causing the load moments at the inner knives certainly do not fulfil this requirement, but according to the principle of Saint-Venant [19] the exact solution still apply far from the inner knives. The deviations from the exact solution found near the inner knives will decay rapidly on a length scale set by the thickness of the piezoresistor test-chip ($t = 350\,\mu\mathrm{m}$).

In the exact pure bending solution, the surface will become an anticlastic surface [19] with the curvature $1/r$ in the x–z plane and the curvature $-\nu/r$ in the y–z plane. In the present experiments the beams are oriented along the [1 1 0] direction, where Poisson's ratio ν has its minimum value in silicon and germanium ($\nu < 0.07$). Thus, the effect of curvature in the y–z plane is small, but still this will cause the load moment to be unevenly, but symmetrically distributed at the inner knives, again causing deviations from the exact pure bending solution. According to the principle of Saint-Venant the deviations will decay rapidly on a length scale equal to half the width of the chip, $W/2$. Taking into account the anisotropic elastic properties of silicon these conclusions are still valid. The exact solution remains essentially the same, as seen if the derivation given in Timoshenko and Goodier [19] is redone with the elastic parameters of silicon for a beam oriented along the [1 1 0] direction, where the pertinent rotated tensor elements of the compliance tensor are $S'_{11} = 1/2(S_{11} + S_{12} + S_{44}/2)$, $S'_{12} = 1/2(S_{11} + S_{12} - S_{44}/2)$, and $S'_{13} = S_{12}$. The primed symbols are the rotated tensor elements and the unprimed symbols are the tensor elements in the crystal coordinate system. The Poisson's ratio mentioned in the curvature discussion above is related to these tensor elements in the following manner, $\nu = S'_{12}/S'_{11}$. In summary, we can safely assume a unidirectional stress given by Eq. (8) at the piezoresistors because the chip is thin, and because the resistors are placed more than half the width of the chip from the inner knives.

2.3. Piezoresistivity

For practical applications of Eq. (3) the tensors can be transformed into new coordinate systems oriented in any arbitrary direction compared to the ⟨1 0 0⟩ coordinate system. The substrates used in the present work have a (0 0 1) surface orientation and the piezoresistors are implemented in the surface plane. Thus, applying a uniaxial stress we can write

$$\frac{\Delta R'}{R_0} = \pi'_{\mathrm{eff}}\sigma'_{xx}, \tag{9}$$

where $\Delta R'/R_0$ is the relative resistance change in a resistor, R' and σ'_{xx} is the applied uniaxial stress, both directed along any arbitrary direction with respect to the [1 0 0] direction. Now, sine and cosine functions are incorporated in the term of the effective piezoresistive coefficient, π'_{eff}.

The $\boldsymbol{\pi}$ tensor is known for silicon, thus one can do the transformations described above and find the relation

$$\frac{\Delta R'}{R_0} = \frac{\sigma'_{xx}}{2}[\pi_{11} + \cos(2\phi)\cos(2\theta)(\pi_{11} - \pi_{12}) + \pi_{12} + \sin(2\theta)\sin(2\phi)\pi_{44}], \quad (10)$$

where θ and ϕ are the angles of the direction of the resistor and the stress, respectively, with respect to the [1 0 0] direction. The samples in this paper are all stressed along the [1 1 0] direction, i.e. $\phi = -45^\circ$, thus

$$\frac{\Delta R'}{R_0} = \sigma'_{xx}\pi'_{\text{eff}}, \quad (11)$$

with the effective piezoresistive coefficient

$$\pi'_{\text{eff}} = \frac{\pi_{11} + \pi_{12} - \pi_{44}\sin(2\theta)}{2}. \quad (12)$$

This equation defines the theoretical value of the effective piezoresistive coefficient of a silicon resistor rotated an angle θ with respect to the [1 0 0] direction, and subjected to a uniaxial stress along the [1 1 0] direction on a (0 0 1) substrate. By inserting the values of the piezoresistive coefficients obtained by Smith [6] we can compare our results with the values generally accepted.

In the case of strained $Si_{1-x}Ge_x$ Eq. (12) is also valid if π_{44} is replaced by π_{66}.

In silicon the maximum value of Eq. (12) is reached when the resistor is directed along the [1 1 0] direction, i.e. $\theta = -45^\circ$. In this case, when the current flows parallel to the stress direction the effective piezoresistive coefficient becomes the well-known longitudinal piezoresistive coefficient, π_l. In the same manner, the transversal piezoresistive coefficient, π_t, appears when the current flows perpendicular to the stress direction.

3. Experimental

In the following sections the experimental work is presented. This includes a description of the fabrication process for the piezoresistive test chips, a presentation of the chip layout, and an explanation of the experimental setup.

3.1. Fabrication

The samples investigated in this study were grown in a VG80-S MBE system equipped with Airco-Temescal magnetically scanned e-beam evaporators for evaporation of high purity silicon and germanium [20]. The base pressure in the system is 5×10^{-11} Torr and during growth the pressure remains below 3×10^{-10} Torr. Doping of the layers were performed by evaporation of 5N5 elemental boron using an Oxford Applied Research mini e-beam evaporator.

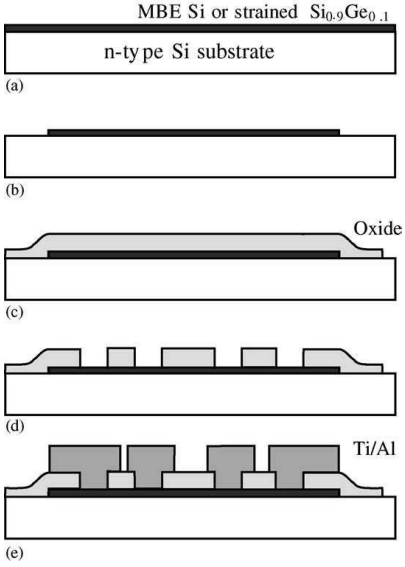


Fig. 2. A 200 nm p-type silicon or strained $Si_{0.9}Ge_{0.1}$ layer is grown using MBE on top of a n-type silicon substrate (a). The resistors in the epitaxial layer are defined with RIE (b). A 500 nm PECVD oxide is deposited on top (c), and contact windows are opened using BHF etching (d). Finally, a lift off of 100 nm Ti and 700 nm Al defines the metal paths (e).

Silicon and strained $Si_{0.9}Ge_{0.1}$ layers with a thickness of 200 nm were grown on n-type, 10 Ω cm, (0 0 1) double sided polished silicon substrates with a thickness of $t = 350\,\mu$m. The growth temperature was 500 °C with growth rates of around 0.1 nm/s. Layers with a doping concentration of around $N_A = 10^{18}$ cm^{-3} and $N_A = 10^{19}$ cm^{-3} were grown. Before growth the native oxide was removed by heating the wafer to 860 °C in a silicon flux of 0.04 nm/s.

Prior to growth, the silicon substrates were patterned with alignment marks, made using anisotropic KOH etching, determining the [1 1 0] direction with a precision of ±0.2°. Fig. 2 illustrates the fabrication process after the epitaxial layer has been grown. The piezoresistors were defined using reactive ion etching, RIE, through the grown layers. To maintain the strained structures low temperature processing was necessary, and therefore a plasma enhanced chemical vapor deposition, PECVD, 500 nm oxide was used for isolation. Metal conductors were defined in an evaporated 100 nm Ti/700 nm Al layer using a lift off process, and annealed at a temperature of 475 °C for 15 min. Finally, deep reactive ion etching, DRIE, using the Bosch process [21], isolate the chips. This step was performed in order to obtain an accurate definition of the chip edge to the crystal orientation and to ensure an accurate definition of the chip width. The RIE, PECVD, and DRIE processes were performed with a STS multiplex cluster tool.

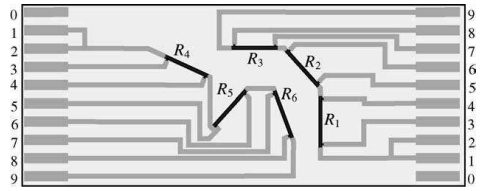


Fig. 3. Sketch of the chip layout (not to scale). The resistors R_1, R_2, and R_3 are series connected, and the corresponding metal paths are directed to one end of the chip. R_4, R_5, and R_6 are connected in the same manner, with metal paths directed to the opposite end of the chip. The resistors are placed in the center region of the chip, and metal paths (dark grey) assure electrical contact from the contacts to the resistors.

3.2. Chip layout

The chip layout is illustrated in Fig. 3. Six resistors, designed for four point measurements, are placed in the middle of the chip. These resistors are rotated different angles with respect to the [1 1 0] stress direction. The angle between the stress and the resistor direction for resistor R_1 to R_6 is 90, 45, 0, 22.5, −45, and 67.5°, respectively. The resistor pair R_2 (45°) and R_5 (−45°), which in theory should yield identical measurement results in the experiments presented here, are included to serve as a tool to detect misalignment in the measurement setup or the chip fabrication.

The resistors R_1, R_2, and R_3 are series connected and the corresponding metal paths are directed to one end of the chip. Likewise, the metal paths leading to R_4, R_5, and R_6 are directed to the opposite end of the chip. The contacts are denoted from 0 to 9, where contact 0 is connected to the substrate.

By copying the layout of a flat flexible cable, FFC, to the two ends of the chip we can insert each end into a FFC zero insertion force connector and obtain electrical connection. This results in an easy "plug and measure" method. Furthermore, this connection principle will not affect the stress distribution in the chip significantly.

The length to width ratio of the resistors is 20 resulting in a resistance in each resistor of approximately 40 kΩ for $N_A = 10^{18}$ cm^{-3} and 10 kΩ for $N_A = 10^{19}$ cm^{-3}. Fig. 4 shows a close up photograph of the center region of a fabricated chip.

3.3. Set-up

The resistance of each resistor is measured using conventional four point measurements at different stresses. With the use of this measurement principle we eliminate the contribution from the contact resistance. This is the main argument for using this type of measurement instead of for example a Wheatstone bridge configuration. However, in the four point measurement it is essential to control accurately the measurement temperature to minimize errors due to the large temperature coefficient of the resistivity. The stress in the material can be found by applying a known force, F, to the upper blades of the four point bending fixture. F is changed by placing different loads on top of the upper blades. The realized four point bending fixture is shown in Fig. 5.

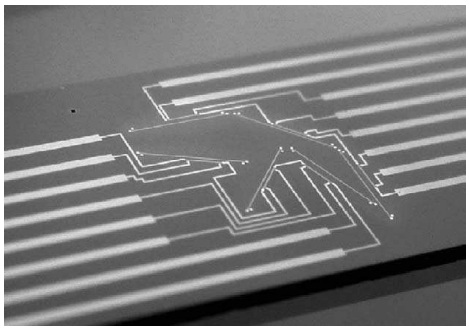


Fig. 4. Close up of the resistor configuration on a fabricated chip. The resistors are distributed as illustrated in Fig. 3.

With the use of a Keithley 2400 sourcemeter a constant current is forced through the series connected resistors. A Keithley 2700 Multimeter with a 7700 Multiplexer card measures the voltage drop along each resistor. The electrical connection to the chip is done with the use of the FFC connector.

During the measurements, contact 1 or 2 and contact 9, illustrated in Fig. 3, are connected to the current source, and a current is thereby forced through the three series connected resistors. That is resistors R_1, R_2, and R_3 on one side of the chip, and R_4, R_5, and R_6 on the other side of the chip.

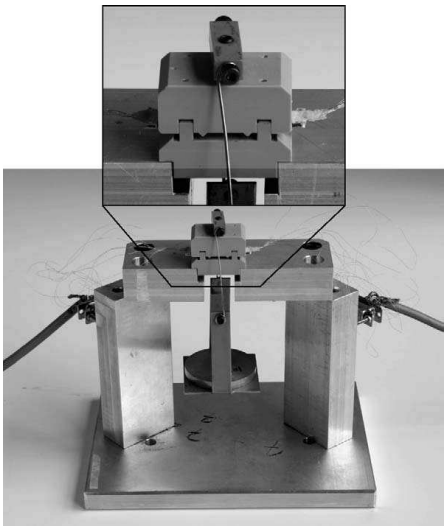


Fig. 5. Realized four point bending fixture. The upper and lower blades can both be seen in the enlarged photograph. The stress is applied to the chip, by placing loads on the scale.

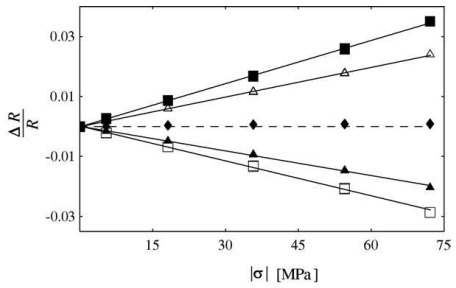


Fig. 6. Piezoresistive measurements performed on strained $Si_{0.9}Ge_{0.1}$ with a doping level of $N_A = 10^{19}$ cm^{-3}. The data series of R_1 (□), R_3 (■), R_4 (△), and R_6 (▲), and the corresponding linear fits are shown. These are oriented with an angle of 90, 0, 22.5, and 67.5°, respectively, with respect to the [1 1 0] stress direction. The data series of R_2 (♦) and R_5 (◇) are almost identical, and therefore it is difficult to see the data series of R_5. Since R_2 and R_5 are oriented at an angle of 45 and −45°, respectively, with respect to the stress direction, they are expected to be equal.

The effective piezoresistive coefficient, π'_{eff} in Eq. (11) is then found from the measured data of the relative resistance change and the applied stress. Fig. 6 shows an example of measurements on strained $Si_{0.9}Ge_{0.1}$ resistors with a doping level of $N_A = 10^{19}$ cm^{-3} and the corresponding linear regression fits. The effective piezoresistive coefficient in each resistor direction is then equal to the slope found from the linear regression.

In the case of both silicon and strained $Si_{0.9}Ge_{0.1}$ preliminary linearity tests were performed in order to determine the validity of the proposed linear model. For both materials it was found that the measured data followed the linear model at stress values below $\sigma_{\max} = -75$ MPa. Since the numerical value of the stress is significantly lower than the numerical value of the grown-in stress $\sigma_{||} \simeq -700$ MPa linearity in this range was expected.

4. Results

The obtained results of the effective piezoresistive coefficients in both silicon and strained $Si_{0.9}Ge_{0.1}$ are listed in Table 1. This table consists of results from measurements on samples with doping concentrations of $N_A = 10^{18}$ cm^{-3} and $N_A = 10^{19}$ cm^{-3}, respectively. The effective piezoresistive coefficients calculated with the use of the values in ref. [6] for silicon, are also listed.

4.1. Silicon

For silicon there is a reduction in the extracted piezoresistive coefficients for $N_A = 10^{19}$ cm^{-3} compared to a doping level of $N_A = 10^{18}$ cm^{-3}. This behavior is also expected in the generally used model by Kanda [22]. According to this model the value of the piezoresistive coefficients should decrease by a factor of approximately 0.8 when the doping level is increased to $N_A = 10^{19}$ cm^{-3}. This is in good agreement with the obtained results. The model by Kanda describes the doping level effects and the thermal effects on the piezoresistive coefficients. Primarily carrier transfer effects between the bands as function of the fermi level are considered, assuming that the relaxation time of the carriers is only a function of energy. The resistivity, ϱ, of p-type material is approximately given by $\varrho = 1/(e^2\tau_{hh}p_{hh}/m_{hh} + e^2\tau_{lh}p_{lh}/m_{lh})$, where e is the unit charge, p_i the hole concentration, m_i the effective mass, and τ_i the relaxation time in band i, where i can denote either the heavy or light hole band. The effective masses in the complex hole bands are known to be affected by the stress [23], thus the Kanda model might not be too accurate for p-type material, but excellent for n-type material.

The effective piezoresistive coefficients of R_1 and R_3 can be used to obtain the value of the π_{44} coefficient. With the use of Eq. (12) one finds the relation

$$\frac{\Delta R_3}{R_0} - \frac{\Delta R_1}{R_0} = \sigma'_{xx}\pi_{44}. \tag{13}$$

Thus, the π_{44} coefficient can now be found as

$$\pi_{44} = \frac{\Delta R_3}{R_0}\frac{1}{\sigma'_{xx}} - \frac{\Delta R_1}{R_0}\frac{1}{\sigma'_{xx}} = \pi_{\text{l}} - \pi_{\text{t}}. \tag{14}$$

In strained $Si_{1-x}Ge_x$ the similar calculation also yields a single piezoresistive coefficient $\pi_{66} = \pi_{\text{l}} - \pi_{\text{t}}$.

By inserting the results from Table 1, the π_{44} piezoresistive coefficient in silicon and π_{66} in strained $Si_{0.9}Ge_{0.1}$ can be found. The extracted values are listed in Table 2. It is found that the π_{44} coefficient in silicon is equal to 103×10^{-11} Pa^{-1} and 81×10^{-11} Pa^{-1} at a doping level of $N_A = 10^{18}$ cm^{-3} and $N_A = 10^{19}$ cm^{-3}, respectively. The set-up contributes to an

Table 1
Comparison of effective piezoresistive coefficients of both silicon and strained $Si_{0.9}Ge_{0.1}$, with doping levels of $N_A = 10^{18}$ cm^{-3} and $N_A = 10^{19}$ cm^{-3}

Material	π_{t} (10^{-11}Pa^{-1})	π_{l} (10^{-11}Pa^{-1})	$\pi_{22.5°}$ (10^{-11}Pa^{-1})	$\pi_{67.5°}$ (10^{-11}Pa^{-1})
$Si_{0.9}Ge_{0.1}$ $N_A = 10^{18}$ cm^{-3}	−60	76	53	−42
$Si_{0.9}Ge_{0.1}$ $N_A = 10^{19}$ cm^{-3}	−39	48	33	−27
Si $N_A = 10^{18}$ cm^{-3}	−48	56	37	−37
Si $N_A = 10^{19}$ cm^{-3}	−40	42	29	−29
Si low doped bulk [6]	−66.3	71.8	51.6	−45.7

The samples are stressed along the [1 1 0] direction. The piezoresistive coefficients $\pi_{22.5°}$ and $\pi_{67.5°}$ are the effective piezoresistive coefficients in resistors directed in angles of 22.5 and 67.5° with respect to the stress direction, respectively. The generally accepted values obtained by Smith [6] have been used to calculate the values shown for comparison in the bottom of the table.

Table 2
Comparison of the obtained results of the π_{44} coefficient in silicon and π_{66} in strained $Si_{0.9}Ge_{0.1}$, with doping levels of $N_A = 10^{18}\,cm^{-3}$ and $N_A = 10^{19}\,cm^{-3}$

	Si π_{44} ($10^{-11}Pa^{-1}$)	$Si_{0.9}Ge_{0.1}$ π_{66} ($10^{-11}Pa^{-1}$)	$\Delta\pi/\pi$ (%)
$N_A = 10^{18}\,cm^{-3}$	103	136	4
$N_A = 10^{19}\,cm^{-3}$	81	87	4
[6]	138.1		
[14]	93		7.5
[15]	105		8–10

For comparison, the experimental values obtained by Smith [6] in lightly doped bulk silicon, and Beaty and Jaeger [14] and Lund [15] in thin film silicon are also listed.

uncertainty of 4% on the magnitude of the applied stress. This uncertainty is mainly caused by sample thickness errors. The uncertainty on the stress exceeds the uncertainty on the electrical measurements by an order of magnitude, thus π_{44} for Si and π_{66} for strained $Si_{0.9}Ge_{0.1}$ is determined with a 4% uncertainty. For comparison, Table 2 contains values of the π_{44} coefficient obtained experimentally by Smith [6], Beaty and Jaeger [14], and Lund [15]. It is seen, that the measured value of π_{44} in silicon with $N_A = 10^{18}\,cm^{-3}$ is approximately 28% lower than that of Smith, which was measured on lightly doped bulk silicon. Approximately, the same result was found in refs. [14,15]. Thus, experimental results indicate that the piezoresistive coefficient π_{44} in silicon is lower in a thin film layer, than it is in a lightly doped bulk material, or that the values in ref. [6] might overestimate the piezoresistivity.

4.2. Strained $Si_{0.9}Ge_{0.1}$

In Table 1 it is seen, that the effective piezoresistive coefficients in strained $Si_{0.9}Ge_{0.1}$ are larger than those in silicon. This relative difference is approximately 30% for a doping concentration of $N_A = 10^{18}\,cm^{-3}$. The longitudinal piezoresistive coefficient in strained $Si_{0.9}Ge_{0.1}$ is 27% larger than the longitudinal piezoresistive coefficient in silicon for a doping level of $N_A = 10^{18}\,cm^{-3}$. With doping concentrations of $N_A = 10^{19}\,cm^{-3}$ this large difference decrease significantly. The π_{66} coefficient in strained $Si_{0.9}Ge_{0.1}$ is found to be $\pi_{66} = 136 \times 10^{-11}\,Pa^{-1}$ and $\pi_{66} = 87 \times 10^{-11}\,Pa^{-1}$ for doping concentrations of $N_A = 10^{18}\,cm^{-3}$ and $N_A = 10^{19}\,cm^{-3}$, respectively.

To compare the obtained results of silicon and strained $Si_{0.9}Ge_{0.1}$ a polar plot is useful. A polar plot shows the effective piezoresistive coefficients for each resistor oriented in a certain angle with respect to the stress direction. Therefore, the longitudinal and the transversal piezoresistive coefficient will be presented on the x-axis and the y-axis, respectively.

The polar plot in Fig. 7a compares the measurements performed on silicon and strained $Si_{0.9}Ge_{0.1}$, both with a doping level of $N_A = 10^{18}\,cm^{-3}$. It is clear to see that the strained $Si_{0.9}Ge_{0.1}$ layer has a much larger piezoresistive effect than the silicon layer.

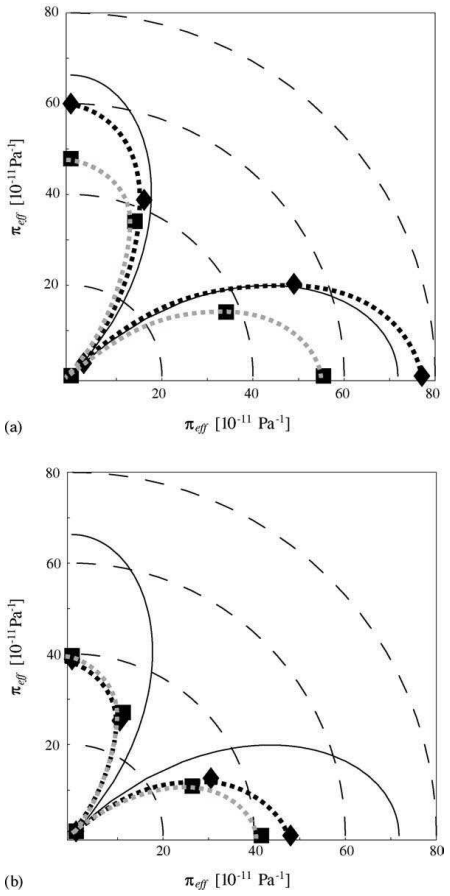


Fig. 7. Polar plots illustrating the piezoresistive results obtained, when the samples are stressed along the [1 1 0] direction in both silicon (■) and strained $Si_{0.9}Ge_{0.1}$ (♦), at doping levels of $N_A = 10^{18}\,cm^{-3}$ (a), and $N_A = 10^{19}\,cm^{-3}$ (b). The theoretical behavior in silicon is illustrated by the thin solid line, where the values of the piezoresistive coefficients obtained by Smith in ref. [6] are used. The data points are from measurements on all six resistors. For both silicon and strained $Si_{0.9}Ge_{0.1}$ the effective piezoresistive coefficients of R_2 and R_5 are almost identical as expected. The thick grey and black dotted lines are only drawn to indicate that both silicon and strained $Si_{0.9}Ge_{0.1}$ seem to show a behavior similar to that described in theory for silicon. More measurements on resistors directed along other directions need to be performed in order to fully verify this behavior in strained $Si_{0.9}Ge_{0.1}$.

Fig. 7b shows a polar plot of the obtained effective piezoresistive coefficients with a doping level of $N_A = 10^{19}\,cm^{-3}$. There is a decrease in the values of the effective piezoresistive coefficients of approximately 20 and 37% for silicon and strained $Si_{0.9}Ge_{0.1}$, respectively, compared to the values obtained for a doping level of $N_A = 10^{18}\,cm^{-3}$. In both Fig. 7a and b the model theory of the effective piezoresistive

coefficient in silicon, found from Eq. (12), is sketched. The values of the piezoresistive coefficients obtained by Smith [6] have been used to produce this graph.

In silicon, π_{11} and π_{12} are both relatively small compared to π_{44}, according to Smith $\pi_{44}/(\pi_{11}+\pi_{12}) \approx 25$. Since strained $Si_{0.9}Ge_{0.1}$ shows same behavior as silicon, see Fig. 7, the relative magnitude of the coefficients π_{11}, π_{12}, and π_{66} must be comparable to the relative magnitude of π_{11}, π_{12}, and π_{44} in silicon. However, more measurements need to be performed on resistors directed along other directions in order to fully verify this behavior.

5. Conclusion

Experimentally obtained results of the piezoresistivity in p-type silicon and strained $Si_{1-x}Ge_x$ have been presented.

From the results obtained with the silicon piezoresistive test chips stressed along the [1 1 0] direction we can conclude the following: The transversal and longitudinal piezoresistive coefficients in silicon with a doping concentration of $N_A = 10^{18}\,cm^{-3}$ are approximately 30% lower than the currently accepted values obtained by Smith [6]. Experiments in ref. [14,15] obtain the approximate same results as the results of this paper. Thus, the piezoresistivity in thin film silicon seems to be 30% lower than that in ligthly doped bulk silicon, or the values obtained in ref. [6] might overestimate the piezoresistive effect. The relative reduction in the transversal and longitudinal piezoresistive coefficients in silicon, caused by an increase in doping concentration from $N_A = 10^{18}\,cm^{-3}$ to $N_A = 10^{19}\,cm^{-3}$ is 17 and 25%, respectively. This decrease in the values of the piezoresistive coefficients is in reasonable agreement with the model by Kanda [22] that predicts a decrease of 20%.

To the authors's knowledge, this is the first time the piezoresistive effect in strained $Si_{0.9}Ge_{0.1}$ has been experimentally investigated. The results presented in this paper prove that strained $Si_{0.9}Ge_{0.1}$ has a larger piezoresistive effect than that seen in silicon. By comparison of the measured piezoresistive effect in silicon and strained $Si_{0.9}Ge_{0.1}$, stressed along the [1 1 0] direction, the following three main results have been obtained: At a doping concentration of $N_A = 10^{18}\,cm^{-3}$ the π_{66} piezoresistive coefficient is approximately 30% larger in strained $Si_{0.9}Ge_{0.1}$ than the π_{44} coefficient in silicon. At a doping concentration of $N_A = 10^{19}\,cm^{-3}$ this large difference decrease significantly. Finally, it is found that the relative magnitude of π_{11}, π_{12}, and π_{66} in strained $Si_{0.9}Ge_{0.1}$ must be similar to the relative magnitude of π_{11}, π_{12}, and π_{44} in silicon.

The results obtained from the strained $Si_{0.9}Ge_{0.1}$ piezoresistive test chips show a promising future for the use of this material in MEMS devices. The results prove that strained $Si_{0.9}Ge_{0.1}$ can be used to obtain a higher sensitivity for piezoresistive devices, than MEMS devices based on silicon, even though the improvements in the signal to noise ratio will be only marginal.

Acknowledgement

We acknowledge Ph.D. Kristian Mølhave for his idea of using FFC connectors as connection between the chip and the electrical equipment.

References

[1] Z. Xiao, Silicon micro-accelerometer with mg resolution, high linearity and large frequency bandwidth fabricated with two mask bulk process, Sens. Actuators: Phys. A 77 (1999) 113–119.
[2] J. Thaysen, Cantilever-based bio-chemical sensor integrated in a microliquid handling system, Proc. MEMS (2001) 401–404.
[3] H. Jung, Design of smart piezoresistive pressure sensor, Sci. Technol. 1 (2001) 202–205.
[4] G. Friis Eriksen, R. de Reus, C. Christensen, Packaging-friendly flat-surface pressure sensor for harsh environments, Technical Digest Transducer (1999) 1470–1473.
[5] G. Abagal, Electromechanical model of a resonating nano-cantilever-based sensor for high-resolution and high-sensitivity mass detection, Nanotechnology 12 (2001) 100–104.
[6] C.S. Smith, Piezoresistance effect in germanium and silicon, Phys. Rev. 94 (1954) 42–49.
[7] W.P. Mason, J.J. Forst, L.M. Tornillo, Recent developments in semiconductor strain tranducers, Semicond. Conventional Strain Gauges (1962) 110–120.
[8] O.N. Tufte, P.W. Chapman, Silicon diffused-element piezoresistive diaphragms, J. Appl. Phys. 33 (3) (1962) 3322–3327.
[9] J.D. Cressler, Re-engineering silicon: Si–Ge heterojunction bipolar technology, IEEE Spectr. 33 (1995) 49–57.
[10] R. People, Indirect band gap and band aligment for coherently strained Si_xGe_{1-x}; bulk alloys on germanium (0 0 1) substrates, Phys. Rev. B 34 (1986) 2508–2510.
[11] R.J.P. Lander, Y.V. Ponomarev, J.G.M.v. Berkum, W.B. de Boer, High hole mobilities in fully-strained $Si_{1-x}Ge_x$ layers ($0.3 < x < 0.4$) and their significance for SiGe pMOSFET performance, IEEE Trans. Electron Devices 48 (2001) 1826–1832.
[12] K. Rim, J. Welser, J.L. Hoyt, J.F. Gibbons, Enhanced hole mobilities in surface-channel strained-Si p-MOSFETs, IEDM Tech. Dig. (1995) 1026.
[13] D.K. Nayak, K. Goto, A. Yutani, J. Murota, Y. Shiraki, High mobility strained-Si PMOSFETs, IEEE Trans. Electron Devices 43 (1996) 1709–1716.
[14] R.E. Beaty, R.C. Jaeger, Evaluation of piezoresistive coefficient variation in silicon stress sensors using a four-point bending test fixture, IEEE Trans. Components Hybrids Manuf. Technol. 15 (1992) 904–914.
[15] E. Lund, Measurement of the temperature dependency of the piezoresistance coefficients in p-type silicon, Adv. Electron. Packag. 1 (1999) 215–218.
[16] J.F. Nye, Physical Properties of Crystals, first ed., Oxford University Press, 1957.
[17] J.C. Bean, L.C. Feldman, A.T. Fiory, S. Nakahara, I.K. Robinson, $Si_{1-x}Ge_x$/Si strained-layer superlattice grown by molecular beam epitaxy, J. Vac. Sci. Technol. A 2 (1984) 436–440.
[18] E. Lund, T.G. Finstad, Design and construction of a four-point bending based set-up for measurement of piezoresistance in semiconductors, Rev. Sci. Instr. 75 (2004) 4960–4966.
[19] S.P. Timoshenko, J.N. Goodier, Theory of Elasticity, third ed., McGraw-Hill, 1970.
[20] J. Lundsgaard Hansen, S.Yu. Shiryaev, E.V. Thomsen, Improvement of the morphological quality of the Si surface using an optimised in-situ oxide removal procedure prior to MBE growth, J. Cryst. Growth 157 (1995) 317–322.

[21] F. Laermer and A. Schilp, Patent DE4241045 (U.S. Pat. No. 5,501,893), 1994.
[22] Y. Kanda, A graphical representation of the piezoresistance coefficients in silicon, IEEE Trans. Electron Devices ED-29 (1982) 64–70.
[23] P. Kleimann, B. Semmache, M. Le Berre, D. Barbier, Stress-dependent hole effective masses and piezoresistive properties of p-type monocrystalline and polycrystalline silicon, Phys. Rev. B 57 (1998) 8966–8971.

Biographies

Jacob Richter holds a M.Sc. degree in mechanical and electrical engineering at the Technical University of Denmark, DTU. He has been affiliated with the Department of Micro and Nanotechnology, MIC since 2000 and has worked with many fields of microtechnology, among others piezoresistive pressure sensors, MPW test chips, and electronic interface circuits. His current work is focused on the piezoresistive effect in different semiconductor crystals.

Ole Hansen received the M.Sc. degree from the Semiconductor Laboratory, DTU, in 1977. Since then he has done research in silicon based micro- and nano-technology and its applications, first at the Semiconductor Laboratory, and later at the Department of Micro and Nanotechnology, MIC. Current research interests include Deep Reactive Ion Etching of silicon, $Si_{1-x}Ge_x$/Si heterostructures, microreactors for catalysis, and cantilever based microprobes for nano-science. He is presently teaching three lecture courses: Semiconductor Technology, Semiconductor Devices and Microelectromechanical Systems. Since 1990 he has been an Associate Professor at MIC.

Arne Nylandsted Larsen is associate professor at Institute of Physics and Astronomy, University of Aarhus. He is holding a M.Sc., a Ph.D. and a Dr.Scient. in physics from University of Aarhus. Arne Nylandsted Larsen has been affiliated with University of Aarhus since 1981, and has been working with studies of defects and atomic diffusion in semiconductors. His current interests also include MBE growth of group-IV semiconductors, and synthesis and characterization of group-IV nanocrystals.

John Lundsgaard Hansen is running the SiGe MBE facility at the University of Aarhus, Denmark. He was educated as Electronic Engineer at the Danish Airforce and later on received a M.Sc. in physics from The University of Aarhus. He has been running the MBE facility since 1992 and his current interest is components based on nanodots in Si and SiO_2.

Gert F. Eriksen is head of the R & D department at Grundfos Semiconductor in Denmark. He holds a M.Sc. and a Ph.D. in electrical engineering from Technical University of Denmark, DTU. He has been working with MEMS devices and packaging since 1992.

Erik V. Thomsen is group leader for the prototyping activities at the MEMS section at MIC - Department of Micro and Nanotechnology, Technical University of Denmark, DTU, where he is affiliated as associate professor. He holds a M.Sc. in physics from Odense University and a Ph.D. in electrical engineering from DTU. Erik V. Thomsen has been affiliated with MIC since 1992 and has been working with fabrication of semiconductor devices. His current interests include micromechanical multi-sensors, piezo resistivity of strained layers and microsystem packaging. He teaches in solid state electronics and nano and microfabrication.

APPENDIX

C Piezoresistive tensor simplification

The piezotensor $\boldsymbol{\pi}$ describes the linear relation between the resistivity $\boldsymbol{\rho}$ of a material and a given stress $\boldsymbol{\sigma}$

$$\frac{\Delta\rho_{ij}}{\bar{\rho}} = \pi_{ijkl}\sigma_{kl}, \tag{C.1}$$

where $\bar{\rho}$ is the mean resistivity at zero stress. According to the theorem by Onsager [53] the resistivity tensor is symmetric, i.e. $\Delta\rho_{ij} = \Delta\rho_{ji}$. This is directly transferred to the piezotensor $\pi_{ijkl} = \pi_{jikl}$, for example $\pi_{1231} = \pi_{2131}$. The piezotensor is a tensor of fourth rank and contains 81 coefficients. However, with the symmetry considerations above the number of independent coefficients reduces to 45 and the piezotensor is then visualized in the following manner

$$\boldsymbol{\pi} = \begin{bmatrix} \begin{pmatrix} \pi_{1111} & \pi_{1112} & \pi_{1113} \\ \pi_{1121} & \pi_{1122} & \pi_{1123} \\ \pi_{1131} & \pi_{1132} & \pi_{1133} \end{pmatrix} & \begin{pmatrix} \pi_{1211} & \pi_{1212} & \pi_{1213} \\ \pi_{1221} & \pi_{1222} & \pi_{1223} \\ \pi_{1231} & \pi_{1232} & \pi_{1233} \end{pmatrix} & \begin{pmatrix} \pi_{1311} & \pi_{1312} & \pi_{1313} \\ \pi_{1321} & \pi_{1322} & \pi_{1323} \\ \pi_{1331} & \pi_{1332} & \pi_{1333} \end{pmatrix} \\ \begin{pmatrix} \pi_{1211} & \pi_{1212} & \pi_{1213} \\ \pi_{1221} & \pi_{1222} & \pi_{1223} \\ \pi_{1231} & \pi_{1232} & \pi_{1233} \end{pmatrix} & \begin{pmatrix} \pi_{2211} & \pi_{2212} & \pi_{2213} \\ \pi_{2221} & \pi_{2222} & \pi_{2223} \\ \pi_{2231} & \pi_{2232} & \pi_{2233} \end{pmatrix} & \begin{pmatrix} \pi_{2311} & \pi_{2312} & \pi_{2313} \\ \pi_{2321} & \pi_{2322} & \pi_{2323} \\ \pi_{2331} & \pi_{2332} & \pi_{2333} \end{pmatrix} \\ \begin{pmatrix} \pi_{1311} & \pi_{1312} & \pi_{1313} \\ \pi_{1321} & \pi_{1322} & \pi_{1323} \\ \pi_{1331} & \pi_{1332} & \pi_{1333} \end{pmatrix} & \begin{pmatrix} \pi_{2311} & \pi_{2312} & \pi_{2313} \\ \pi_{2321} & \pi_{2322} & \pi_{2323} \\ \pi_{2331} & \pi_{2332} & \pi_{2333} \end{pmatrix} & \begin{pmatrix} \pi_{3311} & \pi_{3312} & \pi_{3313} \\ \pi_{3321} & \pi_{3322} & \pi_{3323} \\ \pi_{3331} & \pi_{3332} & \pi_{3333} \end{pmatrix} \end{bmatrix}. \tag{C.2}$$

Due to the symmetry of the silicon crystal the piezotensor can be reduced further. Silicon belongs to the point group $m3m$ which requires three symmetry elements to be fully described. The transformation law of a fourth rank tensor is

$$\pi'_{ijkl} = M_{im}M_{jn}M_{ko}M_{lp}\pi_{mnop}, \tag{C.3}$$

where $M_{\alpha\beta}$ ($\alpha = i, j, k, l$ and $\beta = m, n, o, p$) are the coefficients in the $\boldsymbol{M}$ transformation matrix. The three symmetry elements that describes the silicon crystal, which is an FCC Bravais lattice with a basis of two atoms, can be written as the transformation matrices below [99]

- $m \perp X$ (mirror plane perpendicular to the X axis)

$$\boldsymbol{M} = \begin{bmatrix} -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{C.4}$$

- $3 \parallel [111]$ (Threefold rotation parallel to [111])

$$\boldsymbol{M} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix} \tag{C.5}$$

- $m \perp [110]$ (mirror plane perpendicular to [110])

$$\boldsymbol{M} = \begin{bmatrix} 0 & -1 & 0 \\ -1 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{C.6}$$

Applying each of the three transformations to Eq. (C.3) and using Neumanns principle (measurements made in symmetry related directions must give the same property coefficients) we obtain for each symmetry element

- $m \perp X$

$$\boldsymbol{\pi} = \begin{bmatrix} \begin{pmatrix} \pi_{1111} & 0 & 0 \\ 0 & \pi_{1122} & \pi_{1123} \\ 0 & \pi_{1132} & \pi_{1133} \end{pmatrix} & \begin{pmatrix} 0 & \pi_{1212} & \pi_{1213} \\ \pi_{1221} & 0 & 0 \\ \pi_{1231} & 0 & 0 \end{pmatrix} & \begin{pmatrix} 0 & \pi_{1312} & \pi_{1313} \\ \pi_{1321} & 0 & 0 \\ \pi_{1331} & 0 & 0 \end{pmatrix} \\ \begin{pmatrix} 0 & \pi_{1212} & \pi_{1213} \\ \pi_{1221} & 0 & 0 \\ \pi_{1231} & 0 & 0 \end{pmatrix} & \begin{pmatrix} \pi_{2211} & 0 & 0 \\ 0 & \pi_{2222} & \pi_{2223} \\ 0 & \pi_{2232} & \pi_{2233} \end{pmatrix} & \begin{pmatrix} \pi_{2311} & 0 & 0 \\ 0 & \pi_{2322} & \pi_{2323} \\ 0 & \pi_{2332} & \pi_{2333} \end{pmatrix} \\ \begin{pmatrix} 0 & \pi_{1312} & \pi_{1313} \\ \pi_{1321} & 0 & 0 \\ \pi_{1331} & 0 & 0 \end{pmatrix} & \begin{pmatrix} \pi_{2311} & 0 & 0 \\ 0 & \pi_{2322} & \pi_{2323} \\ 0 & \pi_{2332} & \pi_{2333} \end{pmatrix} & \begin{pmatrix} \pi_{3311} & 0 & 0 \\ 0 & \pi_{3322} & \pi_{3323} \\ 0 & \pi_{3332} & \pi_{3333} \end{pmatrix} \end{bmatrix}. \tag{C.7}$$

In the above transformation Neumanns principle is applied to $\pi'_{ijkl} = -\pi_{ijkl}$. This is only true if $\pi_{ijkl} = 0$.

- $3 \parallel [111]$

$$\boldsymbol{\pi} = \begin{bmatrix} \begin{pmatrix} \pi_{1111} & 0 & 0 \\ 0 & \pi_{1122} & 0 \\ 0 & 0 & \pi_{1133} \end{pmatrix} & \begin{pmatrix} 0 & \pi_{1212} & 0 \\ \pi_{1212} & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} & \begin{pmatrix} 0 & 0 & \pi_{1212} \\ 0 & 0 & 0 \\ \pi_{1212} & 0 & 0 \end{pmatrix} \\ \begin{pmatrix} 0 & \pi_{1212} & 0 \\ \pi_{1212} & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} & \begin{pmatrix} \pi_{1133} & 0 & 0 \\ 0 & \pi_{1111} & 0 \\ 0 & 0 & \pi_{1122} \end{pmatrix} & \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & \pi_{1212} \\ 0 & \pi_{1212} & 0 \end{pmatrix} \\ \begin{pmatrix} 0 & 0 & \pi_{1212} \\ 0 & 0 & 0 \\ \pi_{1212} & 0 & 0 \end{pmatrix} & \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & \pi_{1212} \\ 0 & \pi_{1212} & 0 \end{pmatrix} & \begin{pmatrix} \pi_{1122} & 0 & 0 \\ 0 & \pi_{1133} & 0 \\ 0 & 0 & \pi_{1111} \end{pmatrix} \end{bmatrix}. \tag{C.8}$$

- $m \perp [110]$

$$\boldsymbol{\pi} = \begin{bmatrix} \begin{pmatrix} \pi_{1111} & 0 & 0 \\ 0 & \pi_{1122} & 0 \\ 0 & 0 & \pi_{1122} \end{pmatrix} & \begin{pmatrix} 0 & \pi_{1212} & 0 \\ \pi_{1212} & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} & \begin{pmatrix} 0 & 0 & \pi_{1212} \\ 0 & 0 & 0 \\ \pi_{1212} & 0 & 0 \end{pmatrix} \\ \begin{pmatrix} 0 & \pi_{1212} & 0 \\ \pi_{1212} & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} & \begin{pmatrix} \pi_{1122} & 0 & 0 \\ 0 & \pi_{1111} & 0 \\ 0 & 0 & \pi_{1122} \end{pmatrix} & \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & \pi_{1212} \\ 0 & \pi_{1212} & 0 \end{pmatrix} \\ \begin{pmatrix} 0 & 0 & \pi_{1212} \\ 0 & 0 & 0 \\ \pi_{1212} & 0 & 0 \end{pmatrix} & \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & \pi_{1212} \\ 0 & \pi_{1212} & 0 \end{pmatrix} & \begin{pmatrix} \pi_{1122} & 0 & 0 \\ 0 & \pi_{1122} & 0 \\ 0 & 0 & \pi_{1111} \end{pmatrix} \end{bmatrix}. \tag{C.9}$$

The piezotensor is thus due to symmetry simplified to obtain only three independent coefficients. These coefficients are normally written in 6 vector notation

$$\begin{aligned} \pi_{1111} &\rightarrow \pi_{11} \\ \pi_{1122} &\rightarrow \pi_{12} \\ \pi_{1212} &\rightarrow \tfrac{\pi_{44}}{2} \end{aligned} \tag{C.10}$$

where the factor of $\frac{1}{2}$ in front of π_{44} is due to the symmetry of the stress tensor, for example $\pi_{1212}\sigma_{12} + \pi_{1212}\sigma_{21} = 2\pi_{1212}\sigma_{12}$. If the symmetry of the stress tensor is applied in Eq. (C.2) one obtains a fourth rank tensor with only 36 independent coefficients and all shear coefficients are multiplied with a factor of 2. By using the simplifications obtained during the application of the transformation matrices Eq. (C.2) is written in 6 vector notation as

$$\boldsymbol{\pi} = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix}. \tag{C.11}$$

This representation is normally used to describe the piezoresistive effect in silicon.

APPENDIX

D Transformation of coordinate system

Any rotation of a coordinate system can be described with three rotations as shown in Fig. D.1. Mathematically this can be done by using a rotation matrix **M** defined by

$$\mathbf{M} = \begin{bmatrix} l_1 & m_1 & n_1 \\ l_2 & m_2 & n_2 \\ l_3 & m_3 & n_3 \end{bmatrix} = \mathbf{ABC} \tag{D.1}$$

where the three individual rotations **A**, **B** and **C** are given by (this is known as the "y-convention" for the rotation matrices)

$$\mathbf{A} = \begin{bmatrix} \sin\phi & -\cos\phi & 0 \\ \cos\phi & \sin\phi & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad \mathbf{B} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos\theta & \sin\theta \\ 0 & -\sin\theta & \cos\theta \end{bmatrix} \quad \mathbf{C} = \begin{bmatrix} -\sin\psi & \cos\psi & 0 \\ -\cos\psi & -\sin\psi & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

The definition of the angles ϕ, θ, and ψ is shown in Fig. D.1. Performing the multiplications we

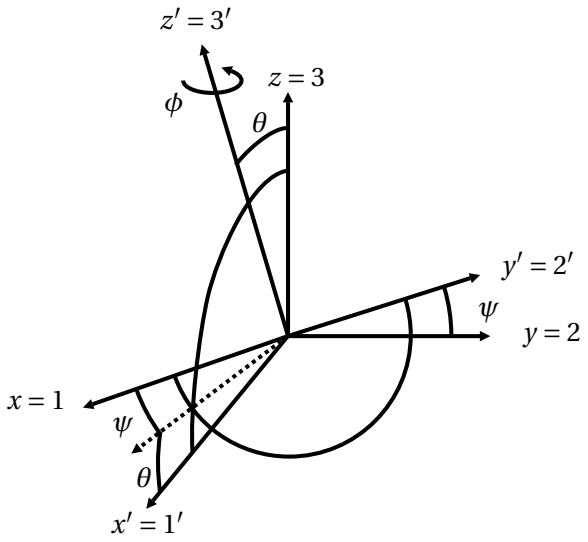


Figure D.1: Definition of the Euler angles defining the rotation from the unprimed to the primed system.

have,

$$\mathbf{M} = \begin{bmatrix} \sin\phi & -\cos\phi & 0 \\ \cos\phi & \sin\phi & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos\theta & \sin\theta \\ 0 & -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} -\sin\psi & \cos\psi & 0 \\ -\cos\psi & -\sin\psi & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{D.2}$$

$$= \begin{bmatrix} -\sin\phi\sin\psi + \cos\phi\cos\theta\cos\psi & \sin\phi\cos\psi + \cos\phi\cos\theta\sin\psi & -\cos\phi\sin\theta \\ -\cos\phi\sin\psi - \sin\phi\cos\theta\cos\psi & \cos\phi\cos\psi - \sin\phi\cos\theta\sin\psi & \sin\phi\sin\theta \\ \sin\theta\cos\psi & \sin\theta\sin\psi & \cos\theta \end{bmatrix} \tag{D.3}$$

The numbers l_3, m_3 and n_3 depends on the orientation of the substrate. For a wafer of orientation (l,m,n) the numbers are given by

$$\begin{bmatrix} l_3 \\ m_3 \\ n_3 \end{bmatrix} = \frac{1}{\sqrt{l^2+m^2+n^2}} \begin{bmatrix} l \\ m \\ n \end{bmatrix} \tag{D.4}$$

For the (001) silicon substrate there is no rotation of the x and y axis meaning that both θ and ψ in Fig. D.1 equal zero. The only rotation possible is the rotation around the z-axis given by the angle ϕ in Fig. D.1. The numbers l_3, m_3 and n_3 are found using Eq. (D.4)

$$\begin{bmatrix} l_3 \\ m_3 \\ n_3 \end{bmatrix} = \begin{bmatrix} \sin\theta\cos\psi \\ \sin\theta\sin\psi \\ \cos\theta \end{bmatrix} = \frac{1}{\sqrt{1+0+0}} \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} \tag{D.5}$$

Then, the other coefficients are obtained from Eq. (D.3)

$$\mathbf{M} = \begin{bmatrix} l_1 & m_1 & n_1 \\ l_2 & m_2 & n_2 \\ l_3 & m_3 & n_3 \end{bmatrix} = \begin{bmatrix} +\cos\phi & \sin\phi & 0 \\ -\sin\phi & \cos\phi & 0 \\ 0 & 0 & 1 \end{bmatrix}. \tag{D.6}$$

This transformation matrix can be used to transform any tensor in the xy plane on a (001) substrate.

APPENDIX

E Electric field relation to resistance

The electrical resistance of the resistor in Fig. E.1 is defined as

$$R = \frac{V}{I} = \frac{\int_A^B \boldsymbol{E} \cdot \boldsymbol{dl}}{I}, \tag{E.1}$$

where I is the current, V is the potential drop, and $\boldsymbol{E}$ is the electric field vector from A to B in the direction described by the vector $\boldsymbol{dl}$. In the following the current I is constant and directed along the E_x direction.

The resistance of the resistor in Fig. E.1 along the length of the resistor in the E_x direction is given by

$$R = \frac{V}{I} = \frac{\int_0^L E_x \cdot dl}{I} = \frac{E_x \cdot L}{I}. \tag{E.2}$$

The same equation is valid for a resistance R_0 where E_x is substituted with E_0. Thus one can write

$$\frac{E_x - E_0}{E_0} = \frac{R_x - R_0}{R_0}. \tag{E.3}$$

Here it is assumed that the resistor dimensions do no change in the two cases of R_0 and R_x. If there is a change in dimensions one needs to add an extra term describing this change. For example,

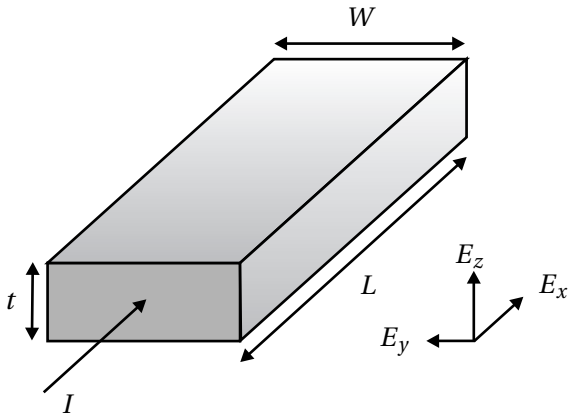


Figure E.1: Illustration of a simple rectangular resistor where t is the thickness, W is the width, and L is the length.

if the change is caused by a stress applied to the resistor the change is proportional to $(1+2\nu)\varepsilon$, where ν is the poisson's ratio and ε is the strain resulting from the applied stress. In silicon this term is significantly smaller than the change in the electric field and is thus considered negligible.

Now consider the potential drop perpendicular to the current density vector. We define $R_H = \frac{V_\perp}{I_\parallel}$, where $V_\perp$ is the potential drop (in the xy plane) perpendicular to the current direction described by I.

$$R_H = \frac{V_\perp}{I} = \frac{\int_0^W E_y \cdot dl}{I} = \frac{E_y \cdot W}{I}. \tag{E.4}$$

The sheet resistance $R_\square$ of the resistor in Fig. E.1 is defined as

$$R_\square = \frac{1}{\int_0^t qN(z)\mu(z)dz}, \tag{E.5}$$

where t is the thickness, q is the carrier charge, $N(z)$ is the doping concentration in the resistor and $\mu(z)$ is the carrier mobility. Assuming a constant doping profile in the resistor the equation is simplified to

$$R_\square = \frac{1}{qN\mu\int_0^t dz} = \frac{1}{qN\mu t} = \frac{\rho}{t}, \tag{E.6}$$

where ρ is the resistivity. Now, defining $E_0 = J_x\rho_0$ we write (where the subscript 0 is for zero stress)

$$R_{\square,0} = \frac{\rho_0}{t} = \frac{E_0}{J_x t} = \frac{E_0 W t}{I t} = \frac{E_0 W}{I}. \tag{E.7}$$

Thus,

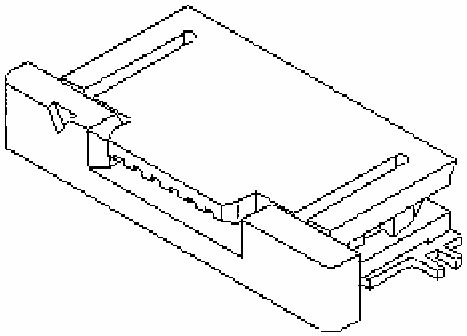
$$\frac{E_y}{E_0} = \frac{R_H}{R_{\square,0}}. \tag{E.8}$$

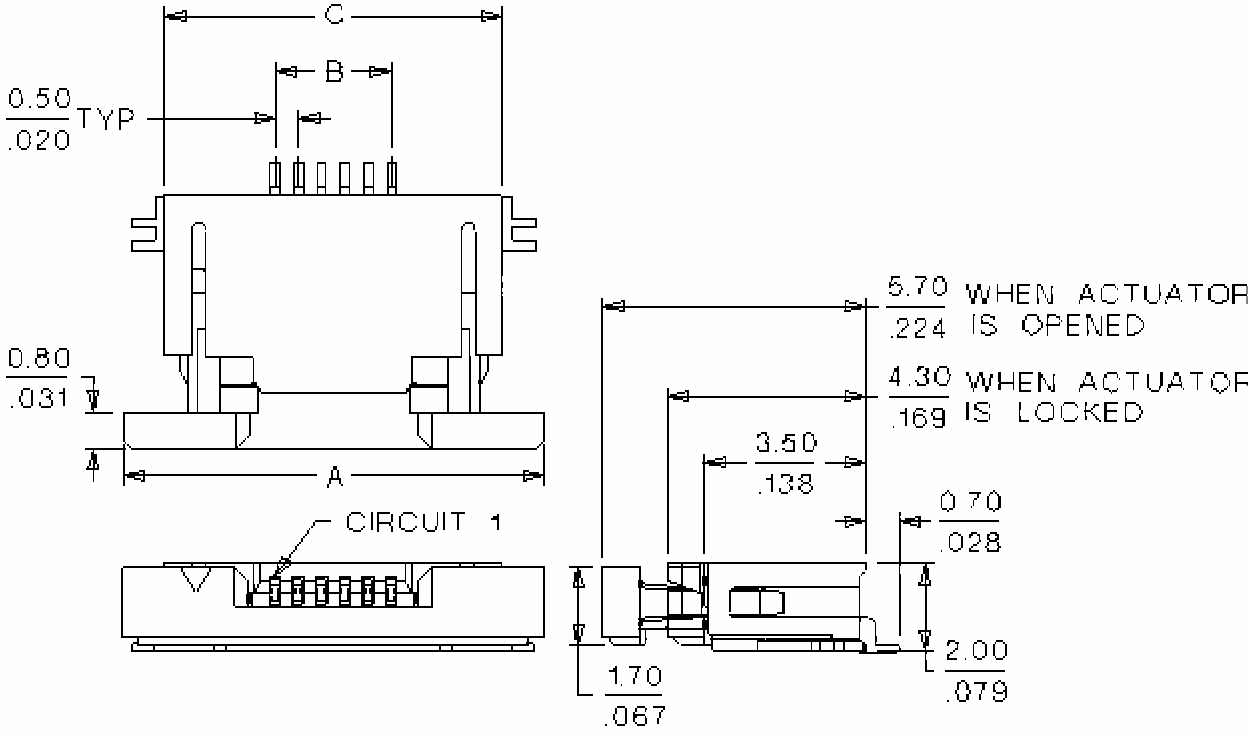
APPENDIX

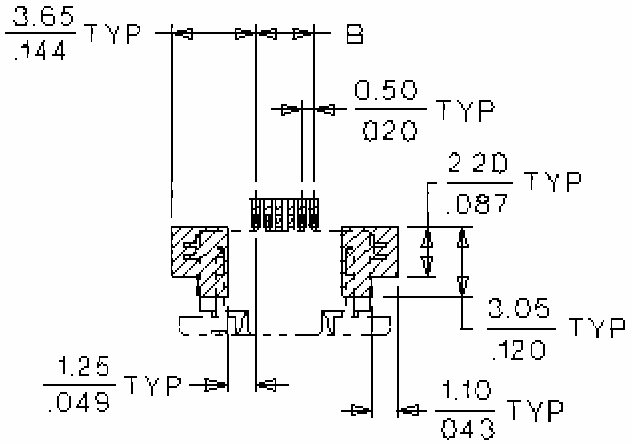
F

Data sheet of Zero Insertion Force, ZIF, connector

FFC/FPC-to-Board 0.50mm (.020") SMT, Right Angle, ZIF, Top Contact Style Receptacle
52745 / 52435







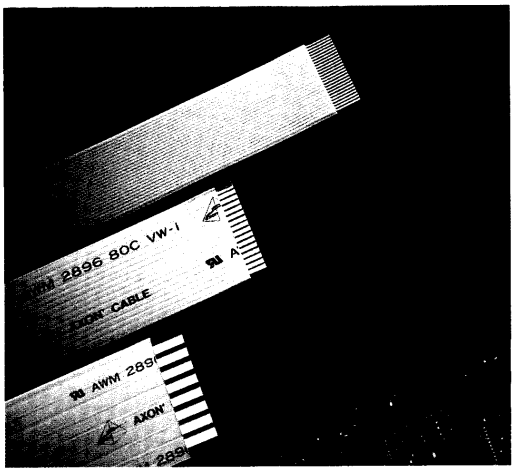
PCB LAYOUT: SOLDER SIDE

APPENDIX

G Data sheet of Flat Flexible Cable, FFC

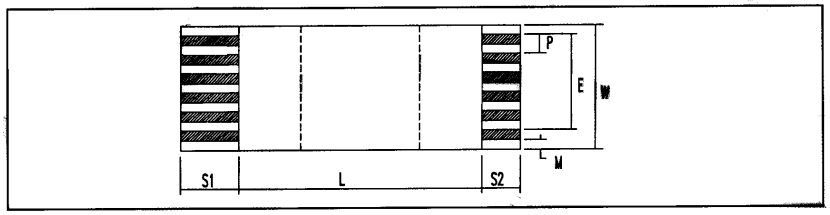
AXOJUMP® FLAT FLEXIBLE CABLES

AXOJUMP® Flat Flexible Cables consist of flat tin plated copper conductors insulated between Polyester based tapes. Dependant on the type of interconnection used, reinforcement tapes can be added to the cable ends.

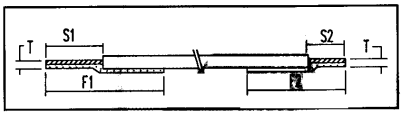


STRIPPING/CONNECTION

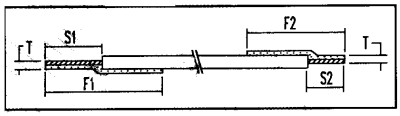
General scheme (Type A)



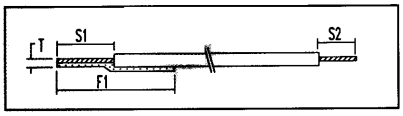
Type A Connector/Connector



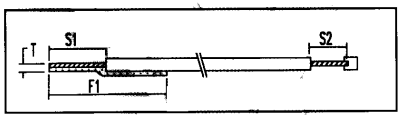
Type D Connector/Connector (opposite)



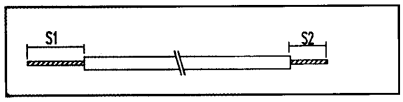
Type B Connector/Solder



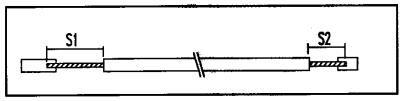
Type E * Connector/Solder



Type C Solder/Solder



Type F * Solder/Solder



* Note : The overlapping length of insulation on the conductor at the pre-stripped end is approximately 1 mm.

GENERAL CHARACTERISTICS (standard products)

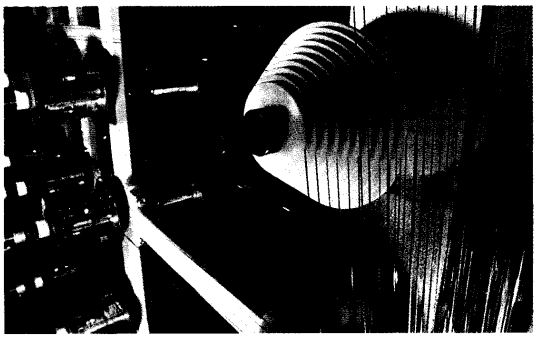
PITCH:P	mm	0.50	0.80	1.00	1.25	1.27	2.54
TYPES		A-D-E-F		A-B-C-D-E-F			
NUMBER OF CONDUCTORS (N)							
TYPES A and D (min./max.)		9 to 91	5 to 104	4 to 99	3 to 79	3 to 77	2 to 38
TYPES B and C (min./max.)		ON REQUEST		4 to 99	3 to 79	3 to 77	2 to 38
TYPES E and F (min./max.)		13 to 59	8 to 36	6 to 29	5 to 23	5 to 22	2 to 10
CABLE WIDTH : W		(N+1) 0.50	(N+1) 0.80	(N+1) 1.00	(N+1) 1.25	(N+1) 1.27	(N+1) 2.54
MARGIN : M	mm	0.35	0.55	0.65	0.85	0.87	1.75
CONDUCTOR WIDTH : C	mm	0.30	0.,50	0.70	0.80	0.80	1.57
STRIP LENGTH : S	mm	2-3-4-5-6-7					
REINFORCEMENT LENGTH : F	mm	6-8-9-10-15					
INSULATED LENGTH : L (*)	mm	TYPES A and D = 20 to 1500 TYPES E and F = 40 to 1500		TYPES A-B-C-D = 20 to 9999 TYPES E and F = 40 to 9999			
END THICKNESS : T	mm	0.30 +/- 0.05					
CONDUCTOR THICKNESS							
STANDARD : S (TYPES A-B-C-D-E-F)	mm	0.10					0.076
FLEXIBLE : F (TYPES A-B-C-D)	mm	0.05					ON REQUEST
EXTRA-FLEXIBLE : E (TYPES A and D)	mm	ON REQUEST		0.035			

(*) Insulated length for extra-flexible versions = 60 to 1500 mm
NOTE : for non-standard configurations a design can be provided on request

QUALITY : ISO 9001

AXON' CABLE continues to invest in Quality Assurance. The company is approved to several international standards including ISO 9001 and the Quality Department ensures that standards are constantly maintained. Internationally recognised programmes and methods such as "Statistical Process Control" and TPM (Total Productive Maintenance) are applied throughout our manufacturing area in order to improve productivity. The AXO-JUMP® range of cables has obtained the approvals listed hereafter :

UL STYLE	VOLTAGE	TEMPERATURE
UL STYLE 2896	30 V A.C.	80 °C (176 °F)
UL STYLE 2643	300 V A.C.	105 °C (221 °F)
UL STYLE 20624	60 V A.C.	80 °C (176 °F)
UL STYLE 20696	30 V A.C.	80 °C (176 °F)
UL STYLE 2537	300 V A.C.	80 °C (176 °F)
UL STYLE 2737	300 V A.C.	80 °C (176 °F)
UL STYLE 20566	90 V A.C.	105 °C (221 °F)



STANDARD PRODUCTS

FFC 1.00 A 25 / 200 - L - 5 - 5 - 10 - 10 - S - B

MARKING :
A = Not marked
B = Standard marking
(with UL STYLE 2896 or 20624
and AXON' logo)
Other marking types on request.

CONDUCTOR THICKNESS :
S (standard) = 0.1 mm/0.004 in
(0.076/0.003 in for pitch 2.54)
F (flexible) = 0.05 mm/0.02 in
E (extra-flexible) = 0.035 mm/0.001 in
(only for 1.00 mm - 1.25 mm - 1.27 mm pitches)

REINFORCEMENT LENGTH in mm (F2)-END 2

REINFORCEMENT LENGTH in mm (F1)-END 1

STRIP LENGTH in mm (S2)-END 2

STRIP LENGTH in mm (S1)-END 1

TYPE OF TAPES : see table below

INSULATED LENGTH in mm = L

NUMBER OF CONDUCTORS (N)

TYPE OF STRIPPING
A : Stripped at both ends on 2 sides with reinforcements on the same side.
B : One end : stripped on 2 sides with reinforcement. Other end : stripped on 2 sides without reinforcement.
C : Stripped at both ends on 2 sides without reinforcement.
D : Stripped at both ends on 2 sides with reinforcements on opposite sides.
E : One end : stripped on both sides with reinforcement. Other end : pre-stripped on 2 sides without reinforcement.
F : Pre-stripped at both ends on 2 sides without reinforcement.

PITCH = 0.50/0.80/1.00/1.25/1.27/2.54 mm

FFC = FLAT FLEXIBLE CABLE

Reinforcement types

- Polyester reinforcements (standard version) for terminating with connector.
- Polyimide reinforcements (on request) for "hot bar" soldering.
- Combination of polyester/polyimide reinforcements (on request).

Type of tapes

Tape Reference	Colour	Standard Conductor (S)	Flexible Conductor (F)	Extra-flexible Conductor (E)	UL Style	Types of Stripping
L	White	X	X		2896	A-B-C-D-E-F
H	White	X	X		2643-20566-2537-2737	A-B-C-D
E	White			X	20696-2896-20624	A and D
R	White	X	X		20696	A-B-C-D
P	White	X	X		20624	A-B-C-D
M	Black	X	X		2896	A-B-C-D
N	Black			X	20696-2896-20624	A and D

AXON' reserves the right to change the composition of FFC cables without prior notice.

APPENDIX

H Calculation of self-heating in resistors

The self-heating of a resistor can cause significant errors in a piezoresistor. This appendix contains brief calculations of the self-heating in resistors. For a more detailed description, see Ref. [13].

The steady-state temperature rise $T_{ss,I}$ for a constant current I can be approximated to

$$T_{ss,I} = \frac{R_0 R_T I^2}{1 - \alpha_R R_0 R_T I^2}, \tag{H.1}$$

where α_R is the temperature coefficient of resistance, R_0 is the resistance at room temperature and R_T can be approximated to be

$$R_T = \frac{1}{\pi L \kappa} \ln(10), \tag{H.2}$$

when assuming the cross section of the resistor has a semicircle shape lying in the surface of the substrate with a length L. The temperature is assumed to be constant in a distance of 10 times the radius of the semi circle. κ is the thermal conductivity.

The temperature coefficient of resistance is, in the worst case scenario, that is at low doping concentration and low temperature approximately $\alpha \approx 0.005\ \mathrm{K}^{-1}$.

The worst case value for κ is for undoped Si: $\kappa = 148\ \frac{W}{m \cdot K}$. Thus,

$$R_T = \frac{\ln(10)}{3.14 \cdot 148 \cdot L} = 5 \cdot 10^{-3} \frac{1}{L}. \tag{H.3}$$

The length of one resistor is $L = 500\ \mu$m. This gives the result

$$R_T = 10 \frac{K}{W} \tag{H.4}$$

In the piezoresistive measurements $\frac{\Delta R}{R} \approx 0.1\%$ in the worst case examples. If the accuracy should be 0.1%, the self-heating induced error should be less than one part in 10^6. Thus, the maximum permitted value of T_R is

$$T_{R,max} = \frac{10^{-6}}{\alpha_R} \approx 0.0002K \tag{H.5}$$

when using the worst case value of $\alpha = 0.005$, i.e. the maximum value. By inserting this in Eq. (H.1) and again assuming worst case scenario, i.e. $T_{ss} = T_{R,max} \approx R_0 R_T I^2$, one obtains

$$I_{max} = \sqrt{\frac{T_{R,max}}{R_0 R_T}} \approx \sqrt{\frac{0.0002}{50 \cdot 10^3 10}} = 20 \mu A \tag{H.6}$$

where the maximum resistance is $R_0 = 50$ kΩ. Thus, with these worst case scenarios a maximum current of $I_{max} = 20$ μA can be forced through the resistor in order to obtain the accuracy stated above. For smaller resistance values the maximum current is larger according to Eq. (H.6).

The calculations give a good estimate of what magnitudes of current is allowable to prevent that self-heating of the resistors influence the results. Since the piezoresistive measurements are carried out with currents of approximately $I = 20$ μA, and the above investigation is done with worst case scenarios, it is not expected that self-heating of the resistor affects the results.

APPENDIX

I Process flows

I.1 KOH crystal alignment

Step	Process	Parameters	Comments
1 . 0	Silicon substrate (100)		
2 . 0	Oxidation	Batch 1: Recipe:WET_1100 Temp: 1100degC Time: 35min Thickness: 5000Å	Save one wafer for oxide etch in later process
2 . 1	Ellipsometer	Oxide thickness on testwa	Measured thickness:
3 . 0	Photolithography	KOH: Alignment marks	
3 . 1	HMDS	Time: 30min+10min coolin	Use program 4
3 . 2	Resist on backside	1.5um recipe: PR1_5	Clean nozzle
3 . 3	Resist on frontside	1.5um recipe NO BAKE: PR1_5nb	Clean nozzle
3 . 4	Baking	oven for 30min Use 90 Degrees	
3 . 5	Expose in alligner	Time: 10sec Use hard contact 100/10 Separation 20um	6sec at airdamp 50% to 10sec at airdamp 40%
3 . 6	Development	Time: 60sec	
3 . 7	Baking	oven for 25min Use REV120	Check resist on testwafer Reset to 90degC
4 0	Plasma asher	Manual mode Oxygen 50 ccm Nitrogen 50 ccm Power 150 W Time: 10 min	To remove the remaning resist
5 . 0	BHF etch	Oxide etch Time: 5min	Use testwafer to determine time
6 . 0	Resist strip Acetone	Bath 1: 1min Bath 2: 3min + US	
7 . 0	7up	Temp: 80degC Time: 10min	Remove resist totally rinse 5min
8 0	BHF etch	15s Use bath next ot KOH Rinse 2 min crude 3 min fine	Make sure there is no oxide in the holes
9 . 0	KOH (PH14)	Etchrate in Si: 1.3um/min Etchrate in ox: 60Å/min Temp: 80degC Time: 13min30sec	
10 . 0	BHF etch	Oxide removal Time: 7min	All Oxide is removed
11 . 0	Characterize		The wafers are characterized to find the best crystal alignment

I.2 MBE grown strained crystals

Step	Process	Parameters	Comments
1.0	Oxidation	Batch 1: Recipe:WET_1100 Temp: 1100degC Time: 35min Thickness: 5000Å	Save one wafer for oxide etch in later process
1.1	Ellipsometer	Oxide thickness on testwa	Measured thickness:
2.0	Photolithography	KOH: Alignment marks	
2.1	HMDS	Time: 30min+10min coolir	Use program 4
2.2	Resist on backside	1.5um recipe: PR1_5	Clean nozzle
2.3	Resist on frontside	1.5um recipe NO BAKE: PR1_5nb	Clean nozzle
2.4	Baking	oven for 30min Use 90 Degrees	
2.5	Expose in alligner	Time: 10sec Use hard contact 100/10 Separation 20um	6sec at airdamp 50% to 10sec at airdamp 40%
2.6	Development	Time: 60sec	
2.7	Baking	oven for 25min Use REV120	Check resist on testwafer Reset to 90degC
2.8	Plasma asher	Manual mode Oxygen 50 ccm Nitrogen 50 ccm Power 150 W Time: 10 min	To remove the remaning resist
3.0	BHF etch	Oxide etch Time: 5min	Use testwafer to determine time
4.0	Resist strip Acetone	Bath 1: 1min Bath 2: 3min + US	
5.0	7up	Sulfuric acid 1 spoon of ammoniumhydroxide 80°C 10min	Remove resist totally rinse 5min
6.0	BHF etch	15s Use bath next ot KOH Rinse 2 min crude 3 min fine	Make sure there is no oxide in the holes
7.0	KOH (PH14)	Etchrate in Si: 1.3um/min Etchrate in ox: 60Å/min Temp: 80degC Time: 13min30sec	
8.0	BHF etch	Oxide removal Time: 7min	All Oxide is removed

9.0	Characterize	Optical microscope	The wafers are characterized to find the best crystal alignment
10.0	MBE growth		
11.0	Photolithography	IMP mask	
11.1	HF etch of oxide	1min., rinse 5min	
11.2	Spin-on of resist	Positive 1.5um, PR1_5	Clean nozzle
	Bake	Oven: 30min, 90deg no manual baking if track1 is used	
11.3	Exposure in aligner	Exposure time: 7s hard contact Alignment separation: 30um	Use test wafer for determining exposure time Check small contact holes!
11.4	Development	Time: 55s	Make new developer Inspect test wafer to determine development time
11.5	Plasma asher	Time: 2min Power: 200W Gases: O2: 225sccm N2: 50sccm	Remove resist residues
12.0	HF etch of oxide	1min, Rinse 5min	Remove native oxide
13.0	RIE	mba_NANO P=36mTorr O2 flow= 24 sccm CHF3 flow=10 sccm SF6 flow=30 sccm Effekt=20W Time: 25s for MBA_NANO	
14.0	Resist strip	Rough strip: 1min Fine strip: 3min US	
15.0	7-up clean	Sulfuric acid 1 spoon of ammoniumhydroxide 80°C 10min	
16.0	Dektak inspection		Measure step heigth - use prepared note
17.0	Photolithography	RIE mask	
17.1	HF etch of oxide	1min., rinse 5min	
17.2	Spin-on of resist	Positive 1.5um, PR1_5	Clean nozzle
	Bake	Oven: 30min, 90deg no manual baking if track1 is used	
17.3	Exposure in aligner	Exposure time: 7s hard contact Alignment separation: 30um	Use test wafer for determining exposure time

17.4	Development	Time: 55s	Make new developer Inspect test wafer to determine development time
17.5	Plasma asher	Time: 2min Power: 200W Gases: O2: 225sccm N2: 50sccm	Remove resist residues
17.6	Bake	30min at 120deg	ONLY IF OH_POLYA IS USED AS RIE RECIPE!
18.0	HF etch of oxide	1min, Rinse 5min	Remove native oxide
19.0	RIE	MBA_NANO P=36mTorr O2 flow= 24 sccm CHF3 flow=10 sccm SF6 flow=30 sccm Effekt=20W Time: 2min 30s	Use test wafer for determining etch time
20.0	Resist strip	Rough strip: 1min Fine strip: 3min US	
21.0	Piranha clean	20min Sulfuric acid Hydrogenperoxide	
22.0	Dektak inspection		Measure step heigth - use prepared note
23.0	PECVD oxide	Recipe: Standard Deposition rate: 0.176mm/min Temp: 300degC Time: 2min40sec	Two test wafers for HF etch Target thickness: 5000Å Test wafer, Measured thickness: Use RIE test wafer for PECVD oxide
23.1	Ellipsometer	Oxide thickness on testwa	Measured thickness:
24.0	Photolithography	ALL CON mask	
24.1	HMDS	30min + 10min cooling	
24.2	Spin-on of resist	Positive 1.5um, PR1_5	
24.3	Bake	Oven: 30min, 90deg no manual baking if track1 is used	
24.4	Exposure in aligner	Exposure: 7sec Hard contact alignment separation: 30um	Use test wafer for determining exposure time
24.5	Development	Time: 55sec	Make new developer Inspect test wafer to determine development time
24.6	Plasma asher	Time: 2min Power: 200W Gases: O2: 225sccm N2: 50sccm	Removal of resist residues

25.0	HF-etch of oxide	Time: Approximately 6min	Open contact holes test wafer used for determining time
26.0	Lithography	M20 Mask	
26.1	HMDS	30min + 10min cooling	
26.2	Spin-on of resist	Positive 2.2um, PR2_2	
26.3	Bake	Oven: 30min, 90deg no manual baking if track1 is used	
26.4	Exposure in aligner	Exposure: 4.5sec Hard contact alignment separation: 30um	Use test wafer for determining exposure time
26.5	Bake	Oven. Temp: 120deg Time: 30min or Hotplate 120deg 2min	Inversion bake Rest for 10min after baking
26.6	Flood exposure	Time 35sec	
26.7	Development	Time: 70sec	Make new developer Inspect test wafer to determine development time
27.0	HF etch of oxide	1min, Rinse 5min	Remove native oxide
28.0	Deposition of metal on frontsi	Wordentec Ti Thickness: 100nm Al Thickness: 700nm	
29.0	Liftoff	Acetone: 1min+3min US	
30.0	Photolithography	ASE mask	
30.1	HMDS	30min + 10min cooling	
30.2	Spin-on of resist	positive 9.5um, PR9_5	
30.3	Bake	Oven: 30min, 90deg no manual baking if track1 is used	
30.4	Exposure in aligner	Exposure: 90sec Hard contact alignment separation: 30um	Use test wafer for determining exposure time
30.5	Development	Time:4min30sec	Make new developer Inspect test wafer to determine development time
30.6	Bake	Hotplate 120deg 100sec	
31.0	Advanced silicon etch	Selectivity: Si:PR 40:1 Recipe: Deepetch cycles: 250	
32.0	Resist strip	Rough strip: 1min Fine strip: 3min US	
32.1	Plasma asher	Program 12 time: 15min	

I.3 Gaussian profile boron doped piezoresistors

Step	Process	Parameters	Comments
1 . 0	Silicon substrate n-type (100)	n-type (100) 1-20 Ωcm Thickness: 350 μm Double sided polished 25 wafers	
2 . 0	Ion Implantation	boron doses: 8e15 cm-2 1e15 cm-2 8e13 cm-2 Energy=30 keV	
3 . 0	BHF etch	Oxide removal Time: 2min	All Oxide is removed from all wafers.
4 . 0	Photolithography	RIE mask	2 extra test wafers for RIE-depth rate
4 . 1	HMDS	Program 4 Time: 30min+10min cooling	To dry the wafers
4 . 2	Resist	Positive 1.5um PR1_5	Clean nozzle
4 . 3	Expose in alligner	Time: 10sec Use hard contact 100/10 Separation 30um	6sec at airdamp 50% to 10sec at airdamp 40%
4 . 4	Development	Time: 60sec	
4 . 5	Plasma Asher	Time: 2min Power: 200W Gas: 225sccm O2 50 N2 Program: 32	Removal of resist residues Had problems with getting all the resist residues off. Run a few tests before putting the wafers into the RIE. Perform a BHF dip before RIE
4 . 6	Baking	Oven 120degC for 25min	
5 . 0	RIE	RIE 2. Recipe: OH_POLYA Depth: 280-300nm = 55s	Etch of implant layer, to define resistor structures. Remember different etch-times for different thicknesses. Run two test wafers and check thickness and uniformity.
6 . 0	Acetone stripper Resist strip	Bath 1: Time: 1min Bath 2: Time: 3min + US	
7 . 0	7up	Temp: 80degC Time: 10min	Remove resist totally rinse 5min
8 . 0	Photolithography	Sub con mask	
8 . 1	HMDS	Program 4 Time: 30min+10min cooling	To dry the wafers
8 . 2	Resist	Positive 2.2um PR2_2	Clean nozzle
8 . 3	Expose in alligner	Time: 10sec Use hard contact 100/10	6sec at airdamp 50% to 10sec at airdamp 40%

9	.	0	Implant	High dose Phosfor implant: Energy:45keV Dose:5E15cm-2 Current:<100uA	To make a good contact to the substrate.
10	.	0	Acetone stripper Resist strip	Bath 1: Time: 1min Bath 2: Time: 3min + US	
10	.	1	Plasma Asher	Time: 20min Power: 1000W Gas: 225 sccm O2 (500) Gas: 10 sccm CF4 (5) Program: 37	
10	.	2	7up	Temp: 80degC Time: 10min	Remove resist totally rinse 5min
11	.	0	RCA		Cleaning of wafers
12	.	0	Dry oxidation Oxidation and anneal Phosfor Drive	LPCVD Thickness: 1200-1500Å Time: 80min Temp: 1100degC	Testwafer for further processing (Oxid-etch time) Measured thickness:
12	.	1	Ellipsometer	Oxide thickness on testwafer	
13	.	0	Photolithography	CON mask	Contact holes Image reversal
13	.	1	HMDS	Program 4 Time: 30min+10min cooling	To dry the wafers
13	.	2	Resist	2.2um PR2_2	Clean nozzle
13	.	3	Expose in alligner	Time: 4.7sec Use hard contact 100/10 Separation 30um	
13	.	4	Baking	Track 1: Hot plate Recipe: REV_100s Time: 100s Temp: 120degC After baking: Rest for 10min	
13	.	5	Flood exposure	Time: 35sec	
13	.	6	Development	Time: 70sec	
13	.	7	Baking	Oven 120degC for 25min	
14	.	0	BHF	Etchrate in oxide: approx 900-1000Å/min Time: approx 4min	oxide etch
15	.	0	Acetone stripper Resist strip	Bath 1: Time: 1min Bath 2: Time: 3min + US	
16	.	0	7up	Temp: 80degC Time: 10min	Remove resist totally rinse 5min
17	.	0	Photolithography	M20 or M80	Titanium paths Image reversal
17	.	1	HMDS	Program 4 Time: 30min+10min cooling	

17	.	2	Resist	Track: 1 2.2um PR2_2 hot plate: 90degC; 60sec	
17	.	3	Expose in alligner	Time: 4.7sec Use hard contact 100/10 Separation 30um	6sec at airdamp 50% to 10sec at airdamp 40%
17	.	4	Baking	Track 1: Hot plate Recipe: REV_100s Time: 100s Temp: 120degC After baking: Rest for 10min	
17	.	5	Flood exposure	Time: 35sec	
17	.	6	Development	Time: 70sec	
18	.	0	BHF	Time: 15sec	To be sure that there is no oxide in contact holes before deposition of metal.
18	.	1	Ti/Al deposition	Alcatel Ti Thickness: 100nm Al Thickness: 700nm	
18	.	2	Lift off	3min + 20min US	
19	.	0	Plasma Asher	Program 2 Time: 15min	
20	.	0	Al anneal	Time: 30min Temp: 425degC or Time: 15 Temp: 475degC	Time and temp depends on sample. After anneal test with probes for contact.
21	.	0	Photolithography	ASE	
21	.	1	HMDS	Program 4 Time: 30min+10min cooling	To dry the wafers
21	.	2	Resist	Track 2: 9.5um PR9_5 Rest 10min	Clean nozzle
21	.	3	Expose in alligner	KS Aligner Time: 90s Use hard contact 100/10 Separation 30um ci2	
21	.	4	Development	Time: 4min30sec	
21	.	5	Baking	Hot plate Use REV120: 120degC, time: 100s	
22	.	0	ASE	Selectivity: Si:PR 40:1 Recipe: deepetch cycles:250	Etch approx 300μm down. Run test to determine etch-rate
23	.	0	Acetone stripper Resist strip	Bath 1: Time: 1min Bath 2: Time: 3min + US	
23	.	1	Plasma Asher	Program 2 Time: 15min	

I.4 Gaussian profile phosphorus doped piezoresistors

Step	Process	Parameters	Comments
1.0	4 Silicon substrate p-type (100)	p-type (100) and n-type (100) 1-20 Ωcm Thickness: 350 μm Double sided polishec	
2.0	Thermal oxidation	Recipe:dry1050 Time: 35 min Temp: 1050C	
2.1	Filmtek	Check oxide thickness on test wafer	Thickness: 560 Å
3.0	Ion Implantation	Energy: 30keV: Wafer no 3,4: Phosphorous dose: 9E14 cm-2 Wafer no 6,7: Phosphorous dose: 8E13 cm-2	
4.0	Photolithography	RIE mask	2 extra test wafers for RIE-depth rate
4.1	HF	4 min rinse 5 min	Etch existing oxide and prepare the wafers for photolithography
4.2	Resist	Positive 1.5um PR1_5	Clean nozzle
4.3	Expose in alligner	Time: 10sec Use hard contact 100/10 Separation 30um	6sec at airdamp 50% to 10sec at airdamp 40%
4.4	Development	Time: 60sec	
4.5	Plasma Asher	Time: 2min Power: 200W Gas: 225sccm O2 50 N2 Program: 32	Removal of resist residues Had problems with getting all the resist residues off. Run a few tests before putting the wafers into the RIE. Perform a BHF dip before RIE
4.6	Baking	Oven 120degC for 25min	
4.7	HF	HF dip before RIE. 30 secs rinse 5 min	To obtain a nice surface after RIE
5.0	RIE	RIE 2. Recipe: OH_POLYA Depth: 500nm = ca 2 min	Etch of implant layer, to define resistor structures. Run two test wafers and check thickness and uniformity before running til real wafers.
5.1	Acetone stripper Resist strip	Bath 1: Time: 1min Bath 2: Time: 3min + US	
5.2	7up	Temp: 80degC Time: 10min	Remove resist totally rinse 5min
6.0	RCA	RCA clean	
6.1	Oxidation and annealing	Recipe: dry1000 Temperature: 1000C Time: 160 min	Include 3 testwafers for use to determine etch rate later.
6.2	Filmtek	Oxide thickness on testwafer	Recipe: SiO2-4inches-5points-thin
7.0	Photolithography	Sub mask	
7.1	HMDS	Program 4 Time: 30min+10min cooling	To dry the wafers
7.2	Resist	Positive 2.2um PR2_2	Clean nozzle

7	.	3	Expose in alligner	Time: 10sec Use hard contact 100/10 Separation 30um	6sec at airdamp 50% to 10sec at airdamp 40%
7	.	4	Development	Time: 60sec	
7	.	5	Oven Hardbake	Oven 250degC for 30min	
8	.	0	HF	HF Time: 2min Rinse: 5 min	Etch holes in oxide where implantations are planned. The structures are big and etch rate is not that important - as long as the oxide is etched away its ok.
9	.	0	Implant	Wafer: 1,2,3,4,6,7,8,9,10,11: High dose Boron implant: Energy:45keV Dose:5E15cm-2 Current:<100uA Wafer: 13-22:	To make a good contact to the substrate.
9	.	1	Acetone stripper Resist strip	Bath 1: Time: 1min Bath 2: Time: 3min + US	
9	.	2	Plasma Asher	Time: 30-40min Power: 1000W Gas: 225 sccm O2 (500) Gas: 10 sccm N (5) Program: 37	Make sure all the resist is off.
9	.	3	Filmtek	Check oxide thickness on test some of the wafers	The oxid should still be around 100nm
9	.	4	7up	Temp: 80degC Time: 10min	Remove resist totally rinse 5min
10	.	0	Photolithography	Con mask	
10	.	1	HMDS	Program 4 Time: 30min+10min cooling	To dry the wafers
10	.	2	Resist	Positive 1.5um PR1_5	Clean nozzle
10	.	3	Expose in alligner	Time: 7sec Use hard contact 100/10 Separation 30um	Run tests first. The development needs to be checked - small contacts holes, diameter 3um, in the center (100um radius) of the circular resistor. 6sec at airdamp 50% to 10sec at airdamp 40%
10	.	4	Development	Time: 60sec	
10	.	5	Plasma Asher	Time: 2min Power: 200W Gas: 225sccm O2 50 N2 Program: 32	Removal of resist residues Had problems with getting all the resist residues off. Run a few tests before putting the wafers into the RIE. Perform a BHF dip before RIE
10	.	6	Oven Hardbake	Oven 250degC for 30min	
11	.	0	HF	HF Time: Rinse: 5 min	Etch holes in oxide where implantations are planned. IMPORTANT: Use testwafers to find the etch rate. Some of the
12	.	0	Implant	Wafer: 3,4,6,7: High dose Phosphorous implant: Energy:45keV Dose:5E15cm-2 Current:<100uA	To make a good contact to the resistor.
12	.	1	Acetone stripper Resist strip	Bath 1: Time: 1min Bath 2: Time: 3min + US	

12	.	2	Plasma Asher	Time: 20min Power: 1000W Gas: 225 sccm O2 (500) Gas: 10 sccm CF4 (5) Program: 37	
12	.	3	7up	Temp: 80degC Time: 10min	Remove resist totally rinse 5min
13	.	0	RCA		Cleaning of wafers.
14	.	0	Anneal	Anneal furnace Nitrogen atmosphere Temperature: 1000 Time: 30 min	Annealing the implanted areas.
15	.	0	Photolithography	M80 mask on wafer 1,2,13,14 M20 mask on the rest og the wafers	Mettalization lift-off Image reversal process
15	.	1	HMDS	Program 4 Time: 30min+10min cooling	
15	.	2	Resist	Track: 1 2.2um PR2_2 hot plate: 90degC; 60sec	
15	.	3	Expose in alligner	Time: 4.7sec Use hard contact 100/10 Separation 30um	6sec at airdamp 50% to 10sec at airdamp 40%
15	.	4	Baking	Track 1: Hot plate Recipe: REV_100s Time: 100s Temp: 120degC After baking: Rest for 10min	
15	.	5	Flood exposure	Time: 35sec	
15	.	6	Development	Time: 70sec	
15	.	7	BHF	Time: 15sec	To be sure that there is no oxide in contact holes before deposition of metal.
16	.	0	Ti/Al deposition	Alcatel/Wordentec Ti Thickness: 100nm Al Thickness: 600nm	
16	.	1	Lift off	3min + 20min US	Check wafers every 5 minutes
16	.	2	Plasma Asher	Program 2 Time: 15min	
16	.	3	Al anneal	Time: 15 Temp: 475degC	
17	.	0	Photolithography	ASE	Include test wafer for ASE process
17	.	1	HMDS	Program 4 Time: 30min+10min cooling	To dry the wafers
17	.	2	Resist	Track 2: 9.5um PR9_5 Rest 10min	Clean nozzle
17	.	3	Expose in alligner	KS Aligner Time: 90s Use hard contact Separation 30um ci2	
17	.	4	Development	Time: 4min30sec	
17	.	5	Baking	Hot plate Use REV120: 120degC, time: 100s	
18	.	0	ASE	Selectivity: Si:PR 40:1 Recipe: deepetch cycles:250	Etch approx 300μm down. Run test to determine etch-rate
18	.	1	Acetone stripper Resist strip	Bath 1: Time: 1min Bath 2: Time: 3min + US	
18	.	2	Plasma Asher	Program 2 Time: 15min	

I.5 Uniformly doped piezoresistors

Step			Process	Parameters	Comments
1	.	0	3 SOI device layer p-type (100) 1 SOI devcie layer n-type (100)	p-type (100) and n-type (100) 1-20 Wcm Substrate thickness: 350 mm Oxide thickness: 2um Device layer thickness: 2um Double sided polished	
2	.	0	Thermal oxidation	1. oxidation: Recipe:wet1100 Time: 600 min Temp: 1100C BHF etch 2. oxidation: Recipe:wet1100 Time: 20 min Temp: 1100C	To thin the device layer. After this step the device layer is 320-400nm thick.
2	.	1	BHF	Etch oxide	
3	.	0	Ion Implantation	10 wafers (all Energy: 50keV: 1 Phosphorous dose: 1.1E15 cm-2 1 Boron dose: 1.5E15 cm-2 1 Boron dose: 1.5E14 cm-2 1 Boron dose: 1.5E13 cm-2	
4	.	0	Photolithography	RIE mask	2 extra test wafers for RIE-depth rate
4	.	1	HF	2 min rinse 5 min	Etch existing oxide and prepare the wafers for photolithography
4	.	2	Resist	Positive 1.5um PR1_5	Clean nozzle
4	.	3	Expose in alligner	Time: 10sec Use hard contact 100/10 Separation 30um	6sec at airdamp 50% to 10sec at airdamp 40%
4	.	4	Development	Time: 60sec	
4	.	5	Plasma Asher	Time: 2min Power: 200W Gas: 225sccm O2 50 N2 Program: 32	Removal of resist residues Had problems with getting all the resist residues off. Run a few tests before putting the wafers into the RIE
4	.	6	Baking	Oven 120degC for 25min	
4	.	7	HF	HF dip before RIE. 30 secs rinse 5 min	To obtain a nice surface after RIE
5	.	0	RIE	RIE 2. Recipe: OH_POLYA Depth: 500nm = ca 2 min	Etch of implant layer, to define resistor structures. Run two test wafers and check thickness and uniformity before running til real wafers. Can we check that the device layer is etched with end-point detection?
5	.	1	Acetone stripper Resist strip	Bath 1: Time: 1min Bath 2: Time: 3min + US	
5	.	2	7up	Temp: 80degC Time: 10min	Remove resist totally rinse 5min
6	.	0	RCA	RCA clean	
6	.	1	Oxidation and annealing	Recipe: dry1000 Temperature: 1000C Time: 160 min	It is your recipes that need to be here.Include 3 testwafers for use to determine etch rate later.
6	.	2	Filmtek	Oxide thickness on testwafer	Recipe: SiO2-4inches-5points-thin
7	.	0	Photolithography	Con mask	
7	.	1	HMDS	Program 4 Time: 30min+10min cooling	To dry the wafers
7	.	2	Resist	Positive 1.5um PR1_5	Clean nozzle
7	.	3	Expose in alligner	Time: 7sec Use hard contact 100/10 Separation 30um	Run tests first. The development needs to be checked - small contacts holes, diameter 3um, in the center (100um radius) of the circular resistor. 6sec at airdamp 50% to 10sec at airdamp 40%
7	.	4	Development	Time: 60sec	
10	.	5	Plasma Asher	Time: 2min Power: 200W Gas: 225sccm O2 50 N2 Program: 32	Removal of resist residues.
7	.	6	Oven Hardbake	Oven 250degC for 30min	

8	.	0	HF	HF Time: Rinse: 5 min	Etch holes in oxide where implantations are planned. IMPORTANT: Use testwafers to find the etch rate. Some of the
9	.	0	Implant	High dose Phosphorous implant: Energy:45keV Dose:5E15cm-2 Current:<100uA High dose Boron implant: Energy:45keV Dose:5E15cm-2 Current:<100uA	To make a good contact to the resistor.
9	.	1	Acetone stripper Resist strip	Bath 1: Time: 1min Bath 2: Time: 3min + US	
9	.	2	Plasma Asher	Time: 30min Power: 1000W Gas: 225 sccm O2 (500) Gas: 10 sccm N2 (5)	
9	.	3	7up	Temp: 80degC Time: 10min	Remove resist totally rinse 5min
10	.	0	RCA	NO HF dip!!!!!!! Since there is oxide on the wafers!!!	Cleaning of wafers.
11	.	0	Anneal	Anneal furnace Nitrogen atmosphere Temperature: 1000 Time: 30 min	Put in the time and temperature that you have found. Annealing the implanted areas.
12	.	0	Photolithography	M80 mask on wafer 1,2,13,14 M20 mask on the rest og the wafers	Mettalization lift-off Image reversal process
12	.	1	HMDS	Program 4 Time: 30min+10min cooling	
12	.	2	Resist	Track: 1 2.2um PR2_2 hot plate: 90degC; 60sec	
12	.	3	Expose in alligner	Time: 4.7sec Use hard contact 100/10 Separation 30um	6sec at airdamp 50% to 10sec at airdamp 40%
12	.	4	Baking	Track 1: Hot plate Recipe: REV_100s Time: 100s Temp: 120degC After baking: Rest for 10min	
12	.	5	Flood exposure	Time: 35sec	
12	.	6	Development	Time: 70sec	
12	.	7	BHF	Time: 15sec	To be sure that there is no oxide in contact holes before deposition of metal.
13	.	0	Ti/Al deposition	Alcatel/Wordentec Ti Thickness: 100nm Al Thickness: 600nm	
13	.	1	Lift off	3min + 20min US	Check wafers every 5 minutes
13	.	2	Al anneal	Time: 15 Temp: 475degC	
14	.	0	Photolithography	ASE	Include test wafer for ASE process
14	.	1	HMDS	Program 4 Time: 30min+10min cooling	To dry the wafers
14	.	2	Resist	Track 2: 9.5um PR9_5 Rest 10min	Clean nozzle
14	.	3	Expose in alligner	KS Aligner Time: 90s Use hard contact Separation 30um ci2	
14	.	4	Development	Time: 4min30sec	
14	.	5	Baking	Hot plate Use REV120: 120degC, time: 100s	
14	.	6	BHF	Time:	Etch the oxide layer in the ASE trenches of approx 2 um.
15	.	0	ASE	Selectivity: Si:PR 40:1 Recipe: deepetch cycles:250	Etch approx 300mm down. Run test to determine etch-rate
15	.	1	Acetone stripper Resist strip	Bath 1: Time: 1min Bath 2: Time: 3min + US	

I.6 Silicon nanowires

Step	Process	Parameters	Comments
1.0	SOI device layer p-type (100)	p-type (100) 1-10 Wcm (approx. 5*10^15 cm-3) Substrate thickness: 525 mm Oxide thickness: 1um Device layer thickness: 340nm	Measure resistivity and thickness.
2.0	Thermal oxidation (If device layer is too thick)	1. oxidation: Recipe:wet1100 Time: 600 min Temp: 1100C BHF etch for approximately 27min (80nm/min) 2. oxidation: Recipe:wet1100 Time: 220 min Temp: 1100C	1. oxidation gives ~2100nm oxide. after 2. oxidation there should be 500nm silicon (if 2µm initially).
2.1	BHF	Etch oxide for approx.16 min	80nm/min
3.0	Ion Implantation	10 wafers (all Energy: 50keV) 1 Boron dose: 1E13 cm-2 1 Boron dose: 1E16 cm-2	final NW has 10^17 and 5*10^19 respectively (athena). Measure the actual resistivity.
4.0	Overhead mask (if device layer is gone at alignment mark positions)	HF (adhesion), Resist, Exposure, Develop, RIE (Si), HF (oxide), Acetone strip	Use overhead transparent mask to etch through device and oxide down to handle at alignment locations.
5.0	Handle thinning	If wafer is too thick (i.e. >350µm)	
5.1	BHF	Remove all oxide	
5.2	PECVD1	kar_nitr, 12 min for 580nm on device layer side	Run test first.
5.3	KOH	Thin handle. Approx. 1,24µm/min => ~2h30m for thinning 525µm wafer to < 350µm.	Prepare 1 hour in advance. BHF ethces pecvd nitride faster than SiO2!
5.4	BHF	6-8min	Remove nitride
6.0	Photolithography	KOH mask	Only on wafers that need contact implantation.
6.1	HMDS	Program 4 Time: 30min+10min cooling	
6.2	Resist	1.5um PR2_2 hot plate: 90degC; 60sec	
6.3	Expose in alligner	Time: 7sec Use hard contact 100/10 Separation 30um	
6.4	Development	60s	
6.5	RIE	kar-nano 4min	define alignment marks in device layer
6.6	Acetone stripper	3min + 1min	
7.0	Photolithography	Contact mask	Will mask the test structures under RIE of NW. These structures are to large to be made by EB.
7.1	HMDS	Program 4 Time: 30min+10min cooling	
7.2	Resist	Positive 1.5um PR1_5	Clean nozzle
7.3	Expose in alligner	Time: 7sec Use hard contact 100/10 Separation 30um	Run tests first. The development needs to be checked - small contacts holes, diameter 3um, in the center (100um radius) of the circular resistor. 6sec at airdamp 50% to 10sec at airdamp 40%
7.4	Development	Time: 60sec	
7.5	Plasma Asher	Time: 2min Power: 200W Gas: 225sccm O2 50 N2 Program: 32	Removal of resist residues. Use dummy wafers inbetween wafers.
7.6	Oven Hardbake	Oven 250degC for 30min	
7.7	HF	HF Time: 2 min Rinse: 5 min	Etch holes in oxide where implantations are planned. IMPORTANT: Use testwafers to find the etch rate. Some of the structures are very small (a few um)!
8.0	Implant	High dose Boron implant: Energy:45keV Dose:5E15cm-2 Current:<100uA	To make a good contact to the resistor. This step is NOT necessary to perform on the wafers which have high doping concentration (>5e19).
8.1	Acetone stripper Resist strip	Bath 1: Time: 1min Bath 2: Time: 3min + US	

8	**.**	**2**	Plasma Asher	Time: 30min Power: 1000W Gas: 225 sccm O2 (500) Gas: 10 sccm N2 (5)	
9	**.**	**0**	RCA	NO HF dip!!!!!!! Since there is oxide on the wafers!!!	Cleaning of wafers.
9	**.**	**1**	Anneal	Anneal furnace Nitrogen atmosphere Temperature: 1000 Time: 30 min	In case of boat fuse error: Switch to manual and move boat halfway out, then switch back to automatic.
10	**.**	**0**	Photolithography	AL mask	Will mask the test structures under RIE of NW. These structures are to large to be made by EB.
10	**.**	**1**	HMDS	Program 4 Time: 30min+10min cooling	
10	**.**	**2**	Resist	Track: 1 2.2um PR2_2 hot plate: 90degC; 60sec	
10	**.**	**3**	Expose in alligner	Time: 4.7sec Use hard contact 100/10 Separation 30um	
10	**.**	**4**	Baking	Track 1: Hot plate Recipe: REV_100s Time: 100s Temp: 120degC After baking: Rest for 10min	
10	**.**	**5**	Flood exposure	Time: 35sec	
10	**.**	**6**	Development	70sec	
10	**.**	**7**	Ti/Au Deposition	10 nm Ti and 60 nm Au	Less than 5% wafer coverage
10	**.**	**8**	Lift off	Acetone with ultrasound	approx 10 min, check wafers regularly.
11	**.**	**0**	E-beam lithography	EB Mask	
11	**.**	**1**	Resist	~2ml ZEP520A (positive) 1:1 anisol 5.5%, 2000RPM (accl. 500rpm/s) for 60s gives ~158 nm	Use N2 to clean wafers before spin coating. Make sure that alignment marks are covered with ZEP.
11	**.**	**2**	Baking	Hotplate, 2 min at 160degC	
11	**.**	**3**	E-Beam	200-250µC/cm2, 100KeV, 0.2nA	Should not take more than 1 hour in total.
11	**.**	**4**	Development	1 min 30 sec in ZED-N50, rinse with IPA	Holes where the resistors are, ZEP everywhere else.
11		**5**	Descum	4s RIE. 99sccm N2, 20 sccm O2, 30W, 800mTorr (recipe: mscdscum)	
11	**.**	**6**	Ti/Au Deposition	Alcatel: 10nm Ti and 60nm Au	
11	**.**	**7**	Lift off	s1165 microposit remover with ultrasound, continue until done. Rinse every 2 min and change remover if needed	There should now be Au on all structures. Petri-dish in us-bath.
11	**.**	**8**	RIE	Si-etch (KAR_NANO) through device layer	The Au from step 4 will protect test structures here. Approx. 4min 40sec for 340nm
11	**.**	**9**	Ti/Au removal	Potassium Iodide for 1min 30sek. Rinse in water. RCA1 for 1min 30sek Rinse with water. RCA recipe: Mix H20, NH4OH and H2O2 in 100:25:25 respectively.	Remove metal. RCA1 is done in the RCA fumehood to avoid contamination of the RCA.
12	**.**	**0**	Nitride		LOCOS
12	**.**	**1**	RCA	RCA clean	
12	**.**	**2**	Dry thermal oxide	35nm (20min at dry1000 according to athena)	To avoid swelling of nitride.
12		**3**	Nitride	150nm	To mask during oxidation thinning
13	**.**	**0**	Photolithography	NIT mask	Covers everything but the NWs and the silicon thickness teststructure
13	**.**	**1**	HMDS	Program 4 Time: 30min+10min cooling	
13	**.**	**2**	Resist	Positive 1.5um PR1_5	
13	**.**	**3**	Expose in alligner	Time: 7sec Use hard contact 100/10 Separation 30um	

13	**.**	**4**	Development	Time 60sec	
13	**.**	**5**	RIE	Etch nitride with OH_POLY_A	1200Å has been done in 7min
13	**.**	**6**	RIE	Etch anti-swelling oxide	Can perhaps use same process as in 7.5 or might not be necessary at all (only 35nm oxide)
14	**.**	**0**	Oxidation thinning	Anneal-Bond oven?	
14	**.**	**1**	RCA	RCA clean	
14	**.**	**2**	Oxidation thinning	Recipe depends on final NW thickness. 20min with wet1100 will remove 160nm.	Will thin contacts and teststructures as well
14	**.**	**3**	Nitride etch	Phosphoric acid at 160degC (50Å/min)	RCA clean?
14	**.**	**4**	BHF	Remove oxide from 8.2	
15	**.**	**0**	Oxidation	Anneal-Bond oven	
15	**.**	**1**	Dry oxide	18min in anneal-bond oven at 900C. Total time ~ 3h20m	For good pasivation of NW. Approx. 5-7nm.
15	**.**	**2**	Ellipsometer	Oxide thickness on testwafer	
15	**.**	**3**	TEOS	11min in TEOS LPCVD oven (recipe: TEO	approx. 140nm, total time: ~1h30m + standby
15	**.**	**4**	Filmtek	Oxide thickness on testwafer	
16	**.**	**0**	Photolithography	MET mask	Metalization lift-off Image reversal process
16	**.**	**1**	HMDS	Program 4 Time: 30min+10min cooling	
16	**.**	**2**	Resist	Track: 1 2.2um PR2_2 hot plate: 90degC; 60sec	
16	**.**	**3**	Expose in alligner	Time: 4.7sec Use hard contact 100/10 Separation 30um	
16	**.**	**4**	Baking	Track 1: Hot plate Recipe: REV_100s Time: 100s Temp: 120degC After baking: Rest for 10min	
16	**.**	**5**	Flood exposure	Time: 35sec	
16	**.**	**6**	Development	Time: 70sec	
16	**.**	**7**	BHF	Time: 15sec depending on the oxide thickness	To be sure that there is no oxide in contact holes before deposition of metal.
16	**.**	**8**	Ti/Al deposition	Alcatel/Wordentec Ti Thickness: 100nm Al Thickness:1000nm	1000nm Al for sufficient step-coverage
16	**.**	**9**	Lift off	3min + 20min US	Check wafers every 5 minutes
16	**.**	**10**	Al anneal	Time: 30 min (total: 42 min) Temp: 400degC	anneal400 in the anneal-al oven
17	**.**	**0**	Photolithography	ASE	Include test wafer for ASE process
17	**.**	**1**	HMDS	Program 4 Time: 30min+10min cooling	To dry the wafers
17	**.**	**2**	Resist	Track 2: 9.5um PR9_5 Rest 10min	Clean nozzle
17	**.**	**3**	Expose in alligner	KS Aligner Time: 90s Use hard contact Separation 30um ci2	
17	**.**	**4**	Development	Time: 4min30sec	
17	**.**	**5**	Baking	Hot plate Use REV120: 120degC, time: 100s	
17	**.**	**6**	BHF	Time: depends on BOX thickness	Etch the oxide layer in the ASE trenches
18	**.**	**0**	ASE with HF dip at oxide layer	Selectivity: Si:PR 40:1 Recipe: deepetch cycles:250 (try 180 if 280µm substrate)	Etch approx 300mm down. Run test to determine etch-rate (50µm wide ASE lines => 5-6 µm/m)
18	**.**	**1**	Acetone stripper Resist strip	Bath 1: Time: 1min Bath 2: Time: 3min + US	

I.7 Circular *n*-type piezoresistor

Step			Process	Parameters	Comments
1	.	0	4 Silicon substrate p-type (100)	p-type (100) and n-type (100) 1-20 Ωcm Thickness: 350 μm Double sided polishec	
2	.	0	Ion Implantation	Energy: 30keV Phosphorous dose: 8E13 cm-2	
3	.	0	Photolithography	RIE mask	2 extra test wafers for RIE-depth rate
3	.	1	HF	4 min rinse 5 min	Etch existing oxide and prepare the wafers for photolithography
3	.	2	Resist	Positive 1.5um PR1_5	Clean nozzle
3	.	3	Expose in alligner	Time: 10sec Use hard contact 100/10 Separation 30um	6sec at airdamp 50% to 10sec at airdamp 40%
3	.	4	Development	Time: 60sec	
3	.	5	Plasma Asher	Time: 2min Power: 200W Gas: 225sccm O2 50 N2 Program: 32	Removal of resist residues Had problems with getting all the resist residues off. Run a few tests before putting the wafers into the RIE. Perform a BHF dip before RIE
3	.	6	Baking	Oven 120degC for 25min	
3	.	7	HF	HF dip before RIE. 30 secs rinse 5 min	To obtain a nice surface after RIE
4	.	0	RIE	RIE 2. Recipe: OH_POLYA Depth: 500nm = ca 2 min	Etch of implant layer, to define resistor structures. Run two test wafers and check thickness and uniformity before running til real wafers.
4	.	1	Acetone stripper Resist strip	Bath 1: Time: 1min Bath 2: Time: 3min + US	
4	.	2	7up	Temp: 80degC Time: 10min	Remove resist totally rinse 5min
5	.	0	RCA	RCA clean	
5	.	1	Oxidation and annealing	Recipe: dry1000 Temperature: 1000C Time: 160 min	Include 3 testwafers for use to determine etch rate later.
5	.	2	Filmtek	Oxide thickness on testwafer	Recipe: SiO2-4inches-5points-thin
6	.	0	Photolithography	Sub mask	
6	.	1	HMDS	Program 4 Time: 30min+10min cooling	To dry the wafers
6	.	2	Resist	Positive 2.2um PR2_2	Clean nozzle
6	.	3	Expose in alligner	Time: 10sec Use hard contact 100/10 Separation 30um	6sec at airdamp 50% to 10sec at airdamp 40%
6	.	4	Development	Time: 60sec	
6	.	5	Oven Hardbake	Oven 250degC for 30min	
7	.	0	HF	HF Time: 2min Rinse: 5 min	Etch holes in oxide where implantations are planned.

8	.	0	Implant	High dose Boron implant: Energy:45keV Dose:5E15cm-2 Current:<100uA	To make a good contact to the substrate.
8	.	1	Acetone stripper Resist strip	Bath 1: Time: 1min Bath 2: Time: 3min + US	
8	.	2	Plasma Asher	Time: 30-40min Power: 1000W Gas: 225 sccm O2 (500) Gas: 10 sccm N (5) Program: 37	Make sure all the resist is off.
9	.	3	Filmtek	Check oxide thickness on test some of the wafers	The oxid should still be around 100nm
8	.	4	7up	Temp: 80degC Time: 10min	Remove resist totally rinse 5min
9	.	0	Photolithography	Con mask	
9	.	1	HMDS	Program 4 Time: 30min+10min cooling	To dry the wafers
9	.	2	Resist	Positive 1.5um PR1_5	Clean nozzle
9	.	3	Expose in alligner	Time: 7sec Use hard contact 100/10 Separation 30um	Run tests first. The development needs to be checked - small contacts holes, diameter 3um, in the center (100um radius) of the circular resistor. 6sec at airdamp 50% to 10sec at airdamp 40%
9	.	4	Development	Time: 60sec	
10	.	5	Plasma Asher	Time: 2min Power: 200W Gas: 225sccm O2 50 N2 Program: 32	Removal of resist residues Had problems with getting all the resist residues off. Run a few tests before putting the wafers into the RIE. Perform a BHF dip before RIE
9	.	6	Oven Hardbake	Oven 250degC for 30min	
10	.	0	HF	HF Time: Rinse: 5 min	Etch holes in oxide where implantations are planned. IMPORTANT: Use testwafers to find the etch rate. Some of the structures are very small (a few um)!
11	.	0	Implant	High dose Phosphorous implant: Energy:45keV Dose:5E15cm-2 Current:<100uA	To make a good contact to the resistor.
11	.	1	Acetone stripper Resist strip	Bath 1: Time: 1min Bath 2: Time: 3min + US	
11	.	2	Plasma Asher	Time: 20min Power: 1000W Gas: 225 sccm O2 (500) Gas: 10 sccm CF4 (5) Program: 37	

11	.	3	7up	Temp: 80degC Time: 10min	Remove resist totally rinse 5min
12	.	0	RCA		Cleaning of wafers.
13	.	0	Anneal	Anneal furnace Nitrogen atmosphere Temperature: 1000 Time: 30 min	Annealing the implanted areas.
14	.	0	Photolithography	M80 mask on wafer 1,2,13,14 M20 mask on the rest og the wafers	Mettalization lift-off Image reversal process
14	.	1	HMDS	Program 4 Time: 30min+10min cooling	
14	.	2	Resist	Track: 1 2.2um PR2_2 hot plate: 90degC; 60sec	
14	.	3	Expose in alligner	Time: 4.7sec Use hard contact 100/10 Separation 30um	6sec at airdamp 50% to 10sec at airdamp 40%
14	.	4	Baking	Track 1: Hot plate Recipe: REV_100s Time: 100s Temp: 120degC After baking: Rest for 10min	
14	.	5	Flood exposure	Time: 35sec	
14	.	6	Development	Time: 70sec	
14	.	7	BHF	Time: 15sec	To be sure that there is no oxide in contact holes before deposition of metal.
15	.	0	Ti/Al deposition	Alcatel/Wordentec Ti Thickness: 100nm Al Thickness: 600nm	
15	.	1	Lift off	3min + 20min US	Check wafers every 5 minutes
15	.	2	Plasma Asher	Program 2 Time: 15min	
15	.	3	Al anneal	Time: 15 Temp: 475degC	
16	.	0	Photolithography	ASE	Include test wafer for ASE process
16	.	1	HMDS	Program 4 Time: 30min+10min cooling	To dry the wafers
16	.	2	Resist	Track 2: 9.5um PR9_5 Rest 10min	Clean nozzle
16	.	3	Expose in alligner	KS Aligner Time: 90s Use hard contact Separation 30um ci2	
16	.	4	Development	Time: 4min30sec	
16	.	5	Baking	Hot plate Use REV120: 120degC, time: 100s	
17	.	0	ASE	Selectivity: Si:PR 40:1 Recipe: deepetch cycles:250	Etch approx 300μm down. Run test to determine etch-rate
17	.	1	Acetone stripper Resist strip	Bath 1: Time: 1min Bath 2: Time: 3min + US	
17	.	2	Plasma Asher	Program 2 Time: 15min	

APPENDIX

J Measurements

J.1 *p*-type silicon

T °C	$\pi_{44}(N_A = 1.5 \cdot 10^{17}\ \mathrm{cm}^{-3})$ $10^{-11}\ \mathrm{Pa}^{-1}$	$\pi_{44}(N_A = 2 \cdot 10^{18}\ \mathrm{cm}^{-3})$ $10^{-11}\ \mathrm{Pa}^{-1}$	$\pi_{44}(N_A = 2.2 \cdot 10^{19}\ \mathrm{cm}^{-3})$ $10^{-11}\ \mathrm{Pa}^{-1}$
30	118	110	85
40	113	106	83
50	112	103	82
60	109	101	80
70	107	99	79
80	106	97	77

Table J.1: Measured piezocoefficient π_{44} for uniformly boron doped silicon piezoresistors on SOI substrates.

T °C	$\pi_{44}(N_A = 9 \cdot 10^{17}\ \mathrm{cm}^{-3})$ $10^{-11}\ \mathrm{Pa}^{-1}$	$\pi_{44}(N_A = 9.4 \cdot 10^{18}\ \mathrm{cm}^{-3})$ $10^{-11}\ \mathrm{Pa}^{-1}$	$\pi_{44}(N_A = 4.6 \cdot 10^{19}\ \mathrm{cm}^{-3})$ $10^{-11}\ \mathrm{Pa}^{-1}$
25	119	99	72
35	117	98	71
45	114	95	69
55	110	92	67
65	106	89	66
75	103	85	63
85	97	81	60

Table J.2: Measured piezocoefficient π_{44} for boron doped silicon piezoresistors with a Gaussian doping profile.

J.2 *n*-type silicon

T °C	$\pi_{11}(N_D = 5.1 \cdot 10^{17}\ \mathrm{cm}^{-3})$ $10^{-11}\ \mathrm{Pa}^{-1}$	$\pi_{11}(N_D = 5.1 \cdot 10^{17}\ \mathrm{cm}^{-3})$ $10^{-11}\ \mathrm{Pa}^{-1}$	$\pi_{11}(N_D = 5 \cdot 10^{18}\ \mathrm{cm}^{-3})$ $10^{-11}\ \mathrm{Pa}^{-1}$	$\pi_{11}(N_D = 5 \cdot 10^{18}\ \mathrm{cm}^{-3})$ $10^{-11}\ \mathrm{Pa}^{-1}$
30	-92	-97	-78	-77
40	-92	-94	-75	-74
50	-90	-90	-74	-72
60	-86	-87	-73	-71
70	-84	-84	-72	-70
80	-82	-81	-70	-68

Table J.3: Measured piezocoefficient π_{11} for phosphorus doped silicon piezoresistors with a Gaussian doping profile.

T °C	$\pi_{11}(N_D = 1.3 \cdot 10^{19}\ \mathrm{cm}^{-3})$ $10^{-11}\ \mathrm{Pa}^{-1}$
25	-62
35	-65
45	-61
55	-59
65	-55
75	-52
85	-50

Table J.4: Measured piezocoefficient π_{11} for uniformly phosphorus doped silicon piezoresistors on a SOI substrate.

T °C	$\pi_{12}(N_D = 5.1 \cdot 10^{17}\ \mathrm{cm}^{-3})$ $10^{-11}\ \mathrm{Pa}^{-1}$	$\pi_{12}(N_D = 5.1 \cdot 10^{17}\ \mathrm{cm}^{-3})$ $10^{-11}\ \mathrm{Pa}^{-1}$	$\pi_{12}(N_D = 5 \cdot 10^{18}\ \mathrm{cm}^{-3})$ $10^{-11}\ \mathrm{Pa}^{-1}$	$\pi_{12}(N_D = 5 \cdot 10^{18}\ \mathrm{cm}^{-3})$ $10^{-11}\ \mathrm{Pa}^{-1}$
30	42	43	36	36
40	39	39	34	34
50	40	40	34	33
60	41	40	34	33
70	40	40	33	32
80	40	40	33	32

Table J.5: Measured piezocoefficient π_{12} for phosphorus doped silicon piezoresistors with a Gaussian doping profile.

T °C	$\pi_{12}(N_D = 1.3 \cdot 10^{19}\ \mathrm{cm}^{-3})$ $10^{-11}\ \mathrm{Pa}^{-1}$
25	24
35	21
45	22
55	22
65	21
75	21
85	21

Table J.6: Measured piezocoefficient π_{12} for uniformly phosphorus doped silicon piezoresistors on a SOI substrate.

T °C	$\pi_{44}(N_D = 5.1 \cdot 10^{17}\ \mathrm{cm}^{-3})$ $10^{-11}\ \mathrm{Pa}^{-1}$	$\pi_{44}(N_D = 5.1 \cdot 10^{17}\ \mathrm{cm}^{-3})$ $10^{-11}\ \mathrm{Pa}^{-1}$	$\pi_{44}(N_D = 5 \cdot 10^{18}\ \mathrm{cm}^{-3})$ $10^{-11}\ \mathrm{Pa}^{-1}$	$\pi_{44}(N_D = 5 \cdot 10^{18}\ \mathrm{cm}^{-3})$ $10^{-11}\ \mathrm{Pa}^{-1}$
30	-12	-11	-12	-11
40	-13	-7	-11	-11
50	-12	-11	-11	-11
60	-13	-12	-12	-11
70	-13	-12	-12	-11
80	-11	-10	-12	-11

Table J.7: Measured piezocoefficient π_{44} for phosphorus doped silicon piezoresistors with a Gaussian doping profile.

J.3 Strained *p*-type silicon and silicon germanium

T °C	$\pi_{44}(\mathrm{Si}_{\epsilon=0})$ 10^{-11} Pa^{-1}	$\pi_{66}(\mathrm{Si}_{\epsilon=0.002})$ 10^{-11} Pa^{-1}	$\pi_{66}(\mathrm{Si}_{\epsilon=0.004})$ 10^{-11} Pa^{-1}
30	93	93	69
47	87	89	68
64	81	85	67
81	76	82	65

Table J.8: Measured π_{66} piezocoefficient for MBE grown silicon and tensile strained silicon at a doping concentration of $N_A = 3 \cdot 10^{18}$ cm^{-3}.

N_A cm^{-3}	π_{44} Si Pa^{-1}	π_{66} $\mathrm{Si_{0.9}Ge_{0.1}}$ Pa^{-1}
$1.6 \cdot 10^{18}$	103	136
$1.7 \cdot 10^{19}$	81	86.8

Table J.9: Measurements of the piezocoefficient π_{44} in Si and the piezocoefficient π_{66} in compressive strained $\mathrm{Si_{0.9}Ge_{0.1}}$ ($\epsilon = -0.004$).

J.4 *p*-type silicon nanowires

N_A cm^{-3}	t nm	w nm	π_{44} 10^{-11} Pa^{-1}
$1.5 \cdot 10^{17}$	340	-	124
$1.5 \cdot 10^{17}$	340	320	135
$1.5 \cdot 10^{17}$	340	280	165
$1.5 \cdot 10^{17}$	340	280	163
$1.5 \cdot 10^{17}$	340	340	170
$1.5 \cdot 10^{17}$	340	210	138
$1.5 \cdot 10^{17}$	340	160	198
$1.5 \cdot 10^{17}$	340	140	180
$1.5 \cdot 10^{17}$	340	140	212
$1.5 \cdot 10^{17}$	200	140	910
$1.2 \cdot 10^{20}$	340	-	48
$1.2 \cdot 10^{20}$	340	370	52
$1.2 \cdot 10^{20}$	340	370	53
$1.2 \cdot 10^{20}$	340	280	54
$1.2 \cdot 10^{20}$	340	280	42
$1.2 \cdot 10^{20}$	340	280	41
$1.2 \cdot 10^{20}$	340	160	50
$1.2 \cdot 10^{20}$	340	160	48
$1.2 \cdot 10^{20}$	340	160	48
$1.2 \cdot 10^{20}$	340	160	47
$1.2 \cdot 10^{20}$	340	160	27
$1.2 \cdot 10^{20}$	340	110	40
$1.2 \cdot 10^{20}$	340	110	40
$1.2 \cdot 10^{20}$	340	60	7
$1.2 \cdot 10^{20}$	340	60	1
$1.2 \cdot 10^{20}$	340	60	1
$1.2 \cdot 10^{20}$	340	60	0

Table J.10: Measurements of the piezocoefficient π_{44} in boron doped silicon nanowires with thickness t and width w. The reference measurements on micrometer sized piezoresistors are identified by "-" in the w column.

t nm	w nm	π_{44} 10^{-11} Pa^{-1}
340	-	18
340	330	20
340	225	21
340	150	24
340	100	25

Table J.11: Measurements of the piezocoefficient in boron doped polysilicon nanowires with thickness t and width w. The reference measurements on micrometer sized piezoresistors are identified by "-" in the w column. The nanowires all have the resistivity $\rho = 0.15$ Ωcm.