High Performance Low Cost Digitally Controlled Power Conversion Technology

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Publication date:
2008

Document Version
Publisher's PDF, also known as Version of record

Technical University of Denmark

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Innovation PhD thesis, December 2007

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1 Abstract

Digital control of switch-mode power supplies and converters has within the last decade evolved from being an academic subject to an emerging market in the power electronics industry. This development has been pushed mainly by the computer industry that is looking towards digital power management in order to reduce the power consumption of servers and datacenters.

The work presented in this thesis includes digital control methods for switch-mode converters implemented in microcontrollers, digital signal controllers and field programmable gate arrays.

Microcontrollers are cheap devices that can be used for real-time control of switch-mode converters. Software design in the assembly language of the microcontroller is important because of the limited resources of the microcontroller. Microcontrollers are best suited for power electronics applications with low bandwidth requirements because the execution time of the software algorithm that realises the digital control law will constitute a considerable delay in the control loop.

Digital signal controllers are powerful devices capable of performing arithmetic functions much faster than a microcontroller can. Digital signal controllers are well suited for digital control schemes involving multiple control loops such as digital control of a switch-mode power supply with several converter stages.

Customised digital control solutions implemented in application specific integrated circuits are the best solution for high bandwidth digital control of non-isolated DC-DC converters. A customised digital control solution for a voltage mode control scheme should include a digital pulse width modulator which can generate a pulse width modulated signal with high switching frequency and high resolution, a digital compensator with a short execution time and an analogue to digital converter with a short sampling time.

A digital self-oscillating modulator is proposed in the present thesis. The modulator is a free-running modulator which operates without an external carrier signal.

Customised digital control solutions offers the best performance for non-isolated DC-DC converters. The best digital control solution presented in this thesis, which was implemented with the digital self-oscillating modulator, performs comparable to common analogue control IC solutions. It is however possible to achieve an even better performance with an analogue control circuit built with separate analogue components.

2 Resumé på dansk

Digital regulering af switch-mode strømforsyninger og konvertere har indenfor de sidste ti år udviklet sig fra at være et videnskabeligt emne til et spirende marked i effektelektronikindustrien. Denne udvikling er hovedsageligt blevet skabt af computer-industrien, der ser digital power management som en måde at reducere strømforbruget i servere og datacentre.

Arbejdet, der præsenteres i denne afhandling, omhandler digitale reguleringsmetoder for switch-mode konvertere implementeret med microcontrollere, digitale signal controllere og field programmable gate arrays.

Microcontrollere er billige enheder, som kan benyttes til realtids regulering af switch-mode konvertere. Softwaredesign i microcontrollerens eget assemblersprog er vigtigt på grund af microcontrollerens begrænsede ressourcer. Microcontrollere er bedst egnede til effektelektronikapplikationer med behov for lav båndbredde, fordi eksekveringstiden for software-algoritmen der realiserer den digitale regulering, vil udgøre en betragtelig forsinkelse i reguleringssløjfen.

Digitale signal controllere er hurtige enheder, som er i stand til at udføre aritmetiske beregninger hurtigere end en microcontroller. Digitale signal controllere er velegnede til reguleringssystemer med adskillige reguleringssløjfer såsom digital regulering af en switch-mode strømforsyning med flere konvertertrin.

Specielt udviklede digitale reguleringssystemer implementeret i 'application specific integrated circuits' er den bedste løsning til digital regulering af uisolerede DC-DC konvertere med høj båndbredde. Et specielt udviklet digitalt reguleringssystem med spændingsstyring bør omfatte en digital pulsbredde modulator med høj opløsning, en digital kompensator med kort eksekveringstid og en analog til digital konverter med kort måletid.

En digital selvsvingende modulator bliver introduceret i denne afhandling. Modulatoren er en fritløbende modulator, som fungerer uden et eksternt bærebølge signal.

Specielt udviklede digitale reguleringssystemer leverer den bedst mulige ydeevne til DC-DC konvertere. Det bedste digitale reguleringssytem beskrevet i denne afhandling, som er implementeret med en digital selvsvingende modulator, har en ydelse, der er sammenlignelig med almindelige analoge IC-løsninger. Det er imidlertid muligt at opnå en endnu bedre ydelse med et analogt reguleringssystem opbygget med separate komponenter.

3 Contents

4 Acknowledgements

The present PhD thesis could never have been written without the support of my family and my colleagues at the Technical University of Denmark.

My mother deserves the place of honour because she has always patiently listened to me complain about my technical and personal problems. I want to express my gratitude for her support and belief in me through good and hard times. I also want to thank my sister for always being there to discuss my problems and to tell me that I was not the only PhD candidate who doubted if he was capable of achieving the PhD degree.

I want to thank my supervisor Professor Michael Andersen for giving me the possibility to pursue the PhD degree as a member of the Power Electronics Group at the Technical University of Denmark and his constant support and help. I would likewise like to thank the Technical University of Denmark for the Innovation PhD scholarship that has funded my studies.

Industrial PhD Mikkel Høyerby and I have had many interesting discussions about both analogue and digital control and power electronics in general. These discussions have been a great inspiration and help to me and I want to express my appreciation to Mikkel Høyerby.

I would like to thank my other colleagues in the Power Electronics Group for creating a pleasant working environment and for their readiness to be of help to me at all times.

5 List of abbreviations

ADC	Analogue to Digital Converter
AIM	Astable Integrating Modulator
ALU	Arithmetic Logic Unit
ASIC	Application Specific Integrated Circuit
BOM	Bill of Materials
CMC	Current Mode Control
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
D-FF	Data Flip-Flop
DAC	Digital to Analogue Converter
DLL	Delay Locked Loop
DPWM	Digital Pulse Width Modulator
DSC	Digital Signal Controller
DSP	Digital Signal Processor
FIFO	First-In First-Out
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
IC	Integrated Circuit
IIR	Infinite Impulse Response
ISR	Interrupt Service Routine
KSPS	Kilo-Samples-Per-Second
LTI	Linear Time Invariant
MAC	Multiplier/Accumulator
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSPS	Mega-Samples-Per-Second
OCC	One Cycle Control
PFC	Power Factor Correction
PID	Proportional-Integral-Derivative
PLL	Phase Locked Loop
PWM	Pulse Width Modulation

ROM	Read Only Memory
SAR	Successive Approximation ADC
SMPS	Switch-Mode Power Supply
TDM	Time Division Multiplexing
UPS	Uninterruptible Power Supplies
VCO	Voltage Controlled Oscillator
VMC	Voltage Mode Control
VRM	Voltage Regulator Module

6 Introduction

Digital control of power electronics is a very broad definition which covers subjects ranging from the control of a non-isolated Buck converter delivering a few watts of power to the control of an inverter in a 5 Megawatt wind turbine. The specifications and performance criteria are very different for the Buck converter and the inverter and it is therefore impossible to make a general definition of what is meant by high performance and low cost.

The purpose of this thesis is to investigate digital control solutions for switch-mode power converters in the power range from 10W up to 1kW. High performance is in thesis defined as accurate control of the output voltage and high control loop bandwidth. The digital control schemes presented in this thesis are the results of three years of research of the PhD project entitled “High Performance Low Cost Digitally Controlled Power Conversion Technology”. The main body of the work relates to digital control of non-isolated DC-DC converters, but experiments within digital control of AC-DC converters have also been carried out.

The PhD project has been part of the Innovation PhD programme at the Technical University of Denmark which is new programme that has been started as an experiment. The purpose of the Innovation PhD programme is to educate candidates with a scientific PhD degree and knowledge of high-tech innovation and the business aspects of their area of research.

The work towards the Innovation PhD degree has encompassed market analysis of the power electronics market and specifically the market for digital control ICs. The market analysis has been used to write a business plan for a start-up company based on one of the ideas generated during the three year PhD project.

Because the project has been an Innovation PhD project the focus of the research has been on development of practical hardware and software solutions rather than theoretical analysis of the interaction between the digital control hardware and the switch-mode converter.

The advancements made in digital control of switch-mode power converters over the last few years have primarily been driven by the needs of the computer industry. The power

consumption of both PCs and servers has increased as a result of the development of faster CPUs etc. The need for digital power management to supervise and control the power supplies in a server has given a boost to the research in high performance digital control methods for both DC/DC and AC/DC converters. Digital control of switch-mode power supplies and converters is not directly related to digital power management but it makes sense to combine the two in new products if digital power management is a requirement.

Analogue control of switch-mode converters has been developed over the last 35-40 years and has reached a very high level of performance. At the beginning of the PhD project existing digital control methods could not deliver performance that was anywhere near as good as the performance of analogue control methods. One of the aims of the project was therefore to come up with a new digital control method that was capable of delivering performance equal to the performance of state-of-the-art analogue control and at a competitive price.

The biggest difference between analogue and digital control is that there is almost no delay in the analogue control loop. Digital control implementations have inherent delays in the analogue to digital converter that is sampling the output voltage and/or the inductor current and the digital controller core performing the calculations necessary to compute the duty cycle of the PWM signal controlling the converter. There will always be a delay regardless of the choice of hardware for the digital controller, but the choice of hardware has a huge impact on how long the delay is. The final converter performance is strongly determined by the delay as will be shown throughout the thesis.

The PhD project has included work with low cost microcontrollers, Digital Signal Controllers (DSCs) and Field Programmable Gate Arrays (FPGAs).

In the beginning of the three year period the work focussed on digital control with microcontrollers, specifically 8-bit microcontrollers with a small number of I/O ports and an internal bus-width of 8 bit. The reason for choosing 8-bit microcontrollers as the subject of research was that academic research up to the year 2004 had for the most part been focussed on DSC implementations and it was thought that microcontrollers might represent a viable low cost alternative.

In order to obtain high performance digital control the software algorithms performing the control law was optimized with regards to minimizing the execution time of the algorithm. Experiments were performed with pure voltage mode control and mixed signal

control schemes which combines the microcontroller with analogue control circuitry to improve system performance.

The next step was to investigate the limitations of state-of-the-art DSCs. It was quickly found that even though a DSC can perform computations faster than a microcontroller due to higher clock frequency and an on-chip hardware multiplier/accumulator module it is still not fast enough to deliver control loop performance comparable to existing analogue solutions.

Customised digital control solutions implemented in an FPGA have been developed and tested in the second half of the PhD project. The work was divided into the development of VHDL implementations of a digital PID compensator with short computation time and low complexity and a complete controller implementation with a digital PWM modulator and the digital compensator. The author of this thesis and his supervisor has proposed a new Digital Self-Oscillating Modulator (DiSOM) that has been filed as a patent application.

The thesis describes some general properties of the digital controls method that have been researched in the PhD project. The thesis is supported by eleven appendices which is to be considered as an integral part of the thesis. The appendices comprise a number of papers published at international conferences and the patent application previously mentioned. The appendices describe some of the details of the different digital control methods that have been researched. It is recommended that the reader reads the appendices that are mentioned in a chapter of the thesis before the reading the chapter. Chapter 14 on page 105 shows which appendices should be read before each chapter.

7 State-of-the-art Analysis

Digital control technology for switch-mode power converters has evolved from mainly a research topic at universities to play an increasingly important role in the electronics industry. The progress achieved through university research and product development in the industry is indeed impressing and has shown that there definitely is a future for digital control of switch-mode power supplies.

The purpose of this chapter is to give an overview of the most important technologies that have been described in recently published scientific papers, patent applications and patents. There will also be some references to datasheets and user manual for specific products to highlight which technologies have actually made it through to the power electronics market.

The State-of-the-art analysis is divided into three main subjects, digital Pulse Width Modulators (DPWMs), digital control methods for power converters and digital hardware implementations.

The DPWM has proven to be of great importance in the design of digitally controlled power converters both in terms of the accuracy and speed of the digital controller.

The digital control methods will be extended to include mixed signal controllers since they incorporate some digital control elements and in some cases present very promising results.

The purpose of the State-of-the-art analysis is to describe different solutions, but not to compare them. The analysis will to some extent try to pinpoint the advantages and disadvantages of each solution, but the description be somewhat biased by the perception of the author since the specifics of the practical implementations are not always known.

7.1 Digital PWM modulators

Digital PWM modulation is extremely important in modern digital control techniques for switch-mode power converters and especially DC/DC converters. The tendency is that the switching frequency used in power converters is increasing in order to reduce the size of capacitors and magnetic components in the converter. The use of higher switching frequencies has been made possible by advances made in MOSFET technology over the last decade. It is therefore important to be able to generate PWM signals with high switching frequencies digitally in order for digital control to be a viable alternative to analogue control.

The most common DPWM is based on a counter clocked by a high frequency digital clock and a digital comparator. Fig. 7-1 shows the basic operation of a counter based PWM modulator. The counter based DPWM emulates a typical analogue PWM circuit where a triangular or sawtooth voltage is compared to a control signal that determines the duty cycle. The sawtooth voltage is emulated by a counter, which counts from zero to a preset value, which determines the PWM frequency, f_{sw}. If the counter value is smaller than the compare value, which can be changed by the digital control law such as a digital PID compensator, the PWM output is high, and if the counter value is larger than or equal to the compare value the PWM output is low.

The described implementation of a counter based DPWM generator is commonly used in a large number of microcontrollers and Digital Signal Controllers (DSCs) available from a number of manufacturers.

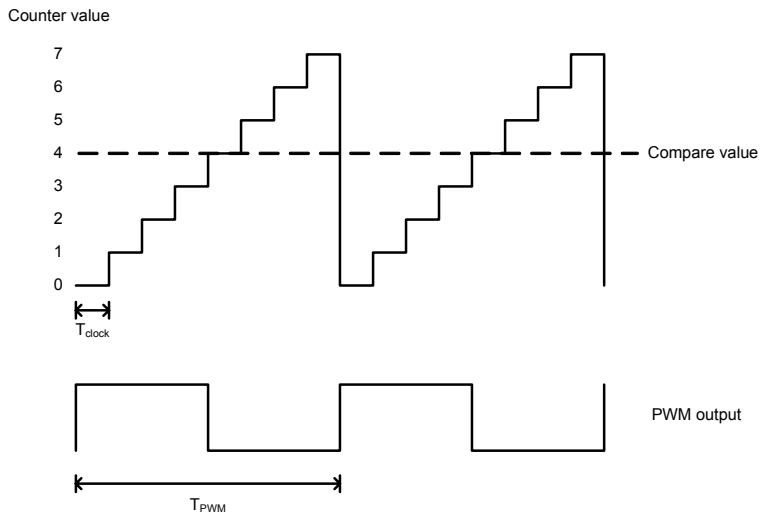


Fig. 7-1 Operation of a basic counter based DPWM

The DPWM modulator can be considered as a 1-bit D/A converter, which converts the digital control signal into an analogue signal. The effective resolution of the DPWM is determined by the clock frequency and the PWM frequency (see equation 7.1).

$$\text{DPWM resolution} = \log_2\left(\frac{f_{sw}}{f_{clock}}\right) \tag{7.1}$$

The DPWM resolution is of great importance in modern switch-mode converters, because the demands for high accuracy of the output voltage regulation are increasing. The

phenomena of *limit cycling* on the converter output voltage occurs if the DPWM resolution is too low [1,2]. Fig. 7-2 shows an illustration of what limit cycling is. Limit cycling results in a periodic oscillation on the output voltage at a frequency lower than the switching frequency.

In most modern day applications the basic counter based DPWM will not have the required resolution unless it is clocked at several GHz, which is virtually impossible to realise. If for instance a 1 MHz PWM signal with 12 bits of resolution were to be generated by a counter based DPWM block, the clock frequency would have to be 4.096 GHz.

One of the main areas of research within digital control of switch-mode converters in the last 6-7 years has been how to improve the DPWM resolution without operating at clock frequencies in the GHz range. In the following sub-sections, the most important methods to improve DPWM resolution will be briefly described.

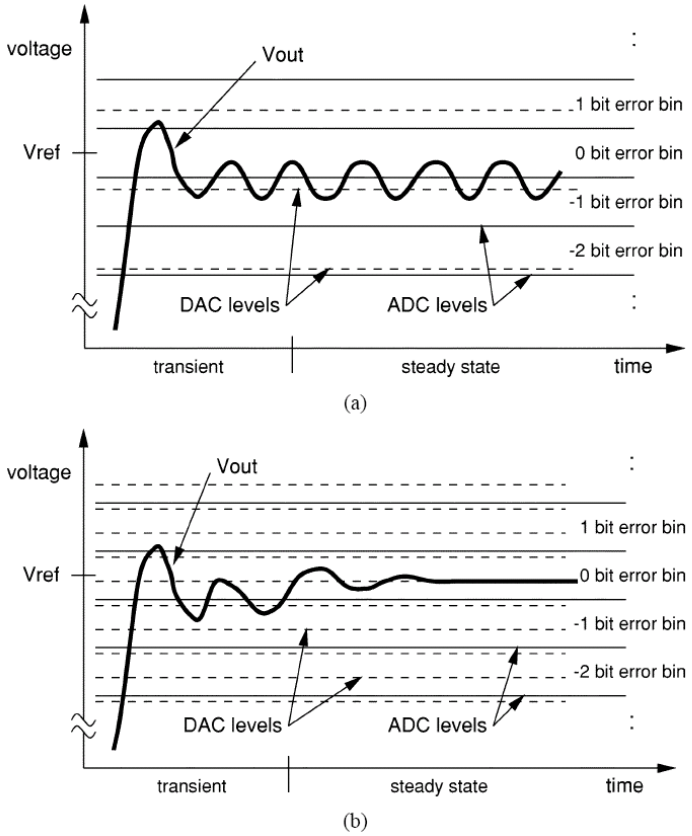


Fig. 7-2 Illustration of limit cycling in a digitally controlled switch-mode converter (a) DPWM resolution is lower than ADC resolution resulting in limit cycling on the output voltage (b) DPWM resolution is higher than ADC resolution resulting in a steady output voltage [1]

7.1.1 Dithering

The simplest way to increase the effective resolution of a counter based DPWM is by adding dithering to the duty cycle command for the counter based DPWM. The principle of dithering (see Fig. 7-3) is to change the duty cycle by the smallest possible change, i.e.

by changing the least significant bit (LSB) of the duty cycle command to the DPWM modulator in a periodic manner. It is thereby possible to set the average duty cycle of the PWM signal in increments smaller than the change achieved by changing the LSB of the duty cycle command. By letting the dithering algorithm run over several PWM periods the effective resolution of the dithered PWM signal can be increased. If for example the PWM resolution must be increased by three bits the dithering algorithm would run over eight PWM periods. The dithering process will add sub-harmonic ripple currents and voltages in the switch-mode converter during steady state conditions, because the duty cycle command is periodically changed at a frequency lower than the switching frequency. The extra ripple voltage added by the dithering process will generally be smaller than the limit cycling oscillation that would occur without the use of dithering.

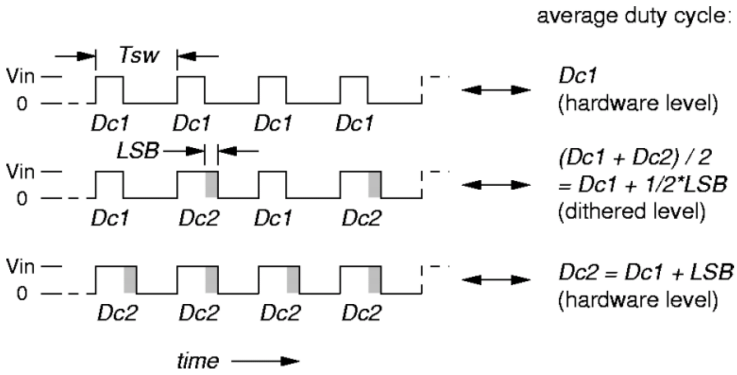


Fig. 7-3 Principle of dithering [1]

The disadvantage of the dithering process is that the sub-harmonic ripple introduced at the output voltage increases to an unacceptable level if the increase in resolution added by dithering is larger than 4-5 bits. The sub-harmonic ripple voltage will for a large increase in effective resolution get so large that the A/D converter (ADC) that samples the output will register the ripple and cause limit cycling in spite of the dithering process.

There are several ways of implementing dithering in a digital controller IC, which will not be described in detail. Dithering is included in several digital control ICs that are available on the market at the time this thesis was written [3-5].

7.1.2 Hybrid DPWM modulators

A DPWM modulator based on a ring oscillator consisting of a number of delay elements, e.g. an inverter cell, can be implemented without the use of an external clock signal. The ring oscillator generates the PWM frequency automatically, and the minimum time step that the duty cycle can be adjusted in is equal to the propagation delay of one

delay element. The disadvantage of the ring oscillator DPWM module is that it requires a large number of delay elements, thus requiring a large chip area in an IC implementation.

The hybrid DPWM modulator is basically composed of a small ring oscillator and a counter, which is clocked by the ring oscillator [6]. The oscillating frequency of the ring oscillator is higher than the switching frequency, and the counter is used to divide the oscillating frequency down to the switching frequency. The ratio between the oscillating and switching frequencies is typically low and the counter has a low number of bits. The counter sets the PWM frequency and determines the duty cycle in coarse steps. The exact point of transition from high to low for the duty cycle is determined by the delay line of the ring oscillator.

Fig. 7-4 shows a block diagram of a 4-bit hybrid DPWM modulator. The ring oscillator is composed of the four D Flip-Flops (D-FF) at the top of the block diagram. Comparator 2 is used to set the PWM frequency by dividing the system clock, i.e. the signal Q_3 from the ring oscillator, by four. The output of comparator 2 in conjunction with Q_3 is used to set PWM output on the S-R latch. Comparator 1 and the multiplexer (MUX) determine the duty cycle, where comparator 1 compares the counter output with the two most significant bits of the duty cycle command, d[3:2]. The two least significant bits of the duty cycle command, d[1:0], selects one of the four inputs to the MUX (Q_0, Q_1, Q_2 or Q_3) as the second input to the AND gate controlling the reset input of the S-R latch.

Since the four Q signals are shifted in time because of the propagation delay of the D-FFs it is possible to control the negative transition of the PWM output in steps that are equal to one quarter of the period time of the system clock. The delay line can be extended to a larger number of delays to be able to adjust the duty cycle in finer time steps, thereby increasing the effective resolution. Reference 6 reports a delay line based DPWM modulator with a switching frequency of 1 MHz with a ring oscillator frequency of 8 MHz. The counter is a 3-bit counter and the delay line adds 5 bits of resolution to make the effective DPWM resolution 8 bits.

The duty cycle can be adjusted in time steps equal to the propagation delay of one D-FF. In the basic configuration shown in Fig. 7-4 the propagation delay needs to be exactly equal to one fourth of the time period of the system clock. Otherwise the relationship between the duty cycle and the duty cycle command will not be a linear function.

Mass production of the delay line based DPWM will not allow tuning of the propagation delay to an acceptable level. CMOS process variations and temperature dependency is unavoidable and the design of the DPWM modulator will not meet the requirements for

linearity in its basic form. To achieve linear operation a digital delay locked loop (DLL) can be added, which tunes the number of delay elements in the delay line [7]. The effective resolution of the DPWM will in this case vary with temperature and CMOS process variations, but the overall performance will most likely be better than for the basic delay line based DPWM.

If several PWM signals have to be generated by delay line based DPWM modules, the CMOS area that will be taken up by the DPWM block will be quite large. The reason is that it is necessary to have a delay line for each PWM signal that is generated. The number of multiplexers and comparators will also increase. Reference 8 proposes a structure in which one multiplexer and one comparator is time shared between several PWM modules. The idea is that it will always be known, which PWM signal is the next to change state, and the multiplexer and comparator can be assigned to the correct PWM output by a simple logic block. The idea is intended for implementation in a Field Programmable Gate Array (FPGA), but it is equally applicable to IC integration.

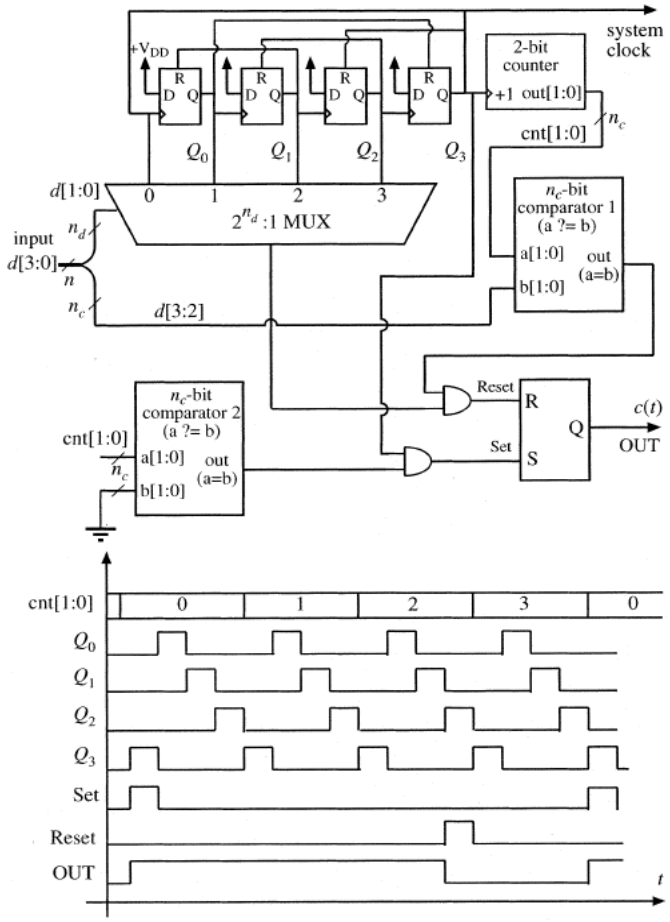


Fig. 7-4 Schematic and timing diagram for a delay line based DPWM modulator [6]

Texas Instruments have introduced a high resolution DPWM module in several Digital Signal Controllers (DSCs) and Application Specific Integrated Circuit (ASIC) products that is similar to the hybrid DPWM [9]. The Texas Instruments DPWM module runs of an external clock, which is typically 100 MHz. A delay line that receives the clock signal as input is used to increase the DPWM resolution in the same manner as in the hybrid DPWM. The number of delay elements in the delay line can be tuned so that the total delay matches one clock period in order to achieve linear operation of the DPWM. The delay line is not used as a ring oscillator, but it simply generates a number of positive edges shifted in time relative to the clock pulse.

Extensions of the hybrid DPWM modulator for multiphase interleaved Buck converters have been proposed in reference [10] and [11]. The main purpose of the proposed multiphase hybrid DPWMs is to simplify the design in order to reduce the complexity and implementation size of the modulator. Both of the proposed multiphase modulators use time sharing of a single delay line for all PWM outputs instead of having one delay line for each output. The disadvantage of the proposed modulators is that the duty cycle of each phase will be the same, which does not enable the digital control scheme to include active current sharing.

7.1.3 Sigma-Delta DPWM modulators

Sigma-Delta modulator techniques have been used in both Analogue to Digital and Digital to Analogue converters and are well described in literature. In audio applications the Sigma-Delta modulator relies on over-sampling and extensive digital filtering to achieve very high DPWM resolution and a large signal-to-noise ratio. In practical applications of digital control of DC/DC converters both price and power consumption is of importance, and a simpler implementation of the Sigma-Delta modulator is necessary.

Fig. 7-5 shows an example of a Sigma-Delta DPWM modulator designed for low power portable applications. The modulator consists of a 3-bit counter based DPWM and a digital filter that turns a 9-bit duty cycle command into a 3-bit command for the counter based DPWM. The digital filter shapes the 3-bit signal in such a way that the average value is equal to the 9-bit input signal. The filter will generate some high frequency noise with a wide spectrum, which the DC/DC converter output filter will have to attenuate so as not to disturb the load on the output of the converter. The noise power spectrum will be attenuated at low frequencies and increase at higher frequencies. The noise power

spectrum is dependent on the switching frequency and the update rate of the duty cycle command *d[n]*.

The Sigma-Delta DPWM modulator works best for switching frequencies in the MHz range, because the noise power will be low at lower frequencies, thereby allowing the DC/DC converter output filter to effectively attenuate the quantisation noise generated by the Sigma-Delta modulator.

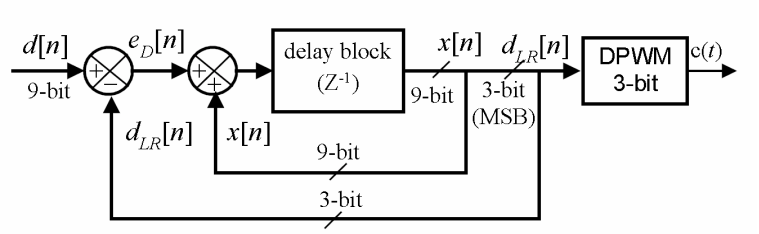


Fig. 7-5 Block diagram of multi-bit Sigma-Delta DPWM [12]

The effective resolution is a function of the number of PWM periods over which the digital filter averages the 3-bit duty cycle command for the counter based DPWM and of the resolution of the counter based DPWM.

One important disadvantage of the Sigma-Delta modulator is that it requires a number of PWM periods to average the duty cycle command in order to achieve high DPWM resolution. It will be necessary to sample the output voltage with a sampling frequency that is an integer multiple of the PWM frequency to take advantage of the Sigma-Delta modulator's high resolution. The lower sampling frequency limits the achievable control loop bandwidth thereby resulting in a slower dynamic response of the DC-DC converter than for other DPWM technologies. Reference 12 therefore proposes a dual sampling compensator that samples with a low sampling frequency during steady state conditions and increases the sampling frequency if the error signal exceeds a certain preset limit.

Sigma-Delta modulators for DC-DC converters have been proposed in a number of scientific papers [12,13], but at the time of writing the present thesis no commercial controller ICs utilize the technology.

7.1.4 Other DPWM techniques

Apart from the three main types of digital PWM modulators with high duty cycle resolution several other DPWM modulators have been proposed in scientific papers [14-16]. Common for these solutions are that they are the work of researchers from a single

university and that they have not yet been used in the industry. For this reason the different solutions will only be briefly described.

Reference 14 proposes a DPWM modulator with either fixed ON- or OFF-time. In the case of fixed ON-time the PWM resolution is increased for small duty cycle values and converges towards the resolution of a basic counter based DPWM for duty cycles close to unity. This is a desirable characteristic in Voltage Regulator Modules (VRM) that typically operate at a duty cycle around 0.1. In some applications it can be a disadvantage that the switching frequency varies with duty cycle, but in Point of Load Converters (POLs) and VRMs it is generally acceptable because the duty cycle variations are small during steady state operation. Reference 14 describes a combination of a constant frequency/constant ON-time modulator that achieves improved resolution with only small variations in the switching frequency. This type of modulator can be used if constant switching frequency is an important design parameter.

In reference 15 the digital carrier signal is generated with two high frequency clock signals operating with two different frequencies. The modulation technique is double-edged PWM modulation where the two slopes of the digital carrier signal are clocked by the two different clock signals. Thus, the positive slope is controlled by the first clock and the negative slope by the second clock. The PWM resolution is in this case determined by the difference in frequency between the two clocks. The smaller the difference in frequency between the two clock signals the higher the DPWM resolution. The authors of reference 15 propose that one clock signal is generated by a crystal oscillator and the second clock signal is generated by Phase Locked Loop (PLL) clocked by the crystal oscillator.

Reference 16 presents a way to increase PWM resolution in digital control systems implemented in an FPGA. The idea is to utilize the DLL that is included in many modern FPGAs. The DLL is in many cases able to create phase shifted versions of the internal clock, typically shifted by 90, 180 and 270 degrees. The additional transitions of the phase shifted clocks can be used to control the transition of the PWM signal thereby increasing the PWM resolution. The practical implementation is similar to the implementation of the hybrid DPWM where a counter is used to control the coarse positioning of the PWM transitions and the delay line is used to control the exact position of the edge. In this case a

digital circuit utilizing the phase shifted clock signals generated by the PLL replaces the delay line.

In section 7.1.2 two hybrid DPWM modulators for interleaved converters were briefly mentioned. These methods only applied to hybrid DPWM modulators, but other DPWM schemes can also be used to control interleaved converters. The simplest method for generating interleaved PWM signals is to generate one master signal. That signal is delayed by a fraction of the PWM period to generate the phase shifted PWM signal. One way to generate the delay is to configure a First-In-First-Out (FIFO) register as a ring buffer (see Fig. 7-6a). The ring buffer has two pointers; one to point to the address where new data is written and one to point to the address where the data is read. The FIFO is clocked by a high frequency clock and shifts the contents of the ring buffer one position for every clock cycle. By adjusting the read address of the ring buffer it is possible to adjust the delay of the PWM signal from input to output. Reference 17 proposes to cascade a number of FIFO phase-shifters (see Fig. 7-6b) to generate multiple phase shifted signals. The delay of each phase-shifter should be equal to 360/*n* degrees, where the integer *n* is the number of phases in the interleaved converter. The practical implementation in ref. 17 utilizes a FIFO IC from Texas Instruments and the control loop can be either analogue or digital because it simply feeds a PWM signal to the FIFO phase-shifters.

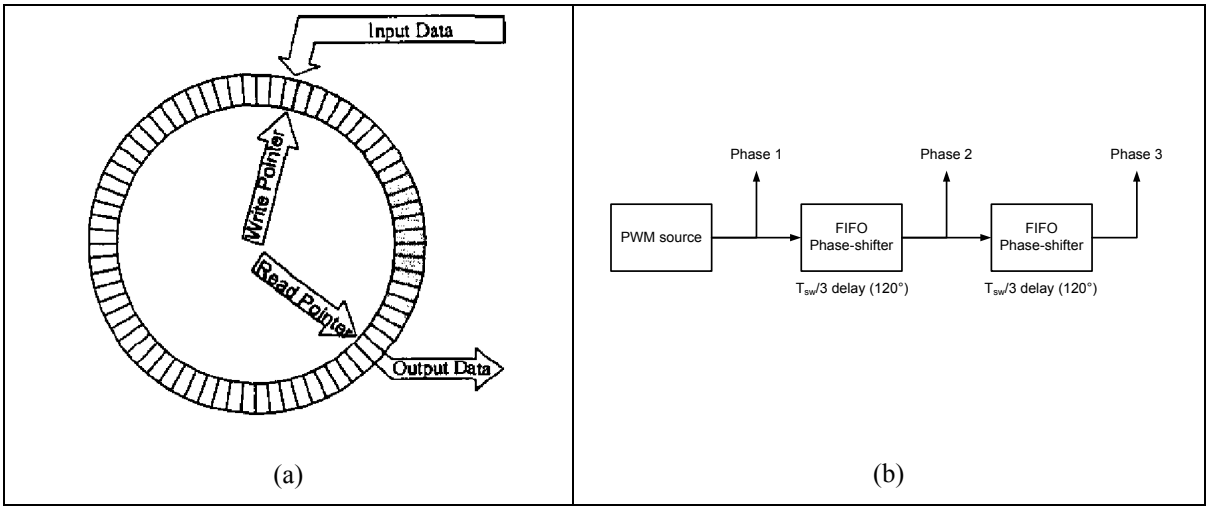


Fig. 7-6 FIFO based multiphase PWM generation [17]

(a) FIFO configured as a ring buffer (b) 3-phase PWM module with FIFO Phase-shifters

The use of FIFOs to generate phase shifted PWM signals from a single signal is straightforward but it does present a drawback in modern power electronics namely that

each phase gets exactly the same duty cycle. It is increasingly important to be able make slight adjustments in the duty cycle of each phase in an interleaved VRM module to ensure symmetrical phase currents. Variations in MOSFET ON resistance, inductor series resistance and different PCB layout for each phase can result in asymmetrical phase currents in an interleaved Buck converter. To achieve symmetrical current sharing it is necessary to adjust the duty cycle of each phase individually, which is not possible with the FIFO design proposed in reference 17.

7.2 Digital control methods

Digital control for a switch-mode power converter can be implemented in a number of different ways. The last five years of academic research have covered a large number of different digital control methods and it will not be possible to describe every solution in detail here. The subject has therefore been divided into four main groups which will be described generally in addition to one or two examples of practical implementations for each group.

7.2.1 Mixed Signal Control

As the name suggests mixed signal control is not a purely digital control method. It involves combining analogue and digital control methods, typically with the purpose of reducing the complexity of the digital control system but also in order to improve system performance. The main idea is to remove the generation of the PWM signal from the digital domain and into the analogue domain, thereby removing the problem of limit cycling encountered in digital PWM generation due to poor resolution in the DPWM modulator.

The most common mixed signal control method is a dual loop control system involving an analogue current control loop and a digital voltage control loop [18-20]. The current loop controls the inductor current in a typical switch-mode power converter, and it can be implemented as peak current mode control (see Fig. 7-7) [18], average current mode control [19] or some other current control scheme, e.g. hysteretic current mode control or one cycle control (OCC) [20].

The benefit of implementing the current control loop with analogue circuitry is reduced limit cycling on the output voltage and a more simple digital control implementation. The problem of limit cycling is reduced because the analogue current loop theoretically has infinite PWM resolution as it has no clock to determine when the PWM signal can change from high to low or vice versa. The digital voltage loop is sampling the output voltage with

an ADC and is calculating a reference value for the current loop. The current reference is converted into an analogue reference voltage by a Digital to Aanalogue Converter (DAC). The voltage loop will typically have a relatively simple control law such as a digital PID compensator.

Because the digital part of the controller only needs to sample the output voltage to implement a current mode control scheme it is possible to use a cheap A/D converter. The number of calculations that needs to be performed by the digital controller is also reduced since the current loop is analogue instead of digital.

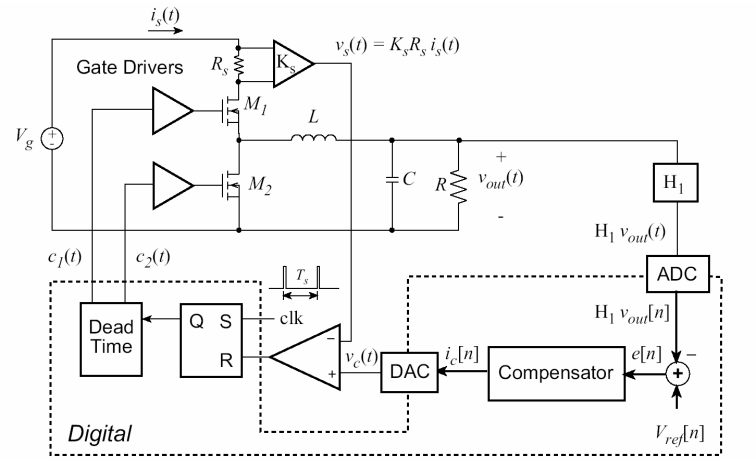


Fig. 7-7 Typical mixed signal control scheme for a DC/DC converter [18]

Mixed signal controllers of the above-mentioned type have been proposed for virtually any type of application that switch-mode power converters are used in. The application range spans from Power Factor Correction circuits to low power DC/DC converters for Point of Load applications.

Other mixed signal control methods have been proposed with very different implementations and design criteria. One of the more interesting ideas is to change the system configuration dramatically so that sampling the output voltage and/or inductor current is avoided. An example of this is given in reference [21] (see Fig. 7-8), where the control method is built around two DACs that generate analogue reference voltages for the inductor current and output voltage error respectively. The current reference is a constant voltage whereas the voltage reference is a DC voltage superimposed by a ramp. The two MOSFETs, S1 and S2, are controlled by a very simple logic block that takes the two comparator outputs CompV and CompI as inputs. The digital logic is asynchronous in nature thus allowing the MOSFETs to be turned on and off at the exact instant the

comparator outputs change. The control method is referred to as synchronous/asynchronous because the control of the DACs is synchronous and the control of the MOSFETs is asynchronous. The same idea can be extended to pure voltage mode control and has been demonstrated on different converter topologies [22-24].

Other mixed signal control schemes have been proposed for special applications such as DC-DC converters with multiple outputs sharing a single inductor [25-27]. These methods differ in their implementation and the purpose of the design, but common to them is that the control scheme utilizes mixed signal methods.

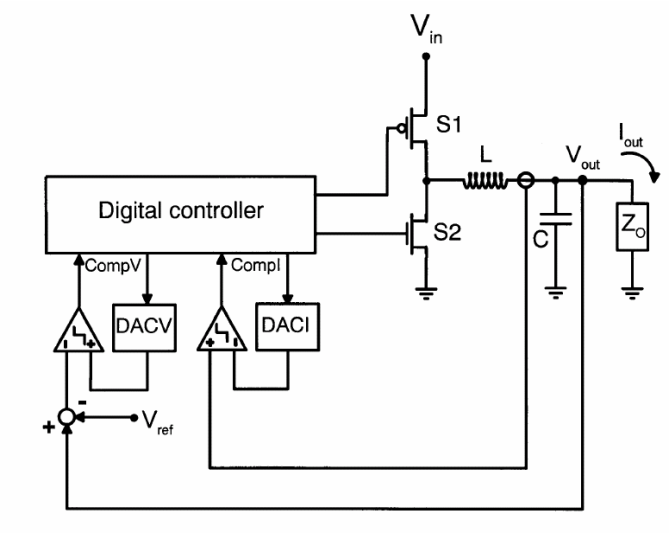


Fig. 7-8 Mixed signal control scheme without an ADC [21]

7.2.2 Digital Voltage Mode Control

Digital voltage mode control is the simplest form of digital control for a switch-mode power converter. The main application for digital voltage mode control is non-isolated DC-DC converters, primarily VRMs and general purpose POLs.

In this section digital voltage mode control is defined as a control system that samples the output voltage and based on that calculates the new duty command for the digital PWM module (see Fig. 7-9). All control schemes described in this section are based on linear control laws (for non-linear control methods see section 7.2.4).

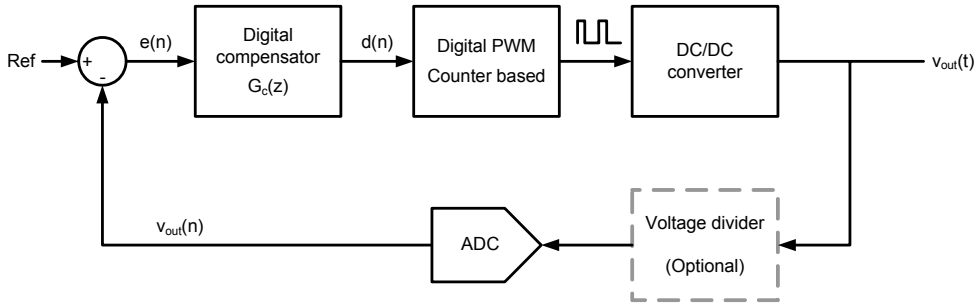


Fig. 7-9 Block diagram for a basic VMC control scheme for a DC/DC converter

The most common voltage mode control scheme is to implement the compensator $G_c(z)$ as a PID controller emulating the most common analogue control scheme [28-32]. The digital PID compensator has a transfer function, which is typically defined in the z-domain by equation 7.2. There are some slight differences in the definition of the transfer function for digital PID compensator, where some papers add one or two extra poles at high frequencies.

$$G_c(z) = \frac{b_0 + b_1 \cdot z^{-1} + b_2 \cdot z^{-2}}{1 - z^{-1}} \tag{7.2}$$

The implementation of the voltage mode control scheme in references [28] to [32] differs in the type of digital hardware and ADC that is used, but the basic control scheme is the same.

The sampling frequency of the ADC has a large impact on the control loop bandwidth of the digitally controlled DC/DC converter. Traditionally the sampling frequency is equal to the switching frequency of the DC/DC converter and the output voltage is sampled at the beginning of each PWM period. The digital controller calculates the new duty cycle and updates the duty cycle command for the DPWM modulator at the beginning of the next PWM period. The limitation in sampling frequency and the delay caused by the traditional sampling scheme will limit the control loop bandwidth that can be achieved for a given converter.

To increase the control loop bandwidth it has been proposed to sample the output voltage at a faster rate than the switching frequency [31-34]. In multiphase converters the sampling frequency can be equal to the switching frequency of each phase multiplied by the number of phases in the converter, since the duty cycle can be updated for the individual phases at the beginning of the switching period of every phase.

Other implementations of digital voltage mode control can be found in references [35] through [39].

7.2.3 Digital Current Mode Control

Digital current mode control is a dual loop control scheme which samples both the output voltage and the inductor current. The voltage loop calculates a reference current for the current loop and the current loop calculates the duty cycle command to achieve the correct inductor current. Digital current mode control can be implemented in a number ways, e.g. peak or average current mode control, depending on how the inductor current is sampled [40]. Reference 40 gives an overview of predictive current mode control techniques. The idea of predictive current mode control is that the digital controller predicts what the duty cycle should be in the following PWM period in order to obtain a certain inductor current at the end of the following PWM period. Almost every digital current control scheme is predictive in nature since the digital controller samples the current in one switching cycle, but it can only change the duty cycle in the following switching cycle. Fig. 7-10 shows a schematic of a typical implementation of a predictive current mode control scheme.

Predictive digital current mode control is most often implemented as average current mode control [41-49]. The digital controller samples the average inductor by sampling the current in the middle of either the ON- or OFF-time of the PWM signal controlling the switch-mode converter [41]. In that way the digital controller can sample the average current without sampling the current at a much higher rate than the switching frequency. Another advantage of the proposed sampling scheme is that there will be no switching noise on the current measurement since the ADC samples the current in the middle of either the ON- or OFF-period.

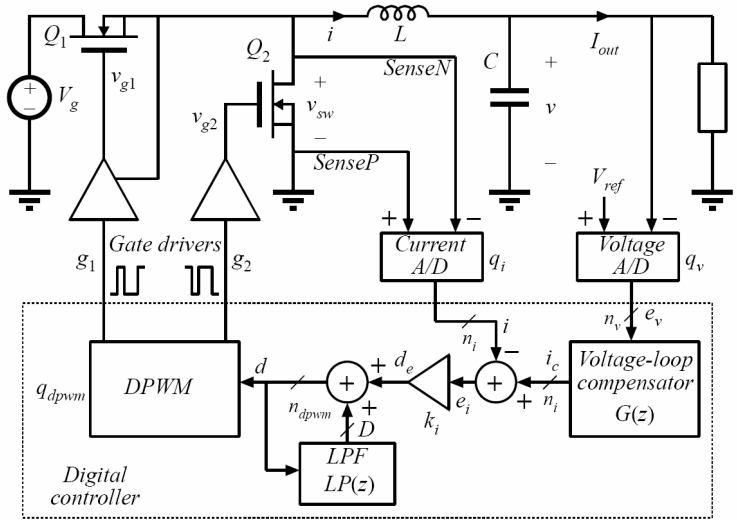


Fig. 7-10 Digital current mode control implementation [48]

Predictive current mode control has been implemented in Digital Signal Processors (DSPs), FPGAs and custom designed ICs. The most common approach is to use a DSP because the DSP is easy to program and it has a number of A/D inputs, which makes it possible to sample both the output voltage and inductor current [41-46]. The current loop is most often realised with a PI- or PID-compensator and the voltage loop as a PI-controller. The number of calculations that must be performed to implement the current loop will in many cases limit the switching frequency that it is possible to achieve for a certain DSP. The limitation is a result of the sampling point of the ADC sampling the current is moving in time as described above. As a result of this the time the DSP has to calculate the new duty cycle command varies with the duty cycle of the PWM signal, which means that a certain minimum calculation time must be allowed in order for the digital controller to complete the calculations. That can easily achieved by reducing the switching frequency. The switching frequency for predictive current control schemes implemented in a DSP are reported up to 200 kHz, which makes it suitable for Power Factor Correction (PFC) applications and high power DC/DC converters.

If the predictive current mode control scheme is implemented in an FPGA or an Application Specific Integrated Circuit (ASIC) the switching frequency can be increased. It is, however, questionable whether the digital current mode control is better than voltage mode control for DC/DC converters with very high switching frequencies, since the predictive current mode control scheme is basically an average current mode control scheme. The current loop in average current mode control typically has a bandwidth that is 5 to 10 times lower than the switching frequency and that will limit the control loop bandwidth of the voltage loop to an even lower frequency. The requirements for converters operating at high switching frequencies is typically high control loop bandwidth for the output voltage and generally it will therefore be a better choice to use a pure voltage mode control scheme.

Predictive current control methods calculates the duty cycle command based on the sampled current and the parameters of the switch-mode converter, such as the inductor size and input voltage. The predictive current control scheme will therefore only be operating optimally when the actual converter parameters match the parameters used in the design of the control law. A simplified digital current mode control technique has been proposed in references 50 and 51. This technique alleviates some of the problems related to predictive

current mode control as described above. The control scheme is very simple with a proportional compensator in the current loop and can be used in both peak and average current mode control. Because of the simple structure of the control scheme it can also be used to control DC-DC converters with high switching frequency.

A derivation of an OCC control scheme for the inductor current is to use a very fast ADC, which samples the inductor current at a much faster rate than the switching frequency and digitally integrates the sampled current [52]. The PWM signal is generated by comparing the integrated inductor current with a digital current reference which is calculated by the voltage loop. If the integrated inductor current is smaller than the current reference the PWM signal is high. Once the sampled current is equal to the reference the PWM signal is set to low. The integrator is reset to zero at the beginning of each switching period. The control scheme just described is a quite expensive solution since it needs an ADC that samples the current at 20 Million Samples Per Second (MSPS) to control a converter with a switching frequency of just 50 kHz.

7.2.4 Non-linear Control

Digital control of switch-mode converters with linear control methods will generally not be able to achieve as high a control bandwidth as can be achieved with analogue control. The main reason is that the sampling frequency of the digital controller is equal to the switching frequency and the delays of the digital implementation.

One way to improve the transient response is through non-linear control techniques. Non-linear control is in this context defined as a control scheme where the control law changes as a function of the controlled parameter, e.g. the output voltage error. Non-linear control is therefore a very broad definition that includes a number of different implementations.

The fastest way to detect a change in the load current is to measure the output capacitor current, since a change in load current will be immediately reflected in the capacitor current. Measuring the capacitor current is however impracticable in high performance DC/DC converters since a small sense resistor is typically inserted in series with the capacitor, which will increase the output voltage ripple and power losses in the converter. Instead of measuring the capacitor current it is possible to estimate it by sampling the output voltage at a faster rate than the switching frequency and integrating the sampled output voltage error [53]. Alternatively the capacitor current can be estimated by

connecting an LCR-network in parallel with the capacitor, which has a characteristic impedance that is similar to the characteristic impedance of the capacitor, and measuring the current in LCR-network [55]. Once the capacitor current estimator has detected the load current change, the next step is to apply a sequence of PWM signals that restores the output voltage to the steady state value set by the voltage reference.

Reference 53 proposes the Proximate Time-Optimal Digital (PTOD) control scheme, which uses switching surface analysis to reach the steady state output voltage in the shortest time possible. The implementation of the PTOD scheme is a simple state machine that takes over the generation of the PWM signal from a linear PID compensator combined with a DPWM block. The implementation of PTOD scheme is so simple that it can easily be added to any linear control scheme and the performance of the DC/DC converter is dramatically increased during transient load conditions. The only drawback is that the output voltage needs to be sampled at a very high frequency to be able to estimate the capacitor current accurately.

Another way of achieving that the output voltage is returned to its steady state condition in the shortest possible time and with the least overshoot is by changing the control law if the output voltage error exceeds a preset limit [54]. The non-linear control scheme is designed for a Buck converter and the idea is to set the PWM signal to ‘1’ if the output voltage is lower than the lower boundary. The period of time the PWM signal is high is calculated based on an estimation of the output current. Next the PWM signal is set to ‘0’ for the period of time that is required to return the output voltage to its steady state value. This non-linear control requires a large number of computations to find the correct ON- and OFF-times to achieve the optimal response to a step change in the load current.

During the transient condition the non-linear control scheme of reference 55 switches from linear voltage mode control to hysteretic current control for the estimated capacitor current. The control scheme requires that the estimated capacitor current is sampled at a very fast rate to achieve precise hysteretic control of the capacitor current.

The transient response of multiphase interleaved DC/DC converters can be improved by saturating the PWM signals of all phases to either ‘0’ or ‘1’ if the output exceeds an upper or lower threshold error voltage respectively [56]. Once the output voltage is within the threshold voltage the control scheme returns to interleaved operation and the linear control law resumes control of the duty cycle command.

A different approach to non-linear control is to let a PID compensator operate with a variable gain, which depends on the magnitude of the output voltage error [57]. The larger the output voltage error is, the larger is the gain of the PID compensator. The choice of compensator gain may theoretically result in an unstable system for a large output voltage error but because the error will converge towards zero the system will be stable in practice.

7.3 Digital Hardware Implementations

Cost and performance of a digital controller for a switch-mode power converter is greatly influenced by the choice of digital hardware used to implement the digital controller. This section aims to give a short description of the three main types of digital hardware used in digital control of switch-mode converters and mention some of the advantages and limitations of the different solutions.

7.3.1 Microcontrollers

Microcontrollers have been around for several decades and have been used in almost any kind of industrial and consumer electronics. The term microcontroller has been used to describe anything from simple 8-bit controllers with few I/O ports to large 32-bit processors with many I/O ports, and advanced features such as a hardware multiplier for faster calculations. A microcontroller is in this thesis defined as a low cost digital controller with an 8- or 16-bit databus including features such as PWM outputs and A/D converters. The clock frequency of this type of devices is typically lower than or equal to 40 MHz, which limits the number of calculations that can be performed in the software algorithm that performs the control law for the switch-mode converter. The DPWM module in microcontrollers of this class is in general counter based with no extra features to enhance the DPWM resolution.

Microcontrollers can also be used to add extra functionality to switch-mode power supplies with an analogue control circuit [58-59]. In this case the microcontroller does not perform any real-time control of the output voltage or the inductor current, but it is used to supervise and act as controller on a system level. The microcontroller can also be used to add features such as current sharing between converters connected in parallel and to set an external voltage reference for the power supply [58].

The microcontroller adds functionality that could be added with analogue circuitry as well, but it would be more difficult to do so with analogue circuitry.

The microcontroller is reprogrammable, which makes it possible to change the functionality without having to change the hardware design.

The microcontroller can additionally be used to improve system performance by introducing a precise reference to the analogue control circuit [59] thus enhancing system performance. In reference 59 the microcontroller supplies a perfect sine wave reference for the current loop of a PFC to ensure low input current distortion.

None of the above-mentioned features, which can be added with a microcontroller, are included in the definition digital control, but they are examples of how microcontrollers are most often used in power electronics.

Actual real-time digital control of switch-mode power converters have been implemented in microcontrollers with varying results [19, 60-62]. Reference 60 describes a digital voltage mode controller implemented in a microcontroller from Microchip. The control law is a PID compensator implemented with gains that can only be selected as powers of 2. The time it takes to complete the computations necessary to implement the PID compensator is between 18 and 28 μs and the sampling frequency is limited to 20 kHz for a converter with a switching frequency of 78 kHz. Because of the poor adjustability of the PID compensator coefficients and the low sampling frequency, the transient response of the Buck converter tested in the reference is not especially fast. Another issue concerning the design of a voltage mode control scheme in a microcontroller is the low DPWM resolution due to the low clock frequency, which can cause limit cycling.

References 19, 61 and 62 present different mixed-signal controls schemes based on a microcontroller and some simple analogue hardware. The microcontroller used in all three designs is the PIC16C782 from Microchip [63], which includes a Programmable Switch Mode Controller (PSMC). The PSMC (see Fig. 7-11) includes two comparators, which can be used to compare the inductor current with the current reference, which can be set by an 8-bit DAC that is also included in the PIC16C782. The switching frequency can take on values equal to the clock frequency divided by powers of 2. The maximum and minimum duty cycle that the PSMC can generate is programmable by two 2-bit registers.

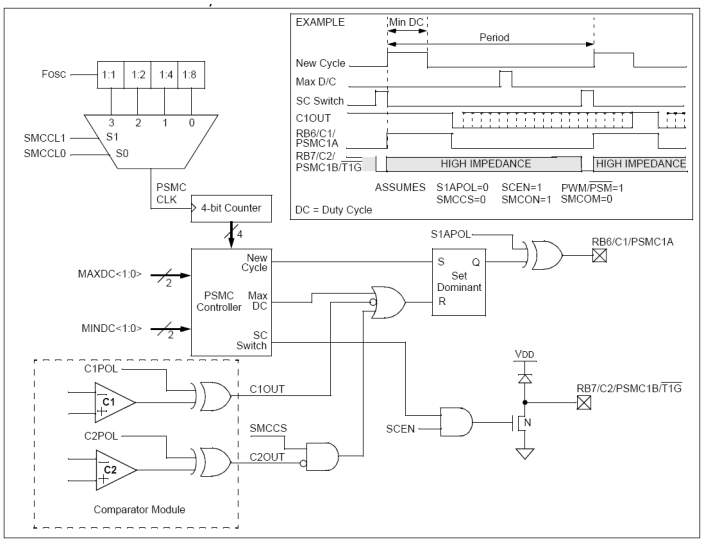


Fig. 7-11 PIC16C782 Programmable Switch Mode Controller [63]

The voltage loop of the mixed signal control scheme is implemented in software in the PIC16C782 and the sampling frequency ranges from 31 to 52 kHz in the cited references. The control laws, which are either a PI compensator [19, 61] or a Fuzzy Logic control law, have been implemented with 8 bit accuracy and all multiplications are performed by bit shifting.

Due to the low sampling frequency and the poor adjustability of the PI compensator or Fuzzy Logic control law the microcontroller based solutions published this far are only suitable for low bandwidth applications.

7.3.2 Digital Signal Processors/Controllers (DSPs/DSCs)

Digital Signal Processors have been used to control power electronics for many years. Typical applications have been motor drives, uninterruptible power supplies and other power converters connected to the utility grid.

Common for these applications is that the cost of the DSP is only a fraction of the total cost and the complexity of the control algorithm is so complex that it requires a large number of calculations. The DSP will typically be quite expensive compared to the total cost of the power supply for most offline SMPSs and DC/DC power supplies.

First of all it is important to define what is understood by a DSP and why the term digital signal controller (DSC) is more appropriate for the kind of device used in digital control of switch-mode power converters.

A DSP is traditionally a component designed to perform a large number of arithmetic operations in a very short time. Typical applications for DSPs have been signal processing in audio and audio/visual applications implementing finite impulse response (FIR) filters and infinite impulse response (IIR) filters.

Filter algorithms depend on two types of mathematical operations, multiplication and addition, and the DSP is designed to perform the filter algorithm effectively. A multiplier/accumulator (MAC) module that can perform one multiplication and one addition in a single clock cycle is therefore an integral part of the DSP. The DSP also has large data and program memory areas to enable advanced filter algorithms.

The traditional DSP is very good at running filter algorithms for high order digital filters, but it lacks other features such as logic operations to compare numbers or single bits. DSPs typically do not include an ADC module, which has to be added as an external component.

The DSC on the other hand is a hybrid between a microcontroller and a DSP. In many cases the DSC also includes a MAC module, but in some devices it only has a dedicated hardware multiplier module that can perform a multiplication in one or two clock cycles. Furthermore the DSC includes other features like a full set of logic operations and in most cases several timers to support multiple PWM outputs and high performance ADCs. Different manufacturers of DSCs target different applications and the term DSC covers quite a large range of devices. A few examples of typical AC/DC and DC/DC converters controlled by a DSP or DSC will be described to give an idea of what the strength of the DSP/DSC is.

The DSP/DSC is well suited for control schemes including several loops, e.g. a current and a voltage loop, and perhaps extra signal processing to enhance system performance. A good example of that is a digital control scheme for a PFC with high control loop bandwidth [41]. The control scheme includes a current and a voltage loop plus an additional comb filter that attenuates the output voltage ripple in the output voltage feedback path. The comb filter has an order of 41 in this example and it is only practicable to implement a filter of that order in a DSP. Another example of a digital control scheme for a PFC implemented in a DSP is reference 44.

A simple voltage mode control scheme for a DC/DC Buck converter, which is based on a DSC, is described in reference 28. The advantage of using the DSC, which in this case is a DSC from the TMS320F280x family from Texas Instruments, is that it runs at a much

higher clock frequency than a typical microcontroller and also that a MAC module is part of the DSC. The MAC module combined with the high clock frequency allows the DSC to sample the output voltage at the same rate as the converter is switching, i.e. 250 kHz in reference [28], which makes it possible to achieve higher control loop bandwidth and faster transient response than what is possible with a microcontroller. It should however be noted that the DSC is capable of much more than controlling a single Buck converter and that it is therefore an expensive solution in this kind of application.

7.3.3 Field Programmable Arrays / Custom ICs

Both microcontrollers and DSCs are general purpose digital devices that can be used in a number of applications. Some of those devices have been designed with switch-mode converters as the primary application, but not for a specific converter topology or converter application. It follows from this that the manufacturer of a power supply almost certainly buys a device that can perform more operations than what is necessary in a specific product. The result is that the cost of the power supply is higher than strictly necessary.

Customised digital control ICs are increasingly popular in both academic research and the industry because they can offer a solution that is targeted for a specific application. The number of solutions that have been presented in scientific papers and introduced by semiconductor manufacturers is quite large and the solutions are very diverse. The subject is therefore divided into selected groups of solutions to highlight some of the trends.

Solutions programmed in FPGAs are included in this description because FPGA implementations presented in papers are used to show a new control method that should be implemented in an IC if the control method was to be sold commercially. FPGAs are good for prototyping but they are too big and expensive to be considered for use in low cost switch-mode power supplies.

7.3.3.1 PID compensator implementations

The digital PID compensator is the most common control law used in digital control for switch-mode converters. The digital PID compensator is actually an IIR filter and can be represented by the general difference equation 7.3.

$$d(n) = a_1 \cdot d(n-1) + \cdots + a_i \cdot d(n-i) + b_0 \cdot e(n) + b_1 \cdot e(n-1) + b_j \cdot e(n-j) \qquad (7.3)$$

where d is the duty cycle command for the DPWM, e is the error signal, n is the current sample number and i and j represents the number of poles and zeroes of the IIR filter. For the typical PID compensator (see equation 7.2) i is equal to 1 and j is equal to 2.

In a DSP/DSC the difference equation is solved with the MAC module, which performs the necessary multiplications and additions and the same method can be used in a custom IC [64-65]. Reference 64 presents a fixed-point 16-bit DSP core that is custom designed for digital control of switch-mode converters. Unlike a general purpose DSP/DSC the customised DSP core has a very limited instruction set (less than 30 instructions) which makes it a much simpler task to program the control algorithm. The DSP core has a 16×16 bit hardware multiplier and a 32-bit ALU to perform the MAC operations. The gate count of the custom designed DSP core is small because of the limited instruction set thus reducing the physical size and power consumption.

An even simpler DSP core have been described in reference 65 to further reduce the size and cost of the digital control IC. That design utilizes an asymmetrical hardware multiplier with different word-lengths for the two inputs. The idea is that one of the input signals to the multiplier can be represented by a small number of bits, e.g. the error signal, whereas the other signal, e.g. the coefficient b_n, must be represented with a higher number of bits. The complexity and thereby the physical size of the hardware multiplier is reduced by reducing the number of bits of one input and ultimately the cost of the digital control IC is reduced.

The lookup table based design is an alternative to the MAC based DSP core just described [66]. Instead of using a hardware multiplier block, which can be a quite large and expensive block in an IC design, the results of all possible multiplications can be calculated in advance and stored in a lookup table. The result of the multiplication of any error value and corresponding compensator coefficient can be read from memory during the calculation of the difference equation defining the PID compensator. The amount of memory that is allocated for the lookup table depends on the number of error values, which is determined by the ADC resolution and the required word-length for the compensator coefficients. The implementation of flash memory in an IC may be more expensive than having a larger amount of digital logic, e.g. a hardware multiplier, and there will be a trade-off that needs to taken into consideration when choosing which solution to use. A more critical issue in connection with the lookup table based design is that it is much harder to change the compensator coefficients on the fly, since the complete lookup table has to be updated rather than just a few registers storing the compensator coefficients.

A third way of realising a PID compensator is to split the compensator transfer function into three terms, i.e. a proportional (P), an integral (I) and a derivative (D) term, that are solved separately and in parallel as shown in Fig. 7-12 [67]. The time it takes to compute the new duty cycle command is very short in this PID compensator implementation because the three terms are computed simultaneously.

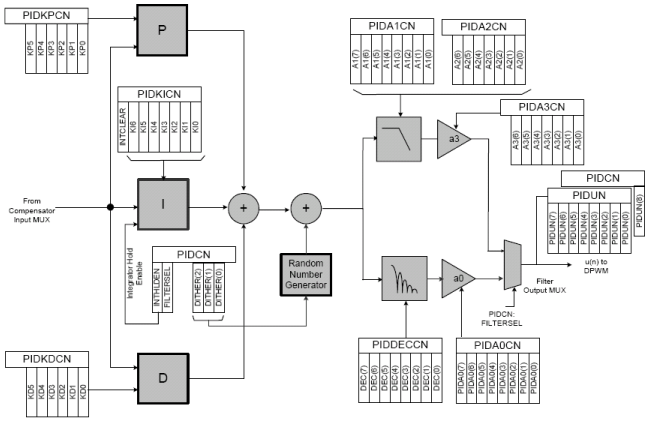


Fig. 7-12 PID compensator wit separate P, I and D terms [67]

7.3.3.2 Multimode controller ICs

The efficiency of switch-mode converters is typically low at light loads where the switching losses in the power stage are the dominating power loss. Light load efficiency can be improved by changing the modulation scheme from pulse width modulation to pulse frequency modulation (PFM). The power losses at heavy load is however larger for PFM than for PWM. Several multimode controllers that change modulation scheme depending on the load current have been proposed in order to optimize efficiency at both light and heavy load conditions.

Multi-mode control ICs for low power DC/DC converters in portable applications can help reduce standby power consumption without degrading performance at heavy load currents [68-69]. To reduce system cost and power consumption the typical external high frequency clock has been removed and the PWM signal is generated by a ring oscillator, which consist of a number of delay elements connected in a ring (see Fig. 7-13). In PWM mode the output voltage is controlled by a PID compensator and the DPWM block. In PFM mode the output voltage is compared to the reference voltage and every time the output voltage is lower than the reference voltage a pulse of a fixed width is sent to the

high side MOSFET. The operating mode is chosen based on the load current and a set of efficiency curves for PFM and PWM operation.

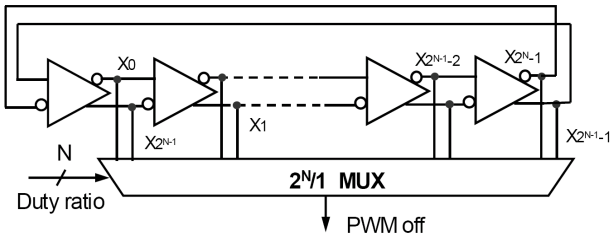


Fig. 7-13 Ring oscillator for PWM generation in multi-mode control IC [68]

The mixed-mode control scheme can also be used in voltage regulator modules to improve light load efficiency [70]. Pulse skipping in the DPWM module is used rather than the traditional PFM control scheme to improve efficiency at light loads. The idea is that if the duty cycle command calculated by the digital compensator is below a minimum value the PWM pulse is simply skipped. The result is the same as in PFM mode, but the digital implementation is different.

7.3.3.3 Other digital control schemes

Most digital control schemes presented so far in this state-of-the-art analysis have been based around an ADC, which samples the output voltage and perhaps the inductor current. A few papers have proposed alternative methods for the analogue to digital conversion of the output voltage.

In reference 71 the ADC is replaced by four voltage controlled oscillators (VCOs) and an appropriate digital hardware implementation. The oscillating frequencies of the VCOs are determined by a string of counters and added together to get the result of the I- and D-terms of the digital PID compensator. The VCO outputs are also used as clock signals to generate the PWM output for the DC-DC converter. Any change in output voltage due to transient load conditions will directly affect the switching of the PWM output because the PWM output is clocked by the VCOs. Only simulations are shown in reference 71 and it is questionable how well the control scheme will perform in a practical implementation.

Another digital control that focuses on reducing the delay uses an analogue comparator to compare the output voltage with a sawtooth voltage generated a DAC [72]. The control scheme is basically a PID compensator and a counter based DPWM module. The advantage of the design is claimed to be a very short delay from the instant the output

voltage is ‘sampled’ by the DAC/Comparator circuit to the time the duty cycle command is updated.

8 Microcontrollers in Power Electronics Converters

The subject of this chapter is the use of microcontrollers for real-time control of switch-mode power converters. In the following the definition of a microcontroller used in this project is given and important microcontroller features that makes them suitable for real-time control of switch-mode power converters are described. The importance of optimizing the software algorithm that performs the calculations pertinent to the digital control law will be discussed together with a detailed description of the software design. The discussion of microcontrollers in power electronics will be supported by four papers published at international conferences and one manuscript submitted for the IEEE Transactions on Power Electronics. The four conference papers are reproduced in appendices A – C and G and the manuscript can be found in appendix J. The papers describe important details of the experiments carried out with microcontrollers throughout the PhD project and the reader is encouraged to read the papers.

In 2004, at the beginning of the PhD project, a search for literature on the subject of digital control showed that the preferred solution for digital control at that time was the DSP/DSC. My supervisor Professor Michael Andersen and I thought that it should be possible to use a low cost microcontroller instead of a DSP without degrading the performance of the power converter, thereby reducing the cost of the digital control solution. The aim of the work has therefore been to use cheap microcontrollers and through optimized software design find the limits in control loop performance imposed by the specifications of the microcontroller. Another reason for choosing a microcontroller rather than a DSP was that the power consumption of the microcontroller is lower than that of a DSP. The power consumption of the digital control device is especially important in converters with low output power such as POLs, where the power consumption of the digital control device can have a large impact on the converter efficiency.

8.1 Microcontroller definition

Generally a microcontroller is defined as a device that combines a processor core and some peripheral devices, e.g. A/D converters and PWM modulators, in a single IC. The processor core can be very simple in cheap microcontrollers, e.g. the PIC16 family that has an 8-bit databus and an instruction set of just 35 commands, or it can be very advanced and expensive with a 32-bit databus, hardware multipliers for advanced arithmetic operations and large instruction sets. The advanced type of microcontrollers is in many ways quite

similar to DSCs as described in section 7.3.2 of the state-of-the-art analysis and it is a matter of taste whether they are called a microcontroller or a DSC. Common for the advanced type of microcontrollers is that they have a large number of I/O pins and operate at a relatively high clock frequency, typically in the range from 50 to 100 MHz. The result is a large supply current for the device and a large footprint on the PCB.

The purpose of using a microcontroller in the first place was to use a cheaper device than a DSP/DSC, and the scope of microcontrollers considered for this project has been limited to 8- or 16-bit microcontrollers with a clock frequency up to 40 MHz and a small number of I/O pins. A list of devices that are suitable for real-time control of switch-mode power converters and which are commercially available at the time of publication of this thesis is given in Table 8-I. The microcontrollers in the table have been selected based on the above-mentioned requirements of low cost and a small number of I/O pins and important parameters such as ADC resolution and sampling frequency, PWM resolution, and the internal bus-width of the microcontroller. The three most important parameters are the clock frequency, PWM resolution and ADC sampling frequency.

	Max. clock frequency	Databus-width	Timers	PWM outputs	PWM resolution @ f_{sw} = 250 kHz	ADC sampling rate	ADC resolution
ATMEL ATTiny26	16 MHz	8 bit	2 × 8 bit	2	8 bit	77 KSPS	10 bit
Texas Instruments MSP430F2012	16 MHz	16 bit	1 × 16 bit	2	6 bit	200 KSPS	10 bit
Freescale MC68HC908LB8	40 MHz	8 bit	1 × 16 bit	3	10 bit	62.5 KSPS	8 bit
Microchip PIC18F2410	40 MHz	8 bit	1 × 8 bit 3 × 16 bit	2	7.3 bit	114 KSPS	10 bit
Silicon Laboratories C8051F330	25 MHz	8 bit	4 × 16 bit	3	6.6 bit	200 KSPS	10 bit

Table 8-I Examples of low cost microcontrollers suitable for power electronics applications

The clock frequency is important because it determines how many instructions the microcontroller can perform in one second, typically measured in MIPS. The number of MIPS that one microcontroller can perform is not comparable with the number of MIPS of a different microcontroller for two reasons. The bus-width determines how large numbers that can be handled by the Arithmetic/Logic Unit (ALU) in a single instruction. It will be

necessary in most applications to use 16-bit arithmetic, which means that for an 8-bit microcontroller an addition of two numbers will take more than one instruction to compute, whereas a 16-bit microcontroller can perform the addition in a single command cycle.

The resolution of the PWM module in a microcontroller together with the ADC resolution and the ADC sampling frequency determines the accuracy with which the output voltage can be controlled and also the achievable control loop bandwidth.

It is interesting to notice that the microcontrollers in Table 8-I have widely differing parameters and that there is no optimal choice that incorporates the optimal set of specifications. High bandwidth digital control requires that the output voltage is sampled once for each PWM period and the highest sampling rate of the microcontrollers listed in Table 8-I is 200 KSPS. For some of the microcontrollers the sampling rate is much lower which can seriously limit the switching frequency of the switch-mode converter controlled by the microcontroller. Experiments performed as part of this project has however shown that the ADC in the ATTiny26 from ATMEL is capable of sampling at 125 kHz if the effective resolution does not have to be higher than 8 bits.

8.2 Software design for real-time control of switch-mode converters

Software design is the most challenging problem in real-time control of switch-mode power converters with a microcontroller. The algorithm that computes the control law, e.g. a PID compensator must be executed in the shortest possible time for two reasons. The first for the need for a short execution time is that any delay in a control system adds negative phase shift, which makes it difficult to design a compensator that ensures high control loop bandwidth and a fast transient response. The second reason, which turns out to be a much more serious obstacle, is that the time it takes the microcontroller to complete the control law algorithm limits the sampling frequency. For instance, if the computation time is 10 μs then the maximum sampling frequency is 100 kHz. In publications by He et al. [61,62] on real-time control of switch-mode converters with a microcontroller the sampling frequency has always been lower than the switching frequency.

Writing software for a microcontroller can be done in the assembly language of the microcontroller or in ANSI C. The choice of programming language is very important since the development time can be reduced considerably by programming in ANSI C rather than assembly language. The advantage of programming in assembly language on

the other hand is that the engineer writing the software has full control over the number of commands that the microcontroller has to perform as part of the control law algorithm. A C compiler will generally use a set of standard libraries to convert the C code into machine code for the microcontroller and these standard libraries are designed to handle a number of different situations. The result is that the C compiler will add a number of instructions that can be left out if the software designer knows exactly what is required to perform the necessary operation.

Programming the control law algorithm in assembly language can reduce the execution time by as much as a factor of 3 to 4, which can be of great importance when fast execution time is important.

A digital PID compensator was written in C code for the ATMEL ATTiny26 microcontroller as part of a student project concerning digital control for a Flyback converter [73]. The execution time of the control law including ADC sampling and updating the duty cycle command was found to be 18.9 µs. The PID compensator was implemented with the same basic parameters as the designs presented in appendices B and C, where the execution time for an optimized assembly language implementation was 4.88 µs. To get the shortest possible execution time both the C code and assembly language implementations used lookup tables stored in the program memory of the microcontroller as an alternative to performing real-time multiplication algorithms, which would have to multiply an 8-bit error signal with a 16-bit coefficient.

An ATMEL application note describes a PID compensator for the ATMEL AVR family written in C code [74]. The PID compensator is programmed with separate P, I and D terms and anti-integrator windup to avoid saturating the integrator. The execution time of the algorithm is 877 clock cycles, which corresponds to 55 µs at a clock frequency of 16 MHz. The execution time of the PID compensator described by the ATMEL application note is 11 times longer than that of the implementation described in appendices B and C.

It is obvious that there must be some fundamental differences in the two implementations considering the large the difference in execution time. The following description will focus on how it is possible to reduce the execution time by a factor of 11 and what limitations the assembly language implementation imposes on the PID compensator performance.

Before going into details with the optimization of the algorithm, it is worthwhile to look at the main features of the ATTiny26 CPU core (see Fig. 8-1) and the instruction set of the AVR 8-bit family.

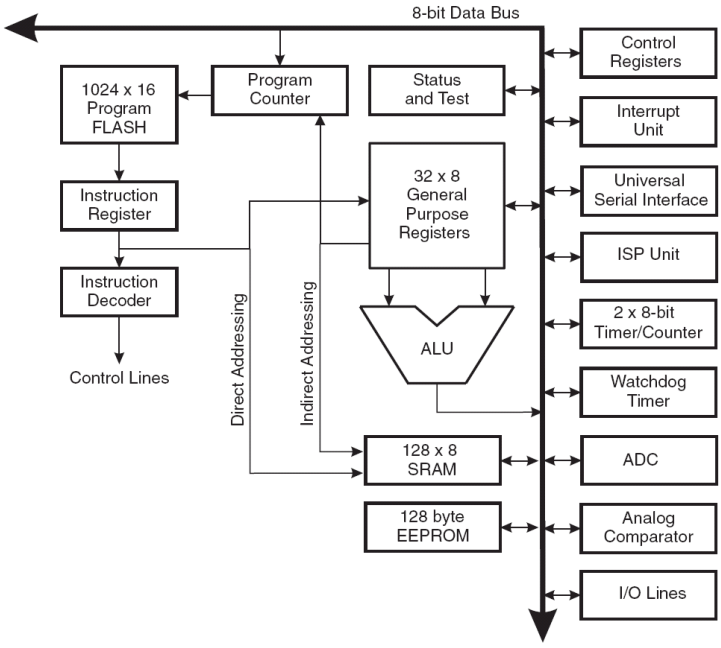


Fig. 8-1 Block diagram of the ATTiny26 CPU core [76]

The ATTiny26 has 2048 bytes of program memory, which is partitioned in 1024 words of 16 bits. Each instruction that is stored in the program memory has an opcode[1] of 16 bit, which means that a maximum of 1024 instructions can be stored. The number of instructions that can be stored in program memory will be reduced if part of the program memory is used to store one or more lookup tables. Temporary data can be stored in 128 bytes of SRAM and in 32 general purpose 8-bit registers.

The general purpose registers are used in connection with the execution of instructions involving the arithmetic logic unit (ALU) and for other purposes such as indirect addressing for memory. The ALU of the ATTiny26 can perform 8-bit additions and subtractions and a large number of logic operations such as comparing two numbers or checking if a status register bit has been set. Important data that needs to be accessed quickly can be stored in some of the general purpose registers depending on the data memory requirements. In that case the design engineer writing the microcontroller software must allocate some of the general purpose registers for specific variables while

[1] An opcode is the machine language code, which tells the microcontroller what command to perform and with which registers to perform the instruction.

leaving other registers free for other operations. This cannot be done automatically in the development software and it is up to the design engineer to make sure that data is not inadvertently changed during the execution of the software. This is especially important if C code and assembly code are combined in a project.

The advantage of allocating general purpose registers for specific variables is that it saves a load command when the program needs to process the specific variable and a store command once the new value of the variable has been calculated, thereby reducing the execution time of the algorithm.

Reading data stored in the program memory of the microcontroller can be performed with the *LPM* instruction in the AVR instruction set [77]. The address of the data is a 16-bit word, which is stored in the Z-address register. The Z-address register is actually composed of the general purpose registers r30 and r31. The use of the *LPM* instruction involves loading the address from which the data should be read in program memory into the Z-address register. After loading the address the 8-bit data is read and stored in a general purpose register. The instruction set of the AVR microcontroller family also makes it easy to read 16-bit data stored consecutively as two bytes in program memory, which makes it very easy to use 16-bit lookup tables and arithmetic in the PID compensator algorithm.

The assembly code implementation of the PID compensator algorithm for the ATMEL ATTiny26 that was utilized in the designs described in appendices B and C relies on several methods that reduce the execution time. The transfer function of the PID compensator is shown in equation 8.1.

$$G_c(z) = \frac{d(z)}{e(z)} = \frac{a + b \cdot z^{-1} + c \cdot z^{-2}}{1 - z^{-1}} \tag{8.1}$$

The compensator transfer function expresses the relation between the duty cycle command *d(z)* and the error signal *e(z)*.

Based on the basic features of the ATTiny26 CPU core and the AVR instruction set, it was possible to write the PID compensator algorithm described in appendices B and C. The steps that have been taken to reduce the execution time of the PID compensator

algorithm will be described in detail below. The flowchart for the algorithm is shown in Fig. 8-2 and the assembly code file can be found on the CDROM.

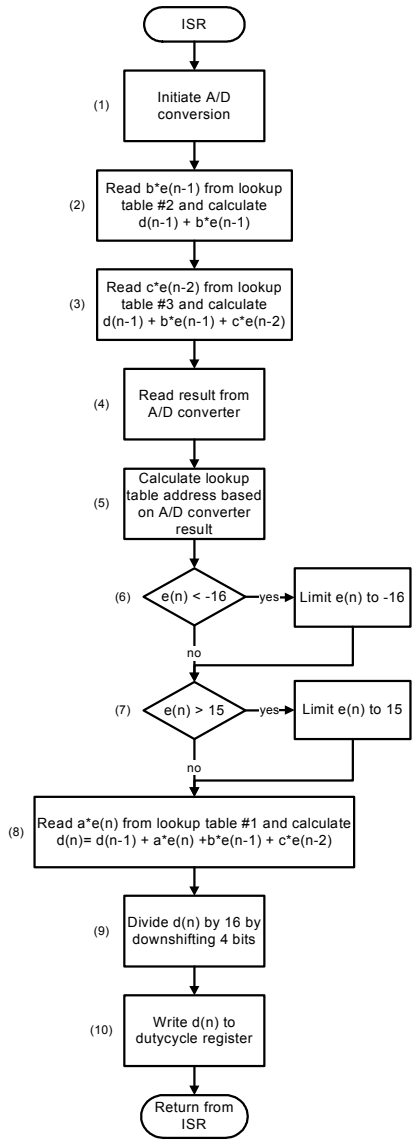


Fig. 8-2 Flowchart for microcontroller PID compensator algorithm (see appendix C)

- The calculations are performed in an optimal order of execution which minimizes the execution time. The algorithm starts by initiating the A/D conversion and while it is waiting for the ADC to finish the conversion it reads the terms *b·e(n-1)* and *c·e(n-2)* from the to lookup table and adds the two terms to *d(n-1)* thereby handling part of the computations while the ADC is sampling the output voltage. The order in which the calculations are performed in the logical order once the result of the A/D conversion is ready.
- Instead of polling the ADC 'End of Conversion'-bit to determine when the conversion has finished, the conversion time in clock cycles was calculated when

the algorithm was written and used in the software design. In the actual design presented in appendices B and C, the A/D conversion has finished some clock cycles before the result is read. That ensures the best flow in the PID compensator algorithm, because the software algorithm does not have to be inactive while it is waiting for the ADC to perform the A/D conversion.

- The error range is limited to ÷15 to 16. The error range was chosen to keep the memory allocated for the lookup tables at an acceptable level. The memory allocated for each coefficient, i.e. *a*, *b* and *c*, is 64 bytes, which gives a total of 192 bytes of program memory allocated for the lookup tables. The three lookup tables are stored in the program memory consecutively (see Fig. 8-3) with the first table starting at address $200.

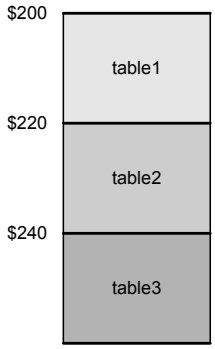


Fig. 8-3 Memory allocation for lookup tables in PID compensator algorithm

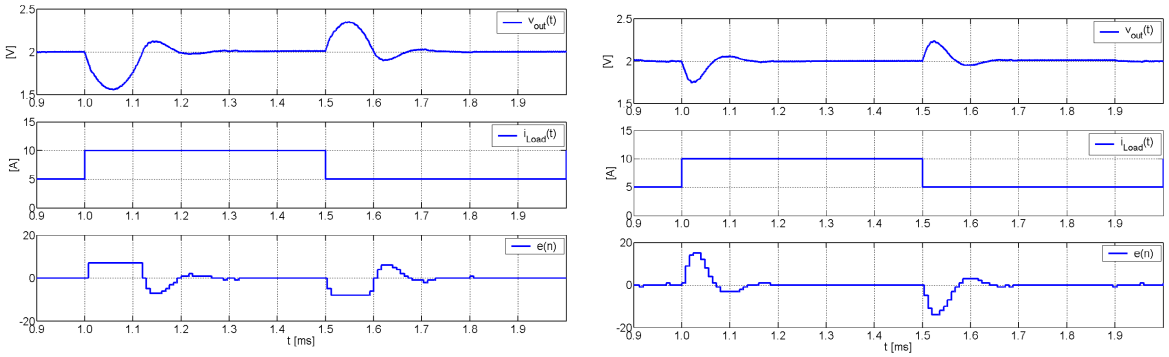
- Another reason for limiting the error range to 32 values is the possibility of using the command *ADIW* in the AVR instruction set. The *ADIW* command adds a so-called literal, i.e. an integer number, to the contents of the Z-address register. The literal can only take on values between 0 and 63. The *ADIW* is used in the PID compensator algorithm to read the result of $b \cdot e(n-1)$ from program memory in the beginning of the compensator algorithm. The reason for using the *ADIW* command is that the Z-address register points to the second byte of the address corresponding to the output voltage error of the previous sample, i.e. $e(n)$, which becomes $e(n-1)$ in the following sampling period. The first address for the 16-bit word representing $b \cdot e(n-1)$ is therefore equal to the address stored in the Z-address register plus 63 with the selected error range. If the error range was larger than 32 values it would not be possible to use the *ADIW* command and the execution time would be longer.

- All temporary data including the duty cycle command *d(n)* are stored using the general purpose registers in order to avoid using the load and store commands necessary to access data stored in the SRAM. Five general purpose registers are thus exclusively allocated to store the error signals and the duty cycle command, which still leaves 27 general purpose registers available for other uses.

The optimized PID compensator algorithm has some disadvantages caused by the way the algorithm has been written so as to reduce the execution time to a minimum.

The main disadvantage is that the error range has been limited to a small range around the reference value to reduce the amount of program memory allocated for the lookup tables and to be able to use the *ADIW* command of the AVR instruction set. The disadvantage of limiting the error range is that the output voltage may actually exceed the range of the digital error signal during transient conditions, e.g. a step in the load current, which will make the settling time longer for the output voltage. Whether or not the output voltage will actually exceed the effective measuring range of the ADC set by the limited error range is a matter of ADC resolution and the ADC input voltage range and the error range defined by the microcontroller software. The error range should preferably be selected so that the error signal never saturates during normal transient conditions.

Fig. 8-4 shows a simulation of a load step on one of the prototype converters described in appendix B and C. In Fig. 8-4a the error signal is limited to an even smaller range than the actual limitation set by the software algorithm. The simulation shows that the error signal saturates and the output voltage deviation from the steady state condition is larger if the error range is too narrow. Fig. 8-4b shows the same simulation but with the error range set in the actual microcontroller software.



(a) (b)

Fig. 8-4 Simulation of a load step response for the ‘PWM-DAC‘ design of appendix C
(a) Error range limited to -7 to +8 (b) Error range limited to -15 to +16

Another disadvantage of the PID compensator algorithm is the use of lookup tables as a substitute for a hardware multiplier circuit in the microcontroller. If the PID compensator frequency response has to be changed the contents of all three lookup tables must be reprogrammed. It is possible to do so while the microcontroller is running because the AVR instruction set allows the software to change the contents of the program memory. It is however very difficult to change the lookup tables on the fly, i.e. when the microcontroller is actively controlling a switch-mode power converter. The difficulty lies in the time it will take to update the contents of the lookup tables. The update process will run over a number of PWM cycles and the compensator will perform in a manner that can not be predicted, which may cause catastrophic failure in the converter.

8.2.1 Software reuse and development time

Writing the software algorithm described in appendices B and C took quite a long time because it was necessary to figure out the optimization methods just described. The development time will probably be considered too long from an industry perspective where time-to-market is often one of the more important aspects in the development of a new product. The engineer writing the software must be proficient in assembly programming and have a good understanding of how a microcontroller works to be able to optimize the code sufficiently for the microcontroller to be able to control a switch-mode converter with good performance. Software reuse is therefore essential for any company to consider using microcontrollers in the company's products.

Under the assumption that the control law does not have to be changed, i.e. the basic transfer function does not have to be changed, the PID compensator frequency response can be changed by changing the contents of the three lookup tables. Once the lookup tables have been changed it is simply a matter of compiling the code with the new lookup tables and programming the microcontroller with an in-circuit serial programmer. Switching and sampling frequency can also be changed easily by changing a few numbers in the microcontroller code. It becomes considerably more difficult if the hardware design dictates a change in either ADC input or PWM output port, but it is still possible without too much trouble to reuse the original software.

Changing the control law from the basic PID compensator to a different compensator transfer function with extra zeros or poles is however a longer process. Zeros can be added by adding one or more lookup tables and changing the software. In the design described in

appendix G an extra zero was added to the compensator transfer function. The sampling frequency for that converter was 125 kHz, which made it possible to add the extra zero and still keep the execution time smaller than the sampling time.

Even though the same principles were used and the code for the PID compensator was partly reused it took both time and effort to find a way to add the extra zero. The new control law had an execution time of 6.5 µs, which is an increase of 1.6 µs compared to the PID compensator algorithm. Besides the extra zero, which involves an extra lookup table, the new algorithm features a duty cycle limiter that limits the duty cycle to values between 0 and 0.5. The duty cycle is limited because the converter is a two-switch forward converter that should not be operated with a duty cycle above 0.5. The total execution time is increased by almost 30% by adding two relatively simple functions and that was only achieved by rethinking much of the design, which shows that software reuse can be challenging even if only apparently minor changes have to be made.

8.3 Microcontrollers and power electronics applications

Different power electronics applications have different performance requirements. The control loop bandwidth of converters connected to the utility grid delivering power above 100 W will typically be below 1-2 kHz, but they must at the same time comply with the regulations as to Power Factor and input current harmonics, which in Europe are set out in the EN61000-3-2. Low to medium power DC/DC converters on the other hand must have quite high control loop bandwidth. That is especially true for POLs and VRMs that are typically non-isolated DC/DC converters of the Buck topology.

Experiments have been carried out with the type of microcontrollers considered in this chapter and three different converters that cover the full range of power levels.

8.3.1 Non-isolated DC-DC converters

Non-isolated DC-DC converters are used extensively to supply DC voltages below 5V for digital devices in a variety of applications. The most popular converter topology is the Buck converter in systems with an intermediate bus architecture. The bus voltage will typically be 12 or 24V and the Buck converter will operate with a small duty cycle to generate the low DC output voltage.

The challenge for a microcontroller controlling a Buck converter in this type of application is twofold. The first challenge is to generate a PWM signal with high PWM resolution to control the output voltage accurately. The second challenge is to achieve high control loop bandwidth for the Buck converter. High bandwidth is increasingly important

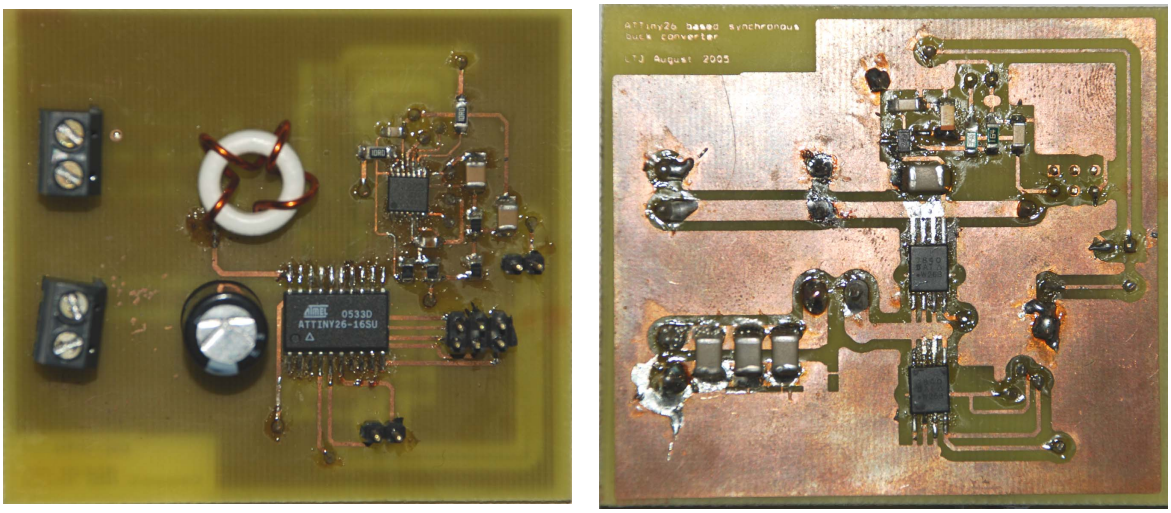
in POL and VRM applications where the load current can change with very high slew rates. High control loop bandwidth helps reduce the transient overshoot and the settling time of the output voltage due to a load step with high current slew rate. The limiting factor when aiming for high bandwidth is the execution time of the PID compensator algorithm, which can be considered as a delay in a discrete control system. The delay causes a negative phase shift, which has to be compensated for in the compensator design to achieve a stable control system with a good phase margin.

The software design that was described in section 8.2 aimed to reduce the execution time of the PID compensator algorithm as much as possible. An execution time of approximately 5 μs is still a very considerable delay in a converter switching at several hundreds of kHz. The switching frequency is a secondary but related problem to the execution time of the software algorithm. The optimal sampling scheme for a microcontroller is to sample the output voltage once for every switching period. A high switching frequency can make it impossible to achieve the optimal sampling scheme. The switching frequency will however also be limited by the clock frequency of the microcontroller, which limits the PWM resolution if the switching frequency is selected too high.

Mixed signal control schemes based on the ATTiny26 for low voltage Buck converters are described in appendices B and C. The mixed signal control scheme was chosen because it gives several advantages over a pure voltage mode control scheme. The mixed signal control scheme is based on an analogue peak current mode control scheme and a digital voltage loop. The control-to-output transfer function for the Buck converter with peak current mode control has only one pole rather than a complex pole pair, which makes it easier to achieve a stable control system despite the delay caused by the execution time of the software algorithm. The disadvantage of the mixed signal control scheme is the additional analogue components in the control circuit. The additional components increase both the Bill of Materials (BOM) of the converter and the board space on the PCB.

The best performing Buck converter in appendices B and C is the “PWM-DAC” design, which has an expensive DAC that generates the reference voltage for the analogue current loop. The theoretically calculated bandwidth is 9 kHz for a converter switching at 250 kHz, which can be easily improved if the delay is reduced (see for instance reference [28]). Reducing the delay, i.e. the execution time of the compensator algorithm, will however require a faster digital controller device such as a DSP or the clock frequency of the microcontroller must be higher.

A third prototype Buck converter (see Fig. 8-5) was designed with a Voltage Mode Control (VMC) scheme programmed for the ATTiny26. The control-to-output transfer function in this case has a complex pole pair due the LC output filter on the Buck converter and a third zero has been added to the compensator to get a stable control loop. The specifications of the Buck converter are the same as those for the converter with the DAC in appendices B and C except for the inductor, which for this converter is only 1.0 µH.



(a) (b)

Fig. 8-5 Buck converter controlled by the ATTiny26 with a Voltage Mode Control scheme.
(a) Top side (b) Bottom side

The software for the VMC prototype in Fig. 8-5 is similar to the software used for the offline converter presented in appendix G. The compensator has three zeros plus one integrator, but unlike the software algorithm for the offline converter the duty cycle is not limited. The real difference however is in the timing of algorithm.

The switching frequency of the Buck converter is 250 kHz, which is two times the sampling frequency. To improve the bandwidth of the Buck converter the compensator algorithm has been programmed with the purpose of minimizing the delay in the control loop. Fig. 8-6 shows the sampling scheme that the microcontroller used for the Buck converter. The microcontroller samples the output voltage at the beginning of a PWM period after which it calculates the new duty cycle before the beginning of the next PWM period. During the next PWM period the microcontroller finishes the calculations and it is ready to sample the output again at the beginning of the following PWM period. In this way the delay from the time of sampling the output voltage to the time the duty cycle command is updated is equal to one PWM period, which is equal to half the sampling

period. The total execution time of the compensator algorithm is 5.5 µs and the compensator utilizes 69% of the microcontroller's resources.

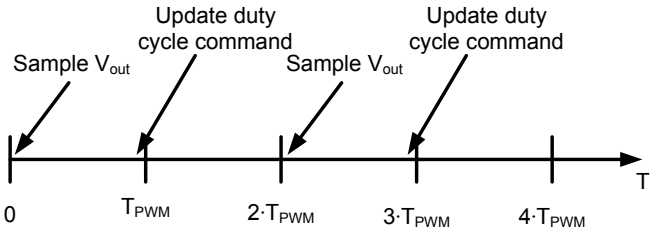


Fig. 8-6 Timing diagram for the software for the ATMEL VMC design for a Buck converter

Fig. 8-7 shows a load step measurement for the Buck converter. Compared to the load step measurements for the mixed signal designs the voltage mode controlled Buck converter has a ringing on the output voltage after the load step. The frequency of the ringing is equal to the output filter resonance frequency and it occurs because there is no analogue current loop to attenuate the ringing in the inductor current. The voltage mode controlled design is simpler and cheaper than the mixed signal designs but the performance is not quite as good.

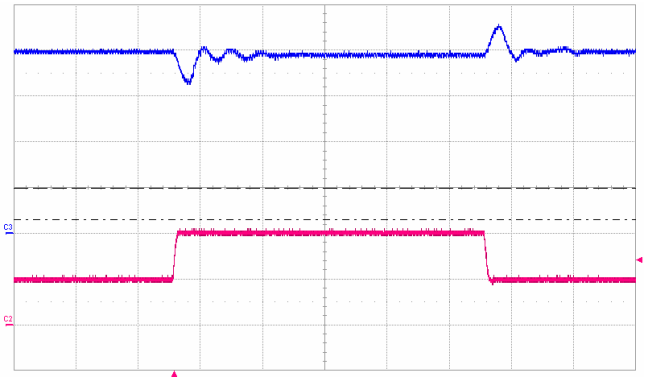


Fig. 8-7 Measurement of load step on Buck converter controlled by an ATMEL ATTiny26

Upper trace: v_{out} 500mV/div (DC)

Lower trace: i_{out} 5A/div (DC)

Time scale: 100 µs/div

8.3.2 Offline converter with galvanic isolation

The offline converter with galvanic isolation was designed with the purpose of making a simple design for a switch-mode converter with digital control and galvanic isolation. The details of the design have been published in the paper of appendix G.

What is interesting about the offline converter design is that it is probably the prototype that is closest to a design that could be put into production of all the prototypes built throughout the PhD project. The combination of the UCC3960 from Texas Instruments on the primary side of the two-switch forward converter and the ATTiny26 on the secondary side solves a numbers of problems inherent to digital control for switch-mode converters with galvanic isolation.

The UCC3960 is an analogue IC that can generate a PWM signal on startup and synchronise to an external PWM signal once the microcontroller on the secondary side has been powered up and starts generating a PWM signal. The real advantage lies in the fact that the UCC3960 has a start up current of 150 μA, which means that it can be supplied through a bleeder resistor from the rectified line voltage for start up. Another feature of the UCC3960 is the currents sense input, which is used for over-current protection. Finally, the UCC3960 has a soft start feature that ramps up the duty cycle of the PWM signal slowly. Over-current protection and soft start could be included in the digital control scheme, but it would be more difficult. Also the microcontroller will probably not be fast enough to handle the over-current protection if real short circuit protection is required.

The prototype PCB was prepared for a digital current mode control scheme with a current sense transformer on the secondary side of the two-switch forward converter and an external ADC that could measure both output voltage and inductor current. It was found that the number of calculations required to implement a full digital current mode control scheme in the ATTiny26 was too large for it to be a feasible solution. The digital current mode control scheme that was implemented was the simplest one that could be found in literature [50] but the conclusion drawn was that digital current mode control for converters operating at a switching above 50 kHz is not possible with a low cost microcontroller.

The software algorithm for the offline converter has already been mentioned in section 8.2.1 about software reuse. The execution is 6.5μs, which is 1 μs more than the execution time of the algorithm used to control the Buck converter with VMC. The basic compensator transfer function is the same for the two designs except that the algorithm for the offline converter limits the duty cycle to values between 0 and 0.5. Another difference is that the external ADC was used because the PCB was designed for digital current mode control. The data acquisition from the external ADC adds some extra commands to the control algorithm, which is a part of the reason for the longer execution time. Changing the

hardware to use the internal ADC of the ATTiny26 would both reduce the BOM of the converter and the execution time of the compensator algorithm.

8.3.3 Boost converter with Power Factor Correction

The idea for the Boost PFC originates from the Danish pump manufacturer Grundfos A/S and the first prototype was built as part of my MSc. thesis project. The primary purpose of that project was to develop and optimize the microcontroller software for the control scheme. Grundfos A/S already had a microcontroller in the existing electronic circuit for their pumps, which was used to control the inverter that drives the pump motor, and the idea was to include the digital control loop of the mixed signal control scheme in the same microcontroller. The reason for changing from an analogue control IC to the mixed signal control scheme is that the analogue hardware multiplier block used in typical average current mode control ICs for PFCs have very large gain variations, which makes it difficult to design a stable control loop with good performance. The multiplication of the output voltage feedback signal, the inverted RMS voltage feedforward signal and the rectified input voltage is partly calculated by the microcontroller and partly by a simple circuit, called a switched multiplier.

The PIC16F877A from Microchip was used in the first prototype together with a 512 kb EPROM, which was used to store a lookup table. The large EPROM made it possible to reduce the utilization of the microcontroller's resources to less than 5% for the simplest design. The sampling frequency was 500 Hz because the control loop bandwidth for the voltage loop in a PFC is very low to get low input current distortion. A more detailed description of the first prototype and the microcontroller software can be found in appendix A.

The first prototype of the Boost PFC demonstrated that the mixed signal control scheme worked well, but the cost of the microcontroller and EPROM made it unattractive for industrial purposes. The second prototype was designed to show that it is possible to control a Boost PFC with low harmonic distortion on the input current with a simple microcontroller and a few analogue components. The microcontroller used in the second prototype was the PIC12F683 from Microchip. The PIC12F683 is an 8-pin microcontroller with both a PWM module and several ADC inputs. The analogue control circuit is virtually the same as in the first prototype but the microcontroller software had to be changed to make it possible to use the PIC12F683. The software algorithm for the PIC12F683 utilizes 9.1% of the microcontroller's resources, which is still very little. The main reason for the

higher utilization factor is that the PIC12F683 has to perform a 24- by 16-bit division in the software algorithm. Appendix J gives a thorough description of both designs and a comparison of their performance.

The advantages of the mixed signal control scheme for the Boost PFC are simplicity and low cost compared to purely digital control schemes implemented in DSCs or FPGAs. The performance of the PFC is good as far as the input current distortion is concerned whereas the control of the output voltage needs to be improved. The compensator in the digital control loop for the output voltage is only a Proportional (P) compensator and as a result the output voltage decreases with increasing load current. The actual voltage drop is approximately 25V from 385V with no load current to 360V at nominal output power, which is 1kW. The compensator of the voltage loop can quite easily be changed to a Proportional-Integral (PI) compensator since the microcontroller has plenty of unused resources. The PI compensator ensures a constant output voltage irrespective of the output power level but the transient response of the PFC will be slower with a PI compensator than with a P compensator.

Another disadvantage of the mixed signal control scheme for the PFC is, that the microcontroller will probably not be able to control any isolated DC/DC converter connected to the output of the PFC despite the fact that the utilization of the microcontroller is quite low. The bandwidth of the DC/DC converter is generally much higher than that of the PFC and the microcontroller will have to sample the output voltage of the DC/DC converter at a much higher rate.

Two things make it difficult to use the type of microcontrollers considered in this chapter for a two-stage PFC solution. The first limitation is the number of computations that the microcontroller is capable of performing. The PIC12- and -16 families from Microchip can only do 5 MIPS and they have a very limited instruction set, which makes it hard to program fast algorithms. A 16-bit addition will take six instructions, whereas the same addition in the ATTiny26 only takes two command cycles. The ATTiny26 or some other microcontroller from the AVR family from ATMEL would probably be a better choice. The real problem, however, is the ADC sampling frequency, because the ADC will have to sample several signals at different sample rates. The best solution would be to use an external ADC together with the microcontroller. Using an external ADC increases the cost and it is questionable if a cheap DSC is not a cheaper solution than the microcontroller plus ADC solution. The board space on the PCB will at least be reduced by using the DSC and the software design will not be any more difficult with a DSC.

8.4 Conclusions and recommendations – The future of microcontrollers in power electronics

Most experts have ruled out microcontrollers as a viable solution for real-time control of switch-mode converters in modern power electronics. The arguments given why the microcontroller is not a viable solution are that microcontrollers are too slow to perform the calculations necessary for real-time control and that software development takes too much time. It is interesting to note that very few papers have been published at conferences or in IEEE transactions about the subject. The question is therefore:

"Can microcontrollers be used in any power electronics applications without degrading the performance of the converter/power supply?"

The answer is not a simple yes or no, but rather that depending on the application and the performance requirements. Microcontrollers can in some cases be the best solution considering cost and performance. Microcontrollers will be best suited for applications that does not require very high switching and sampling frequencies and with moderate control loop bandwidth, which includes PFCs and the offline converters with galvanic isolation. For applications such as non-isolated DC/DC converters, especially POLs and VRMs, microcontrollers are not the obvious choice since the delay of the software execution limits the control loop bandwidth to an unacceptably low frequency.

The research within the field of microcontrollers for power electronics applications carried out as part of this PhD project have shown that good software design is the key to achieving good performance. The developed software algorithms are quite simple, which is the reason why the execution time is very short, and some compromises have been made to achieve the end goal. Even though the execution time of the compensator algorithms written throughout the PhD project are quite short for microcontrollers of the type specified in section 8.1, it is still too long compared to what can be achieved with a DSC/DSP. There are two primary reasons why the execution time is longer for the microcontroller than for a DSC/DSP. The first and obvious reason is that most DSC/DSPs operate at a higher clock frequency than the PICs and AVRs used in this work. The second reason is that the PICs and AVRs are 8-bit microcontrollers that handle 8-bit numbers in the ALU and when loading data from a lookup table. The execution time could probably be reduced by as much as 30-40% if a 16-bit microcontroller was used. Unfortunately, there was no time to experiment with the 16-bit MSP430 family from Texas Instruments for a mixed signal control scheme for the low voltage Buck converter.

The optimal microcontroller for high bandwidth control would have a 16-bit core, operate at 100 MHZ or more and have an ADC with a sampling rate of at least 1 MSPS. To keep the price of the microcontroller low it would be ill-advised to add a hardware multiplier, since that would bring the microcontroller very close to being a DSC. The optimal microcontroller would also have a peripheral block for communication over a serial bus, which is a feature that many low cost microcontrollers do not have. External communication for supervision and programming of control loop parameters is becoming a very important sales argument for digital control and the microcontroller must support serial communication to be a viable alternative to DSC/DSPs.

9 Digital Signal Controllers/Processors in Power Electronics Converters

Digital Signal Controllers or Processors were the primary choice of digital device in the wave of research in digital control of switch-mode power electronics that began around the year 2000. The reasons for choosing DSC/DSPs are that they are powerful devices that can perform a large number of arithmetic operations and that they were already used extensively in motor drives and Uninterruptible Power Supplies (UPS).

DSCs, which will be the term used throughout this chapter, are still used extensively in motor drives and UPSs as well as inverters for renewable energy sources delivering power to the utility grid. DSCs are also slowly gaining industry acceptance for applications such as AC/DC rectifiers for telecommunications and datacenters.

As digital control for switch-mode power supplies has developed to an early stage of market adoption, the industry has found that DSCs are well suited for high power products. In telecom rectifiers the output power level is typically 1–2 kW and performance is not simply a measure of control loop bandwidth and the accuracy of the output voltage regulation, but just as much a matter of adding extra functionality to the product. The extra functionality can be anything from external communication over an I^2C interface, such as the PMBUS™, or startup sequencing of multiple power supplies or outputs.

A power supply in general needs a lot of functionality such as soft start, Under Voltage Lock Out (UVLO) and temperature monitoring. A DSC is capable of handling all of those functions, which may actually make the cost of the complete control circuit cheaper for a digitally controlled power supply than for a power supply with analogue control.

A DSC has only been used in one prototype in this PhD project because it was deemed that other scientists had already determined the capabilities and limitations of DSCs through their research. The information in this chapter will therefore primarily be based on results found in papers published by other scientists but will be supported by the experience gained through the one prototype that was designed by the author of this thesis.

9.1 DSC definition and devices

DSC devices are manufactured by several companies and as in the case of microcontrollers the specifications differ from device to device. The definition of a DSC used in the present thesis is a device that has a 16- or 32-bit CPU core and includes peripherals such as PWM modules and ADCs. Unlike a microcontroller, which may have a

hardware multiplier for arithmetic operations, the DSC has a Multiplier/Accumulator (MAC).

The MAC has been a central part of DSPs used in audio and video applications because it allows the DSP to perform one multiplication and one addition in a single clock cycle. The MAC makes the computations required in digital filters much faster than if separate multiply and accumulate operations had to be performed by a microcontroller with a hardware multiplier.

The number of new DSC devices that are manufactured and sold by some of the big companies in the industry have increased considerably over the last few years. Table 9-I shows an incomplete list of devices that could be considered for digital control of switch-mode power converters. Most of the devices on the list are not intended for that specific application but for other control applications in power electronics such as motor drives. The XC226x family from Infineon is actually called a microcontroller by Infineon which goes to show that the border between microcontrollers and DSCs is somewhat fluid.

	Max. clock frequency	Databus-width	PWM outputs	PWM resolution @ f_{sw} = 250 kHz	ADC sampling rate	ADC resolution	MAC module
Microchip dsPIC30F2010	40 MHz	16 bit	6	7.3 bit	1.00 MSPS	10 bit	Yes
Freescale 56F801	80 MHz	16 bit	6	8.3 bit	0.70 MSPS	12 bit	Yes
Infineon XC226x family	66 MHz	16 bit	4	8.0 bit	0.83 MSPS	10 bit	Yes
Texas Instruments TMS320F2808	100 MHz	16/32 bit	16	14.7 bit	6.25 MSPS	12 bit	Yes

Table 9-I List of DSCs suitable for digital control of switch-mode power converters

The last DSC in Table 9-I has considerably better specifications than the other devices in the list. The TMS320F28xx family from Texas Instruments has been developed with digital control of switch-mode converters as the primary application. The two most important parameters of the TMS320F2808 are the very high PWM resolution and the fast sampling rate of the ADC.

The high PWM resolution is achieved by using a combination of a counter based PWM modulator and a delay line as described in section 7.1.2. The propagation delay of one delay element is 150 ps, which in turn makes it possible to adjust the duty cycle of the PWM signal in 150 ps steps. Only 6 out of the 16 PWM outputs on the TMS320F2808 can

have the high PWM resolution whereas the rest will operate as normal counter based PWM modulators.

The TMS320F2808 has an advanced ADC module that can sample signals on several inputs in sequence or just one signal at a rate of 6.25 MSPS. The fast conversion time is important when controlling converters switching in the MHz range, which is possible because of the high PWM resolution. The TMS320F2808 is thus the first DSC that is truly capable of controlling an interleaved Buck converter switching at 1 MHz per phase or it can control several independent converters with high control loop bandwidth.

9.2 Applications and performance

The strength of DSCs is the ability to perform a large number of arithmetic operations with the MAC. The most common applications for DSCs in switch-mode converters are therefore power supplies with multiple control loops. Multi-loop control requires a large number of computations and a typical DSC with a MAC module is the perfect digital device for this kind of application. To give a complete picture of the capabilities of DSCs both single-loop and multi-loop digital control with DSCs will be described.

9.2.1 Single-loop digital control of switch-mode converters

Single-loop control for switch-mode converters is almost always VMC because it is the output voltage that has to be kept constant. VMC is most often used in low power DC/DC converters since it is not a requirement to control the input current of the converter and also as it makes it more difficult to design a control loop for the output voltage with high bandwidth if digital current mode control is chosen as control scheme.

The most important things in digital VMC are short delays and high PWM resolution as described chapter 8. Controlling just one DC/DC converter with a DSC that costs somewhere between 3 and 6 USD is a bad business proposition and very little research has therefore been carried out with DSCs for single loop control of switch-mode converters.

One example though is the design of a control loop for a Buck converter with a switching frequency of 250 kHz [28]. The design used the TMS320F280x family already mentioned and the control algorithm was programmed in the assembly language of the DSC. The transfer function of the compensator had two poles and two zeros and the execution time of the algorithm was just 26 clock cycles, which corresponds to 260 ns. The total execution time was approximately 400 ns since the duty cycle command had to be updated by the Interrupt Service Routine (ISR) and the DSC has to handle the interrupt request generated by the timer used to generate the PWM signal. The control scheme

sampled the output voltage in the middle of the switching period and the duty cycle command was updated at the beginning of the following switching period. The total delay was thus equal to half a switching period in this design. The maximum switching frequency that can be supported by the DSC is theoretically equal to 2.5 MHz (1/400 ns) if the sampling scheme was changed to sample at the beginning of the switching period.

A comparison of the performance of a VMC control scheme implemented in the TMS320F2801 and a custom digital control scheme implemented in an FPGA was made for a DC/DC converter with variable output voltage (see appendix E). The digital compensator had two zeros and one pole and it was programmed in ANSI C for the DSC. Besides calculating the compensator output the ISR also has to limit the duty cycle command to the range from 0.01 to 0.99 and update the duty cycle registers for two PWM outputs. The sampling frequency was 500 kHz and the execution time of the ISR was found to be approximately 1 μs. Considering the simple compensator structure the execution time is quite long which shows that it is advantageous to program in assembly language if the DSC resources are to be optimally utilized. On the other hand it can be argued that the DSC can be very easy to use in real-time control of switch-mode converters since it is possible to write the software in C which only takes a fraction of the time it takes to program in assembly language.

9.2.2 Multi-loop digital control of switch-mode converters

A DSC is an obvious choice for digital control of switch-mode converters with multiple control loops. Examples of multi-loop control are digital current mode control for a DC/DC converter [43] or a digital control system for a full switch-mode power supply with multiple converter stages [42,78]. Digital control of a PFC is another multi-loop control system that has received much attention in the academic community. The reason why this particular application has received so much interest is twofold. Firstly it is a control problem that can be solved without placing very high demands on the DSC. Secondly it can be difficult to design a PFC with analogue control that has very low input current distortion and a fast dynamic response.

The typical digital current mode scheme used in a DSC is the predictive average current mode control [43]. The control scheme requires the DSC to sample the output voltage and the average value of the inductor current. The calculations are divided into a current control loop and a voltage loop. The voltage loop algorithm is executed first and the result

is a reference value for the current loop. The current loop calculates the duty cycle command for the PWM output based on the predictive control scheme. The multi-loop control system requires the inductor current to be sampled once per switching cycle whereas the output voltage can be sampled at a lower rate if the control loop bandwidth for the voltage loop does not have to be high.

Reference 43 describes a digital current mode control scheme for an interleaved Buck converter with two phases which requires the DSC to compute two current loops and a voltage loop for every switching cycle (see the block diagram in Fig. 9-1). The DSC has to sample the inductor currents at a specific instant in time in order to sample the average current. The timing for the sampling of the inductor currents is handled by the DSC timer hardware, which can generate interrupts at different points in time. This kind of functionality is inherent in most DSCs, and that makes it easy for the design engineer to program even complex multi-loop control systems.

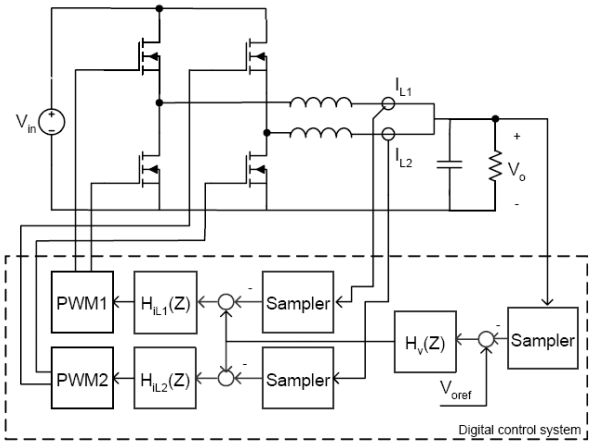


Fig. 9-1 Block diagram of digital current mode control scheme for an interleaved Buck converter [43]

The DSC used in reference 43 is a 150 MHZ TMS320F2812 from Texas Instruments and the switching frequency is 50 kHz. There is no information regarding the software implementation or how great a workload the software algorithm represents for the DSC in this specific application. There is however no doubt that the DSC is capable of handling this kind of multi-loop control algorithm and that the switching frequency could be increased considerably without overloading the DSC.

Reference 78 describes a digital control scheme for a telecom rectifier designed with the UCD9501 from Texas Instruments. The telecom rectifier has an interleaved Boost PFC

stage followed by a phase shifted full bridge converter to generate the regulated DC output voltage of 48 V.

The control scheme in this case has five control loops that must be computed in order to control the PFC stage with current sharing in the interleaved Boost PFC stage and the phase shifted full bridge converter with a VMC scheme.

The Interrupt Service Routine (ISR) uses Time Division Multiplexing (TDM) to operate parts of the control loop algorithm that does not have to be executed at the same rate as the ISR (see Fig. 9-2).

The idea of TDM has been described in [79] and the purpose of TDM is to utilize the resources of the DSC to the fullest extent. Rather than having multiple ISR functions with different sampling rates and different priorities the TDM scheme has only one ISR and part of the ISR code is divided into time slices that are selected by the ISR consecutively for each run of the ISR.

DSCs and TDM are very well matched because the DSC has an instruction set with microcontroller features as well as the capabilities of the MAC. The microcontroller features of the DSC makes it easy to program a decision tree that decides which time slice is to be executed as part of the ISR.

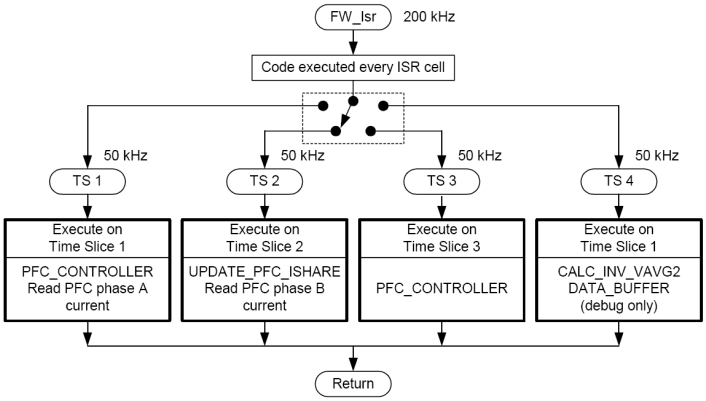


Fig. 9-2 Time Division Multiplexing in ISR [78]

A similar control scheme implemented in the MC56F8323 from Freescale Semiconductor can be found in [42]. The SMPS is built with the same converter topology but in this case the control scheme for the phase shifted full bridge converter is a current mode control scheme.

Even though the MC56F8323 only operates at a clock frequency of 60 MHz, as opposed to the 100 MHz of the UCD9501, and the control scheme is more complex the MC56F8323 is still capable of handling the control scheme. However, the main difference

between the two DSCs is in the sampling time of the on-chip ADC which is 1.2 μs for the MC56F8323 and 160 ns for the UCD9501. The sampling time though is not the limiting factor because the duty cycle command, which is calculated based on the sampled values, is not used until the beginning of the following switching period. Both SMPS designs are very good examples of applications well-suited to DSCs and show just how powerful DSCs are.

9.3 Conclusion

Digital control of SMPSs or applications with multiple converters that needs to be controlled independently are obvious applications for DSCs. DSCs are quite expensive compared to analogue control ICs, but if factors such as PCB board space and advanced functionality is taken into consideration the DSC becomes a good alternative to analogue control.

Controlling a single low power DC/DC converter with a DSC is too expensive a solution and an ASIC designed for that specific purpose is a much better solution. The reason is partly that the customer pays for more than he or she needs when buying the DSC because it is a general purpose device that can be used in a variety of applications.

Software design in assembly language for DSCs can be quite complex because the instruction sets for DSCs have a much higher number of commands that needs to be understood than microcontrollers have. If the execution time is not a major concern in the design it will be possible to write the software in C thereby saving time and trouble. Software reuse is again an important part, which will make the effort spent on programming important compensator functions in assembly language pay off in the long run even though it is initially expensive to develop.

10 Customised Digital Control Solutions

High performance digital control for low voltage DC/DC converters has evolved from being a question of designing a stable control loop with no limit cycling on the output voltage and tight output voltage regulation to a state where control loop bandwidth and fast transient response are just as important design parameters. The two most important parts of a high performance digital control solution are a Digital Pulse Width Modulator (DPWM) with high resolution and a digital compensator implementation with short execution time to reduce the delay inherent in a digital control system.

The best way to get both things is with an Application Specific Integrated Circuit (ASIC) design because the ASIC is designed for the application at hand and is not a general purpose device. Unlike DSCs and microcontrollers where the design of the digital control scheme has to be adapted to the digital device the ASIC is designed to fit the desired specifications. ASIC design is an expensive solution, and it takes a long time to develop an ASIC for production. An FPGA is therefore the preferred choice of digital device for rapid prototyping since the design can be quickly changed through the software written in a Hardware Description Language (HDL) and tested again at virtually no cost.

The second half of the PhD project has focussed on developing a number of customised digital control solutions and to test them in an FPGA. The work covered the subjects DPWM and digital compensators as well as some ideas for the ADC which is an integral part of the digital control scheme.

10.1 DiSOM – Digital Self-Oscillating Modulator

The basic idea for the customised digital control solution developed as part of this PhD project started with a very simple digital modulator inspired by an analogue self-oscillating modulator used in audio amplifiers [80].

The Astable Integrating Modulator (AIM) is a very simple analogue circuit, and it turned out that the digital derivation of the AIM was just as simple. The idea was developed into a family of Digital Self-Oscillating Modulators (DiSOM). A patent application describing the DiSOM was filed in March 2006 (see appendix K).

The DiSOM is basically a closed loop control system that generates the PWM signal for the power converter without the use of an external carrier signal such a sawtooth or triangular signal generated by a counter. Thus unlike other digital PWM modulators the

DiSOM does not need an external carrier signal generated by a counter together with a comparator to provide a PWM signal but it generates its own carrier signal. In the DiSOM the PWM signal is normally generated by a digital comparator with hysteresis which is part of the self-oscillating loop.

The DiSOM is a free-running modulator and the advantage of that is that the delay from the time the duty cycle command is changed on the input of the DiSOM to the time it takes effect on the output is shorter than for other DPWMs. The DiSOM is primarily used in Voltage Mode Control (VMC) schemes but it can be extended to include Current Mode Control (CMC).

The DiSOM family can be divided into two different types of systems as described in appendix K. Type 1 modulators have a self-oscillating loop in which the feedback is taken at a switching node. The point of feedback can be either the output of the digital comparator with hysteresis or it can be a node voltage in the switch-mode converter sampled by an ADC. By using the output of the comparator with hysteresis as the point of feedback, the DiSOM becomes a purely digital modulator which greatly simplifies the practical implementation.

Type 2 modulators are single loop control systems for switch-mode converters which includes the 2^{nd} order output filter of the switch-mode converter in the self-oscillating loop. The point of feedback in type 2 DiSOMs is the output voltage and the feedback signal has to be sampled by an ADC. Because the type 2 DiSOM is a single loop self-oscillating control system it will have the highest possible control loop bandwidth that can be achieved for a switch-mode converter for a certain choice switching frequency. The open loop bandwidth is equal to the switching frequency of the converter since the crossover frequency is equal to the switching frequency for a self-oscillating control system.

Type 2 DiSOMs are unfortunately also the most complicated and expensive to implement, which limits their usefulness somewhat. The problem lies in the fact that digital implementation will have to sample the output voltage at a very high sampling rate in order to get good performance. The optimum solution is to sample the output voltage at the same rate as the clock frequency, which would be around the 50 -100 MHz in a typical system. A sampling rate that high not only places very high demands on the ADC but the digital implementation also has to be able to perform the control loop algorithm at the same rate.

A type 2 DiSOM is that it is self-oscillating because of the ripple voltage on the output of the switch-mode converter. The ripple voltage is amplified by the frequency dependent loop filters in the DiSOM and is fed to the comparator with hysteresis. The comparator changes state on the output whenever the amplified ripple voltage crosses either of the two levels at which the comparator changes state. Most DC-DC converters have a small ripple voltage and the ADC resolution would have to be high to be able to accurately detect the ripple which it must be able to do in order for the DiSOM to be self-oscillating.

Type 1 DiSOMs on the other hand can be quite simple to implement especially if they are implemented as a purely digital entity. The disadvantage of the type 1 modulator is that it requires an outer control loop if it is used in digital controller IC for a DC-DC converter. The reason is that the type 1 DiSOM only controls the PWM output and has no control of the actual output voltage. The type 1 DiSOMs implemented in a purely digital form can therefore be considered as a DPWM module comparable to other DPWM implementations described in section 7.1.

The most basic type 1 DiSOM modulator has been described in appendices D and E and used in two different DC/DC converter applications. The main advantages of the DiSOM are that the sampling frequency and update rate of the digital compensator can be higher than the switching frequency of the DiSOM and that the DiSOM is actually a separate control loop that can correct for quantisation errors on the PWM signal due to a limited clock frequency. Higher sampling frequency combined with a very short delay in the DiSOM modulator makes it possible to design a digitally controlled DC-DC converter with high bandwidth and fast transient response as described in appendices D and E.

Presenting the idea behind the DiSOM at conferences has shown that some further explanation of what is understood by a digital self-oscillating modulator is necessary for many people to understand it properly. A self-oscillating circuit is generally understood as a circuit that oscillates without being excited by an external clock signal. The DiSOM AIM (see Fig. 10-1) is a digital system with an external clock but the closed loop implementation of the DiSOM with the feedback path from the switching output and back to the input is oscillating, i.e. generating a PWM signal, at a frequency that is dependent on the configuration of the loop.

The oscillating/switching frequency of the DiSOM AIM of Fig. 10-1 as a function of the duty cycle command has been determined in appendix D by a simple time domain

calculation. The general definition of oscillation is the Barkhausen oscillation criterion which states that a closed loop system will oscillate at a certain frequency if the loop gain is equal to one, i.e. 0 dB, and the phase shift is ÷180° at that exact frequency. The Barkhausen oscillation criterion is valid for closed loop systems with negative feedback.

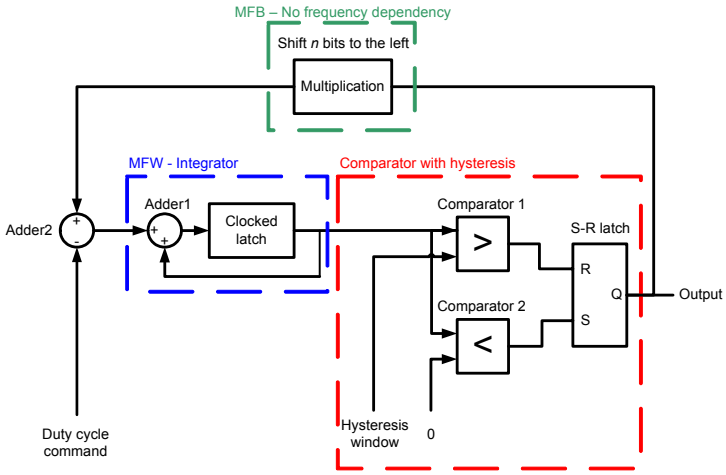


Fig. 10-1 Type 1 DiSOM AIM described in appendices D and E

The comparator with hysteresis which is an important component in the DiSOM AIM has a non-linear behaviour and the frequency response of the comparator is complex to calculate. It is therefore difficult to calculate the frequency response and make a Bode plot for the DiSOM AIM. It can however be simulated in MATLAB/SIMULINK.

A simulation of the loop gain for the DiSOM AIM mentioned in appendices D and E shows that the crossover frequency is approximately 500 kHz (D = 0.5) and the phase is ÷180° at the crossover frequency. The parameters used in the simulation are the same as those given for the DiSOM AIM in appendix E. The switching frequency of the DiSOM AIM was calculated to be 500 kHz according to the theoretical expression derived in appendix D. The DiSOM AIM therefore fulfils the Barkhausen oscillation criterion and can be considered a self-oscillating system despite the fact that it is a digital system with an external clock source.

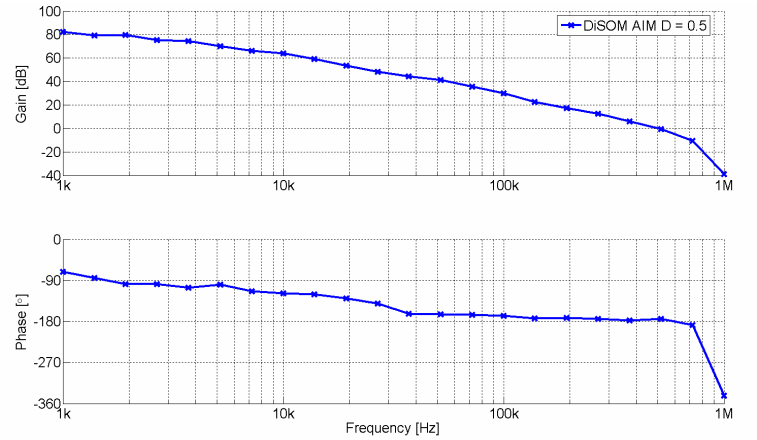


Fig. 10-2 Simulated open loop gain for DiSOM AIM

Fig. 10-3 and Fig. 10-4 shows block diagrams for two other type 1 DiSOMs that could be used as an alternative to the basic DiSOM AIM described in appendices D and E. In the DiSOM LP1 in Fig. 10-3 the integrator has been replaced by a first order IIR lowpass filter. The comparator with hysteresis has been changed with regards to the hysteresis window which is centered around zero. The actual implementation of the 'Gain' block has not been considered since this is only an example which has not been programmed in VHDL and synthesized for an FPGA.

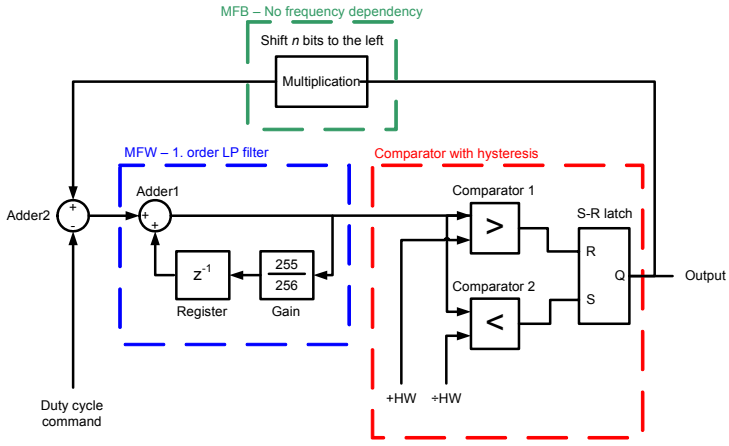


Fig. 10-3 DiSOM LP1 with lowpass filter as Main Forward Block

In Fig. 10-4 the frequency dependent block, which is necessary to make the DiSOM LP2 oscillate, has been moved from the forward path to the feedback path. The lowpass filter is the same as the lowpass filter of DiSOM LP1 except that the gain of the 'Gain' block has been changed. The most important difference is however that because the lowpass filter has a low-frequency gain dependent on the constant in the 'Gain' block the bit-width of

duty cycle command is different from the other two DiSOMs. The feedback block of the first two DiSOMs simply shifts the output of the comparator with hysteresis *n* bits to the left thereby multiplying by 2^n and the duty cycle command can take on values in the range from 0 to 2^n-*1* corresponding to the full duty cycle range from 0 to 1. In the DiSOM LP2 of Fig. 10-4 the duty cycle command can take on values between zero and the low-frequency gain of the lowpass filter.

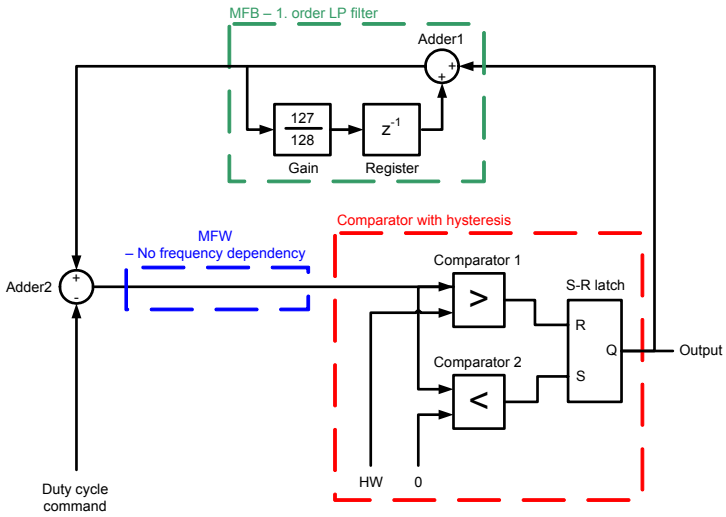


Fig. 10-4 DiSOM LP2 with lowpass filter as Main Feedback Block

SIMULINK models of the three DiSOMs described above have been made to compare the performance of the three designs. The hysteresis window for the three designs have been selected in such a way that the switching frequency for D = 0.5 is the same in all three cases. The switching frequency as a function of the normalised duty cycle command has been plotted in Fig. 10-5.

It is interesting to notice that DiSOM LP1 ceases to oscillate if the duty cycle command is below 0.05 or above 0.95. This is caused by a saturation of the lowpass filter output. If the difference between the feedback signal and the duty cycle command multiplied by the low-frequency gain of the lowpass filter is smaller than the hysteresis window the filter saturates and the DiSOM LP1 ceases to oscillate/switch. The saturation point is determined by the 'Gain' block which determines the low-frequency gain of the lowpass filter.

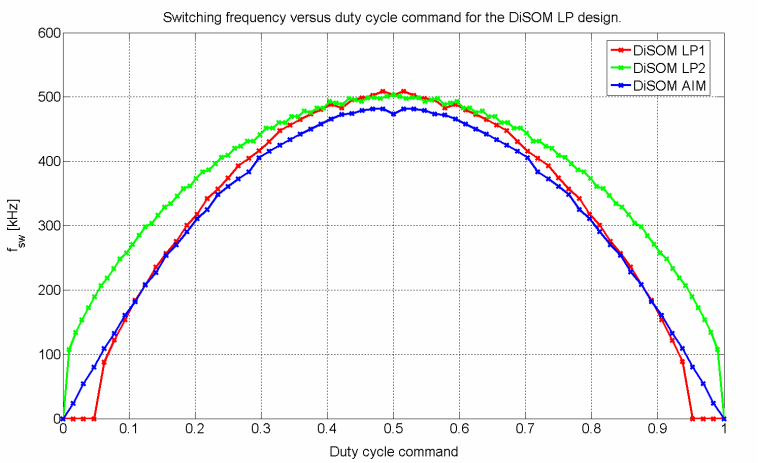


Fig. 10-5 Switching frequency versus duty cycle command for the three DiSOM designs

Fig. 10-6 shows the actual duty cycle of the three DiSOMs as a function of the normalised duty cycle command. The DiSOM LP1 for duty cycle commands between 0.05 and 0.95 and the DiSOM AIM have good linearity whereas the DiSOM LP2 design is somewhat non-linear.

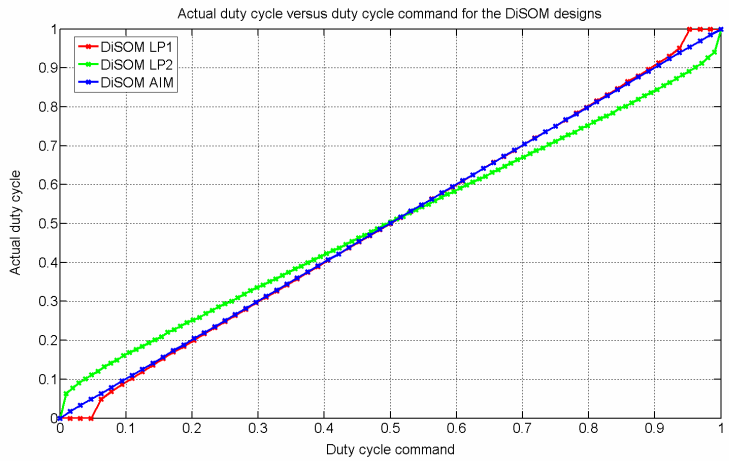


Fig. 10-6 Actual duty cycle versus duty cycle for the three DiSOM designs

The non-linearity of the DiSOM LP2 design does not necessarily exclude it from being used for digital control of DC-DC converters such as POLs and VRMs. The real problem related to both DiSOM LP1 and LP2 is that the minimum duty cycle is approximately 0.05. The dynamic response of the DC/DC converter will not be quite as good with the DiSOM LP1 or LP2 compared to the DiSOM AIM in case the digital compensator commands a duty cycle lower than 0.05. If a duty cycle command lower than 0.05 is given to the

DiSOM LP1 or LP2, the PWM signal would in practice be set low as long as the duty cycle command is lower than 0.05. The dynamic response to a load step would therefore not be slower because of the limited duty cycle range but the output voltage response might have a larger ringing when settling to its steady state condition because the DiSOM enters a non-linear mode of operation.

Fig. 10-2 shows that the loop gain of the DiSOM AIM has a -20dB slope from very low frequencies because of the integrator in the forward path. The DiSOM AIM will be able to suppress the quantisation noise caused by the limited clock frequency at low frequencies because of the high loop gain. The quantisation noise is still present but it is present at higher frequencies where the loop gain is low. This performance is similar to that of a Sigma-Delta modulator but unlike the Sigma-Delta the DiSOM does not impose a limitation on the sampling frequency of the digital compensator in order to perform well. The loop gain of DiSOM LP1 and LP2 on the other hand has a constant gain at frequencies below the cutoff frequency of the lowpass filters (see the Bode plots in Fig. 10-7). Therefore they will not be able to suppress the quantisation noise as well.

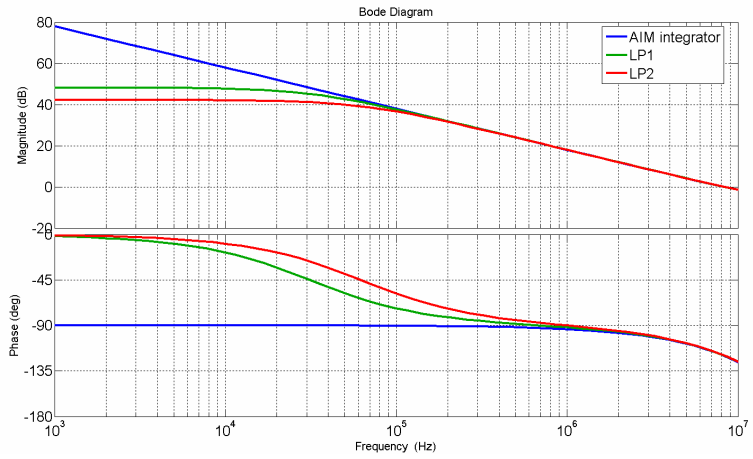


Fig. 10-7 Bode plots for the frequency dependent loop filters of the three DiSOM designs

It is however questionable if it will be possible to see any difference in the performance of the three DiSOMs once they are used in a control loop with an outer loop that controls the output voltage. The reason being that the outer loop almost always includes an integrator that will also help to suppress any output voltage errors caused by the quantisation noise which can be detected by the ADC.

10.1.1 Fixed switching frequency operation in the DiSOM

Interleaved Buck converters in VRMs and POLs are becoming increasingly popular as the output current levels are increasing and the supply voltage for CPUs and other digital devices at the same time is decreased. Interleaving several Buck stages requires that the DPWM module can generate PWM signals that are phase shifted relative to each other. The DiSOM family in it itself is a free running system with a variable switching frequency as described above and it cannot in its basic form be used to generate phase shifted PWM signals with a constant phase shift.

A solution to the problem of generating phase shifted PWM signals with the DiSOM has therefore been sought and was found. It involves constant frequency operation of the DiSOM. Constant frequency operation can also be advantageous in other applications where the duty cycle command can vary a lot because the output voltage is not constant but is changed dynamically. An example of an application with dynamically changing output voltage is a power supply for an RF power amplifier which has been described in appendix E.

A simple way to keep the switching frequency constant in a type 1 DiSOM is to change the hysteresis window as a function of the duty cycle command. This method has been described in appendix K and a block diagram of how it can be implemented is shown in Fig. 10-8.

An expression for the hysteresis window as a function of the duty cycle command if the switching frequency is kept constant is found by rearranging the expression for the switching frequency as a function of the duty cycle command given in appendix D. The hysteresis window can be calculated in real-time by the hysteresis window control block (HWC in Fig. 10-8) or it can be stored in a lookup table to simplify the digital implementation.

To reduce the size of the lookup table the duty cycle command can be divided up into intervals for which the same hysteresis window applies. The switching frequency will not be completely constant but the reduction in the memory required to store the lookup table is so great that it is worthwhile to make a compromise.

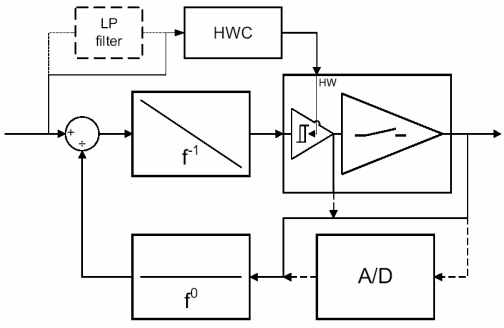


Fig. 10-8 DiSOM AIM with constant switching frequency

If a large change in the duty cycle command occurs, the hysteresis window may be changed by a large factor by the HWC. The DiSOM may in that case counteract the outer control loop generating the duty cycle command thus causing unstable operation because the signal stops switching for a longer period of time. An optional lowpass filter can be inserted between the HWC and the duty cycle command to prevent that. The lowpass filter may be as simple as an 2nd order moving average filter which calculates the average of the previous and the present duty cycle command.

Keeping the switching frequency constant is not enough to generate interleaved PWM signals with the DiSOM because it is only the frequency but not the phase of PWM signal that is controlled. Several solutions were considered to generate interleaved PWM signals with the DiSOM.

One solution is to use a PLL for the DiSOM of each phase in the interleaved converter. The PLL could control the hysteresis window dynamically to achieve constant frequency operation and the correct phase for each DiSOM module.

The solution that was chosen was to replace the comparator with hysteresis with a comparator with a synchronisation input. The comparator synchronises the positive transition of the PWM signal to an external pulse. The idea has been described in appendix K and was used to control an interleaved Buck converter with two phases. The interleaved Buck converter with two phases has been described in appendix F.

A DiSOM that has an external synchronising input is strictly speaking not self-oscillating and as result the performance of the synchronised DiSOM is not as good as that of the self-oscillating DiSOM. Synchronising the DiSOM creates the same delay as in a counter based DPWM. The sampling frequency of the compensator can still be higher than the switching frequency but that is also the case for an interleaved Buck converter controlled by a number of counter based DPWMs (see, for instance, reference 31). The

delay caused by the synchronisation of the DiSOM is a function of the duty cycle. The small signal model for a counter based DPWM expressed in the continuous time domain is given by equation 10.1 where D is the duty cycle and T_s is the time period of the PWM signal [81]. The small signal model shows that the DPWM introduces a negative phase shift at higher frequencies. That would also the case for the synchronised DiSOM.

$$G_{DPWM}(s) = K_{DPWM} \cdot e^{-s \cdot D \cdot T_s} \tag{10.1}$$

The synchronised DiSOM retains the advantage of being a closed loop system that corrects for quantisation errors although the performance in this respect is not quite as good as for the free-running DiSOM.

10.2 Digital compensator implementation in ASICs

The development of the DiSOM family started the process of designing a digital compensator in VHDL with a short execution time. The digital compensator is a key component in any high performance ASIC solution for two reasons. The first reason is that the time it takes to calculate the result of the compensator algorithm affects the control loop performance because it introduces a delay to the control loop. The second reason is that the complexity of the digital compensator implementation affects the die size of the ASIC and through that its cost. The complexity is related to the number of bits used to represent the signals internally in the compensator and how the compensator is realised.

The type of compensators considered in this chapter are Linear Time Invariant (LTI) systems, which in essence are digital IIR filters. The practical implementations of a digital compensator can vary quite a lot as discussed in section 7.3.3.1 of the State-of-the-art analysis and it has not been possible to compare all possible solutions because of limited time and resources.

Two basic compensator designs have been used in the prototypes described in appendices D, E, F and I. The compensator transfer function is the same for all the prototypes (see equation 10.2 below) except that the coefficients b_0, b_1, and b_2 were changed. The transfer function is also same as the one implemented in the microcontroller designs of appendices B and C.

$$G_{Comp}(z) = \frac{d(z)}{e(z)} = \frac{b_0 + b_1 \cdot z^{-1} + b_2 \cdot z^{-2}}{1 - z^{-1}} \tag{10.2}$$

In the first compensator implementation, which was used in appendices D and E, the compensator was implemented with a lookup table. In the second implementation used in appendices F and I a Multiplier/Accumulator module (MAC) was used.

The lookup table is used to store the results of the multiplication of the three error signals and the three coefficients of the transfer function. The lookup table design was chosen because it was thought that the MAC module would be too expensive in an ASIC implementation to be sold commercially. Another reason for choosing to use a lookup table was that the FPGA that was chosen for the design had a small memory block that can be configured as Read Only Memory (ROM) which made it easy to implement the lookup table in the FPGA.

The FPGA that was used is the LCMXO1200C CPLD/FPGA from Lattice Semiconductor which is actually a hybrid between an FPGA and CPLD [82]. The LCMXO1200C is not a large FPGA with on-chip hardware multipliers prepared for DSP applications but it has been sufficient for the digital control solutions that are described in the present thesis and its appendices.

A block diagram and timing diagram along with a detailed description of how the compensator is designed is given in appendix D. The compensator described in appendix D has an internal word-length of 18 bits and the memory requirements for the lookup table is 432 bytes.

The details of the second compensator implementation can be studied in appendix F. It is a traditional IIR filter implementation with a MAC module known from digital signal processing. The design utilizes the idea of an asymmetrical hardware multiplier with different word-lengths for the two inputs described in reference 65. The design is otherwise very similar to the one with the lookup table.

Table 10-I shows a comparison of the compensator based on the lookup table (LUT) and the compensator based on the multiplier/accumulator (MAC). The total execution time is the time it takes the FPGA to complete the full compensator algorithm. It is longer for LUT implementation because the lookup table has to be addressed in one clock cycle before the contents can be read in the following clock cycle. The total execution time is only of interest if extremely high sampling frequencies are considered. The maximum sampling frequency that can be sustained with the MAC based implementation is thus $1/6^{th}$ of the clock frequency. More important is the actual delay from the time the ADC output is

read to the time the compensator updates the duty cycle command. This delay is very short for both implementations designs which shows that they are both suitable for high performance digital control.

	LUT compensator	MAC compensator
Total execution time	10 clock cycles	6 clock cycles
Delay from reading ADC result to update of D	3 clock cycles	2 clock cycles
Number of SLICEs in FPGA	72	123
Non-volatile memory usage	432 bytes	36 bits (4.5 bytes)

Table 10-I Comparison of LUT and MAC based PID compensator implementations in the LCMXO1200C

The number of SLICEs utilized in the FPGA is a measure of the complexity of the digital logic of the compensator design. A SLICE in the LCMXO1200C (see Fig. 10-9) consists of two 4-bit LUTs, which can perform any logic function for a 4-bit input and two latches/registers as outputs. The SLICEs can be combined to make digital arithmetic units or any other logic function that is necessary. The number of SLICEs utilized by the MAC compensator is 71% higher than that of the LUT compensator.

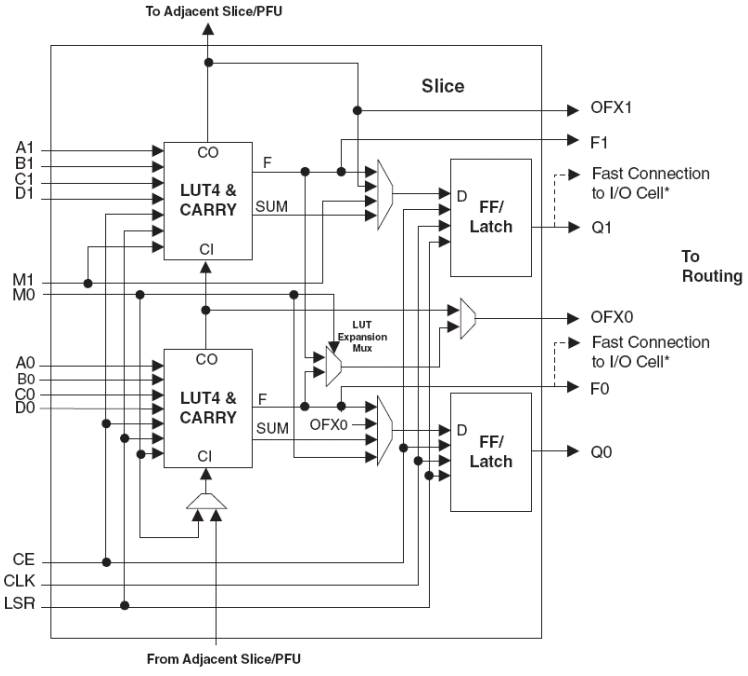


Fig. 10-9 Block diagram of a SLICE in the LCMXO1200C [82]

The memory usage on the other hand is almost a 100 lower times for the MAC compensator than for the LUT compensator because the MAC compensator only needs to

store the three coefficients b_0, b_1 and b_2 in non-volatile memory whereas the LUT compensator stores an 18 bit value for each possible error value.

The MAC compensator is preferable because it has a shorter execution time and because non-volatile memory is quite expensive to include on an IC. The fact that the memory requirements is so much smaller in the MAC compensator easily makes up for the increase in logic especially since 123 SLICEs is quite a small amount of logic. Another advantage of the MAC compensator compared the LUT compensator is that it is easy to reprogram the three coefficients to change the frequency response of the compensator.

If a shorter execution time is a requirement then parallel processing with multiple hardware multipliers is a possible solution. Parallel processing is achievable at the cost of a more expensive digital implementation. The MAC compensator also has the advantage that it is relatively simple to change the transfer function to include more poles or zeros without increasing the complexity too much.

10.3 Analogue to Digital Converters for High Performance Digital Control ICs

Selecting an Analogue to Digital Converter (ADC) for high performance digital control of low voltage DC/DC converters is a compromise between sampling frequency, sampling time, input voltage range and power consumption. The sampling rate is in most control schemes for DC/DC converters not higher than 1-2 MSPS for converters switching at 1-2 MHz. Sampling rates of 1-2 MSPS can be achieved with a successive approximation (SAR) ADC. SAR ADCs have excellent linearity and low power consumption but the sampling time is quite long compared to the sampling frequency. Take for example the TLV571 from Texas Instruments. It is an 8-bit SAR ADC with a sampling rate of 1.25 MSPS and the sampling time is 800 ns. The TLV571 was used together with a microcontroller (ATTiny26) in appendix G and the sampling time of the ADC did not have a negative impact on the performance because the execution time of the compensator algorithm in the microcontroller was much longer than the sampling time. If on the other hand the TLV571 was used together with the digital compensators described in section 10.2 the sampling time would be the dominant delay in the control loop. Short sampling time in the ADC is therefore essential to be able to fully utilize the digital compensators and DiSOM modulators previously described.

The FPGA development board used in the experiments performed with the DiSOM solutions was designed by the author of the present thesis. The ADC that was mounted on

the development board was a 10-bit pipelined ADC that has a sampling time equal to six clock cycles. The sampling time of a pipelined ADC depends on the number of pipeline stages and the clock frequency of the ADC. The pipelined ADC contributed the largest delay in the customised digital control solutions described in appendices D and E even though a sampling time of six clock cycles with a clock frequency of 50 MHz is a very short delay. If the full potential of the digital compensator and DiSOM are to be realised it is necessary to have an even faster ADC.

A flash ADC can sample the analogue voltage in a single clock cycle. The flash ADC (see the block diagram in Fig. 10-10) is composed of a number of comparators comparing the input voltage with different voltage levels generated by a resistor ladder and a logic decoder block that generates the appropriate digital word. The two reference voltages at the top and bottom of the resistor ladder sets the input voltage range of the flash ADC. The output of the logic decoder can be read once every clock cycle by the digital compensator which makes the sampling time equal to a single clock cycle.

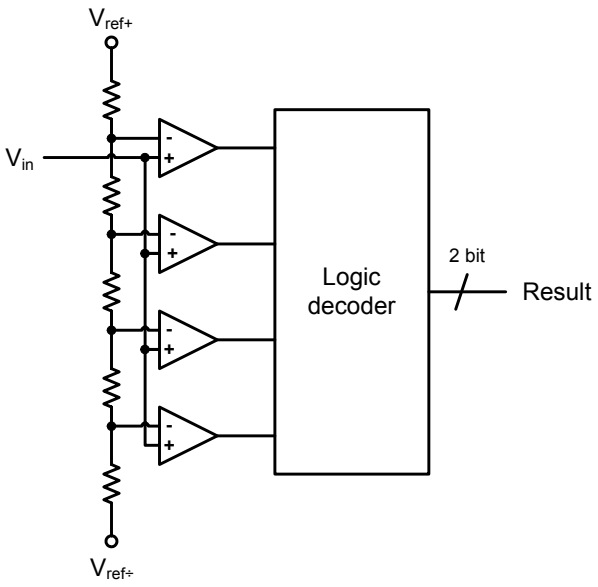


Fig. 10-10 Block diagram of 2-bit flash ADC

The drawback of the flash ADC is the power consumed by the resistor ladder and the comparators. The higher the input bandwidth of the comparators has to be the higher is the power consumption of the comparators. The resistance of the resistor ladder influences the linearity of the flash ADC where the linearity is improved if the resistance is reduced. Reducing the resistance unfortunately increases the power consumption of the flash ADC.

The flash ADC is the best choice of ADC for customised digital control solution for POLs and VRMs because of the short sampling time. The drawbacks are higher power consumption and a higher price since the chip area needed on an ASIC for the resistor ladder can be quite large. The pipelined ADC is a good alternative to the flash ADC and it will in most cases be sufficient to use a pipelined ADC to achieve acceptable control loop performance.

10.3.1 Non-linear ADCs

ADCs in traditional industrial and consumer applications have linear characteristics over a large input voltage range to accommodate the requirements in that type of applications. The idea of non-linear ADCs for digital control of switch-mode converters has been explored in a publication [83] and a patent [84]. The general idea is to improve the performance of the digital control solution and/or reduce the cost of the digital control device by simplifying the ADC design. Non-linear ADCs are only relevant for ASIC designs since non-linear ADCs can not be bought of the shelf and that the type of non-linear behaviour that is desired may vary from one design to the next which makes it unprofitable for companies to manufacture non-linear ADCs since the sales numbers will be small.

Reference 83 proposes what is termed a windowed ADC which has small quantisation steps, i.e. high accuracy, in a voltage range or window centered around the reference voltage for the output of the switch-mode DC/DC converter. The quantisation steps are increased as the input voltage to ADC is further away from the reference voltage. The windowed ADC allows the digital control scheme to accurately control the steady state output voltage but also to detect larger output voltage deviations from the steady state condition in coarser quantisation steps.

The windowed ADC is intended to be an extension of traditional linear flash ADCs with a limited input voltage range. The number of comparators in the windowed ADC is reduced compared to the number of comparators in a linear ADC with a quantisation step equal to the small quantisation step of the windowed ADC but with the same input voltage range. The windowed ADC is therefore cheaper to manufacture and has a lower power consumption than a linear ADC.

The customised digital controller designed for a power supply for an RF power amplifier described in appendix E uses the idea of the windowed ADC. The actual ADC used in

appendix E was a pipelined ADC and the non-linear behaviour was implemented with a special decoder logic in the VHDL design for the digital compensator. The reason for using a non-linear ADC decoding scheme was that the compensator was implemented with a lookup table. The size of the lookup table was limited by the memory available in the FPGA. The non-linear ADC decoding was the only way to be able to use the compensator based on a lookup table and at the same time have a large error range to get a fast dynamic response. Fig. 10-11 shows the relationship between the input voltage of the ADC and the digital error signal used for the non-linear decoding scheme used in appendix E. The decoding scheme was divided into intervals with varying quantisation steps to get the optimal performance with the smallest possible number of quantisation steps.

There is an infinite number of possible decoding schemes for the windowed ADC which can be chosen according to the requirements in any particular control IC.

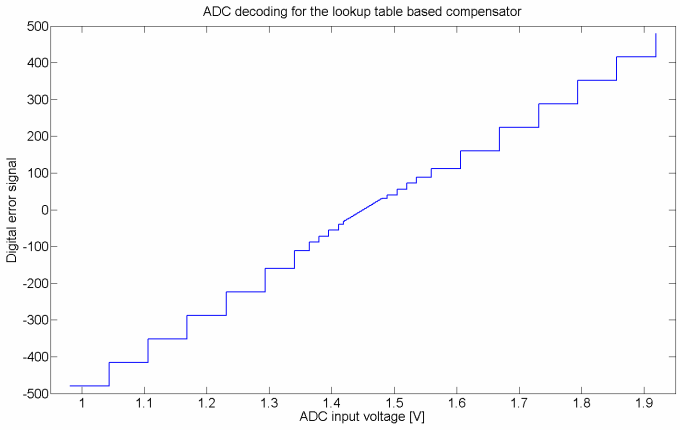


Fig. 10-11 Digital error signal versus input voltage for a windowed ADC (see appendix E)

10.4 Interleaved Buck converter with efficiency improving control scheme

Appendix I describes the design of an interleaved Buck converter with a digital control scheme intended to optimize the efficiency of the converter over the full load range. The work was carried out during a three month visit at the Universidad Politecnico de Madrid (UPM) and was considered as a part of the PhD project at the Technical University of Denmark.

The efficiency of an interleaved Buck converter is generally low at low load currents because of the switching losses in each separate phase of the interleaved Buck converter. The efficiency optimization scheme controls the number of active phases in the interleaved

Buck converter as a function of the load current. At low load current the number of active phases is reduced to achieve a high efficiency.

The advantages of a customised digital control solution are obvious for this kind of application. The digital control scheme can measure the output current and decide when to change the number of active phases. It can also control the phase shift between the active phases to achieve the minimum ripple voltage on the output.

The interesting thing about the work described in appendix I is the predictive current sharing scheme. The purpose of the predictive current sharing scheme is to ensure that the average current, i.e. the DC current level, in all active phases is equalised in one or two PWM periods after the number of active phases have been changed without having to measure the DC current level in each phase.

Fig. 10-12 is a block diagram of the DPWM module for the interleaved Buck converter where the number of active phases can be changed. The PWM signals for the interleaved Buck converter are generated by a counter based DPWM module with separate counters for each phase. Each comparator receives a separate duty cycle command which is the sum of the duty cycle command calculated by the digital compensator and a duty cycle command calculated according to the predictive current sharing scheme. When the 'Phase control' block makes a decision to change the number of active phases it changes the phase shift of the active phases. At the same time the digital control scheme calculates the extra duty cycle command for each active phase to ensure equal DC current in all phases.

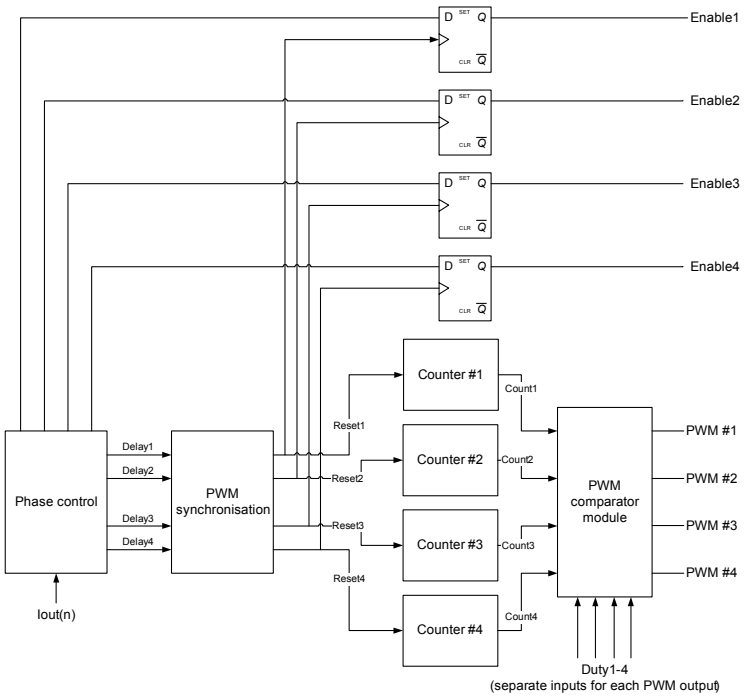


Fig. 10-12 Block diagram of the DPWM module for the interleaved Buck converter described in appendix I

The predictive current sharing scheme could be implemented in a DSC but the freedom to design the system without any limitations imposed by the choice of digital device makes it much easier to design the best possible solution in a customised digital control solution.

10.5 Conclusion - Digital versus Analogue Control

The main purpose of the work presented in this thesis has been to find digital control solutions with a performance equal to the performance of analogue control. The customised digital control solution with the DiSOM modulator has been the best solution out of the different solutions described in this thesis. So how well does the customised digital control solution perform compared to the traditional analogue control solutions?

A student at the Technical University of Denmark build two prototype POL converters with a Buck converter identical to that described in appendix D but with analogue control. The first prototype used a standard VMC control IC (TL5001) from Texas Instruments and the second design was built with a customised analogue design. The customised analogue control solution used a 150 MHz operational amplifier as an error amplifier.

The results of the comparison can be found in appendix H. It was found that performance of the customised digital control solution with the DiSOM is comparable to that which can be achieved with the TL5001. The limitation in the analogue control design is the error amplifier in the TL5001 which has Gain-Bandwidth product of 1.5 MHz. Analogue control ICs with a Gain-Bandwidth product of up to 15 MHz can be bought but simulations showed that the improvement in performance that is gained is insignificant.

The performance of the digitally controlled converter was to some extent limited by a poor hardware implementation. The ADC was as already mentioned mounted on the FPGA development board and the output voltage feedback signal is connected from the converter PCB to the FPGA development board by a coaxial cable. The performance of the design can be improved by mounting the ADC close to the converter output on the converter PCB and transfer the logic signals from output of the ADC by a cable. Logic signals are much less sensitive to noise and the converter performance should be improved which would make it possible to increase to the bandwidth of the digitally controlled converter.

The customised analogue solution had a performance that was significantly improved compared to digital control ICs. It can therefore be concluded that LTI digital control still cannot perform quite as well as an optimised analogue solution. It should be taken into account that the customised analogue solution is not a feasible solution for industrial

purposes as it is quite expensive because of the 150 MHz operational amplifier and a number of other components necessary to make it work.

11 Conclusions

The work presented in this thesis shows the broad scope of digital control for switch-mode power converters and the almost infinite number of ways that it can be realised. The idea has been to investigate the three different solutions for digital control of switch-mode power converters to ascertain which type of solution that is best suited for a particular application.

Microcontrollers are cheap digital devices with a CPU core and important peripherals such as PWM modules and Analogue to Digital Converters (ADCs) in a single device. The type of microcontrollers that have been considered in this thesis for real-time control of switch-mode converters are low cost devices with only a few I/O pins that operate at relatively low clock frequencies.

Software design is the most important issue when designing a digital control scheme with a microcontroller because of the limited computational resources. Programming the important compensator algorithm in assembly language rather than in a high level programming language such as ANSI C can reduce the execution time 3 to 4 times for an ATMEL AVR microcontroller. The compensator algorithm was programmed using lookup tables because the microcontroller did not have a hardware multiplier to perform multiplications.

Microcontrollers are best suited for applications with low performance requirements in terms of control loop bandwidth. Examples of that are PFC pre-regulators and off-line DC-DC converters. Mixed signal control schemes that combines a microcontroller and a few simple analogue components is a good way to improve the performance that can be achieved with a microcontroller.

The execution time of the compensator algorithm could be reduced dramatically by using a 16-bit microcontroller instead of the 8-bit microcontrollers that have been used in the work presented in this thesis.

If the author of this thesis should design the optimal microcontroller for real-time control of a switch-mode converter it would have a 16-bit CPU core, a fast ADC and it should be able to operate at a clock frequency of 100 MHz or more. A useful feature to add to the optimal microcontroller apart from the basic features of the microcontroller is a serial communications interface. The serial interface can be used to supervise the status of the switch-mode converter and program important control loop parameters.

Digital Signal Controllers are more powerful devices than microcontrollers and they are therefore better suited for real-time control of switch-mode power converters. DSCs have a Multiplier/Accumulator (MAC) module as part of the arithmetic logic unit in the CPU core. The MAC module enables the DSC to execute the compensator algorithm much faster than a microcontroller can. The ADC module in a DSC is capable of sampling at a higher rate than that of an ADC in a microcontroller. DSCs are however also more expensive than microcontrollers and they have a larger power consumption.

DSCs are very versatile because of their capability of performing complex arithmetic functions and can be used in uninterruptible power supplies, inverters in motor drives and switch-mode power supplies.

DSCs are well-suited for digital control schemes with multiple control loops that requires a large number of computations to be performed. The best example of control scheme with multiple loops is a control scheme for a switch-mode power supply with a Boost converter input stage with PFC and an isolated DC-DC converter to generate the tightly regulated output voltage. The advantage of the DSC in this type of application is that it is capable of handling the digital control scheme and at the same time will be able to handle added functionality such as UVLO and other features that a power supply must have.

The strength of DSCs are their versatility but that is also a weakness when it comes to developing a digital control scheme for a DSC. The assembly languages of DSCs include a large number of instructions and it requires an expert in programming to utilize the full potential of a DSC. An alternative would be to use a more expensive DSC that will be able to the same performance with ANSI C programming as the cheaper DSC does with assembly programming.

Customised digital control solutions for switch-mode power converters span a very broad range of solutions. They give the design engineer the freedom to select any solution that is found to give the best possible performance.

Customised digital control solutions are best suited for ASIC implementations to be sold in high volume markets for two reasons. The first reason is that the development costs for an ASIC are high which means that the ASIC must be sold in large numbers to cover the development costs. The second reason is that the production costs for an ASIC are decreased if a large volume is manufactured in a single batch. Digital control ICs for

interleaved Buck converters used in either Point of Load (POL) converters or Voltage Regulator Modules (VRMs) are the best example of ASICs designed for very high volume markets. Other markets such as the control of certain popular switch-mode converter topologies may be considered in the future if the market is big enough.

A high performance digital control solution for a low voltage DC-DC converter requires a good Digital Pulse Width Modulator (DPWM), a digital compensator that can calculate the duty cycle command very fast and an ADC with a short sampling time and high resolution.

The Digital Self-Oscillating Modulators that are proposed in this thesis is a family of digital control schemes for a switch-mode power converter. The DiSOM is a closed loop system that oscillates/switches at a frequency determined by the configuration of the DiSOM, that is with no external carrier signal to set the switching frequency. The DiSOM can be used as a DPWM block in a digital control solutions and has the advantage that it has a shorter delay than other DPWMs. Another advantage of the DiSOM is that it allows the sampling frequency of the digital compensator to be higher than the switching frequency. The DiSOM used as a DPWM is a simple digital implementation which requires a small amount of logic which makes it a low cost solution.

A simple digital compensator with short delay from the time the result on the ADC is read to the time that the compensator updates its output can be implemented in digital logic with a single MAC module or a lookup table stored in flash memory. The cheapest solution and the one with the shortest delay is the compensator with the MAC module because it requires a much smaller amount of flash memory than the compensator with the lookup table.

The choice of a fast ADC can be either a pipelined architecture or a flash architecture. The advantage of the pipelined ADC is that it has good linearity over a large input voltage range and a relatively low power consumption. The flash ADC has the advantage of the shortest possible sampling time but at the cost of high power consumption and typically a small input voltage range. The input voltage range of a flash ADC can be extended by designing a windowed ADC which does not have the same resolution over the full input voltage range.

The purpose of the Innovation PhD project presented in this thesis was to come up with high performance and low cost solutions for digital control of switch-mode power converters. The question is: how far did the project get towards meeting these goals?

The DiSOM used as a DPWM is the best performing digital solution of this thesis. The performance of this is comparable to an analogue control scheme implemented with a commerically available control IC. However, the performance of the analogue system can however be improved by designing a better control circuit whereas the limits of the digital design seems to have been reached.

The price of the customised digital control solution is hard to judge from a VHDL design synthesized for an FPGA. An ASIC design is under development but is has not been finished. It is therefore hard to tell what the final chip area and cost is going to be. Preliminary work on the ASIC based on the DiSOM and MAC compensator design nevertheless does show that the IC implementation will be quite small and that it should be competitive compared to other digital control ICs for single phase Buck converters.

The future of digital control for switch-mode power supplies and converters seems to be high volume markets such as digital control ICs for Voltage Regulator Modules and Point of Load converters. Another market where digital control will be adopted by the power electronics is AC/DC rectifiers for telecommunication and server applications. In the long term digital control may replace analogue control in almost any market. However, that will only happen if digital control ICs that are cheaper than analogue control ICs are developed. What is most likely to happen is that a new generation of mixed signal control ICs, which combines the best of the two worlds, will emerge for price sensitive markets.

12 Suggestions for future work

The main chapters of this thesis and the appendices relates to the practical issues of digital control of switch-mode power converters. It is therefore primarily the digital hardware and software designs that have been described in the thesis and the appendices instead of a theoretical study of digital control of switch-mode power converters.

One subject that it would be interesting to investigate is theoretical modelling of the DiSOM family. A theoretical small-signal model of the DiSOM would make it possible to accurately predict the performance of a DiSOM without having to do time consuming simulations in MATLAB/SIMULINK.

The customised digital control schemes based on the DiSOM are considered so promising that a research assistant have been employed by the Technical University of Denmark to develop an ASIC. The aim is that the ASIC will include a DiSOM modulator, a digital compensator and a flash ADC. The work has not finished at the time this thesis was written but some results have already been obtained. The results so far show that the size of the digital compensator will be 330 μm by 290 μm in a 0.35 μm CMOS process from Austrian Microsystems (C35B4C3). The DiSOM AIM will have a size of 160 μm by 170 μm.

A second generation of the ASIC design should, in addition to the main components mentioned above, also include an 8-bit CPU core and a slower ADC as well as an I^2C interface to support a communication protocol such as the PMBUS™. By adding these features to the ASIC it will be prepared to handle some digital power management which will make it more interesting for the power electronics industry.

Digital power management is in itself an interesting subject that is closely related to digital control of switch-mode power converters. Digital power management has not been studied in the PhD project presented in this thesis but it would be natural to extend the studies to digital power management in the future.

From a more general point of view, another area of interest is system identification and auto-tuning for the digital control loop in order to optimize the open loop transfer function. One interesting application for auto-tuning is Point of Load converters (POLs) that are typically sold with a small output capacitance in the POL-module and where the customer may add more capacitance on the output. Auto-tuning can adjust the compensator transfer

function coefficients to achieve an optimal crossover frequency and gain margin for the digitally controlled POL independent of how much output capacitance is present. Auto-tuning is probably one of the strongest arguments for making the change from analogue to digital control because auto-tuning adds value to the digitally controlled switch-mode power converter. The added value, which can not be obtained with analogue control, can convince the industry to change even though the digital solution is more expensive than the analogue solution.

Auto-tuning in a digital control scheme with the DiSOM could perhaps also change the sampling frequency to achieve the optimal compensator configuration. Using the sampling frequency as a tuning parameter would however require an accurate model of the DiSOM and how the control system responds to changes in the sampling frequency.

13 References

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14 Cross reference for chapters and appendices

Fig. 14-1 shows a graphical representation the three main chapters of the thesis and which appendices that should be read together with the chapter.

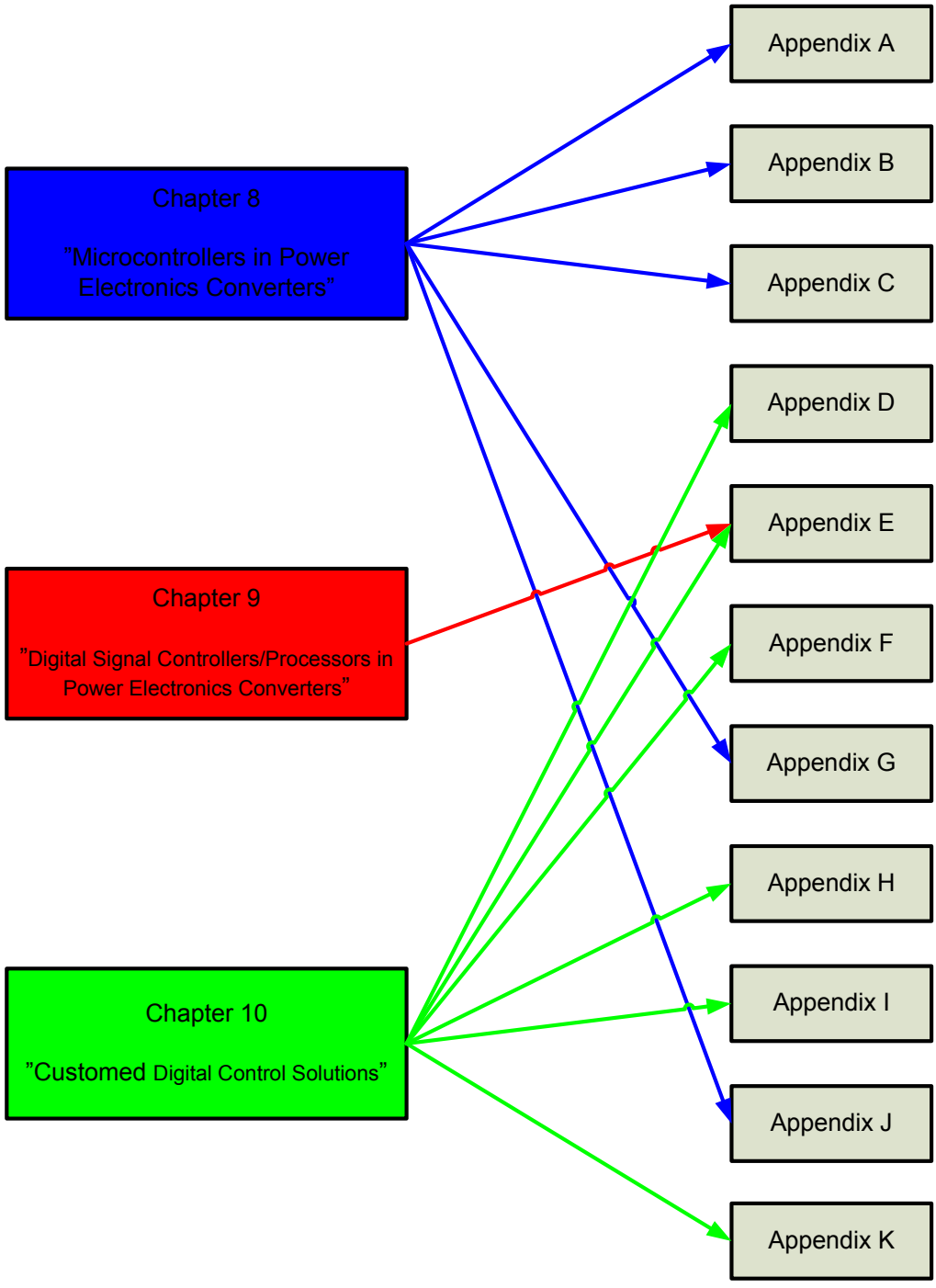

Fig. 14-1 Cross reference for chapters and appendices

15 Appendix A – Publication by L. T. Jakobsen et al.

Lars T. Jakobsen, C. Wolf, N. Nielsen and M. A. E. Andersern

"Hybrid Control Method for a Single Phase PFC using a Low Cost Microcontroller"

IEEE Applied Power Electronics Conference 2005, vol. 3, pp. 1710 – 1715, 2005

Hybrid Control Method for a Single Phase PFC using a Low Cost Microcontroller

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***Abstract*- This paper presents a hybrid control method for single phase boost PFCs. The high bandwidth current loop is analog while the voltage loop is implemented in an 8-bit microcontroller. The design focuses on minimizing the number of calculations done in the microcontroller. A 1 kW prototype has been designed and tested.**

I. INTRODUCTION

The use of digital control for power electronics converters is a fast growing field of research. The use of powerful DSPs or FPGAs are common but the added system costs is generally so high that the improvements gained by using digital controls mostly can not justify the added system cost.

The idea of controlling a PFC digitally has been discussed in several papers. The most recent designs are based on a high speed DSP [1, 2] or a FPGA [3] and feature different techniques to eliminate the problem of input current distortion due to the propagation of the output voltage ripple through the feedback circuitry. A different approach to implementing digital control of a PFC is to let the inner control loop which controls the input current be analog while the outer control loop is digital [4]. The design presented in [4] uses an UC3854 for the current loop together with a multiplying DAC to generate the input current reference. The outer loop is implemented in a 80C196 microcontroller.

In this paper a simple hybrid control scheme for a 1 kW PFC based on a boost converter is presented. The design is based on an 8-bit PIC microcontroller and the analog control circuitry is build using cheap standard components. The digital control scheme implemented in the microcontroller utilizes as little as 4.8 % of the microcontrollers computing power.

II. THE HYBRID CONTROL SCHEME

The control scheme proposed in this paper is illustrated in Fig. 1. The control scheme is similar to the control scheme implemented in the analog controller UC3854 with an inner control loop controlling the input current and an outer control loop controlling the output voltage. The input current must be proportional to the input voltage to obtain a power factor close to 1. The voltage loop controls the input power of the PFC by adjusting the amplitude of the input current. To ensure a low distortion of the input current the control signal from the voltage loop must be constant for at least half a period of the input voltage during steady state operation.

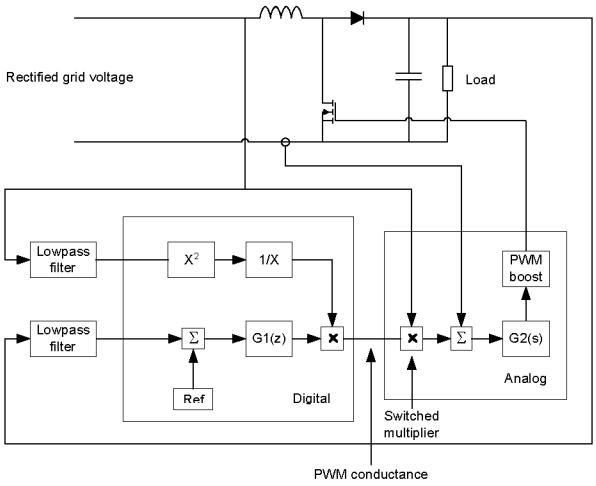

Figure 1 Proposed control scheme for a hybrid control of a PFC

The goal of this design is to use a digital microcontroller in the outer voltage loop. The reason for implementing the voltage loop controller in a microcontroller is to avoid the variations in the gain of the analog hardware multiplier that generates the input current reference signal in devices such as the UC3854 from Texas Instruments.

The implementation in the microcontroller must be optimized for a short execution time and low sampling frequency to minimize the load on the microcontroller. The idea is that the same microcontroller must be able to control a second converter connected to the PFCs output in a purely digital form with a high closed loop bandwidth. The current control circuit is analog because of the high bandwidth (typically 20 kHz) of the current control loop. If the current control is implemented in the microcontroller a sampling frequency of at least 200 kHz is necessary. The input current is controlled using average current mode control.

III. THE CURRENT CONTROL LOOP

The inductor current in the boost converter is controlled using average current mode control. The current is sensed with

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a resistor and compared to the current reference signal. The reference signal for the input current is generated in a switched multiplier (see Fig. 2). The switched multiplier is controlled by the PWM signal 'PWM conductance' generated by the microcontroller.

The gain of the switched multiplier is adjusted by changing the dutycycle, D, of the PWM signal. The low frequency gain of the switched multiplier is

$$G_{sw,mult} = \frac{v_{ref}(t)}{v_{in}(t)} = \frac{(1-D)\cdot R2}{R1+(1-D)\cdot R2} \qquad (1)$$

The expression for the low frequency gain has been found using circuit averaging over one period of the PWM signal. The lowpass filter on the output of the switched multiplier consisting of R3 and C2 reduces the switching ripple on the input current reference signal. The transfer function of the switched multiplier has two poles both of which are placed at 2.5 kHz. If the poles are placed too low the reference signal will be distorted compared to the rectified grid voltage resulting in increased input current distortion.

The PWM oscillator circuit for the boost converter is synchronized with the 'PWM conductance' signal controlling the switched multiplier to avoid subharmonic oscillations in the current control loop.

IV. The Voltage Loop

The design of the voltage loop is based on the model in Fig. 3. Two types of compensators were considered for the voltage loop. The P compensator has the advantage of a faster stepresponse at loadsteps than the PI compensator but has the disadvantage that the output voltage decreases when the load power increases. The higher the proportional gain is the smaller the voltage drop on the output voltage will be with increasing load.

The output capacitor adds - 90° to the phase of the open-loop transfer function of the voltage loop. If a PI compensator is used the total phase is -180° at frequencies below the compensators zero. The system will be unstable if the open-loop gain is larger than 1 and the phase is equal to -180°.

The P compensator was chosen because it is simpler to implement in the microcontroller and thereby utilizes less of the microcontroller's computing power than the PI compensator. Another reason is to avoid the instability of the voltage loop at low frequencies with a PI compensator.

To reduce the distortion of the input current a lowpass filter is added in the feedback of the output voltage. The filter can be either an analog filter on the input of the A/D converter sampling the output voltage or a digital filter implemented in the microcontroller. The advantage of using an analog filter is a low utilization of the microcontroller because the microcontroller doesn't have to complete a filtering algorithm. The advantage of the digital filter is that the filters transfer function doesn't change with the temperature or over time.

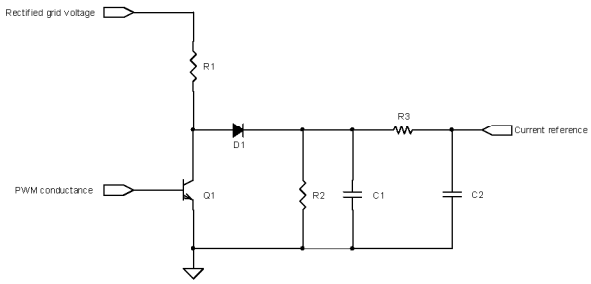

Figure 2 Switched multiplier

An analog first order filter and a digital first order IIR filter were considered in the design of the voltage loop. A description of both kinds of filters is given in the following paragraphs.

A. Analog first order filter

The analog first order filter is easily realised by adding a capacitor in parallel with the bottom resistor in the voltage divider which reduces the output voltage to a level that the microcontrollers A/D converter can measure. A schematic of the analog first order filter is shown in Fig. 4.

The cutoff frequency of the analog filter is placed at 15 Hz leading to a phase margin of 27° and an open loop crossover frequency of 30 Hz for the voltage loop.

B. Digital first order IIR filter

The proposed IIR filter has the transfer function

$$H_{IIR}(z) = \frac{1-a}{1-a\cdot z^{-1}} \qquad (2)$$

The pole/zero plot for the digital filter is shown in Fig. 5. The filter has a zero at the origin and a pole determined by the constant a. The closer a is to 1 the lower the filter's cutoff frequency is.

A simple implementation of the digital filter in the program code for the microcontroller is of great importance to ensure a low utilization of the microcontrollers computing power. The digital IIR filter can realized as shown in Fig. 6.

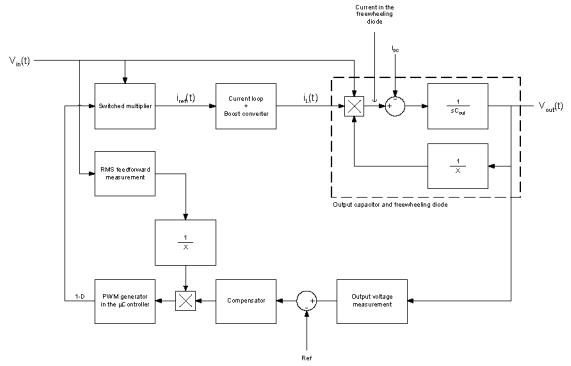

Figure 3 Model of the voltage loop

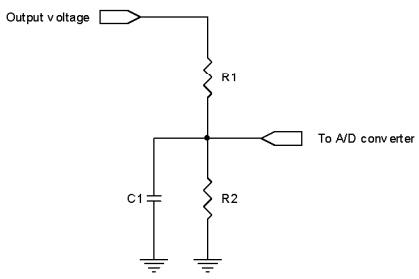

Figure 4 Analog first order lowpass filter

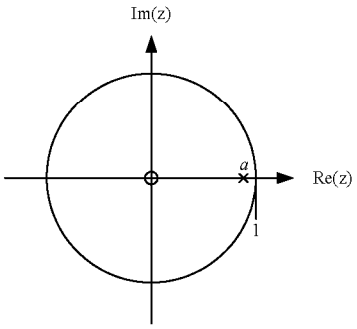

Figure 5: Pole/zero plot for the first order IIR filter

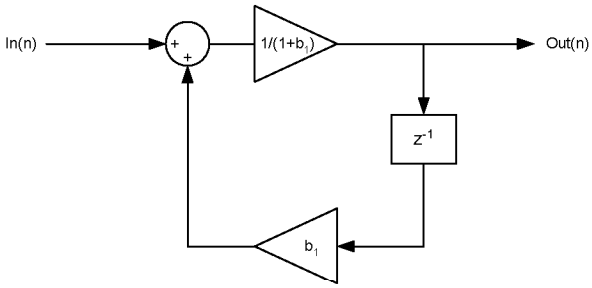

Figure 6 Realization of the digital IIR filter

The factor b_1 in the implementation of the IIR filter is selected as a power of 2 to enable the microcontroller to do the multiplication by shifting routines. The other multiplication is implemented as a division. The placement of the pole of the filter is limited by this implementation but it greatly simplifies the program code for the microcontroller and thereby reduces the utilization of the microcontroller's computing power.

In the final implementation of the voltage loop using the digital filter the pole of the IIR filter has been placed at $a = 8/9$ which results in a phase margin of 24° and a crossover frequency of 24 Hz.

C. Feedforward of the RMS value of the grid voltage

To ensure a constant gain in the voltage loop the control signal on the output of the compensator is divided by the square of the input voltage RMS value. Several methods for calculating the RMS value digitally were considered including methods involving sampling of the input voltage with high or low sampling frequencies. The method chosen is to use an analog second order lowpass filter with two real poles at 15 Hz on the input of the A/D converter measuring the input voltage. The method is chosen because of its simplicity. The filter reduces the rectified grid voltage to a DC voltage proportional to the input voltage RMS value assuming the grid voltage to be a pure sinewave.

V. A/D CONVERTER AND PWM GENERATOR RESOLUTION

The A/D converter and the PWM generator resolution is important in relation to the input current distortion. If the resolution of the dutycycle on the PWM signal controlling the switched multiplier is low the distortion of the input current will be large at low output power. A low resolution results in a large change in the switched multipliers gain if the least significant bit of the dutycycle-register in the PWM generator changes value. The result is a large change in the input power drawn from the grid and as a consequence of this the output voltage may rise or fall more than the deviation from the reference value was before the controller changed the dutycycle on the control signal.

A low resolution in the A/D converter measuring the output voltage will similarly result in quantisation error.

In the implementation of the hybrid control of the PFC in a PIC16F877A microcontroller the resolution of the PWM generator is 9 bits at a switching frequency of 39.1 kHz. The clock-frequency of the microcontroller is 20 MHz. The A/D-converter in the PIC16F877A has a resolution of 10 bits. The actual resolution has been increased by reducing the measuring range to 1/5 of the full input range of the A/D converter.

The resolution of the input voltage RMS value measurement is 8 bits.

VI. DIGITAL HARDWARE AND SOFTWARE IMPLEMENTATION

The following description of the software implementation describes the case where the analog filter is used to filter the feedback signal of the output voltage.

Referring to equation (1) it can be seen that the amplitude of the input current drawn from the utility grid is proportional to $1 - D$ where D is the dutycycle of the PWM signal controlling the switched multiplier. It follows from this that the compensator must calculate $1 - D$. To set the dutycycle in the microcontroller however it is necessary to calculate D. The equation describing the dutycycle of the control signal for the switched multiplier is given in (3).

$$D(n) = D_{\max} - \frac{\left(Ref - v_{out}(n)\right)}{v_{in,RMS}^2(n)} \cdot K_p \qquad (3)$$

where D_{max} is the maximum dutycycle of the PWM signal. The maximum dutycycle is as close to 1 as possible to enable the microcontroller to shut down the PFC. If the dutycycle is equal to 1 the gain of the switched multiplier is zero and the current reference signal will be zero as stated in (1).

The order in which the calculations in equation (3) are done is important for the accuracy of the result. The correct order of calculations is shown in Fig. 7.

The proportionl gain K_p for the prototype designed must be 8500 to obtain a voltage drop of no more than 20V at full load compared to the nominal output voltage of 385V. The gain K_p is a 14 bit number and the resolution of the output voltage measurement is 10 bit. The microcontroller has to do a 16×16 bit multiplication and the result can be limited to a 24 bit number. The execution time of a 16×16 bit multiplication followed by a 24×16 bit division would be quite high for the 8 bit microcontroller PIC16F877A.

Instead of doing the calculations realtime in the microcontroller the resulting dutycycle for every combination of input and output voltage can be stored in a lookup table and read by the microcontroller very fast. Since this solution will be much faster than doing the calculations realtime it has been used in the hardware implementation of the hybrid controlled PFC.

The resulting values of the dutycycle has been calculated and programmed in a 512 kb EPROM that is connected to the PIC16F877A. A flowchart for the interrupt service routine in the PIC16F877A is shown in Fig. 8.

The lookup table has been adapted to the input voltage range of the PFC. If the input voltage is out of range the microcontroller sets the dutycycle to D_{max} to shut down the PFC.

If the voltage loop is realized using the digital IIR filter instead of the analog first order filter an extra block is added to the flowchart in Fig. 8. The filter block is inserted in the flowchart after the measurement of the output voltage and the input voltage.

VII. TEST RESULTS

The PFC has been tested with a grid voltage of 230 V_{RMS} and a grid frequency of 50 Hz. The input voltage is an ideal sinewave supplied by an electronic source.

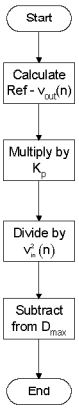

Figure 7 Order of calculations in software

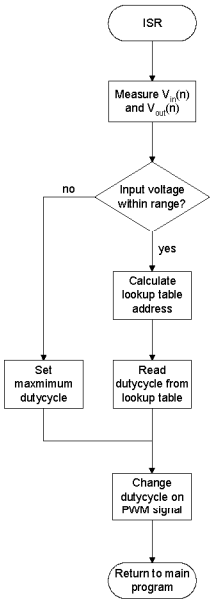

Figure 8 Flowchart for the microcontroller software

Measurements have been performed for both types of filter in the feedback loop of the output voltage.

A plot of the input current at load powers of 100 W and 1 kW respectively can be seen Fig. 10 and Fig. 11 using an analog filter in the output voltage feedback loop. The harmonic content of the input current at 1 kW load power is shown in Fig. 12. The measurement of the harmonic content of the input current shows that the PFC complies with the demands of EN61000-3-2 class A. The rapid changes occurring close to the peak of the input current occurs because the microcontroller samples the input and output voltage and changes the control signal. The input current has a large degree of distortion which is mainly due to quantization errors in the digital implementation of the voltage loop but in a smaller degree to limitations in the analog current loop.

The distortion of the input current is of a different nature than in an analog system because of the hybrid control system. The input current will in theory be proportional to the grid voltage in between samples but will change suddenly directly after an update of the control signal. If the sampling frequency is equal to the grid frequency multiplied by an integer the harmonic spectrum of the input current will only contain odd harmonics of the grid frequency. If the sampling frequency is not equal to the grid frequency multiplied by an integer the spectrum of the input current will have inter-harmonic distortion. The problem of inter-harmonic distortion won't occur at 50 Hz because the sampling frequency has been selected at 500 Hz. If the PFC should operate at 60 Hz it would be advantageous to select a sampling frequency of 600 Hz to avoid inter-harmonic distortion.

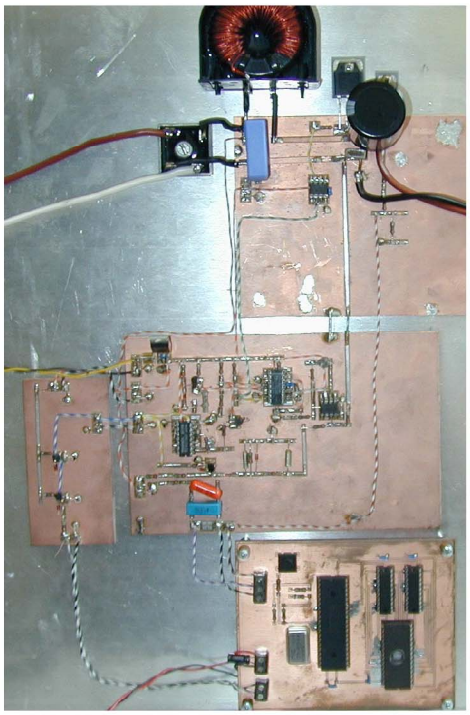

Figure 9 The experimental setup

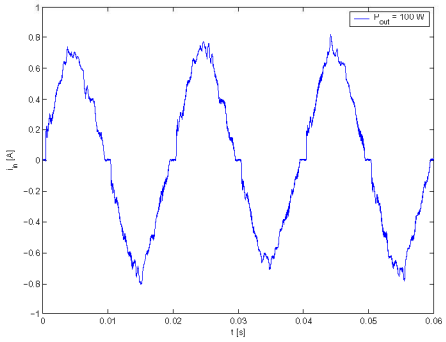

Figure 10 Input current for V_{in} = 230 V_{RMS} and P_{out} = 100 W with the analog filter in the voltage loop

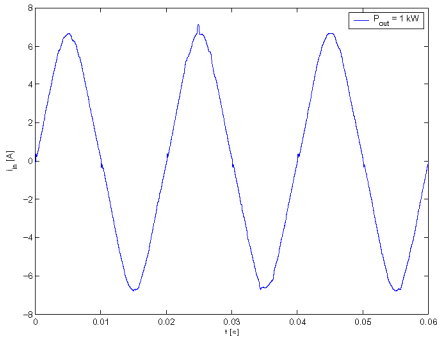

Figure 11 Input current for V_{in} = 230 V_{RMS} and P_{out} = 1.0 kW with the analog filter in the voltage loop

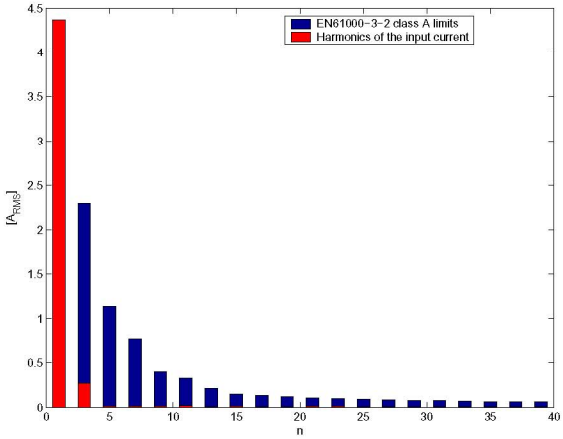

Figure 12 Harmonic content of input current for V_{in} = 230 V_{RMS} and P_{out} = 1.0 kW with the analog filter in the voltage loop

Similar measurements of the input current have been performed on the PFC with the digital IIR filter in the voltage loop. The results are shown in Fig. 13 to Fig. 15. The measurements show that the input current is less distorted using the digital IIR filter compared with the analog filter especially at low levels of the output power. The total harmonic distortion at 1 kW is practically the same using the two different filters although the amount of third harmonic distortion is lower using the digital IIR filter.

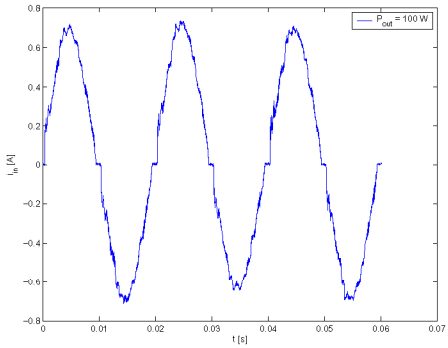

Figure 13 Input current for V_{in} = 230 V_{RMS} and P_{out} = 100 W with the digital IIR filter in the voltage loop

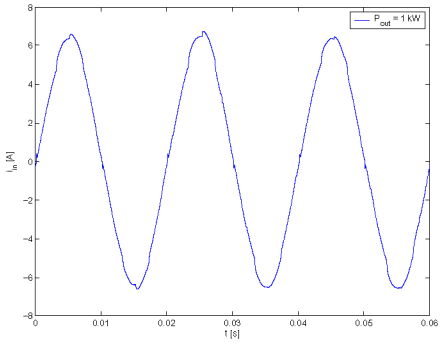

Figure 14 current for V_{in} = 230 V_{RMS} and P_{out} = 1.0 kW with the digital IIR filter in the voltage loop

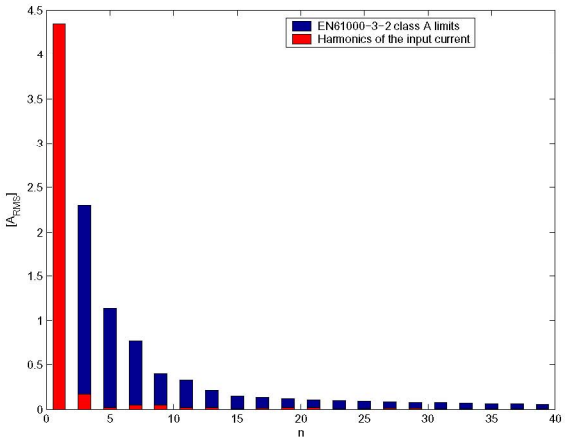

Figure 15 Harmonic content of input current for V_{in} = 230 V_{RMS} and P_{out} = 1.0 kW with the digital IIR filter in the voltage loop

The dynamic response of the PFC at a loadstep has been measured with an electronic load (see Fig. 16 and Fig. 17). The electronic load draws a constant current which explains the ripple on the plot of the output power. The steady state output voltage at 100 W was 389 V and at 1.0 kW it was 367 V with both the analog and the digital IIR filter in the voltage loop.

The overshoot and undershoot of the output voltage is smaller with the analog filter than with the digital IIR filter which is due to fact that the phase margin of the voltage loop is higher with the analog filter. The settling time after a step is similarly shorter with the analog filter which can also be explained by the higher phase margin.

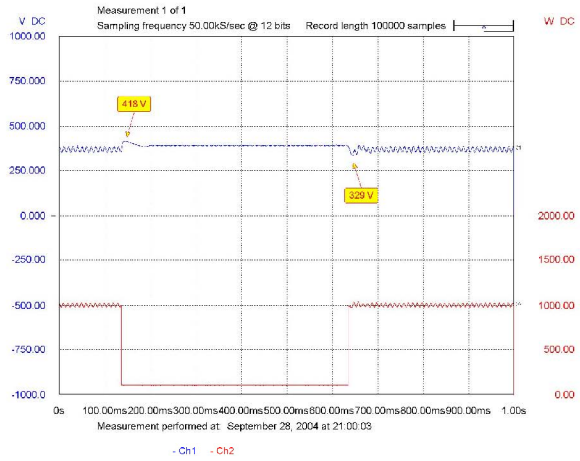

Figure 16 Stepresponse between 100 W to 1.0 kW output power with the analog filter in the voltage loop

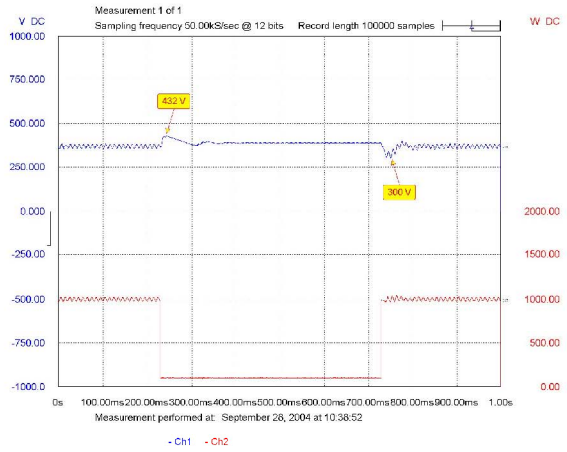

Figure 17 Stepresponse between 100 W to 1.0 kW output power with the digital IIR filter in the voltage loop

VIII. Conclusions

The proposed hybrid control scheme has been shown to give satisfactory test results. The harmonic distortion is low and the dynamic response of the designed PFC is equal to similar analog controlled PFCs. The utilization of the microcontroller is very low. The disadvantages of the design are a large EPROM used as a lookup table and the issue of inter-harmonic distortion if the sampling frequency doesn't equal the grid frequency multiplied by an integer.

A cheaper implementation of the proposed hybrid control scheme could be realized by leaving out the lookup table and using a microcontroller with a lower pincount e.g. a PIC12F683 microcontroller from Microchip.

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16 Appendix B – Publication by L. T. Jakobsen et al.

L. T. Jakobsen and M. A. E. Andersen

”High Performance Mixed Signal Controllers for DC/DC Converters”

Nordic Workshop on Power and Industrial Electronics 2006 , 2006

High Performance Mixed Signal Controllers for DC/DC Converters

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Abstract— **This paper describes how mixed signal controllers combining a cheap microcontroller with a simple analogue circuit can offer high performance digital control for DC/DC converters. Mixed signal controllers have the same versatility and performance as DSP controllers if the microcontroller software is optimized.**

Two mixed signal controller designs based on the same 8-bit microcontroller are compared both theoretically and experimentally on a typical Point of Load converter. A 16-bit digital PID controller using lookup tables with a sampling frequency as high as 200 kHz implemented on the 16 MIPS, 8-bit ATTiny26 microcontroller is demonstrated.

Index Terms—**Digital control, microcontroller, Point of Load converter**

I. Introduction

Research in digital control techniques for DC/DC converters has mainly focused on the use of Digital Signal Processors (DSP) [1,2]. The purpose of the research in DSP based control is to show the possibilities a DSP gives to obtain a high performance digitally controlled DC/DC converter generally without considering the cost of the DSP. Compared to analogue control ICs DSPs are expensive and consume more power. The advantage of DSPs is that the DSPs are versatile and can be used to control almost any DC/DC converter topology simply by adapting the DSP software to the specific application.

A different approach that is increasingly popular is custom designed ICs implementing a digital control scheme for a specific type of converter or application [3]. The main disadvantage of this solution is the lack of versatility since the IC is designed for a specific application, such as Point Of Load Converters (POL) or Power Factor Correction (PFC) [4]. A few custom designed digital control ICs have however appeared on the market and these products deliver both good control loop performance and features such as external supervision at prices that are competitive compared to DSP based solutions.

The proposed mixed signal control scheme combines analogue circuitry with a cheap 8-bit microcontroller that can deliver the same control loop performance as a DSP based controller. It has the versatility of the DSP solutions and can be implemented in single IC thereby combining the best of both of the abovementioned methods and at a lower cost. The proposed mixed signal control scheme will be demonstrated on a low voltage synchronous Buck converter that typically would be used in POL applications.

II. Mixed signal controllers versus DSP based controllers

Research in digital control of DC/DC converters in the recent years has focused on digital controllers which sample both the inductor/switch current and the output voltage of the DC/DC converter. There are two major disadvantages of this approach. The first disadvantage is that the A/D converter of the digital controller must have a high sample rate. Not only does it need to sample two parameters (current and voltage), typically once every switching period of the DC/DC converter, but the results of the A/D conversions must be available in time for the DSP to calculate the dutycycle of the PWM signal controlling the DC/DC converter before the beginning of a new switching period (see Figure 1). The second disadvantage of the fully digital control method is that the number of calculations performed by the digital controller is quite high because the digital controller actually includes two control loops, i.e. a current and a voltage loop.

In order to meet these demands for the digital controller the digital hardware must run at a high clock frequency (typically around 100 MHz) and include a fast A/D converter (at least 1 MSPS for a converter with a switching frequency of 100 kHz). To meet these demands the digital controller will be quite expensive compared to what is achieved in terms of control loop performance and it certainly will have a high price compared to analogue solutions.

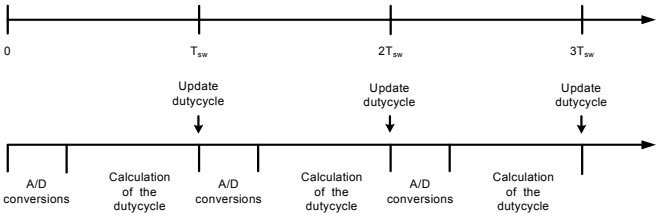


Figure 1: Typical timing diagram of a DSP based digital controller

Sampling and controlling the inductor current in DC/DC converter in a DSP presents another challenge beside the demands on the digital hardware. In order to get good control of the current it is necessary to sample either the peak or average inductor current. The digital controller has to sample

the inductor current at the right instant of time to measure the correct current value [5]. This increases the complexity of the DSP software because it must calculate and control the correct instant in time at which the inductor current is sampled.

The mixed controller described in this paper solves almost all of the abovementioned challenges by using analogue circuitry to control the inductor current of the DC/DC converter while keeping the output voltage control loop digital. A general block diagram of a mixed signal controller is shown in Figure 2. The current loop controller is analogue whereby the need to sample the inductor current is removed. The analogue current loop controller can be implemented using peak, average or hysteresis current mode control depending on the application and the preference of the design engineer.

The output voltage is sampled by an A/D converter followed by a digital voltage loop controller. The voltage loop controller calculates a reference signal for the analogue current loop and the reference signal is converted to an analogue reference voltage by a D/A converter. The sampling rate of the A/D converter can be selected based on the demands for the control loop bandwidth of the DC/DC converter. The higher the control loop bandwidth is the higher the sampling rate must be. Since the digital controller only has to compute one control loop, i.e. the voltage loop, the number of computations will be reduced considerably making it possible to use cheaper devices than DSPs. Because of the reduced number of calculations the digital control will also be able to run at a lower clock frequency therby reducing the power consumption of the control circuit compared to a DSP based solution.

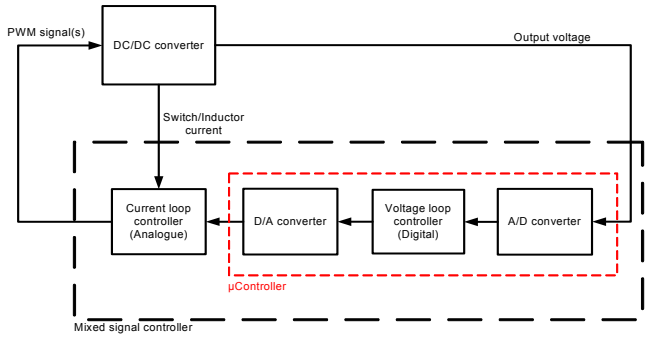


Figure 2: General block diagram of a mixed signal controller

III. Comparison of two different mixed signal controllers based on an 8-bit microcontroller

Two different mixed signal controllers using peak current mode control will be described and compared in this section. Both mixed signal controllers have been built and tested on a low voltage buck converter with synchronous rectification.

A diagram of the first design designated “PWM-DAC” is shown in Figure 3. The analogue peak current mode controller is realised by the D flip-flop and the comparator. The PWM signal generated by the microcontroller has two functions. The first function is to control the switching frequency of the buck converter by clocking the D flip-flop. The second function of the PWM signal generated by the microcontroller is to work as a 1-bit D/A converter in conjunction with a lowpass filter consisting of two resistors and capacitor to generate an analogue reference on the inverting input of the comparator.

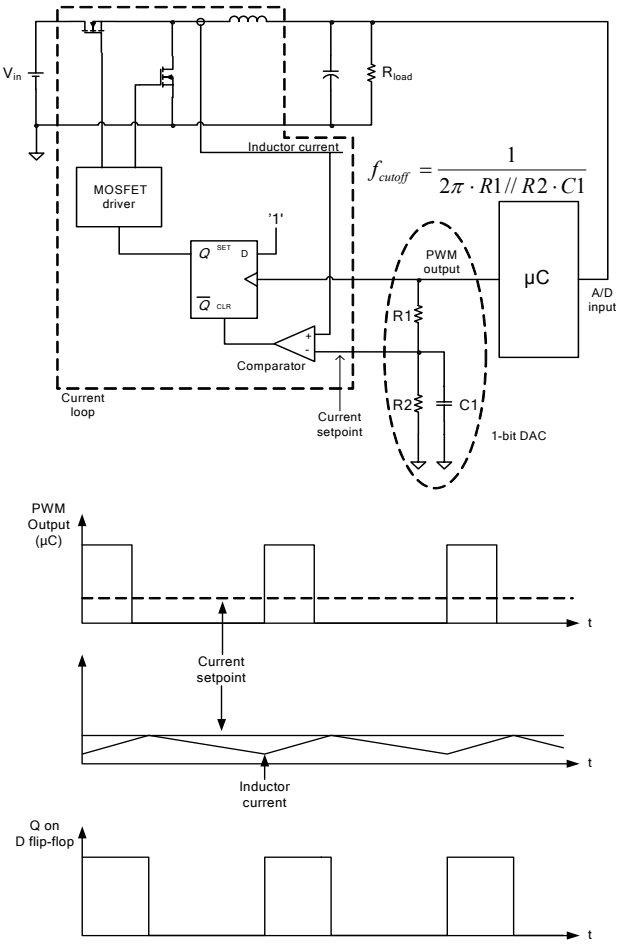


Figure 3: Schematic showing the principle of the “PWM-DAC” mixed signal controller

Many microcontrollers have at least one PWM output and using the PWM output of the microcontroller as a D/A converter is cheap and simple. It has however certain disadvantages which must be taken into consideration. The analogue reference voltage is a function of the dutycycle of the PWM signal and the resolution of the dutycycle is limited by the clock frequency of the microcontroller. This will in turn limit the resolution of the 1-bit D/A converter which results in limited output voltage regulation.

Ripple on the reference voltage generated by the 1-bit D/A converter can affect the stability of the analogue current control circuit. The ripple must be attenuated to an acceptable level. This can only be done by selecting the cutoff frequency of the lowpass filter considerably below the frequency of the PWM signal as expressed in (1).

$$f_{cutoff} << f_{sw} \qquad (1)$$

The lowpass filter will add a phase shift to the output voltage control loop and reduce the phase margin. A low cutoff frequency for the lowpass filter will therefore limit the voltage loop bandwidth that can be obtained.

The second mixed signal controller (designated "DAC") is practically the same as the one described above. The only difference is that a multibit D/A converter (see Figure 4) is used instead of the combination of a PWM signal and a lowpass filter. The advantages of using a multibit D/A converter are twofold. The first advantage is that the D/A converter resolution in terms of bit can be chosen freely and the second advantage is that the multibit D/A converter is much faster than the PWM/Lowpass filter solution. A fast D/A converter gives a much smaller phase shift in the output voltage control loop. The smaller phase shift gives better phase margin or it can be converted into higher control loop bandwidth by increasing the control loop gain.

The use of a multibit D/A converter will increase the price of the mixed signal controller but the increase in control loop bandwidth gained with the multibit D/A converter will justify the cost increase in applications where a fast control loop is essential.

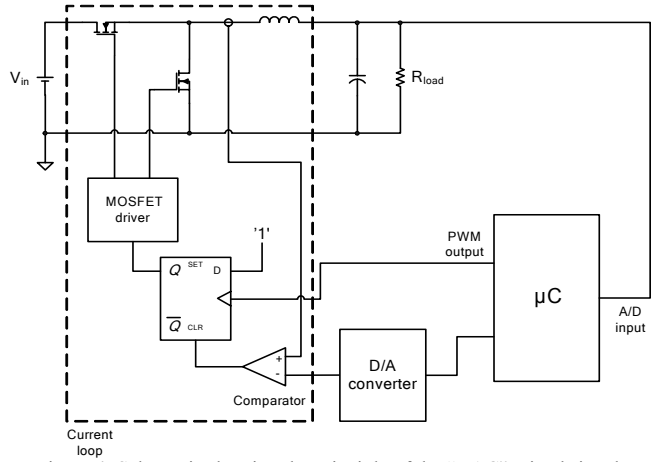


Figure 4: Schematic showing the principle of the "DAC" mixed signal controller

IV. MICROCONTROLLER SOFTWARE

The choice of microcontroller is critical in terms of control loop performance. Important parameters are the A/D conversion rate, the computational capabilities of the microcontroller in terms of Million Instructions Per Second (MIPS) and PWM resolution. Different manufacturers of microcontrollers choose to optimise their products for different applications. ATMEL's AVR family of 8-bit microcontrollers is overall the best suited low cost microcontroller for power electronics applications such as the mixed signal controllers described in this paper. The AVR family has a 10-bit 75 kilosamples per second A/D converter and a computational speed of 16 MIPS. The PWM signal is generated from an internal 64 MHz PLL allowing a PWM resolution of 8 bits at 250 kHz.

The goal of the prototype designs was to program a digital controller that gave as high a control loop bandwidth as possible. The specific goal for the microcontroller software was to program a digital PID converter with a sampling frequency of 200 kHz and 16 bits resolution.

The discrete time transfer function for the PID controller is given in equation (2).

$$G_c(z) = \frac{d(z)}{e(z)} = \frac{a + b \cdot z^{-1} + c \cdot z^{-2}}{1 - z^{-1}} \qquad (2)$$

where e is the difference between the sampled output voltage and the voltage reference and d is the dutycycle of '*PWM control*'.

The sampling period is 5 µs and the command execution time for a single cycle command in the ATTiny26 is 62.5 ns at a clock frequency of 16 MHZ. This means that the microcontroller can execute 80 single cycle commands in each sampling period. The Interrupt Service Routine (ISR) can only use 72 out of the 80 commands because the microcontroller uses four clock cycles both to enter and exit the ISR. To be able to program the 16 bit PID with just 72 single cycle commands it was necessary to use lookup tables stored in the microcontrollers program memory because the microcontroller doesn't have a hardware multiplier to perform multiplications by the three coefficients a, b and c. The results of the multiplication of e by each of the three coefficients a, b and c in equation (2) is stored in three separate lookup tables designated table #1, #2 and #3. The internal resolution is 16 bits as already mentioned which means that two bytes must be read for each multiplication since the internal data structure of the ATTiny26 is 8 bits.

The error e is limited to values between -16 and 15 in order to reduce the size of the lookup tables which each takes up 64 bytes of program memory. The three constants can be chosen in the range from -64 to 64 in steps of 0.0625 ($1/16^{th}$).

A flowchart of the software used in the "PWM-DAC" prototype is shown in Figure 5. The numbers beside each operation in the flowchart will be used in the following description of the ISR. The ISR of the "DAC" prototype is very similar to the ISR described in this section and will not be described in detail.

The basic idea is that at the occurrence of an interrupt the ISR initiates an A/D conversion (*1)* and while the A/D converter measures the output the software begins calculating the new dutycycle by reading the results of the multiplications of b and c by the errors of the two previous samples from table #2 and #3 (*(2)* and *(3)*) and adding the values read from the lookup tables to the dutycycle calculated by the previous run of the ISR *d(n-1)*. Next the result of the A/D conversion, i.e. the measured output voltage, is read by the ISR *(4)*. The software is written under the assumption that the A/D converter has finished sampling the output voltage when the ISR reads the A/D converter result. This can easily be assumed since the A/D conversion time is constant and can be calculated beforehand. In a typical microcontroller application

the software would poll a bit indicating whether the A/D converter has finished the A/D conversion or is in the process of sampling but that would increase the execution time of the ISR, which must be optimized to get as high a sampling frequency as possible.

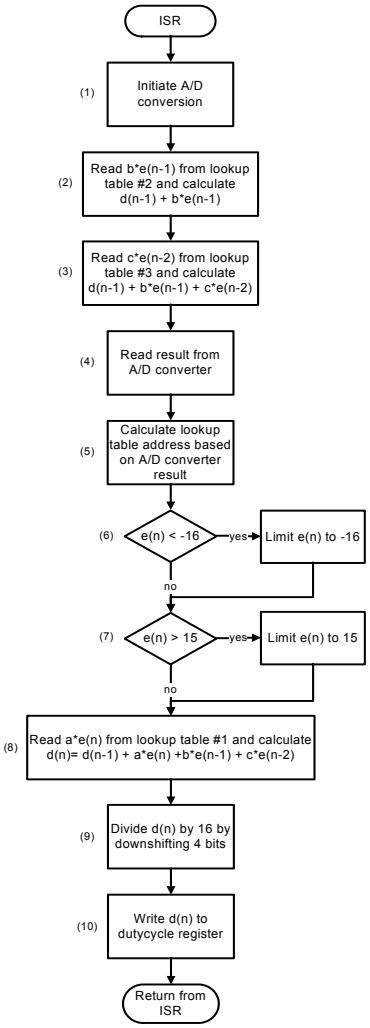


Figure 5: Flowchart of the Interrupt Service Routine

Once the A/D converter result has been read the ISR calculates the lookup table address corresponding to the measured output voltage *(5)*. As already mentioned the range of the error signal *e* is limited to reduce the space taken up by the lookup tables in the program memory (*(6)* and *(7)*). Next the result of the multiplication of *a* and *e* is read from lookup table #1 and the new dutycycle *d(n)* is calculated and written to the dutycycle register (*(8)*, *(9)* and *(10)*). The division of *d(n)* by 16 in step *9* is done because the coefficients *a*, *b* and *c* have been multiplied by 16 when the lookup tables were generated in MATLAB. The result is that the Least Significant Bit (LSB) in the calculation of the dutycycle represents $1/16^{th}$ thereby increasing the accuracy with which the zeros of the digital controller can be placed in the frequency domain. Dividing by 16 in step *9* ensures that the LSB of the number written to the dutycycle register corresponds to 1, i.e 2^0.

The ISR software routine consists of 54 assembly commands with a total execution time of 70 command cycles, which is very close to the maximum of 72 command cycles available. An overview of the partitioning of the software and the execution time for each partition is given in Table 1.

TABLE 1: SOFTWARE PARTITIONING AND EXECUTION TIMES

Function	Execution time in number of clock cycles
Reading data from lookup tables	32
Calculate dutycycles (additions)	16
A/D converter control	9
Error limiting	6
House keeping	7
Hardware interrupt handling	8
Total	78

V. DERIVATION OF SYSTEM TRANSFER FUNCTIONS

A model of the converter and the mixed signal controller has been developed in order to be able to select the coefficients *a*, *b* and *c* of the controller transfer function given in equation (1). A block diagram of the control loop model for the 'PWM-DAC' controller described in section III is shown in Figure 6. The model consists of five blocks some of which are modeled in the continuous time s-domain and some in the discrete time z-domain. The idea is that the digital controller, which is implemented in a microcontroller, has a discrete time nature because it samples the output voltage at a constant sample rate while the converter transfer function and PWM/lowpass filter DAC is easily modeled in the continuous time. In order to plot the open loop transfer function of the control loop the continuous time transfer functions will be converted to discrete time transfer functions using the Tustin approximation (see equation (3)) [8]. The time T_s in the Tustin approximation is the sampling period of the discrete time transfer function.

$$s \cong \frac{2}{T_s}\frac{1-z^{-1}}{1+z^{-1}} \qquad (3)$$

The transfer function of the digital controller is given by equation (2). The computational delay in the control loop model represents the execution time of the ISR described in section IV. The sampling time of the A/D converter is included in the computational delay because the software starts the A/D conversion and reads the result from the A/D converter in the ISR. The actual delay from the occurrence of the interrupt until the dutycycle of the PWM output is updated is determined by the period time of the PWM signal and not the execution time of the ISR. The PWM signal is generated by a counter, that counts from 0 to 255. When the counter is reset to 0 the PWM output is set to '1'. The counter value is compared to the dutycycle register (an internal register in the microcontroller) and the PWM output is set to '0' when the counter value is equal to value of the dutycycle register. The dutycycle register is written by the ISR as shown in the flowchart (see Figure 5). The dutycycle register is a latched register and the latch is updated when the counter is reset to 0.

This means that the actual computational delay will be equal to the period time of the PWM signal, because even if the ISR could calculate the new dutycycle faster than the period time of the PWM signal it wouldn't have an impact on the PWM signal until the dutycycle register latch is updated, i.e. at the beginning of a new PWM period. If the execution time of the ISR is greater than the period time of the PWM signal the dutycyle register will be updated at the beginning of the first PWM period after the ISR has written the dutycycle register. The computational delay is therefore equal to an integer number from 1 and upwards multiplied by the period time of the PWM signal.

The transfer function of the computational delay is given by equation (4) and has the same sampling time as the controller transfer function (2).

$$G_{delay}(z) = z^{-1} \tag{4}$$

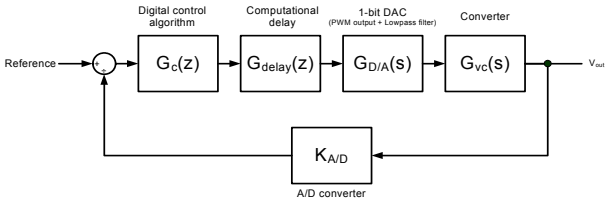


Figure 6: Block diagram of the control loop model

The transfer function of the 1-bit D/A converter given by equation (5) combines the gain of the PWM output with the transfer function of the first order lowpass filter.

$$G_{D/A}(s) = \frac{V_{DD}}{2^{n_{PWM}}} \cdot \frac{\omega_c}{s + \omega_c} \tag{5}$$

where V_{DD} is the supply voltage of the microcontroller, n_{PWM} is the resolution of the PWM output and ω_c is the cutoff frequency of the lowpass filter. It is assumed the PWM output has a constant gain.

In the "DAC" prototype the D/A is assumed to have a constant gain and no frequency dependency (see equation (6)), corresponding to an assumption of zero settling time on the D/A converter output.

$$K_{D/A} = \frac{\Delta V_{D/A}}{2^{n_{D/A}}} \tag{6}$$

where $\Delta V_{D/A}$ is D/A converter output voltage range and $n_{D/A}$ is the D/A converter resolution in bits.

The converter transfer function $G_{vc}(s)$ (see equation (7)) is the first order approximation of a peak current mode controlled Buck converter derived in [7].

$$G_{vc}(s) = \frac{R_{load}}{s \cdot C \cdot R_{load} + 1} \tag{7}$$

where R_{load} is the load resistance and C is the output capacitance of the converter.

Finally the A/D converter gain $K_{A/D}$ is given by equation (8).

$$K_{A/D} = \frac{\Delta V_{A/D}}{2^{n_{A/D}}} \tag{8}$$

where $\Delta V_{A/D}$ is the A/D converter input voltage range and $n_{A/D}$ is the A/D converter resolution in bits.

The open loop transfer function is calculated and plotted in MATLAB and expression of the open loop transfer will not be shown here because of its complexity.

VI. Experimental results

Two prototypes have been built to be able to compare the two mixed signal controllers described in the previous section. The electrical specifications of the two prototypes are given in Table 2.

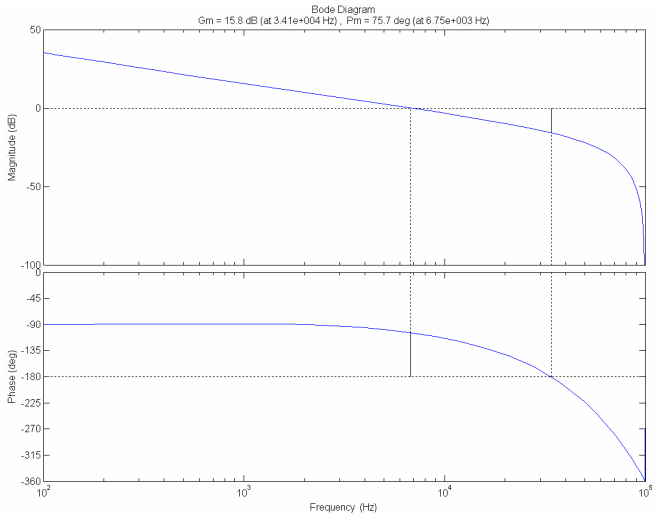
The digital voltage loop controller is implemented in the ATTiny26 microcontroller from the ATMEL AVR family. The differences in switching and sampling frequency for the two prototypes were dictated by hardware limitations. The controller software routine is run as an Interrupt Service Routine (ISR) and has an execution time of 5µs. This corresponds to a sampling frequency of 200 kHz but the internal A/D converter of the ATTiny26 is only capable of a sampling frequency of 75 kHz. To be able to sample the output voltage at 200 kHz necessary an external A/D converter was added to the "PWM-DAC" prototype.

The "DAC" prototype uses an external 8-bit D/A converter to generate the analogue reference voltage but because of a limited number of I/O ports on the ATTiny26 it wasn't possible to have both D/A and A/D converters connected at the same time. The "DAC" prototype therefore uses the internal A/D of the ATTiny26 sampling at a higher rate than recommended by ATMEL. The sampling rate, which is higher than recommended, is possible because the controller only the uses the 8 most significant bits of A/D converter result.

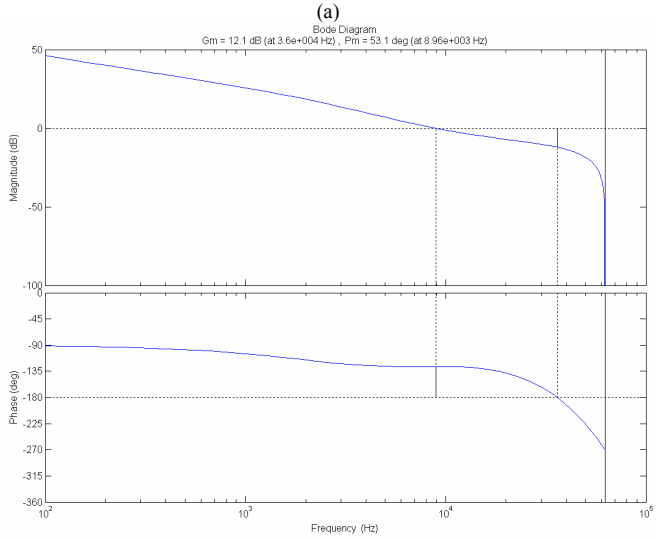
Open loop Bode plots for the two prototypes are shown in Figure 7. The constants *a, b* and *c* in the controller transfer (given by equation (1)) has been selected based on root-locus analysis of the converter transfer function. The control loop specifications are listed in Table 3.

TABLE 2: ELECTRICAL SPECIFICATIONS

	Mixed signal controller "PWM-DAC"	Mixed signal controller "DAC"
Input voltage range	4.5 – 6.0 V	4.5 – 6.0 V
Output voltage	2.0 V	2.0 V
Output current	10 A	10 A
Switching frequency	400 kHz	250 kHz
Inductance	2.0 µH	2.0 µH
Output capacitance	300 µF	300 µF
Sampling frequency	200 kHz	125 kHz
Computational delay	5 µs	4 µs



(a)



(b)

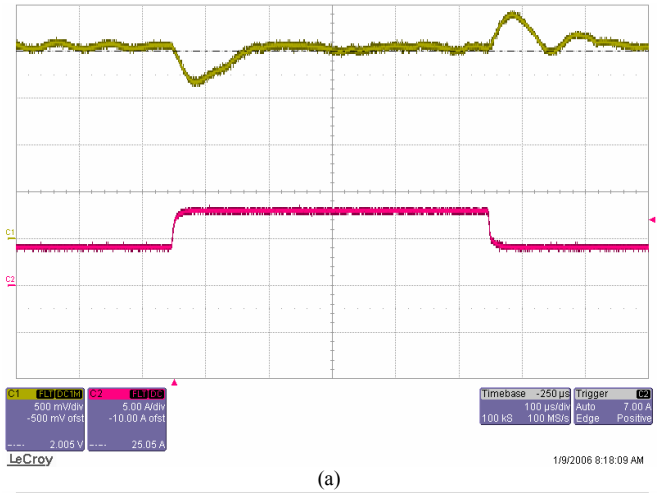
Figure 7: (a) Open loop Bode plot for "PWM-DAC"
(b) Open loop Bode plot for "DAC"

TABLE 3: CONTROL LOOP SPECIFICATIONS

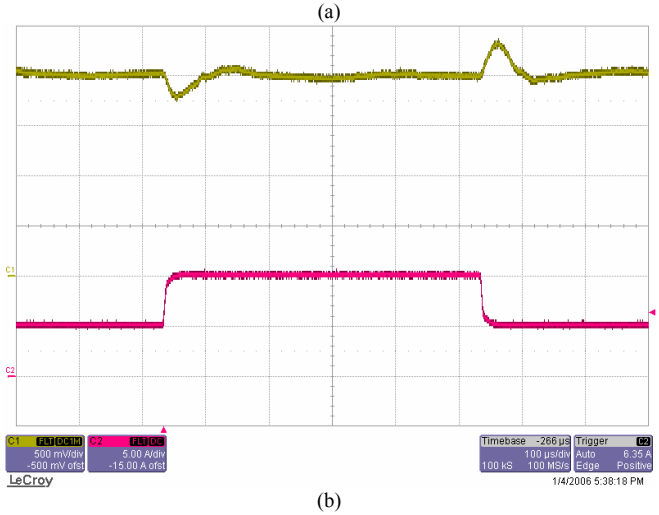
	Mixed signal controller "PWM-DAC"	Mixed signal controller "DAC"
a	3.0000	6.0000
b	-3.9375	-6.3750
c	1.0625	1.6250
$n_{PWM} / n_{D/A}$	7.3 bit	8 bit
$V_{DD} / \Delta V_{D/A}$	4.0V	2.6V
$n_{A/D}$	8 bit	8 bit
$\Delta V_{A/D}$	4.0V	4.0V

The open loop Bode plots shows that the crossover frequency is higher for the "DAC" prototype than for the "PWM-DAC" prototype as would be expected. The increase in crossover frequency from 6.75kHz to 8.96kHz is quite significant. The result of the higher crossover frequency of the "DAC" prototype is lower high frequency output impedance compared to the "PWM-DAC" prototype. The lower output impedance will result in a better loadstep response in terms of smaller overshoot and faster settling time.

The performance of the two prototypes has been tested by measuring the output voltage response to a loadstep (see Figure 8). The measurement on prototype "PWM-DAC" is a loadstep between 4 and 8A while the loadstep on prototype "DAC" is between 5 and 10A. The reason that the two measurements aren't measured with the same loadstep is that prototype "PWM-DAC" has a tendency to become unstable with a loadstep from 5 to 10 A. The instability is caused by the fact that the analogue reference signal controlling the peak current has an upper limit close to 10A. When the controller tries to increase the current to compensate for the loadstep it reaches the upper limit and becomes unstable.



(a)



(b)

Figure 8:
(a) Loadstep "PWM-DAC". v_{out} (Upper trace) and i_{out} (Lower trace)
(b) Loadstep "DAC". v_{out} (Upper trace) and i_{out} (Lower trace)

A comparison of the two loadstep measurements shows that both the overshoot and settling times are shorter for the "DAC" prototype than for the "PWM-DAC" prototype. The overshoot on the "PWM-DAC" prototype is approximately 0.4V or 20% of nominal output voltage and the settling time is

approximately 110µs. For the "DAC" prototype the overshoot and settling times are 0.3V and 75µs respectively. The overshoot of the output voltage for the "DAC" prototype is 15% of the nominal output voltage, which is unacceptable in most POL applications. The size is determined by the control loop bandwidth of the DC/DC converter and by the size of the output capacitor. The output voltage overshoot is comparable to the measurements shown in [1] if the size of the output capacitor is taken into consideration. Increasing the size of the output capacitor can reduce the output voltage overshoot at loadsteps.

VII. CONCLUSIONS

Mixed signal controllers based on cheap microcontrollers are a good alternative to DSPs for digital control of DC/DC converter in POL applications. The performance can be optimized through good software programming to be comparable to the performance that can be obtained using a DSP running at a much higher clock frequency. It has been shown that a 16 MIPS ATMEL ATTiny26 microcontroller can be used as 16-bit PID controller with a sampling frequency of 200kHz. The important feature of the microcontroller software described in this paper is the use of lookup tables stored in the microcontrollers program memory. Without lookup tables it would be impossible to obtain sampling frequencies high enough to be able to control a DC/DC converter with high control loop bandwidth using cheap and simple microcontrollers such as the ATTiny26 from ATMEL.

Mixed signal controllers are in no way a new invention [6], but the results shown in this paper demonstrates that mixed signal controllers based on cheap microcontrollers can replace DSPs in even the most demanding DC/DC converter applications such as Point of Load converters.

The mixed signal controller can be even more competitive if the analogue circuitry used in the current loop is combined with a cheap microcontroller core in a single IC especially if the microcontroller core is run at a clock frequency slightly higher than what low cost microcontrollers run at today.

To achieve sample rates as high enough to meet the demands of DC/DC converter applicationsthe engineer writing the software to be experienced in microcontroller programming. Most power electronics specialists generally don't have that kind of experience and it is therefore crucial that power electronics specialists cooperate with software engineers to make it possible to use microcontrollers in high performance mixed signal controllers.

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17 Appendix C – Publication by L. T. Jakobsen et al.

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"Comparison of Two Different High Performance Mixed Signal Controllers for DC/DC Converters"

IEEE Workshop on Computers in Power Electronics 2006, pp. 129 – 135, 2006

2006 IEEE COMPEL Workshop, Rensselaer Polytechnic Institute, Troy, NY, USA, July 16-19, 2006

Comparison of Two Different High Performance Mixed Signal Controllers for DC/DC Converters

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***Abstract*— Mixed signal controllers based on a cheap microcontroller and a few analogue components can deliver high performance digital control of DC/DC converters through an optimized software design. The mixed signal controllers have the same versatility as DSP controllers and can be adapted to any DC/DC converter topology and application.**

A comparison, both theoretically and experimentally, of two different mixed signal controller designs based on the same 8-bit microcontroller is presented for a low voltage Buck converter. A 16-bit digital PID controller using lookup tables with a sampling frequency as high as 200 kHz implemented on the 16 MIPS, 8-bit ATTiny26 microcontroller is demonstrated and an exhaustive description of the software is given.

***Index Terms*—Digital control, microcontroller, DC/DC converter**

I. Introduction

Digital control of switch mode power supplies is a topic of increasing interest not only in academic research but also in the power electronics industry. Research within the area has mainly focused on two different types of solutions.

The first solution is the Digital Signal Processor (DSP) based solution in which the digital control scheme is implemented in software on a powerful DSP [1,2]. The goal of the research within the DSP based solutions has been to show the possibility of implementing advanced control schemes in software which can improve the performance of the power supply compared to the traditional analogue control techniques. Compared to analogue control ICs, which are the preferred solution in commercially available switch mode power supplies, DSPs are expensive and have much higher power consumption.

The second solution is custom designed ICs which are designed for a specific converter topology or application [3]. The custom designed IC has the advantage that because it is developed for a single application the complexity of the digital circuitry can be reduced considerably compared to the complexity of a DSP reducing the cost of the digital control circuit. The main disadvantage of the custom designed IC is the lack of versatility since the IC is designed for a specific application, such as Point Of Load Converters (POL) or Power Factor Correction (PFC) [4].

An increasing number of custom designed digital control ICs appear on the market and these products deliver both good control loop performance and features such as external supervision at prices that are competitive compared to DSP based solutions.

The mixed signal control scheme proposed in this paper combines analogue circuitry with a cheap 8-bit microcontroller. The mixed signal controller can deliver the same control loop performance as a DSP based controller and it has the versatility of the DSP solutions. The mixed signal control scheme can furthermore be integrated in a single IC thereby combining the best of both of the abovementioned methods and at a lower cost. Two mixed signal control schemes are proposed and demonstrated on a low voltage synchronous Buck converter that would typically be used in Point Of Load (POL) applications. A comparison of the control loop performance of the two control schemes is presented both theoretically and by experimental results.

II. Mixed signal controllers versus DSP based controllers

Research in digital control of DC/DC converters in the recent years has mainly focused on digital controllers which sample both the inductor/switch current and the output voltage of the DC/DC converter. One disadvantage of this approach is that the A/D converter of the digital controller must have a high sample rate. Not only does it need to sample two parameters (current and voltage), typically once every switching period of the DC/DC converter, but the results of the A/D conversions must be available in time for the DSP to calculate the dutycycle of the PWM signal controlling the DC/DC converter before the beginning of the next switching period (see Figure 1). Another disadvantage of the fully digital control method, controlling both the inductor/switch current and the output voltage, is that the number of calculations performed by the digital controller is quite large because the digital controller actually includes two control loops, i.e. a current and a voltage loop. The large number of calculations will increase the demands for a fast DSP.

In order to meet these demands for the digital controller the digital hardware must run at a high clock frequency (typically around 100 MHz) and include a fast A/D converter (around 1 MSPS for a converter with a switching frequency of 100 kHz). To meet these demands the digital controller, typically a DSP, will be quite expensive compared to what is achieved in terms of control loop performance and it will definitely have a high price compared to analogue solutions.

Sampling and controlling the inductor current in a DC/DC

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converter in a DSP presents another challenge beside the demands on the digital hardware. In order to get good control of the current it is necessary to sample either the peak or average inductor current. The digital controller has to sample the inductor current at the right instant of time to measure the correct value of the current [5]. This increases the complexity of the DSP software because it must calculate and control the correct instant in time at which the inductor/switch current is sampled.

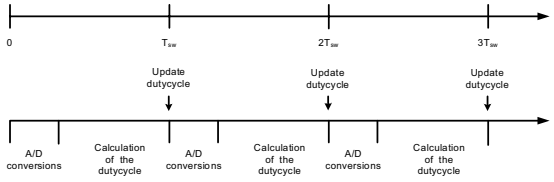

Figure 1: Typical timing diagram of a DSP based digital controller

The mixed signal control scheme resolves almost all of the abovementioned challenges by using analogue circuitry to control the inductor/switch current of the DC/DC converter while keeping the output voltage control loop digital.

A general block diagram of a mixed signal control scheme is shown in

Figure 2. The current control loop is analogue whereby the need to sample the inductor current and have a digital current loop in software is removed. The analogue current loop controller can be implemented using peak, average or hysteresis current mode control.

The output voltage is sampled by an A/D converter followed by a digital voltage loop controller. The voltage loop controller calculates a reference sign

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current loop and the reference signal is converted to an analogue reference voltage by a D/A converter. The sampling rate of the A/D converter can be selected based on the demands for the control loop bandwidth of the DC/DC converter. Since the digital controller only has to compute one control loop, i.e. the voltage loop, the number of computations will be reduced considerably making it possible to use a cheap microcontroller instead of an expensive DSP.

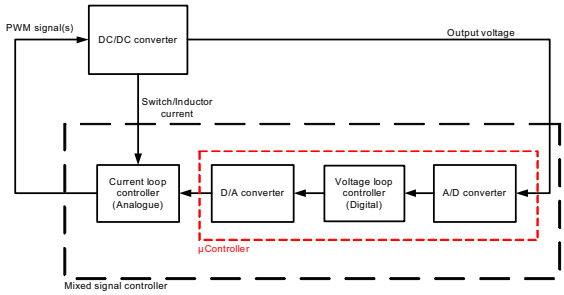


Figure 2: General block diagram of a mixed signal controller

III. Comparison of Two Different Mixed Signal Controllers Based on an 8-bit Microcontroller

Two different mixed signal controllers based on peak current mode control will be described and compared in this section. Both mixed signal controllers have been built and tested on a low voltage Buck converter with synchronous rectification.

A block diagram schematic of the first design designated "PWM-DAC" is shown in Figure 3 along with a typical set of waveforms in the circuit. The analogue peak current mode controller is realized with the D flip-flop and the comparator. The PWM signal generated by the microcontroller has two functions. The first function is to control the switching frequency of the Buck converter by driving the clock input of the D flip-flop. The second function of the PWM signal generated by the microcontroller is to work as a 1-bit D/A converter in conjunction with a lowpass filter consisting of R1, R2 and C1. The 1-bit DAC generates an analogue reference voltage on the inverting input of the comparator.

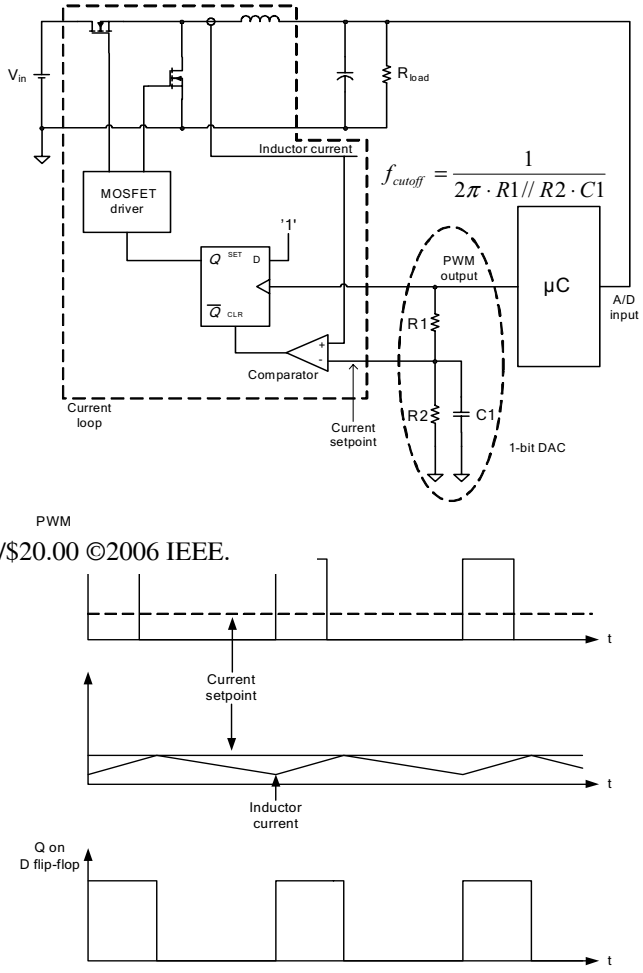


Figure 3: Schematic showing the principle of the "PWM-DAC" mixed signal controller and a typical set of waveforms

Many microcontrollers have at least one PWM output and using the PWM output of the microcontroller as a D/A converter is cheap and simple. Certain disadvantages of the 1-bit D/A converter must however be taken into consideration. The analogue reference voltage is a function of the dutycycle of the PWM signal and the resolution of the dutycycle is limited by the clock frequency of the microcontroller. This will in turn limit the resolution of the 1-bit D/A converter which results in limited output voltage regulation.

Ripple on the reference voltage generated by the 1-bit D/A

converter can affect the stability of the analogue current control circuit and the ripple must therefore be attenuated to an acceptable level. This can only be achieved by selecting the cutoff frequency of the low pass filter considerably below the frequency of the PWM signal as expressed in (1).

$$f_{cutoff} << f_{sw} \quad (1)$$

The low pass filter will add a phase shift to the output voltage control loop and thus reduce the phase margin. A low cutoff frequency for the low pass filter will therefore limit the control loop bandwidth that can be obtained for the voltage loop.

The second mixed signal controller (designated "DAC") is practically the same as the one described above. The only difference is that a dedicated multibit D/A converter (see

Figure 4) is used instead of the 1-bit D/A converter described above. The advantages of using a multibit D/A converter are twofold. Firstly the D/A converter resolution in terms of bits can be chosen freely and secondly the multibit D/A converter is much faster than the PWM/Low pass filter solution. A higher resolution D/A converter mean better output voltage regulation because the analogue reference for the current loop can be set more accurately. A fast D/A converter results in a much smaller phase shift in the output voltage control loop. The smaller phase shift gives better phase margin, which can be converted into higher control loop bandwidth by increasing the control loop gain.

A multibit D/A converter will increase the price of the mixed signal controller. The cost increase will be justified by the increase in control loop bandwidth gained through the use of a multibit D/A converter in applications where a fast output voltage control loop is essential.

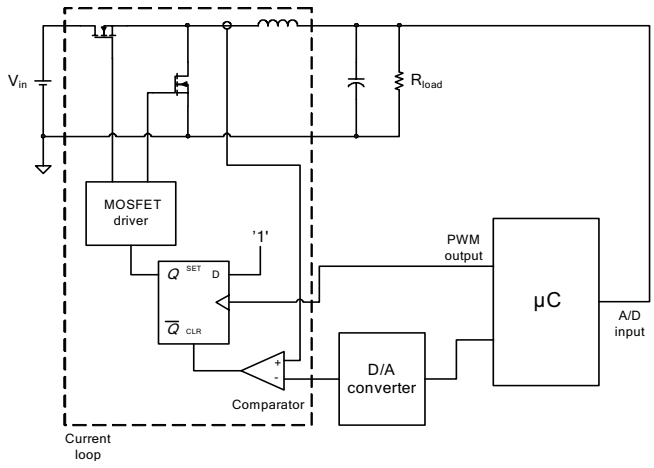


Figure 4: Schematic showing the principle of the "DAC" mixed signal controller

IV. MICROCONTROLLER SOFTWARE

The microcontroller software is the key feature of the mixed signal controller scheme presented in this paper. The Interrupt Service Routine (ISR), which performs the actual digital control algorithm, must have a very short execution time for the digital controller to have a high sampling frequency. A short execution time would normally be obtained through the use of a DSP or microcontroller with a hardware multiplier to reduce the number of commands in the ISR. Alternatively, as presented in the following description, a cheap 8-bit microcontroller with no hardware multiplier can be used with excellent results if the software is designed utilizing the capabilities of the microcontroller.

The choice of microcontroller that is selected for this kind of application is critical because it directly affects the control loop performance of the system. The important parameters that should be taken into consideration when selecting a microcontroller are the A/D conversion rate, the computational capabilities of the microcontroller in terms of Million Instructions Per Second (MIPS) and the PWM resolution if the 'PWM-DAC' mixed signal control scheme is used.

The best suited microcontrollers for power electronics applications such as the mixed signal controllers described in this paper has been found to be the AVR family of 8-bit microcontrollers from ATMEL. The AVR microcontroller selected for the two prototypes presented in the "Experimental results" section is the ATTiny26. The ATTiny26 has a 10-bit 75 kilosamples per second A/D converter and a computational speed of 16 MIPS. The ATTiny26 has an internal 64 MHz PLL, which is used as a clock to the PWM module. The PWM module in the ATTiny26 is a traditional counter based digital PWM generator and the PWM resolution is 8 bits at a switching frequency of 250 kHz.

The ISR software is written to implement a digital PID controller with the discrete time transfer function given in equation (2).

$$G_c(z) = \frac{d(z)}{e(z)} = \frac{a + b \cdot z^{-1} + c \cdot z^{-2}}{1 - z^{-1}} \quad (2)$$

where e is the difference between the sampled output voltage and the voltage reference and d is the output of the digital controller, which is either the dutycycle of '*PWM control*' in the 'PWM-DAC' control scheme or the output to the D/A converter in the 'DAC' control scheme.

The internal resolution of the computations should be 16 bits to have a high accuracy in the internal calculations of the ISR and the design goal was to write a software algorithm that could sustain a sampling frequency of 200 kHz corresponding to a sampling period of 5 μs. The command execution time for a single cycle command in the ATTiny26 is 62.5 ns at the maximum clock frequency of 16 MHZ. This corresponds to 80 clock cycles per sampling period, which means that the microcontroller can perform 80 single cycle commands in each sampling period. By a single cycle command is understood an assembly command that can be performed in a single clock cycles. A few commands in the AVR instruction set takes two or three clock cycles to perform and using these commands reduces the total number of assembly commands that can be completed within the sampling period of 5 μs.

In reality the ISR can only use 72 out of the 80 commands because the microcontroller uses four clock cycles both to

enter and exit the ISR. If some background software is running on the microcontroller it might also be necessary to store some variables temporarily in the data memory while the ISR was completed reducing the number of available commands in the ISR even further. It was assumed that no background software routine would be running on the ATTiny26.

Since the ATTiny26 doesn't have a hardware multiplier to perform multiplications, lookup tables stored in program memory are used. The results of the multiplication of *e(n)*, *e(n-1)* and *e(n-2)* by each of the three coefficients *a*, *b* and *c* in equation (2) is stored in three separate lookup tables designated table #1, #2 and #3. The internal resolution is 16 bits as already mentioned, which means that two bytes must be read for each multiplication since the internal data structure of the ATTiny26 is 8 bits. The error *e* is limited to values between -16 and 15 in order to reduce the size of the lookup tables to 64 bytes of program memory for each table. The ISR calculates the lookup table address corresponding to the error based on the sampled output voltage. The calculation of the address for table #1 is defined by equation (3).

$$Address(table\#1) = SA(table\#1) + v_{out}(n) - (Ref - 16) \qquad (3)$$

where *SA(table#1)* is the start address of table #1, $v_{out}(n)$ is the sampled output voltage and *Ref* is the output voltage reference.

The bit configuration used in the 16 bit calculations is illustrated in Figure 5. The ISR uses 2's complement numbers and Figure 5 shows how the principle is for positive numbers but there is no significant difference for negative numbers.

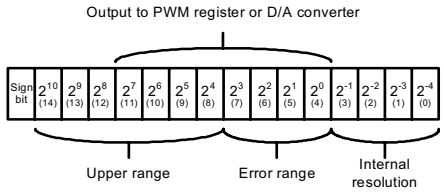


Figure 5: Bit configuration in 16 bit calculations

The four least significant bits are used to increase the internal resolution making it possible to adjust the three coefficients *a*, *b* and *c* in steps of 0.0625 (2^{-4}). The four next bits (bits 4 through 7) represent the error *e* (range 0 to 15) and the 7 following bits is the upper range which theoretically allows the coefficients *a*, *b* and *c* to be in the range from –128 to 128. The output to the PWM register or D/A converter is the middle 8 bits (bits 4 through 11).

A flowchart of the ISR used in the "PWM-DAC" prototype is shown in Figure 6. Beside each operation in the flowchart is given a number in parentheses. These numbers will be used in the following description of the ISR. The ISR of the "DAC" prototype is very similar to the ISR described in this section and will not be described in detail.

At the occurrence of an interrupt generated at the rising edge of the PWM output the ISR initiates an A/D conversion (*1)* and the software begins the calculation of the dutycycle while the A/D converter measures the output voltage. The calculation of the new dutycycle consists of reading the results of *e(n-1)* and *e(n-2)* multiplied by *b* and *c* respectively from lookup table #2 and #3 (*(2)* and *(3)*) and adding the results read from the lookup tables with the dutycycle calculated by the previous run of the ISR *d(n-1)*.

The next operation *(4)* is reading the result of the A/D conversion, i.e. the measured output voltage, and storing it in the appropriate register. It is assumed that the A/D converter has finished sampling the output voltage when the ISR reads the A/D converter result. The assumption is valid because the A/D conversion time is constant and can be calculated when the microcontroller software is written. In a typical microcontroller application the software would poll a bit indicating whether the A/D converter has finished the A/D conversion or is in the process of sampling. Polling the A/D converter to ascertain when the A/D conversion has been finished would increase the execution time of the ISR, which must be optimized to get as high a sampling frequency as possible. It was therefore chosen to skip polling the A/D converter and make sure that the A/D conversion has finished by the time the ISR reads the measured output voltage.

Once the A/D converter result has been read the ISR calculates the lookup table address corresponding to the measured output voltage *(5)* with the expression given in equation (3). As already mentioned the range of the error signal *e* is limited in operation *(6)* and *(7)* to reduce the amount of program memory allocated to the lookup tables.

The result of the multiplication of *a* and *e(n)* is read from lookup table #1 and the new dutycycle *d(n)* is calculated and written to the dutycycle register (*(8)*, *(9)* and *(10)*). The division of *d(n)* by 16 in step *9* is done because the coefficients *a*, *b* and *c* have been multiplied by 16 when the lookup tables were generated in MATLAB. The result is that the Least Significant Bit (LSB) in the calculation of the dutycycle represents $1/16^{th}$ thereby increasing the accuracy with which the zeros of the digital controller can be placed in the frequency domain. Dividing by 16 in step *9* ensures that the LSB of the number written to the dutycycle register corresponds to 1, i.e. 2^0, as illustrated in Figure 5.

The complete ISR software routine is made up of 54 assembly commands with a total execution time of 70 command cycles, which is very close to the maximum of 72 command cycles available. An overview of the software partitioning and the execution time for the each partition is given in Table 1.

The microcontroller software described in this section only uses 9 bytes of data memory out of 128 bytes available and about 500 bytes of program memory out of 2kB. It would therefore be possible to add extra software features such as serial communication or special startup routines if the clock frequency of the ATTiny26 wasn't limited to 16 MHZ.

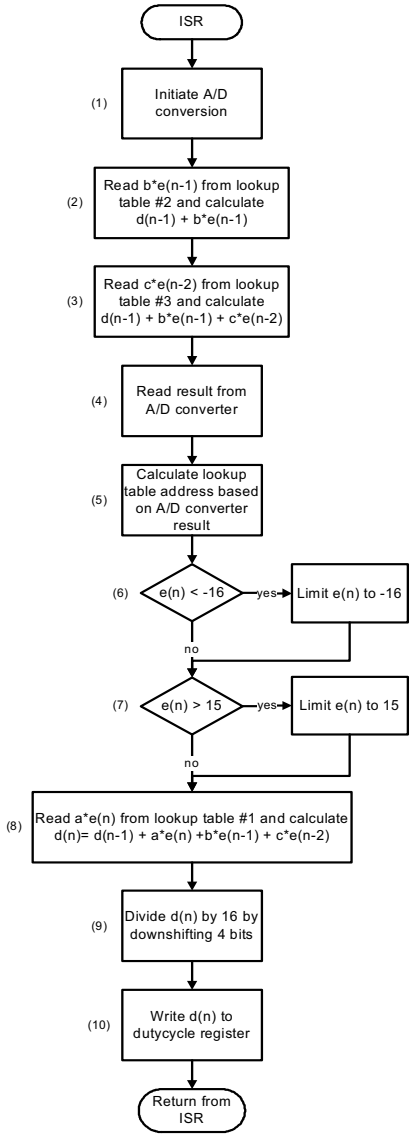


Figure 6: Flowchart of the Interrupt Service Routine

TABLE 1: SOFTWARE PARTITIONING AND EXECUTION TIMES

Function	Execution time in number of clock cycles
Reading data from lookup tables	32
Calculate dutycycles (additions)	16
A/D converter control	9
Error limiting	6
House keeping	7
Hardware interrupt handling	8
Total	78

V. EXPERIMENTAL RESULTS

Two prototypes have been built to compare the two mixed signal control schemes described in section III. The electrical specifications of the two prototypes are given in Table 2.

The differences in switching and sampling frequencies of the two designs were dictated by the fact that an external A/D converter was used in the 'PWM-DAC' prototype while an external D/A converter was used in the 'DAC' prototype.

The A/D converter included in the ATTiny26 is specified as a 10 bit 75 ksps A/D converter but can in practice be programmed for higher sampling rates if a lower resolution is acceptable. Experiments has shown that it isn't capable of sampling at 200 ksps with 8 bits resolution and it is therefore necessary to use an external 1 MSPS A/D converter in the 'PWM-DAC' prototype. For the 'DAC' prototype an external multibit D/A converter had to be added to the hardware and connected to the ATTiny26 and the A/D converter in the ATTiny26 had to be used because it wasn't possible to have both A/D and D/A converter connected externally at the same time. The sampling rate of the A/D converter was reduced to 125 ksps to get 8 bit resolution.

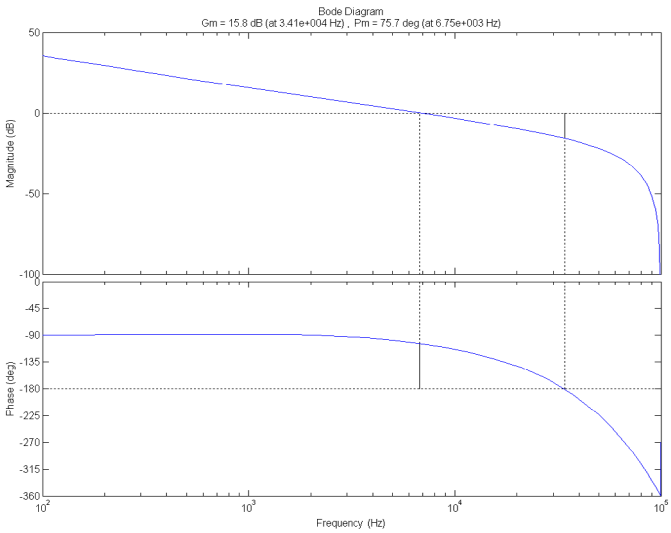
TABLE 2: ELECTRICAL SPECIFICATIONS

	Mixed signal controller "PWM-DAC"	Mixed signal controller "DAC"
Input voltage range	4.5 – 6.0 V	4.5 – 6.0 V
Output voltage	2.0 V	2.0 V
Output current	8 A	10 A
Inductance	2.0 µH	2.0 µH
Output capacitance	300 µF	300 µF
Switching frequency	400 kHz	250 kHz
Sampling frequency	200 kHz	125 kHz
Computational delay	5 µs	4 µs

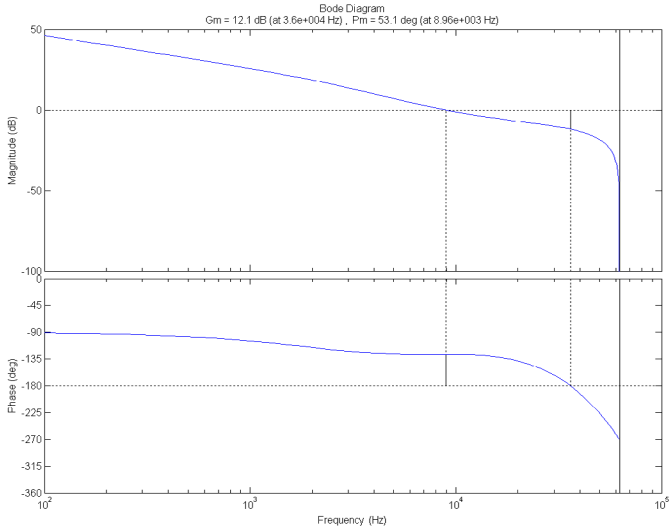
Open loop Bode plots for the two prototypes are shown in Figure 7. The constants a, b and c in the controller transfer (given by equation (1)) has been selected based on root-locus analysis of the converter transfer function. The control loop specifications are listed in Table 3 including the resolution of the A/D and D/A converters.

TABLE 3: CONTROL LOOP SPECIFICATIONS

	Mixed signal controller "PWM-DAC"	Mixed signal controller "DAC"
a	3.0000	6.0000
b	-3.9375	-6.3750
c	1.0625	1.6250
n_{PWM} / $n_{D/A}$	7.3 bit	8 bit
$n_{A/D}$	8 bit	8 bit



(a)

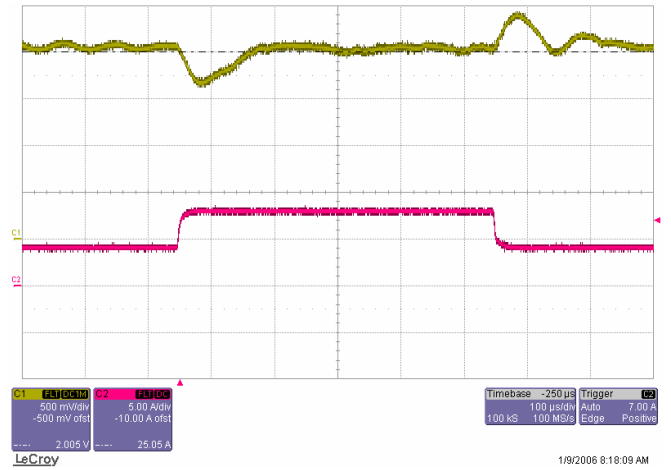


(b)

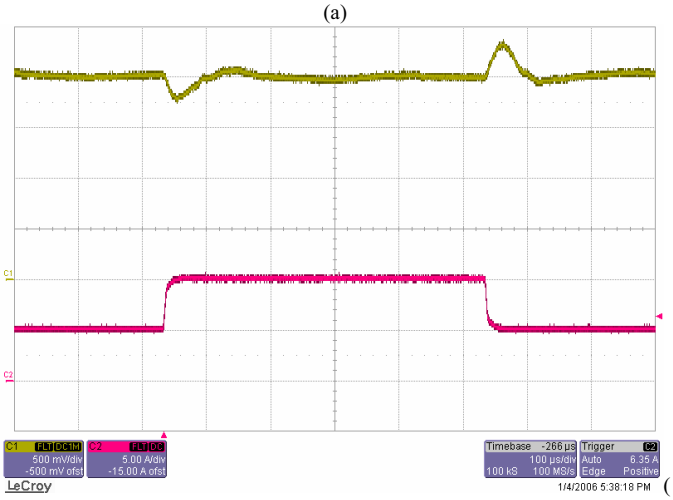
Figure 7: (a) Open loop Bode plot for "PWM-DAC"
(b) Open loop Bode plot for "DAC"

The open loop Bode plots shows that the crossover frequency is higher for the "DAC" prototype than for the "PWM-DAC" prototype as would be expected. The increase in crossover frequency from 6.75 kHz to 8.96 kHz is quite significant. The result of the higher crossover frequency of the "DAC" prototype is lower high frequency output impedance compared to the "PWM-DAC" prototype. The lower output impedance will result in a better loadstep response in terms of smaller overshoot and faster settling time. When comparing the crossover frequency of the two designs it must also be taken into consideration that the sampling frequency of the 'DAC' prototype is lower than the sampling frequency of the 'PWM-DAC' prototype making the increase in loop gain even more significant.

The performances of the two prototypes have been tested by measuring the output voltage response to a loadstep between 50% and 100% of nominal output current (see Figure 8).



(a)



b)

Figure 8:
(a) Loadstep "PWM-DAC". v_{out} (Upper trace) and i_{out} (Lower trace)
(b) Loadstep "DAC". v_{out} (Upper trace) and i_{out} (Lower trace)

A comparison of the two loadstep measurements shows that both the overshoot and settling times are smaller for the "DAC" prototype than for the "PWM-DAC" prototype. The overshoot on the "PWM-DAC" prototype is approximately 0.4V or 20% of nominal output voltage and the settling time is approximately 110µs. For the "DAC" prototype the overshoot and settling times are 0.3V and 75µs respectively and the response is better damped than the response of the 'PWM-DAC' prototype. The loadstep measurements shows that the 'DAC' has the best control loop performance of the two mixed signal control schemes as expected.

The overshoot of the output voltage for the "DAC" prototype is 15% of the nominal output voltage, which is unacceptable in most POL applications. The amplitude of the transient overshoot is determined by the control loop bandwidth of the DC/DC converter and by the size of the output capacitor. The output voltage overshoot is comparable to the measurements shown in [1] if the size of the output capacitor is taken into consideration. Increasing the size of the output capacitor can reduce the output voltage overshoot at loadsteps.

VI. CONCLUSIONS

The mixed signal control scheme based on cheap microcontrollers is an excellent alternative to DSPs in digital control of DC/DC converters. The idea of the mixed signal control scheme isn't a new idea [6], but this paper has shown that high sample rates and good control loop performance can be achieved with cheap 8-bit microcontrollers. The proposed mixed signal control scheme can replace the DSP based solution in most DC/DC converter applications with equally good control loop performance and at a lower cost.

The software design for the microcontroller is crucial if the mixed signal control is to perform well and it will be necessary for the software designer to optimize the software in an iterative process. This means that software development may take longer time than for the DSP based solution.

A 16 MIPS ATMEL ATTiny26 microcontroller can be used as 16-bit PID controller with a sampling frequency of 200kHz. The important feature of the microcontroller software described in this paper is the use of lookup tables stored in the microcontrollers program memory. Without lookup tables it would be impossible to obtain sampling frequencies high enough to be able to control a DC/DC converter with high control loop bandwidth using cheap and simple microcontrollers such as the ATTiny26 from ATMEL. Even though lookup tables are used the memory allocated in the ATTiny26 is only a fraction of the available memory.

The mixed signal controller can be even more competitive if the analogue circuitry used in the current loop is combined with a cheap microcontroller core in a single IC. It would also greatly enhance the possibilities of the mixed signal control scheme if the microcontroller had a higher clock frequency than what commercially available low cost microcontrollers has today.

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18 Appendix D – Publication by L. T. Jakobsen et al.

L. T. Jakobsen and M. A. E. Andersen

"Digitally Controlled Point of Load Converter with Very Fast Transient Response"

European Conference on Power Electronics and Applications 2007, pp. 1 – 10, 2007

Digitally Controlled Point of Load Converter with Very Fast Transient Response

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Keywords

DC power supply, Converter control, Pulse Width Modulation (PWM), Signal Processing

Abstract

This paper presents a new Digital Self-Oscillating Modulator (DiSOM) that allows the duty cycle to be changed instantly. The DiSOM modulator is shown to have variable switching that is a function of the duty cycle. Compared to a more traditional digital PWM modulator based on a counter and comparator the DiSOM modulator allows the sampling frequency of the output voltage control loop to be higher than the switching frequency of the power converter, typically a DC/DC converter. The features of the DiSOM modulator makes it possible to design a digitally controlled DC/DC converter with linear voltage mode control and very fast transient response.
The DiSOM modulator is combined with a digital PID compensator algorithm is implemented in a hybrid CPLD/FPGA and is used to control a synchronous Buck converter, which is used in typical Point of Load applications. The computational time is only three clock cycles from the time the A/D converter result is read by the control algorithm to the time the duty cycle command is updated.
A typical POL converter has been built and the experimental results show that the transient response of the converter is very fast. The output voltage overshoot is only 2.5% of the nominal output voltage when a load step of 50% - 100% of nominal output current is applied to the converter. The settling time is approximately 8 PWM cycles.

Introduction

Digital control of DC/DC converters has developed hugely over the past couple of years. By now digital control has emerged as a real alternative to traditional analogue control methods for DC/DC converters. Modern digital control techniques can meet the demands for fast transient response and accurate control of the output voltage as well as be cost competitive [1]. Several different solutions have been proposed to obtain fast dynamic response in a digitally controlled DC-DC converter, but the way they are implemented varies. The simplest way to implement digital control is to use voltage mode control with a linear compensation scheme [2-4]. The use of linear voltage mode control limits the obtainable control loop bandwidth for single phase DC-DC converters, because the sampling frequency is limited by the switching frequency of the converter. Reference [3] however shows that it is possible for a multiphase interleaved converter to obtain very high control loop bandwidth without increasing the switching frequency.
Another approach is to use digital current mode control [5-7] typically implemented as a predictive average current mode control scheme. Reference [5] presents a digital peak current mode control scheme, which works by sampling the inductor current at a sampling rate of 25MHz, which is very inhibitive in

terms of cost. Digital current mode control in general increases the complexity and thus the cost of the digital controller and does not necessarily lead to better transient responses for the DC-DC converter. Controllers mixing analogue and digital elements have also been proposed for high bandwidth digital control of DC-DC converters [8-9]. The results are promising but a mixed signal design will not lead to simpler system configuration and integrating both analogue and digital elements in one control IC will lead to higher production costs.
Non-linear control for DC-DC converters is another way to obtain fast dynamic response for DC-DC converters [10-11]. The proposed non-linear control scheme of ref. [10] relies on a non-uniform A/D converter, which is a cheap and easy solution with greatly improved dynamic performance. Reference [11] relies on a software implementation, where the control law is changed according to the output voltage error. The disadvantage of this is that the digital controller must perform a number of computations in order to decide which control law to use. This increases the cost of the controller as it has to run at a higher clock frequency, than a controller for a linear control scheme, to be able to sustain a sample rate equal to the sample rate of the linear control scheme.
Common for most of the above mentioned digital control solutions for DC/DC converter is that the PWM modulator is based on the traditional digital counter and comparator based implementation. This PWM modulator implementation imposes limitations on the digital controller implementation.
The problem of the digital PWM modulator is the basic design, which is based on a counter and a comparator. The issue is that the counter counts from zero to a preset value and the counter value is compared to the duty cycle register, which is set by the digital control law, e.g. a PID compensator. The PWM output is high when the counter value is lower than the duty cycle register and changes to low when the counter value exceeds the duty cycle register. The duty cycle register is latched in order to avoid unwanted changes on the PWM output, and the latch is enabled/updated when the counter is reset to zero. Depending on the sampling scheme, i.e. the time the output voltage is sampled in relation to the PWM signal, the delay from the time when the output voltage is sampled to the time when the duty cycle register is updated can be up to one PWM period in state-of-the-art digital control solutions. The time delay results in negative phase shift, which will limit the control loop bandwidth. The update rate of the duty cycle register is limited to once per switching period independent of the sampling scheme.
Most systems sample the output voltage at the beginning of a PWM period and the resulting new duty cycle is latched into the duty cycle register for the following PWM period [2]. In this case the computational delay of the digital controller is not very important as long as it can calculate the new duty cycle during one PWM period. New modulators for multiphase interleaved converters have been proposed that allows the sampling frequency of the output voltage control loop to be higher than the single phase PWM frequency [3]. In this case the computational delay of the digital control algorithm becomes the limiting factor for the control loop bandwidth.
A new digital modulator called a Digital Self-Oscillating Modulator (DiSOM) is presented in this paper along with a digital PID compensator with very short computational delay. An advantage of the DiSOM modulator over counter based PWM modulators is that the duty cycle register can be updated at any instant in time without unwanted shifts on the PWM output. This feature of the DiSOM allows the use of linear control for a DC-DC converter with very fast transient response.

Digital Self-Oscillating Modulator

The DiSOM modulator described in this paper is just one of a family of modulators that are included in a new invention described in reference [14]. The DiSOM modulator (see Fig. 1) is a self-oscillating modulator with a local feedback loop placed around the switching output. The modulator consists of a comparator with hysteresis, a feedback block (MFB) and a forward block (MFW). In this implementation of the DiSOM modulator the feedback block is a simple multiplication/gain but it could also be a digital filter if advantageous. The forward block is a digital integrator and the output of the integrator, also called the carrier, will be a triangular waveform under steady state conditions. The "*Ref*" input defines the duty cycle of the switching output because it affects the slope of the carrier.

 ISBN : 9789075815108

One disadvantage of the DiSOM modulator is that the switching frequency changes with the duty cycle. The switching frequency as a function of the duty cycle command is a parabolic function, which goes to zero for duty cycles equal to 0 and 1. A mathematical derivation of the switching frequency as a function of the duty cycle is derived in the following subparagraph.
Fig. 2 shows a simulated example of the transient response of the DiSOM modulator to a change on the reference input, "*Ref*". The reference input is changed from 0.8 to 0.2 in the middle of a switching period at $t = 7.5\mu s$. The output of the DiSOM change from high to low almost immediately after the reference input is changed and the new duty cycle can be observed after $t = 8.0\mu s$. This ability to change the duty cycle in the middle of a switching period allows the control system to react faster to transient conditions, such as a load step.

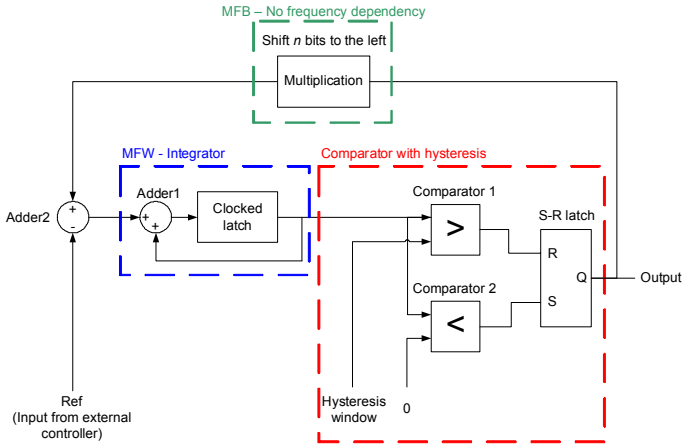

Fig. 1: Block diagram of the DiSOM modulator

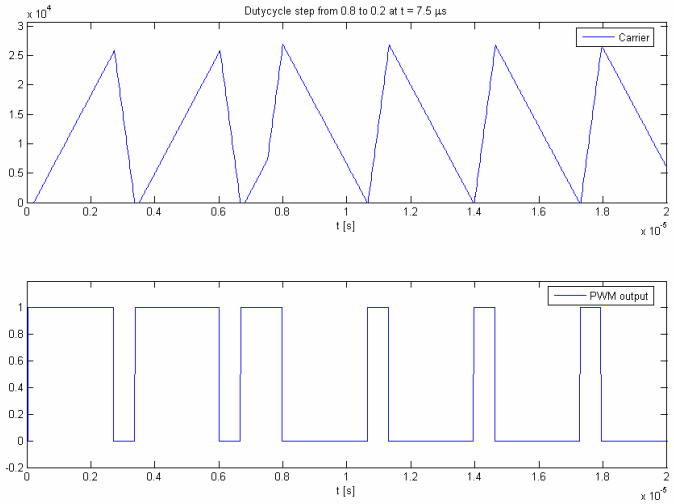

Fig. 2: Duty cycle change from 0.8 to 0.2 for the DiSOM modulator

Derivation of the switching frequency versus duty cycle for the DiSOM modulator

The switching frequency of the DiSOM modulator of Fig. 1 can be derived from a time domain analysis of the system. Fig. 3 shows the internal signals of the DiSOM modulator. The mathematical expression for the switching frequency is derived without taking into account the discrete time nature of the DiSOM modulator. That means that it is assumed that the carrier will oscillate between 0 and the hysteresis window, *Window*, without exceeding either limit due to clock frequency quantization.

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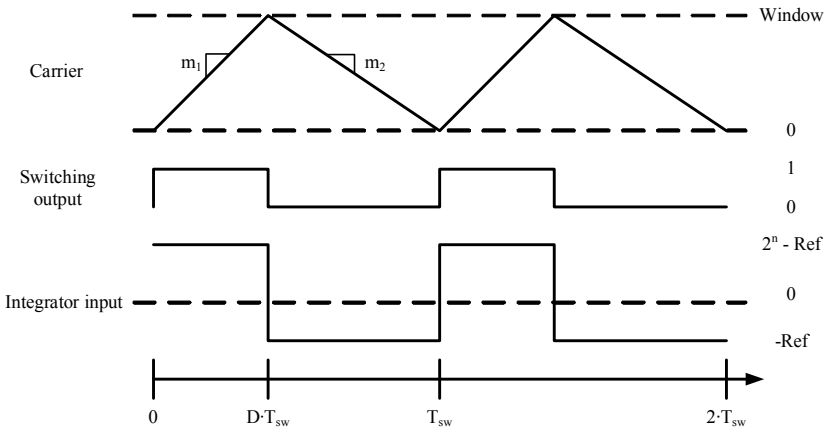

Fig. 3. Internal signals of the DiSOM modulator

The slopes of the carrier m_1 and m_2 depend on the integrator input and the clock frequency of the system (see equation (1) and (2)). The variable n is the number of bits used to represent the reference input, *Ref*, in the digital implementation of the DiSOM modulator and f_{clock} is the clock frequency.

$$m_1 = \left(2^n - Ref\right) \cdot f_{clock} \tag{1}$$

$$m_2 = -Ref \cdot f_{clock} \tag{2}$$

During the ON period of the switching output the carrier will change from *0* to *Window* and during the OFF period it will return to 0. The switching frequency is calculated by equating the ON time of the switching signal with the change in the carrier signal during the ON time as expressed in equation (3).

$$D \cdot T_{sw} = \frac{Carrier\left(T_{sw}\right) - Carrier\left(0\right)}{m_1} = \frac{Window}{\left(2^n - Ref\right) \cdot f_{clock}} \tag{3}$$

Finally by inserting the relationship between the reference input, *Ref*, and the duty cycle, *D*, (see equation (4)) into the expression for the switching frequency it is possible to derive a mathematical expression for the switching frequency as a function of the duty cycle (see equation (5)).

$$D = \frac{Ref}{2^n} \tag{4}$$

$$f_{sw}\left(D\right) = \frac{2^n \cdot f_{clock}}{Window} \cdot \left(D - D^2\right) \tag{5}$$

Digital controller implemented in a Hybrid FPGA/CPLD

A special digital PID compensator has been designed in VHDL and implemented in a hybrid CPLD/FPGA (LCMXO1200C) from Lattice semiconductor. The computational delay of the PID algorithm is nine clock cycles from the instant of sampling the output voltage to the time the duty cycle input of the DiSOM is updated. The digital PID controller is implemented with the specific purpose of working as a PID controller and it can not easily be changed. The advantage of the implemented PID compensator compared

to a more conventional Digital Signal Processor (DSP) implementation [12] is that because it is specifically designed as a PID compensator, it can be optimized to give as short a computational delay as possible. In this way the complexity of the digital hardware can be optimized as well.
A principal block diagram of the PID compensator is shown in Fig. 4. The Digital PID compensator is implemented using a lookup table stored in non-volatile memory rather than with a multiplier/accumulator structure as known from DSPs. The digital PID compensator has the discrete time transfer function of equation (6) and the digital implementation must calculate the result of a difference equation (equation (7)) in order to implement the PID compensator.

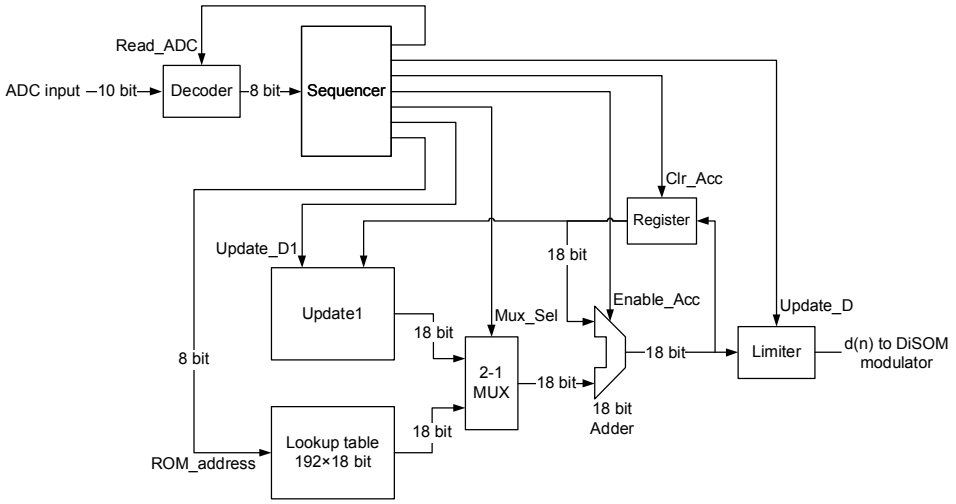

Fig. 4: Block diagram of digital PID compensator implementation in the FPGA

$$G_{PID}(z)=\frac{d(z)}{e(z)}=\frac{b_0+b_1\cdot z^{-1}+b_2\cdot z^{-2}}{1-z^{-1}} \tag{6}$$

$$d(n)=d(n-1)+b_0\cdot e(n)+b_1\cdot e(n-1)+b_2\cdot e(n-2) \tag{7}$$

where b_0, b_1 and b_2 are constant coefficients, d is the duty cycle command, e is defined as the difference between the output voltage reference and the measured output voltage and n is the sample number.
A short functional description of each block in Fig. 4 is given below:

- Sequencer – The sequencer is a state machine that controls the timing of the digital PID compensator. A counter clocked by the system clock is counting from 0 to 63 and is used to define the states. The control signals for the other blocks of the PID compensator are defined for each state. A timing diagram for the operation of the PID compensator is shown in Fig. 5.
- Decoder – The Decoder takes the A/D converter (ADC) result, which is 10 bit wide, and calculates the appropriate address for the lookup table for the error *e(n)*. The ADC result is 10 bits because a 10 bit ADC is mounted on the FPGA development board but the error is reduced to 6 bits in order to reduce the size of the lookup table. The Read_ADC signal from the Sequencer commands the Decoder to update the 8-bit address based on the current ADC result.
- Lookup Table – The Lookup Table holds the results of the multiplication of *e(n)*, *e(n-1)* and *e(n-2)* by b_0, b_1 and b_2 respectively. The Lookup Table has an 8-bit address input in order to address the 192 positions in the table. That is 64 positions for each error signal, i.e. *e(n)*, *e(n-1)* and *e(n-2)*. The result of each multiplication is 18 bits wide and the five least significant bits are used to represent fractions of 1. That means that each of the coefficients b_0, b_1 and b_2 can be adjusted in

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steps of 1/32 (0.03125) and the coefficients can take on values in the range of -64 to +64. The Lookup Table is stored in a special memory area of the FPGA and takes up 432 bytes of memory.

- Update1 – Update1 takes the duty cycle calculated as *d(n)* and stores it for use as *d(n-1)* for the next run of the PID algorithm. Update1 also limits the duty cycle to the range from 0 to 1, so that internal overflow can not occur in the compensator. Update1 is controlled by the Update_D1 signal.
- 2-1 MUX – This is a two input multiplexer, which is used to select if the output of either Update1 or the Lookup Table is fed to the Accumulator. The multiplexer is controlled by the Mux_sel signal.
- Accumulator – The Accumulator is composed of the 18-bit Adder and the Register. The Register holds the result of the Accumulator and is connected to one input of the adder. The Accumulator can be cleared by the setting the Clr_Acc signal high and enabled by setting Enable_Acc high.
- Limiter – The Limiter has two functions. The first is to limit the duty cycle from approximately 0.01 to 0.99 and the other is to reduce the 18 bit result of the Accumulator to a 10 bit representation for the DiSOM modulator. The output of the Limiter is updated by pulling Update_D high.

The timing diagram of Fig. 5 shows that the Read_ADC signal is asserted at state no. 4 and the Update_D signal is asserted state no.7. This corresponds to a delay of three clock cycles but the total delay of the actual implementation is nine clock cycles as already stated. The extra delay is due to the choice of ADC, which for the FPGA development board is a 10 bit pipelined ADC. The pipelined ADC has 5 pipeline stages resulting in a total sampling delay of 6 clock cycles. The ADC is running on the same clock as the FPGA and the thus the total delay, i.e. sampling + computational delay, is nine clock cycles. If a flash ADC had been used instead, the total delay could be reduced to four clock cycles reducing the negative phase shift caused by the delay even further.
The ROM_address signal takes on three values (Address0, Address1 and Address2) during the computation of the duty cycle. The three addresses refer to each of the three values that must be read from the lookup table. Address0 refers to the present error, *e(n)*, Address1 to the previous error *e(n-1)*, and Address2 to the error of two samples previously, *e(n-2)*.

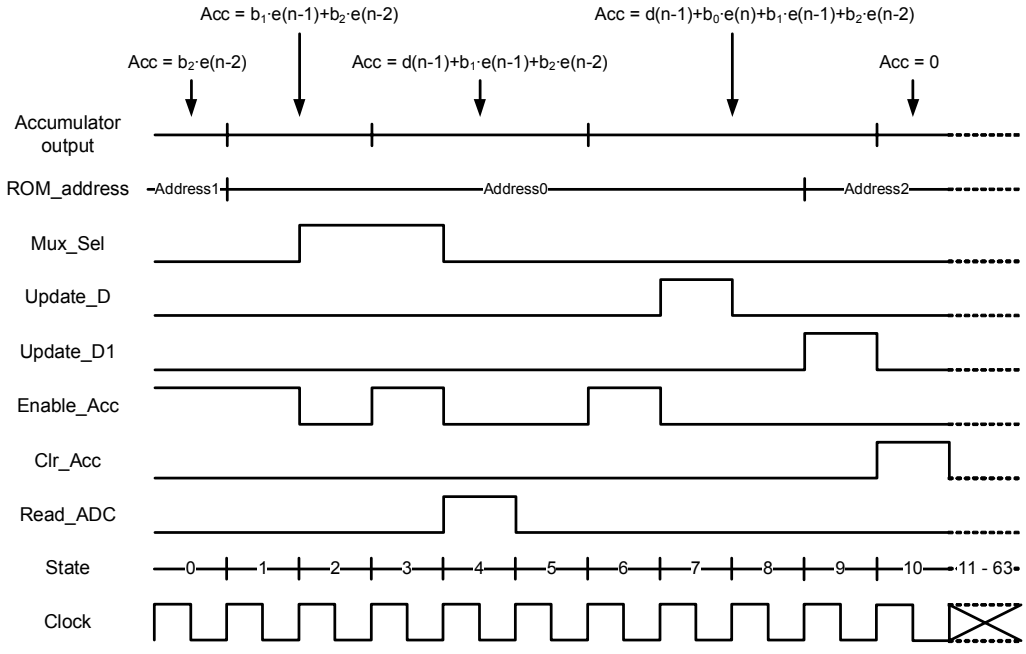

Fig. 5: Timing diagram for the digital PID compensator implementation

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The total computation time is eleven clock cycles and the maximum sampling frequency is limited to one eleventh of the clock frequency. This is due to the fact that delays have to be inserted in the algorithm because of the need for pipelining signals in the FPGA. The time it takes to complete the algorithm could be reduced further by using a parallel implementation of the PID compensator as proposed in ref. [13]. A parallel implementation does on the other hand increase the complexity and price of the digital control solution and in most cases it will not be necessary to run at very high sampling frequencies.

Experimental results

A Buck converter with synchronous rectification has been built and tested together with DiSOM modulator and digital PID compensator blocks implemented in the Lattice Semiconductor LCMXO1200C CPLD/FPGA and with the ADC10065 ADC from National Semiconductor. The specifications for the Buck converter and control scheme are given in Table I and the specifications for the digital implementation of the DiSOM modulator and PID compensator are given in Table II. The output capacitance is four 100µF ceramic capacitors in parallel to achieve as low equivalent series resistance and inductance as possible. The Buck converter design has been optimized for efficiency since the purpose of the design was to prove the feasibility of the proposed digital controller.
A picture of the experimental setup is shown in Fig. 6, where the FPGA development board is on the left and the Buck converter PCB is on the right. Fig. 7 shows a block diagram of the prototype setup.

Table I: Prototype specifications

Parameter	Value
Input voltage	9 – 15 V
Output voltage	2.0 V
Output current	0 – 10 A
Inductor size	1.5 µH
Output capacitance	400 µF
Output capacitance ESR	<2 mΩ
Nominal switching frequency @ D = 0.5	625 kHz

Table II: Specifications for the digital controller

Parameter	Value
Clock frequency	50MHz
Reference input resolution	10 bit
Hysteresis window	20480
Effective ADC resolution	6 bit
Effective ADC range	1.419 – 1.481V
Sampling frequency	800 kHz

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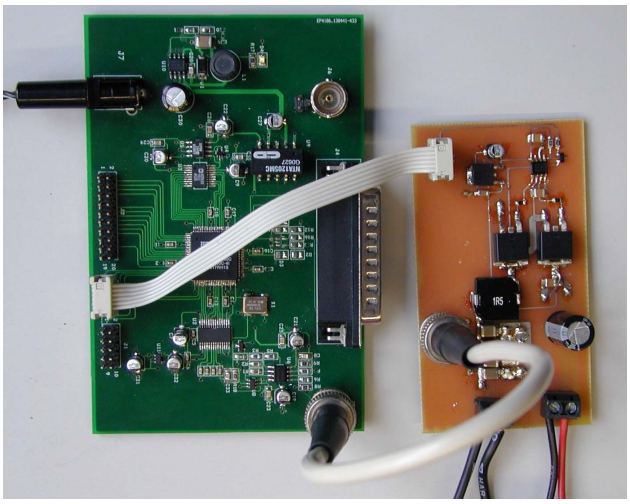

Fig. 6: The experimental setup. FPGA/CPLD board on the left and Buck converter PCB on the right

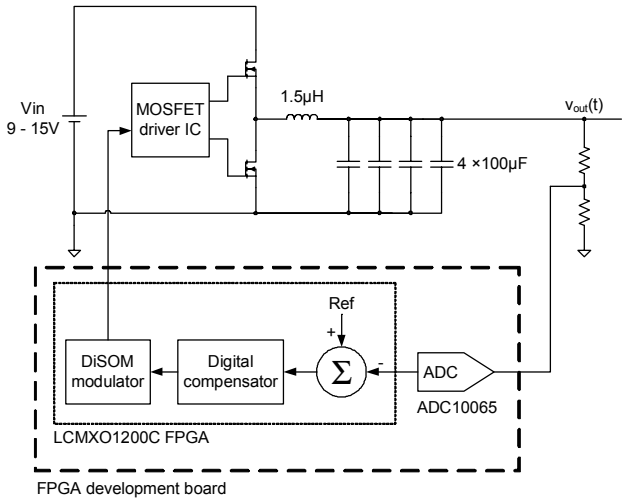

Fig. 7: Block diagram of the prototype setup

The digital PID compensator transfer function for the prototype design is given in equation (8).

$$G_c(z) = \frac{12.8125 - 22.6875 \cdot z^{-1} + 9.9375 \cdot z^{-2}}{1 - z^{-1}} \tag{8}$$

Fig. 8 shows the theoretical and measured open loop Bode plots for the prototype. The computational delay of the digital PID controller has been included in the theoretical small signal model of the system, so the two Bode plots are comparable. The prototype has a phase margin of 60 degrees and a crossover frequency of 37 kHz. The gain margin is 22 dB at 151 kHz. At frequencies higher than the crossover frequency the prototype has more negative phase shift than the model, which is probably due to the fact that the DiSOM modulator will have a delay of one or two clock cycles which hasn't been included in the model. The resonant peak at the output filter resonance frequency is not apparent in the experimental measurement, which is not easily explained. One explanation could be that the Gain/Phase analyzer, used to measure the Open loop transfer function, increased the test frequency in too large steps around the resonant frequency, thereby missing the resonant peak.

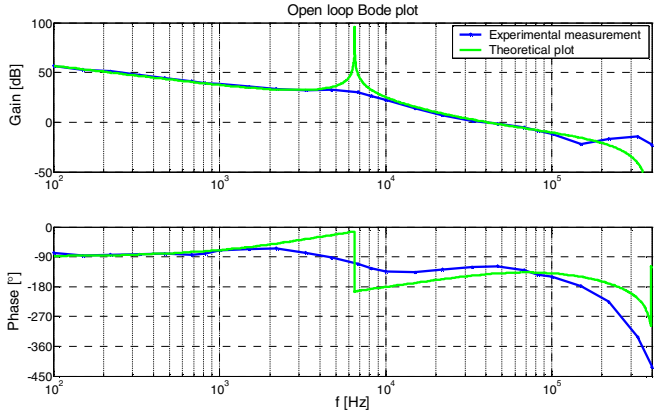

Fig. 8: Theoretical and measured open loop Bode plots

The transient response to a 50% load step has been measured for both positive and negative load steps, see Fig. 9. The upper trace is the output voltage with the oscilloscope AC coupled (20mV/div) and the lower trace is the output current (5A/div). The time scale of the measurements is 10µs/div. During the load step

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the output current has a rate of change of approximately 1A/µs, which was limited by the electronic load used in the experiment. Simulations have shown that the converter performs almost as well if the rate of change is 100A/µs. The output voltage overshoot is 50 mV, which is 2.5% of the nominal output voltage and the settling time is approximately 20 µs.
Fig. 10 is a measurement of the output during steady state conditions. The upper trace is the output voltage (AC coupled 10mV/div) and the lower trace is the output current (5A/div). The trace in the middle shows the switch node voltage of the Buck converter (10V/div) and it shows that the switching frequency is a little below 500 kHz at nominal output current. The output voltage has a non-periodic limit cycle with an amplitude of 12 mV or 0.6% of the nominal output voltage. The limit cycling can to a certain extent be explained by the fact that the ADC measurement is disturbed by switching noise. It is however also attributable to the fact that the output voltage is sampled at faster rate than switching frequency and with a very high resolution, which means the output voltage ripple is sampled and fed through the digital compensator. This will disturb the PWM signal generated by the DiSOM and may cause the output voltage to limit cycle.

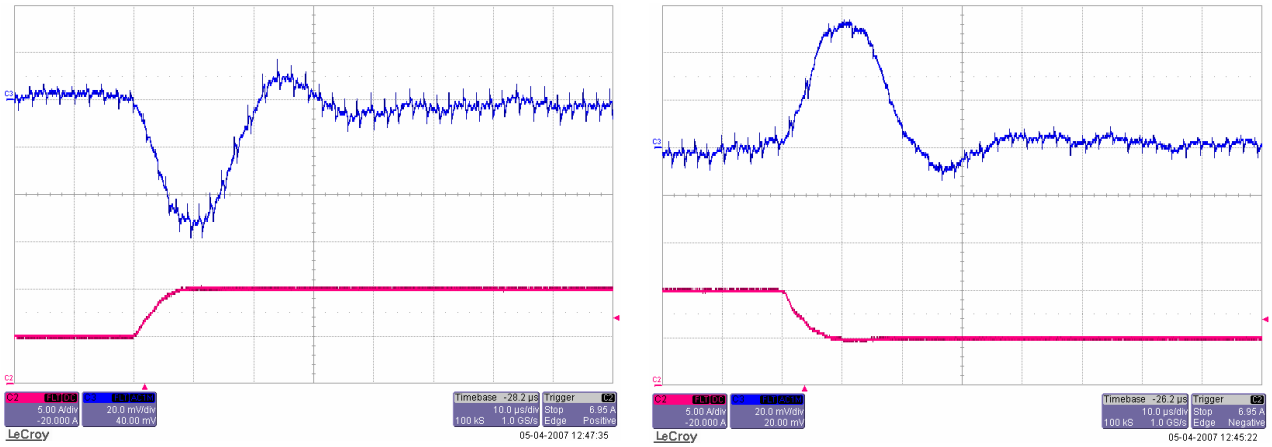

Fig. 9: Positive load step from 5A to 10A (V_{in} = 12V).
Upper trace: V_{out} 20mV/div, Lower trace: I_{out} 5A/div, Time scale: 10µs/div

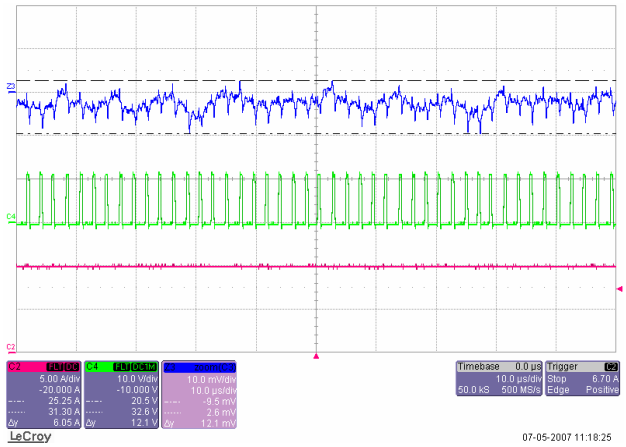

Fig. 10: Limit cycling on the output voltage (V_{in} = 12V, I_{out} = 10A). Upper trace: V_{out} 10mV/div
Middle trace: Switch node 10V/div, Lower trace: I_{out} 5A/div, Time scale 10µs/div

Conclusion

A new Digital Self-Oscillating Modulator (DiSOM) based on a local feedback loop around the switching output has been presented. The duty cycle command of the DiSOM modulator can be updated at any

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instant in time irrespective of the state of the output. This gives the DiSOM modulator the ability to change its duty cycle at any time and makes it possible for a linear control loop to sample the output voltage at a higher rate than the switching frequency thereby enabling higher control loop bandwidth.It has been shown that the switching frequency of the DiSOM modulator is a parabolic function with maximum switching frequency at a duty cycle of 0.5 and going towards zero for duty cycles equal to 0 or 1.

A digital PID compensator has been implemented in a hybrid CPLD FPGA, resulting in a computational delay of just three clock cycles between availability of the ADC result and the following update of the duty cycle command. The total delay from the instant the output voltage is sampled until the duty cycle command is updated is nine clock cycles because a pipelined ADC was used.

The DiSOM modulator and digital PID controller have been combined in a digital controller for a low voltage synchronous Buck converter. The experimental results show that the converter has high control loop bandwidth and very fast transient response. For a load step from 50% to 100% of nominal output current the output voltage overshoot is 2.5% of nominal value and the settling time is equal to approximately eight switching cycles.

There is some non-periodic limit cycling on the output but it is mainly caused by noise on the output voltage that disturbs the control loop. The limit cycling is approximately 0.6% of nominal output voltage.

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19 Appendix E – Publication by L. T. Jakobsen et al.

L. T. Jakobsen and M. A. E. Andersen

"Digitally Controlled Envelope Tracking Power Supply for an RF Power Amplifier"

IEEE International Telecommunications Energy Conference 2007, pp. 636 – 642, 2007

Digitally Controlled Envelope Tracking Power Supply for an RF Power Amplifier

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***Abstract* – A new Digital Self-Oscillating (DiSOM) modulator is presented in this paper. The advantage of the DiSOM is that it allows the sampling frequency of the digital compensator to be higher than the switching frequency, but it also has the ability to shape the quantization noise on the switching output due to clock frequency quantization. An envelope tracking power supply for an RF Power Amplifier (RFPA) can help improve system efficiency by reducing the power consumption of the RFPA. To show the advantage of the DiSOM over traditional counter based Digital PWM modulators two designs were compared in both simulation and by experiment. The results shows that the DiSOM could give an increase in open loop bandwidth by more than a factor of two and an reduce the closed loop output impedance of the power supply by a factor of 5 at the output filter resonance frequency.**

I. INTRODUCTION

The efficiency of an RF Power Amplifier (RFPA) transmitting an amplitude modulated signal can be improved by using an envelope tracking power supply that tracks the envelope of the RFPA. For a given instantaneous output power level, the RFPA supply current is constant and the power consumption is proportional to the input voltage. By adapting the supply voltage of the RFPA to the RF output amplitude the power consumption of the RFPA can be reduced considerably. Fig. 1 shows a block diagram of how a RFPA can be combined with an envelope tracking supply. The baseband processor and modulator block generates the RF input for RFPA and the RF envelope signal, which is used as a reference for the tracking power supply. The tracking power supply is in this case digitally controlled. The tracking power supply generates an output voltage proportional to the reference signal. The bandwidth of the tracking power supply is important in two ways. Firstly high control loop bandwidth makes it possible for the tracking power supply to generate an output voltage with short rise and fall times. Secondly high control loop bandwidth will result in low output impedance which is important so as not to distort the RF output because of fluctuations in the RFPA supply voltage. For the same reason it is desirable to have low ripple voltage on the power supply output which would generally be solved by using a large output capacitance and high switching frequency. If on the other hand the tracking power supply must be able to track a high frequency reference signal a large output capacitor is undesirable.

Several papers have proposed solutions for similar application using either analogue or digital control schemes [1-4]. The output voltage and power ranges of the different solutions previously published vary largely and it is therefore hard to make comparisons. Reference [1] presents a combination of a digitally controlled DC/DC converter and an RFPA for battery powered applications. The DC/DC converter does not track the envelope of the RF output but is used to optimize the DC supply voltage to achieve maximum efficiency. Envelope tracking power supplies are presented in [2-4] with closed loop bandwidth ranging from 3.5kHz to 50kHz. The preferred converter in [2] and [4] is a four phase interleaved buck converter. This converter topology was chosen in order to reduce output voltage ripple whereas [4] uses a single Buck stage with a 4^{th} order output filter. The digitally controlled solution of [3] has the lowest open loop control bandwidth and shows the need for a better digital control solution.

In this paper a new Digital Self-Oscillating Modulator (DiSOM) is presented enabling the design of a high bandwidth digitally controlled envelope tracking power supply. The advantage of the DiSOM is that it allows the digital compensator to sample the output voltage at a sample frequency which is higher than the switching frequency. To show the advantage of the DiSOM over more traditional counter based digital PWM modulators (DPWM) two designs have been simulated and tested experimentally. The first design is based on the Texas Instruments Digital Signal Controller (DSC) TMS320F2801, which has a special high resolution counter based DPWM, and the second design is based on the DiSOM modulator implemented in an FPGA.

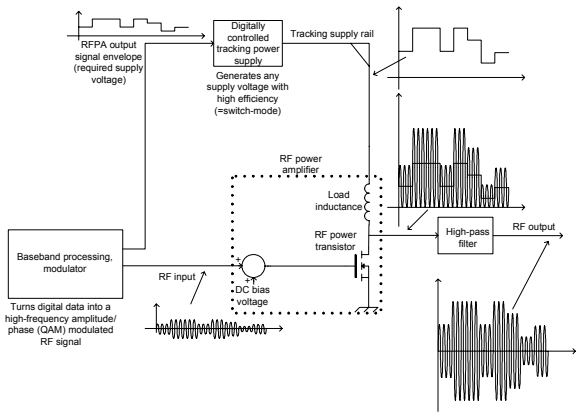

Fig. 1: Block diagram of RFPA system with tracking power supply

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TABLE I lists the basic specifications of the tracking power supply and the RFPA used in the comparison of DiSOM versus DPWM. The specifications does not address a specific application but was selected to represent a typical RFPA application on which it would suitable to compare the DiSOM against the typical counter based DPWM.

TABLE I
RFPA AND TRACKING POWER SUPPLY SPECIFICATIONS

Parameter	Value
RFPA output power - Continuous wave	80W
RFPA supply voltage	12 – 28V
RFPA supply current – average	1A
RFPA supply current – peak	5A
Frequency range of interest	DC – 50kHz

No specific design goals have been set for other important parameters such as output impedance and reference to output bandwidth and the goal is to achieve the best possible performance, i.e. the lowest possible output impedance and the highest possible reference to output bandwidth.

II. THE DISOM MODULATOR

Designing a digital PWM modulator with high switching frequency and high duty cycle resolution has been the subject of intense research in the past years. Many different solutions have been proposed and they almost all have in common that the basic carrier is generated by a counter [5-7]. Fig. 2 shows a block diagram together with a representation of the basic operation of a counter based digital PWM modulator (DPWM). The PWM output is generated by the S-R latch which is set to high when the counter value is equal to zero. The duty cycle value *d(n)* is read into the shadow register at the beginning of the switching period, i.e. at the same time the PWM output is set to high. The shadow register is used to avoid spurious switching in the middle of switching period if *d(n)* is changed by the digital compensator. The PWM output is reset to low when the counter value is equal to the duty cycle value in the shadow register. The counter is a free running counter that will reset to zero when it reaches a predefined value, which controls the duration of the switching period. The maximum sampling frequency of the digital compensator is limited to the switching frequency because the shadow is updated once per switching period. In practice it is possible to sample the output voltage at a higher rate than the switching but it will not improve the control loop bandwidth of the switching converter since the update rate of the control signal is limited by the shadow register.

The basic operation of the counter based DPWM in Fig. 2 is shown below the block diagram. At the time the counter is reset to zero the value of *d(n)*, i.e. 6, is read into the shadow register. Even though the value of *d(n)* is changed from 6 to 4 in the middle of the first switching period the duty cycle is still 6/8 (0.75) because of the shadow register. In the next switching period the duty cycle is 4/8 (0.5).

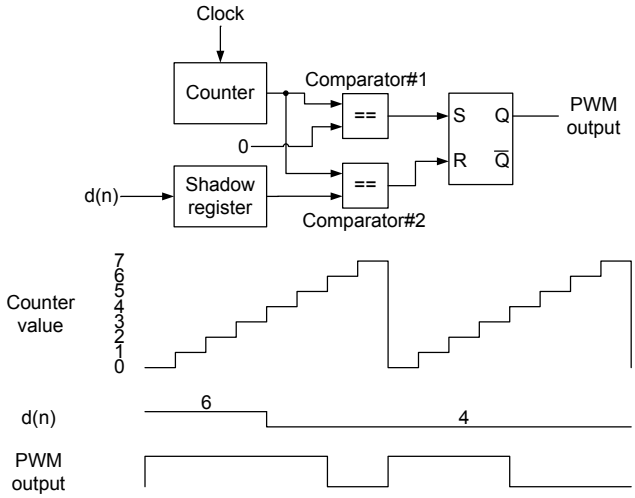

Fig. 2: Block diagram and priciple of operation for counter based DPWM

A block diagram of the Digital Self-Oscillating Modulator is shown in Fig. 3. This is just one of a family of Digital Self-Oscillating Modulators described in [8]. The general features of the DiSOM family is that it includes one or more control loops that include the switching output in the control loop and it has no free running counter to set the switching frequency. The DiSOM of Fig. 3 is characterised by being a purely digital modulator that receives a duty cycle command (*Ref*) from en external source, typically the digital compensator that calculates the required duty cycle to adjust the output voltage to the reference setpoint.

The DiSOM consists of three main blocks. The first block is a comparator with hysteresis that generates the switching output based on the input signal, that is called the carrier. The carrier is generated by the main forward block (MFW), which in this case is a digital integrator. The integrator input is the difference between the signal generated by main feedback block (MFB) and the *Ref* input. In this case the MFB is a simple multiplication with no frequency dependency.

Fig. 4 shows an example of the carrier signal and switching output of the DiSOM modulator for three different duty cycle values. The carrier is a trianguler wave form as would be expected since the integrator is integrating a square wave. One of the defining features of the DiSOM is that the switching frequency is dependent of the duty cycle. The switching frequency can be expressed as a function of the duty cycle

$$f_{sw}(D) = \frac{2^n \cdot f_{clock}}{Window} \cdot \left(D - D^2\right) \qquad (3)$$

where D is the duty cycle, n is the number of bits used to represent the *Ref* input, f_{clock} is the clock frequency of the integrator and *Window* is the hysteresis window [9].

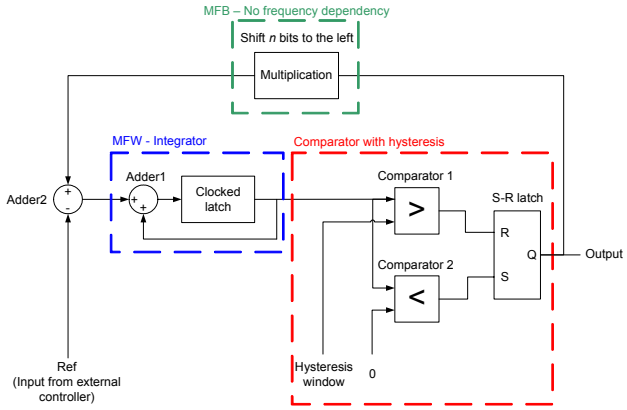

Fig. 3: Block diagram of the DiSOM modulator

The structure of the DiSOM modulator allows the *Ref* input to be changed at any time. If the *Ref* input is changed during a switching period it will affect the slope of the carrier but it will not directly affect the switching output.

Another important feature of the DiSOM is that the switching output is fed back to the integrator whereby any noise due to clock frequency quantization is integrated. Thus the DiSOM is automatically correcting for quantization noise on the switching output. It can be compared to a noise shaper used in digital audio to reduce total harmonic distortion. The choice of transfer function for the MFW and MFB can be used to shape the quantization noise spectrum on the switching output.

III. DPWM VERSUS DISOM

Two different control schemes for the envelope tracking power supply are presented in this section. The first design is based on the Texas Instruments TMS320F2801 Digital Signal Controller (DSC) and uses the counter based high resolution DPWM module included in the DSC. The TMS320F2801 has a clock frequency of 100MHz and includes peripherals such as six high resolution DPWM modules and a 12 bit Analogue to Digital Converter (ADC) with a sampling time of 160 ns.

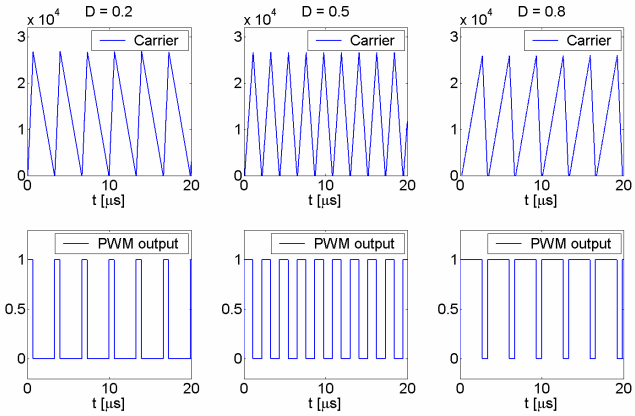

Fig. 4: DiSOM waveforms for three different duty cycle values

Fig. 5 shows a block diagram of the first design. The power conversion stage is a Buck converter with synchronous rectification. The output voltage is subtracted from the analogue reference voltage before the error voltage is sampled by the ADC of the TMS320F2801. The analogue reference is lowpass filtered in order to avoid large overshoot and ringing on the output voltage. The phase margin of the control loop would typically have to be greater than 90 degrees if a square wave reference is applied directly to the compensator and no overshoot is allowed. By performing the initial subtraction of the output and reference voltage the ADC only needs to sample one voltage, i.e. the error voltage, rather than both the reference voltage and the output voltage. If a digital reference was supplied it would be preferable to sample the output voltage directly and do the subtraction in the DSC.

A digital PID compensator with two zeroes and an integrator (see (2)) has been written in C code and it has an execution time of approximately 1µs including the 160ns sampling time of the ADC. The control algorithm samples the error signal at the beginning of a switching period and calculates the duty cycle before the beginning of the next switching period.

$$G_{comp}(z) = \frac{b_0 + b_1 \cdot z^{-1} + b_2 \cdot z^{-2}}{1 - z^{-1}} \qquad (2)$$

The second design is the DiSOM based design with a custom designed digital compensator implemented in an FPGA. The FPGA used is the LCMXO1200C from Lattice Semiconductor and it has a clock frequency of 50 MHz. The FPGA development board used in the prototype is a 10 bit pipelined ADC (ADC10065) from National Semiconductors.

Once again the output voltage is subtracted from the reference in an analogue difference amplifier as in the DPWM based design. This method was actually adapted because the pipelined ADC has an input voltage range from 0.95V to 1.95V. The pipelined ADC therefore would not be able to measure an attenuated version of the output voltage directly since it can not measure voltages down to zero Volts.

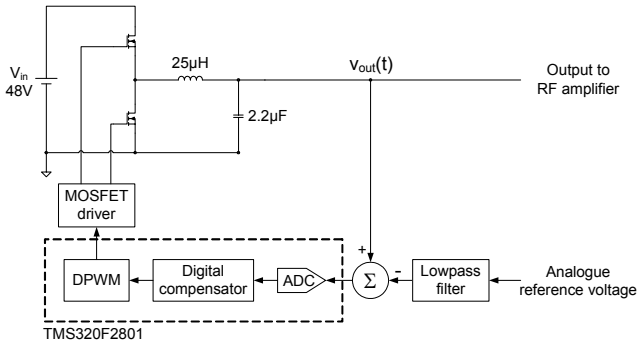

Fig. 5: Block diagram for the TMS320F2801 DSC based design

The digital PID compensator of the DiSOM based design has the same basic transfer function as the DPWM based design but it is implemented using lookup tables rather than a hardware multiplier/accumulator module. The lookup tables stores the results of the three multiplications of b_0, b_1 and b_2 with the current and past error signals. A special ADC decoding scheme has been implemented to reduce the size of the lookup tables (see Fig. 7). The idea behind the decoding scheme is that high resolution is needed when the error signal is close to 0 but as the error increases it is acceptable to increase the quantization steps. Alternatively the error signal could have been limited to a small range around 0 but it was found that this slowed down the step response of the converter if a large step occurs on the reference. The internal resolution of the digital PID compensator is 24 bits and the ADC decoding schemes has 85 values, resulting in a total memory allocation for the lookup tables of 765 bytes. A detailed description of a similar lookup table based PID compensator can be found in [9].

The main difference between the two designs is that the sampling frequency of the DiSOM based implementation is twice that of the DPWM based design and that the computational time of the digital compensator is shorter for the DiSOM based design. The system specifications for the two digital controller implementations are given in TABLE II.

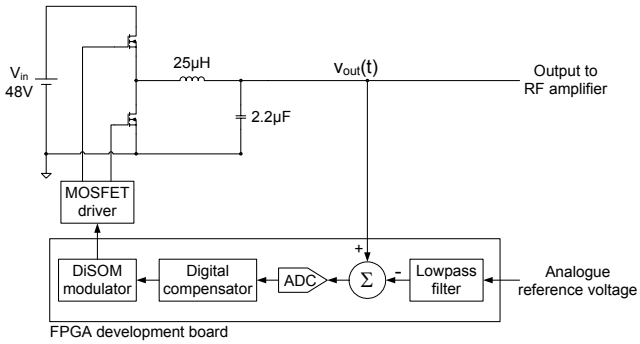

Fig. 6: Block diagram for the DiSOM based design

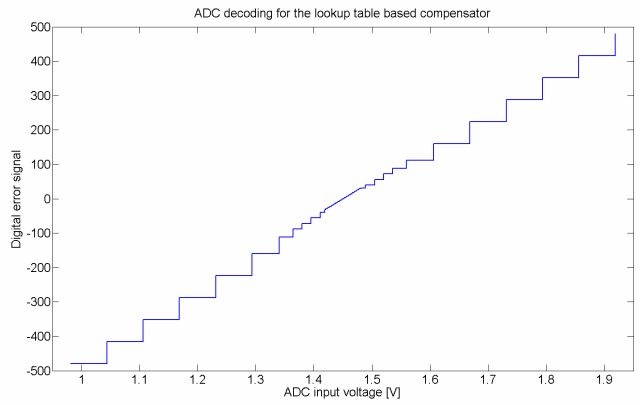

Fig. 7: ADC decoding scheme for the look table based compensator

TABLE II
DIGITAL CONTROLLER PARAMETERS

Parameter	DPWM	DiSOM
Clock frequency	100 MHz	50 MHz
Sampling frequency	500 kHz	1 MHz
Switching frequency	500 kHz	500 kHz*
Duty cycle command resolution	13.6 bit	10 bit
PID compensator internal resolution	32 bit	24 bit
Sampling + computational time	2 µs	200 ns
b_0	20.875	4.875
b_1	-39.1875	-9.28125
b_2	19.625	4.5

*Nominal switching frequency @ D = 0.5. Hysteresis window = 25600

IV. SIMULATIONS AND EXPERIMENTAL RESULTS

A set of hardware specifications for the envelope tracking converter have been selected and the system has been simulated in Matlab/Simulink before the prototype hardware was build and tested. The input voltage is 48V and the output voltage range is 10 to 30V. The output filter inductor is 25µH and the output capacitor is 2.2µF which gives a filter resonance frequency of 21.5kHz. All simulations and measurements have been made under no-load conditions, which is the worst case condition for the control loop.

The Matlab/Simulink models for the DPWM and DiSOM design are switching models and take into account such things as quantization in the fixed point calculations, computational delays and the series resistance of the inductor to make the model as accurate as possible.

Fig. 8 shows the output ripple voltage as a function of duty cycle. The simulation has been performed by setting the reference voltage to a level that corresponds to the specified duty cycle and measuring the peak-peak ripple voltage. The simulation has been performed a number of times to generate the plot of in Fig. 8. The simulation of the output ripple shows that the maximum ripple voltage of the DPWM design is 100mV while the maximum ripple voltage of the DiSOM design is 350mV. This is clearly in favour of the DPWM design and the reason it has lower ripple voltage for duty cycle values close to 0 and 1 is that the switching frequency is constant. The switching frequency of the DiSOM design falls to approximately 150kHz for duty cycle values of 0.1 and 0.9 (see Fig. 9) whereas the switching frequency of the DPWM is constant at 500kHz. It should be noted that the duty cycle will vary from 0.2 to 0.6 in the defined output voltage range and that the maximum ripple voltage in this case is approximately 200mV. The ripple voltage is in general quite high for the application and it would be advantageous to increase either the switching frequency or the size of the output capacitor to improve the performance of the system.

The loop gain and output impedance and step response have both been simulated and tested experimentally. Fig. 10

shows a picture of the prototype PCBs of the DiSOM based design. The same Buck converter power stage was used with the Texas Instruments TMS320F2801 ezDSP board and a small PCB with the analogue difference amplifier for the DPWM based prototype.

The simulation and measurement results for the loop gain are presented in Fig. 11 and Fig. 12 for the DPWM and DiSOM solutions. The resonance frequency of the output filter is slightly higher in the measurements, which is due to component tolerances. The open loop bandwidth and phase margin of the DPWM prototype are 43.2kHz and 30.7 degrees respectively and the gain margin is 3.9dB at a frequency of 66.5kHz. For the DiSOM prototype the open loop bandwidth is 97.2kHz with a phase margin of 36.3 degrees. The gain margin of the DiSOM prototype is 4.6dB at 178kHz. The DiSOM prototype outperforms the DPWM prototype by more than a factor of 2 in terms of open loop bandwidth.

The simulation and measurement results for the output impedance are shown in Fig. 13. The peak output impedance for the DPWM prototype is 10Ω and for the DiSOM prototype it is 1.4Ω, which is an improvement by a factor of 7. The output impedance of the DiSOM prototype is approximately 5 times lower at the output filter resonance frequency.

One of the big questions still to be answered regarding digital control of DC/DC converters is whether it can outperform analogue control. Reference [10] presents three different analogue control solutions for an envelope tracking power supply with similar specifications as those used in this paper. The open loop bandwidth and output impedance of the DiSOM prototype is comparable to the poorest of the three analogue control solutions, but there is still some way to go before it can compete with state-of-the-art analogue control solutions.

The simulated step responses of the DPWM and DiSOM solution (see Fig. 14) shows an approximate rise time of 60µs but with the difference that the step response of the DiSOM solution is smooth monotonously rising while the DPWM solution has some ringing. The simulated step response of the DPWM and DiSOM solution corresponds well with the measurements of Fig. 15 and Fig. 16.

The rise time of the step response is limited by the lowpass filter that lowpass filters the reference voltage. The lowpass filter in both designs has a cut off frequency of 10kHz, which limits the rise time to approximately 60µs as both simulations and measurements show. Faster step responses could therefore be achieved by increasing the cut off frequency but at the cost of some overshoot and ringing on the output voltage. Faster step response is not necessarily required [11] depending on the specific application the envelope tracking power supply is designed for, but it will help improve overall system efficiency in some applications.

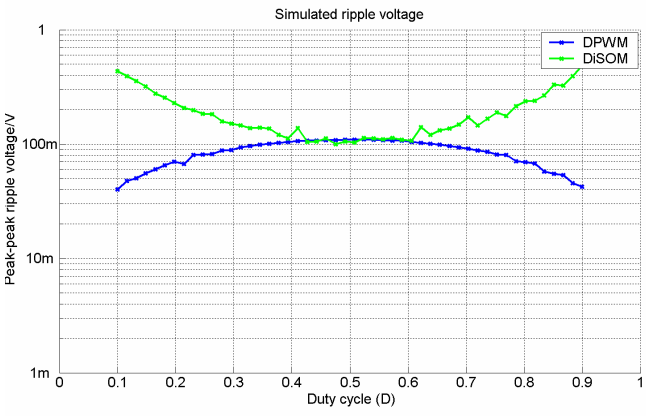

Fig. 8: Simulated ripple voltage versus duty cycle

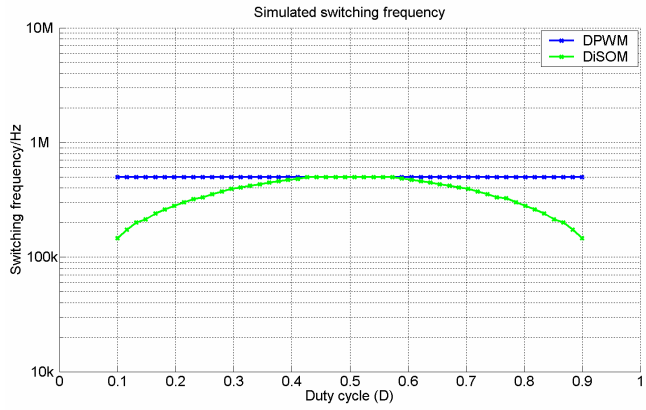

Fig. 9: Simulated switching frequency versus duty cycle

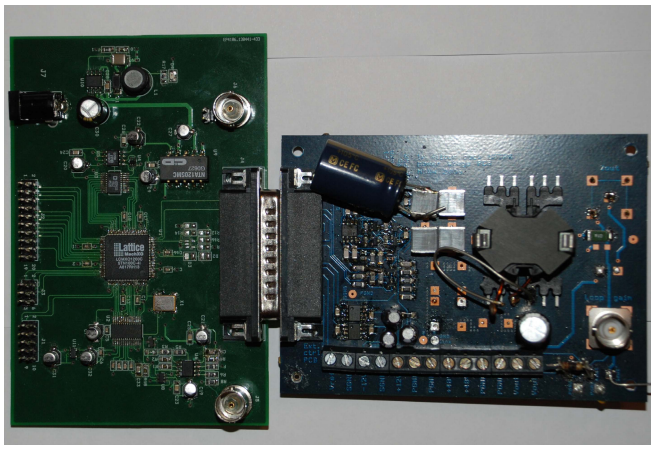

Fig. 10: Prototype PCB for the DiSOM solution. FPGA development board (right) and Buck converter power stage (left)

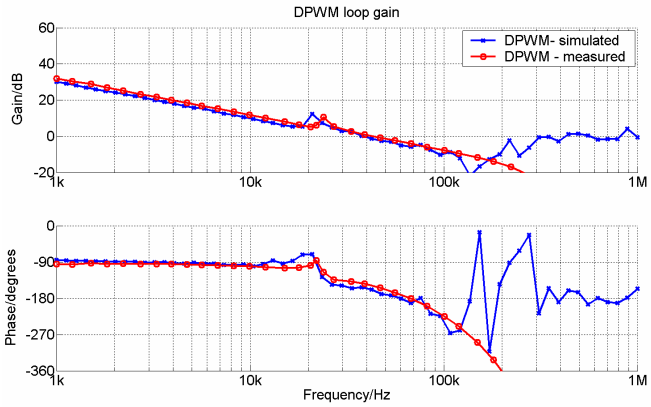

Fig. 11: Simulated and measured loop gain for the DPWM implementation

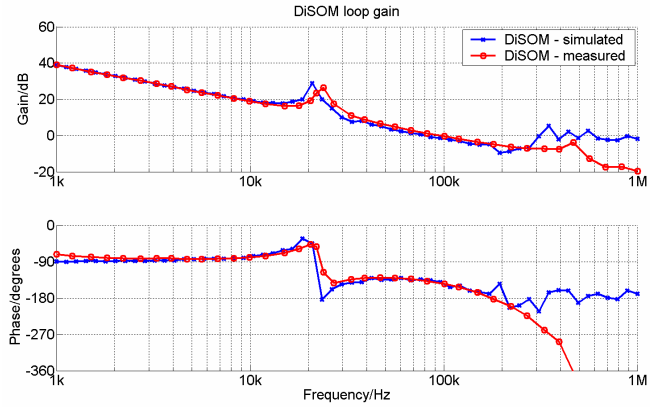

Fig. 12: Simulated and measured loop gain for the DiSOM implementation

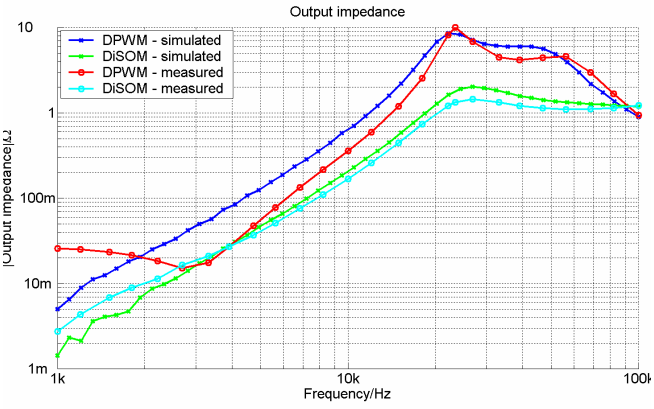

Fig. 13: Simulated and measured output impedance versus frequency

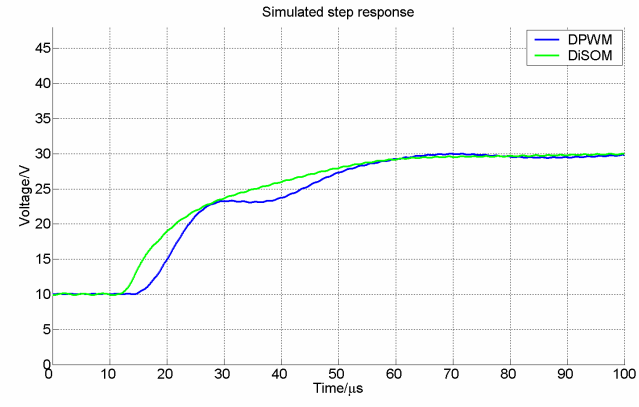

Fig. 14: Simulated step response

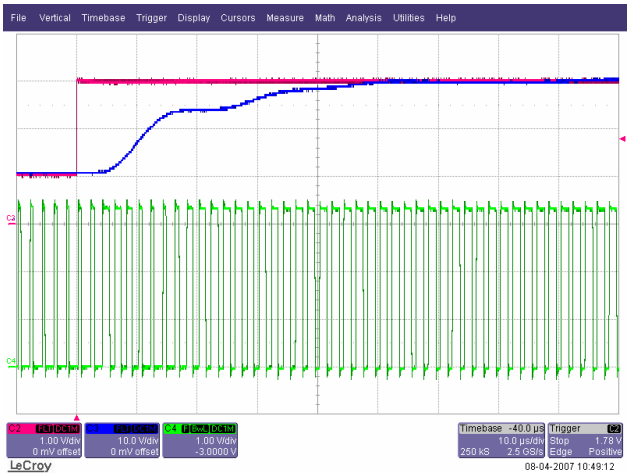

Fig. 15: Positive reference step for the TMS320F2808 DSP based design
C2: Reference voltage (1 V/div)
C3: Output voltage (10 V/div)
C4: High side PWM signal (1 V/div)
Time scale: 10 µs/div

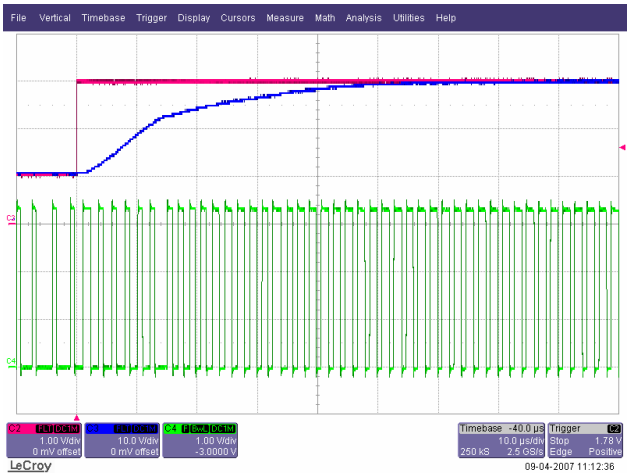

Fig. 16: Positive reference step for the DiSOM based design
C2: Reference voltage (1 V/div)
C3: Output voltage (10 V/div)
C4: High side PWM signal (1 V/div)
Time scale: 10 µs/div

V. CONCLUSION

A new Self-Oscillating modulator (DiSOM) has been presented and it has been shown that the DiSOM modulator allows higher sampling frequencies in a digital control scheme for a DC/DC converter than the traditional counter base Digital PWM (DPWM) modulator.

An envelope tracking power supply for an RF Power Amplifier has been designed and a counter based DPWM control scheme has been compared with the DiSOM based control scheme in simulations and by experimental verification.

The comparison shows that it is possible to more than double the open loop bandwidth with the DiSOM based design. The maximum output impedance of the DiSOM based prototype design is more than 7 times lower than that of the DPWM based prototype.

The step response of the envelope tracking converter has a rise time that is limited because the reference voltage is passed through a lowpass filter with a cut off frequency of 10kHz. The step response of the DiSOM based design is monotonously rising whereas the DPWM based design has some ringing on the step response.

The maximum ripple voltage was twice as high for the DiSOM based design compared to the DPWM based design. The reason being, that the switching frequency is dependent on the duty cycle of the PWM signal and falls towards zero for duty cycles of 0 and 1. It is possible to make the switching frequency of the DiSOM constant by changing the hysteresis window as a function of the duty cycle command or with a phase locked loop.

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20 Appendix F – Publication by L. T. Jakobsen et al.

L. T. Jakobsen and M. A. E. Andersen

"Two-Phase Interleaved Buck Converter with a New Digital Self-Oscillating Modulator"

7'th International Conference on Power Electronics 2007, pp. 760 – 765, 2007

Two-Phase Interleaved Buck Converter with a new Digital Self-Oscillating Modulator

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Abstract— This paper presents a new Digital Self-Oscillating Modulator (DiSOM) for DC/DC converters. The DiSOM modulator alllows the digital control algorithm to sample the output voltage at a sampling frequency higher than the converter switching frequency. This enables higher control loop bandwidth than for traditional digital PWM modulators given a certain switching frequency. A synchronised version of the DiSOM modulator is derived for interleaved converters. A prototype interleaved Buck converter for Point of Load applications has been designed and built to test the performance of DiSOM modulator. The DiSOM modulator and a digital control algorithm have been implemented in an FPGA. Experimental results show that the converter has a very fast transient response when a loadstep is applied to the output. For a loadstep of 50% of nominal output current the output voltage overshoot is less than 2.5% of the nominal output voltage and the settling time is just 8 switching periods.

I. INTRODUCTION

To design a digitally controlled DC-DC converter with fast transient response is a big challenge even though great advances have been made in the last decade. One of the main limitations in a digital controller for a DC/DC converter is the PWM modulator. Many papers have been published about digital modulators that solve either the limit cycling problems due to clock frequency quantization or the problem of how to obtain high control loop bandwidth in a digitally controlled DC/DC converter [1-3]. It can generally be said for the previously published work that the switching frequency is increased in order to increase the control loop bandwidth. This is due to the fact that the digital PWM modulators only allow the sampling frequency of the digital controller to be equal to but not higher than the switching frequency. This limitation has come into play as advanced implementations of the control law, e.g. a digital PID compensator, has reduced the computation time. Previously the main limitation was due to computational delays because microcontrollers or slow DSPs were used [4]. This paper introduces a new Digital Self-Oscillating Modulator (DiSOM) [5] that has the advantage that the digital controller can sample the output voltage at a higher sampling rate than the converter switching frequency thereby allowing the control loop bandwidth to be increased without increasing the switching frequency. A synchronised DiSOM modulator is introduced allowing the DiSOM to be used in interleaved DC/DC converters. A prototype two-phase interleaved Buck converter has been built and tested with the synchronised DiSOM modulator.

II. DISOM -DIGITAL SELF-OSCILATTING MODULATOR

The Digital Self-Oscillating Modulator is a new invention that covers a whole family of digital modulators, which are all self-oscillating by nature. The simplest form of the DiSOM modulator is shown in Fig. 1. It consists of a comparator with hysteresis (the red box in Fig. 1), a main forward block (MFW, the blue box in Fig. 1) configured as an integrator and a main feedback block (MFB, the green box in Fig. 1) that performs a simple multiplication. The reference signal Ref sets the duty cycle and is subtracted from the output signal of the MFB. According to the invention the MFB and MFW can both be frequency dependent and can be implemented as any kind of digital filter. By choosing other characteristics for the MFB and MFW the characteristics and performance of the DiSOM modulator can be changed. The modulator could for instance be designed to suppress quantization errors in the low-frequency band, as known from noise-shapers in class-D audio amplifiers and D/A converters. The comparator with hysteresis generates the switching output by comparing the output of the integrator to either of the hysteresis limits depending on the state of the switching output.

The output of the integrator will be a triangular waveform under steady state conditions. It can be shown that the switching frequency of the DiSOM modulator shown in Fig. 1 is given by equation (1), where n is the number of bits that is used to represent the reference input, *Window* is the hysteresis window and T_{clock} is the period time of the clock that runs the DiSOM modulator.

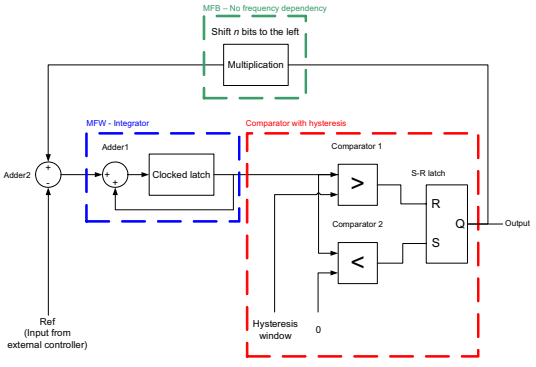

Fig. 1: A block diagram of the DiSOM modulator

$$f_{sw}(D) = \frac{2^n}{Window \cdot T_{clock}} \cdot \left(D - D^2\right) \qquad (1)$$

Fig. 2 shows a typical plot of the switching frequency versus duty cycle, where the duty cycle (D) is normalised from 0 to 1. The big advantage of the DiSOM modulator over traditional PWM modulators is that the duty cycle command, i.e. the Ref input set by the digital compensator, doesn't directly affect the PWM output as it would in traditional digital PWM modulators based on a counter and comparator. Thereby unwanted transitions on the PWM output can be avoided when the duty cycle command is updated. If the duty cycle command for the DiSOM modulator, i.e. the Ref input, is changed during a switching cycle it will change the slope of the triangular waveform on the output of the integrator, but it will not instantaneously affect the PWM output. It is therefore possible for the digital compensator, which controls the output voltage, to sample the output voltage at a higher frequency than the switching frequency and update the duty cycle command at the same rate as the sampling frequency. By increasing the sampling frequency it will be possible to obtain a higher control loop bandwidth for the digitally controlled DC/DC converter, without increasing the switching frequency of the system.

III. SYNCHRONISATION OF THE DISOM

The DiSOM modulator described in the previous section is very well suited for a typical DC/DC converter such as a Buck converter, but it isn't directly applicable to interleaved converters. The problem is that the switching frequency changes with the duty cycle, which means that the period time of the PWM signal isn't constant. The challenge then is how to ensure that the phases in an interleaved converter have the correct phase shift relative to each other, e.g. 180 degrees phase shift in a two-phase interleaved Buck converter. The solution used in the prototype converter presented in this paper is to replace the comparator with hysteresis with a clocked comparator as shown in Fig. 3. The comparator has a synchronising input, and the PWM output will transition from low to high on the positive edge of the synchronising signal. When the integrator output is equal to the hysteresis window the PWM input will transition from high to low. The principle of operation is illustrated in Fig. 4 for duty cycle values of 0.125, 0.25 and 0.375, where the "carrier" is the output of the integrator.

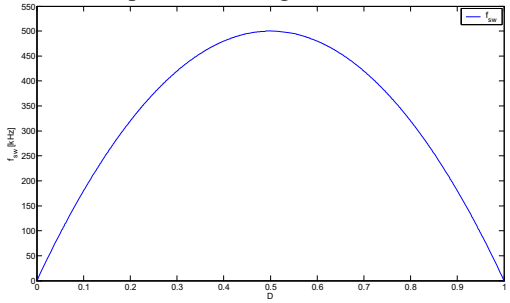

Fig. 2: Switching frequency v.duty cycle for the DiSOM

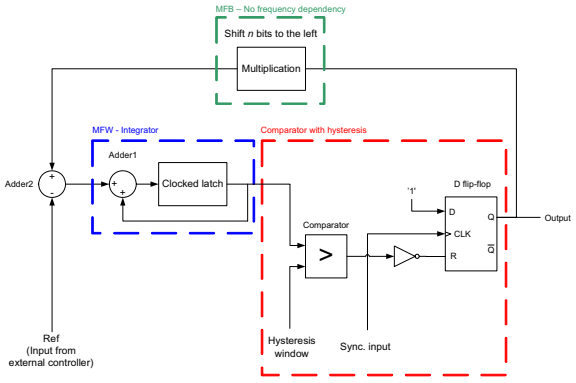

Fig. 3: DiSOM modulator with synchronisation input

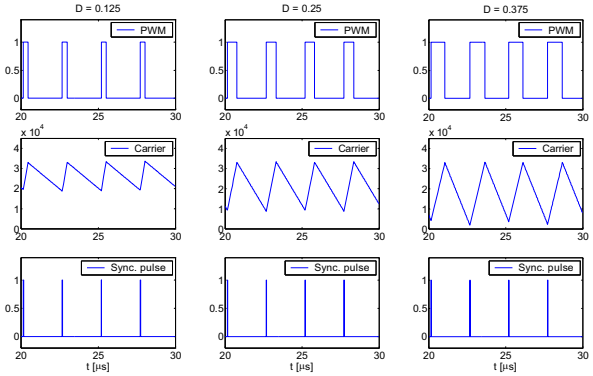

Fig. 4: Carrier and PWM signals for the synchronised DiSOM modulator

It should be noted that by adding synchronistaion to the DiSOM modulator we introduce a limitation to the PWM output. The duty cycle is now limited to the range from 0 to 0.5, which is similar to the duty cycle limitation known from analogue peak current mode control. The problem can be solved by digitally adding a negative slope to the integrator output if the converter design requires duty cycles larger than 0.5. With the new synchronised DiSOM modulator it is possible to generate phase shifted PWM signals by phase shifting the synchronisation signal for each modulator. A block diagram showing how two synchronised DiSOM modulator can be used to create interleaved control signals for two Buck stages is shown in Fig. 5. The timing is controlled by a counter and the synchronisation pulses are generated by comparing the counter value to preset phase delays. The digital PID compensator sets the same duty cycle for both synchronised DiSOMs. In most digital control schemes for interleaved Buck converters the output voltage is sampled at the same rate as the per phase switching frequency effectively limiting the control loop bandwidth to the same bandwidth as would be achievable in a single phase Buck converter switching at the same frequency. Ref [1] proposes a digital control scheme where the sampling frequency is equal to N times the per phase switching frequency, where N is the number of phases of the interleaved converter. The control loop bandwidth can in that case be significantly increased, but the simulations and measurements shown in [1] shows a lot of noise on the output voltage during transient conditions. The noise is to a large extent attributable to the very high

sampling frequency of the output voltage control loop and the fact that the duty cycle of the separate phases in the interleaved converter differs during the transient condition.

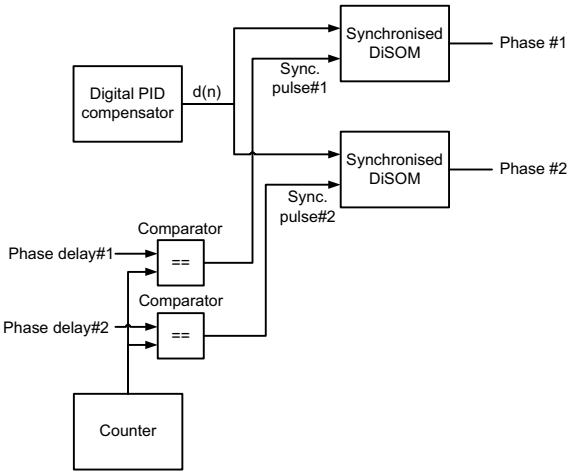

Fig. 5 Interleaving of multiple synchronised DiSOM modulators

IV. IMPLEMENTATION OF DIGITAL PID COMPENSATOR WITH SHORT COMPUTATION TIME

When designing a digital controller for a high bandwidth DC/DC converter it is important to keep the time delays to a minimum, since any delay causes negative phase shift in the control loop. The negative phase shift will have to be compensated for in the control loop design and will very often limit the performance. There are three main contributors to the delay in the digital controller. The first contributor is the PWM modulator, which for a typical uniformly sampled digital PWM modulator has the transfer function

$$G_{PWM}(s) = \frac{e^{-sDT_s}}{c_{PK}} \qquad (2)$$

where D is the duty cycle of the PWM signal, T_s is the period time of the PWM signal and c_{PK} is the amplitude of the digital carrier generated by a counter [6].

The other two contributors to the time delay in the digital controller is the ADC sampling time and the time it takes to compute the digital control law, e.g a digital PID compensator. The design of a digital PID compensator in VHDL for implementation in an FPGA can help reduce the delay time compared to implementations in a Digital Signal Processor/Controller (DSP/DSC) such as the TMS320F2801 [7].

Fig. 6 and 7 shows a block diagram and a timing diagram respectively for the digital PID compensator used in the prototype presented in this paper. The PID compensator of Fig. 6 implements the transfer function $G_c(z)$ (see equation (3)), which has to zeros and an integrator in the frequency domain.

$$G_c(z) = \frac{d(z)}{e(z)} = \frac{b_0 + b_1 \cdot z^{-1} + b_2 \cdot z^{-2}}{1 - z^{-1}} \qquad (3)$$

The digital implementation of the PID compensator calculates the difference equation (4).

$$d(n) = d(n-1) + b_0 \cdot e(n) + b_1 \cdot e(n-1) + b_2 \cdot e(n-2) \qquad (4)$$

where *d(n)* is the duty cycle command for the two synchronised DiSOM modulators, *d(n-1)* is the duty cycle command of the previous sample and *e(n), e(n-1)*and *e(n-2)* is the present and two past samples of the error signal, i.e. the difference between the digital reference and the sampled output voltage.

To explain the operation of the digital PID compensator each block in the block diagram will be explained in the following description.

- Decoder – The decoder takes the input from a 10 bit ADC and reduces the resolution to 6 bits centered around the digital reference, which defines the output voltage. The ADC input is 10 bits because the FPGA development board used in the experimental work had a 10 bit pipelined ADC installed. The decoder updates the error signal *e(n)* when the Read_ADC signal transitions from low to high.
- The sequencer is a simple state machines that generates the control signals for the remaining blocks of the PID compensator. The sequencer has a state variable that is generated by a counter, which counts from 0 to 62 and then resets to 0. The counter is clocked by a 50MHz clock and the operation of the PID compensator is synchronised to the counter. The resulting sampling frequency is equal to 794 kHz.
- The 20-bit adder and the 20-bit register works as an accumulator. The accumulator can take the previous result on the output of the accumulator and add it to the result on the output of the 6×14 bit multiplier or the sequencer can preload the duty cycle d(n-1) that is read from the limiter.
- The 6×14 bit multiplier is used to multiply an error signal with its corresponding coeffecient, e.g. e(n) and b_0. The coefficients b_0, b_1 and b_2 are represented as 14 bit numbers. The 5 least significant bits represents fractions of 1 and the most significant bit is a sign bit. All calculations are performed using 2's complement binary numbers. The remaining 8 bits allows the coefficients to take on values in the range from – 256 to +256. In a typical DSP both inputs on the multiplier would have the same word length but that increases the complexity of the multiplier. The idea of limiting the word length of one input to match the error signal is presented in [8] with the purpose of reducing the

complexity and cost of the digital compensator logic.

- The two multiplexers (labelled 3-1 MUX) are used to select, which error signal and coefficient is fed to the inputs of the multiplier. Both multiplexers are controlled by the 2-bit Mux_sel signal.
- The two 6-bit registers stores the error signals *e(n-1)* and *e(n-2)*. The registers reads and stores the input signal on the rising edge of the control signal, i.e. Update_e1 and Update_e2.
- The limiter reads the output of the accumulator and limits it to duty cycle values between 0 and 0.5 on the rising edge of Update_D.

The digital PID compensator has a delay of two clock cycles from the ADC input is read by the decoder until the duty cycle command is updated by the limiter. The ADC is a 10-bit pipelined ADC with a sampling delay of 6 clock cycles. Both the ADC and the digital PID compensator is clocked by a 50 MHz clock and the total delay is 8 clock cycles, which makes the delay 160 ns.

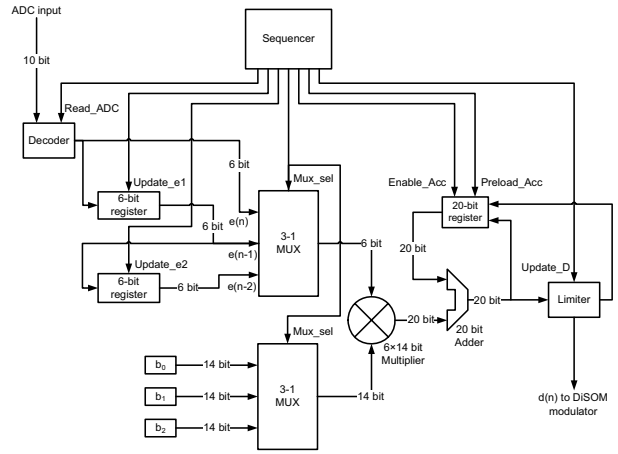

Fig. 6 Block diagram of the digital PID compensator implemented in an FPGA

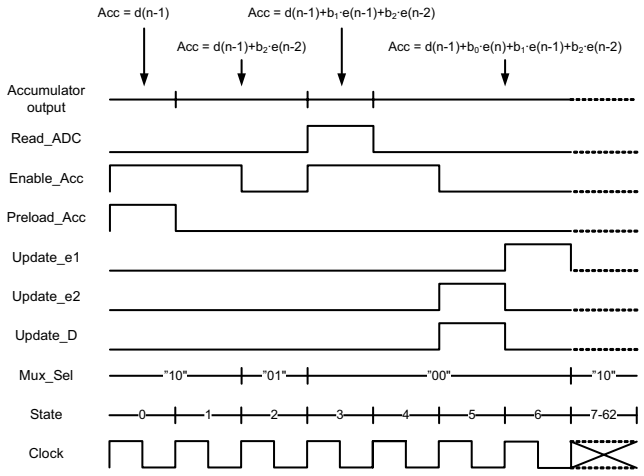

Fig. 7 Timing diagram for the digital PID compensator

The disadvantage of the digital PID compensator described above is that it can not be changed easily. If for example the designer wants to add an extra zero or a pole to the transfer function the VHDL code will have to be modified and the design has to be simulated and tested once again. Compared to a more traditional DSP design [9], where it is a matter of rewriting a piece of assembly or C code, it is a much more challenging task to change the VHDL design.

V. EXPERIMENTAL RESULTS

A two-phase interleaved buck converter has been designed and built to verify verify the performance of the synchronised DiSOM modulator. The specifications of the hardware prototype are given in Table 1. The output capacitor is in fact eight 100µF ceramic capacitors (X5R) for low ESR. A picture of the prototype is shown in Fig. 8.

The DiSOM modulators and the digital compensator are implemented in an LCXMO1200 FPGA from Lattice Semiconductor. The ADC used in the design is the ADC10065 from National Semiconductors.

TABLE 1
PROTOTYPE SPECIFICATIONS

Parameter	Value
Input voltage	9 – 15V
Output voltage	2.0V
Output current	0 – 20A
Inductor size	1.5 µH
Output capacitance	800 µF
Switching frequency per phase	400 kHz
Sampling frequency	800 kHz

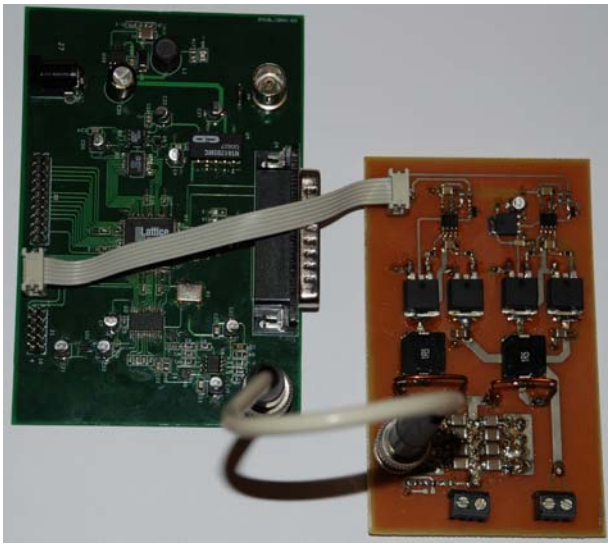

Fig. 8: Prototype POL converter board (Right) and FPGA development board (left)

A MATLAB/SIMULINK model of two-phase interleaved Buck converter and the digital controller was used to simulate the design. The Buck converter model takes into account parameters such as capacitor ESR, inductor series resistance and the MOSFET driver propagation delay.

Fig. 9 shows a comparison of the simulated and measured open loop gain of the interleaved Buck converter. The

simulated loop gain is found by injecting a sinewave into the control loop at the converter output in the same way as the loop gain is measured by a Gain/Phase analyser. The loop gain measurement shows that the open loop bandwidth of the interleaved Buck converter is 41 kHz and the phase margin is 56 degrees.

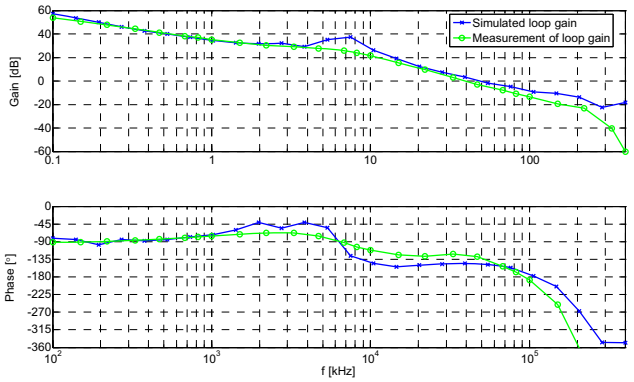

Fig. 9 Open loop gain simulation and measurement

Simulations of the output voltage response to a load step from 10 to 20A for two different current slew rates (see Fig. 10) shows that the output voltage deviation from the steady state voltage of 2.0V is 50mV for a current slew rate of 1000A/µs. If the load step has a first order lowpass response with an average slew rate of 1A/µs the output voltage deviation is approximately 40mV. The settling time is approximately 15µs for the slow load step and 20µs for the fast load step.

Fig. 11 shows the measured output voltage response to a loadstep from 10 to 20A. The output voltage deviation is less than 50mV and the settling time is less than 20µs. The electronic load used in the measurement limits the current slew to approximately 1A/µs and the measurement is comparable to the blue trace in Fig. 10. The measured output voltage deviation is slightly larger than the simulation result and the settling time is also slightly longer. The difference between simulation and measurement can be due to component tolerances and poor PCB design.

Fig. 12 shows a steady state measurement of the output voltage at nominal output current. The output voltage has some fluctuations, which isn't the ripple voltage generated by the ripple current in the inductor. Part of the explanation is the relatively low ratio between the per phase switching frequency and the clock frequency of the synchronised DiSOMs. The ratio between switching and clock frequency is 1/126, which correpsonds to a PWM duty cycle resolution of 7 bits. The resolution of the duty cycle command of the digital PID compensator is 10 bits. The reason that the fluctuations on the output voltage have an amplitude of less than 10 mV peak to peak is the nature of the synchronised DiSOM modulator. The DiSOM is a closed loop system that feeds back the PWM signal and compares it with the duty cycle command and the integrator will suppress the low frequency errors. The DiSOM is in that sense similar to sigma-delta modulators that shapes the quantisation noise in such a way that noise power is low at low frequencies and increases at high frequencies.

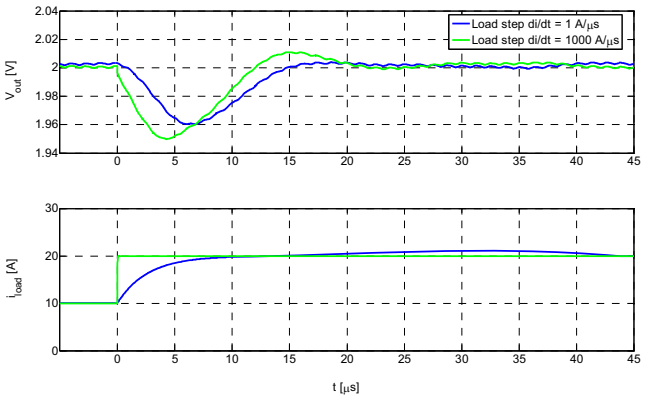

Fig. 10 Simulated load step response for V_{in} = 12V

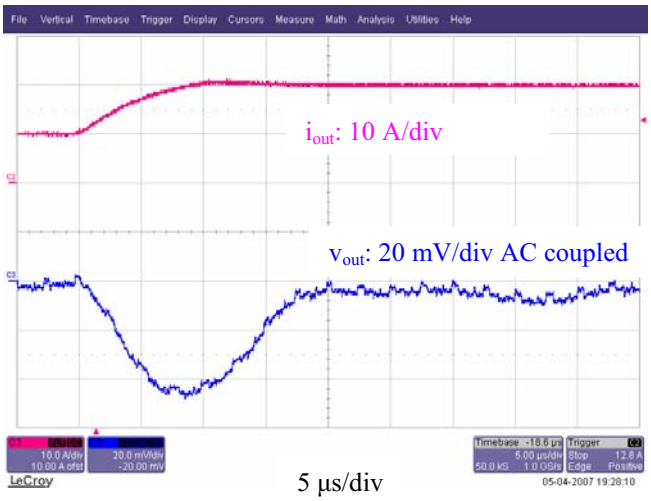

Fig. 11: Positive loadstep 10A to 20A V_{in} = 12V

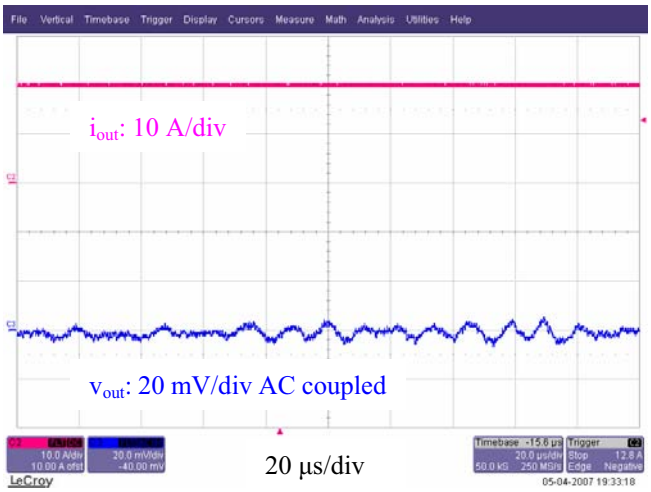

Fig. 12 Steady state measurement of the output voltage for I_{out} = 20 A

VI. CONCLUSION

This paper describes a two-phase interleaved buck converter with very fast transient response. A new digital modulator, called the DiSOM modulator is described and a synchronised DiSOM modulator is derived. A prototype

2.0V 20A two-phase interleaved Buck converter has been built to test the proposed modulator. The output voltage response, to a loadstep of 50% of the nominal output current, is less than 2.5% of the nominal output voltage. The settling time after a loadstep is less than 20μs, which corresponds to just 8 switching cycles.

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21 Appendix G – Publication by L. T. Jakobsen et al.

L. T. Jakobsen and M. A. E. Andersen

"Digitally Controlled Offline Converter with Galvanic Isolation Based on an 8-bit Microcontroller"

IEEE Industrial Electronics Conference 2007, pp. 1943 – 1949, 2007

The 33rd Annual Conference of the IEEE Industrial Electronics Society (IECON)
Nov. 5-8, 2007, Taipei, Taiwan

Digitally Controlled Offline Converter with Galvanic Isolation Based on an 8-bit Microcontroller

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Abstract – **This paper presents an offline AC/DC converter with digital control and galvanic isolation that can be implemented using cheap commercially available components. An ATMEL ATTiny26 8-bit microcontroller is used to control the converter. The microcontroller is placed on the secondary side of the converter and an analogue primary side startup controller is used on the primary side. A prototype two-switch forward converter has been designed and experimental results are included to show the feasibility and performance of the proposed design.**

I. INTRODUCTION

Digital control of switch mode converters, especially non-isolated DC/DC converters and converters with Power Factor Correction, have been the subject of extensive research over the last ten years. The aspect of designing a switch mode converter with galvanic isolation has only been treated in a few publications [1, 2].

In reference [1] a digital control IC specifically designed for low power flyback converters with PFC capabilities is described. The control IC is placed on the primary side of the flyback converter and the output voltage is measured on an auxiliary winding on the flyback transformer during the MOSFET Off period, at which time the output voltage is reflected on the auxiliary winding. Reference [1] does not deal with the supply current drawn by the control IC.

Reference [2] describes a two chip solution where the digital control IC is placed on the primary side of an isolated switch mode converter and an Analogue to Digital Converter (ADC) is placed on the secondary side, so that it can measure the output voltage directly. The ADC data is transferred over the isolation barrier through a high speed optocoupler. The control IC on the primary side has a supply current of 2mA. The two chip solution is designed for low voltage isolated DC/DC converters.

The design presented in this paper is a digitally controlled offline converter with galvanic isolation running of the AC mains with a nominal voltage of $230V_{RMS}$. The control scheme is based on a primary side startup controller, which can generate a PWM during startup. Once the converter has started switching and the output voltage is close to the nominal voltage the primary side startup controller synchronizes to the PWM signal generated by the main controller placed on the secondary side of the converter. The secondary side controller is digital and implemented in a low cost 8-bit microcontroller. The primary side startup controller has a very low startup current, which makes it possible to deliver the startup current through a resistor directly from the rectified AC mains without negatively affecting the overall converter efficiency. The prototype design is built using commercially available components.

II. CHOICE OF ISOLATION BARRIER

Galvanic Isolation in traditional analogue controlled switch mode power supplies is achieved with an optocoupler that is integrated in the compensator circuit [3,4]. This approach is most commonly realised by combining a shunt regulator, e.g. the TL431, and the optocoupler in such a way that the shunt regulator works as an error amplifier and reference at the same time. Fig. 1 shows an example of how the circuit could be implemented, but other implementations are possible. The big advantage of this approach is that the integrator of the compensator is placed on the secondary side by placing capacitor C1 across the shunt regulator. In this way the non-linear behaviour of the Current Transfer Ratio of the optocoupler is eliminated and the output voltage compensation is linear. Further poles and zeroes in the compensation can be added in the feedback loop of the error amplifier on the primary side, typically included in the primary side PWM controller, e.g. the UC3844 from Texas Instruments [5].

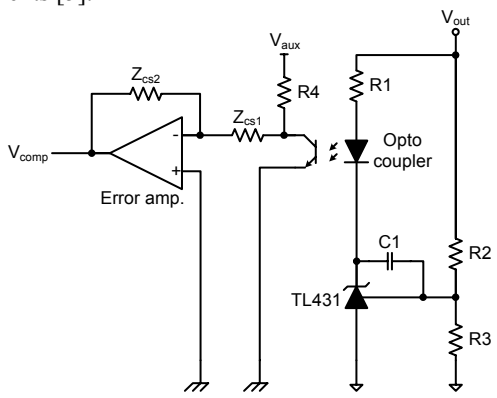

Fig. 1: Typical analogue implementation of galvanic isolation

In a digitally controlled switch-mode power supply it is customary to do the compensation in the digital controller as well as generate the PWM signal digitally. The digital controller can be placed on either the primary or the secondary side of the isolation barrier.

Two solutions are considered for the galvanic isolation of a digitally controlled offline converter. The first solution uses

an isolation amplifier to obtain isolation in the feedback loop (see Fig. 2). The block diagram of Fig. 2 shows a two-switch forward converter, but any converter topology with transformer isolation could be used. The digital controller, which can be a microcontroller, DSP or an ASIC, is placed on the primary side and generates a PWM output that drives the gatedrive IC. Because the digital controller is placed on the primary side and is directly driving the gatedrive IC, it has to be powered up and start generating a PWM signal in order for the converter to start. Unlike an analogue control IC such as the UC3844, a digital controller needs a relatively large supply current to initialise and begin generating PWM pulses. This means that if the supply current for the digital controller has to be supplied through a resistor from the rectified mains voltage during startup, the resistor would dissipate quite a lot of power. The microcontroller used in the prototype described in section V draws a supply current of 15mA and if this current was to be supplied through a resistor from a $325V_{DC}$ voltage on rectifier the power dissipation would be almost 5W. In comparison a typical analogue control IC only needs a startup current of 0.5 to 1mA resulting in a power loss of less than 0.5W. In a converter with 100 Watts of output power the difference in efficiency would be in the neighbourhood of 5% which is a considerable difference.

The resistor can be disconnected once the converter has begun switching and the digital controller can be supplied by an auxiliary winding on the transformer, thereby removing the power loss, but that would entail using a high voltage enhancement FET that can be turned off once the converter is running.

Another issue in the isolation scheme shown in Fig. 2 is the use of an isolation amplifier in the feedback loop. Commercially available isolation amplifiers have sufficient bandwidth for most offline converter applications and have excellent linearity. The price of isolation amplifiers does however inhibit their use in low cost power supplies in most industrial applications.

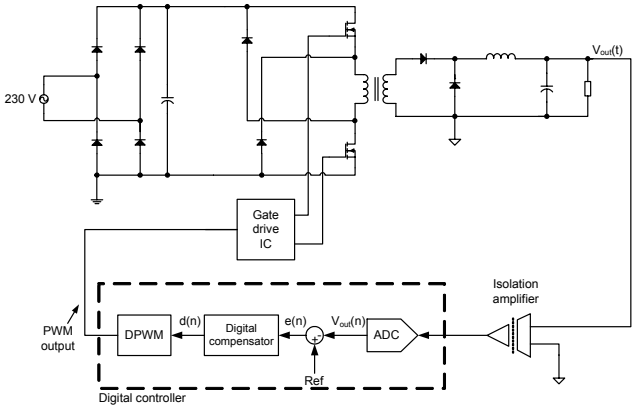

Fig. 2: Galvanic isolation scheme #1

The second and preferred isolation scheme is shown in Fig. 3. The digital controller is placed on the secondary side of the converter and the PWM signal from the controller is transferred across the isolation barrier. The isolation is based on the use of the primary side startup controller, e.g. the UCC3960 from Texas Instruments [6]. The idea of the primary side startup controller is that it can generate a PWM signal during startup independently of the digital controller. Once the digital controller on the secondary side starts generating a PWM signal the primary side startup controller synchronizes the PWM signal driving the gate drive IC to the signal generated by the digital controller. The PWM signal is highpass filtered before it is applied to the signal transformer transferring the signal across the isolation barrier. This means that the signal transformer transfers short pulses instead of transferring the original PWM signal. Because of that the signal transformer can be wound on a smaller ferrite core than if the PWM square wave was transferred. The disadvantage of transferring pulses rather than the original PWM signal is that the pulse needs to be of a certain width for the primary side startup controller to detect the pulse, thus limiting the minimum pulse width of the PWM signal. This is only of concern if the load current is very small in which case the converter works in discontinuous conduction mode and the output voltage will increase because the duty cycle becomes higher than dictated by the PWM signal generated by the digital controller.

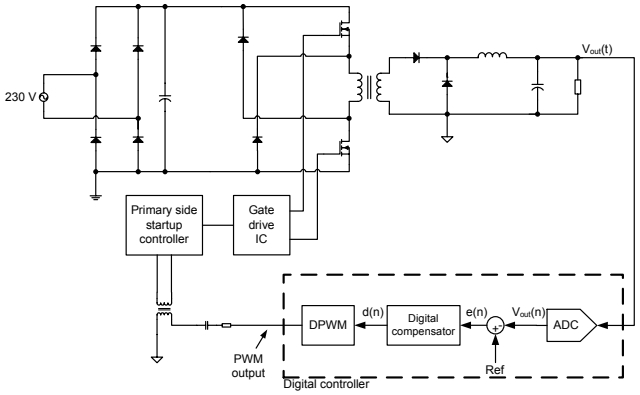

Fig. 3: Galvanic isolation scheme #2

III. DIGITAL CONTROLLER AND COMPENSATOR DESIGN

The digital controller can, as already mentioned, be a microcontroller, a DSP or an ASIC. The choice of digital controller does to some extent determine the performance of the overall converter. Most importantly the duty cycle resolution of the digitally generated PWM signal and the ADC resolution determine the accuracy with which the output voltage can be regulated, but also if the output voltage will limit cycle. Limit cycling occurs if the ADC resolution is greater than the resultant change in output voltage if the least significant bit (LSB) of the PWM duty cycle register is changed [7,8]. This can be expressed mathematically for the forward converter as shown in equation (1). The general way to avoid limit cycling is by reducing the ADC resolution until

the effective ADC resolution is smaller than the effective DPWM resolution.

$$n_{A/D} \le \log_2\left[\Delta V_{A/D} \cdot \frac{2^{n_{PWM}}}{N \cdot V_g \cdot H}\right] \quad (1)$$

where:

$n_{A/D}$ is the ADC converter resolution in bit
$\Delta V_{A/D}$ is the ADC measuring range in volts
n_{PWM} is the DPWM resolution in bit
N is the transformer winding ratio
V_g is the DC input voltage of the converter
H is the output voltage feedback divider ratio

The control loop bandwidth may be limited by the computational delay of the digital controller, i.e. the time it takes from the output voltage is sampled to the time the duty cycle register of the DPWM block is updated by the digital compensator. The delay adds negative phase shift to the compensator frequency response, which the compensator design must take into account. If the computational delay is long compared to the PWM period time it will often be necessary to reduce the gain of the controller to get a stable control loop, thereby reducing to open loop bandwidth of the converter. Low control loop bandwidth results in poor transient response in the event of fast changes in load current or input voltage. The computational delay is determined by which features the chosen digital controller has, such as hardware multipliers and internal word-length, as well as the clock frequency it runs at.

For the prototype design presented in this paper an ATMEL ATTiny26 microcontroller of the 8-bit AVR family was chosen. The ATTiny 26 has several features, which makes it suitable to use as a low cost digital controller for a switch mode converter [9]. It has a clock frequency of 16 MHz and single cycle command execution, meaning that it can perform most assembly commands in a single clock cycle. It has a built in 10-bit 75 kilo-samples per second (ksps) ADC with 8 multiplexed inputs. The ADC can sample at faster sample rates than 75 ksps, but the resolution will be decreased proportionately with the increase in sampling rate. Finally the ATTiny26 has an internal 64 MHz PLL that drives the DPWM module. The DPWM module is capable of generating a 250 kHz PWM signal with 8 bit resolution running on the 64 MHz clock generated by the PLL (see equation (2)). The DPWM module is implemented as a counter clocked by the PLL and a comparator, which compares the counter value with the value written by the digital compensator to the duty cycle register. The counter is an 8 bit counter, which limits the maximum resolution to 8 bit even if the PWM frequency is selected lower than 250kHz. The DPWM clock can be divided by 2, 4, 8 etc. in a prescaler, in order to achieve switching frequencies lower than 250 kHz without losing resolution.

$$\text{DPWM resolution} = \log_2\left(\frac{f_{PLL}}{f_{PWM}}\right) = \log_2\left(\frac{64M}{250k}\right) = 8 \quad (2)$$

The electrical specifications of the prototype converter for which the compensator is designed are given in TABLE I and the basic control loop parameters assumed in the design of the compensator are listed in TABLE II. The computational delay is based on the assumption that the digital controller samples the output voltage at the beginning of a PWM period, i.e. at the instant in time at which the PWM signal transitions from low to high, and calculates the new duty cycle in a period of time shorter than the PWM period. The duty cycle is set by writing the duty cycle value calculated by the compensator to the duty cycle register. The software will be further described in section IV.

TABLE I
PROTOTYPE CONVERTER ELECTRICAL SPECIFICATIONS

Parameter	Value
Input voltage range	210 – 265 V_{RMS}
Output voltage	12.0V
Nominal output current	10A
Input capacitance	150 µF
Transformer winding ratio, N	0.1
Output filter inductance	32 µH
Output capacitance	2 × 330 µF

TABLE II
CONTROL LOOP PARAMETERS

Parameter	Value
Switching frequency	125 kHz
Sampling frequency	125 kHz
Computational delay	8 µs
DPWM resolution, n_{PWM}	8 bit
ADC resolution, $n_{A/D}$	7 bit
ADC range, $\Delta V_{A/D}$	2.5 V
Feedback divider ratio, H	6.1

The switching frequency is 125kHz and it is generated in the ATTiny26 by dividing the 64MHz PLL clock by 2, thereby achieving a resolution of 8 bit for the DPWM. Inserting the DPWM resolution and the feedback divider ratio given in TABLE II together with the relevant numbers from TABLE I into equation (1) it is found that the ADC resolution, $n_{A/D}$, must be less than 6.7 bit at the highest input voltage of 265V_{RMS}. The ADC resolution is selected at 7 bit even though this theoretically should lead to limit cycling. This turns out to work because the effective ADC resolution is lower than 7 bit.

The digital compensation scheme can either be voltage mode control (VMC) or current mode control (CMC). In VMC the digital controller samples the output voltage and calculates the duty cycle of the PWM signal based on that. As in analogue control the converter transfer function, i.e. the small signal model for the converter output voltage as a function of the duty cycle, is a second order function with a complex pole pair. This means that the compensator will

typically have two zeroes and an integrator, often known as a PID-compensator, to get a stable control system. In CMC on the other hand the inductor current is directly controlled and the converter transfer function is reduced to a first order function with one pole. The compensator can thus be simplified to a PI-compensator, with one zero and an integrator. CMC is easy to realize in an analogue control circuit, e.g. peak current mode or average current mode control, but it poses certain problems when implemented as a digital control scheme as will be described in section IV.B.

The digitally controlled offline converter is therefore controlled using VMC because of the practical problems posed by digital CMC. The converter transfer function is given by equation (3) [10].

$$G_{vd}(s) = \frac{\hat{v}_{out}(s)}{\hat{d}(s)} = V_g \cdot N \cdot \frac{1}{s^2 \cdot LC + s \cdot L/R_{load} + 1} \quad (3)$$

The compensator is designed in the discrete time domain, better known as the z-domain. The converter transfer function is defined in the continuous time domain (s-domain) and must be rewritten as a z-domain transfer function. The Tustin-approximation [11] is used to rewrite the transfer function of equation (3) by substituting s with the expression given in equation (4).

$$s \cong \frac{2}{T_s}\frac{1-z^{-1}}{1+z^{-1}} \quad (4)$$

The rest of the control loop can be directly described in the z-domain and it will not be described in detail. The designed compensator has three zeroes and an integrator (see the transfer function in equation (5)). To get a stable control loop with a good phase margin it was necessary to use three zeroes in the transfer function. The three zeroes introduces positive phase to the open loop transfer function, and is used to compensate for the large negative phase caused be the computational delay. The negative phase caused by the computational delay is frequency dependent and goes towards -180 degrees at the Nyquist frequency, which is half the sampling frequency. The phase shift added by the computational delay is plotted as a function of frequency in Fig. 4.

$$G_c(z) = \frac{b_0 + b_1 \cdot z^{-1} + b_2 \cdot z^{-2} + b_3 \cdot z^{-3}}{1 - z^{-1}} \quad (5)$$

Fig. 5 shows the root locus and open loop Bode plot for the offline converter with the compensator coefficients given in TABLE III. The open loop bandwidth is just under 2 kHz and the phase margin is 37.6 degrees.

TABLE III
Compensator coefficients

Compensator coefficient	Value
b_0	24
b_1	-49.6875
b_2	29.125
b_3	-3.375

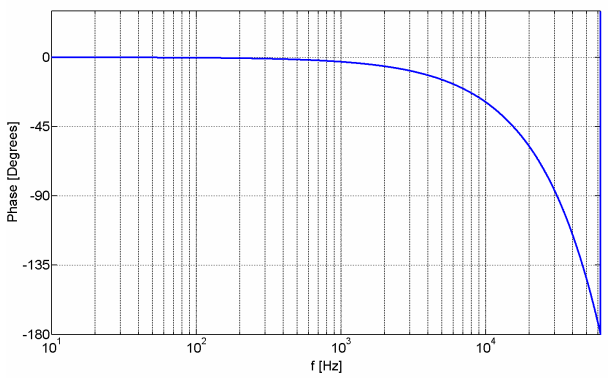

Fig. 4: Phase shift added by the computational delay

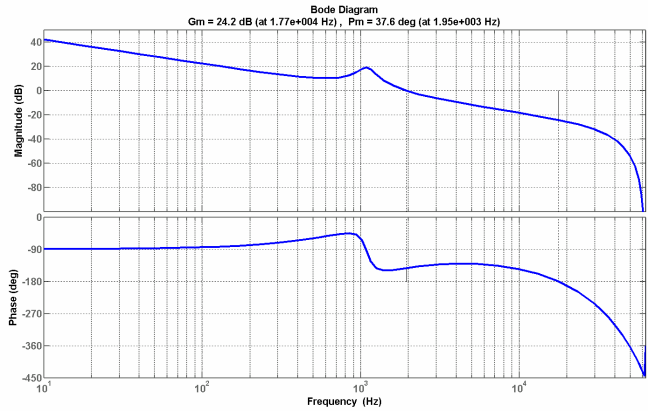

Fig. 5: Root locus and open loop Bode plot for the control system

IV. SOFTWARE IMPLEMENTATION

The control algorithm for the ATTiny26 is written in assembly language because it allows the programmer to optimize the control loop algorithm with regards to the execution time. This is important since the computational delay, which is dictated by the execution time, is one of the limiting factors when the compensator is designed. It is more time consuming to program in assembly language rather than a high level programming language such as C, but the reduction in execution time that can be obtained by writing the software in assembly language will generally justify the longer development time.

Since the ATTiny26 does not have a hardware multiplier to do multiplications the software utilizes lookup tables stored in program memory. The software is basically written following the guidelines of reference [12].

A. Voltage Mode Control

The theoretical compensator design determined that the compensator should have three zeroes and an integrator (see equation (5)). The software interrupt service routine (ISR) must calculate the result of the difference equation (6) derived from the compensator transfer function.

$$d(n) = d(n-1) + b_0 \cdot e(n) + b_1 \cdot e(n-1) + b_2 \cdot e(n-2) + b_3 \cdot e(n-3) \quad (6)$$

Four lookup tables are defined in the software. Each lookup table contains the results of the multiplications of b_0, b_1, b_2 and b_3 with the error signal corresponding to each coefficient. This is much faster than doing the actual multiplication since the ATTiny26 does not include a digital hardware multiplier. The error signal is limited to values between -16 and +15 and the coefficients can be set to values between -64 and +64 adjustable in steps of 1/16th (0.0625). The internal resolution of all calculations is 16 bit.

The total execution time of the ISR is 6.5µs and the execution requires 13 Million Instructions Per Second (MIPS) out of the 16 MIPS available in the ATTiny26. This leaves 3 MIPS that can be utilized by adding a serial interface to the digital controller. The serial interface could be used to provide features such as status information or the possibility to change control parameters such as compensator coefficients and the output voltage.

B. Current mode control

Digital CMC can be implemented in several different ways with the common feature that they include two control loops. The inner loop controls the inductor current and the outer loop controls the output voltage by calculating a reference signal, i.e. the current reference, for the inner loop [13, 14]. It is obvious that digital CMC places higher demands on the digital controller since it has to execute both control loops in software. It is however not just a matter of how many calculations/commands the digital controller has to perform. The ADC needs to sample two signals (voltage and current) for every switching period for the controller to work optimally instead of just the out voltage in VMC. The biggest challenge in the design of digital CMC is when to sample the inductor current relative in time to the PWM signal since this affects the performance of the current control loop. Most digital CMC schemes samples either the average or the peak current which means that the sampling instant is moving in time relative to positive transition of the PWM signal. The digital controller should be able to finish the computations before the beginning of the next PWM period. For this to be possible the digital controller will either have to be very fast or the duty cycle will have to limited to a certain range in order to be sure that the new duty cycle can be written in time.

In reference [14] a digital CMC scheme is proposed, which samples the current at the beginning of the PWM period and implement a digital valley current mode control scheme with what turns out to be a simple proportional (P) compensator. The big advantage is that a proportional compensator is very simple to implement in software since it only requires one subtraction and one multiplication.

The digital current control scheme just mentioned was sought implemented in the ATTiny26, but it turned out that several problems made it impossible to make it work. First it should be mentioned that the compensator in the outer loop (output voltage) can be simplified to removing one zero thus reducing the computational delay of the outer loop.

The main reason why digital CMC could not be implemented was simply that the computational delay of the overall control scheme exceeded the switching period of 8µs. The computational delay could be reduced to 10.5µs by optimizing the sequence in which the computations were performed in the software. Another problem was that the compensator of the inner loop was also implemented using a lookup table, but in this case the error range could not be reduced like it was in the compensator described in section IV.A., because the current should be able to change very rapidly if the load current changes. If a large change in current is necessary the error signal has to be big and if the error is limited it will reduce the bandwidth of the inner current loop. Reduced bandwidth of the current loop will reduce the open loop bandwidth of the voltage loop resulting in a slower dynamic response on the output voltage during load steps.

Based on the abovementioned issues related to implementing digital CMC in the ATTiny26 it was decided to use voltage mode control in the prototype design.

On a practical note it should be mentioned that digital CMC in itself does not guarantee better performance of the overall converter and that it will probably still be necessary to have an analogue over-current protection circuit since digital CMC can not necessarily be relied on to provide adequate short circuit protection for the converter output. Digital CMC can be used if a faster digital controller such as Digital Signal Controller/Processor is used, but that will be a more expensive solution.

V. EXPERIMENTAL RESULTS

The prototype converter has been designed and built on a 2-layer PCB (see Fig. 6). The primary side startup controller used in the design is the UCC3960 from Texas instruments and the pulse transformer is wound on an RM4 core in the N87 ferrite material. The pulse transformer has been designed so that the pulses transmitted to the primary side startup controller meets the requirements specified in the UCC3960 datasheet (shown in Fig. 7). The inductance of the pulse transformer is 6µH and the capacitor and resistor of the highpass filter are 1nF and 330Ω. An oscilloscope measurement of the pulses on the pulse transformer is shown in Fig. 8. The pulse is around 200ns wide and the time it exceeds 1V is approximately 30ns. The pulse measured on the pulse transformer has an amplitude of 1.3V, which shows that it is attenuated by parasitic components. It does however meet the specifications and the converter is working correctly.

In Fig. 9 and Fig. 10 the output voltage response to a positive and negative load step is shown. The measurement is performed with an input voltage of 230VRMS corresponding to a DC input voltage of 325V and the current is alternating between 5A and 10A. The load used in the measurement of the load step response is an electronic load, which is coupled

as a constant current load. The output voltage has a transient overshoot of approximately 600mV for the positive load step and 665mV for the negative load step. The settling time is 800µs for both the positive and the negative load step. This corresponds reasonably well with the theoretical control loop bandwidth, which is just below 2kHz. The small ringing on the output voltage before it settles at the nominal output voltage is due to the fact that the phase margin is only around 38 degrees according to the theoretical compensator design.

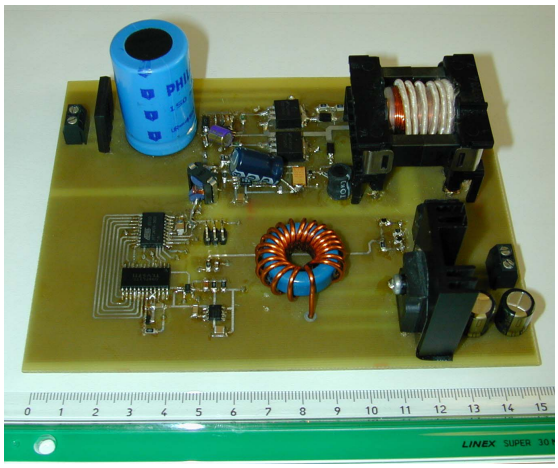

Fig. 6: Prototype PCB

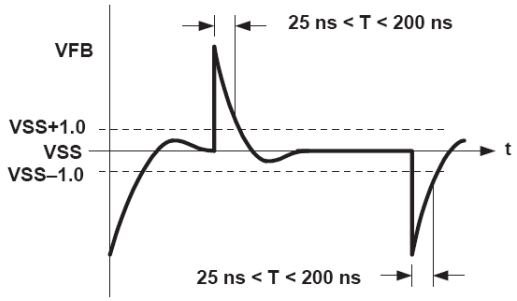

Fig. 7: Specifications for pulse duration and amplitude on the input of the primary side startup controller

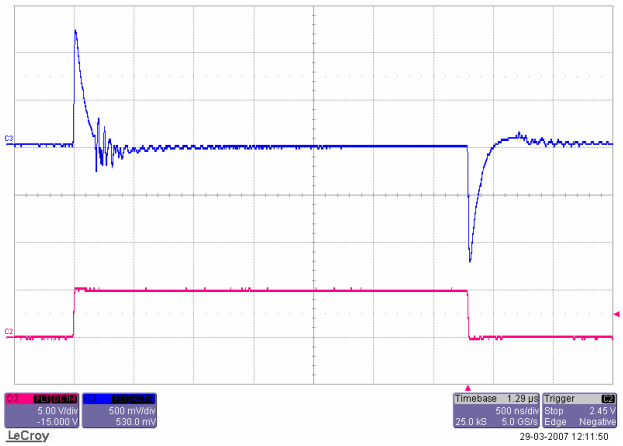

Fig. 8: Pulse transformer signals
Upper trace: Pulse transformer signal 0.5V/div
Lower trace: µController PWM output 5V/div
Time scale: 500 ns/div

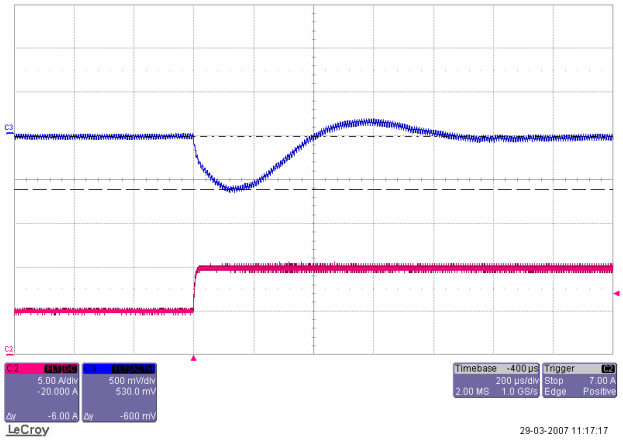

Fig. 9: Positve load step from 50 – 100% of nominal output current.
Upper trace: v_{out} 500mV/div
Lower trace: i_{out} 5A/div
Time scale: 200 µs/div

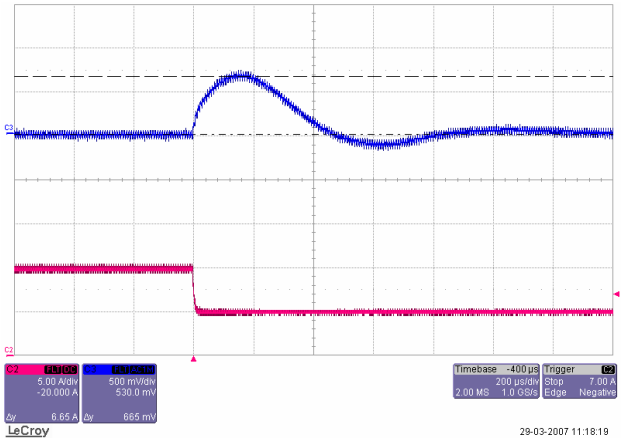

Fig. 10: Negative load step from 100 – 50% of nominal output current.
Upper trace: v_{out} 500mV/div
Lower trace: i_{out} 5A/div
Time scale: 200 µs/div

VI. CONCLUSION

A simple way to build an offline converter with galvanic isolation and digital control has been described theoretically and demonstrated by measurements on a prototype converter. Galvanic isolation is achieved using commercially available components and the digital control algorithm is implemented in a low cost 8-bit microcontroller.

The computational delay in the digital controller gives rise to negative phase, which must be compensated for. This is done by having three zeroes in the digital compensator along with an integrator to ensure a constant DC output voltage.

The experimental results show that the performance of the prototype converter is comparable to the performance of most offline converters with analogue control. By adding digital control extra features such as programmability of the output voltage and compensator coefficients can be added by extending the microcontroller software.

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22 Appendix H – Publication by L. T. Jakobsen et al.

L. T. Jakobsen, H. Schneider and M. A. E. Andersen

"Comparison of State-of-the-Art Digital Control and Analogue Control for High Bandwidth Point of Load Converters"

IEEE Applied Power Electronics Conference 2008, pp. 1440 – 1445, 2008

Comparison of State-of-the-Art Digital Control and Analogue Control for High Bandwidth Point of Load Converters

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***Abstract*- The purpose of this paper is to present a comparison of state-of-the-art digital and analogue control for a Buck converter with synchronous rectification. The digital control scheme is based on a digital self-oscillating modulator that allows the sampling frequency to be higher than the switching frequency of the converter. Voltage mode control is used in both the analogue and digital control schemes. The experimental results show that it is possible to design a digitally controlled Buck converter that has the same performance as can be achieved using commercially available analogue control ICs. The performance of the analogue system can however be increased by using a separate operational amplifier as error amplifier. Thus analogue control is still the best option if high control bandwidth and fast transient response to load steps are important design parameters.**

I. INTRODUCTION

Over the last 5 years digital control of switch mode power converters has emerged as a real alternative to traditional analogue control methods developed over the last 40 years. Digital control of DC/DC converters can improve overall system performance by adding features such as supervision of system status, reprogrammability of control loop parameters and dynamic dead time control to improve converter efficiency [1]. All of these features can be added to a converter with analogue control, but digital control will generally reduce system cost when the abovementioned features must be incorporated into a design. The dynamic properties of digital control schemes are often claimed to be better than or equal to analogue control schemes, but this is generally only true if the digital control methods relies on non-linear techniques [2-7] that are not directly comparable to well known analogue control methods.

In this paper a comparison of a State-of-the-Art digital control scheme for a DC/DC converter with high control loop bandwidth [8] is compared to an analogue Voltage Mode Control scheme with fixed switching frequency. Both the analogue and digital control methods are Linear Time Invariant (LTI). A low voltage Buck converter with synchronous rectification that would typically be used as a Point Of Load converter was chosen as the control object since fast dynamic response to changes in the load current is important in this type of application.

A comparison of the digital control scheme and an analogue solution based on a commercially available control IC is presented. The comparison shows that the error amplifier of analogue control IC limits the performance of the analogue control scheme and an improved analogue design is introduced, which shows that an optimal analogue control circuit has better performance than digital control for LTI systems.

II. THE ANALOGUE AND DIGITAL CONTROL SCHEME

The purpose of this chapter is to describe the analogue and digital control schemes theoretically and the differences between the two control methods. Both the PWM modulators and the compensators of the analogue and digital control schemes differs and the reason for this will be explained.

The analogue control scheme utilizes a Type III compensation network as shown in Fig. 1. The combined effect of the two zeroes and poles from the Type III transfer function results in a maximum phase boost of 180 degrees which is necessary in order to achieve a phase margin of 45 degrees or greater. The values of the passive components in the compensation network are calculated based on the desired phase boost and crossover frequency as a function of the K factor as described in [9] and [10]. The transfer function of the analogue compensator is shown in (1).

The two zeros, ω_{z1} and ω_{z2}, boosts the phase to achieve a good phase margin and the two poles are placed at frequencies above the intended crossover frequency of the control loop to attenuate any noise on the output voltage in the feedback loop. Resistor R_4 in Fig. 1 has a negligible effect on the compensator transfer function and is therefore not included in the transfer function.

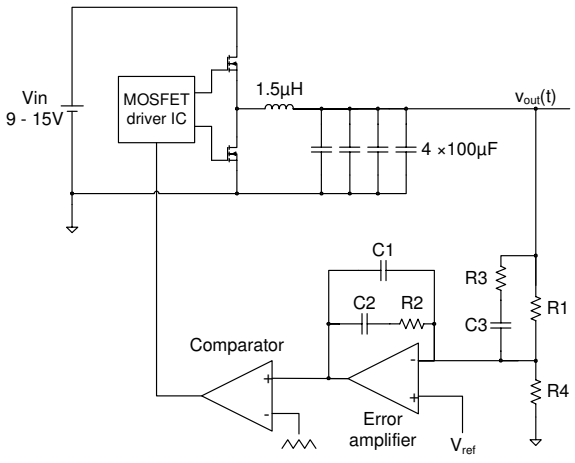

Fig. 1. Block diagram of the analogue design

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$$G_{comp,analogue}(s) = K \cdot \frac{(s+\omega_{z1})(s+\omega_{z2})}{s(s+\omega_{p1})(s+\omega_{p2})} \quad (1)$$

where

$$K = \frac{R_1 + R_3}{R_1 \cdot R_3 \cdot C_1} \quad (2)$$

$$\omega_{z1} = \frac{1}{R_2 \cdot C_2} \quad (3)$$

$$\omega_{z2} = \frac{1}{(R_1 + R_3) \cdot C_3} \quad (4)$$

$$\omega_{p1} = \frac{C_1 + C_2}{R_2 \cdot C_1 \cdot C_2} \quad (5)$$

$$\omega_{p2} = \frac{1}{R_3 \cdot C_3} \quad (6)$$

The digital control scheme shown in Fig. 2 is based on a Digital Self-Oscillating Modulator [8] that allows the sampling frequency of the digital compensator to be higher than the switching frequency. A block diagram of the DiSOM modulator used in the digital control scheme presented in this paper is shown in Fig. 3. The DiSOM generates a triangular carrier on the input of the comparator with hysteresis by integrating the difference between the switching output, i.e. the PWM signal, and the duty cycle command (designated 'Ref' in Fig. 3). One important feature of the DiSOM modulator is that the switching frequency is a function of the duty cycle command. Equation (7) gives the mathematical expression for the switching frequency as a function of the duty cycle[8].

$$f_{sw} = \frac{2^n \cdot f_{clock}}{Window} \cdot (D - D^2) \quad (7)$$

where f_{sw} is the switching frequency, D is the duty cycle command, f_{clock} is the clock frequency of the DiSOM, n is the resolution of the duty cycle command in bits and *Window* is the hysteresis window.

The digital design is an LTI control system and the digital compensator used in the design is a PID compensator with two zeros and an integrator. Both the DiSOM modulator and the digital compensator have been implemented in an FPGA to reduce computational delays. The transfer function of the digital PID compensator is

$$G_{comp,digital}(z) = \frac{b_0 + b_1 \cdot z^{-1} + b_2 \cdot z^{-2}}{1 - z^1} \quad (8)$$

The digital compensator has two zeros given by (9) and one integrator, but no high frequency poles to attenuate noise on the output voltage. The compensator transfer function was chosen because it was simple to implement in the FPGA, but also because adding high frequency poles only works if the sampling frequency is very high. Any high-frequency noise above the Nyquist frequency present on the output voltage should be attenuated by an analogue anti-aliasing filter to avoid unwanted aliasing of the high-frequency noise. The frequency, at which the two zeros are placed, can be calculated by using the general definition of the z variable given in (10), where f is the frequency and T_s is the sampling time of the digital compensator.

$$z_{1,2} = \frac{-b_1 \pm \sqrt{b_1^2 - 4 \cdot b_0 \cdot b_2}}{2 \cdot b_0} \quad (9)$$

$$z \equiv e^{j2\pi f \cdot T_s} \quad (10)$$

The difference between an analgoue and a digital control system is that the analogue system works in continous time whereas the digital system is a discrete time system. The ADC is the sampling element of the digital control system and the sampling frequency imposes a limitation on the attainable control loop bandwidth for the Buck converter. A rule of thumb says that the open loop bandwidth of any digital control system must be 6 to 10 times lower than the sampling frequency. The upper limit for the open loop bandwidth of a Buck converter with analogue control is approximately 3 times lower than the switching frequency. For the digitally controlled Buck converter to have a bandwidth equal to that of the analogue controlled Buck converter the sampling frequency must be higher than the switching frequency. Most digital PWM modulators for a single phase Buck converter do not allow the sampling frequency to be higher than the switching frequency which was the reason for choosing the DiSOM modulator.

The implementation of the digital compensator and PWM modulator in the FPGA will add a delay between the time the ADC samples the output voltage and the time the duty cycle command for the PWM modulator is updated and takes effect on the PWM output. The delay will cause negative phase shift in the open loop transfer function. Further negative phase shift will require an extra boost in the phase of the compensator to achieve the same phase margin as for a system with no delay. The delay of the digital implementation of the DiSOM modulator and the digital PID compensator is just nine clock cycles, which corresponds to 180ns with a clock frequency of 50MHz.

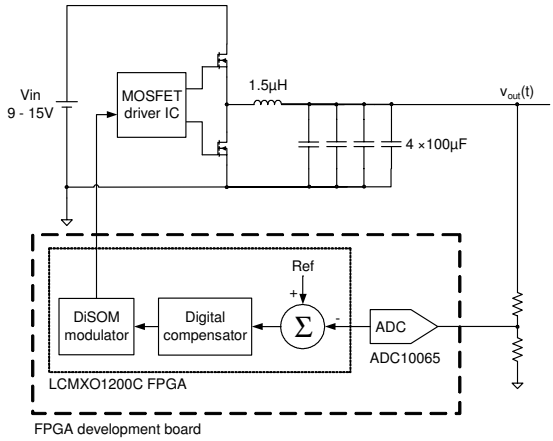

Fig. 2. Block diagram of the digital design

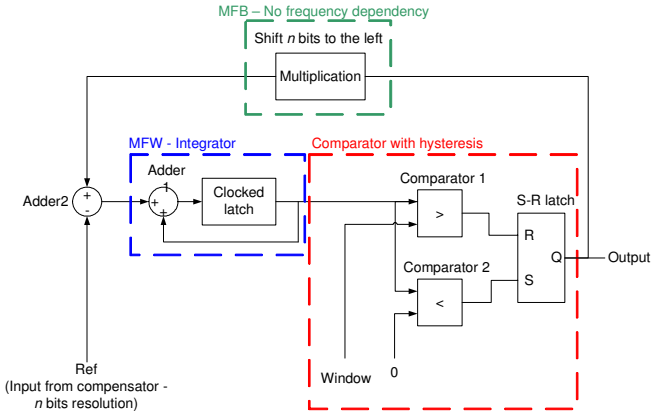

Fig. 3. The DiSOM modulator

In this design the delay is not a major concern because it is less than 1/10th of the PWM time period. The sampling frequency is selected at two time the nominal switching frequency of 400kHz. The switching frequency varies slightly with load current because the duty cycle is increased to account for the conduction losses in the MOSFETs at high output current, but the ratio between sampling and switch frequency remains approximately 2 to 1.

III. Experimental Results

One digital prototype and two analogue prototypes was designed for the comparison. The common converter specifications of the prototypes are listed in Table I and their individual control specifications are listed in Table II. A picture of Digital #1 and Analogue #1 are shown in Fig. 4 and 5 respectively. The analogue prototypes where build because no analogue reference designs where found matching the digital design mainly due to the large filter inductor and small filter capacitor.

TABLE I
COMMON CONVERTER SPECIFICATIONS

Input voltage	9-15Vdc
Output voltage	2.0Vdc
Output current	0-10A
Filter inductor	1.5µH
Four filter capacitors (ceramic X7R)	4x100µF
Single filter capacitor ESR	1.4mΩ

TABLE II
INDIVIDUAL CONTROL SPECIFICATIONS

Prototype	Switching frequency	Band-width	Phase margin	Control
Digital #1	~400kHz	38kHz	60°	FPGA
Analogue #1	400kHz	40kHz	60°	TL5001
Analogue #2	400kHz	80kHz	45°	TL5001

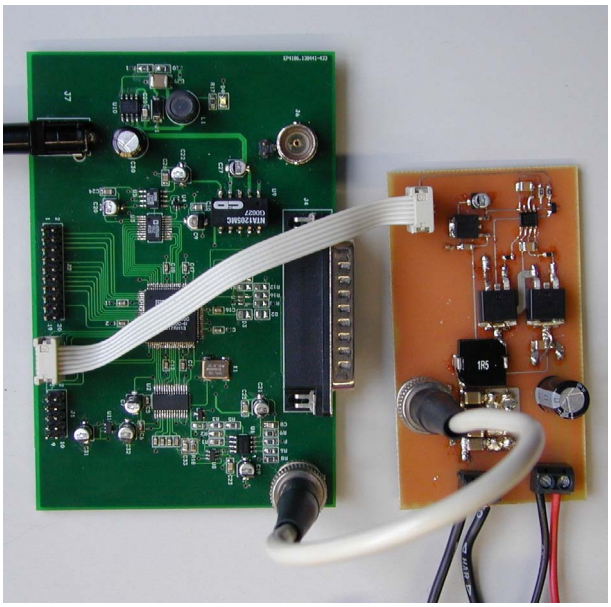

Fig. 4. Digital #1 prototype

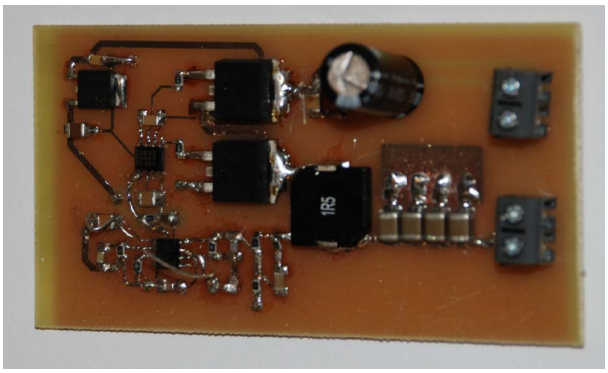

Fig. 5. Analogue #1 prototype

The closest analogue reference designs found were [11] and [12]. In reference [11] the switching frequency is 600kHz and the open loop bandwidth is 37.5kHz. The output capacitance was 3280 µF and the inductor was 400nH.

The small output capacitance used in this paper is realized with four ceramic capacitors achieves small physical size but places higher demands on the compensator to achieve a fast transient response than if a large electrolytic capacitor had been used. The ESR of the output capacitor adds a zero to the output filter, which adds +90° at frequencies above the zero. Due to of very low ESR the zero is moved to a very high frequency and the phase shift of the output filter is -180° at the crossover frequency. Because the phase is -180° the compensator needs to boost the phase more to achieve a good phase margin. Analogue #1 and Analogue #2 utilize a typical of the shelf voltage mode control chip (TL5001) with a gain bandwidth of 1.5MHz for the error amplifier.

The converter design, component selection and PCB layout for the Digital #1 prototype are copied to all analogue prototypes. Thus it is only control circuitry that is changed which ensures a fair comparison of the control methods.

The digital compensator was designed to achieve the highest possible bandwidth without affecting the stability of the converter. A relatively high phase margin of 60° was chosen because stability is not purely a matter of the theoretical stability margins of control loop but also a matter of the PCB layout and other practical considerations. An improved design with the A/D converter placed right next to the converter output might be less sensitive to noise, which would allow higher gain in the compensator without making the system unstable and the control loop bandwidth of the digital design could be increased.

The compensation network of Analogue #1 was designed to match the open loop characteristics of Digital #1 in order to show that the analogue and digital prototypes are comparable which is confirmed by the measured open loop transfer functions in Fig. 6. The bandwidth is 40 kHz which is 1/10th of the switching frequency. The low frequency gain of Digital #1 is approximately 3 dB higher than that of Analogue #1, which will make the transient response of Digital #1 slightly faster than that of Analogue #1.

Load step measurements for Analogue #1 and Digital #1 are shown in Fig. 7 and Fig. 8 and the performance of the two converters further confirms a fair comparison. The load current is changed from 10 to 5A and the output voltage overshoot of approximately 50mV and a settling time of approximately 20µs. The performance of Digital #1 is a marginally better than the performance of Analogue #1 which can be explained by the slightly higher loop gain of Digital #1 at low frequency.

Analogue #2 was designed to investigate how much better a typical analogue control implementation can be compared to State-of-the-Art digital control. The designed bandwidth was set to 80 kHz which is 1/5th of the switching frequency but Analogue #2 proved to be unstable due to the low bandwidth of the error amplifier in the control IC. Fig. 9 shows the theoretical and measured transfer functions of the compensator and transfer function of the error amplifier. The measured compensator deviates from the theoretical design, due to the insufficient gain and increased negative phase shift at frequencies above 10 kHz in the error amplifier, and thus the phase margin suffers causing the instability.

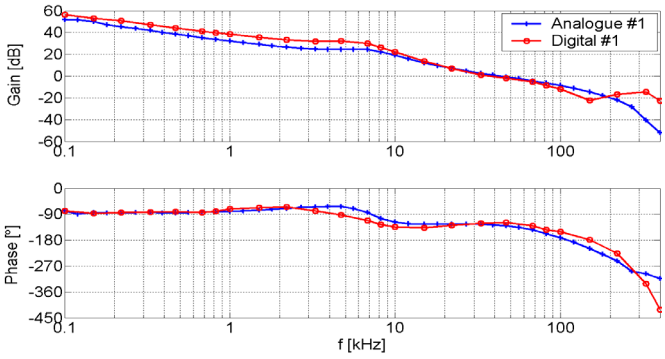

Fig. 6 Open loop transfer function for the Analogue #1 and Digital #1

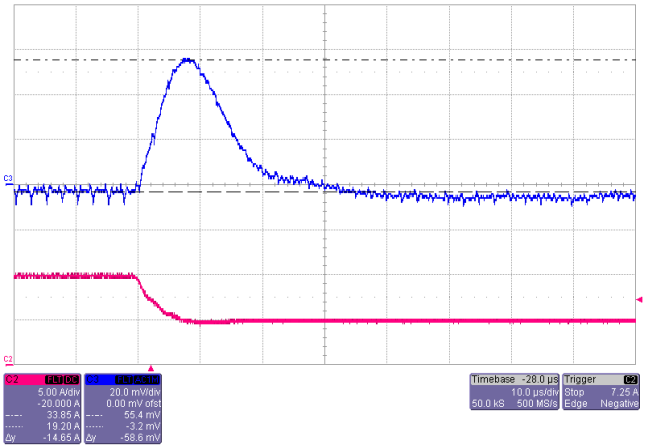

Fig. 7. Load step (10 to 5A) for Analogue #1
Upper trace: Output voltage AC coupled 20 mV/div
Lower trace: Output current 5A/div
Time scale: 10 µs/div

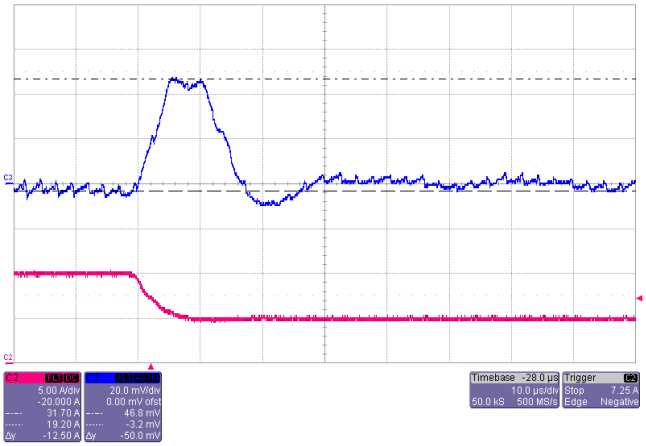

Fig. 8. Load step (10 to 5A) for Digital #1
Upper trace: Output voltage AC coupled 20 mV/div
Lower trace: Output current 5A/div
Time scale: 10 µs/div

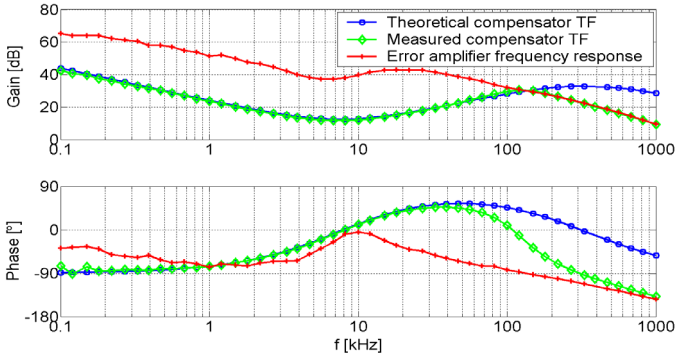

Fig. 9. Comparison of theoretical and measured compensator transfer function

A. Improved analogue control

New and improved controllers with ten times higher error amplifier bandwidth than the TL5001 are available which are integrated in one package with a gate driver, e.g. the ISL6439

from Intersil. But this improvement is not sufficient to show the full advantage of analogue control. A new control circuit was therefore implemented in a 3rd prototype (Analogue #3). A picture of Analogue #3 is shown in Fig. 10. The control circuitry of Analogue #3 is similar to the block diagram in Fig. 1. It consist of an operational amplifier with 150Mhz unity gain bandwidth (ST10502) for the error amplifier, a shunt regulator (ZR431) for the reference voltage, a fast comparator (LMV7219) for PWM generation and a triangular waveform generator implemented as shown in Fig. 11 to generate the carrier. The control circuitry is driven from a single 5V supply created with a linear voltage regulator connected to the input voltage of the converter.

The load step measurement for Analogue #3 in Fig. 12 shows an output voltage overshoot of only 16mV and a settling time of 10µs. The overshoot is 68% lower than Analogue #1 and Digital #1 and the settling time is decreased by a factor of 2. Fig. 13 shows a bode plot of analogue #1 and Analogue #3. Analogue #3 has a bandwidth of 80kHz which is 1/5 of the switching frequency and it has a DC-gain close to 80dB. The high performance of Analogue #3 is due to a factor two increase in bandwidth and a 30dB higher DC-gain.

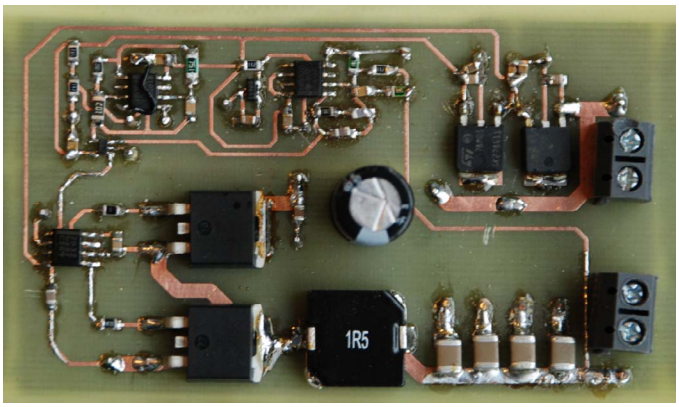

Fig. 10. Analogue #3 prototype

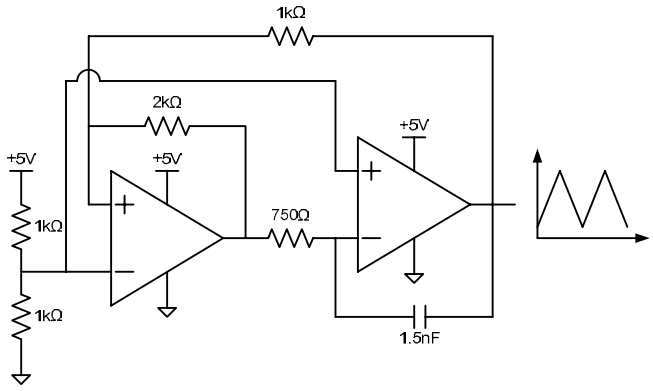

Fig. 11. Single supply 400kHz triangle generator

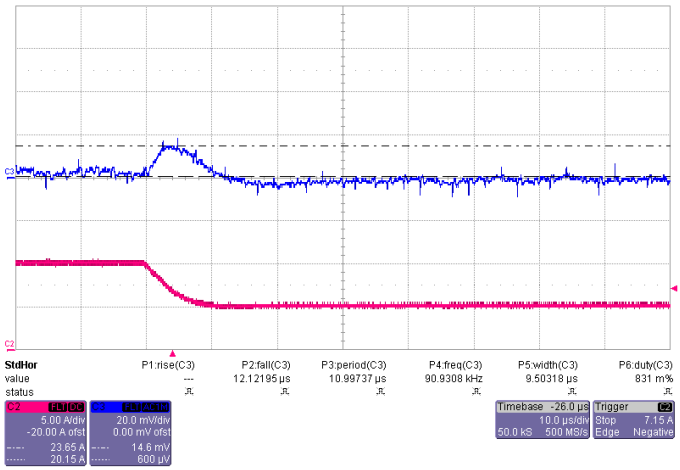

Fig. 12. Load step (10 to 5A) for Analogue #3
Upper trace: Output voltage AC coupled 20 mV/div
Lower trace: Output current 5A/div
Time scale: 10 µs/div

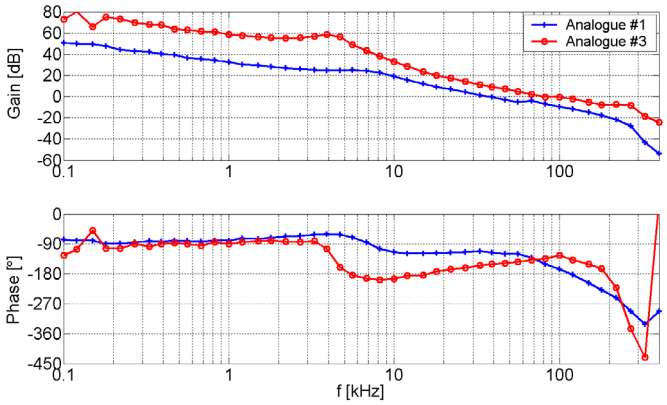

Fig. 13. Open loop bodeplot of Analogue #1 and Analogue #3

B. Compensator specifications

TABLE III is a list of the component values for the compensation network of Analogue #1 and Analogue #3. The parameters for the digital compensation are shown in TABLE IV. The ADC input range is limited by the digital implementation in such a way that it only measures in a small band around the reference voltage of 2.0V. The LSB of the ADC corresponds to 1.34mV on the output voltage.

The placement of the zeros and poles for the three prototypes are given in TABLE V. The zeros and poles of Analogue #3 are moved up in frequency compared to Analogue #1 to get a higher control bandwidth. Because the high frequency poles are placed at frequencies above the switching frequency the converter will be more susceptible to noise which makes it more important to make a good PCB design.

TABLE III
ANALOGUE COMPENSATION PARAMETERS

	Analogue #1	Analogue #2
R_1	10 kΩ	1.1 kΩ
R_2	5.1 kΩ	15 kΩ
R_3	620 Ω	56 Ω
R4	10 kΩ	1.8 kΩ
C_1	140 pF	22 pF
C_2	4.7 nF	480 pF
C_3	2.2 nF	4.7 nF

TABLE IV
DIGITAL COMPENSATION PARAMETERS

Clock frequency	50 MHz
Reference input resolution	10 bit
Hysteresis window	20480
Effective ADC resolution	6 bit
Effective ADC range	1.957 – 2.043V
Sampling frequency	800 kHz
b_0	12.8125
b_1	22.6875
b_2	9.9375

TABLE V
ZERO AND POLE PLACEMENT FOR THE THREE DESIGNS

	Digital #1	Analogue #1	Analogue #3
fz_1	3.06 kHz	6.64 kHz	22.1 kHz
fz_2	29.3 kHz	6.81 kHz	29.29 kHz
fp_1	-	229.5 kHz	504.4 kHz
fp_1	-	116.7 kHz	604.7 kHz

IV. CONCLUSION

A comparison of linear digital and analogue control schemes for a low voltage Buck Converter typically used in Point of load applications has been presented. Both the digital and analogue control schemes use voltage mode control and are based on linear time invariant compensation. The experimental results show that it is possible with a state-of-the-art digital control scheme to achieve similar performance as can be achieved with a typical analogue control IC, in this case the TL5001 from Texas Instruments. The open loop bandwidth of both systems was approximately 40 kHz for a Buck converter switching at 400 kHz. The bandwidth of the analogue control scheme was shown to be limited by the error amplifier of the chosen control IC.

The bandwidth can be increased by using a separate operational amplifier with high gain bandwidth as an error amplifier. A third converter was built with the control circuit designed with discrete components instead of a typical control IC. The control loop bandwidth of the optimized design was 80 kHz. The load step response of the optimized design is about twice as fast as that of the digital design and the overshoot on the output voltage is reduced by 68%. The disadvantage of the optimized analogue control circuit is that it requires an operational amplifier with a gain bandwidth of 150 MHz and the complete control circuit has to be built using discrete components.

The experimental shows that linear digital control still has some way to go before it can perform as well as analogue control.

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23 Appendix I – Publication by L. T. Jakobsen et al.

L. T. Jakobsen, O. Garcia, J. A. Oliver, P. Alou, J. A. Cobos and M. A. E. Andersen

"Interleaved Buck Converter with Variable Number of Active Phases and a Predictive Current Sharing Scheme"

IEEE Power Electronics Specialists Conference 2008, pp. 3360 – 3365, 2008

Interleaved Buck Converter with Variable Number of Active Phases and a Predictive Current Sharing Scheme

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***Abstract*—The efficiency of an interleaved Buck converter is typically low at light load conditions because of the switching losses in each of the switching stages. Improvements in the converter efficiency can be achieved by dynamically changing the number of active phases depending on the load current. This paper addresses the issues related to the transient response of the converter when the number of active phases is changed by a digital control scheme. The problem arises because the current in the individual phases of the interleaved Buck converter will not be equal immediately after the controller has changed the number of active phases. This paper proposes a current equalisation scheme that adjusts the duty cycle of each phase in a manner that ensures equal average inductor current in all active phases in one or two PWM periods. The current equalisation scheme relies on the measurement of the output current and the knowledge of a few converter parameters and it does not require a measurement of the current in each phase. A digital PWM modulator has been designed that allows the current equalisation scheme to work. Simulations and measurements for a four phase interleaved Buck converter are presented and shows that the predictive current equalisation scheme can equalise the phase currents in a single PWM period.**

I. INTRODUCTION

The efficiency of interleaved Buck converters is typically high at power levels close to nominal output power but is falling considerably at light load because of the switching losses in each of the phases in the interleaved Buck converter. It is therefore advantageous to reduce the number of active phases of an interleaved Buck converter at light loads to increase efficiency [1]. Reference [1] presented the mathematical analysis for improving the converter efficiency through changing the number of active phases depending on the load current but the experimental results presented showed some room for improvements. The main problem of turning a phase in an interleaved converter either ON or OFF is that the currents in the phases will not be equal immediately after the change occurs, which will cause the output voltage to deviate from the steady state output voltage.

The purpose of this paper is to develop a dig ital control method for an interleaved Buck converter with a variable number of active phases, which ensures equal average phase currents in a very short time span after a change in the number of active phases. The proposed current equalisation scheme does not rely on the measurement of each phase current but uses a predictive algorithm to determine the duty cycle of each phase, which will result in equal currents in the active phase.

II. PREDICTIVE CURRENT SHARING DURING PHASE TURN-ON OR PHASE TURN-OFF

Predictive current equalisation relies on sampling the output current and determining when to change the number of active phases based on the output current level. Under the assumption that the converter phases are perfectly matched the average current of each active phase is at any time equal to the output current divided by the number of active phases. The concept relies on determining the duty cycle for each phase, which provides equal average inductor current in all phases when the digital control scheme changes the number of active phases. The change in average current in any phase can be expressed as:

$$\Delta i_{L,x} = \frac{I_{out}}{n_{phases}} - I_{avg,x} \quad (1)$$

where $\Delta i_{L,x}$ is the change in current of phase x, I_{out} is the output current, and $I_{avg,x}$ is the average current in phase x before the number of active phases is changed.

The duty cycle command for each phase can be calculated by determining the average slew rate (di/dt) of the inductor current for one switching period as a function of the duty cycle. It is possible to calculate the duty cycle command for each active phase since the necessary change in the current is known from (1).

Fig. 1 shows an example of how the predictive current equalisation scheme works. The figure shows an example where the load current is increasing slowly. The number of active phases is two to begin with and it is changed to three when the load current is 5A. The predictive current equalisation scheme sets the duty cycle for each phase independently to achieve an equalisation of the average inductor current in all active phases in a single PWM period. Without the predictive current equalisation scheme the current in the phases would slowly converge towards the same average value.

The predictive current equalisation scheme works best if the load current changes slowly. For load steps with fast slew rate the predictive current equalisation scheme will not be able to equalise the phase currents perfectly because the load current is not exactly equal to the value

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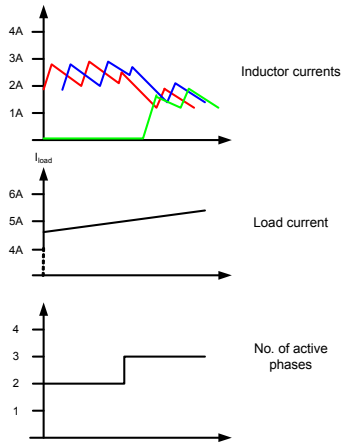

Figure 1. Predictive current sharing during phase turn-ON

that the predictive current equalisation scheme assumes when calculating the duty cycle command for each active phase.

The advantages of the predictive current equalisation scheme are that the phases share the current almost instantaneously after the number of active phases has been changed thereby limiting the stress on the individual phases. The transient response on the output voltage should also be smaller than it would be without the current equalisation scheme.

The inductor current slew rate of each phase for the ON and OFF period of the phase PWM signal is given by equation (2) and (3) and the average slew rate over one switching period is given by (4). Based on equation (4) it is possible to determine the change in the average inductor current as a function of the duty cycle D (5). Equation (5) can be also written as (6), which gives the required duty cycle to achieve a given change in the average inductor current, Δi_L.

$$\alpha_{ON} = \frac{di}{dt} = \frac{V_{in} - V_{out}}{L} \tag{2}$$

$$\alpha_{OFF} = \frac{di}{dt} = \frac{-V_{out}}{L} \tag{3}$$

$$\alpha_{avg} = \left\langle \frac{di}{dt} \right\rangle_{T_{sw}} = \frac{D \cdot V_{in} - V_{out}}{L} \tag{4}$$

$$\left\langle \Delta i_L \right\rangle_{T_{sw}} = T_{sw} \cdot \frac{D \cdot V_{in} - V_{out}}{L} \tag{5}$$

$$D = \frac{\Delta i_L \cdot L}{T_{sw} \cdot V_{in}} + \frac{V_{out}}{V_{in}} \tag{6}$$

The above expression for the duty cycle, D, can be divided into a change in duty cycle, ΔD (see (7)), plus a steady state value, D_{SS} (see (8)). The steady state value of the duty cycle will be equal to the output of the digital PID compensator before the number of active phases is changed and the change in duty cycle is a fixed value for a specific set of parameters, i.e. input voltage V_{in}, inductor size L and PWM time period T_{sw}.

$$\Delta D = \frac{\Delta i_L \cdot L}{T_{sw} \cdot V_{in}} \tag{7}$$

$$D_{SS} = \frac{V_{out}}{V_{in}} \tag{8}$$

The predictive current equalisation scheme works by measuring the output current, and when a change in the number of active phases is necessary it reads the appropriate values of ΔD from a lookup table and adds them to the duty cycle command on the output of the digital PID controller during the equalisation period. Under steady state operation the duty cycle command calculated by the digital compensator determines the duty cycle for all active phases. Depending on the converter specifications it will be possible to equalise the phase currents within one or two PWM periods. If the equalisation scheme has to run over two PWM periods, it will be necessary to calculate the appropriate ΔD for each PWM period.

The duty cycle of a phase that is turned ON has to be higher than the steady state duty cycle and the duty cycle of the other active phases has to be lower than the steady state duty cycle for the phase currents to be equalised. The output voltage of a typical synchronous Buck converter used in Point of Load converter applications is typically much lower than the input output voltage. This means that the converter operates with a low steady state duty cycle. Since the duty cycle can not be lower than zero it will in certain situations not be possible to reduce the current in a phase to the new average current in a single PWM cycle. In that situation it will be necessary to let the predictive current equalisation scheme equalise the current in two or more PWM cycles. The basic operation is the same but the change in duty cycle, ΔD, is divided by the number of PWM periods and applied to the relevant phases in consecutive PWM periods until equalisation has been achieved.

It should be mentioned that the purpose of the predictive current equalisation scheme is to achieve an equalisation of the average inductor current when the number of active phases is changed. If general current sharing in steady state operation is required it must be implemented separately.

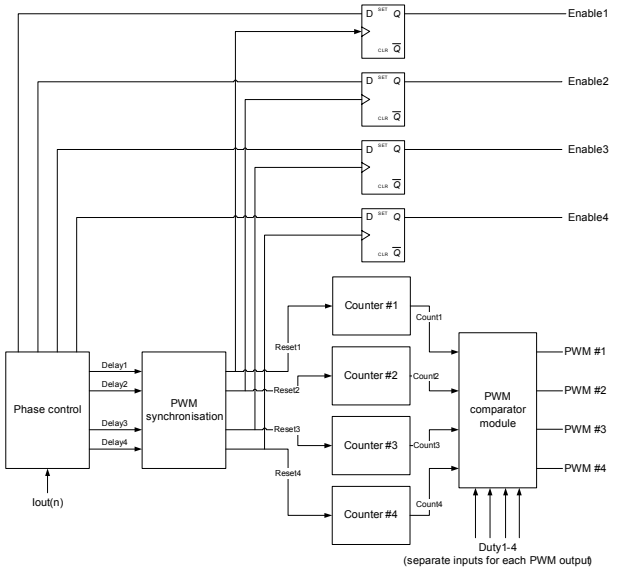

Figure 2. PWM modulator for a four phase interleaved Buck converter with a variable number of active phases

III. PWM Modulator for the Predictive Current Equalisation Scheme

The PWM modulator for the interleaved Buck converter (see Fig. 2) has been designed to accommodate the predictive current equalisation scheme. The PWM modulator consists of four independent counters which are controlled by the 'PWM synchronisation' block. The 'PWM synchronisation' block controls the timing of the active PWM signals for the active phases to ensure that the phase shift between the phases matches the number of active phases. If for instance three phases are active the 'PWM synchronisation' block will generate reset signals for counters #1, #2 and #3 that are 120 degrees out of phase. The PWM synchronisation block receives the phase shift information from the 'Phase control' block. The 'Phase control' block determines the number of active phases based on the sampled output current $I_{out}(n)$.

An enable signal for each phase is generated by a D flip-flop. The D flip-flop is used to synchronise the enable signal with the rising edge of the PWM signal for the phase. Synchronisation of the enable signal is important for the predictive current equalisation scheme to work. If the enable signal is not synchronised to the PWM signal the average current of the phase which is activated will not reach the correct value in the first PWM cycle. Synchronisation is achieved by setting the enable signal high on the D-input of the flip-flop before the reset signal is set. The D flip-flop will set the enable signal on the rising edge of the reset signal from the 'PWM synchronisation' block.

The 'PWM comparator module' generates the PWM signals for the four phases by comparing the output of the four counters with the duty cycle command for the respective phases.

The PWM modulator shown in Fig. 2 has many similarities to other digital multiphase PWM modulator implementations [2-4]. The PWM modulators of [2] and [3] have only one duty cycle command input which is used to determine the duty cycle of all phases. The advantage of this approach is that the complexity and size of the PWM modulator is low but with limitation that the duty cycle cannot be controlled individually for the separate phases. The PWM modulator of [4] has separate duty cycle command inputs for each phase but it does not generate enable signals for each phase.

IV. Charge Pump Supply for Gate Drive ICs

In order for the predictive current equalisation scheme to work it is important that each phase of the interleaved Buck converter can start immediately when the enable signal generated by the digital controller is activated. A charge pump supply for the high side driver of the gate drive ICs has therefore been added to be able to turn ON the high side MOSFET immediately after the gate drive IC has been enabled [5]. A schematic of the charge pump supply is shown in Fig. 3. The charge pump is controlled by the signal *CP_clock* which is generated by the digital controller. The frequency of *CP_clock* is the same as the switching frequency and it has a duty cycle of 50%. The output voltage lies across C102 which is connected to gate drive ICs bootstrap input.

The charge pump supply ensures constant supply voltage for the high side gate drive. An identical charge pump circuit has to be used for each phase which increases the component count and complexity of the interleaved Buck converter.

V. Control System Configuration

Fig. 4 shows a block diagram for the control system for the four phase interleaved Buck converter with the predictive current equalisation scheme. The digital control scheme has been implemented in an FPGA and it can be divided into three main blocks. The PWM modulator has already been described in section III. The digital compensator is a PID compensator with the transfer function:

$$G_{comp}(z) = \frac{b_0 + b_1 \cdot z^{-1} + b_2 \cdot z^{-2}}{1 - z^{-1}} \tag{9}$$

The digital compensator has been implemented as a state machine it can calculate the duty cycle command in just three clock cycles from the time it reads the sampled output voltage from the ADC [6]. The final block of the digital control scheme is the Duty cycle Look-up table which is controlled by the PWM modulator. The Duty cycle Look-up table is controlled by the PWM modulator which determines when the number of active phases must be changed and gives the appropriate command for the Look-up table. When the converter operates in steady state with a fixed number of active phases the Duty cycle Look-up table is inactive and passes the duty cycle $D_{ss}(n)$ directly to all phases. During a transient condition when the number of active phases is changed the Duty cycle Look-up table adds a term to each duty cycle command to ensure current equalisation. The terms added to the duty cycle command have been calculated based on (7) and a set of ΔDs for each possible change in the number of active phases, i.e. an increase or decrease of the number active phases, are stored in the Duty cycle Look-up table.

The system uses two ADCs to sample the output voltage and output current of the interleaved Buck converter. The ADC that samples the output current is an 8-bit 1 MSPS Successive Approximation ADC with an input voltage range from 0 to 3.3V. The ADC sampling the output voltage is a 10-bit 50 MSPS pipelined ADC with an input voltage range from 0.95 to 1.95V. The reason for using two ADCs is that the requirements for the two ADCs are different.

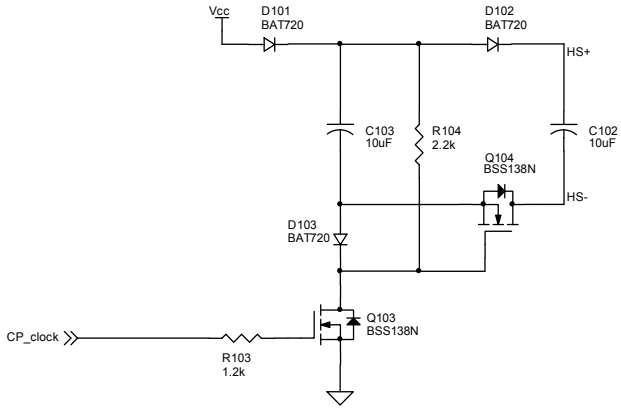

Figure 3. Schematic of the charge pump supply for the high side gate drive

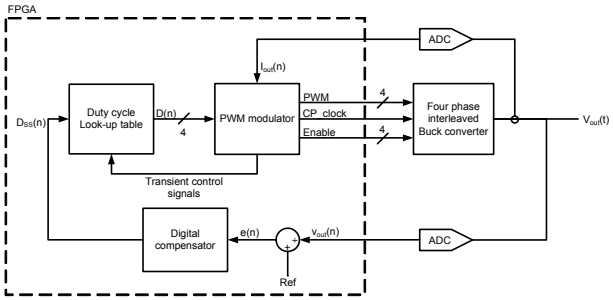

Figure 4. Block diagram of the control system

The ADC sampling the output current must be able to sample current levels over the full output current range but it does not have to be very fast since a small delay in determining when to change the number of active phases is of small consequence. The speed of the ADC sampling the output voltage on the other hand is important because it affects the control loop bandwidth and stability. A fast ADC with a small delay makes it possible to achieve a high control loop bandwidth which leads to a faster transient response.

Ideally the predictive current equalisation scheme should be extended to include a measurement of the converter input voltage. The average inductor current slew rate is a function of the input voltage as expressed in (5). The ΔD values stored in the Duty cycle Look-up table have been calculated at the nominal input voltage and the predictive current equalisation scheme will therefore work well at nominal input voltage but the performance deteriorates when the input voltage different from the nominal value. If the Duty cycle Look-up table was extended to include different set of ΔDs for different input voltage levels the predictive current equalisation scheme would have consistent performance over the full input voltage range.

VI. Simulattions and Measurements

A four phase interleaved Buck converter was designed to test the proposed predictive current equalisation scheme. The converter specifications are shown in TABLE I. and a picture of the prototype design can be seen in Fig. 5. The output current is measured through a shunt resistor and it is sampled at the per phase switching frequency. The output current range is divided into four ranges where only one phase is active in the lowest range, two phases are active in the second range and so on. A small hysteresis band was added around the current levels at which the number of phases changes to ensure stable operation.

TABLE I.

Converter specifications

Parameter	Value
Input voltage	9 – 15V
Output voltage	1.8V
Nominal load current	10A
Inductor size per phase	10µH
Output capacitance	200µF
Switching frequency per phase	208kHz

Figure 5. Prototype converter (right) and FPGA board (left)

Fig. 6 and Fig. 7 show a simulation and the corresponding measurement of a load step for the multiphase interleaved Buck converter without the predictive current equalisation scheme. The output voltage drop is approximately 50mV in the simulation and it is close to 80 mV for the measurement. The phase currents slowly converge towards the same average current due to the series resistance of the inductors.

Fig. 8 and Fig. 9 show simulation and measurement for the same load step but this time the predictive current equalisation scheme is active. The output voltage drop due to the load step has become worse for the simulation whereas the measurement is similar to the measurement of Fig. 7.

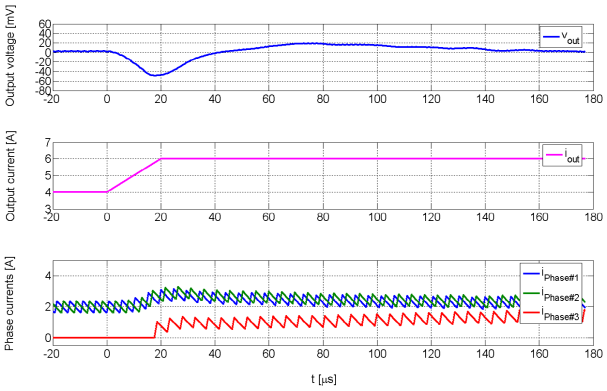

Figure 6. Simulation of load step from 4 to 6A without predictive current sharing

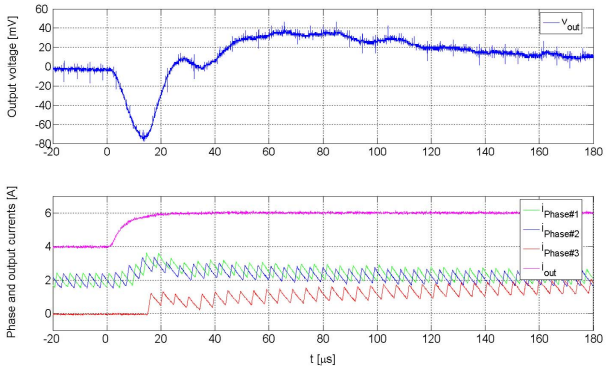

Figure 7. Measurement of load step from 4 to 6A without predictive current sharing

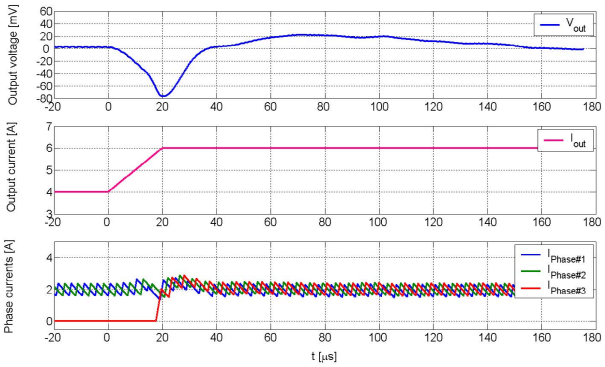

Figure 8. Simulation of load step from 4 to 6A with predictive current sharing

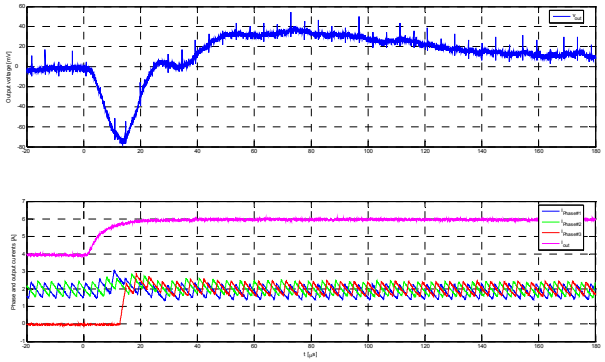

Figure 9. Measurement of load step from 4 to 6A with predictive current sharing

There are two reasons why the predictive current equalisation scheme does not reduce the transient on the output voltage when the number of active phases is changed. The first reason is that there is a short delay between the time the load current passes the 5A threshold and the time the number of active phases is changed. Both Fig. 8 and 9 show that the current in phase #1 and #2 increases slightly before phase #3 is activated and the current equalisation scheme tries to equalise the currents. The second reason is that the digital output voltage control loop under any circumstances will not be able to hold the output voltage constant when a load step occurs. Fig. 10 shows a measurement of the same loadstep from 4 to 6A for the interleaved converter with all four phases active. There is a small improvement in the transient response on the output voltage but it is not much.

It appears that no improvement has been achieved with the current equalisation scheme during a load step where the number of active phases is changed at least not on the transient response of the output voltage. It must however be noticed that by equalising the phase currents the component stresses are the same for all phases, thus minimizing the stress of each phase.

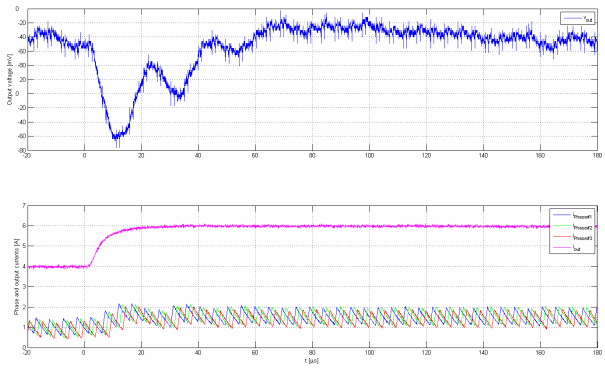

Figure 10. Measurement of load step from 4 to 6A with all phases active

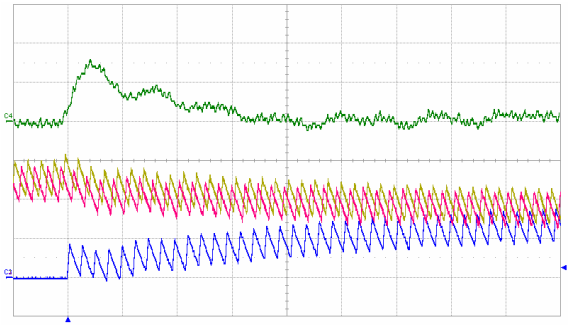

Figure 11. Phase turn-ON with constant load current (I_{load} = 5.0A) without predictive current sharing.
C1: $i_{phase\#1}$ (1A/div DC coupled) Yellow
C2: $i_{phase\#2}$ (1A/div DC coupled) Pink
C3 $i_{phase\#3}$ (1A/div DC coupled) Blue
C4: v_{out} (20mV/div AC coupled) Green
Time base: 20µs/div

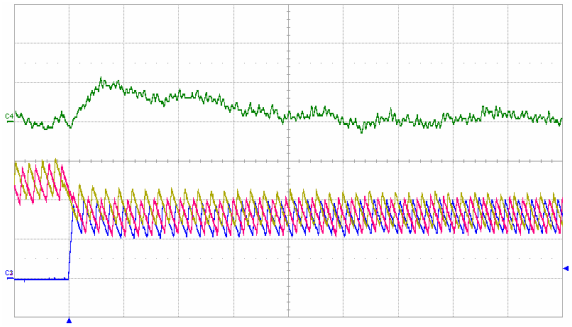

Figure 12. Phase turn-ON with constant load current (I_{load} = 5.0A) with predictive current sharing.
C1: $i_{phase\#1}$ (1A/div DC coupled) Yellow
C2: $i_{phase\#2}$ (1A/div DC coupled) Pink
C3 $i_{phase\#3}$ (1A/div DC coupled) Blue
C4: v_{out} (20mV/div AC coupled) Green
Time base: 20µs/div

In Fig. 10 and Fig. 11 the load current is held constant at 5A while the number of active phases is changed from 2 to 3. The purpose of these measurements is to show the output voltage response to a change in the number of phases under a constant load. The output voltage overshoot is smaller with the predictive current equalisation (Fig. 11) than without the predictive current equalisation scheme (Fig. 10). The digital controller changes the number of active phases in a periodic manner

in the measurements of Fig. 10 and Fig. 11. Under normal operating conditions the digital controller will not change the number of active phases if the load current is constant and the number of active phases is only changed with the purpose of testing the transient response on the output voltage.

VII. CONCLUSION

A predictive current equalisation scheme for an interleaved Buck converter with a variable number of active phases has been presented. The digital control scheme equalises the phase currents by adding a value, which has been calculated in advance, to the duty cycle command of each PWM signal that controls the active phases, depending on the number of active phases and the output current level. Experimental results and simulations show similar responses to a load step, which forces a change in the number of active phases from 2 to 3. A measurement of the change in the number of phases at a constant output current shows that the predictive current equalisation scheme leads to a smaller transient on the output voltage.

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24 Appendix J – Paper draft by L. T. Jakobsen et al.

L. T. Jakobsen and M. A. E. Andersen

"Mixed Signal Control Scheme for a Single Phase Power Factor Correction Preregulator based on an 8-bit Microcontroller"

Submitted for review for the IEEE Transactions on Power Electronics

"Mixed Signal Control Scheme for a Single Phase Power Factor Correction Preregulator based on an 8-bit Microcontroller"

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The contents of this manuscript have been presented in part at the IEEE Applied Power Electronics Conference 2005 (Austin, TX) in March 2005. The paper was entitled "Hybrid Control Method for a Single-Phase PFC Using a Low Cost Microcontroller".

Keywords: Digital Control, Power Factor Correction, Microcontrollers

Abstract: Digital control for PFC preregulators presents certain advantages over analogue control. Digital control does not suffer from temperature and CMOS process variations that are inherent to analogue control ICs. The diadvantage of digital control for a PFC preregulator is that the digital control scheme must sample the inductor current and the rectified line voltage with a sampling frequency that is equal to the switching frequency and calculate the duty cycle command within one PWM period to be able to accuraty control the input current. A Digital Signal Controller can be used to control a PFC preregulator but it is an expensive solution. The mixed signal control scheme that is presented in this paper has an analogue current control loop and a digital output voltage control loop that is implemented in a low cost microcontroller. The mixed signal control scheme incorporates input voltage feed-forward in the microcontroller software algorithm. Two implementations of the mixed signal control scheme implemented in two different microcontrollers are proposed. The first implementation uses a large microcontroller and an external EPROM as a lookup table and the second implementation is implemented in a small 8-pin microcontroller. Both implementations utilize a small fraction of the computational resources of the microcontrollers. The mixed control scheme has been tested on a 1kW Boost PFC preregulator. The two designs meet the specifications of the EN61000-3-2 class A regulations and have good transient responses.

I. INTRODUCTION

Power Factor Correction (PFC) Preregulators have become very important with the introduction of new regulations, such as the EN61000-3-2 in Europe, for input current distortion of electronic devices connected to the utility grid. The PFC preregulator, which is typically a Boost converter, must draw an input current that is in phase with the line voltage and with low total harmonic distortion (THD). The preferred control method for a PFC delivering more than 250W is analogue control with an average current mode control loop to control the input current and a slow control loop to control the output voltage.

A typical control IC for this control method is the UCC3817A from Texas Instruments. The UCC3817A includes an analogue hardware multiplier block, which generates the current reference. The analogue hardware multiplier suffers from large variations in gain as a function of temperature but also because of variations in the CMOS process used in the production of the IC. The hardware multiplier in the UCC3817A is a good example of how much the gain of the hardware multiplier block varies. The hardware multiplier in the UCC3817A has a gain that can vary between 0.5 and 1.5 [1].

The large variations in the gain of the hardware multiplier must be taken into account in the design of the PFC to ensure stable operation. Designing the control while taking the variations in gain into account means that the average current mode control loop must be designed in such a way that it is stable under all conditions. The performance of the average current control loop is thus in most cases not optimal because it was designed to be stable in a worst case situation that rarely occurs.

Digital control of PFC preregulators is a subject that has attracted much attention over the last decade. Digital control has the advantage that the performance is independent of process and temperature variations.

A digital average current mode control scheme that is similar to the analogue control scheme of the UCC3817A has been published several papers [2-4]. The average current mode control scheme

samples the inductor current of the Boost converter and the rectified input voltage for every PWM period. Based on the sampled values of the inductor current and rectified line voltage the current control scheme calculates the duty cycle for the following PWM period. The average current mode control scheme samples the inductor current in the middle of either the ON- or OFF-period of the PWM signal. By sampling in the middle of either the ON- or OFF period the digital control scheme samples the average value of the inductor current directly and without the need for an external lowpass filter [2].

Sampling the inductor current and the rectified input voltage every PWM period and calculating the duty cycle requires a digital device that is capable of performing arithmetic operations quickly. The A/D converter of the digital controller hardware must be able to sample at least two signals for every PWM period in the average current mode control scheme. Low cost microcontrollers are not capable of meeting these requirements and a more expensive Digital Signal Controller (DSC) is typically chosen instead.

Many digital average current controls schemes are implemented without input voltage feed-forward which is used in analogue control ICs to make the performance of the PFC control loop independent of the input voltage RMS value. Input voltage feed-forward requires the digital controller device to perform division of two numbers which is an operation that cannot be done in a few clock cycles. The digital controller must be able to perform all calculations that are required to calculate the new duty cycle command in one PWM period. If the switching frequency is just moderately high it will be impossible even for a modern DSC to perform a division within one PWM period.

One example of a digital control scheme that does implement input voltage feed-forward is reference [4]. Input voltage feed-forward in an analogue control scheme divides by the input voltage RMS value squared. Reference [4] simplifies that by generating an internal sinusoidal reference for the current loop and because the sine wave reference is generated internally with a

fixed amplitude it is only necessary to divide by the input voltage RMS value and not the square of that. The division routine is thereby simplified and can be performed within the allotted time.

Feed-forward current control is a way to reduce the input current distortion in a digitally controlled PFC [5]. The bandwidth of a digital average current mode control loop has an important influence on the input current distortion of the PFC. The distortion will be large if the bandwidth of the digital current loop is low. The feed-forward control can decrease the input current distortion by adding a term to the duty cycle command calculated by the current compensator of the average current mode control scheme. The feed-forward terms is a function of the rectified input voltage, the current reference signal for the current compensator and the output voltage. The feed-forward scheme improves the performance of the PFC but it also increases the number of calculations that the digital controller device must perform.

Reference [6] has a similar control scheme with a feed-forward term but the digital implementation is very different from that of reference [5]. The control scheme in reference [6] has been implemented in an FPGA that can perform multiple parallel operations at the same time whereas the control scheme of reference [5] was implemented in a 16-bit DSP. The advantage of parallel operations is that the digital controller device can operate at a lower clock frequency a DSP and still be able to perform the same calculations. The clock frequency may be lower but the cost of the digital controller hardware is probably higher than the price of DSC.

Another digital control scheme for a PFC implements a digital charge control scheme that samples the inductor current with a sampling rate of 5 MSPS and integrates the sampled current digitally [7]. The control scheme is implemented in an FPGA and with a very fast A/D converter to sample the inductor current.

A general problem in PFCs is that the control loop bandwidth for the output voltage control loop has to be much lower than the frequency of the input voltage in order to achieve low input current distortion. If the bandwidth is too high the ripple voltage on the output, which has a frequency of two times the line frequency, will pass through the compensator in the voltage control loop. If the

ripple voltage passes through the compensator it will be multiplied with the rectified input voltage and cause third harmonic distortion on the reference signal for the current control loop. Low bandwidth will result in a slow transient response to load current changes with a large output voltage deviation.

Reference [8] and [9] proposes digital control schemes that obtain low input currents distortion and fast transient response for a PFC preregulator. Reference [8] proposes that the resolution of the A/D converter sampling the output voltage should be so coarse that it does not detect the ripple voltage. If the A/D converter does not detect the ripple voltage the bandwidth of the voltage loop can be increased without increasing the input current distortion. Reference [9] proposes a digital comb filter that has a large attenuation at harmonic frequencies of the output voltage ripple. The bandwidth of the output voltage control loop can be increased to a frequency that is higher than the frequency of the input voltage without causing high input current distortion.

Mixed signal control schemes for PFC preregulators have been described in references [10], [11] and [12]. The mixed signal control schemes combines analogue control circuitry for the average current mode control loop and a have a digital output voltage control loop. The mixed signal control scheme is chosen because a cheaper digital device can be used to control the PFC preregulator than if a fully digital control scheme is implemented. Reference [10] used the analogue control IC UC3854, which is a predecessor to the UCC3817A, to implement the analogue control circuit. The digital voltage control loop is implemented in a 16-bit microprocessor. A multiplying D/A converter was used to generate an analogue reference signal for the current loop in the UC3854. The current reference signal was passed through the hardware multiplier of the UC3854. The control scheme will therefore encounter the limitations as the analogue control scheme due to the analogue hardware multiplier.

Reference [11] uses a microcontroller (PIC16C782) that has a peripheral module that simplifies the design of a mixed signal control scheme for a PFC preregulator. The control scheme does not utilize input voltage feed-forward and the microcontroller software is a simple PI compensator for

the output voltage control loop. The digital output from the PI compensator is used to control a D/A converter that is included in the PIC16C782. The D/A converter generates the reference signal for the analogue current control loop.

This paper will describe mixed signal control scheme implemented in an 8-bit microcontroller. The mixed signal control scheme incorporates digital input voltage feed-forward. A simple circuit called a switched multiplier is used instead of a multiplying D/A converter. The microcontroller software has been optimized to utilize only a fraction of the computing resources of the microcontroller. Two different designs are presented with the same basic control scheme. The difference between the two designs is the choice of microcontroller is different. In the first design a microcontroller with many I/O ports and a large EPROM is used. The second design is based on a small 8-pin microcontroller and without an external EPROM. The first design has a utilizes a very small percentage of the microcontroller's resources whereas the second design has a higher utilization factor.

II. THE MIXED SIGNAL CONTROL SCHEME

The proposed control scheme (see Fig. 1) is similar to the control scheme in a typical analogue control IC for a PFC, e.g. the UCC3817A from Texas Instruments, with an inner control loop that controls the input current of the PFC and an outer control loop that controls the output voltage. The input current must be in phase with the input voltage to obtain a power factor close to unity. The voltage loop controls the input power of the PFC by adjusting the amplitude of the input current. To ensure low input current distortion the control signal from the voltage loop must be close to constant during steady state operation.

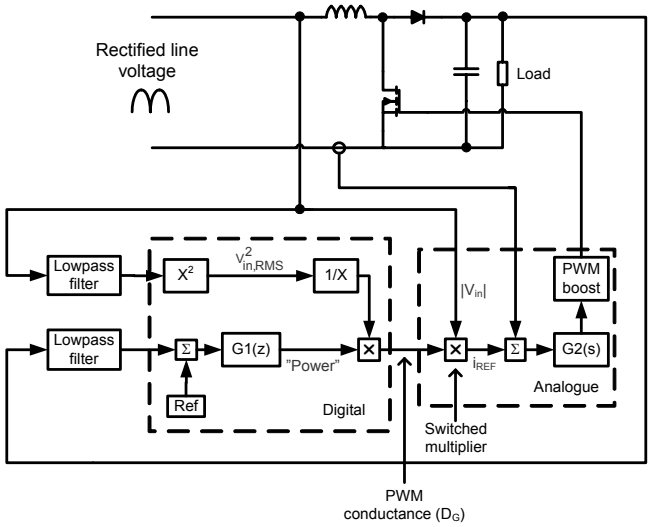

Fig. 1 Proposed control scheme for the mixed signal control scheme for a PFC

The goal of this design is to use a microcontroller in the voltage control loop. The voltage control loop samples two signals. The first signal is the output voltage, which is lowpass filtered to attenuate the output voltage ripple. The ripple voltage on the output of the PFC has a frequency which is two times the line frequency. The second signal is the line RMS voltage, which is used as a feed-forward signal to ensure constant gain in the control loop independent of the line RMS voltage. The output of the compensator, *G1(z)*, is divided by the line voltage feed-forward signal squared. The reason for implementing the voltage loop controller in a microcontroller is to avoid gain variations in the analogue hardware multiplier block that performs this arithmetic operation in

analogue control ICs. There are no gain variations in a microcontroller and it is therefore possible to a control system with better performance.

The software algorithm that performs the control loop calculations in the microcontroller is optimized for a short execution time to minimize the computational load on the microcontroller. By minimizing the computational load it is possible to use a cheap microcontroller running at a low clock frequency. The sampling frequency of the voltage control loop should therefore be low to reduce the number of computations performed by the microcontroller. The idea is that the same microcontroller can be used for other purposes additional to the control loop algorithm for the PFC. The unused resources of the microcontroller could also be utilized by adding functionality such as supervision and external communication to the PFC control algorithm.

The current control circuit is analogue because of the relatively high bandwidth of the current control loop compared to the bandwidth of the control loop for the output voltage. If the current control loop was to be implemented in the microcontroller the inductor current and the rectified line voltage had to be sampled with a sampling frequency equal to the switching frequency of the PFC as described in [2]. Implementing the current control loop in the microcontroller would impose two requirements in the selection of a suitable microcontroller or Digital Signal Controller. The first requirement is the A/D converter sampling rate, which has to be in the order of hundreds of kilo-samples per second or even higher depending on the sampling scheme used in the current control loop. The second requirement is the number of instructions per second, typically given as Million Instructions Per Second (MIPS), that the microcontroller needs to perform. The number of computations that the microcontroller must perform are increased dramatically since it has to compute a new duty cycle value every PWM period. By using an analogue control circuit in the current loop it is only necessary to sample the output voltage and line RMS voltage at low sampling rate since the bandwidth of the output voltage control loop has to be lower than the line frequency to get a power factor close to unity.

The switched multiplier (see Fig. 1) has the same function as the multiplying D/A converter that

was used in reference [10]. The switched multiplier generates the reference signal for the analogue current control loop. The switched multiplier is a very simple circuit with good linearity. A PWM signal generated by the microcontroller controls the switched multiplier

III. The Current Control Loop

Fig. 2 shows a block diagram of the current control loop. The current control loop uses an average current mode control scheme to control the inductor current in the Boost converter. Average cuurent mode control is used because it achieves low input current distortion for the PFC. The inductor current is measured and subtracted from the current reference signal and a PI-compensator generates a control voltage. The control voltage is compared to a sawtooth voltage and the output of the comparator is the "PWM Boost" signal for the Boost converter.

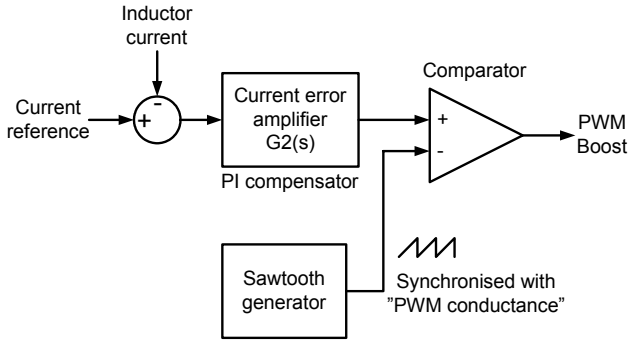

Fig. 2 Block diagram of current control loop

The reference signal for the current control loop is generated by a switched multiplier (see Fig. 3), which works as a multiplying D/A converter as already mentioned in section II. The switched multiplier multiplies the line voltage and the reference signal labeled 'PWM conductance' generated by the microcontroller.

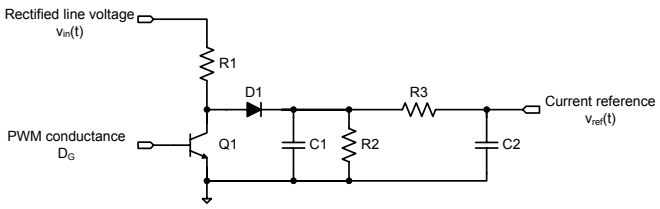

Fig. 3 Schematic for a switched multiplier

The low frequency gain of the switched multiplier is a function of the duty cycle, D_G, of the reference signal. The gain of the switched multiplier is

$$G_{sw,mult} = \frac{v_{ref}(t)}{v_{in}(t)} = \frac{(1-D_G)\cdot R2}{R1+(1-D_G)\cdot R2} \tag{1}$$

The expression for the low frequency gain was determined by using circuit averaging over one period of the PWM signal.

The lowpass filter on the output of the switched multiplier consisting of R3 and C2 reduces the high-frequency ripple on the reference signal for the current control loop. The transfer function of the switched multiplier has two poles both of which have been placed at 2.5 kHz. Fig. 4 shows Bode plots for the switched multiplier for three values of D_G. If the two poles of the switched multiplier are placed at too low a frequency relative to the line frequency, the reference signal will be distorted compared to the rectified grid voltage resulting in increased input current distortion.

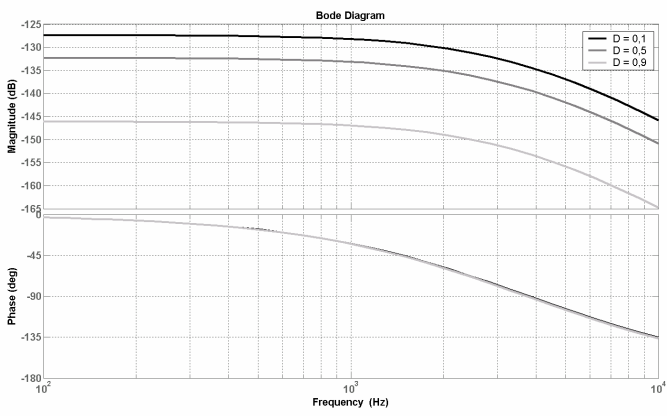

Fig. 4 Bode plots for the switched multiplier for D = 0.1, D = 0.5 and D = 0.9

The Sawtooth generator used in the average current mode control scheme is synchronized with the ’PWM conductance’ signal controlling the switched multiplier to avoid sub-harmonic oscillations of the PWM frequency in the current control loop. Synchronisation is achieved by resetting the sawtooth generator on the rising edge of “PWM conductance”.

IV. The Output Voltage Control Loop

The design of the output voltage control loop was based on the model in Fig. 5. Two types of compensators were considered for the voltage control loop. The first type was a Proportional (P) compensator, which is a simple gain with no frequency dependency and the second type was a Proportional-Integral (PI) compensator which has pole at DC and one zero.

The P-compensator has the advantage of a faster step response at load steps compared to the PI-compensator. The disadvantage of the P-compensator on the other hand is that the output voltage is dependent on the output power since there is no integrator to ensure zero steady state error. The proportional gain determines how strong the dependency of the output voltage is as a function of the output power. The larger the proportional gain is the less the output voltage will decrease as the output power is increased.

If a PI-compensator is used the total phase shift is -180º at frequencies below the zero of the PI-compensator because the output capacitor adds -90º to the phase shift of the open-loop transfer function of the voltage loop and the PI compensator has a phase shift of -90º below the corner frequency. The lowpass filter in the output voltage feedback adds further negative phase shift at frequencies above the filter cutoff frequency and the overall result will be a lower phase margin or reduced open loop bandwidth compared to what is obtainable with the P-compensator.

The P-compensator is chosen mainly because it is less complex to implement in the microcontroller and therefore utilizes less of the microcontrollers computing power than a PI-compensator would. Secondly, the P-compensator will make it possible to achieve higher control loop bandwidth and better phase margin resulting in better dynamic response to transient load conditions.

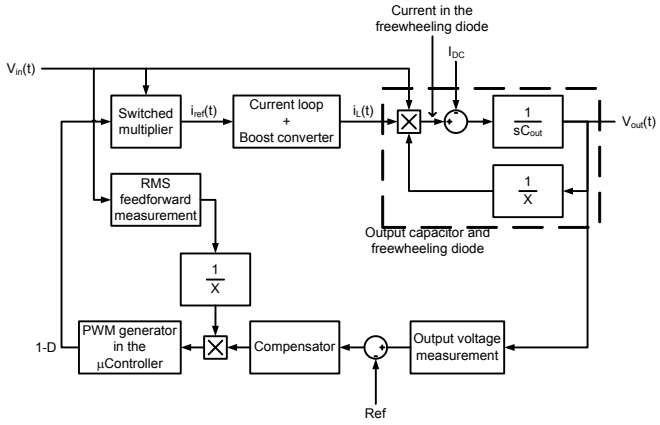

Fig. 5 Model of the voltage loop

The distortion of the input current is mainly due to the ripple voltage on the output of the PFC, which has a frequency that is two times the line frequency. The ripple voltage can pass through the compensator in the voltage loop and is multiplied with the rectified line voltage in the switched multiplier. The distortion caused by the output voltage ripple is mainly third harmonic distortion and can result in large total harmonic distortion of the input current.

To reduce the distortion of the input current a lowpass filter is inserted into the feedback path for the output voltage. The lowpass is inserted into the feedback to attenuate the output voltage ripple in the output voltage control loop. The filter cutoff frequency must lower than the frequency of the output voltage ripple and it can be realised either as an analogue filter on the input of the A/D converter sampling the output voltage or as a digital filter implemented in the microcontroller. The advantage of using an analog filter is that the microcontroller will not have to perform a filtering algorithm. The advantage of the digital filter is that the filter transfer function does not change with temperature or over time, which makes it possible to design a more accurate control loop.

The lowpass filter will limit the control loop bandwidth to a frequency below the output voltage ripple frequency and typically below the line frequency as well. However, the low pass is necessary to reduce the input current distortion. The transient response on the output voltage to a load step will be slow due to the limited control loop bandwidth. If high bandwidth is a requirement the problem can be solved by using a comb filter instead of a simple lowpass filter. The comb filter effectively attenuates the output voltage ripple but without limiting the control loop bandwidth [9].

The use of a comb filter will increase the number of calculations that the microcontroller must perform, especially if a microcontroller without a digital hardware multiplier is used. The comb filter also requires a large memory area and updating the memory every time the control loop algorithm is executed will impose a large burden on the microcontroller. In order to keep the microcontroller utilization to a minimum it was decided not to use a comb filter in the output voltage loop. Another solution proposed in reference [8] was to let the quantization step of the A/D converter that samples the output voltage be larger than the peak-to-peak ripple voltage. The large quatization step effectively removes the output voltage ripple from the digital representation of the output voltage. Reference [8] reports that it is possible to increase the control loop bandwidth because the ripple voltage is removed but the poor A/D converter resolution causes limit cycling to occur on the output voltage at low output power.

It was decided that a first order digital IIR lowpass filter was the best choice. Fig. 6 shows a block diagram of the proposed first order IIR filter. The filter has the transfer function

$$H_{IIR}(z) = \frac{\frac{1}{b+1}}{1 - \frac{b}{b+1} \cdot z^{-1}} \tag{2}$$

A simple implementation of the digital filter in the program code for the microcontroller is of great importance to ensure a low utilization of the microcontroller. The gain b in the implementation of the IIR filter is selected as a power of 2 to enable the microcontroller to do the multiplication by shifting the contents of the digital word that is multiplied by b one or more places to the left. The second multiplication is implemented as a division, which has to be computed by the microcontroller. The choice of filter cutoff frequency is limited by this implementation, because b can only take on values that are powers of 2, but it simplifies the program code for the microcontroller significantly.

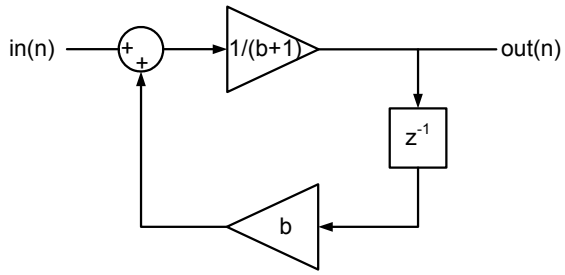

Fig. 6 Realization of the digital IIR filter

The input voltage feed-forward that is part of the digital control scheme requires the a division of the output of the compensator by the square of the line RMS voltage. Several methods for calculating the RMS value digitally was considered, including methods involving sampling of the input voltage with either high or low sampling frequency and different digital filter algorithms. All of the solutions considered were found to involve a large number of computations and a much simpler solution was selected. The chosen method is to use an analogue second order lowpass filter with two real poles placed at approximately 15 Hz on to the rectified line voltage. The voltage of the output of the filter is DC voltage with a small AC ripple. The DC voltage is proportional to the mean value of the rectified grid voltage. For a pure sinewave the ratio between the mean value and RMS value is 0.9 and the mean value can be used as a good approximation of the RMS value. Even if the grid voltage has large third harmonic distortion the ratio between mean and RMS value is still close to 0.9. The voltage on the output of the filter is sampled by the microcontroller and the result is used in the calculation of the duty cycle, D_G.

V. A/D Converter and Digital PWM Resolution

The A/D converter and the PWM generator resolution are important parameters for the mixed signal control scheme. If resolution of the PWM signal that controls the switched multiplier, i.e. the signal “PWM conductance”, is low the distortion of the input current will be large at low output power. Poor resolution results in a large change in the gain of the switched multiplier if the least significant bit of the duty cycle-register in the PWM generator changes value. The result is a large

change in the input power drawn from the grid and the consequence of this will be limit cycling on the output voltage. Poor resolution in the A/D converter measuring the output voltage will also result in limit cycling.

In the implementation of the mixed signal control scheme for the PFC with a PIC16F877A microcontroller the resolution of the PWM generator is 9 bits at a switching frequency of 39.1 kHz. The clock frequency of the microcontroller is 20 MHz. The A/D-converter in the PIC16F877A has a resolution of 10 bits. The effective resolution has been increased by reducing the measuring range to $1/5^{th}$ of the full input range of the A/D converter. The resolution of the input voltage RMS value measurement is 8 bits.

VI. Digital Hardware and Software Implementation

The purpose of the software design is to minimize the number of computations in the microcontroller in order to use as cheap a microcontroller as possible. Two different ways of implementing the software in a microcontroller has been designed. Before the two designs can be described in detail it is necessary to consider which computations the microcontroller needs to perform and what challenges that poses for the micrcontroller.

Referring to (1) it can be seen that the amplitude of the input current drawn from the utility grid is proportional to $1 - D_G$ where D_G is the duty cycle of the PWM signal that controls the switched multiplier. It follows from this that the compensator actually calculates $1 - D_G$, but to set the duty cycle in the microcontroller it is the duty cycle, D_G, that needs to be calculated. The equation, which the microcontroller must solve is given by (3).

$$D_G(n) = D_{\max} - \frac{\left(Ref - v_{out}(n)\right)}{v_{in,RMS}^2(n)} \cdot K_p \tag{3}$$

where D_{max} is the maximum duty cycle of the PWM signal, *Ref* is the digital reference for the

output voltage, $v_{out}(n)$ is the sampled output voltage, $V_{in,RMS}(n)$ is the sampled line RMS voltage and K_P is the proportional gain of the P compensator.

The maximum duty cycle is as close to 1 as possible to enable the microcontroller to reduce the reference signal for the current control loop to zero. If the duty cycle is equal to 1 the gain of the switched multiplier is zero and the current reference signal will be zero.

The order in which the calculations required to solve (3) are performed is important for the accuracy of the result. The correct order of execution for the calculations is shown in Fig. 7. If the calculations are not executed in the correct order important information will be lost, because the microcontroller is a fixed-point processor with limited word length.

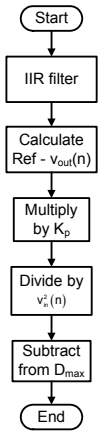

Fig. 7 Order of calculations in software

The IIR filter algorithm constitutes a shift operation to achieve the multiplication by the coefficient *b*, a 16-bit addition and a 16-by-4 bit division. The divisor is limited to 4 bits to reduce the execution time of the division routine. The filter coefficient *b* can only take on values of 1, 2, 4 and 8 because the divisor is limited to 4 bits.

The proportional gain K_p for the designed prototype must be 8034 to obtain a voltage drop of no more than 20V at full load compared to the nominal output voltage of 385V. The gain K_p requires at least a 13-bit number in a fixed point processor and the resolution of the output voltage measurement is 10 bits. In practice the microcontroller has to do a 16-by-16 bit multiplication but the result can be limited to a 24-bit number. The division by the square of the input voltage will be a

24-by-16 bit division. The two subtractions are both 16-by-16 bit subtractions. The execution time for the calculations, assuming a full software implementation with no optimizations, is estimated to be approximately 400μs.

The two software designs presented below are optimized with different aims. The first design is optimized to reduce number of commands performed by the microcontroller to an absolute minimum. The second design is optimized with the aim of using the cheapest possible microcontroller and reduce the number of commands as much as possible. The first design is based on the 40-pin PIC16F877A microcontroller and the second design utilizes the 8-pin PIC12F683 both from Microchip.

The Interrupt Service Routine (ISR), which performs the control loop algorithm, of both designs have been programmed in assembly language. Assembly language allows the programmer to optimize the software to a greater extent than a high level programming language. If the software was programmed in a high level programming language such as C, the C-compiler that compiles code into machine code for the microcontroller would optimize the code according to a predefined optimization algorithm. The optimization algorithm of the compiler does not necessarily fit the requirements of the specific application.

The execution time of a 16-by-16 bit multiplication followed by a 24-by-16 bit division is quite long for the 8-bit microcontrollers from Microchip. Instead of doing the calculations in real time in the microcontroller all calculations can be calculated by a computer and stored in a lookup table. It will be possible fot the microcontroller to read the duty cycle from a lookup table in a shorter time than it takes to perform the calculation in real time. The first design uses a lookup table because it is much faster than performing the calculations in real time it was used in the first implementation.

The resulting values of the duty cycle for each combination of the lowpass filtered output voltage and input voltage was calculated and programmed in a 64 kB EPROM. The EPROM was connected externally to the PIC16F877A. Fig. 8 shows the flowchart for the interrupt service routine in the PIC16F877A.

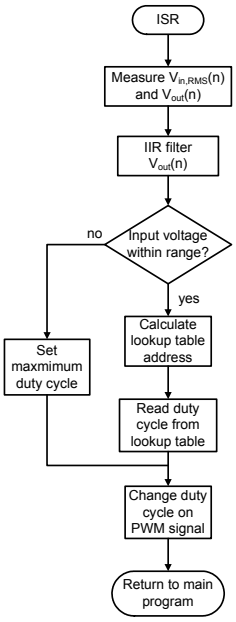

Fig. 8 Flowchart for the microcontroller software for PIC16F877A

First the line RMS voltage and the output voltage is sampled by the microcontroller and stored in $V_{in,RMS}(n)$ and $V_{out}(n)$ respectively. Second the IIR filter algorithm is applied to $V_{out}(n)$. The contents of the lookup table only stores values for the input voltage operating range of the PFC. The microcontroller sets the duty cycle to D_{max} to shut down the PFC if the line voltage is out of range. If the line voltage is within range then the microcontroller calculates the appropriate address for the lookup table and reads the duty cycle, D_G, from the lookup table. The microcontroller finally sets the new duty cycle value for the "PWM conductance" signal and exits the ISR.

TABLE I shows the estimated execution time of the ISR for each of the steps in the flowchart shown in Fig. 8. The clock frequency of the PIC16F877A is assumed to be 20 MHz and each command cycle is completed in 4 clock cycles. A command cycle is defined as the time it takes to complete one assembly command.

TABLE I

Estimated execution time for the control loop algorithm in the PIC16F877A

Interrupt service routine	Execution time [Command cycles]	Execution time [μs]
2 A/D conversions	-	37
IIR filter algorithm	192	38.4
Check if input voltage is within range	23	4.6
Calculate address	43	8.6
Read D_G from lookup table	40	8
Change D_G	14	2.8
Estimated total	312	99.4

The second design is implemented in the PIC12F683 from Microchip. The software algorithm for this microcontroller does not rely on a large lookup table stored in an expensive and physically large EPROM. Therefore all calculations have to be done by the microcontroller. Some optimizations to the program code can however be implemented to reduce the utilization of the microcontroller. Fig. 9 shows the flowchart for the ISR of the cost optimized solution.

The first optimization is to use a small lookup table stored in the program memory area of the PIC12F683 to store the results for the square of line RMS voltage, $V_{in,RMS}(n)$. The lookup table is an alternative to performing an 8-by-8 bit multiplication. The second optimization lies in the multiplication of the error, e, and the proportional gain, K_P. The error is multiplied by shifting the contents of the digital word n bits to the left instead of performing a full 16-by-16 bit multiplication, where n is an integer. The choice of proportional gain is limited to powers of *2* but the reduction in execution time obtained by doing it justifies the simplification. The division of the error multiplied by the proportional gain by the square of the line RMS voltage has to be performed as a full 24-by-

16 bit division algorithm.

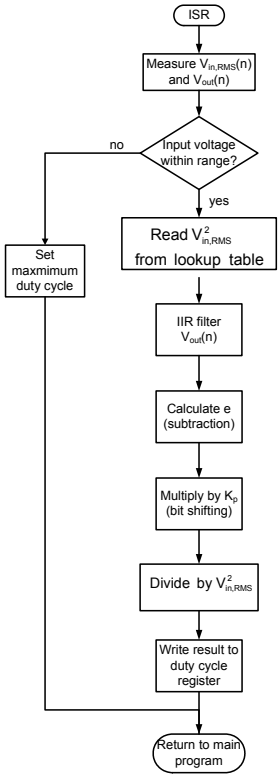

Fig. 9 Flowchart for the microcontroller software for PIC12F683

The estimated execution time of the PIC12F683 control loop algorithm (see TABLE II)) is 183.4 μs. The execution time for the PIC12F683 is almost doubled compared to the execution time of the PIC16F877A.

The difference in execution time is seemingly quite large but the sampling frequency of the system must be taken into account when the two designs are compared. The sampling frequency for the system is set at 500 Hz, which is at least 10 times the expected control loop bandwidth. The CPU utilization is defined as

$$CPU\ utilization\% = \frac{T_{execution}}{T_{sample}} \cdot 100 \tag{4}$$

The CPU utilization is 5.0% for the PIC16F877A based design and 9.1% for the PIC12F683 based design. The clock frequency for both microcontrollers is 20 MHz.

TABLE **II**

Estimated execution time for the control loop algorithm in the PIC12F683

Interrupt Service Routine	Execution time [Command cycles]	Execution time [µs]
2 A/D conversions		37
Check if input voltage is within range	23	4.6
RMS voltage squared (Lookup table)	17	3.4
IIR filter	192	38.4
Calculate e	6	1.2
Multiplication by K_p (Bit shifting)	39	7.8
24×16 bit division	403	80.6
Write result	52	10.4
Estimated total	732	183.4

VII. SIMULATIONS AND EXPERIMENTAL RESULTS

The proposed mixed signal control scheme and the two software implementations have been tested on a 1 kW PFC that has been designed to meet the EN61000-3-2 class A requirements for input current distortion. TABLE III is a list of the most important parameters for the Boost converter and the digital control circuit for both digital control solutions.

The intended application for the PFC was to supply power to an inverter that drives a pump motor. There was no specified hold up time requirement for the PFC. The main criteria in the selection of the output capacitor, was that it should be capable of handling the ripple current at nominal output power. The chosen output capacitor was therefore quite small compared to the output power that the PFC can deliver. The ripple voltage at nominal output power is 25 V

peak-to-peak for a line frequency of 50 Hz.

TABLE III

Converter and digital control circuit parameters

Parameter	PIC16F877A	PIC12F683
Output voltage	385 V	
Output power	1.0 kW	
Input voltage range	150-265 V_{RMS}	
Output capacitor	330 µF	
Inductor	1 mH	
Switching frequency	39.1 kHz	
Sampling frequency	500 Hz	
A/D resolution (Output voltage)	10 bits	
Effective measuring range (output voltage)	340 – 430 V	0 – 455 V
A/D resolution (Line voltage RMS value)	8 bits	
Effective measuring range (Line voltage RMS value)	0 – 335 V_{RMS}	

The input voltage range is not the universal range from 90 to 265 V_{RMS}. The limitation is imposed by the software and can easily be changed if required. The only real difference between the two designs is the effective measuring range of the A/D converter which measures the output voltage. In the PIC16F877A based design the effective range is limited to achieve better accuracy in the measurement of the output voltage. The A/D converter reference voltage is set by two external voltage dividers on the PIC16F877A. The reference voltage for the A/D converter can not be changed on the PIC12F683 because of the limited number of I/O pins. The A/D converter input voltage range for the PIC12F683 is 0 to 5V.

The sampling frequency of the digital voltage control loop must be at least 6-10 times higher than the control loop bandwidth in order for the digital control loop to perform well. The sampling frequency, which is 500 Hz, is ten times higher than the line frequency and the control loop bandwidth is intended to be below the line frequency.

The switching frequency was deliberately chosen to be smaller than 50 kHz. The third harmonic of the switching ripple will thereby be lower than 150 kHz, which is the lower limit in the EMC regulations. The design of the input filter for the PFC is thereby simplified because the filter will not have to attenuate the first or the third harmonic of the switching ripple. The exact switching frequency of 39.1 kHz results in a PWM resolution of 9 bits with a clock frequency of 20 MHz on the microcontroller. The duty cycle of "PWM conductance" is thus adjustable in 512 discrete steps.

The cutoff frequency of the IIR lowpass filter implemented in the control loop algorithm can be changed by changing the coefficient b (see Fig. 6). The choice of cutoff frequency and the proportional gain, K_P, affects the performance of the PFC. The filter cutoff frequency influences both input current distortion and transient response to load steps. A linear SIMULINK model of the PFC based on the model in Fig. 5, was made to investigate the properties of the control loop. The model of the current loop is a linear model and it does not take into account the switching properties of the converter. The linear model is not quite accurate because the reference signal for the analogue current control loop is generated by the switched multiplier. The linear model will however give a good idea of how the voltage control loop will perform and how large the input current distortion will be.

The performance of the mixed signal control scheme is simulated for three values of b (2, 4 and 8). The proportional gain, K_P, is the same for all three cases. The simulations are valid for the PIC16F877A design, which was the initial design. Open loop Bode plots for the three cases (see Fig. 10) shows that the bandwidth of the voltage control loop decreases with increasing values of b. The cutoff frequency of the IIR filter becomes lower when b is increased thereby reducing the open loop bandwidth.

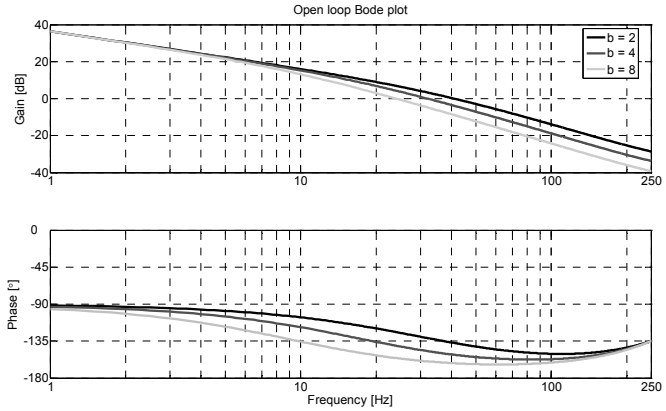

Fig. 10 Theoretical open loop Bode plot for the PIC16F877A based solution

Fig. 11 shows the simulated results for the odd harmonics of the input current and the EN61000-3-2 class A limits. The simulations show that the lower the IIR filter cutoff frequency is, i.e. the higher the value of *b* is, the lower the total harmonic distortion (THD) is. The reason is that the IIR filter attenuates the output voltage ripple most effectively when the cutoff frequency is low. The open loop bandwidth, phase margin and simulated THD of the input current are given in TABLE IV. The simulations show that the mixed signal control scheme for the PFC can meet the requirements of EN61000-3-2 for all three choices of *b.*

The input current THD is however quite high for *b* equal to 2 and 4. Based on the input current THD it would seem obvious to choose the IIR filter with *b* equal to 8 but the output voltage response to transient conditions is also of importance. Fig. 12 shows a simulation of the transient response to a load step from 100W to a 1kW at t = 0.25s and from 1kW to 100W at t = 0.75s. The output voltage falls to 310V during the positive load step for *b* equal to 8 and settles to the new steady state condition in approximately 80ms. For *b* equal to 2 the dip on the output voltage reaches 330V and the settling time is around 40ms.

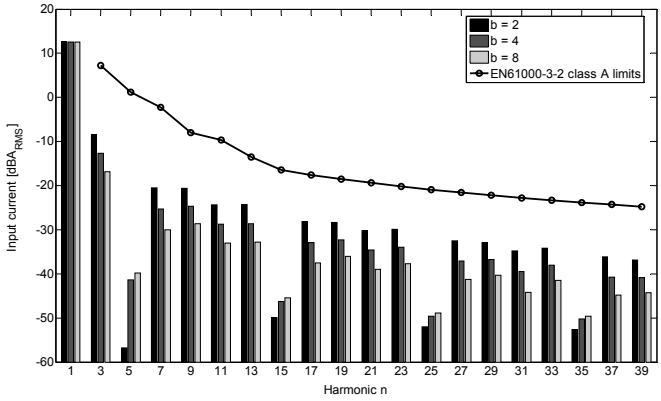

Fig. 11 Simulated harmonic content of input current for the PIC16F877A based design

TABLE IV

Theoretical control loop bandwidth and simulated input current THD for the PIC16F877A based design

	Open loop bandwidth	Phase margin	Input current THD P_{out} = 1.0kW
$b = 2$	40.5 Hz	42.9°	9.85%
$b = 4$	31.8 Hz	33.0°	6.03%
$b = 8$	23.8 Hz	24.5°	3.75%

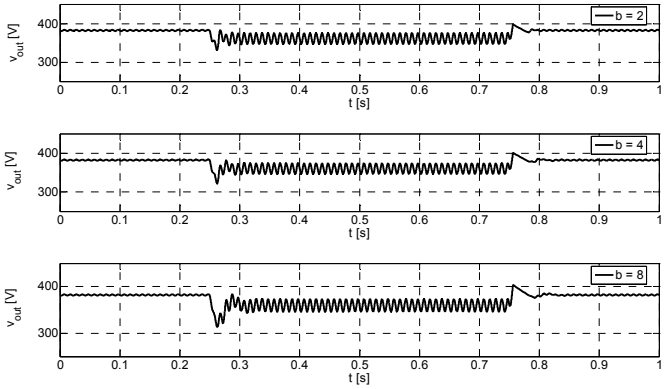

Fig. 12: Simulated response to a load step for the PIC16F877A based design

A. MEASUREMENTS FOR THE PIC16F877A BASED DESIGN

The prototype for the PIC16F877A based design was built to prove the concept of the mixed signal control scheme (see the picture in Fig. 13). The Boost converter is to the left on the picture,

the analogue current control circuit in the middle and the digital hardware is on the right.

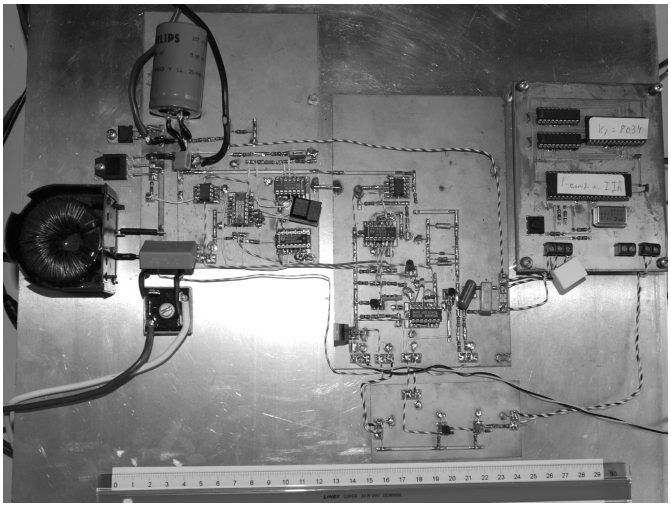

Fig. 13 The prototype for the PIC16F877A based design

Fig. 14 and Fig. 15 show measurements of the line voltage and input current at output power levels of 200W and 1kW respectively. The IIR filter coefficient, b, was equal to 8 in prototype design. The current measurement is lowpass filtered by the oscilloscope to show the mean value of the current by suppressing the switching ripple. The small jumps in the input current that can best be seen in Fig. 15 are caused by the digital control scheme that samples the output voltage with a sampling frequency of 500Hz. The output voltage ripple is not completely suppressed by the IIR filter and the control signal for the switched multiplier, i.e. the duty cycle D_G, will have a AC component with the same frequency as the output voltage ripple. The AC component will distort the input current, but instead of the continuous distortion seen in a PFC with an analogue voltage loop the distortion is discretized by the sampling of the output voltage, thereby causing the above-mentioned jumps on the input current.

The odd harmonics of the measured input current at nominal output power are plotted together with the simulation result (see Fig. 16). The THD of the measured input current is 4.94%, which is more than 1% higher than what the simulation result. The discrepancy can be explained by imperfections in the switched multiplier and the analogue current control loop. The PFC will also have some distortion around the zero crossings of the line voltage where the rectifier bridge stops conducting. The rectified line voltage will also be slightly distorted by a 1μF capacitor, which is

connected across the output of the rectifier bridge to attenuate the high-frequency ripple current in the Boost inductor. Neither the rectifier bridge nor the capacitor across it was included in the simulation model.

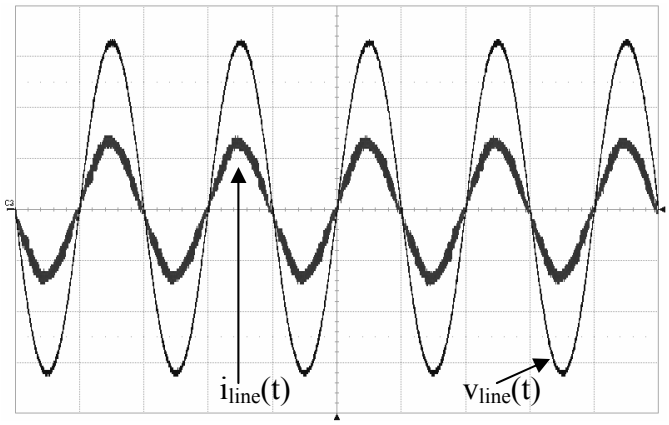

Fig. 14 Measurement of the line current and voltage for V_{in} = 230 V_{RMS} and P_{out} = 200 W (PIC16F877A)

V_{line}: 100V/div, I_{line}: 1A/div

Time scale: 10 ms/div

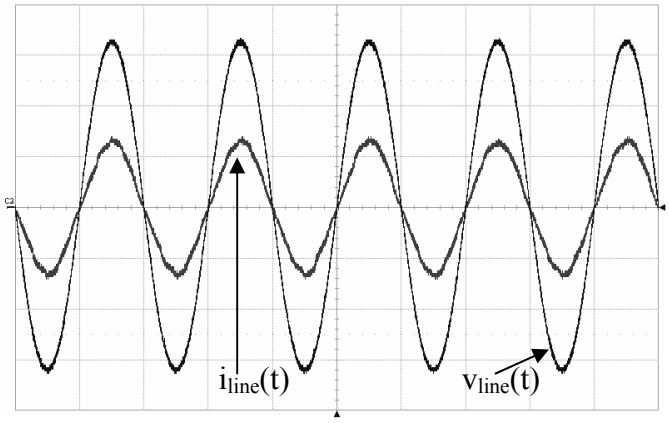

Fig. 15 Measurement of the line current and voltage for V_{in} = 230 V_{RMS} and P_{out} = 1.0 kW (PIC16F877A)

V_{line}: 100V/div, I_{line}: 5A/div

Time scale: 10 ms/div

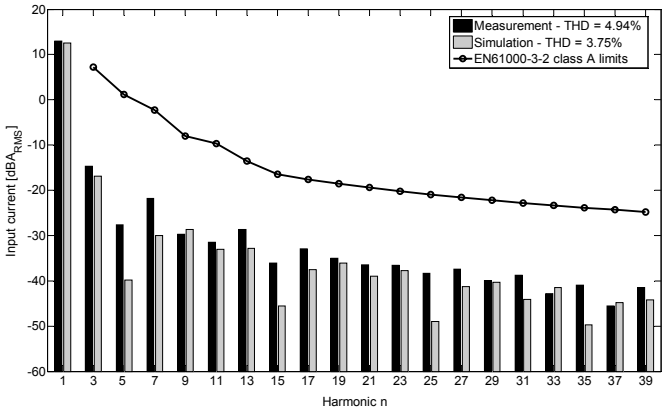

Fig. 16 Harmonic content of the input current – Measurement v. simulation (PIC16F877A)

Fig. 17 shows a measurement of a load step on the output of the PFC. The output power steps between 100W and 1kW and the load is configured as a constant current load. The output voltage falls to 295V during the positive load step and the settling time is approximately 100 ms. Compared to the simulated load step shown in Fig. 18 the transient response of the prototype is not as good as the simulated response. The simulated response has a minimum voltage of 310V and the settling time is 80 ms. The main reason for the difference between simulation and measurement is probably that the actual output capacitance may be smaller than the 330µF used in the simulation. It is also worth noticing that the load step occurs at different points relative to the line current, which will affect the output voltage transient following the load step.

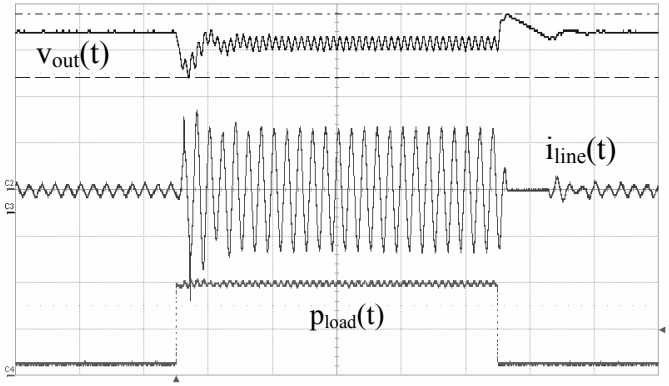

Fig. 17 Measurement of the transient response to a load step between 100 W to 1.0 kW (PIC16F877A)

V_{out}: 100V/div, I_{line}: 5A/div, P_{load}: 500W/div

Time scale: 100ms/div

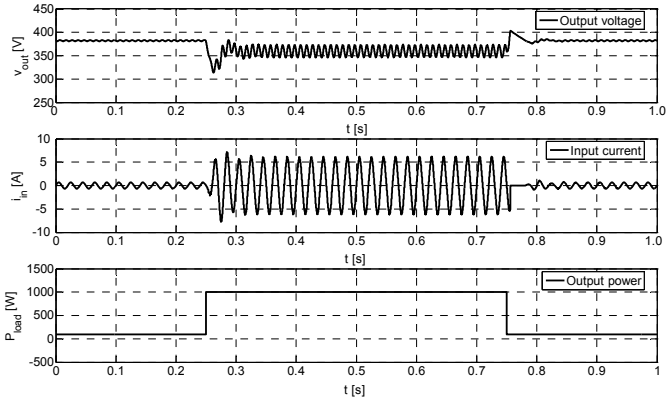

Fig. 18 Simulation of load step between 100W and 1.0kW (PIC16F877A)

B. MEASUREMENTS FOR THE PIC12F683 BASED DESIGN

The prototype for the design based on the PIC12F683 (see picture in Fig. 19) has the same basic circuit configuration as the design based on the PIC16F877A. The only important difference between the prototypes lies in the A/D converter resolution of the output voltage measurement and the software implementation of the digital control loop. The effective A/D converter range on the output voltage measurement is 5 times larger in the PIC12F683 than in the PIC16F877A but the resolution is 10 bit for both designs. The effective A/D converter gain is therefore 5 times smaller in the PIC12F683 and the proportional gain, K_P, needs to be increased by a factor of 5 to achieve the same open loop bandwidth. The proportional gain was 8034 in the lookup table used in the measurements on the PIC16F877A based design. The proportional gain of the PIC12F683 should therefore be 40170 but since the multiplication by K_P is a bit-shifting operation the nearest gain that can be achieved is 32768, which corresponds to shifting the error signal 15 bits to the left. The proportional gain is reduced to approximately $4/5^{th}$ of the optimal gain, which will result in a larger drop in output voltage during positive load steps. The reduced gain will also result in lower input current distortion because the output voltage ripple will be better attenuated by the output voltage control loop.

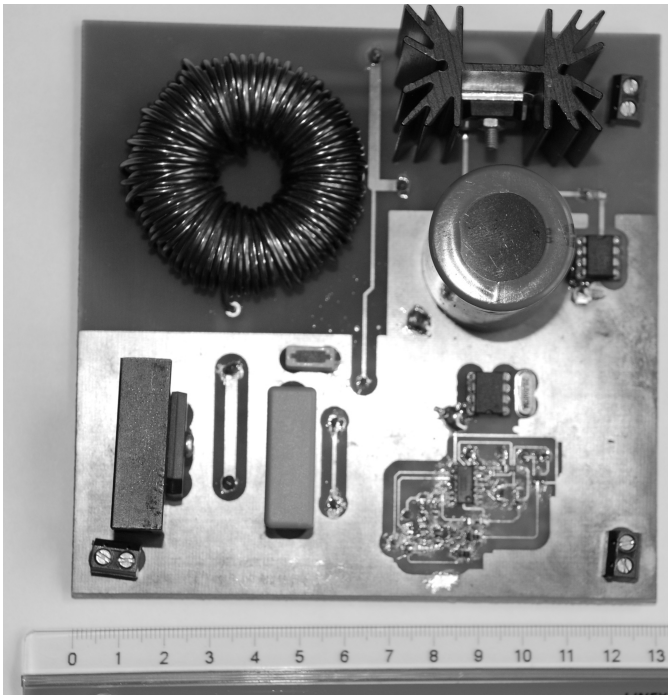

Fig. 19 The prototype for PIC12F683 based design

It is not possible to see any significant difference between the measurements of the input current at 200W and 1kW (see Fig. 20 and Fig. 21) for the PIC12F683 based and measurements for the PIC16F877A based design (see Fig. 14 and Fig. 15). The harmonic content of the input current for two designs (see Fig. 22) shows that there are minor differences in the input current distortion. The PIC12F683 based design has a slightly smaller THD than the PIC16F877A based design. The THD is 4.52% for the PIC12F683 based design and 4.94% for the PIC16F877A based design. It is however more important that both designs meets the EN61000-3-2 class A requirements.

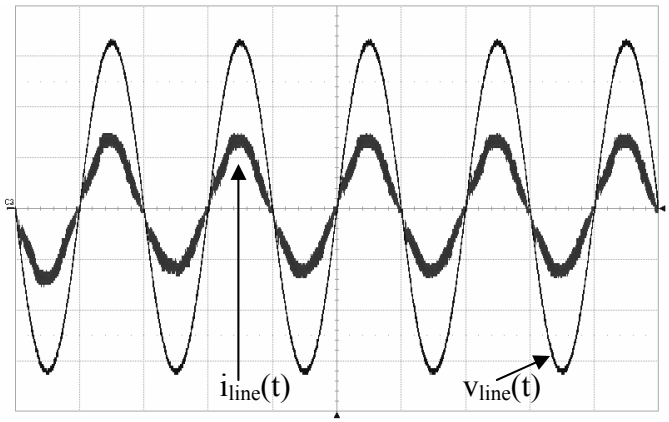

Fig. 20 Measurement of the line current and voltage for V_{in} = 230 V_{RMS} and P_{out} = 200W (PIC12F683)

V_{line}: 100V/div, I_{line}: 1A/div

Time scale: 10 ms/div

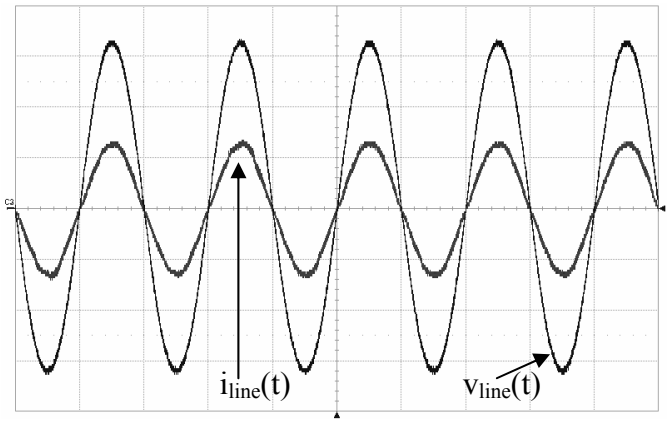

Fig. 21 Measurement of the line current and voltage for V_{in} = 230 V_{RMS} and P_{out} = 1.0kW (PIC12F683)

V_{line}: 100V/div, I_{line}: 5A/div

Time scale: 10 ms/div

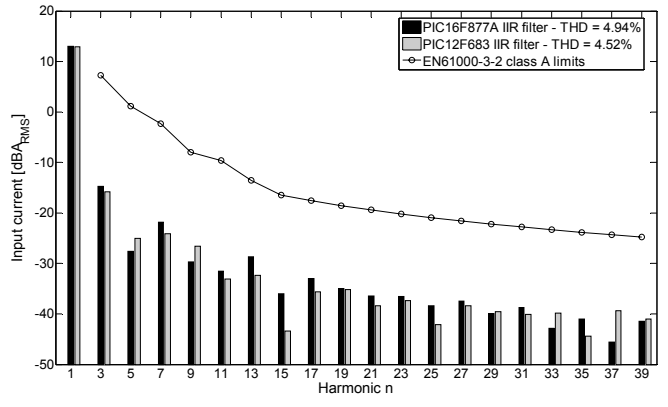

Fig. 22 Measurement of the harmonic content of the input current and the EN61000-3-2 class A limits

Fig. 23 shows a measurement of the transient response to a load step between 100W and 1kW. The transient response of the PIC12F683 based design is very similar to the transient response of the PIC16F877A based design.

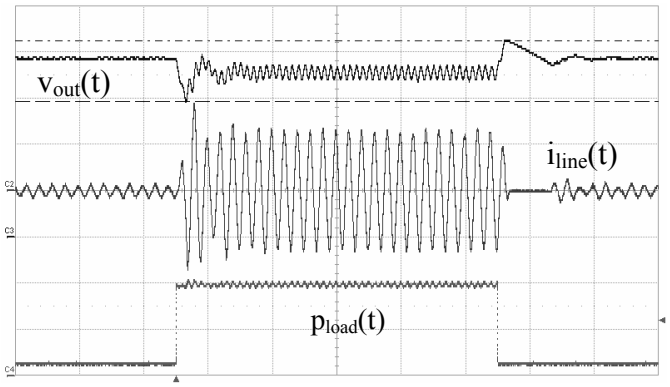

Fig. 23 Measurement of the transient response to a load step between 100 W to 1.0 kW (PIC12F683)

V_{out}: 100V/div, I_{line}: 5A/div, P_{load}: 500W/div

Time scale: 100ms/div

The two designs have very similar performance measured by both input current THD and the transient response to load steps. The main difference between the two designs is therefore price and PCB board area taken up by the control circuit. The EPROM used in the PIC16F877A based design is an almost obsolete component and the design could be improved by using a smaller serial EEPROM and another microcontroller. That does not change the fact that a simplest solution is to avoid the use of a large lookup table when the advantage gained in computational load is very small compared to the capabilities of microcontrollers sold today. Both the designs presented in this paper are based on microcontrollers from Microchip but because of the simplicity of the mixed signal control scheme it is possible to use any microcontroller with two A/D converter inputs and a PWM output.

VIII. CONCLUSIONS

Digital control for a PFC preregulator presents certain advantages over analogue control. Analogue control ICs for an average current mode control scheme includes an analogue hardware multiplier that generates the reference signal for the current control loop. The gain of the analogue hardware varies largely because of temperature and CMOS process variations. There are no variations in the gain in a digital control scheme which makes it possible to design a PFC with better performance with digital control.

In a full digital control scheme with digital current mode control the digital controller device must sample both inductor current and the rectified line voltage every PWM period and calculate the duty cycle for the following PWM period. The digital controller will therefore typically be implemented in a Digital Signal Controller. A microcontroller is not able to perform the required operations in a single PWM period and therefore cannot be used.

A mixed signal control scheme can be implemented in a cheap microcontroller utilizing only a small portion of the resources of the microcontroller. The mixed signal control scheme has an analogue average current mode control loop and a digital voltage control loop which includes input voltage feed-forward. Input voltage feed-forward ensures a good performance of the PFC independent of magnitude of the input RMS voltage.

Two implementations of the digital voltage control loop in two different microcontrollers have been presented. The first implementation uses a PIC16F877A from Microchip and a 512 kbit EPROM as a lookup table. The control scheme utilizes 5% of the computational resources of the PIC16F877A. The second implementation uses the small and cheap PIC12F683 also from Microchip. The second design utilizes 9.1% of the resources of the PIC12F683. The higher utilization is due to the fact that the PIC12F683 has to perform more calculations than the PIC16F877A because it does not have a large lookup table.

Both the implementations of the mixed signal control scheme have been tested on a 1kW PFC preregulator and the performance of the two control schemes was similar. They both meet the

requirements of the EN61000-3-2 class A regulations for input current distortion for electronic devices connected to the utility grid.

The transient response to load steps is comparable to the performance of a typical PFC preregulator. The compensator used in the digital voltage control loop is a proportional compensator. The advantage of the proportional compensator is that it gives a faster transient response than a proportional-integral compensator. The disadvantage of the proportional compensator is that the output voltage is output power dependent. The output voltage of the PFC presented in this paper thus falls from 385V for an output power of 100W to 365V for an output power of 1kW.

The digital compensator implemented in the microcontroller can easily be changed to a proportional-integral compensator if a somewhat higher utilization of the resources of the microcontroller can be accpeted.

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25 Appendix K – Patent application WO2007/098766A

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"Digital Self-Oscillating Modulator"

Patent application WO2007/098766A

Filing date 1 March 2006

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
7 September 2007 (07.09.2007)

PCT

(10) International Publication Number
WO 2007/098766 A1

(51) International Patent Classification:
H03F 3/217 (2006.01) *H03F 1/32* (2006.01)

(21) International Application Number:
PCT/DK2007/000104

(22) International Filing Date: 1 March 2007 (01.03.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
06388014.0 1 March 2006 (01.03.2006) EP
60/780,458 7 March 2006 (07.03.2006) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

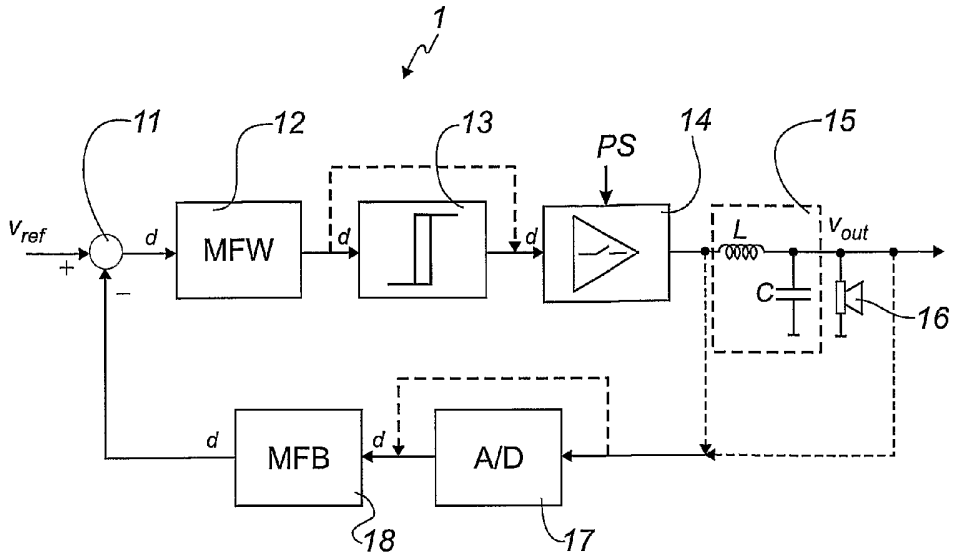
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:
— *of inventorship (Rule 4.17(iv))*

Published:
— *with international search report*
— *with amended claims*

[Continued on next page]

(54) Title: DIGITAL SELF-OSCILLATING MODULATOR



(57) Abstract: A digital self-oscillating modulator (1) having a digital reference signal as input (Vref) comprises a forward loop with a first output and a feedback loop. The feedback loop comprises a feedback block (18) having a transfer function (MFB) and a digital output. The forward loop comprises an alternating output stage (14), and a forward block (12) comprising a filter (12') with a transfer function (MFW) and has a digital output. The digital output from the forward block (12) is input to the alternating stage (14). The forward block (12) is provided with means for calculating the difference between the digi- tal output from the feedback block (18) and the digital reference signal (Vref). The first output is in digital form fed back to the feedback block (18). Provided that the transfer function (MFW) of the forward block (12) is formed by a plurality of integrators, the transfer function (MFB) of the feedback block (18) is not a unity transfer function.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Digital Self-oscillating Modulator

The present invention relates to a digital self-oscillating modulator having a digital reference signal as input and comprising a forward loop with a first output and a feedback loop.

The switching-mode power conversion technology has over the years radically changed the appearance of commercial products, making them far smaller than a few decades ago and leaving the designers with possibilities to experiment with their look and feel without being limited by technology barriers. These benefits are a direct result of the improved efficiency of the power supplies and power amplifiers that use a switching approach instead of a linear one. As a side effect, the amount of heat-sinking material needed is reduced by at least an order of magnitude, which improves the level of integration between the various components, so that the overall board space, weight and volume are significantly reduced and power density is improved. The aforementioned advantages are probably most clearly seen in the switching-mode Class D audio power amplifiers, where the new efficient power conversion principle has opened the doors to some new and challenging application areas, from small low-end portable devices with extended battery life to large high-end audio installations for stage performances with tremendously reduced dimensions.

The achievements in the field of switching-mode audio power amplification in the last few years, described in terms of even higher output power levels and improved audio performance, are drawing this approach on the technology map as one of the most significant breakthroughs that is eventually going to replace linear electronics in most power processing applications. However, this does not mean that the present Class D audio power amplifiers are the only possible solution that fits all applications, and much research is done to take the most advantage from the very high conversion efficiency of the switching-mode approach while still keeping the complexity and component count to a minimum.

These unique challenges, posed predominantly by the audio and video product manufacturers wanting to penetrate the low-end market by cutting production costs and introducing cheap products of satisfactory quality, can be answered by further and closer integration of the constitutive parts of the audio power amplifier, i.e. the switching-mode

power supply and the Class D amplifier, which until now usually have been viewed as separate parts without many touching points.

Several initiatives to improve power conversion systems using a control approach that utilises the self-oscillating principle have been proposed.

DE 198 38 765 discloses a power amplifier employing a hysteresis control for generating pulse width modulated voltages. The difference between the input voltage and the output voltage is integrated in this power amplifier, said difference being stepped down by a factor corresponding to the ratio of the maximum level of the input voltage to the maximum level of the output voltage. The difference between the scaled output signal and the input signal corresponds to the instantaneous amplitude error of the output signal with the result that the integration corresponds to the accumulated error on the output. The output signal of the integrator is triangular, and when the power amplifier is running idle, the slope of said triangle is of the same value for both the positive and the negative flanks. When the power amplifier is to be set, i.e. loaded, these flanks change in such a manner that the positive flank discloses a slope differing from the slope of the negative flank. However, the curve shape remains triangular with straight flanks. As the power amplifier is increasingly loaded, the switch-frequency decreases as well. As a result, for instance the input signal to the power amplifier is sinusoidal, and then the switch-frequency is at maximum at the zero-pass for the sine curve and significantly lower at the maximum and the minimum value, respectively, of said sine curve. When the power amplifier is loaded to its maximum, i.e. when the maximum value of the output voltage is almost identical with the internal DC-voltage of the power amplifier, the switch-frequency becomes very low, almost zero. The triangular signal from the integrator is transferred to a comparator, typically a Schmitt-trigger, which converts the triangular signal into square pulses of a varying pulse width. These square pulses are the switching on signals and the switching off signals, respectively, for the transistors in the power amplifier. These switching on pulses are transferred to the output stage of the power amplifier, viz. to the transistors in the output, and therefore these pulses are upscaled by the relation between said pulse voltages and the internal DC-voltage of the power amplifier. The resulting voltage includes square pulses and is typically of a higher amplitude than the signal voltage. The square voltage is then transmitted to the output filter of the power amplifier, said output filter typically being a second order filter, which is often referred to as a reconstruction filter. The voltage applying after the filter is the output voltage of the power amplifier. The voltage returned to the integrator is the

voltage applying before the output filter. A modulator of this type is often referred to as an Astable Integrating Modulator or an AIM. Such a modulator is encumbered with the problem that the distortions of the output filter have not been taken into account. In addition, the operational amplifier used to construct the integrator has to be of high quality.

WO 02/25357 discloses a controlled oscillation modulator, also called a COM. The COM ensures that the open-loop-phase characteristics involve a phase shift of exactly 180° at the frequency where the open-loop-amplification is 0 dB. The latter is rendered possible by the feedback voltage from the output stage of the power amplifier being forwarded through function blocks causing a phase shift of 180° and/or through function blocks with time delays. The desired phase shift of 180° is obtained by including said phase shift in the function blocks, such as in form of a cascade coupling of poles, and/or by choosing a suitable time delay. When the feedback loop is subsequently closed, the modulator oscillates at the frequency, where the amplification is 0 dB. When the input signal to the power amplifier is 0, the resulting signal is a substantially pure sine. When the input signal differs from 0, the oscillation is superimposed by the input signal. A comparator is subsequently used for generating the switching pulses of the output stage. An increasing loading of the amplifier has the effect that the pure sine resulting from the phase shift of 180° is altered into being something between the pure sine and the triangular voltage known from AIM. The linearity of a modulator depends on variations in the inclination of this signal. As this signal is not a pure triangular curve unlike AIM, but instead something between a sine curve and a triangular curve, the modulator according to the COM principle is nonlinear, and the modulation per se distorts the output signal.

WO 98/19391 describes a way of improving a class D power amplifier. The amplifier includes an internal modulator generating the well-known pulse-width modulated output signal. This signal is transmitted to an output filter, and the resulting filtered signal is the output voltage of the power amplifier. In order to compensate for the distortions of the filter, additional feedback loops have been included, and the characteristics of these feedback loops can compensate for the distortions of said output filter. The described system includes several cascade-coupled feedback loops for compensating the distortions. The system shows an improved procedure structure with respect to power amplifiers without such feedbacks, but the system is per se very complex and requires

much design work in order to achieve the desired effect. A system of this type is often referred to as being Multivariable Enhanced Cascade Controlled or MECC.

WO2004/086629 discloses a pulse width modulator for converting a digital signal into a PWM signal, comprising a plurality of integrators (11) with integrator gains (12) arranged in series, a comparator (17) for comparing the output of the last integrator (11') with a reference, and thereby creating the PWM signal. The modulator further has means (13) for realizing self-oscillation at a desired switching frequency, and a feedback path (14) connected to a point down stream said comparator and leading to a plurality of summing points, each preceding one of said integrators.

WO 04/100356 by the present applicant discloses a switch-mode modulator operating at a two-level voltage and including an alternating output stage, an optional output filter and a feedback including a function block with a transfer function. The modulator furthermore includes a forward block provided with means for calculating the difference between the signal originating from the function block and a reference signal as well as with a transfer function. The output of the forward block is the input of a Schmitt-trigger, which generates switch on signals for changing the output stage. The output voltage of the modulator applying either after the optional output filter or the output stage is fed back through the function block so as to generate the signal fed back. The transfer function of the function block and of the forward block is chosen both in response to the transfer function of the output filter and in response to the desired total open-loop-transfer function of the modulator. The presented modulator is analogue in the sense that the signal input to the modulator is analogue.

US provisional application no. 60/714,077, also by the present applicant, discloses a self-oscillating modulator operating with a two-level output. The modulator comprises an alternating output stage, an optional output filter, a feedback including a function block with a transfer function, a forward block having a transfer function and is provided with means for calculating the difference between the signal originating from said function block and a reference signal. The output voltage of the modulator either from the alternating output stage and/or the output filter is fed back through the function block, and a multiplication element is placed together with the forward block before the alternating output stage. The multiplication element can thus be utilised to change the polarity of the signal sent to the alternating output stage, thereby compensating for the polarity of the power converter, in which the modulator is used.

Self-oscillating modulators represent an interesting alternative to the conventional fixed frequency pulse width modulators (PWM) for all kinds of power converters as found in almost all electronics equipment from audio power amplifiers, converters for renewable energy sources, uninterruptible power supplies to general isolated power converters and power supplies.

The object of the invention is to provide a new and improved digital self-oscillating modulator for all kinds of power converters as found in almost all electronics equipment from audio power amplifiers, converters for renewable energy sources, uninterruptible power supplies to general isolated power converters and power supplies.

This is according to the invention obtained by the feedback loop comprising a feedback block having a transfer function and a digital output, and the forward loop comprising an alternating output stage, and a forward block comprising a filter with a transfer function (MFW) and having a digital output, said digital output from the forward block being input to the alternating stage, said forward block being provided with means for calculating the difference between the digital output from the feedback block and the digital reference signal, with the proviso that the first output in digital form being fed back to the feedback block and wherein provided that the transfer function of the forward block is formed by a plurality of integrators, the transfer function of the feedback block is not a unity transfer function.

By the term self-oscillating is meant a modulator, in which the phase shift of the open-loop transfer function is 360 degrees at the oscillation frequency of the modulator. In analogue self-oscillating modulators, the bandwidth of the modulator is limited by the switching frequency of the output stage, and in digital modulator with fixed frequency pulse width modulation, the bandwidth is limited by the sampling frequency, which is smaller than or equal to the switching frequency. In the proposed digital self-oscillating modulator, the sampling frequency is not limited by a fixed switching frequency. Thereby, the bandwidth is comparable to that of an analogue self-oscillating modulator, but the bandwidth is increased compared to conventional digital modulators. Thus, the digital self-oscillating modulator as such overcomes the Nyquist criteria imposed by the switching frequency. Additionally, an increased loop gain can be achieved. In general, the digital implementation of the self-oscillating modulator makes it possible to achieve a better performance by providing a simple modulator structure with internally created

carrier, high bandwidth equal to the switching frequency, high power supply rejection ratio through intrinsic power supply voltage feedback within the modulator, as well as reduced electromagnetic interference through spread spectrum techniques in variable switching frequency mode. By unity transfer function is meant a non-frequency compensating transfer function, which normally is obtained by a direct feedback via a conductor, and possibly with a gain from an amplifier.

Provided that the transfer function of the forward block (12) is formed by a plurality of integrators, the transfer feedback is not transferred to a plurality of summing points, each preceding one of the integrators.

Provided that the transfer function of the feedback block is a unity transfer function, the transfer function of the forward block is not formed by a plurality of integrators.

According to a first preferred embodiment, the modulator additionally comprises an output filter, wherein said first output is the output from the alternating stage, said first output both being fed to the feedback block and the output filter. According to a second preferred embodiment, the forward loop additionally comprises an output filter, which as input has the output from the alternating stage and as output has said first output. According to a third preferred embodiment, the modulator additionally comprises an output filter, wherein both the output from the alternating stage and the output filter in digital form are fed to the feedback block. Including the output filter within the modulator feedback makes it possible to increase open load stability.

According to a particular embodiment of the modulator, the transfer function of the forward block and/or the transfer function of the feedback block are frequency compensating, i.e. the transfer function has one or more poles or zero points. The transfer functions are preferably transfer functions of digital filters.

According to an embodiment of the modulator, the forward block includes a comparator block. Preferably the forward block includes a comparator with hysteresis, or alternatively a comparator block and a hysteresis block. Hereby modulators with a higher basic linearity and thus lower distortion are obtained.

According to a particular embodiment of the modulator, the comparator block includes a multiplexer and a digital comparator, said multiplexer being adapted to multiplex sig-

nals from the positive and negative sides of the hysteresis block, the output from the multiplexer being sent to the digital comparator, which compares the output from the multiplexer with a digital reference signal. This reference signal can for instance be the output from a filter of the forward block. Hereby it is achieved that the output of the comparator will change according to variations in the reference signal.

In another embodiment of the modulator, the comparator block includes a digital comparator and an S-R latch. Thereby a particular simple implementation of the comparator block is introduced.

According to a particular embodiment of the modulator, the feedback loop additionally comprises an A/D-converter. If the signal fed back is analogue, which will for instance often be the case, if the output from the output filter is fed back, this signal must be converted to a digital signal, which is processed by the feedback block. The A/D-converter thus produces the digital form of said first output signal.

In another embodiment of the modulator according to the invention, the forward block includes an integrator. Hereby a very easy and simple implementation as well as a very high DC- and low-frequency loop gain is obtained.

According to a preferred embodiment of the modulator, the integrator comprises an adder and a clocked latch. This provides a particularly simple digital implementation of the integrator.

According to another preferred embodiment of the digital modulator according to the invention, the transfer function of the forward block, the transfer function of the filter of the feedback block, as well as the transfer function of the optional output filter depend on the desired open-loop transfer function. Thereby, for instance the transfer function of the forward block can be chosen to compensate the error signal (difference between the signal fed back and the reference signal) in an optimised way dependent of the specific modulator, and the transfer function of the output filter can be optimised to reconstruct the signal. The transfer function of the feedback block can in turn be determined from the desired open-loop transfer function.

In a preferred embodiment, the alternating output stage is a switching amplifier with bidirectional switches.

According to a particular embodiment, the means for comparing the signal fed back with the reference signal comprises of two identical digital comparator sections, which have inverted inputs.

In another embodiment according to the invention, a digital multiplication element is placed together with the forward block before the alternating output stage. The multiplication element can thus be utilised to change the digital polarity of the signal sent to the alternating output stage, thereby compensating for the polarity of for instance the power converter, in which the modulator is used.

In a preferred embodiment according to the invention, the alternating output stage is supplied with an AC-voltage from an AC-link converter and the digital multiplication element works by switching between the two identical digital comparator sections with inverted inputs, said switching being controlled by the sign of the AC-voltage from the AC-link converter. Thereby a particular simple implementation of a polarity compensating modulator is achieved.

In a preferred embodiment according to the invention, one or more of the zero points or poles of the feedback block and of the forward block are coinciding or approximately coinciding with the pole or zero points of the optional output filter.

In yet another embodiment according to the invention, the modulator further includes one or more additional output filters, one or more additional feedbacks with transfer functions coupled either after the output stage, after the output filter or after one or more of the additional output filters, as well as one or more forward blocks, which include both means for calculating the difference between one of the signals fed back from the additional function blocks and a reference signal, as well as a transfer function. Thereby even further loops to stabilise the modulator and compensate for error signals have been provided.

Preferably, the transfer function of the function block, the transfer function of the forward block, the additional output filters, the transfer functions of the additional feedback blocks and the transfer function of the additional forward blocks together are generating the desired total transfer function.

In a particularly preferred embodiment of the self-oscillating modulator, the desired total transfer function is similar to a first order low-pass-characteristic or integrator characteristic.

The purpose of the invention is also achieved by a synchronised modulator comprising two of the afore-mentioned digital modulators, wherein a reference voltage is input to a first digital modulator and a digital inverted reference voltage is input to a second digital modulator, the outputs from said first and said second digital modulator being synchronised by use of a synchronisation block.

The invention is now to be described in greater detail with reference to the drawings, in which

Fig. 1 shows a block diagram of a digital self-oscillating modulator (DISOM) according to the invention,

Fig. 2 a block diagram of a DISOM according to the invention with an additional outer control loop,

Figs. 3-7 different embodiments of DISOMs comprising comparators with hysteresis,

Figs. 8-14 different embodiments of GLIM type 1 DISOM modulators,

Figs. 15-21 different embodiments of GLIM type 2 DISOM modulators,

Figs. 22-24 different embodiments of hysteresis modulators with substantially constant switching frequency,

Figs. 25-31 different embodiments of phase shift types of DISOM modulators,

Figs. 32-42 different embodiments of hysteresis comparators for use in DISOMs,

Fig. 43 a block diagram of a prototype for proofing the DISOM concept,

Fig. 44 a plot of the switching frequency as a function of the duty cycle of a prototype for proofing the DISOM concept,

Fig. 45 a DC/DC converter implementing a DISOM,

Fig. 46 and 47 plots of experimental results measured on the prototype,

Fig. 48 a synchronised modulator comprising two DISOMs,

Fig. 49 a digital implementation of a SICAM type DISOM modulator,

Fig. 50 a digital comparator with hysteresis and synchronisation input, and

Fig. 51 a DISOM modulator type 1.1 with variable hysteresis window.

A block diagram of a digital self-oscillating modulator (DISOM) according to the invention is shown in Fig. 1. The structure is very general and can as such include digital versions of any of the conventional analogue self-oscillating modulators found in the power converters or switching audio power amplifiers with DC-link or HF-link power supplies.

The digital error signal from a summing junction 11 is fed to a modulator feed forward block 12 comprising a filter 12' having a transfer function MFW. The feed forward block 12 will optionally include a hysteresis block 13 or a comparator with hysteresis as well as other optional components, which will later be explained. The digital output from the forward block 12 is then fed to the switching amplifier 14, which is supplied with the voltage from a power supply PS. The output from the switching stage or the switching amplifier 14 can optionally be passed through an output filter 15 and to the load 16, which can be a loudspeaker or a general load for a power converter. The output from the switching stage or the switching amplifier 14 can be regarded as either analogue or digital depending on the particular implementation of the switching stage or the switching amplifier 14, which according to a preferred embodiment is a switching power stage.

The output filter 15 is here depicted as a second order low-pass filter with passive LC components, said low-pass filter 15 for instance reconstructing a sinusoidal signal or input signal V_{ref} from the square voltage from the switching stage or the switching amplifier 14. However, the output filter 15 can have any desired frequency compensating

transfer function. The output from either the switching stage or the switching amplifier 14 or the output filter 15 is fed back through the modulator feedback block 18 having a transfer function MFB. The input to the feedback block 18 must be digital. Therefore, the feedback loop can optionally include an A/D-converter 17, which converts an analogue signal to a digital signal. The A/D-converter 17 is thus necessary, if the signal fed back from the switching stage or the switching amplifier 14 and/or the output filter 15 is analogue.

The digital output from the feedback block 18 is fed back to a summing junction 11, which extracts the error signal as the difference between the digital signal fed back and a digital reference signal V_{ref}.

The transfer functions of the feed forward block 12, the feedback block 18 and the output filter 15 can have any desired frequency dependency. The filters can inter alia be high-pass filters, low-pass filters, band-pass filters, band-stop filters or unity filters based on the desired frequency compensation of the particular self-oscillating modulator and the open loop transfer function. According to a preferred embodiment the transfer function MFW of the forward block 12 and/or the transfer function MFB of the feedback block 18 have a frequency compensating effect, i.e. one or more poles or zeros.

The digital self-oscillating modulator 1 according to the invention can have one or more outer control loops, which improve the performance of the modulator 1 even further by introducing additional gain and optimising bandwidth within a control feed forward block 20 with a transfer function CFW and a control feedback block 22 with a transfer function CFB as shown in Fig. 2. In the depicted block diagram, the difference between the signal fed back through the control feedback block 22 and the reference signal V_{ref} is extracted at an additional summing junction 19. Since the output from the DISOM 1 is typically an analogue signal, the additional feedback loop can optionally include an additional A/D-converter 21.

Figs. 3-7 show different embodiments of DISOMs, which include a comparator with hysteresis in the forward block 12. Fig. 3 shows a first embodiment of a DISOM version of a band-pass current control type. This embodiment will typically be combined with an outer control loop (not shown). The illustrations of these transfer functions correspond to Bode plots, which are well known to a person skilled in the art. Fig. 4 shows a second embodiment of a DISOM version of a band-pass current control type. The

current measurement is here replaced with a current estimation, for instance by directly coupling the voltage over the inductor of the LC output filter, by measuring the potential of a winding of the inductor of the output filter or via a transformer. Fig. 5 shows a third embodiment, which corresponds to the embodiment shown in Fig. 4, but where the output from the amplifier stage can be regarded as a digital signal. The fourth embodiment shown in Fig. 6 corresponds to the embodiment shown in Fig. 5 combined with an outer control loop. A fifth embodiment is shown in Fig. 7. This embodiment has a current estimation by use of the voltage at the output. The embodiment does not have an output filter and can for instance be used to drive a speaker directly, also called an active transducer (ACT) or a pulse-modulated transducer (PMT). This embodiment does not need the A/D-converter and can thus be implemented cheaply.

Fig. 8 shows a general block diagram of a digital version of the GLIM type 1 modulators (see also WO 04/100356), and Figs. 9-14 show different embodiments of this type of modulator. To the right in each of the figures, the y-to-x or open loop functions of the different embodiments are shown. This type of digital GLIM has a first order low-pass characteristic for the open loop transfer function. The A/D-converter can be neglected, since both the output from the hysteresis comparator, which optionally can be fed back to the feedback block, and the output from the switching stage or the switching amplifier are digital. The embodiment shown in Fig. 9 corresponds to the AIM-implementation (see also DE 198 38 765). All the GLIM type 1 embodiments are simple and cheap to implement. The embodiments can be part of a power modulator with an output filter and an outer control loop as shown in Fig. 14.

Fig. 15 shows a general block diagram of a digital version of the GLIM type 2 modulators (see also WO 04/100356), and Figs. 16-21 show different embodiments of this type of modulator. This type of digital GLIM also has a first order low-pass characteristic for the open loop transfer function. The A/D-converter must be used in this type of modulator, since the output from the output filter is analogue. Thus, the GLIM type 2 modulators are more expensive to implement, since a fast A/D-converter is necessary. As with the type 1 modulators, these embodiments can be part of a power modulator with an output filter and an outer control loop as shown in Fig. 21. In order to lower expenses, the same A/D-converter can be used for both the inner feedback loop and the outer control loop.

Figs. 22-24 show different embodiments of modulators with a substantially constant switching frequency, all of them being current mode types of hysteresis modulators. Fig. 22 shows a DISOM version of an AIM modulator with a variable hysteresis window, which is carried out in order to achieve a constant switching frequency. This embodiment is very simple to implement, since the input of the hysteresis window of the digital hysteresis comparator shown can be used directly without the use of an A/D-converter, since the signal is digital. Fig. 23 shows a similar embodiment, which incorporates a digital multiplicator, which makes the implementation slightly more complicated and expensive. Fig. 24 shows another embodiment, in which a digital comparator is used for comparing the signal fed back of the power converter output current and the reference signal and thus forms the summing junction 11. This embodiment must include an A/D-converter in the feedback loop.

Figs. 25-31 show different embodiments of phase shift types of modulators, which use a digital power stage without hysteresis, i.e. the hysteresis window is equal to zero. Fig. 25 shows a DISOM version of the COM implementation (see also WO 98/19391). The A/D-converter can be neglected since the output from the switching stage or the switching amplifier is digital. However, an A/D-converter can be used to compensate for errors of the power stage. Fig. 26 shows a similar COM-type power modulator with an output filter and an outer control loop. The outer loop must include an A/D-converter. Fig. 27 shows a DISOM version of a GCOM (see also WO 2004/047286). The A/D-converter must be of a fast type. Fig. 28 shows a similar GCOM-type power modulator with an outer control loop. A single A/D-converter can be used for both the inner feedback loop and the outer control loop. Fig. 29 shows a DISOM version of a CCOM (see also WO 02/25357). The embodiment uses a current measurement at the output of the switching stage or the switching amplifier, and the feedback loop must include a fast A/D-converter. Fig. 30 shows a similar CCOM-type modulator with an outer control loop, which must include a separate A/D-converter. Fig. 31 shows yet another embodiment of the phase-shift type modulator.

Figs. 32-42 show different embodiments of hysteresis comparators for use in DISOMs. In the figures X, "in", and "input" denote the signal from for instance the summing junction or from a filter of the forward block, V_a and V_b are the signals from the positive and negative sides of the hysteresis windows, respectively, V_b usually being a negative number. The embodiment shown in Fig. 32 incorporates a 2-1 multiplexer and a digital comparator, both of which are well known to a person skilled in the art. A and B denote

the input from the positive and negative side of the hysteresis window, respectively, where $A = K*V_a$ and $B = K*V_b$, where K is an arbitrary constant. The digital comparator compares the input X and the output Y from the 2-1 multiplexer. The output of the digital comparator is fed back to the SEL terminal of the 2-1 multiplexer. A and B are input to the 2-1 multiplexer, and the output of the 2-1 multiplexer is either A or B depending on the state of SEL. Fig. 33 shows a similar embodiment, but where the reference point of the input is shifted (with the value B).

Fig. 34 shows yet another embodiment, which incorporates two digital comparators, and an S-R latch, the functions of which all are well known to a person skilled in the art. Fig. 35 is substantially the same embodiment as shown in Fig. 34. The hysteresis window HW input to the digital comparator is the difference between A and B. Fig. 36 shows a simplified embodiment with only one comparator.

Fig. 37 shows a digital power hysteresis comparator including a digital comparator with a hysteresis comparator output (HC Output), which is input to a power stage, the output of which is fed to a feedback loop comprising an A/D-converter and a constant gain K. This embodiment compensates for the voltage drop in the transistors of the power stage. Fig. 38 shows an alternative embodiment of a digital power hysteresis comparator, which includes a 2-1 multiplexer in the feedback loop. As long as the output from the power stage is fed to the SEL terminal of the 2-1 multiplexer, this embodiment functions identical to the embodiment shown in Fig. 37, where both timing errors and voltage supply errors of the power stage are compensated. If the output from the hysteresis comparator (HC Output) is fed to SEL, no compensations are carried out. Figs. 39-41 show similar embodiments. The hysteresis window in Fig. 41 is constant. Fig. 42 shows yet another implementation, where Z_1 is a constant and Z_2 is the hysteresis window, which can be constant or externally controlled.

Fig. 49 shows a digital implementation of a SICAM modulator (see also US provisional application 60/714,077). The input (in) is fed to two identical digital comparators, which compare the input with the signal fed back through the feedback loop. The outputs from the two digital comparators are digitally inverted. The outputs are fed to a 2-1 multiplexer, the output of which is determined by the state of SEL. The output from the 2-1 multiplexer is fed to the alternating output stage, which preferably comprises a switching amplifier with bidirectional switches. The alternating output stage is supplied with an AC-voltage from an HF-link converter, the AC-voltage also being fed to the SEL. The

polarity of the HF-link converter thereby determines the output from the 2-1 multiplexer. The digital output from the alternating output stage is fed back through the feedback loop comprising an A/D-converter and a feedback block with gain K. The transfer functions of the feedback block and forward block can of course be any desired function. The SICAM modulator can also contain an output filter and/or one or more additional feedback loops.

An offline DC/DC converter has been constructed in order to carry out a proof-of-concept of the DISOM concept. A block diagram of the main modulator is shown in Fig. 43. The shown embodiment is one of the simplest forms of a DISOM modulator. The main modulator is digital and has been implemented in a Complex Programmable Logic Device (CPLD). An input REF from an external controller is fed to a summing junction 31, which is also fed by the signal from the feedback loop. The summing junction 31 extracts the difference between these two signals. The output from the summing junction 31 is sent to a latch 32, which also receives a latch enable signal LE. The output from the latch 32 is sent to an integrator 40, which consists of an adder 33 and a clocked latch 34, the output of the clocked latch 34 being fed back to the adder 33. The output of the integrator 40 is sent to a comparator 45 with hysteresis. The comparator 45 comprises two separate comparators 35, 36 and an S-R latch 37. The output from the integrator is fed to both comparators 35, 36, one comparator 35 comparing the signal to the signal from the hysteresis window HW and the other comparator 36 comparing the signal to zero. The output from the two comparators 35, 36 are fed to the R and S terminals of the S-R latch 37, respectively. The output from the S-R latch 37 is fed back to a multiplexer 38, which sets the output to zero if the input is zero and the output to 2^n if the input is one. The output of the multiplexer 38 is fed back to the summing junction 31.

The switching frequency f_{sw} of the main modulator is given as a function of the duty cycle of the modulator output given by the following expression:

$$f_{sw} = \frac{2^n}{T_{clock} \cdot HW} \cdot D \cdot (1-D),$$

where f_{sw} is the switching frequency, n is number of bits of the reference input REF, T_{clock} is the period of time for the clocked latch, HW is the hysteresis window, and D is the duty cycle. A plot of the switching frequency f_{sw} versus the duty cycle D is shown in Fig. 44 for n = 8, T_{clock} = 50 ns and HW = 15360.

The overall control loop including the DC/DC converter is shown in Fig. 45. The CFB block 22 is not included in the feedback loop, since the CFB block simply has a gain of one in the shown embodiment. The CFW block has a transfer function with three zeros and an integrator. The placement of the three zeros determines the overall transfer function of the DC/DC converter.

Some experimental results measured on the prototype are shown in fig. 46 and 47. The output voltage is 12V and the load current is 10A in Fig. 46. The lower trace 42 shows the gate signal for the two MOSFETs in the offline converter and the upper trace 41 shows the output voltage. The switching frequency is approximately 80 kHz. The output voltage is 9V and the load current is 10A in Fig. 47. The duty cycle of the MOSFET gate signal has been decreased and the switching frequency has fallen to 59 KHz. The lower trace 77 shows the gate signal for the two MOSFETs in the offline converter and the upper trace 76 shows the output voltage. The measurements shown in Fig. 46 and 47 correspond well with the theoretical curve shown in Fig. 44, which shows that the switching frequency is decreased by a decrease in duty cycle.

Fig. 48 shows a block diagram of a DISOM version for synchronising two modulators. The DISOM+ 51 and DISOM- 52 can be any type of DISOM modulator, for instance of the phase shift type or the hysteresis type. The reference signal X_{in} is fed to DISOM+ 51 and a digital inverter 54, which inverts the reference signal and feeds it to DISOM- 52. The two modulators 51, 52 are synchronised by the synchronisation block 53. There are several ways to implement the synchronisation, for instance by an optional external synchronisation signal ES, via the capacitors of the output filter, by summing part of the high frequency part of the carrier waves, by summing parts of the hysteresis window, or by master/slave control.

There are two methods for making the DISOM modulator operate with a fixed switching frequency. One is to synchronise the switching output to a signal as shown in Fig. 50. Synchronisation is achieved by using a clocked D flip-flop in the comparator instead of an S-R latch as in the comparator with hysteresis (see Fig. 36). The clock input CLK of the D flip-flop is connected to the Sync. input and the data input D is permanently connected to logic '1'. Whenever the Sync. input transitions from logic '0' to logic '1', i.e. from low to high, the comparator output will be forced to logic '1'. The hysteresis comparator output will be reset to logic '0', when the comparator input (Input) becomes lar-

ger than the hysteresis window. Thus the positive transition of the switching output has been synchronised to the positive transition of the Sync. input.

The second method for making a DISOM modulator operate with a fixed switching frequency is to change the hysteresis window according to the modulation index/duty cycle of the switching output. An example of how this can be achieved is shown in Fig. 51**Fejl! Henvisningskilde ikke fundet.**, which gives a more detailed explanation of the embodiment shown in Fig. 22. A hysteresis window calculator block HWC calculates the hysteresis window size based on the input to the DISOM modulator and sets the hysteresis window. The HWC can be implemented as either a mathematical function that actively calculates the hysteresis window or as a lookup table, where the hysteresis window values have been precalculated and stored.

The following expression gives an example of the mathematical expression for the hysteresis window HW as a function of duty cycle D and switching frequency f_{sw} for the modulator shown in Fig. 51.

$$HW = \frac{2^n}{T_{clock} \cdot f_{sw}} \cdot D \cdot (1 - D)$$

An optional digital lowpass filter can be inserted between the hysteresis window calculator HCW and the modulator input to avoid large changes in the switching frequency during transient conditions.

The above description of the invention reveals that it is obvious that it can be varied in many ways. Such variations are not to be considered a deviation from the scope of the invention, and all modifications, which are obvious to persons skilled in the art, are also to be considered comprised by the scope of the succeeding claims.

Claims

1. A digital self-oscillating modulator (1) having a digital reference signal as input (Vref) and comprising a forward loop with a first output and a feedback loop, wherein
- the feedback loop comprises a feedback block (18) having a transfer function (MFB) and a digital output, and
- the forward loop comprises an alternating output stage (14), and a forward block (12) comprising a filter (12') with a transfer function (MFW) and having a digital output, said digital output from the forward block (12) being input to the alternating stage (14), said forward block (12) being provided with means for calculating the difference between the digital output from the feedback block (18) and the digital reference signal (Vref), and wherein
- the first output in digital form being fed back to the feedback block (18), and
- with the proviso that the transfer function (MFW) of the forward block (12) is formed by a plurality of integrators, the transfer function (MFB) of the feedback block (18) is not a unity transfer function.

2. A digital self-oscillating modulator (1) according to claim 1, wherein the modulator additionally comprises an output filter, and wherein said first output is the output from the alternating stage (14), said first output both being fed to the feedback block (18) and the output filter (15).

3. A digital self-oscillating modulator according to claim 1, wherein the forward loop additionally comprises an output filter (15), which as input has the output from the alternating stage (14) and as output has said first output.

4. A digital self-oscillating modulator according to claim 1, wherein modulator additionally comprises an output filter, and wherein both the output from the alternating stage (14) and the output filter (15) in digital form are fed to the feedback block (18).

5. A digital self-oscillating modulator according to claim any of the preceding claims, wherein the transfer function for the filter of the forward block (12) and/or transfer function of the feedback block (18) are frequency compensating.

6. A digital self-oscillating modulator (1) according to any of the preceding claims, **characterised in that** the forward block (12) includes a comparator block.

7. A digital self-oscillating modulator according to any of the preceding claims, wherein the forward block (12) includes a comparator (13) with hysteresis or a comparator block and a hysteresis block.

8. A digital self-oscillating modulator according to claim 6 and 7, wherein the comparator block includes a multiplexer and a digital comparator, said multiplexer being adapted to multiplex signals from the positive and negative sides of the hysteresis block, the output from the multiplexer being sent to the digital comparator, which compares the output from the multiplexer with a digital reference signal.

9. A digital self-oscillating modulator according to one of claims 6-8, wherein the comparator block includes a digital comparator and an S-R latch.

10. A digital self-oscillating modulator according to any of claims 6-8, wherein the comparator block includes a flip-flop.

11. A digital self-oscillating modulator according to any of claims 6-8, further comprising a hysteresis window calculator for calculating a hysteresis window.

12. A digital self-oscillating modulator according to claim 11, wherein the hysteresis window calculator is implemented using calculation means for actively calculating the hysteresis window or as a lookup table.

13. A digital self-oscillating modulator according to any of the preceding claims, wherein the feedback loop additionally comprises an A/D-converter (17).

14. A digital self-oscillating modulator (1) according to any of the preceding claims, wherein the forward block (12) includes an integrator.

15. A digital self-oscillating modulator (1) according to claim 14, wherein the integrator comprises an adder and a clocked latch.

16. A digital self-oscillating modulator (1) according to any of the preceding claims, wherein the transfer function (MFW) of the filter (12') of the forward block (12), the

transfer function (MFB) of the feedback block (18), as well as the transfer function of the optional output filter (15) depend on the desired open-loop transfer function.

17. A digital self-oscillating modulator (1) according to any of the preceding claims, wherein the alternating output stage (14) is a switching amplifier with bidirectional switches.

18. A digital self-oscillating modulator (1) according to any of the preceding claims, wherein the means for comparing the signal fed back with the reference signal comprises two identical digital comparator sections, which have inverted inputs.

19. A digital self-oscillating modulator (1) according to any of the preceding claims, wherein a digital multiplication element is placed together with the forward block before the alternating output stage.

20. A digital self-oscillating modulator (1) according to claims 18 and 19, wherein the alternating output stage (14) is supplied with an AC-voltage from an AC-link converter and that the digital multiplication element works by switching between the two identical digital comparator sections with inverted inputs, said switching being controlled by the sign of the AC-voltage from the AC-link converter.

21. A digital self-oscillating modulator (1) according to any of the preceding claims, wherein one or more of the zero points or poles of the feedback block (18) and of the forward block (12) are coinciding or approximately coinciding with the pole or zero points of the optional output filter (15).

22. A digital self-oscillating modulator (1) according to any of the preceding claims, further including one or more additional output filters, one or more additional feedbacks (22) with transfer functions (CFB) coupled either after the output stage, after the output filter or after one or more of the additional output filters, as well as one or more forward blocks (20), which include both means for calculating the difference between one of the signals fed back from the additional function blocks and a reference signal, as well as a transfer function (CFW).

23. A digital self-oscillating modulator (1) according to claim 22, characterised by the transfer function (MFB) of the feedback block (18), the transfer function (MFW) of

the forward block (12), the additional output filters, the transfer functions (CFB) of the additional feedback blocks (22) and the transfer function (CFW) of the additional forward blocks (20) together generating the desired total transfer function.

24. A digital self-oscillating modulator according to one of the preceding claims, wherein the desired total transfer function is identical to or similar to a first order low-pass-characteristic or integrator characteristic.

25. A synchronised modulator comprising two digital modulators (51, 52) according to any of the preceding claims, wherein a reference voltage ($X_{in,pos}$) is input to a first digital modulator (51) and a digital inverted reference voltage ($X_{in,neg}$) is input to a second digital modulator (52), the outputs from said first and said second digital modulator being synchronised by use of a synchronisation block.

AMENDED CLAIMS
[Received by the International Bureau on 12 July 2007 (12.07.2007)]

Claims

1. A digital self-oscillating modulator (1) having a digital reference signal as input (Vref) and comprising a forward loop with a first output and a feedback loop, wherein
- the feedback loop comprises a feedback block (18) having a transfer function (MFB) and a digital output, and
- the forward loop comprises an alternating output stage (14), and a forward block (12) comprising a filter (12') with a transfer function (MFW) and having a digital output, said digital output from the forward block (12) being input to the alternating stage (14), said forward block (12) being provided with means for calculating the difference between the digital output from the feedback block (18) and the digital reference signal (Vref), and wherein
- the first output being fed in digital form back to the feedback block (18), and wherein
- provided that the transfer function (MFW) of the forward block (12) is formed by a plurality of integrators, the transfer function (MFB) of the feedback block (18) is not a unity transfer function.

2. A digital self-oscillating modulator (1) according to claim 1, wherein the modulator additionally comprises an output filter, and wherein said first output is the output from the alternating stage (14), said first output both being fed to the feedback block (18) and the output filter (15).

3. A digital self-oscillating modulator according to claim 1, wherein the forward loop additionally comprises an output filter (15), which as input has the output from the alternating stage (14) and as output has said first output.

4. A digital self-oscillating modulator according to claim 1, wherein modulator additionally comprises an output filter, and wherein both the output from the alternating stage (14) and the output filter (15) in digital form are fed to the feedback block (18).

5. A digital self-oscillating modulator according to claim any of the preceding claims, wherein the transfer function for the filter of the forward block (12) and/or transfer function of the feedback block (18) are frequency compensating.

6. A digital self-oscillating modulator (1) according to any of the preceding claims, **characterised in that** the forward block (12) includes a comparator block for calculating the difference between the digital output from the feedback block (18) and the digital reference signal (Vref).

7. A digital self-oscillating modulator according to any of the preceding claims, wherein the forward block (12) includes a comparator (13) with hysteresis or a comparator block and a hysteresis block.

8. A digital self-oscillating modulator according to claim 6 and 7, wherein the comparator block includes a multiplexer and a digital comparator, said multiplexer being adapted to multiplex signals from the positive and negative sides of the hysteresis block, the output from the multiplexer being sent to the digital comparator, which compares the output from the multiplexer with a digital reference signal.

9. A digital self-oscillating modulator according to one of claims 6-8, wherein the comparator block includes a digital comparator and an S-R latch.

10. A digital self-oscillating modulator according to any of claims 6-8, wherein the comparator block includes a flip-flop.

11. A digital self-oscillating modulator according to any of claims 6-8, further comprising a hysteresis window calculator for calculating a hysteresis window.

12. A digital self-oscillating modulator according to claim 11, wherein the hysteresis window calculator is implemented using calculation means for actively calculating the hysteresis window or as a lookup table.

13. A digital self-oscillating modulator according to any of the preceding claims, wherein the feedback loop additionally comprises an A/D-converter (17).

14. A digital self-oscillating modulator (1) according to any of the preceding claims, wherein the forward block (12) includes an integrator.

15. A digital self-oscillating modulator (1) according to claim 14, wherein the integrator comprises an adder and a clocked latch.

16. A digital self-oscillating modulator (1) according to any of the preceding claims, wherein the transfer function (MFW) of the filter (12') of the forward block (12), the transfer function (MFB) of the feedback block (18), as well as the transfer function of the optional output filter (15) depend on the desired open-loop transfer function.

17. A digital self-oscillating modulator (1) according to any of the preceding claims, wherein the alternating output stage (14) is a switching amplifier with bidirectional switches.

18. A digital self-oscillating modulator (1) according to any of the preceding claims, wherein the means for calculating the difference between the signal fed back and the reference signal comprises two identical digital comparator sections, which have inverted inputs.

19. A digital self-oscillating modulator (1) according to any of the preceding claims, wherein a digital multiplication element is placed together with the forward block before the alternating output stage.

20. A digital self-oscillating modulator (1) according to claims 18 and 19, wherein the alternating output stage (14) is supplied with an AC-voltage from an AC-link converter and that the digital multiplication element works by switching between the two identical digital comparator sections with inverted inputs, said switching being controlled by the sign of the AC-voltage from the AC-link converter.

21. A digital self-oscillating modulator (1) according to any of the preceding claims, wherein one or more of the zero points or poles of the feedback block (18) and of the forward block (12) are coinciding or approximately coinciding with pole or zero points of the optional output filter (15).

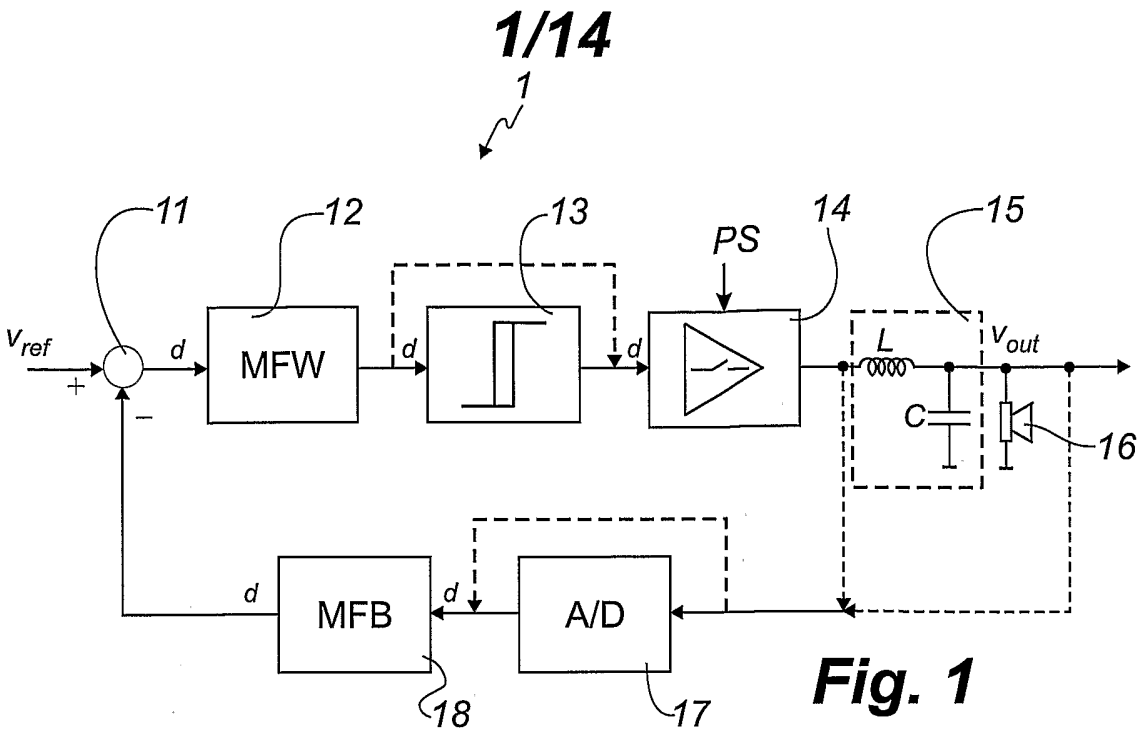
22. A digital self-oscillating modulator (1) according to any of the preceding claims, further including one or more additional output filters, one or more additional feedbacks (22) with transfer functions (CFB) coupled either after the output stage, after the output filter or after one or more of the additional output filters, as well as one or more forward blocks (20), which include both means for calculating the difference be-

tween one of the signals fed back from the additional function blocks and a reference signal, as well as a transfer function (CFW).

23. A digital self-oscillating modulator (1) according to claim 22, characterised by the transfer function (MFB) of the feedback block (18), the transfer function (MFW) of the forward block (12), the additional output filters, the transfer functions (CFB) of the additional feedback blocks (22) and the transfer function (CFW) of the additional forward blocks (20) together generating the desired total transfer function.

24. A digital self-oscillating modulator according to one of the preceding claims, wherein the desired total transfer function is identical to or similar to a first order low-pass-characteristic or integrator characteristic.

25. A synchronised modulator comprising two digital modulators (51, 52) according to any of the preceding claims, wherein a reference voltage ($X_{in,pos}$) is input to a first digital modulator (51) and a digital inverted reference voltage ($X_{in,neg}$) is input to a second digital modulator (52), the outputs from said first and said second digital modulator being synchronised by use of a synchronisation block.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11
12
13
PS
14
15
V_{ref}
+
−
d
MFW
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d
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V_{out}
C
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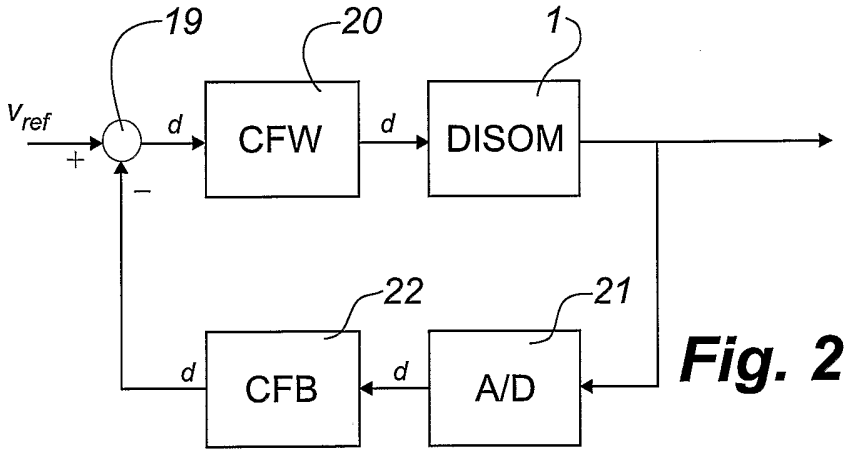
d
MFB
d
A/D
18
17

Fig. 1


19
20
1
V_{ref}
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−
d
CFW
d
DISOM
22
21
d
CFB
d
A/D

Fig. 2

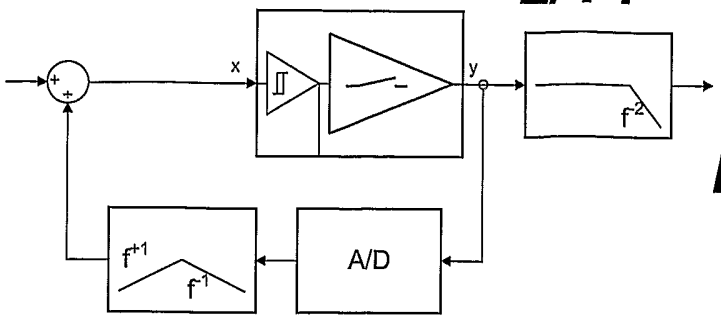


Fig. 3

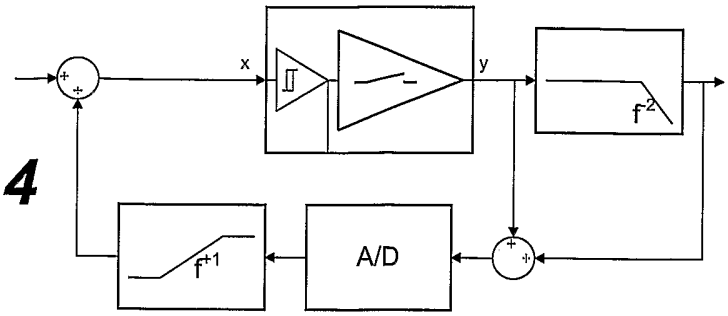


Fig. 4

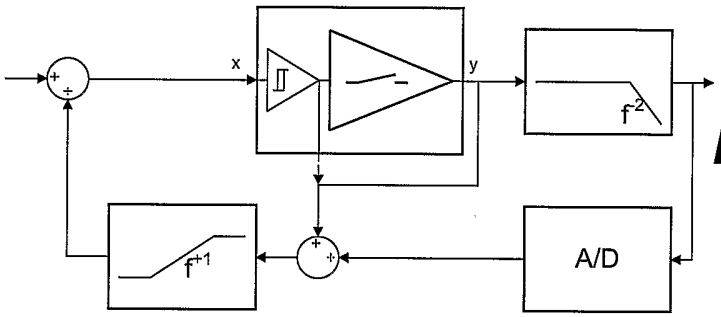


Fig. 5

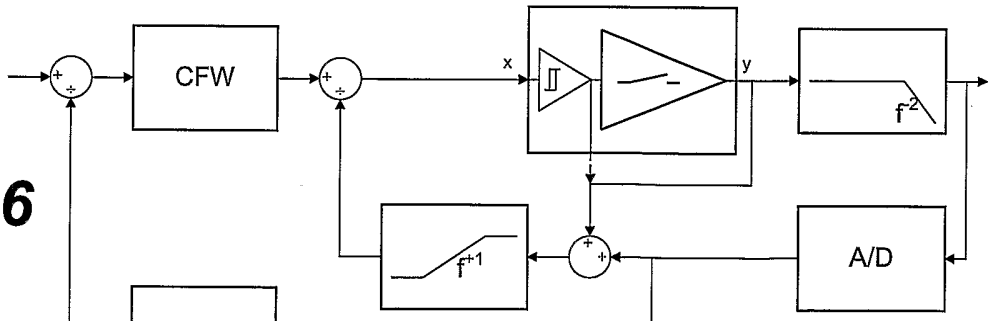


Fig. 6

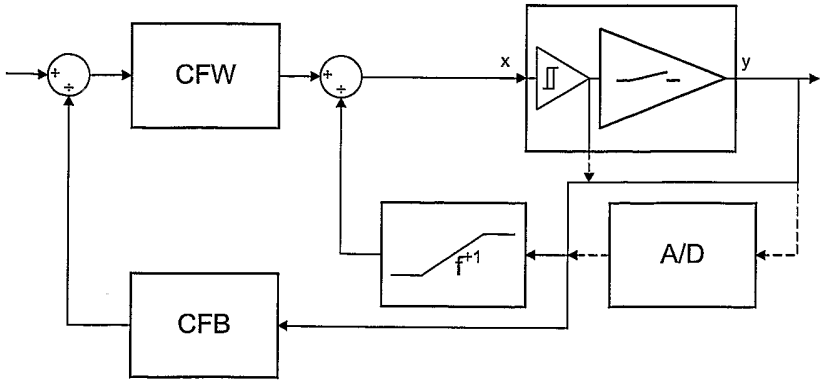


Fig. 7

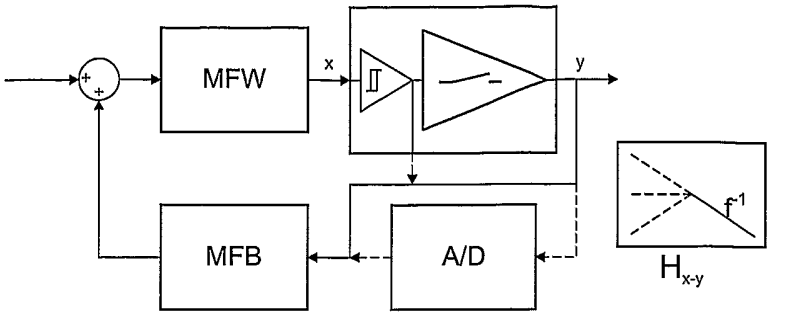


Fig. 8

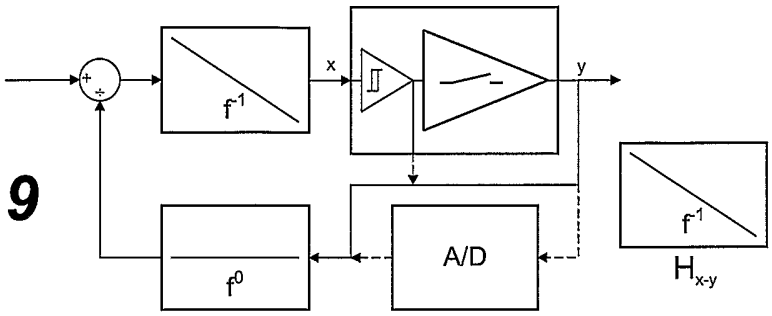


Fig. 9

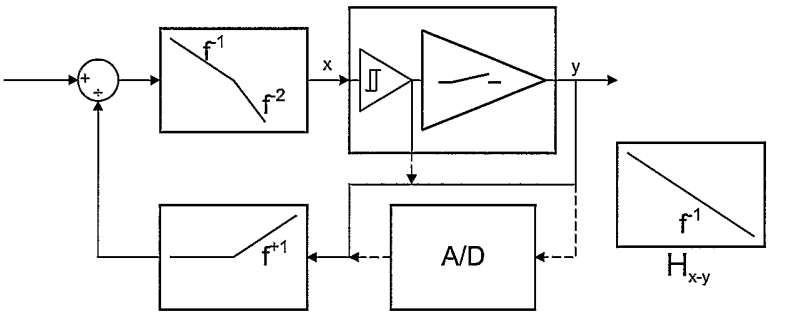


Fig. 10

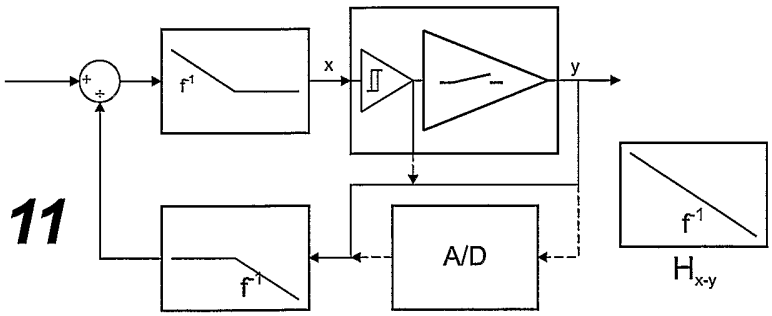


Fig. 11

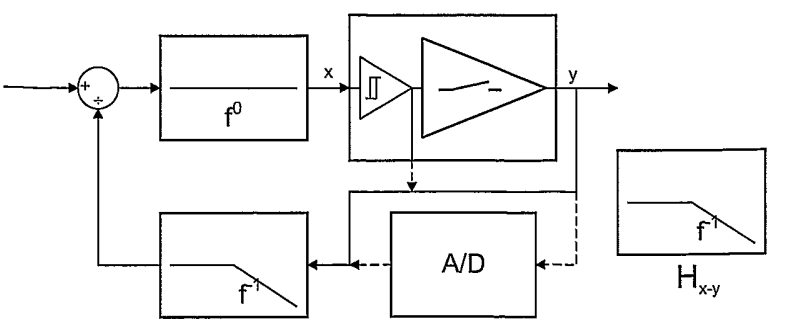


Fig. 12

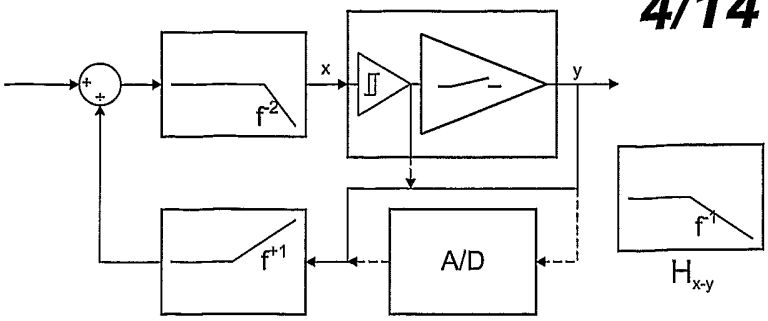
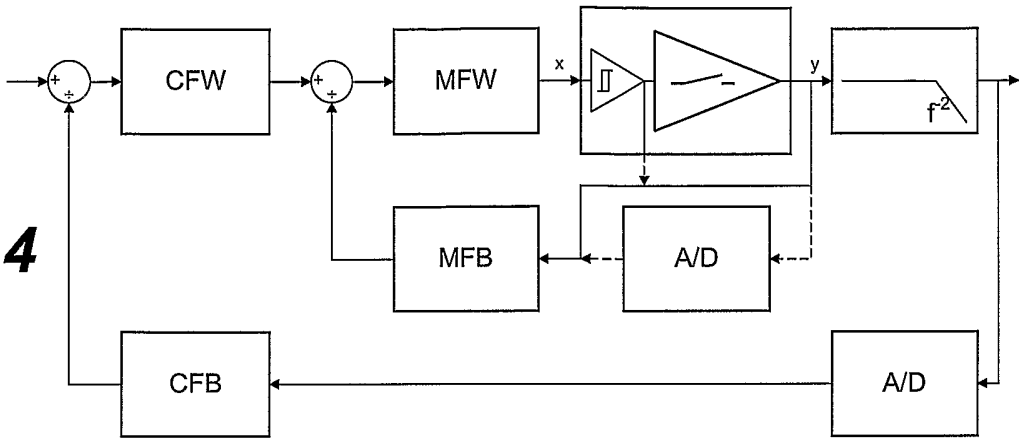


Fig. 13



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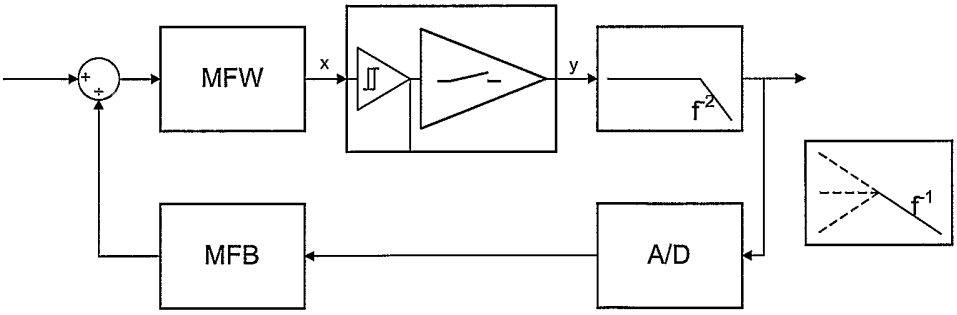

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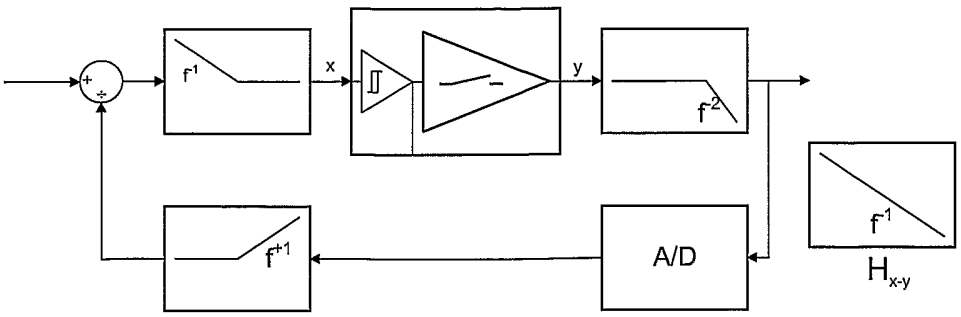

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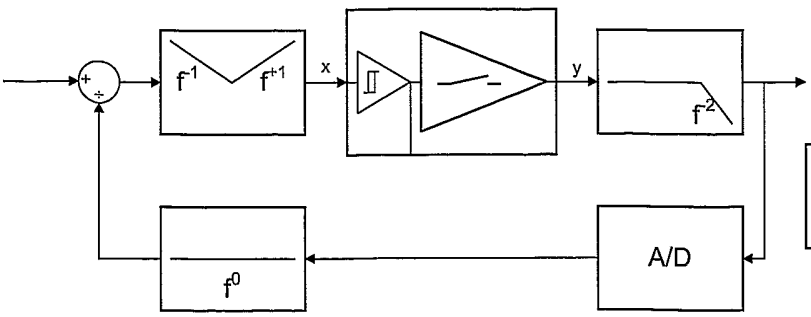

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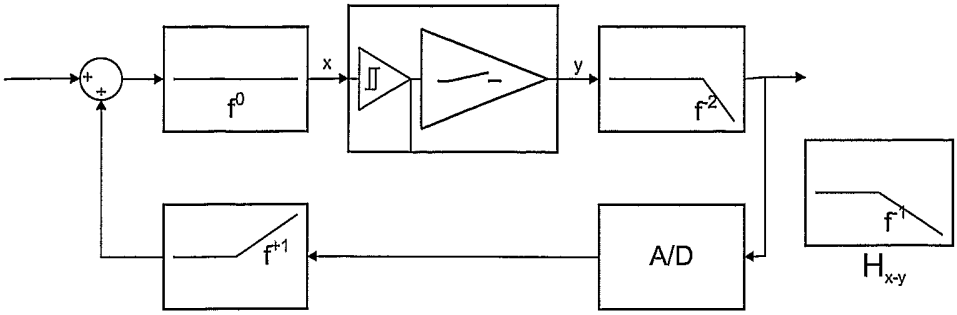

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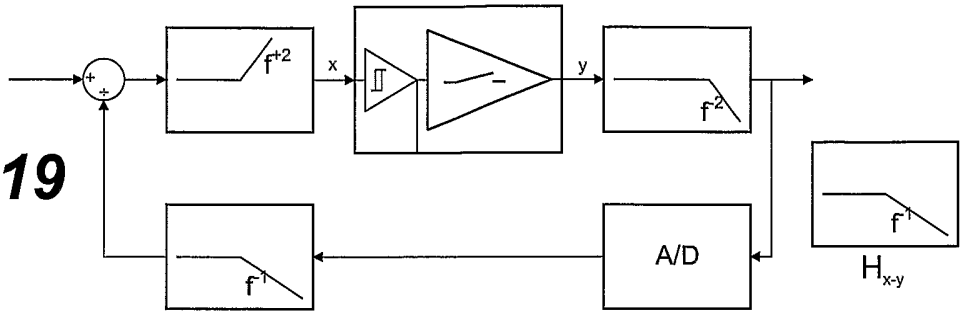

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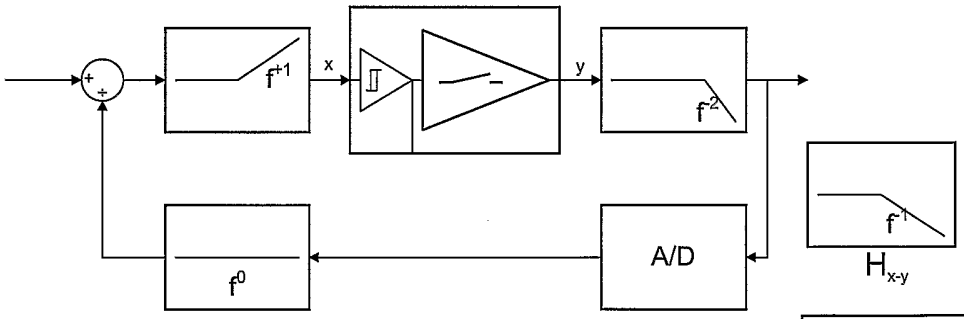

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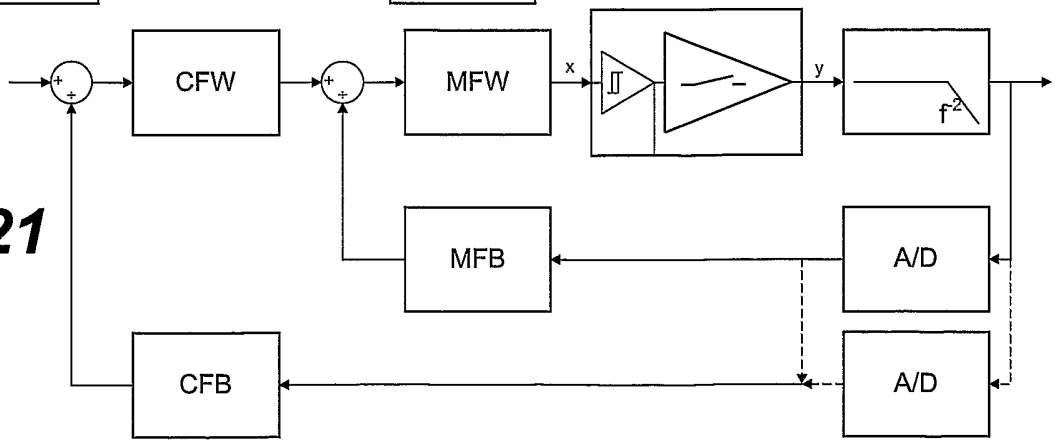

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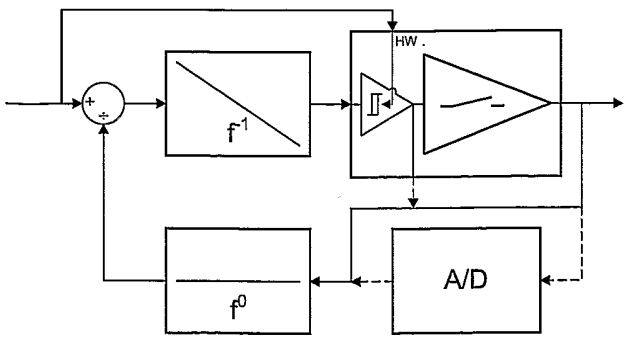

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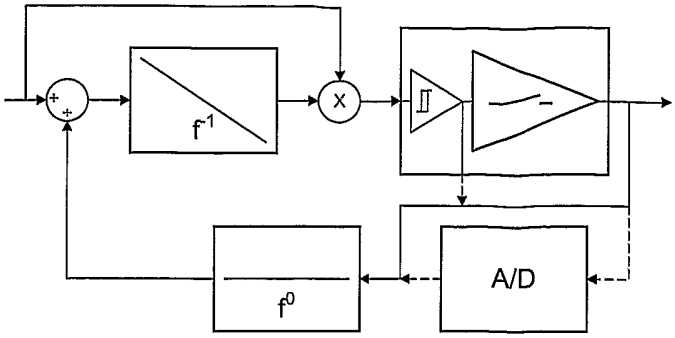

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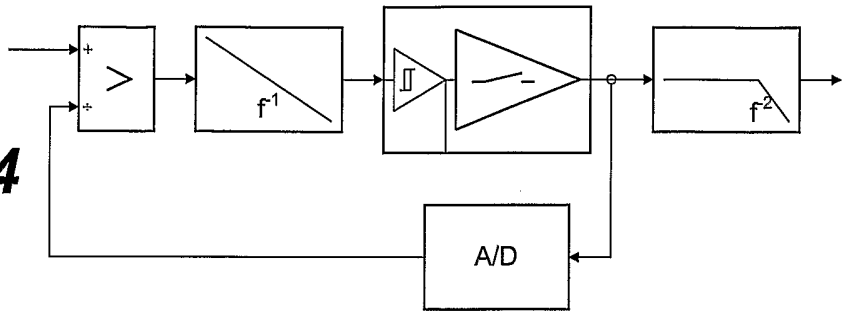

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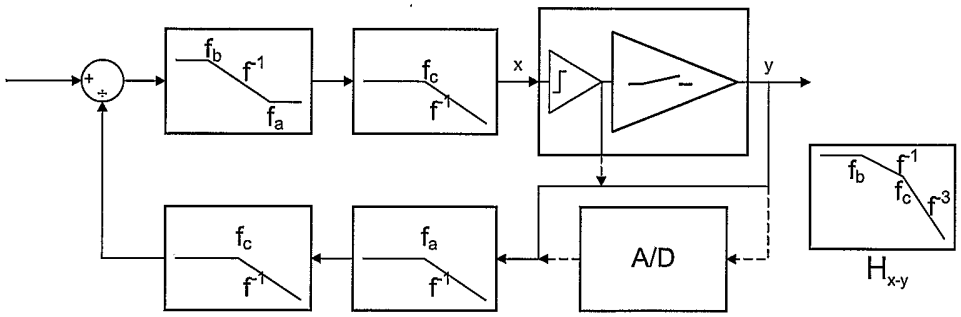

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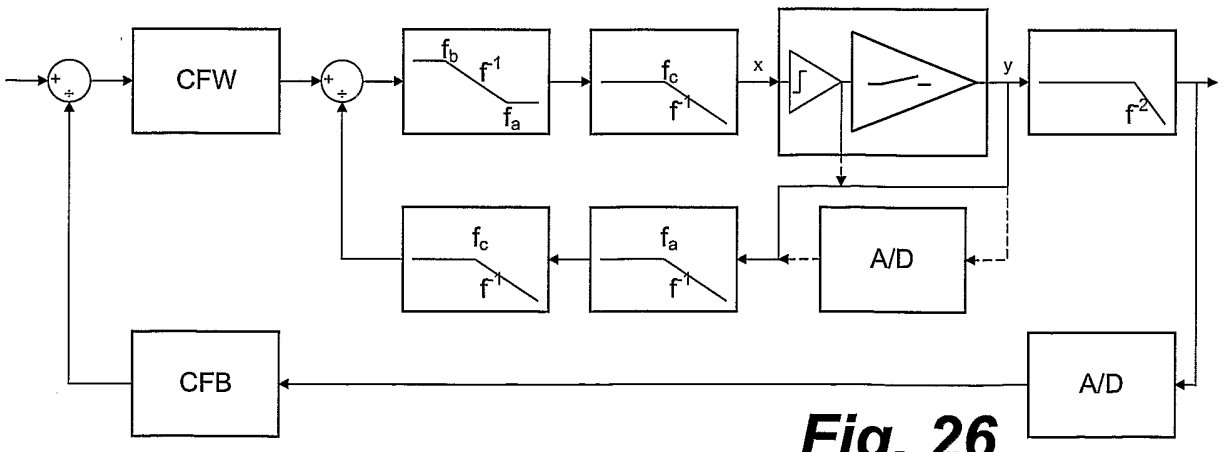

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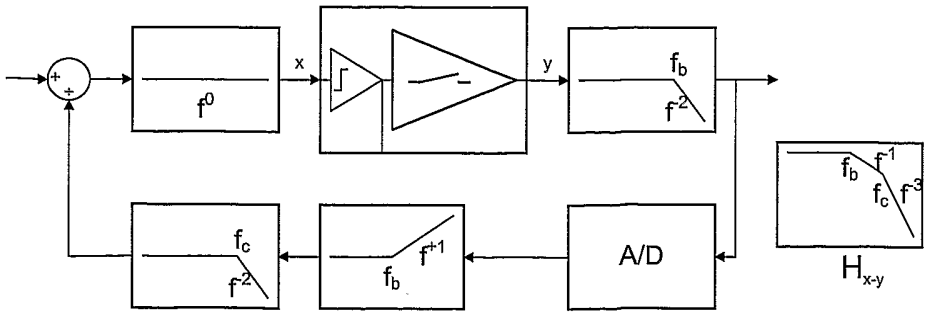

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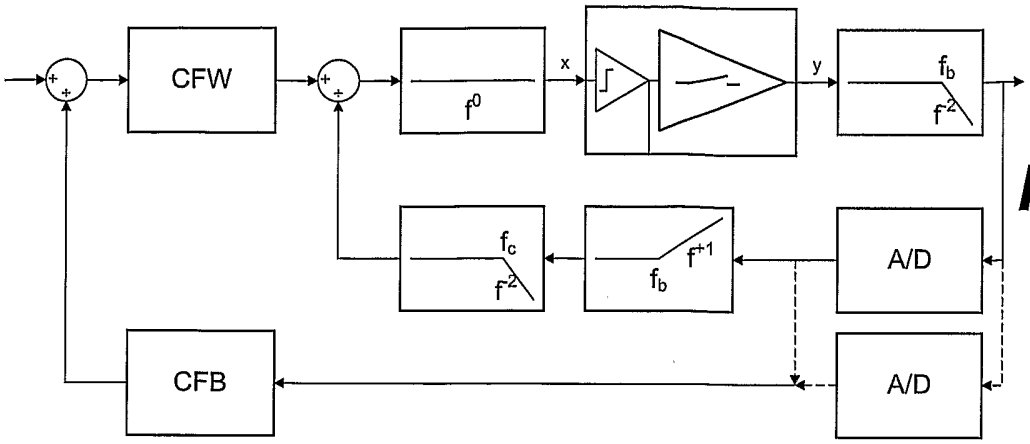


Fig. 28

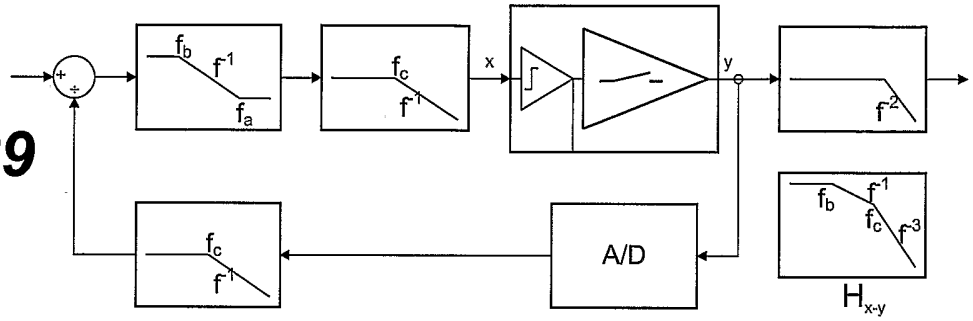


Fig. 29

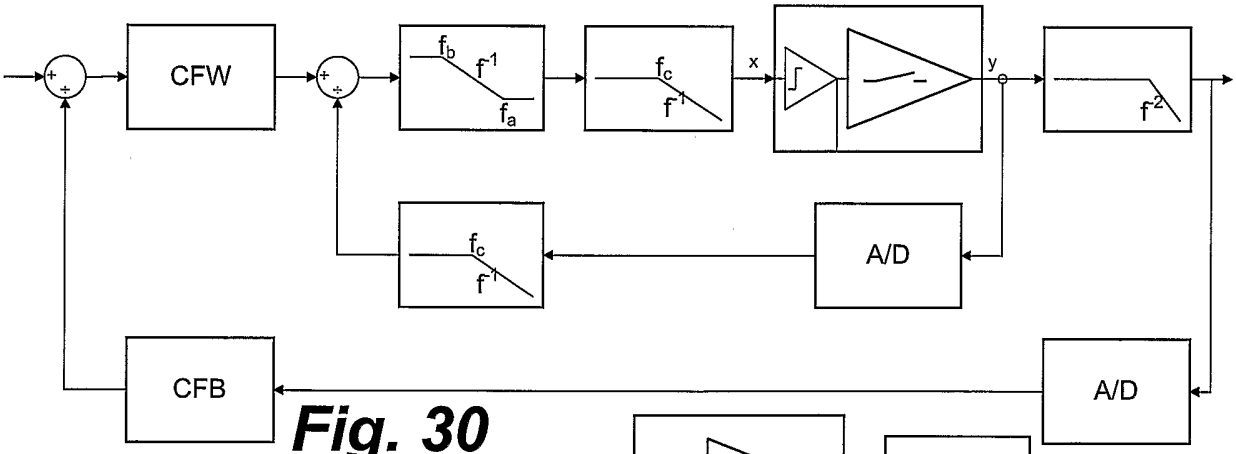
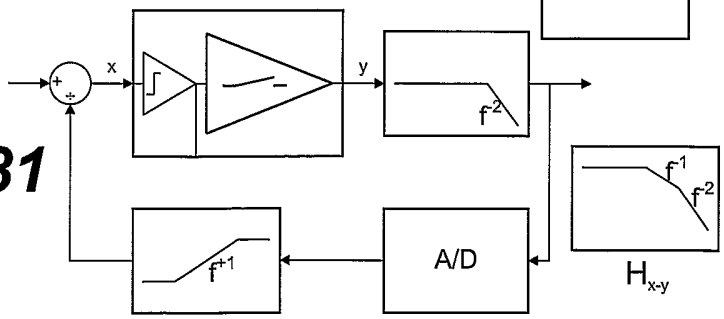


Fig. 30



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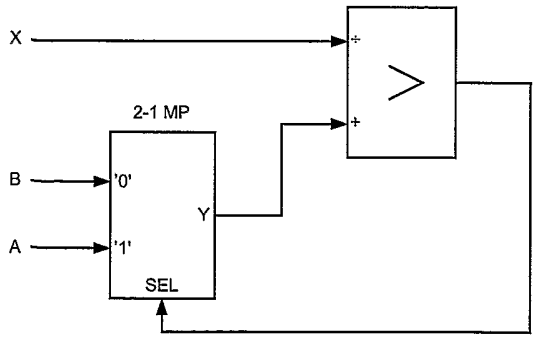

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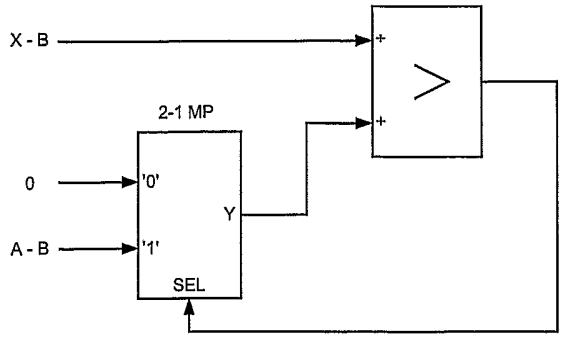

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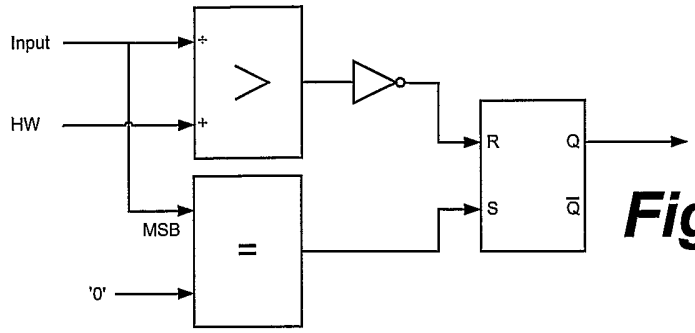

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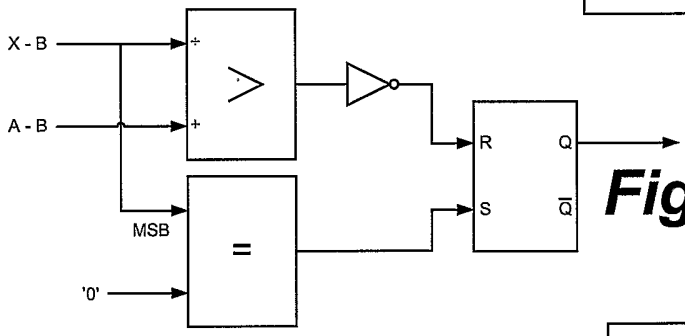

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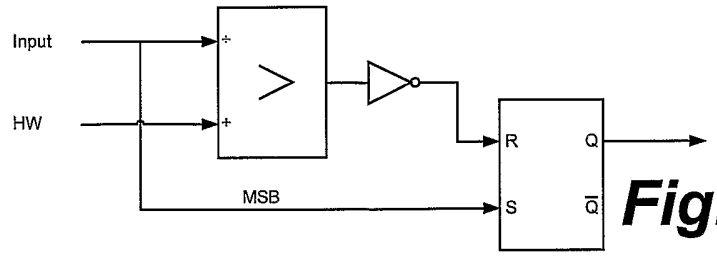

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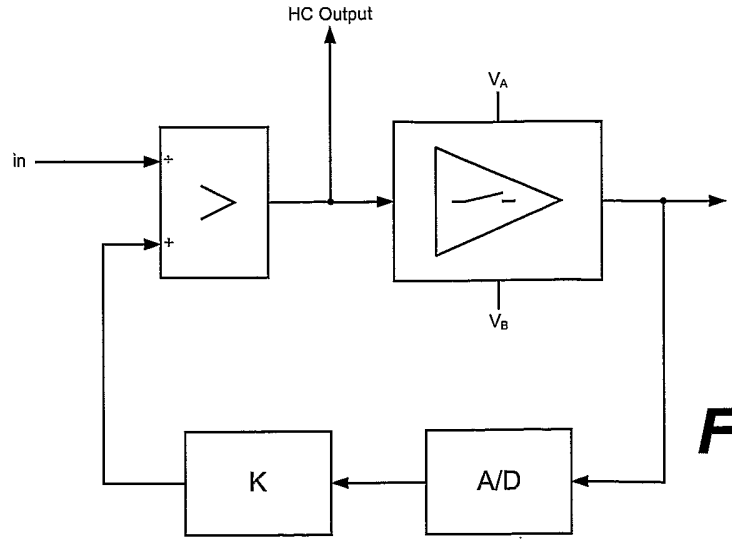

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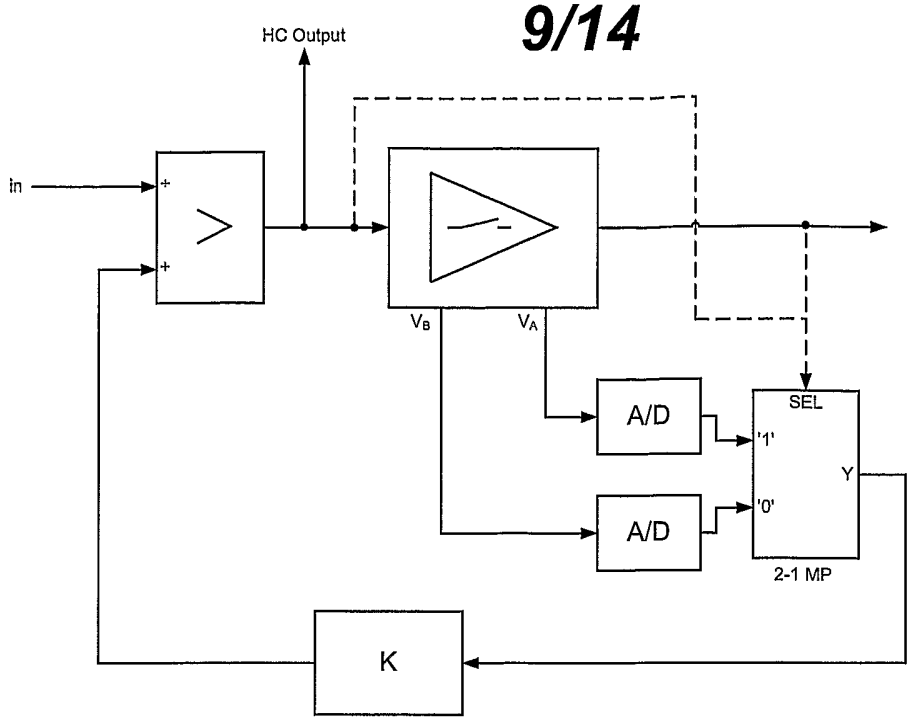

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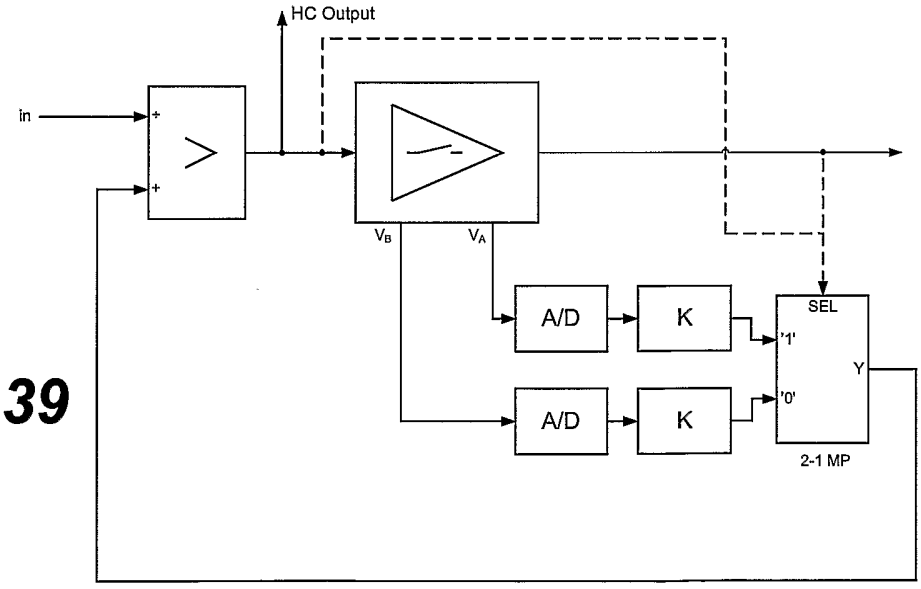

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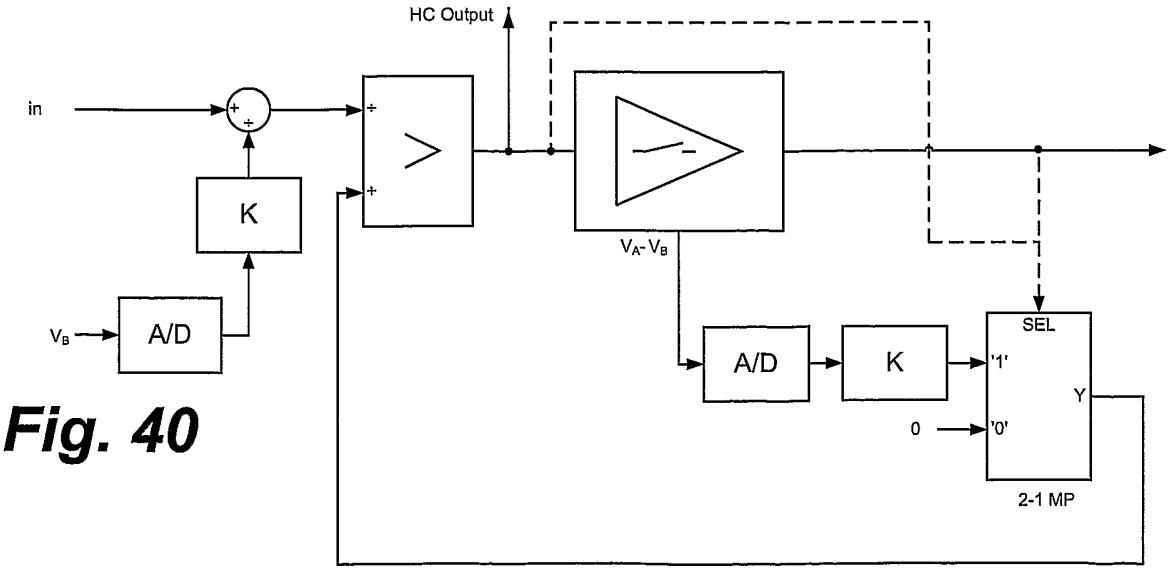

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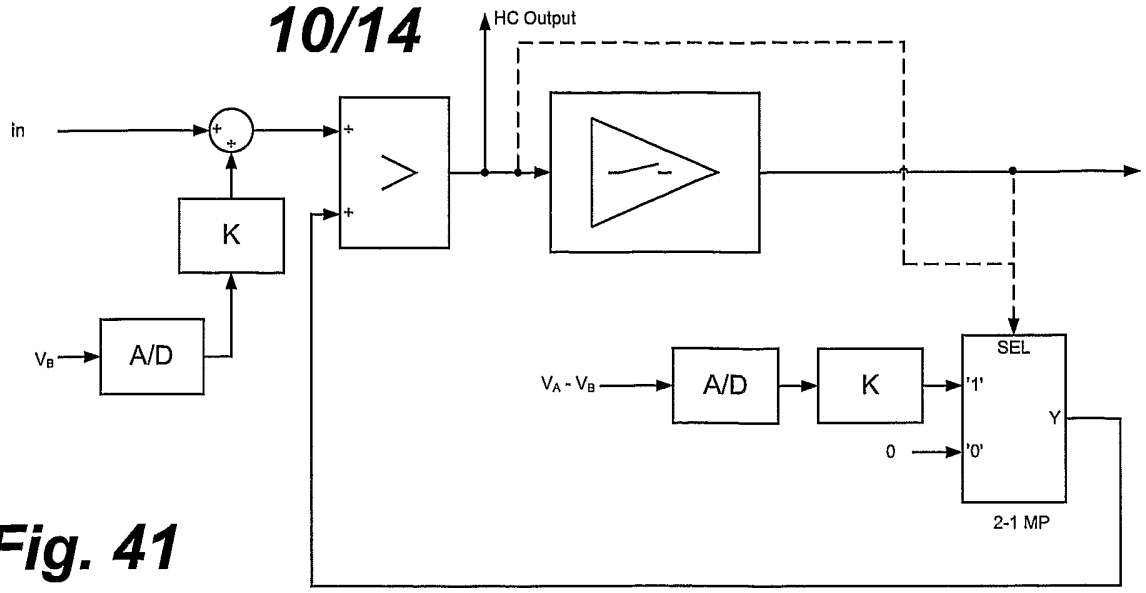

HC Output
in
K
V_B
A/D
$V_A - V_B$
A/D
K
SEL
'1'
Y
0
'0'
2-1 MP

Fig. 41

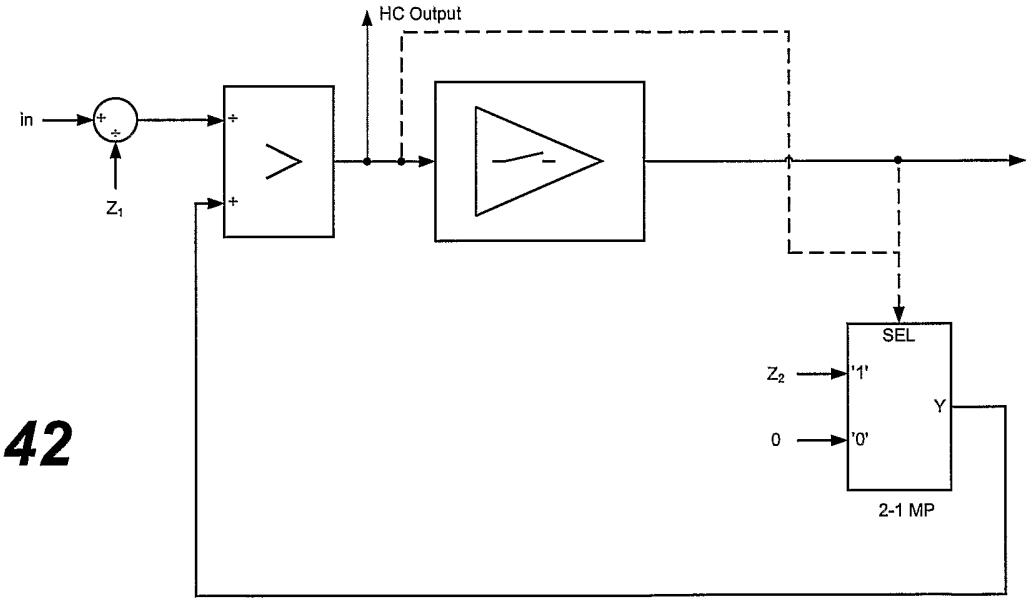
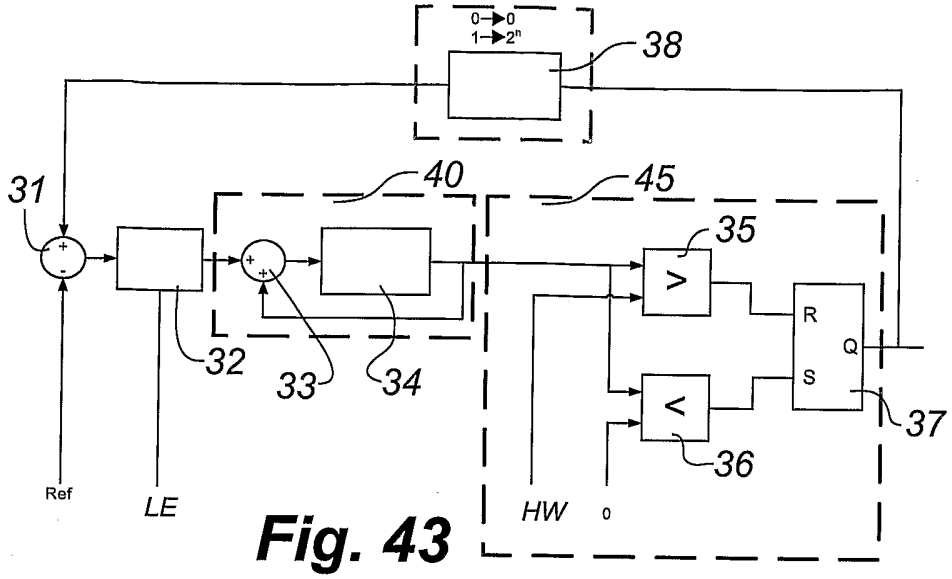

HC Output
in
Z_1
SEL
Z_2
'1'
Y
0
'0'
2-1 MP

Fig. 42



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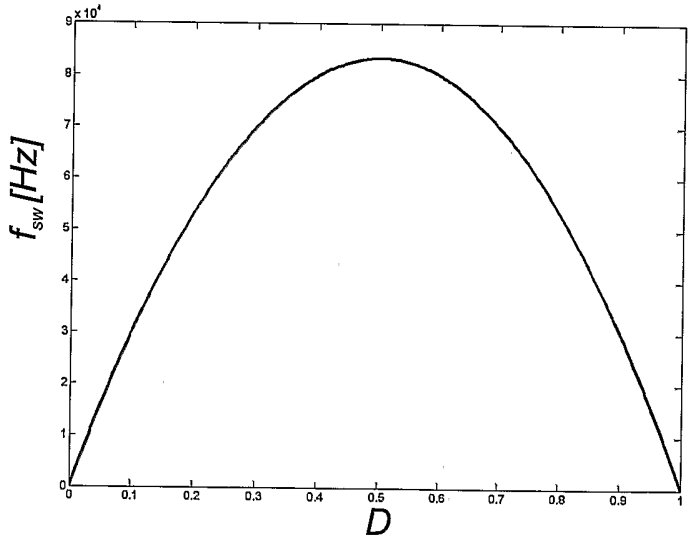

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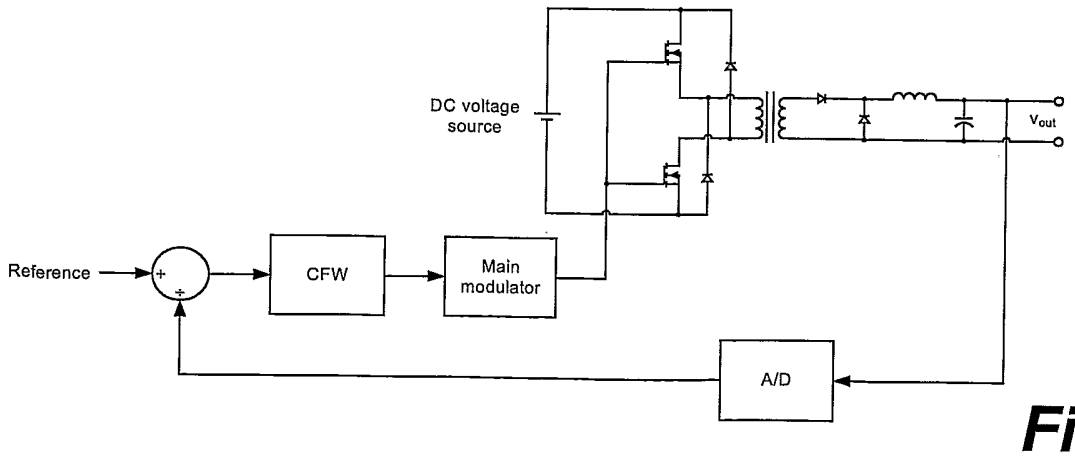

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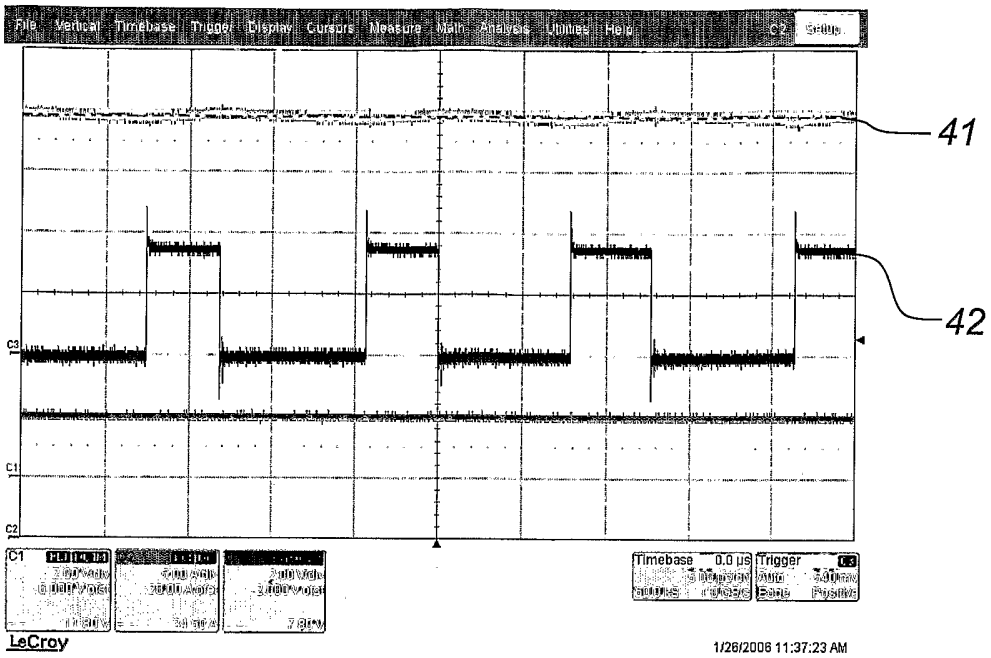
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42
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1/26/2006 11:37:23 AM

Fig. 46

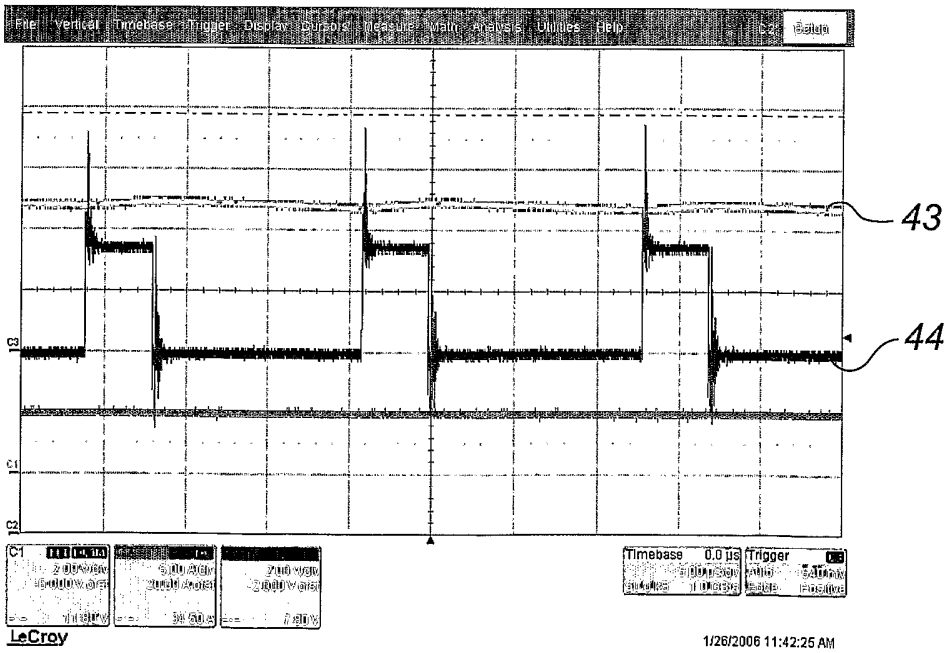
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Fig. 47

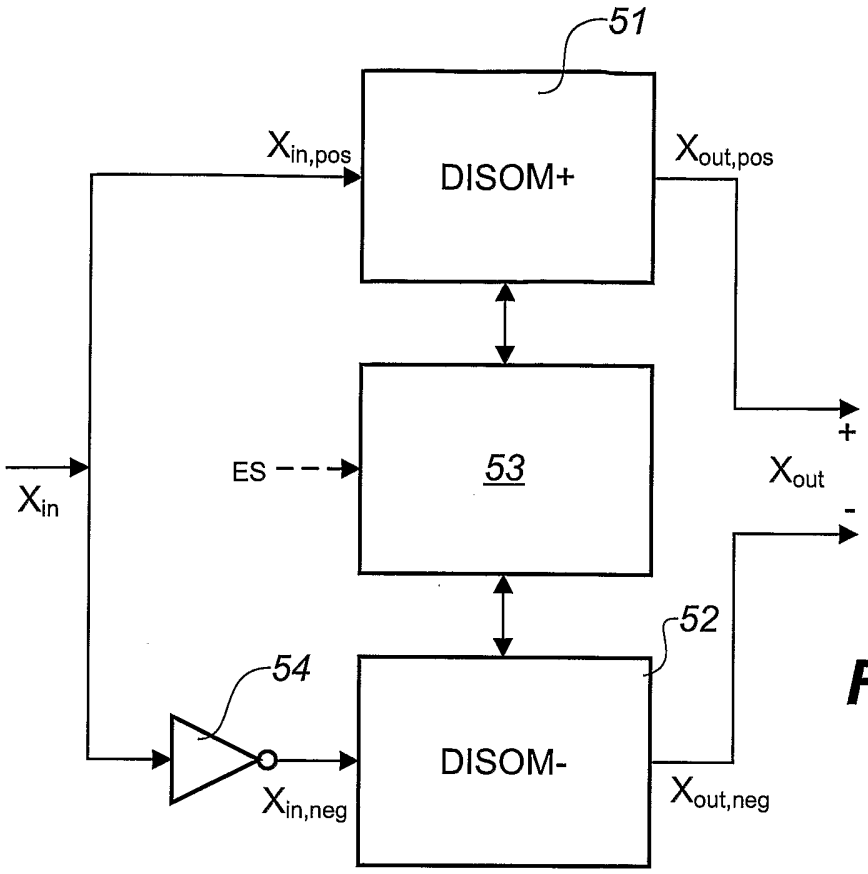
51
DISOM+
$X_{in,pos}$
$X_{out,pos}$
ES
53
X_{in}
+
X_{out}
-
52
54
DISOM-
$X_{in,neg}$
$X_{out,neg}$

Fig. 48

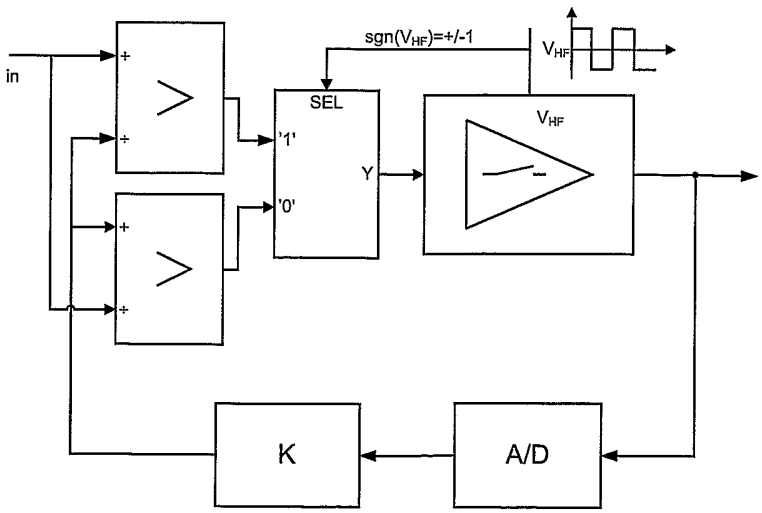
in
sgn(V_{HF})=+/-1
V_{HF}
SEL
'1'
'0'
Y
V_{HF}
K
A/D

Fig. 49

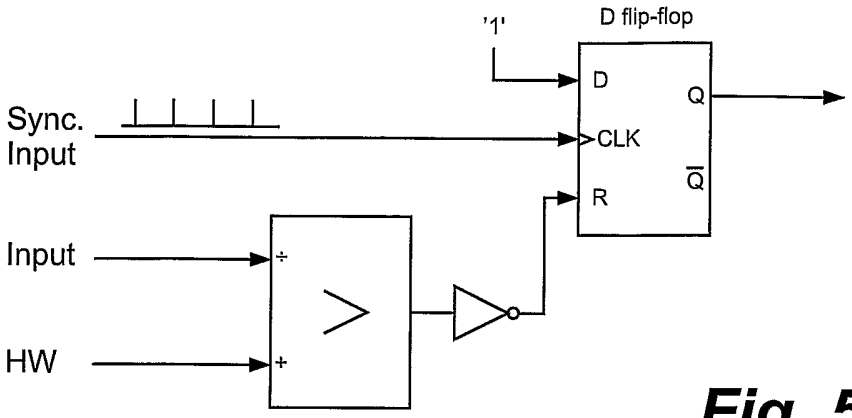
'1'
D flip-flop
D
Q
CLK
Q̄
R
Sync.
Input
Input
HW
÷
+

Fig. 50

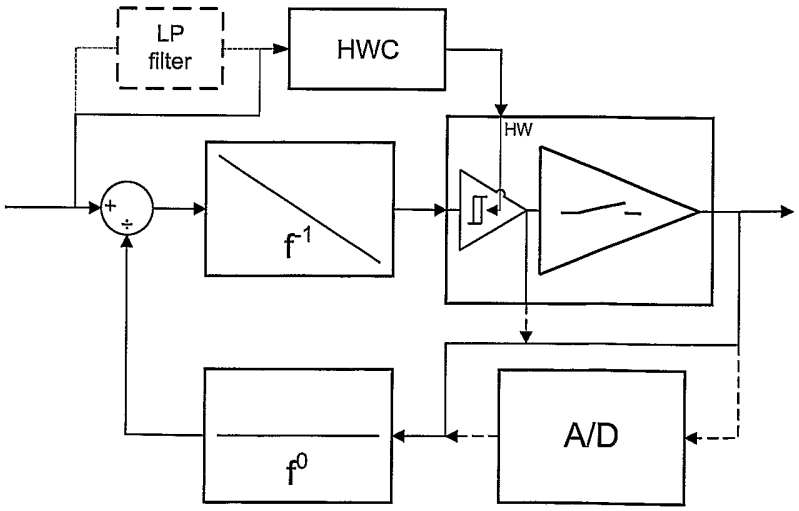
LP
filter
HWC
HW
+
÷
f-1
f0
A/D

Fig. 51

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ISBN 978-87-911-849-01