Low-Power, Low-Voltage Analog to Digital

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Low-Power, Low-Voltage Analog to Digital $\Sigma\Delta$ Modulators

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Abstract

This thesis is the result of three years of research in the field of integrated analog electronics. The research was carried out by Ulrik Wismar as part of the work leading to the PhD title. It is expected that the reader is familiar with basic semiconductor theory.

The topic of this work is various implementations of audio band $\Sigma\Delta$ modulators used as CMOS analog to digital converters. The intended application is hearing aids where analog to digital converters are used to convert the preamplified signal from a microphone into a digital signal which is fed into a microprocessor. A hearing aid is battery driven, and since long operation time is required, low supply voltage and low power consumption are of paramount importance. Consequently, various topologies have been compared to find the most power efficient audio frequency modulator topology.

Chapter 4 of this thesis compares power consumption of two of the most prevalent topologies, the single-loop $\Sigma\Delta$ modulator with integration in discrete time and the single-loop $\Sigma\Delta$ modulator with integration in continuous time. Both modulator topologies are with feedback, and all intermediate signals are in the voltage mode.

Chapter 5 treats a $\Sigma\Delta$ modulator without feedback. Another difference between the modulators described in the two chapters is that the voltage input signal is frequency modulated and handled in the frequency mode internally in the modulator.

For the feedback modulators, the results are based on simulation, whereas the part about modulators without feedback is based on measurements on two prototypes.

Resumé

Denne afhandling er resultatet af tre års forskning inden for området analog elektronik. Forskningen er udført af Ulrik Wismar som et led i arbejdet mod ph.d.-graden. Det forventes, at læseren er bekendt med grundlæggende halvlederteori.

Emnet for dette arbejde er implementering af forskellige audiobånd $\Sigma\Delta$ modulatorer benyttet i CMOS analog til digital konvertere. Den tiltænkte applikation er høreapparater, hvor analog til digital konvertere benyttes til at konvertere det forstærkede signal fra mikrofonen til et digitalt signal, der kan benyttes i en mikroprocessor. Et høreapparat er forsynet fra et batteri, og da lang funktionstid er krævet, har lav forsyningsspænding og effektforbrug førsteprioritet. Derfor er forskellige topologier blevet sammenlignet, således at den mest effektoptimerede audiofrekvensmodulator kan findes.

I kapital 4 sammenlignes effektforbruget i to af de mest fremherskende topologier, enkeltsløjfe $\Sigma\Delta$ modulatoren i en variation med integration i diskret tid og i en variation med integration i kontinuert tid. Begge modulatortopologier er med feedback, og alle interne signaler er spændingssignaler.

Kapitel 5 omhandler en $\Sigma\Delta$ modulator uden feedback. En anden forskel mellem modulatorerne i den første og anden del er, at spændingsindgangssignalet er frekvensmoduleret og behandlet i frekvensdomænet internt i modulatoren.

Resultaterne for modulatoren med feedback er baseret på simuleringer, hvorimod den del, der omhandler modulatorer uden feedback, er baseret på målinger på to prototyper.

Acknowledgments

This PhD scholarship was sponsored by the Technical University of Denmark, and the research was carried out at the Centre for Physical Electronics Ørsted·DTU. The Department of Informatics at the University of Oslo payed the expenses of the chip fabrication.

I would like to thank Pietro Andreani for skilled supervision, my co-supervisor Erik Bruun for guidance, the rest of the Centre for Physical Electronics, Allan Jørgensen for technical support, Dorte Lundsgaard and Luca Vandi for proofreading my thesis. I would also like to thank my industrial contacts Karsten Jensen (GN Resound) and Ivan Jørgensen (Oticon) for answering my questions on hearing aids and Jannik Hammel Nielsen (AudioAsics/Analog Devices) for valuable support in the start-up phase of the work.

The work was partly carried out during my stay at the Department of Informatics at the University of Oslo, and I would like to thank the group for their great encouragement and support. Especially thanks to Dag Trygve Wisland for supervision in professional as well as practical and private matters during my stays in Oslo.

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Chapter 1

Introduction

Ever since hearing aids were just a bulky ear trumpet just barely helping the person with hearing problems, the focus on hearing aids has been increasing. The demands to functionality, design and durability are getting higher, and at the same time hearing problems are not as tabooed as they used to be, and thus the market for hearing aids is growing.

The first electrical hearing aids were just an amplifier amplifying the sound from a microphone to a speaker in the ear. Today the sound is subject to a sophisticated signal processing. Where the controls in the most basic hearing aids were limited to changing the volume up and down, the signal processing in today's hearing aids applies advanced filters such that the user can have pleasure of the hearing aid even in noisy environments such as when a lot of people are gathered. To some extent it is even possible to incorporate the directional information that a normal hearing person possesses.

The signal flow in a modern hearing aid is shown in Fig. 1.1. The signal coming from the microphone is an analog signal. Therefore, an analog to digital conversion (ADC) is needed, possibly in connection with a pre-amplifier. After the digital signal processing, a digital to analog converter (DAC) converts the signal which is power amplified in a driver to enable it to drive the loudspeaker. This thesis deals with the ADC circuits.

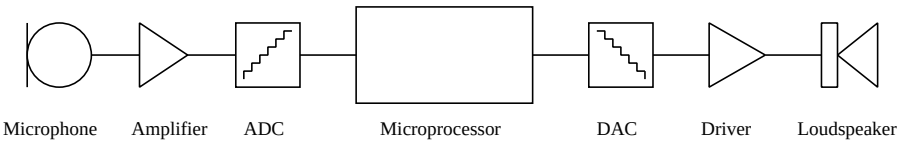

Figure 1.1: Signal flow in a modern hearing aid

The demands on functionalities and sound qualities approaching hifi levels usually require increased power consumption which again requires a bigger battery to keep a decent durability. On the other hand the demands on the hearing aid design set a limit to the dimensions of the device. If the electrical circuits are custom made, they can be quite small, but the battery sets the limit and thus the total power consumption is limited to approximately 1 mW for a complete hearing aid. This leaves a power consumption for the ADC in the range of 100 μW. Therefore the topic of this thesis is to reveal how efficient the different ADC topologies are with respect to power consumption. Besides the power consumption which should be low, the supply voltage should be below 1 V and the bandwidth of the ADC should be audio band (20 Hz - 20 kHz), while 16 bit resolution is preferred. Demands which are difficult to obtain at the same time.

The organization of the thesis is, that Chapter 2 starts with a presentation of ADC in general. This means Nyquist rate and $\Sigma\Delta$ converters. Nyquist converters are shortly presented and supported with an appendix on different types of Nyquist converters as well as with a paper with an implementation. In chapter 3 the noise models for the amplifier and the oscillator used in chapter 4 and 5 are presented. These models are build on the basic noise models of the single components seen in appendix B. In chapter 4 the single-bit single-loop $\Sigma\Delta$ modulators with feedback in discrete and continuous time are studied to find the most power optimal solution of the two. The power consumption of a $\Sigma\Delta$ modulator without feedback is presented with the frequency to digital $\Sigma\Delta$ (FDSM) implementation in chapter 5, and the results from the modulators with and without feedback are compared through a figure of merit (FoM). Chapter 6 contains the conclusions.

Papers written in connection to this work supporting the topic are included in appendix C. The first paper “A Low-Power CMOS Interface Chip for Data Logging Applications” presented at Eurosensors is based on an implementation from the author’s MSc thesis work, but it includes an integrating converter and is related to the Nyquist converters in chapter 2. The Norchip Paper ”Impact of Oscillator Power in Discrete and Continuous Time $\Sigma\Delta$ Converter” presents how jitter noise couples in discrete and continuous time modulators, whereas the second Norchip paper ”Linearity of Bulk-Controlled Inverter Ring VCO in Weak and Strong Inversion” discusses how the modulation in a ring oscillator can be linearized. This topic is also discussed more in depth in the accepted Analog Integrated Circuits and Signal Processing journal paper ”Linearity of Bulk-Controlled Inverter Ring VCO in Weak and Strong Inversion”. The paper ”Power Consumption Optimization in $\Sigma\Delta$ A/D Converters

with Oscillator Co-Design" is also a full length paper on the theoretical comparison of power consumptions in discrete and continuous single-loop modulators. It is currently under review for IEEE Transactions on Circuits and Systems. The first implementation of the FDSM was presented at ESSCIRC with the paper "A 0.2 V 0.44 μW 20 kHz Analog to Digital $\Sigma\Delta$ Modulator with 57 fJ/conversion FoM".

Chapter 2

ADC in general

In this chapter definitions of different ADCs are shortly introduced, since it is important to remember the basics when going to the more advanced $\Sigma\Delta$ modulators. Also Nyquist rate converters are discussed shortly to demonstrate why they are inadequate as power optimized medium to high resolution converters.

2.1 Analog and digital signals

The ADC denotes all circuits that have an analog signal at the input and the corresponding digital signal at the output. A signal is analog when both time and amplitude are continuous, such as the signal from a microphone. Time is quantized after sampling with a periodic sampling clock. The amplitude is quantized with a quantizer. The digital signal is obtained when both time and amplitude are quantized. Each sample represents the amplitude with a binary number (e.g. 3 bit D1 to D3):

$$V_{out} = V_{ref}(\mathrm{D1} \cdot 2^0 + \mathrm{D2} \cdot 2^1 + \mathrm{D3} \cdot 2^2) \tag{2.1}$$

	Non-quantized time	Quantized time
Non-quantized amplitude	Analog signal	
Quantized amplitude		Digital signal

This means that a simple ADC is obtained with a sampler and a comparator. The digital signal obtained with this system is, however, just single-bit which is a quite poor representation of the analog signal. A better representation can be obtained by having more steps in the quantizer. However, regardless of the number of steps the analog signal cannot be modeled precisely.

The digital output of the ADC should thus be seen as the signal at the input and a so-called quantization noise. This means, that the ADC will provide a signal to noise ratio (SNR) defined from the number of bits (B) in the quantizer given in dB as:

$$\text{SNR} = 1.76 + 6.02B \tag{2.2}$$

2.2 Nyquist conversion

A higher number of bits can be obtained in various ways depending on the purpose of the ADC, ranging from high speed and low resolution such as the flash converter to low speed and high resolution such as the integrating converters mentioned in appendix A and measured in paper 1.

The name Nyquist converter relates to the fact that they operate at the Nyquist rate, which is the lowest sampling frequency f_s at which the analog signal can be recreated. This speed is twice the highest conversion band frequency f_b at the input:

$$f_s \geq f_b \cdot 2 \tag{2.3}$$

2.2.1 Anti-aliasing filter

In all Nyquist rate converters the input signal is sampled. This results in a zero order hold signal, meaning that the sinusoidal signal applied to the input is repeated around all integer multiples of f_s. The input signal can be represented as a double sideband signal, consisting of both a positive and a negative frequency contribution.

$$\cos(t\omega) = \frac{e^{-\imath t\omega} + e^{\imath t\omega}}{2} \tag{2.4}$$

When the input frequency becomes higher than half of the sampling frequency, the negative frequency representation repeated at f_s and the positive representation at DC ends up at the same place as illustrated in Fig. 2.1. This problem is known as the aliasing problem.

To avoid this problem it has to be ensured, that the input frequency spectrum is limited to $f_s/2$ with an anti-aliasing filter, if the input signal contains frequencies above $f_s/2$. The filter has to have a high order (high number of poles) giving a steep transaction between the pass and stop band. At the same time the dynamic range of the filter has to be higher than the dynamic range of the converter following

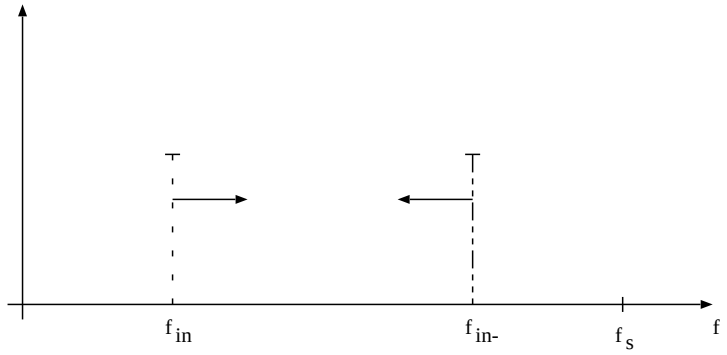

Figure 2.1: The aliasing problem

the filter. It is possible to produce these filters, but the power consumption is quite considerable.

Two main categories are continuous time (CT) filters and discrete time (DT) filters. The DT filters could be switched-cap or switched-opamp for low voltages [8]. The CT filters are often G_mC topologies [43] [52] [60] or in some cases log-domain filters [30] [48], where the signal is compressed with a log function, integrated, and then expanded with an exponential function. The switched circuits are made with MOS transistors, the G_mC filters are made with MOS or bipolar, but the log-domain filters need bipolar transistors making them less compatible with many MOS processes. For low power audio band low-pass applications mainly the G_mC filters are used.

The performance of the state of the art filters can be compared with a figure of merit (FoM) given as [48] [60]:

$$FoM = \frac{P_f}{f_f \cdot N_p \cdot \mathrm{DR}}. \tag{2.5}$$

In the equation P_f is the power consumption of the filter, f_f is the highest 3-dB frequency, N_p is the number of poles in the filter and DR is the dynamic range at the output of the filter. The FoM should be as low as possible, and by using (2.5) performance of different filter types even for different frequency bands, can be compared. In table 2.1 FoMs for some state of the art filters are calculated.

From the FoM values in table 2.1 power consumption can be estimated for any given filter. The G_mC implementation is chosen to eliminate the use of bipolar transistors, and in the following it is assumed, that a FoM of 2e-13 can be used. If the converter following the filter is able to obtain 16 bits resolution, the SNR is 98 dB requiring a DR larger than 98 dB.

If the anti-aliasing problem should be removed, the damping in the filter is as-

Table 2.1: Performance of state of the art filters

Author	Principle	Power	3-dB freq.	DR	V_{dd}	Order	FoM
Palaskas [43]	G_mC	23 mW	20 MHz	48 dB	2.5 V	10	4.6e-13
Villegas [52]	G_mC	2.5 μW	2 kHz	62 dB	1.25 V	2	4.0e-13
Yodprasit [60]	G_mC	240 μ W	50 kHz	75 dB	1.5 V	3	2.8e-13
Krishnapura [30]	log-domain	4.1 μ W	22 kHz	56 dB	1.5 V	2	1.5e-13
Punzenberger [48]	log-domain	23 μ W	320 kHz	57 dB	1.2 V	3	3.4e-14
Cheung [8]	Switched	310 μ W	76 kHz	54 dB	1 V	6	13.6e-13

sumed to be 100 dB at $f_s/2$.

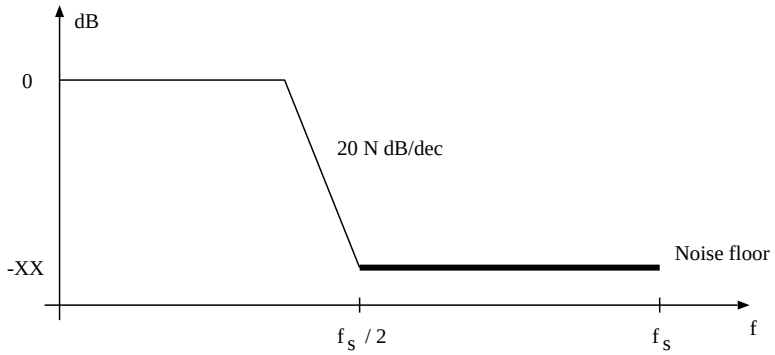

Figure 2.2: Performance of the anti-aliasing filter

It is seen from Fig. 2.2, that the approximate 3-dB frequency is $100/(20N_p)$ decades below half of the converter sampling frequency $f_s/2$. The 3-dB frequency is fixed as f_b, and thus the filtering order and the sampling frequency reveal a trade off. A higher filtering order increases the power consumption according to equation 2.5. If the filtering order is decreased, the sampling frequency is increased, increasing the power consumption in the following converter and in the oscillator. In table 2.2 the necessary sampling frequencies for $f_b = 20$ kHz and different filtering orders are found. The power consumption of the filter is found using an FoM of 2e-13.

From the table it is seen, that even with the lowest filtering order giving a non trivial sampling frequency, the power consumption is 0.4 mW. If the converter should be Nyquist rate, the power consumption for the filter alone is in the mW range which is much higher than what the budget in a hearing aid allows, and the conclusion is that if an anti-aliasing filter is needed, a Nyquist rate converter will not be advantageous. If the lower filtering order is used, the converter needs to oversample which costs a lot of power in a converter designed to operate at Nyquist rate.

Table 2.2: Power consumption and the necessary converter sampling frequency for different filtering orders to obtain 16 bits SNR with a 3-dB frequency of 20 kHz.

Filtering order	Power consumption	Sampling frequency
1	0.4 mW	4 GHz
5	2 mW	400 kHz
10	4 mW	126 kHz
15	6 mW	86 kHz

2.3 Oversampling conversion

Other converters, the so-called oversampling converters, are designed to operate at clock frequencies much higher than the Nyquist rate. This will loosen the anti-aliasing problem found for the Nyquist converters. Some of these converters even have an inherent anti-aliasing filter and extra filtering can be disregarded in many applications.

The number of steps in the quantizer can be reduced in the oversampling converter. Since $f_s >> f_b$, the input signal to the quantizer can be seen as very slowly varying signal (very close to DC). Such a DC value in between the stages of the quantizer can be represented as the mean value of a number of samples. A higher number of samples within the same time is obtained by increasing f_s, and with a conversion frequency band of f_b this results in an increased oversampling ratio (OSR) defined as:

$$\text{OSR} \equiv \frac{f_s}{2f_b}. \tag{2.6}$$

A higher f_s corresponds to a higher number of steps in the quantizer, and thus the SNR of the converter can be increased with increased OSR, where a doubling of OSR results in 3 dB SNR or 0.5 bit [27]:

$$\text{SNR} = 6.02B + 1.76 + 10 \cdot log(\text{OSR}) \tag{2.7}$$

If a low number of quantization steps 2^B is used this, however, still requires a high OSR. The quantization noise spectral density is dependent on the signal, in most situations it is, however, a fair assumption that this noise is white when pure oversampling is used. Only the noise in the signal band is problematic since the rest will be filtered after the converter. This leads to the noise-shaping converter. The principle is that the quantization noise cannot be eliminated, but by moving the noise out of band, the SNR in the signal band can be increased. Thus the quantization

noise should be high-pass filtered as illustrated in Fig. 2.3

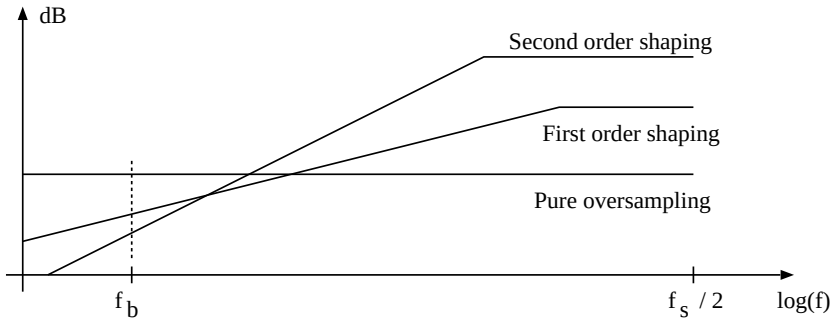

Figure 2.3: Noise shaping versus pure oversampling

It is seen, that a higher noise shaping order can suppress the signal band noise more than a lower filtering order. For an increase of one order, one extra bit or 6 dB extra is obtained for a doubling of OSR, and for first and second order noise shaping, SNR is given as:

$$\text{First order} \qquad \text{SNR} = 6.02B + 1.76 - 5.17 + 30 \cdot log(\text{OSR}) \tag{2.8}$$

$$\text{Second order} \qquad \text{SNR} = 6.02B + 1.76 - 12.9 + 50 \cdot log(\text{OSR}) \tag{2.9}$$

If noise shaping is used, it opens possibility of having a quantizer with just two levels (single-bit). This is often an advantage since the single-bit quantization is inherently linear, a linearity which is difficult to obtain in a multi-bit quantizer.

2.3.1 Noise shaping with a feedback circuit

The circuit commonly used to produce the noise shaping is the $\Sigma\Delta$ modulator with feedback. It consists of a sampler, a filter $H(z)$ and a quantizer. The quantizer provides the output signal $y(n)$, from the quantizer input signal $x(n)$ by adding quantization noise $e(n)$. A simple model of the $\Sigma\Delta$ modulator is seen in Fig. 2.4.

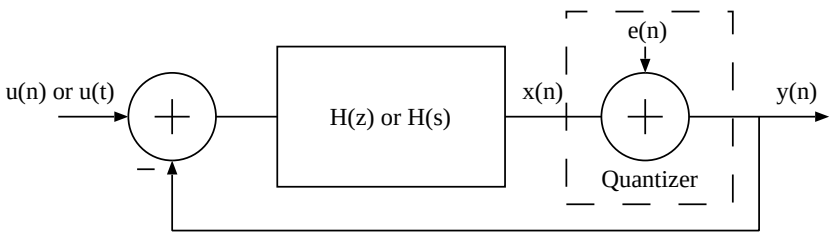

Figure 2.4: Simple model of the $\Sigma\Delta$ modulator

The sampler in the modulator can be placed at the input of the modulator resulting in a DT input signal $u(n)$, where n denotes discrete time, and in DT filtering $H(z)$ where z is discrete frequency. Contrary to the DT modulator the CT modulator has the sampler placed after the filtering. Here the input signal is $u(t)$, where t is continuous time, and the filtering is $H(s)$ where s is frequency in CT. The aliasing problems occur where the sampling takes place. In CT modulators the noise shaping takes place before the sampling, and thus it provides an inherent anti-aliasing filter which is an advantage that CT modulation has compared to DT modulation.

From Fig. 2.4 it is easily detected, that the signal and the quantization noise have two different transfer functions. The signal transfer function S_{TF} and the noise transfer function N_{TF} can be deduced from the figure as:

$$S_{TF} = \frac{H}{1+H} \tag{2.10}$$

$$N_{TF} = \frac{1}{1+H}. \tag{2.11}$$

This indicates that if H is high, S_{TF} equals unity whereas N_{TF} will be minimized. This is preferable in the signal band, and is obtained in the $\Sigma\Delta$ modulator by having an integrator as H, which ideally gives an infinite gain at DC.

The order of the noise shaping will be equal to the order of filtering in H, and thus it is controlled by the number of integrators. It is not only the modulator order which can be controlled, also the cut-off frequency f_{co} of the N_{TF} can be controlled by the coefficients in the loop. As illustrated in Fig. 2.5 it seems to be advantageous to have f_{co} very close to $f_s/2$, it will, however, be seen later that placing f_{co} too high can lead to instability.

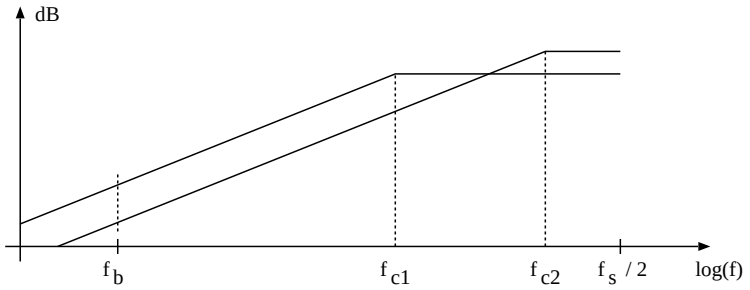

Figure 2.5: N_{TF} with different cut-off frequencies f_{c1} and f_{c2}

An advantage of having a modulator with feedback is that nonlinearities are suppressed due to the high gain in the forward path. It was also mentioned, that if a single-bit quantizer is used, it is perfectly linear. A DAC (not shown in Fig. 2.4)

is needed in the feedback path, but if the single-bit solution is used, this is just a scaling to a reference voltage. It is more problematic if a multi-bit quantizer is used. In this case a multi-bit DAC is needed in the feedback path, and the linearity of this DAC will be limiting the overall linearity of the modulator.

2.3.2 Noise-shaping circuits without feedback

The multi-bit quantizer problem can be solved by having a modulator without feedback. The disadvantage of such a modulator is that there is no suppression of non-linearities due to the feedback path and the high gain.

The modulator without feedback is seen in Fig. 2.6, where the principle is to shape the quantization noise and leave the signal unshaped. In this case the S_{TF} is not necessarily unity, but a gain can be incorporated.

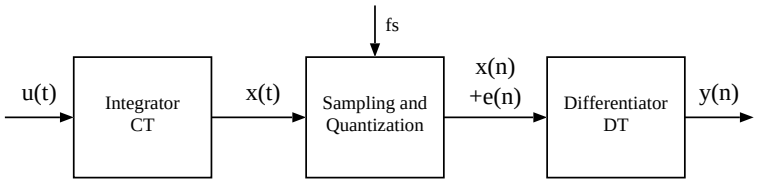

Figure 2.6: Simple model of the modulator without feedback

The CT signal $u(t)$ at the input is first exposed to an integration giving $x(t)$ which is sampled and quantized either as single- or multi-bit. The quantization will introduce quantization noise $e(n)$ on $x(n)$. The quantized signal is differentiated in DT, meaning that the signal is first integrated and then differentiated which results in the input signal transferred to the output with an amplification. The quantization noise $e(n)$ is only differentiated. Differentiating the quantization noise which is assumed white, results in a high-pass filtering as shown in Fig. 2.3.

Intuitively this will work, but based on [22] it will now be shown that the first order system in Fig. 2.6 provides the same DT frequency domain transfer function as the traditional modulator with feedback. Consider the frequency domain description of the modulator with feedback in Fig. 2.7.

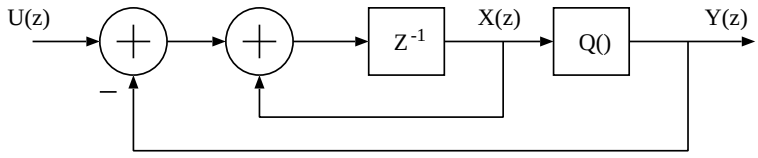

Figure 2.7: First order modulator with feedback

In the figure, Q() represents Z-transformed DT quantizer. The quantizer input is clearly given as:

$$X(z) = \frac{Z^{-1}}{1 - Z^{-1}}(U(z) - Y(z)). \tag{2.12}$$

The modulator output is thus given as:

$$Y(z) = Q\left[\frac{Z^{-1}}{1 - Z^{-1}}U(z) - \frac{Z^{-1}}{1 - Z^{-1}}Y(z)\right]. \tag{2.13}$$

It can be shown [21] that since the output $Y(z)$ has already been quantized, the quantization leaves the last term unchanged and thus $Y(z)$ can be written as:

$$Y(z) = Q\left[\frac{Z^{-1}}{1 - Z^{-1}}U(z)\right] - \frac{Z^{-1}}{1 - Z^{-1}}Y(z) \tag{2.14}$$

or after a rewriting as:

$$Y(z) = (1 - Z^{-1})Q\left[\frac{Z^{-1}}{1 - Z^{-1}}U(z)\right]. \tag{2.15}$$

According to this equation, the transfer function for the first order modulator in Fig. 2.7 could as well be obtained from the modulator shown in Fig. 2.8.

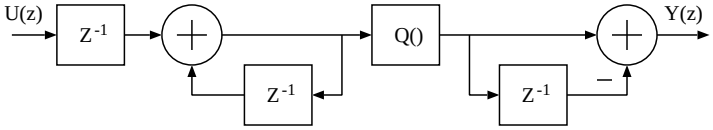

Figure 2.8: Modulator with transfer function as the first order modulator with feedback

It is clear that the system in Fig. 2.8 includes an integrator a quantizer and a differentiator as shown in Fig 2.6. The only difference is the delay at the input, which has no influence on the output spectrum of the modulator without feedback, and thus the modulator without feedback will behave like the traditional modulator with feedback. A similar proof can be made from the CT modulator [21].

Also modulators with an order higher than one can be made without feedback. In the feedback modulator the output of a second order single loop modulator seen in Fig. 2.9 is given as:

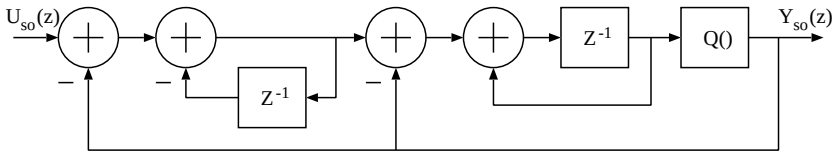

Figure 2.9: Second order modulator with feedback

$$Y_{so}(z) = Q\left[\left(\frac{U_{so}(z) - Y_{so}(z)}{1 - z^{-1}} - Y_{so}(z)\right)\frac{Z^{-1}}{1 - Z^{-1}}\right]. \tag{2.16}$$

which can be rewritten into:

$$Y_{so}(z) = (1 - Z^{-1})^2 Q\left[\frac{z^{-1}U_{so}(z)}{(1 - z^{-1})^2}\right]. \tag{2.17}$$

This transfer function can be implemented as shown in Fig. 2.10. It is thus seen that the second order modulator can be implemented without feedback by cascading to integrators, quantize the result and differentiate it twice. A few implementations of higher order modulators have been made with quite complex multi-stage implementations [11] [13] [23] [24] [49]. Published measurement results are however very few.

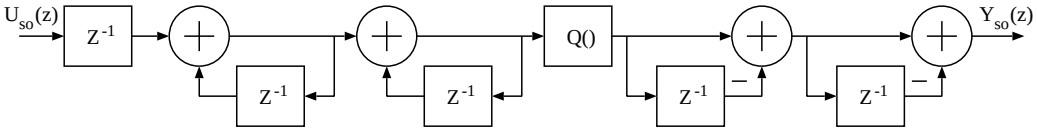

Figure 2.10: Modulator with transfer function as a second order modulator with feedback

Chapter 3

Modeling of noise

In this chapter noise models for different building blocks are examined based on noise models for the single components. The noise models are to be used mainly in chapter 4.

3.1 Noise in combined blocks

Descriptions of the noise in the basic passive and active components are found in appendix B. In this section the noise in the operational amplifier and the comparator will be examined as larger blocks consisting of the components described in the appendix. A number of assumptions are made to simplify the noise calculations.

3.1.1 Noise in operational amplifier

In order to compare the power efficiency of different types of converters, the circuit descriptions will not be detailed, and thus an opamp is always defined as a folded cascode opamp in all circuits, even if another type of amplifier could be a better solution in some of the converters. The folded cascode amplifier with input referred noise sources applied to the MOS transistors can be seen in Fig. 3.1 [6]

Because of symmetry reasons, the noise considerations can be made for one half of the amplifier. The amplifier in Fig. 3.1 is the differential version, in the single ended version V_{B4} is a mirroring of the source voltage of transistor Q_5. It is directly seen, that the noise result will be the same for both circuits.

The load at node X is denoted R_x and at the output node it is denoted R_o, and g_{mx} is the transconductance for transistor Q_x. For symmetry reasons $g_{m1} = g_{m2}$, $g_{m3} = g_{m4}$, $g_{m5} = g_{m6}$ and $g_{m7} = g_{m8}$.

Transconductances are maximized when the MOS transistors are operated in

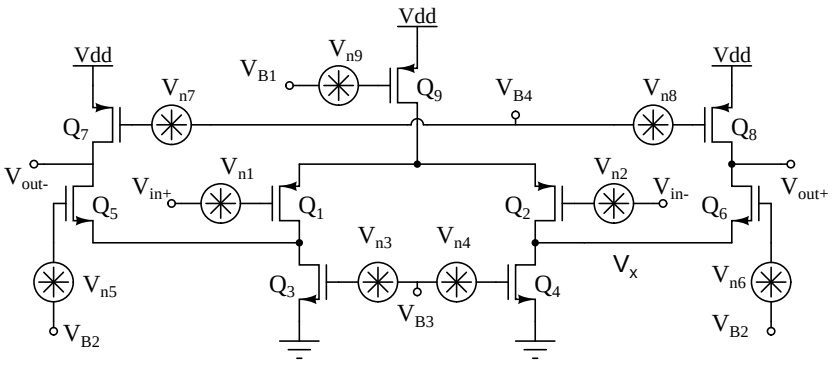

Figure 3.1: Folded cascode amplifier with noise sources applied to the MOS transistors

weak inversion where the gate source voltage biasing the transistor, is below the threshold voltage of the transistor. If the width of a transistor biased with a fixed bias current is increased it will eventually be in the subthreshold region. In this region the transconductance becomes independent of transistor dimensions. The transconductance for a transistor biased in this region is:

$$g_m = \frac{I_D}{nV_T} \tag{3.1}$$

where n is a fitting factor around 1.5 and V_T is the thermal voltage which equals 26 mV at room temperature. The contribution to total input referred amplifier noise from the different transistors in the amplifier is found by calculating the output noise current due to a specific transistor and divide it by the total gain of the amplifier. The contribution from the input transistors Q_1 and Q_2 is given from (3.2). It is calculated as the input referred voltage noise of transistor Q_2, multiplied by g_{m2} which is a noise current giving the small signal gate source voltage of transistor Q_6 when multiplied by R_x. The gate source voltage is multiplied with g_{m6}, and the output noise current due to transistor Q_2 is found. This current is multiplied by R_o to give the output noise voltage.

$$\left|\frac{V_{no+}}{V_{n2}}\right| = g_{m2}R_x g_{m6}R_o. \tag{3.2}$$

Because V_{n2} is at the input node, the factor given in (3.2) is also the total gain of the amplifier. The noise V_{n9} modulates the bias current in the input stage. The influence is negligible compared to the rest of the sources [27] and will not be discussed further. The contribution from the cascode transistor Q_6 is illustrated with the small signal model in Fig. 3.2.

By using KCL the noise output current can be found as:

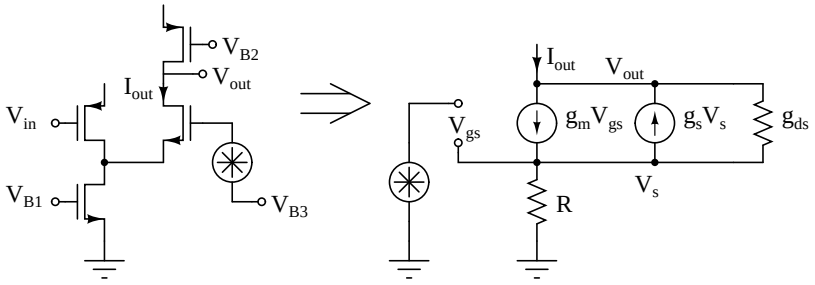

Figure 3.2: Deduction of a small signal model to examine the noise from the cascode transistor

$$i_n = \frac{g_m V_n + V_o g_{ds}}{1 + g_m R + g_s R + g_{ds} R} \approx \frac{g_m V_n}{1 + g_m R} \approx \frac{V_n}{R}. \tag{3.3}$$

Since R is high, the noise from the cascode transistor can be neglected. The noise contributions from the rest of the transistors is found with the same method as explained above to (3.2).

$$\left| \frac{V_{no+}}{V_{n4}} \right| = g_{m4} R_x g_{m6} R_o \tag{3.4}$$

$$\left| \frac{V_{no+}}{V_{n8}} \right| = g_{m8} R_o. \tag{3.5}$$

The total equivalent noise at the input is then found from (3.2), (3.4) and (3.5).

$$V_{eq-}^2(f) = V_{n2}^2(f) + \left(\frac{g_{m4}}{g_{m2}} \right)^2 V_{n4}^2 + \left(\frac{g_{m8}}{g_{m2} R_x g_{m6}} \right)^2 V_{n8}^2. \tag{3.6}$$

R_x is dominated by the input resistance of the cascode stage, and it is assumed that $R_x \approx 1/g_{m6}$. The noise on the positive input terminal is the same as on the negative input terminal, and the total differential input referred noise is twice the noise given in (3.6) [31].

$$V_{eq}^2(f) = 2V_{n1}^2(f) + 2 \left(\frac{g_{m3}}{g_{m1}} \right)^2 V_{n3}^2 + 2 \left(\frac{g_{m7}}{g_{m1}} \right)^2 V_{n7}^2. \tag{3.7}$$

In appendix B it is shown that the noise coming from a MOS transistor consists of two parts, a white noise contribution and a 1/f noise contribution with spectral densities given as:

$$V_{wnm}^2 = 4kT\gamma \frac{g_{d0}}{g_m^2} \approx 4kT\gamma \frac{1}{g_m} \tag{3.8}$$

$$V_{fnm}^2 = \frac{K_f}{2C_{ox}^2 \mu W L f} \tag{3.9}$$

where values for K_f, C_{ox}, γ and μ are process parameters found in the process description and k is Boltzmanns constant. These two noise types leads to the two input referred spectral densities:

$$V_{weq}^2(f) = 8\gamma kT\left(\frac{1}{g_{m1}} + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \frac{1}{g_{m3}} + \left(\frac{g_{m7}}{g_{m1}}\right)^2 \frac{1}{g_{m7}}\right) \tag{3.10}$$

$$V_{feq}^2(f) = \frac{1}{C_{ox}^2 \mu_p f}\left[\left(\frac{K_{fp}}{W_1 L_1}\right) + \left(\frac{2K_{fn}L_1}{W_1 L_3^2}\right) + \left(\frac{K_{fp}L_1}{W_1 L_7^2}\right)\right] \tag{3.11}$$

where it is assumed that Q_1 and Q_7 are biased with the same current giving twice the bias to Q_3.

It is seen, that the input referred noise in the amplifier can be reduced in different ways. One way is to increase the transistor lengths, which will directly decrease 1/f noise. Another solution is to increase g_{m1}. If the transistors are not in deep subthreshold region this can be done through W_1. This solution decreases 1/f noise as well as white noise. If the transistors are in subthreshold region an increased width will not increase g_{m1}, but it will still cause a positive effect on 1/f noise. The only solution reducing white noise in this region is to increase the bias current and thus increase g_{m1}. This solution of course result in an increased power consumption of the stage. Assuming that all transistors have the same length $L_1 = L_3 = L_7$ and that all transconductances are maximized resulting in $g_{m3} = 2g_{m1} = 2g_{m7}$, the 1/f noise and white noise is given from:

$$V_{weq}^2(f) = 32\gamma kT\left(\frac{nV_T}{I_B}\right) \tag{3.12}$$

$$V_{feq}^2(f) = \frac{1}{C_{ox}^2 \mu_p f}\left(\frac{2K_{fp} + 2K_{fn}}{W_1 L_1}\right) \tag{3.13}$$

where I_B is the current biasing Q_1. The required bias current can be found from the maximum allowed noise, and since the folded cascode amplifier has four current branches (3.14) gives the total power consumption of an amplifier, when it is assumed that the prescribed common mode feedback circuit (CMFB) consumes the same amount of power as one of the amplifier branches.

$$P = (4+1)I_B V_{dd}. \tag{3.14}$$

In cases where the amplifier has to supply a current to a load this charging current can be limiting for the bias current required. The amplifier cannot charge with a current larger than the bias current in the differential case.

$$I_B \geq I_{load}. \tag{3.15}$$

3.2 Oscillator noise

The noise produced at the output of an oscillator can be described in either time domain as jitter or in frequency domain as phase noise. In this section both domains are considered since the time domain considerations will be used in the modulator with feedback, where the oscillators performance as a clock generator is explored, whereas the frequency domain considerations will be used in the modulator without feedback, where there is a VCO in the signal path.

3.2.1 Time domain noise

In [54] three types of sampling errors in $\Sigma\Delta$ modulators are considered, related to jitter in the oscillator generating the sampling clock:

- Varying phase lengths which is a non-constant duty cycle on the sampling signal.
- Phase overlap which is when the sampling phase and the hold phase overlap each other e.g. if the hold phase is generated from the sampling phase with an inverter.
- Non-uniform sampling due to jitter on the periods of the sampling signal.

In a low frequency modulator the varying phase lengths are a minor problem, because it can be assumed, that all signals in the modulator have plenty of time to fully settle during the period. In this work only audio frequency modulators are considered, and thus the varying phase is not considered important.

The phase overlap is mainly effective in DT where switched capacitors are used and serious voltage errors according to [54] will be a result of the overlap. In CT the modulator is independent of a hold phase and is thus not subject to noise from the overlapping phases. It is however possible to design non-overlapping clock circuits, which will prevent problems from overlapping phases. In the following it is assumed that non-overlapping clock generators are used. On top of that the overlap time resulting from e.g. an inverter is constant and independent of the clock frequency, meaning that this problem will also be more severe in high frequency applications.

The non-uniform sampling is however relevant in the audio frequency range for both DT and CT modulators, and it is thus important to know the amount of jitter

produced in the oscillator. The output of an oscillator is depending on oscillator phase as [37]:

$$V(t) = V_0 \sin(\omega t + \phi_0). \tag{3.16}$$

The phase consists of an initial phase ϕ_0 and a frequency term ωt. Frequency is seen to be the derivative of phase, and thus the phase at time t is given from:

$$\phi(t) = \int_0^t \omega(t)dt + \phi_0. \tag{3.17}$$

The coherence between the parameters are illustrated in the example shown in Fig. 3.3

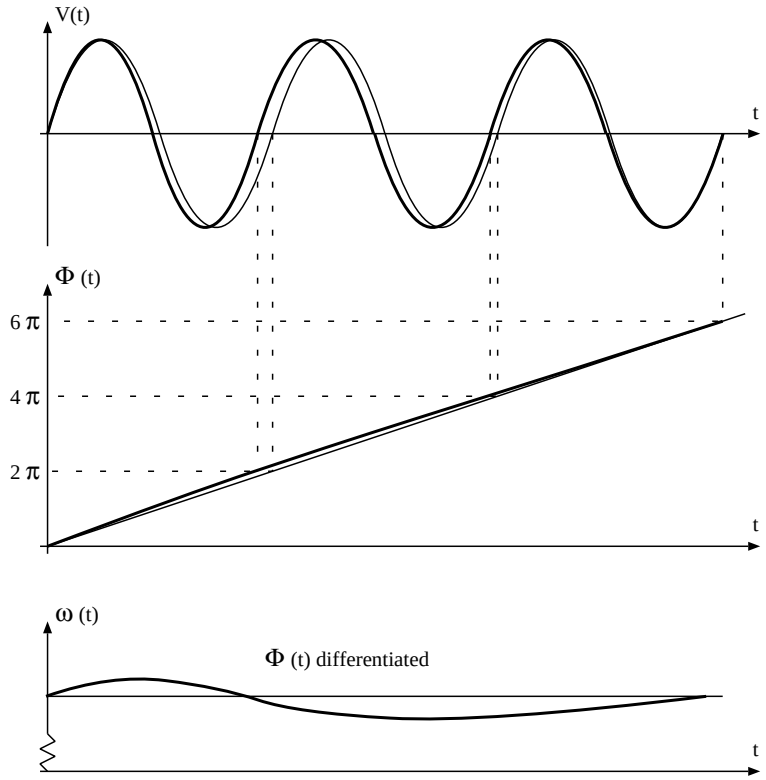

Figure 3.3: The three graphs show the time domain jitter noise, the phase noise and the frequency error illustrated for a sinusoidal signal, but could as well be for a square signal

It is possible to use different types of oscillators having different advantages. These different oscillator types can be separated into two groups, the LC based sinusoidal oscillators and the nonlinear square signal oscillators such as the inverter

ring oscillator. By using the theory of Hajimiri [18] [32] it is seen, that the LC oscillator has noise performances superior to those of the inverter ring oscillator for a given power consumption, but the ring oscillator does not need inductors, which makes it much more suitable in modern CMOS processes. This suitability is especially the case at low frequencies where the LC based oscillators require a large inductance according to the oscillation frequency given as:

$$\omega_0 = \frac{1}{\sqrt{LC}}. \tag{3.18}$$

The ring oscillator in Fig. 3.4 consists of an odd number of inverters placed in a ring. Due to the 180^o phase change and the time delay in each of the inverters, a transition flank will start to circulate around the loop, when the odd number of inverters is higher than one. This oscillator type only consists of inverters and it can be implemented in all standard CMOS processes. It do not require start up circuits, and it can be designed to operate at high as well as low frequencies and even with the transistors biased in the weak inversion region. It is the oscillator used in this work.

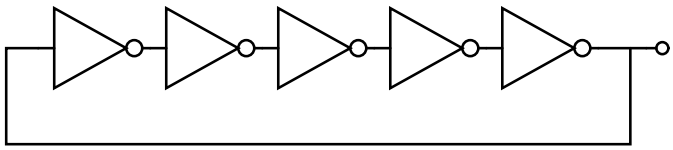

Figure 3.4: The Inverter ring oscillator consisting of an odd number of inverters

The noise in an oscillator consists of coupling noise through the substrate or connections such as power supply, and the inherent thermal and shot noise of the components in the oscillator [56]. The coupling noise can to some extent be removed by a robust layout, for example by shielding with guard rings and with separate supply voltages in the chip. The inherent noise is assumed consisting of uncorrelated noise sources, and the standard deviation is according to [9] [19] given as:

$$\sigma_{\Delta T} = \kappa\sqrt{\Delta T}. \tag{3.19}$$

It is seen that the standard deviation is given as a function of the measurement delay ΔT, which is the time from a reference flank to the time where the jitter is measured. Intuitively it is also clear that the time error on a flank will be larger, if it is referred to a flank 1000 periods earlier than to a flank 2 periods earlier. This is illustrated in Fig. 3.5, where the line in the middle is the ideal noise free signal, and the hatched region is the $1\sigma_{\Delta T}$ region of the output signal with noise.

κ in (3.19) is a proportionality constant examined by Hajimiri [19]. In his work κ is found using the impulse sensitivity function, and the minimum value assuming a perfect symmetrical oscillator is:

$$\kappa = \sqrt{\frac{16\gamma}{3\eta}} \cdot \sqrt{\frac{kT}{P_{jit}}} \tag{3.20}$$

where k is Boltzmanns constant, T is the absolute temperature, P_{jit} is the power supplied to the oscillator, γ is 2/3 in a long channel approximation and η is a proportionality constant approximately equal to 1. With these constants κ is $1.21 \cdot 10^{-10} \cdot \sqrt{1/P_{jit}}$. This result is supported from simulations, and thus paper 2 contains an error when explaining that this value does not fit simulations.

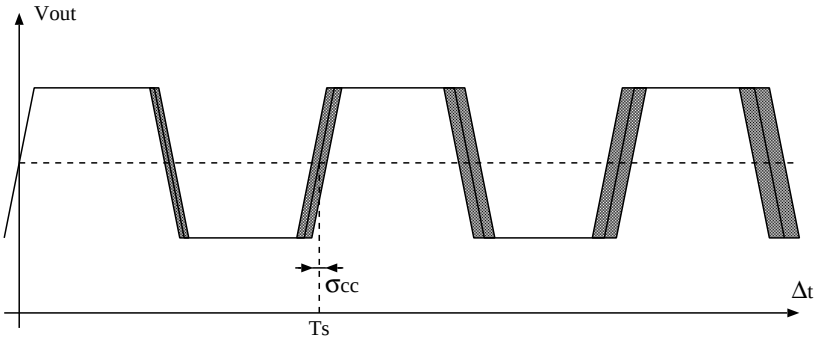

Figure 3.5: Illustration of jitter noise at the output of a square signal oscillator

It is important to realize what ΔT values to use. When the number of periods considered is small, the jitter only makes sense at the transitions. When the number of periods is large, one clock period becomes small compared to the total ΔT. Two types of clock jitter can be derived [58] [61]. One type is the cycle-to-cycle jitter shown as σ_{cc} in Fig. 3.5 and it is calculated from (3.19) with $\Delta T = T_s = 1/f_s$. The other type is the absolute clock jitter, where ΔT is multiples of T_s going towards a non-quantized ΔT when the time is much larger than T_s.

According to (3.19) the noise standard deviation can be calculated as a function of the power supplied to the oscillator, both as absolute clock jitter and as cycle-to-cycle jitter given as:

$$\sigma_{cc} \approx 1.21 \cdot 10^{-10} \cdot \sqrt{\frac{1}{P_{jit} f_s}}. \tag{3.21}$$

This equation will be used in chapter 4 where it is explained how the jitter couples in DT and CT $\Sigma\Delta$ modulators.

3.2.2 Frequency domain noise

All oscillators include noisy components. In the LC based oscillators the inductor and the capacitor are noiseless, but the loss (resistance) in the tank will produce white $4kTR$ noise. Furthermore the negative resistance sustaining the oscillation in the tank is usually obtained from biased transistors producing both white noise and 1/f noise. This is also the case in the ring oscillator, where all of the transistors in the ring are noisy.

Depending on where during the oscillation period the noise is injected, it will influence the system differently [32]. If it is injected near a zero crossing, it will result in a phase change and phase noise arises. If it is injected near a maximum or a minimum, it will result in amplitude noise. The latter situation is however usually compensated by an amplitude limitation in the oscillator, and thus only phase noise is important.

This noise is up-converted to the frequencies around the carrier frequency of the oscillator, a topic explored in [33]. In this work it is shown, how the noise currents are converted into voltages through the tank impedance, which is proportional to $1/\Delta\omega$, where $\Delta\omega$ is the frequency deviation from the carrier. The result is, that $1/f$ noise power is up-converted to $1/f^3$ noise, and the white noise is converted to $1/f^2$ noise, a fact that holds for the ring oscillator as well [18]. This result is also obtained if the oscillator is seen as a noiseless VCO, where $1/f$ and white noise are added at the input. In this case the phase output includes an integration of the input voltage. Using Laplace the integration results in $1/s$ ($s = j\omega$) and a proportionality as in the impedance evaluation is obtained. This is illustrated in Fig. 3.6.

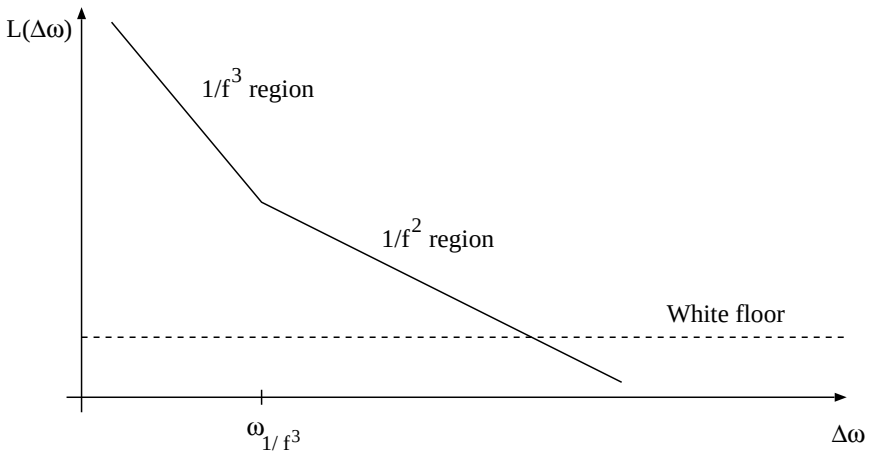

Figure 3.6: Phase noise spectrum around carrier

In the range with up-converted 1/f noise, the noise decreases 30dB/decade. Where up- (and down-) converted white noise dominates, the slope is 20dB/decade. This slope cannot decrease forever. All noise contributors following the oscillator such as buffers or resistances in the connections will not be converted, and thus the noise flattens out in the white noise floor shown with the dashed line in Fig. 3.6. It should be mentioned, that it has been shown in [18] that ω_{1/f^3} do not equal the 1/f corner directly, but is given from the so-called impulse sensitivity function (Γ), which is a time varying function, telling how a noise impulse will impact the output at a given time. The ω_{1/f^3} corner is then given from the DC and RMS value of Γ as:

$$\omega_{1/f^3} = \omega_{1/f} \frac{\Gamma_{DC}^2}{4\Gamma_{RMS}^2} \tag{3.22}$$

Phase jitter $\sigma_{\Delta\phi}$ is related to time jitter $\sigma_{\Delta T}$ as [19]:

$$\sigma_{\Delta\phi} = 2\pi \frac{\sigma_{\Delta T}}{\Delta T} = \omega_0 \sigma_{\Delta T} \tag{3.23}$$

Chapter 4

Power consumption and stability of single-loop $\Sigma\Delta$ modulators with feedback

In this chapter the $\Sigma\Delta$ modulator with feedback is considered, and the power consumptions of CT and DT $\Sigma\Delta$ converters are compared. In both cases the noise produced in the modulator is a function of the power consumption. Dependency to clock oscillator jitter is different in the two types of modulators, and therefore the power consumed by the oscillator producing the jitter is included. The power consumption of the digital decimation filter following the modulator is also included whereas impact from reference sources is assumed to be equal in both cases which is why they are not included in the comparison.

This type of modulator can be unstable, and therefore the comparison above has no relevance if the stability is not considered and this is why the stability is the first topic treated.

4.1 Stability of the feedback modulator

This modulator was presented in section 2.3 where it is seen, that it is stabilized in a regulation system with a negative feedback loop. It is known, that a higher order modulator (where higher order means at least 3) can be driven into instability [53]. Due to the quantization the system is nonlinear, and thus the usual stability analysis can be problematic. The analysis presented here has previously been presented in [28], [39], [50] and [51] and it is an extension of the work in [2]. It is carried out for a modulator in DT, but the result will be applicable for its CT equivalent. The

modulator is assumed to be quantized single-bit, and thus all signals are normalized to quantizer output stages of +1 and -1.

To be able to analyze the stability, a linear quantizer model is needed. In Fig. 2.4 a very simple model is used. This model is however not sufficient for the analysis, and thus it is replaced by the quantizer model in Fig. 4.1

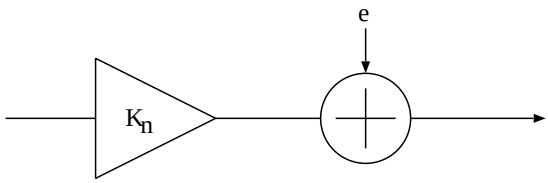

Figure 4.1: Linearized quantizer model

The difference between this model and the previous is the noise gain K_n, resulting in the modulator model in Fig. 4.2. S_{TF} and N_{TF} are therefore changed into:

$$S_{TF} = \frac{K_n H}{1 + K_n H} \tag{4.1}$$

$$N_{TF} = \frac{1}{1 + K_n H} \tag{4.2}$$

which is however not changing the functionality described in section 2.3 due to infinite DC gain of H.

Due to the noise shaping nature of the modulator the signals and the value for K_n will never settle, but it is possible to find equilibrium points for these signal and for K_n in the quantizer, where the equilibrium value will be the long term statistical average value. The equilibrium value for K_n is the value that will minimize the variance of the error at the output of the modulator. In the analysis all signals are

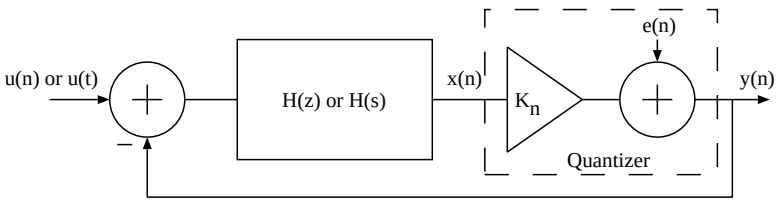

Figure 4.2: ΣΔ modulator model with quantizer from Fig. 4.1

separated into two parts. First part is m_u, m_x, m_e and m_y or $E[u]$, $E[x]$, $E[e]$ and $E[y]$ where $E[z]$ denotes the mean value of the signal z. This part is modulated by the DC part of K_n (K_{DC}). The second part is σ_u, σ_x, σ_e and σ_y which is the deviation for signal u, x, e and y modulated by the AC part of K_n (K_{AC}).

Due to the high OSR, the input signal can be seen as a DC signal with $\sigma_u = 0$. It is also remembered that H is an integration meaning that in a stable modulator in equilibrium its input signal can not contain a DC component, and thus it is required that:

$$m_u = m_y. \tag{4.3}$$

m_e is minimized to 0 by a K_{DC} value of:

$$K_{DC} = \frac{m_y}{m_x} = \frac{m_u}{m_x}. \tag{4.4}$$

This part takes care of the signal and will not influence stability, which is thus investigated through the AC values. This means, that in this analysis DC values are signals, and AC values are noise.

The AC signal is introduced in the quantizer through the quantization noise having a deviation of σ_e. This is however not the only noise found at the output, due to the feedback path a weighted part of the quantization noise from previous samples will be added to the output noise σ_y and thus $\sigma_y \geq \sigma_e$. Therefore it is possible to find a fixed amplification of the noise for the equilibrium situation. The noise amplification factor A is defined as:

$$A \equiv \frac{\sigma_y^2}{\sigma_e^2}. \tag{4.5}$$

The noise at the output is given from the quantization noise multiplied with N_{TF} based on Fig. 4.1. This means, that σ_y, which does not contain any signal information, is given as:

$$\sigma_y^2 = \sigma_e^2 \int_{-f_s/2}^{f_s/2} |N_{TF}(f)|^2 df \tag{4.6}$$

in CT, or its DT equivalent. From a given modulator the integrator or filter in the loop H is known. This means, that only K is unknown, which means that using (4.5) and (4.6) A is given as a function of K from:

$$A(K) = \int_{-f_s/2}^{f_s/2} |N_{TF}(f, K)|^2 df \tag{4.7}$$

or by using Parseval's theorem if preferred, it can be expressed through the DT impulse response as:

$$A(K) = \sum_{n=0}^{n=\infty} n_{tf}^2(n, K). \tag{4.8}$$

$A(K)$ is plotted in Fig. 4.3 for a second order and a third order filter. It is seen, that for the second order filter the curve is monotonically increasing which is also

the case if the first order loop filter is plotted. For the third order filter the curve is ∪-convex, which is the case for all higher order modulators. It is also seen, that the $A(K)$ curve is extremely sensitive to the N_{TF} cut-off frequency f_{co} with a minimum value increasing with an increased f_{co}. This is true for all modulator orders above one.

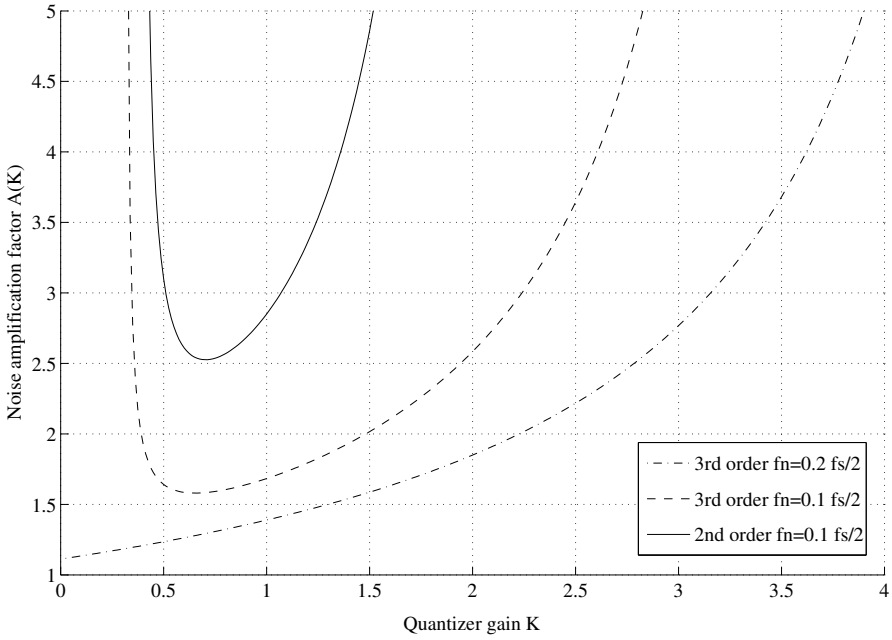

Figure 4.3: Noise amplification factor A versus gain factor K for second and third order modulators

A can also be expressed from the input signal m_u. To do this two more expressions for σ_y are needed. First an expression is found from the definition of variance [29]:

$$\sigma_y^2 \equiv E[(y - Ey)^2] = E[y^2(n)] - E^2[y(n)] = 1 - m_y^2. \tag{4.9}$$

This result is obtained since the quantizer can only provide ± 1. The second expression can be obtained from x and e:

$$\sigma_y^2 = K^2\sigma_x^2 + \sigma_e^2. \tag{4.10}$$

Covariance between x and y is defined as [29]:

$$Cov(x, y) \equiv E[(x - Ex)(y - Ey)] = E[(x - Ex)(Kx + e - E(Kx + e))]. \tag{4.11}$$

Due to the fact that $m_e = 0$ the following result, which is in agreement with [2], occurs:

$$Cov(x, y) = E[Kx^2] - E[x]E[Kx] = K\sigma_x^2. \tag{4.12}$$

By isolating K in (4.12), apply it to (4.10) and use (4.9) the following equation for σ_e^2 can be obtained:

$$\sigma_e^2 = 1 - m_y^2 - \frac{Cov^2(x,y)}{\sigma_x^2}. \tag{4.13}$$

The last term in (4.13) is dependent on the distribution assumed for x. In [51] different distributions are examined, and if gaussian distribution is assumed, (4.13) can be written as:

$$\sigma_e^2 = 1 - m_y^2 - \frac{2}{\pi} exp\left[-2\left(erf^{-1}(m_y)\right)^2\right] \tag{4.14}$$

where erf is the error function (see e.g. [29]). It is now seen that σ_y^2 according to (4.9) can be expressed only through m_y as well as σ_e^2 according to (4.14). $m_u = m_y$ and thus when assuming gaussian distribution of the noise, A can be expressed from m_u as:

$$A(m_u) = \frac{1 - m_u^2}{1 - m_u^2 - \frac{2}{\pi} exp\left[-2\left(erf^{-1}(m_u)\right)^2\right]}. \tag{4.15}$$

The $A(m_u)$ is independent of modulator type, and thus there exists only one curve which is the one seen in Fig. 4.4.

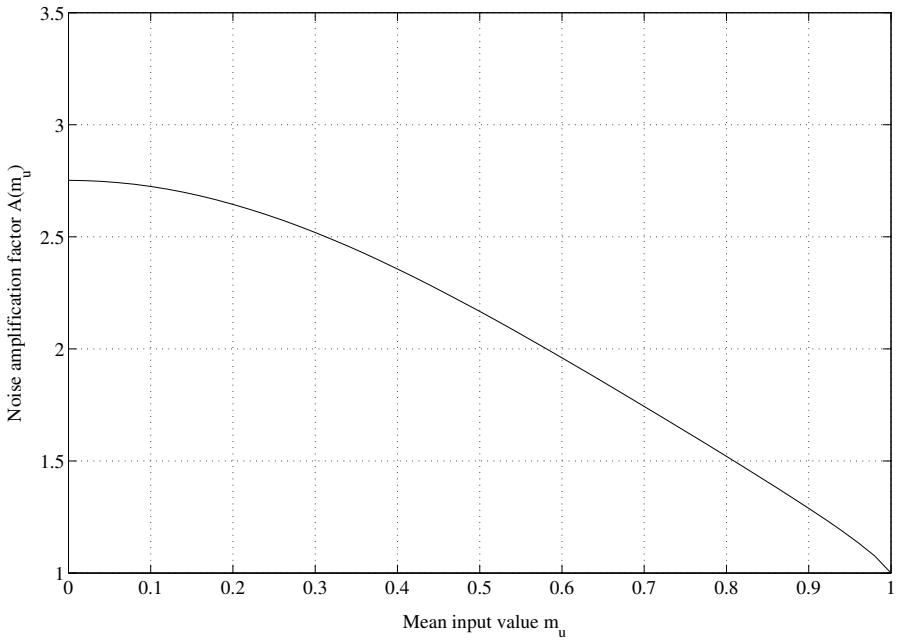

Figure 4.4: Noise amplification factor A versus input mean signal m_u true for all modulators

Due to the high OSR input signals are seen as DC values with each their equilibrium points. The equilibrium point for A is found for a given input value regardless

of modulator type. With the A value an equilibrium point for K can be found for a specific modulator from Fig. 4.3.

The question is how it relates to stability. Assume that a stable modulator has an input signal m_u at a specific point of time. According to (4.15) and Fig. 4.4 this will lead to an equilibrium noise amplification A between 1 and 2.752. According to Fig. 4.3 this will result in 0, 1 or 2 values for the quantizer gain K depending on modulator order and f_n. It can be shown [51] that stable equilibrium points are found at the part of the $A(K)$ curve with positive slope. When m_u is increased, A is reduced as well as K. This can continue until $m_u = 1$ or A reaches its minimum. If m_u from this point is increased further, the modulator will not have an equilibrium point, and is thus not providing a meaningful output. The maximum m_u that has an equilibrium point is named maximum stable amplitude (MSA).

For second order modulators, an equilibrium point is re-found when m_u returns below MSA. This is not the case if the modulator order is higher than two since the equilibrium point will escape on the part of the $A(K)$ curve with negative slope, and a reset is needed. It is also seen, that if f_n is increased, MSA is reduced, and it will at some point reach 0. At this point, the modulator will be unstable even without signal at the input.

4.2 Noise in the discrete time ΣΔ modulator

To examine the noise produced in a DT ΣΔ modulator, the switched capacitor modulator is assumed. In Fig. 4.5 a block diagram of a single ended 4^{th} order ΣΔ is seen. The model is made for the differential counterpart. In this section models will be derived in order to describe the dependencies between noise produced in the modulator and the power consumed by the modulator, taking stability into account. This means, that both signal and noise and thus the SNR in a given modulator can be found. The aim of the model is to predict the optimal modulator with given SNR and conversion band requirements.

Assume that a set of requirements are given for the modulator in terms of SNR or a number of effective bits which can be calculated into SNR according to (2.2). SNR is per definition given from the signal power and the noise power. The signal power is dependent on MSA calculated according to the stability analysis given in the previous section, where it was found that MSA is given from the modulator order and the cut-off frequency of N_{TF}. The MSA is referred to the linear reference voltage range $V_{ref} = K_r \cdot (V_{dd} - V_{ss})$ of the modulator. This voltage range is lower than the supply voltage, but because the implementation is assumed to be a switched

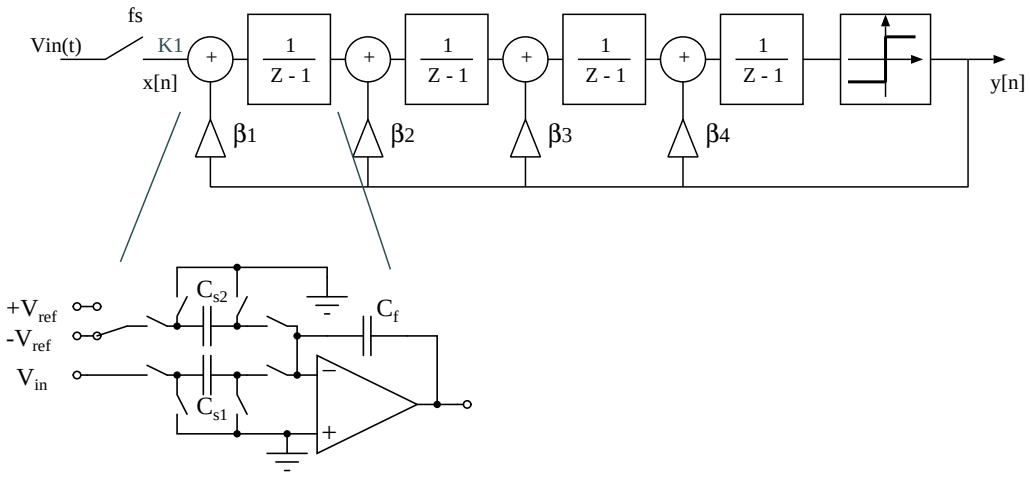

Figure 4.5: Block diagram of 4^{th} order ΣΔ modulator and schematic of one single ended integration stage.

capacitor implementation, the reference voltage is expected to be close to $(V_{dd} - V_{ss})$ (K_r close to unity). The largest allowed peak to peak input signal amplitude is then given as:

$$V_{in} = MSA \cdot K_r \cdot V_{dd}. \tag{4.16}$$

The input signal amplitude voltage with $K_r = 0.8$ for MSA=1 and MSA=0.5 is illustrated in Fig. 4.6.

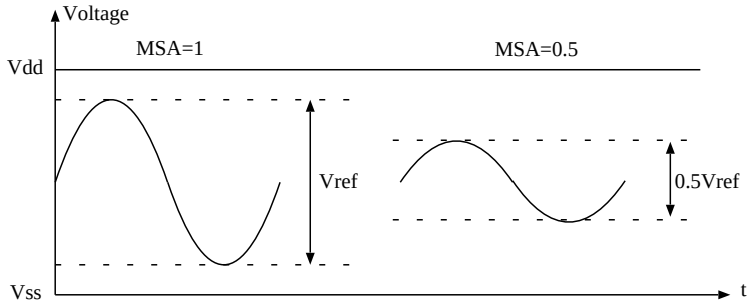

Figure 4.6: Allowed sinusoidal input voltage with MSA=1 and MSA=0.5

In the rest of this section $V_{ss} = 0$ is assumed to simplify the equations. The signal power of the sinusoidal signals in Fig. 4.6 is given from:

$$S_s = \left(MSA \frac{K_r \cdot V_{dd}}{2\sqrt{2}} \right)^2. \tag{4.17}$$

This means that for a given modulator order, a signal power vector can be calculated from a vector of f_{co}. Because of the requirement to SNR, the total noise budget can

be calculated:

$$N_{tot} = \frac{S_s}{10^{\frac{\text{SNR}}{10}}}. \tag{4.18}$$

First of all the noise budget consists of the shaped quantization noise N_q which is always present in a converter. If the total quantization noise is assumed to have a white distribution, the power of the noise in the complete signal band up to the sampling frequency f_s is [27]:

$$N_{qfs} = \frac{1}{12 f_s} \left(\frac{V_{ref}}{2} \right)^2. \tag{4.19}$$

In the modulator this noise is however shaped according to the N_{TF}, which is a high-pass filter. The filter transfer function is controlled by the feedback coefficients in the modulator. In this work it is assumed, that the N_{TF} is implemented as a Butterworth filter. In a complete converter the modulator will be followed by a decimation filter. If a perfect brick-wall low-pass decimation filter with a cut-off frequency of f_b is assumed, the quantization noise at the output is [27]:

$$N_q = \frac{1}{12 f_s} \int_0^{f_b} N_{TF}(f) \, \mathrm{d}f \left(\frac{V_{ref}}{2} \right)^2. \tag{4.20}$$

Besides quantization noise the noise in the modulator consists of noise arising internally in the modulator N_{int} and external noise coupled mainly through the supply voltage, reference voltage and clock signal but also through cross coupling and substrate coupling. The cross and substrate coupling can be greatly reduced with a careful design, and they will not be included in this model. The supply and reference voltage coupling is left out as well since the models are made to compare the DT solution to the CT solution, where the supply and reference voltages will influence both modulators with the same effect. Furthermore we have no control of externally supplied voltages, and they are thus assumed to be of a high enough quality to be disregarded in the total noise. The influence from the clock signal N_{jit} is however much different in DT and CT, and is thus included. The total noise budget from (4.18) is:

$$N_{tot} = N_q + N_{int} + N_{jit} \tag{4.21}$$

4.2.1 Internal noise

The internal noise N_{int} is produced by the amplifiers in the integrators and the switched capacitors. Noise produced in the different integrators does not contribute equally to the noise at the output of the modulator. The noise is shaped according to the stage, in which it is injected. Assume that the input referred noise produced

by the amplifier and switched capacitors is n_1 from the first integrator and n_2 from the second integrator in the second order modulator illustrated in Fig. 4.7:

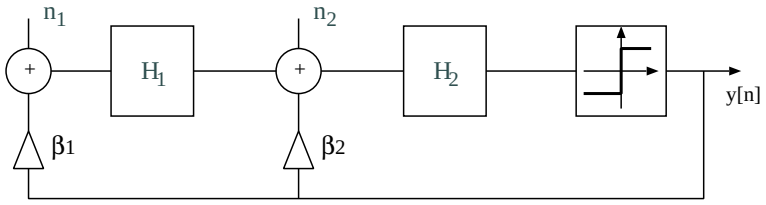

Figure 4.7: Noise injected from first and second stage in a second order modulator

Noise transfer functions for n_1 and n_2 is found as:

$$\frac{y}{n_1} = \frac{H_1 H_2}{1-\beta_2 H_2 - \beta_1 H_1 H_2} \tag{4.22}$$

$$\frac{y}{n_2} = \frac{H_2}{1-\beta_2 H_2 - \beta_1 H_1 H_2} \tag{4.23}$$

The transfer functions H_x are integrators (1/(Z-1)), and it is clearly seen from the equations that n_1 is not shaped which is not a surprise since it adds to the same node as the input signal. It is also seen from the transfer functions, that n_2 is first order shaped. This investigation can be done for higher order modulators as well, where it turns out that the order of noise shaping increases by 1 for each stage in the modulator.

Due to this noise shaping the first stage will be the major noise contributor, or else the power consumption as well as input transistor sizing can be scaled down in the internal stages. The latter of the possibilities is a commonly used technique, and is the one implemented in this model. It can be shown [39] that all stages will contribute equally if the power of stage number ST is scaled as:

$$\text{Scale} = \frac{1}{2\text{ST}-1}. \tag{4.24}$$

Capacitors are noiseless components, but the capacitors C_{s1} and C_{s2} in Fig. 4.5 are charged through the resistive channel in a MOS transistor, and (see also (B.3)) a capacitor C_x produces the noise:

$$N_c = \frac{kT}{C_x}. \tag{4.25}$$

The noise calculated from this equation is the total RMS noise from the RC connection. This noise is assumed to be white and distributed over the complete sampling bandwidth f_s, and the noise spectral density for the fully differential solution is given as [36]:

$$N_{cs}(f) = \frac{8kT}{f_s}\left(\frac{1}{C_{s1}} + \frac{1}{C_{s2}}\right). \tag{4.26}$$

Scaling is usually applied to the feedback factors β in Fig. 4.5 so that β_1 is unity [28] which makes $C_{s1} = C_{s2} = C_s$ in the first integration stage. The total RMS noise from the switched capacitors is found from an integration in the conversion band f_b resulting in:

$$N_{cs} = \frac{16kTf_b}{C_s f_s} \tag{4.27}$$

The other part of the internal noise originates from the transistors in the amplifiers. This noise contribution was found from the derivation in section 3.1.1, where the white noise and the 1/f noise of the amplifier is found with some transistor sizing assumptions in (3.12) and (3.13). The white noise contribution is controlled by the power consumed by the amplifier, whereas the 1/f noise is only dependent on transistor sizing.

The amplifiers are in a feedback loop, and therefore the referred input noise is amplified with the impact of these noise contributions as illustrated in Fig. 4.8

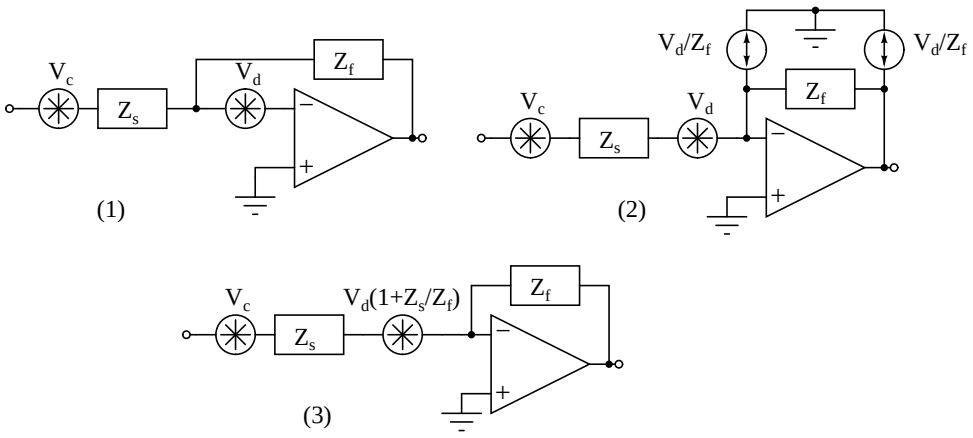

Figure 4.8: The impact from capacitor and amplifier noise on the total modulator input noise. V_d includes both white and 1/f noise and the MOS input impedance is assumed to be extremely high

The summation in Fig. 4.8 is true because the noise sources are indeed correlated since they originate from the same noise source V_d. The two loads Z_f and Z_c are respectively the integration capacitance C_f and the parallel connection of C_{s1} and C_{s2}.

$$N_d = \left(V_{weq}^2 + V_{feq}^2\right)\left(1 + \frac{Z_s}{Z_f}\right)^2 \tag{4.28}$$

The relation between capacitors C_f and C_s controls the unity gain bandwidth of the integrators and thus also the poles in the N_{TF}. When the gain of the feed

forward path on the modulator becomes lower than one, the quantization noise is no longer suppressed. To a certain degree of approximation it can be assumed, that f_{co} equals the unity gain frequency of the integrators. Using this it can be shown, that the amplification of the noise is:

$$N_d = \left(V_{weq}^2 + V_{feq}^2\right)\left(1 + \frac{1}{2f_n}\right)^2 \tag{4.29}$$

4.2.2 Jitter noise contribution

The third noise contribution in equation 4.21 is the noise introduced from the oscillator jitter discussed in section 3.2.1. The time domain jitter noise is converted into a voltage noise when sampled at the input. This noise type is illustrated in Fig. 4.9.

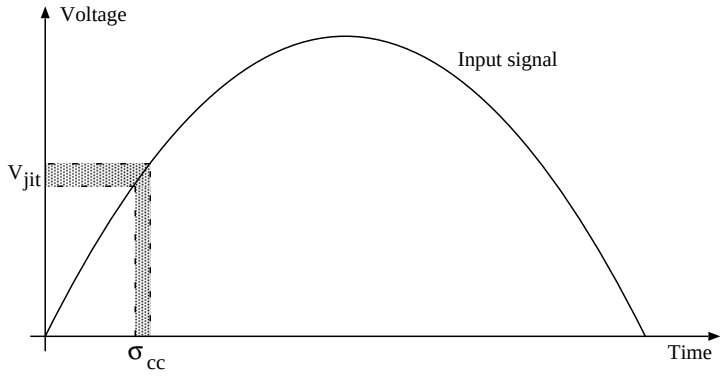

Figure 4.9: Time domain jitter noise to voltage noise conversion

The jitter noise in the modulator is found as the voltage deviation caused by the oscillator clock to clock jitter σ_{cc} (3.19). Assuming a sinusoidal input voltage, the noise voltage is:

$$V_{jit} = \sigma_{cc}\frac{dV_{in}}{dt} = \sigma_{cc}\frac{d(A\sin(\omega t))}{dt} = \sigma_{cc}\omega A\cos(\omega t) \tag{4.30}$$

It is seen, that a higher input frequency or a higher amplitude will result in increased jitter noise. To get the worst case jitter noise, the values used are thus $(MSA{\cdot}V_{ref})/2$ as amplitude, and $2\pi f_b$ as ω. According to the simulations in paper 2 it is a fair assumption that the noise produced is white. The noise will be in the range up to $f_s/2$ and thus integration over the conversion band leading to the jitter noise power in (4.21) is just $2f_b/f_s$:

$$N_{jit} = \frac{16\gamma}{3\eta}\cdot\frac{kT}{f_s P_{jit}}\cdot\left(2\pi f_b\cdot\frac{MSA\cdot V_{ref}}{2}\right)^2\frac{2f_b}{f_s}. \tag{4.31}$$

Insertion of the numbers found in section 3.2.1 results in:

$$N_{jit} = \left(1.2 \cdot 10^{-10}\right)^2 \frac{1}{f_s P_{jit}} \left(2\pi f_b \cdot \frac{MSA \cdot V_{ref}}{2}\right)^2 \frac{2f_b}{f_s}. \tag{4.32}$$

4.3 Power consumption in the discrete time ΣΔ modulator

The equations leading to the required SNR are now known, and the next step is to find the relations between noise in the different blocks and their power consumption. In this way it is possible to optimize power in each block within the limits of the SNR and find a global minimum for the power consumption of the complete modulator. The model includes the power consumption of five blocks

$$P_{tot} = P_{amp} + P_{comp} + P_{cap} + P_{jit} + P_{filter} \tag{4.33}$$

where P_{amp} is the power consumed to bias the integrator amplifiers and their CMFB, P_{comp} is the power consumed by the comparator, P_{cap} the power used to charge the capacitors in the modulator feedback, P_{jit} is the power consumed by the oscillator and P_{filter} is the power consumed in the digital decimation filter. As in the previous section the reference circuit is not included, since its power consumption is independent of topology and thus not interesting in a comparison.

4.3.1 Power consumption related to the integrators

Both P_{int} and P_{cap} are directly related to the integrators, and they will be discussed here. The power consumed in the amplifiers is limited by either slew-rate at the output of the amplifier or by gain bandwidth (GBW) of the amplifier. In both cases the required current will be a function of the capacitiv loading of the amplifier. In both cases the power consumption P_{int} can be found from the required bias current according to (3.14) multiplied by the modulator order:

$$P_{amp} = m(4+1)I_B V_{dd} \tag{4.34}$$

In case of the slew-rate limitation the load experienced by the amplifier is given by the capacitors at the input of the following stage and the capacitors at its own input, since it should be able to move the charge from these C_s capacitors to the integration capacitor C_f. The result is, that in the worst case, the amplifier should be able to charge three capacitors to the reference voltage in half a sampling period assuming that C_s capacitors in all stages have the same value and since $I = dq/dt$ and $q = C \cdot V$, where q is charge and t is time, the minimum required slew-rate

limited current is given as:

$$I_{slew} = 3C_s 2f_s \frac{K_r \cdot V_{dd}}{2} \tag{4.35}$$

The required GBW of the amplifier is found from the time constant τ related to GBW and transconductance (g_m) of the amplifier input transistors as [40]:

$$\tau = \frac{1}{GBW} = \frac{C_f}{g_m} \tag{4.36}$$

τ should be low enough to ensure that the amplifier can move enough charge from the input capacitor C_s to C_f. In the first half sampling period the capacitors C_{s1} and C_{s2} are charged to the input voltage and a reference voltage. This charge is in the following half sampling period transferred to the capacitor C_f. The capacitor is charged by the amplifier with the current shown in Fig. 4.10 [39].

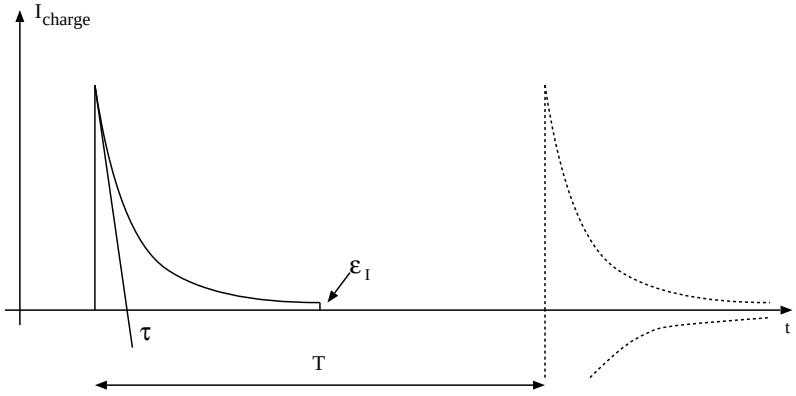

Figure 4.10: Charging current delivered to C_f from the amplifier

According to Fig. 4.10 showing the exponential dependency of the charging current, it is known that the voltage across C_f has an exponential dependency on time. The error $\epsilon_v(t)$ is the ratio between the voltage error $V_\epsilon(t)$ and the complete voltage change on capacitor C_f during time t. Therefore the largest error is obtained when the largest possible voltage change V_{ref} is applied to capacitor C_f. The error $\epsilon_v(t)$ is described as an exponentially decaying function of time as:

$$\epsilon_v(t) = \exp^{-\frac{t}{\tau}} = \frac{V_\epsilon(t)}{V_{ref}}. \tag{4.37}$$

The error should be less than one half LSB to have a resolution of B bits in the modulator. For a full voltage swing V_{ref} the voltage related to half an LSB is given as $V_{LSB} = V_{ref}/2^{(B+1)}$ at time t_0. From Fig. 4.10 it is seen, that this result should be reached at $t_0 = T/2 = 1/(2f_s)$:

$$V_\epsilon(t_0) \leq \frac{V_{ref}}{2^{B+1}}. \tag{4.38}$$

Combining $t_0 = T/2 = 1/(2f_s)$, (4.37) and (4.38) leads to a time constant of:

$$\frac{1}{\tau} \geq 2f_s(B+1)\ln(2). \tag{4.39}$$

If τ in (4.39) is replaced with (4.36) and g_m from (3.1) is applied the necessary drain bias current to the amplifier is found:

$$I_{GBW} = nV_T C_f ln(2)(B+1)2f_s. \tag{4.40}$$

The current that should be used in the calculation of the amplifier power consumption, is found as the higher of the two I_{slew} or I_{GBW}. To be able to compare them a conversion between C_s and C_f is necessary. This conversion is found using the unity gain bandwidth of the integrator:

$$\omega_u = \frac{f_s C_s}{C_f}. \tag{4.41}$$

In the previous section the approximation was made that $\omega_u = 2\pi f_{co}$. Using normalized frequency $f_n = 2f_{co}/f_s$ the relation is:

$$C_s = C_f \pi f_n. \tag{4.42}$$

The capacitors in the feedback path are charged by the comparator. The power consumption required for this charging as well as the charging for the capacitor loading the input signal is thus not included above. The modulator is differential, and thus there are 2(m+1) capacitors. In the worst case they are charged to $V_{ref}/2$ during one sampling period. The current needed to charge each capacitor is:

$$I_{cap} = \frac{q}{t} = \frac{K_r V_{dd}}{2} C_s f_s \tag{4.43}$$

giving a power consumption for the 2(m+1) capacitors of:

$$P_{cap} = \frac{K_r {V_{dd}}^2}{2} C_s f_s 2(m+1). \tag{4.44}$$

4.3.2 Comparator power consumption model

A general model of a comparator is needed for this work. The CMOS clocked comparator includes a differential amplifier stage followed by a cross coupled positive feedback circuit (PFB) as two stages [17] telescopic [16] or in more complicated stages [41]. The model used here is therefore a general two stage comparator as the simplified model showed in Fig. 4.11.

The comparator operates in two different phases, a comparing phase and a hold phase as illustrated in Fig. 4.12:

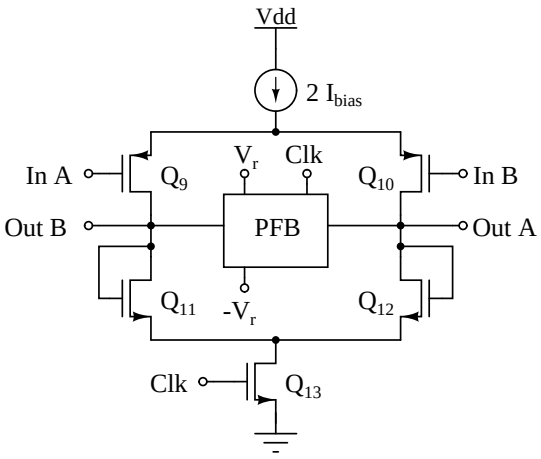

Figure 4.11: Simplified diagram of a comparator

- Comparing phase: This is when the Clk signal is high. If InA=InB, each branch will be biased with I_{bias} and the output voltages will be at some bias voltage V_b. In practice this will not happen since a slight difference in the inputs will create an amplified difference at the output.

- Hold phase: This is when the Clk signal is low. Q_{13} will cut off the biasing of the first stage, and the PFB is enabled. This circuit will provide a positive feedback to the difference on the output nodes, and the outputs will saturate at the reference voltages.

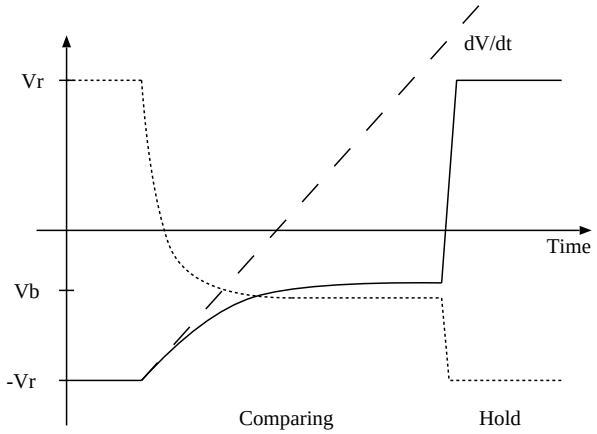

Figure 4.12: Out A and Out B during a Comparing and hold mode

The load during the comparing mode is capacitive, and it is due to parasitic capacitances. The amplification stage results in two drain and one gate capacitance. The PFB is assumed to be cross coupled inverters and is thus contributing with two

drain and two gate capacitances. The total load capacitances is denoted C_x.

When the comparing phase starts, the PFB is disabled, and the amplification stage starts to charge C_x from the reference voltages. The node starting from the positive reference voltage is discharged through Q_{11} or Q_{12}. Since they are diode coupled, the charging current as well as the discharge rate will be high. The node starting from the negative reference voltage is charged through Q_9 or Q_{10}. The diode coupled transistor in this branch will be closed, and the complete bias current $2I_{bias}$ is charging the node. If it is assumed that the diode transistors are wide, this node will limit the speed at which V_b can be reached. The charging rate is:

$$\frac{dV}{dt} = \frac{V_b}{\tau} = \frac{2I_{bias}}{C_x}. \tag{4.45}$$

The system should be able to settle to V_b, which in the following will be assumed half way between the reference voltages. It is assumed, that 5 time constants are needed for the settling:

$$5\tau = \frac{1}{2f_s} \tag{4.46}$$

The result is that the comparator requires a bias current of:

$$I_{bias} = 5f_s C_x K_r V_{dd}. \tag{4.47}$$

Furthermore the PFB needs to charge the output nodes to the reference voltage when going into hold phase. This requires a charge of $K_r V_{dd} C_x$ and it is delivered once per clock period, meaning that the mean current is:

$$I_{PFB} = (K_r V_{dd})^2 C_x f_s \tag{4.48}$$

The comparator consumes $2I_{bias}$ from a supply voltage of V_{dd}, and $2I_{PFB}$ from a supply voltage of $K_r V_{dd}$, and the total power consumption is:

$$P_{comp} = V_{dd} f_s C_x \left(10 K_r V_{dd} + 2K_r^2 V_{dd}\right). \tag{4.49}$$

4.3.3 Power consumption of the oscillator and decimation filter

The power consumption of the oscillator is only dependent on how much jitter noise can be accepted, and the power consumption of the oscillator is found by rearranging (4.31) or (4.32):

$$P_{jit} = \left(1.2 \cdot 10^{-10}\right)^2 \frac{1}{f_s N_{jit}} \left(2\pi f_b \cdot \frac{MSA \cdot V_{ref}}{2}\right)^2 \frac{2f_b}{f_s}. \tag{4.50}$$

The purpose of the filter following the modulator is to down-sample and low-pass filter the digital output stream. The decimation factor D is given as the highest integer fulfilling:

$$D \leq \frac{f_s}{2f_b}. \tag{4.51}$$

Sinc filtering is easily obtained as a running average of the input samples. The averaging over M samples is done according to the transfer function [1] [27]:

$$T_{avg}(z) = \frac{1}{M}\sum_{i=0}^{M-1} z^i \tag{4.52}$$

which should be followed by a down-sampling of a factor M in order not to average the same value more than once. Intuitively averaging a number of values will remove high frequency content in the bit-stream, and thus the bit-stream will be low-pass filtered. It can be shown that the type of filter follows the sinc function, if T_{avg} is rewritten into:

$$T_{avg}(z) = \frac{1}{M}\left(\frac{1-z^{-m}}{1-z^{-1}}\right) \tag{4.53}$$

which since $z = e^{j\omega}$ results in the sinc filter frequency response:

$$T_{avg}(z) = \frac{1}{M}\left(\frac{sinc\left(\frac{\omega M}{2}\right)}{sinc\left(\frac{\omega}{2}\right)}\right). \tag{4.54}$$

If k_s of these filters are cascaded, the filtered output will be filtered again, and their transfer functions are multiplied to form a k_s^{th} order filter:

$$T_{avg}(\omega) = \frac{1}{M^{k_s}}\left(\frac{sinc\left(\frac{\omega M}{2}\right)}{sinc\left(\frac{\omega}{2}\right)}\right)^{k_s}. \tag{4.55}$$

This transfer function is plotted in Fig. 4.13 for a second and a fourth order filter with D=6.

It is clearly seen that the bit-stream is filtered, it is however also seen that the conversion band is not flat. Therefore the sinc filter is usually followed by a sinc compensation filter. Furthermore it is seen, that the ripple in the stop-band is huge close to the pass-band, and thus the last two down-samplings can be performed with half-band filters which have pass-bands from 0 to $f_s/4$ and stop-bands from $f_s/4$ to $f_s/2$. Alternatively the sinc compensation and the half-band filter can be replaced by one IIR filter.

However in this work the decimation filter is simplified, and sinc filtering alone is assumed all the way down to Nyquist rate. The approach used in this work is to cascade D FIR2 filters [39]. A FIR2 filter consists of k_s averaging filters with $M = 2$

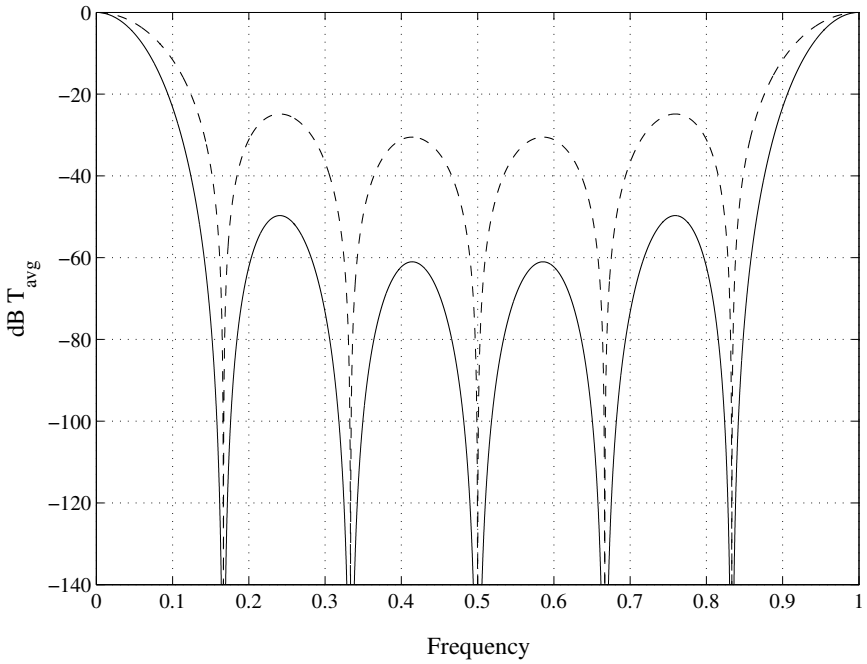

Figure 4.13: Transfer function of two decimation filters of second (dashed) and fourth order (line)

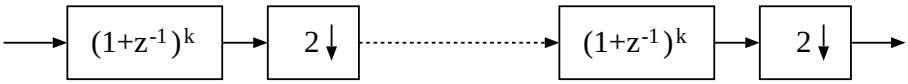

Figure 4.14: Block diagram of the FIR2 decimation filter

cascading each others (averaging two values and down-sampling with a factor of 2) as shown in Fig. 4.14.

To implement the function $(1 + z^{-1})$ for a word length of Q bits, one delay and one summation is required. The delay can be implemented as Q parallel D flip-flops, and the summation requires $Q-1$ full adders and one half adder since the result will never result in a carrier. A decimation filter with D=4 and an order of k_s is shown in Fig. 4.15.

Traditionally the dynamic power consumption has been far the dominating power consumption in digital circuits. This is also assumed in this work even though leakage currents in modern processes is an ever increasing part of the total current consumption. This means that the power consumption of the filter will be proportional to the sampling frequency f_s and the activity factor α. Evaluating Fig. 4.15 leads to a

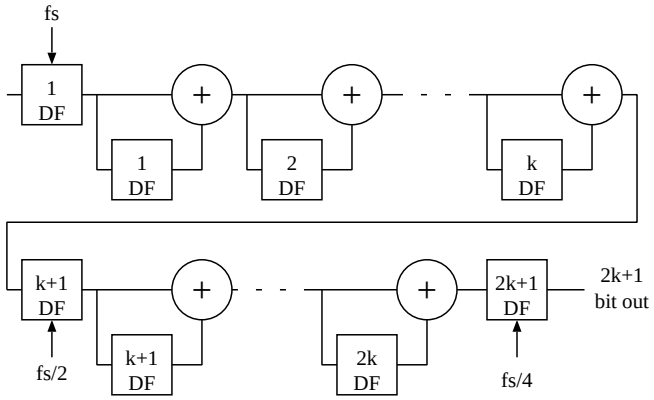

Figure 4.15: Decimation filter with D=4 and an order of k

power consumption in the decimation filter of:

$$P_{filter} = \sum_{i=0}^{log_2 D} \frac{\alpha f_s}{2^i}(ik_s+1)P_{df} + \sum_{i=0}^{(log_2 D)-1} \frac{\alpha f_s}{2^i} \sum_{j=1}^{k_s}((ik_s+j)P_{df}+P_{ha}+(ik_s+j-1)P_{fa}) \tag{4.56}$$

where P_{df}, P_{ha} and P_{fa} are power consumption per Hz for a D flip-flop, a half adder and a full adder respectively.

D and f_s are known from the modulator, but also a filter order k_s is used in the power calculation. It is seen from Fig. 4.15, that at the output of the filter the increase in number of bits is given from:

$$\text{NB} = k_s \cdot log_2 D \tag{4.57}$$

where as in the modulator an increased OSR results in a SNR expressed in bits of:

$$\text{SNR}_B = (m + 0.5)log_2(\text{OSR}). \tag{4.58}$$

Increasing the number of bits in the filter also costs in term of power, but the cost is low compared to the cost of increasing SNR_B in the modulator. Thus the modulator should be limiting the SNR at the output requiring $\text{SNR}_B \geq \text{NB}$. It is clear from (4.57) and (4.58) that k_s should be one order higher than m.

4.4 Using the discrete time model

The results from simulations are power consumption of different discrete time modulators as a function of f_s, f_n and the modulator order m. To use the equations found in this chapter some process parameters are needed as well as the input frequency band width from f_{min} to f_b, the number of bits at the output, dimensions of the input transistors in the integrators and range of capacitor sizes.

4.4.1 Simulation set up

The power consumption calculations are performed for each (f_s,f_n) point starting from the noise budget (4.18). This noise is separated into two parts, oscillator noise N_{jit} and internal electrical noise N_{int}. The optimal way of splitting the noise is found through an iterative method. The power consumption of the oscillator is found directly from N_{jit} according to (4.50).

The internal noise N_{int} first of all needs to be larger than the 1/f noise contribution (3.13), since it is independent of power consumption. Then the value for C_s, needed to meet the power budget, is found. If the capacitor is increased, the noise of switched input capacitors N_{cs} is decreased (4.27). At the same time the amplifier bias increased both when it was limited by slew rate (4.35) and GBW (4.40) resulting in a decreased white noise in the amplifier according to (3.12). On the other hand the increased bias also means increased power consumption. If the equations mentioned above are combined, two values for C_s can be found from solving the following equations. In case of slew-rate limitation:

$$\begin{aligned} N_{int} &= m \cdot ln\left(\frac{f_b}{f_{min}}\right)\frac{2K_{fp}+2K_{fn}}{W_1 L_1 C_{ox}^2 \mu_p}\left(1+\frac{1}{2f_n}\right)^2 + \\ &\quad \frac{m}{C_f}\left(\frac{16kTf_b}{\pi f_n f_s}+\left(1+\frac{1}{2f_n}\right)^2\frac{32\gamma kTf_b nV_T 2}{6\pi f_n f_s K_r V_{dd}}\right) \end{aligned} \tag{4.59}$$

and in the case of GBW limitation:

$$\begin{aligned} N_{int} &= m \cdot ln\left(\frac{f_b}{f_{min}}\right)\frac{2K_{fp}+2K_{fn}}{W_1 L_1 C_{ox}^2 \mu_p}\left(1+\frac{1}{2f_n}\right)^2 + \\ &\quad \frac{m}{C_f}\left(\frac{16kTf_b}{\pi f_n f_s}+\left(1+\frac{1}{2f_n}\right)^2\frac{32\gamma kTf_b}{(B+1)ln(2)2f_s}\right). \end{aligned} \tag{4.60}$$

The noise from input capacitors and amplifier is multiplied by the modulator order m, since it is expected that the power of the stages is scaled according to (4.24), meaning that all stages will result in the same amount of noise.

When the capacitor values are found and thus also the bias currents, all power consumption contributions in (4.33) can be calculated. The result plotted as a function of cut off frequency and sampling frequency is the inverse of the power consumption since the maximum power will be infinite in a case where the modulator can not meet the requirements. The optimal solution is easily found as the maximum point of the plot. The process parameters used in the simulations are for a 0.35 μm process, and the rest of the values used are seen in table 4.1.

Table 4.1: Values used in the discrete time modulator simulation

V_{dd}	1 V	K_r	0.8	k	$1.38*10^{-23}$
B	16 bit	W/l	300	T	300 K
C_x	1 pF	f_{min}	20 Hz	f_b	20 kHz
P_{df}	0.2 pW/Hz	P_{ha}	0.25 pW/Hz	P_{fa}	0.35 pW/Hz

4.4.2 Results from DT simulations

The model is tested on a converter producing 16 bits at the output over the audio frequency band from $f_{min} = 20\ Hz$ to $f_b = 20\ kHz$ from a 1 V supply voltage. The purpose of selecting this converter constellation for the comparison between DT and CT converters is to see if it would be feasible in a hearing aid application. In such an application the converter is allowed to consume in the order of a few hundreds of μW. The results from the simulations are plotted as inverted power as function of f_s and f_n.

First the modulator order is selected, and this selection is based on power consumption. The first order modulator is not considered due to two reasons: First the tonal problem in the first order modulator is much worse in this type of modulator compared to modulators of higher order. These tones are extremely annoying for a hearing aid user. The tones arise when the input signal is low, and therefore silence in the nature might sound more like a refrigerator. Secondly the relatively high resolution of 16 bits (98 dB) requires a gain which is somewhat higher than 98 dB. In the first order modulator this gain is produced by a single stage in contrast to modulators of higher order, where the requirements in terms of gain per stage is lower. This problem will not be found by the model since the amplifier gain is not incorporated, and thus the first order modulator will result in unrealistic results. Examples from simulations on the second order modulator is presented in Fig. 4.16, where the power consumption is plotted without considering jitter or decimation filter.

In the figure the possible solution range is found as the area where the inverted power consumption is different from zero. At high f_n there is no solution because the MSA is decreased until it reaches 0, and the modulator is unstable. At low sampling frequencies the quantization noise cannot be decreased enough within the stable cut off frequencies, and a solution is not found either. The last solution limit found at low f_n is formed by the fact, that if the cut off frequency for a specific sampling frequency becomes too low, the quantization noise becomes too large for a 16 bit resolution.

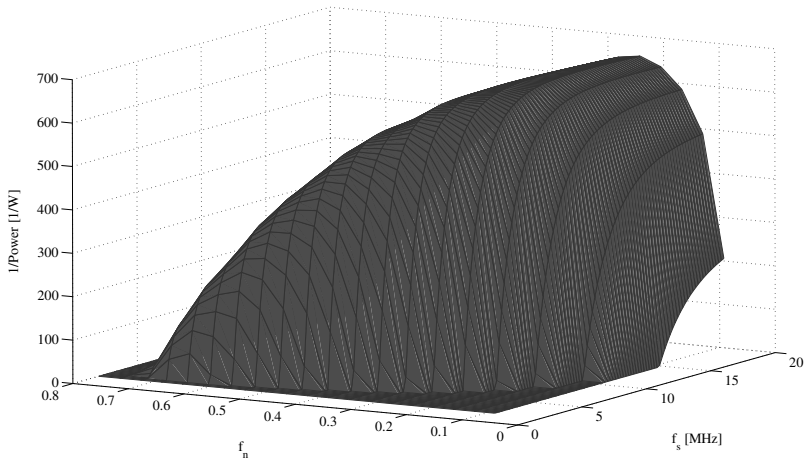

Figure 4.16: Simulation result for the inverted power for a second order DT modulator as a function of sampling frequency is in Hz, and cut off frequency normalized as $(2f_{co})/f_s$

When f_s becomes just high enough to result in a possible solution, the quantization noise is only slightly lower than the total allowed noise, and the power consumed by the modulator is large. This power is decreased as f_s is increased, until the advantage of reducing quantization noise further with f_s is too small to compensate for the increased power consumption due to bandwidth in amplifiers and comparator.

It was seen in Fig. 4.16 that the optimal solution requires a power consumption of 1.51 mW with $f_s = 15\ MHz$ and $f_n = 0.25$. When the jitter is taken into account, the power consumption is of course increased with the power consumed by the oscillator, but since the jitter noise also reduces the noise allowed in the integrators, the power consumption of the amplifiers will also increase. A simulation for the same second order modulator including oscillator jitter is seen in Fig. 4.17. It is clearly seen that the power consumption has increased. It is now 2.19 mW with the same values for f_n and f_s.

The decimation filter does not contribute to the noise in the modulator and thus when including the filter, the power consumed by the modulator will still be as in Fig. 4.17, and the increase in power consumption will be from the filter alone. The result is seen in Fig. 4.18, where the power consumption has increased to 2.25 mW. It is interesting to see, how the power is distributed in the converter. This is illustrated with the pie diagram in Fig. 4.19.

It is important to notice that the power consumption is dominated by the first integrator followed by power consumption of the second integrator. The difference

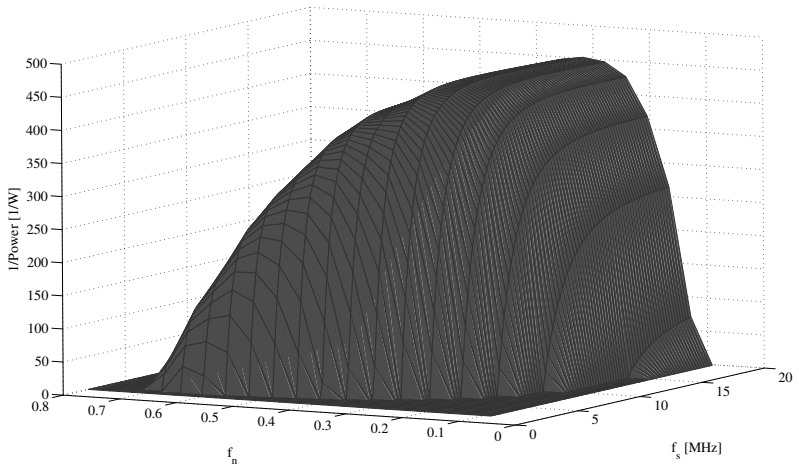

Figure 4.17: Simulation results for a second order DT modulator including oscillator

is caused by the scaling of the integrators. As expected it is also seen, that the power consumption in the oscillator is very limited. The power consumed by the switched input capacitors is also interesting since a considerable part of this power is at the input of the first integrator. This power should be supplied through the input and it might be necessary to apply a buffer, which in the DT case should be carefully designed to withstand a switched load. The power consumption of the filter is also limited and could seem unimportant, but since it does not scale as efficiently with resolution as power consumption in the modulator, it will be very important in converters with lower resolution. As an example the filter will require 25 % of the total power in a 10 bit converter.

An interesting effect in the results is the amplification of the noise in the integrators (4.29) which is increasing when f_n is decreased. Due to stability f_n is decreased when the modulator order is increased. The white noise is reduced by increasing power consumption, whereas 1/f noise is independent of power consumption. This means that with given transistor dimensions, conversion bandwidth and process, there will be a maximum SNR even with an infinite power consumption. This point is reached when the complete noise budget is occupied by 1/f noise. A higher resolution can only be reached by increasing f_{min}. In table 4.2 the maximum SNR for a band from 20Hz-20kHz is given for a 4^{th}, 5^{th} and 6^{th} order modulator with dimensions as shown above. The table also show the minimum frequency required to obtain an SNR of 16 bit.

The optimal solution is thus either the second or third order modulator. Accor-

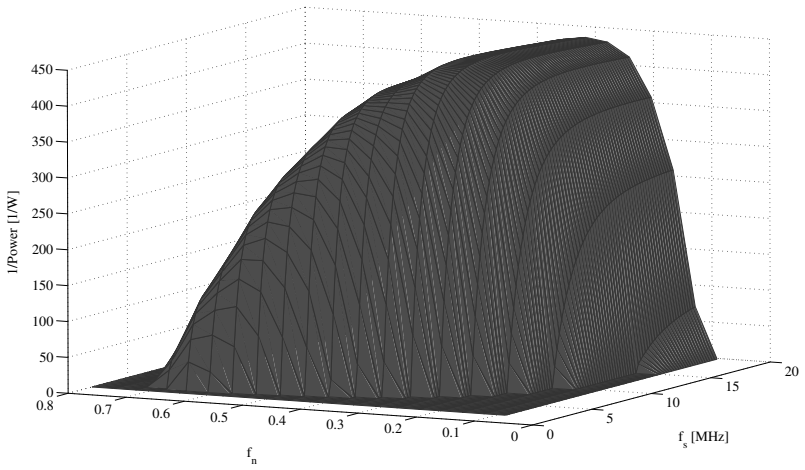

Figure 4.18: Simulation results for a second order DT modulator including oscillator and decimation filter

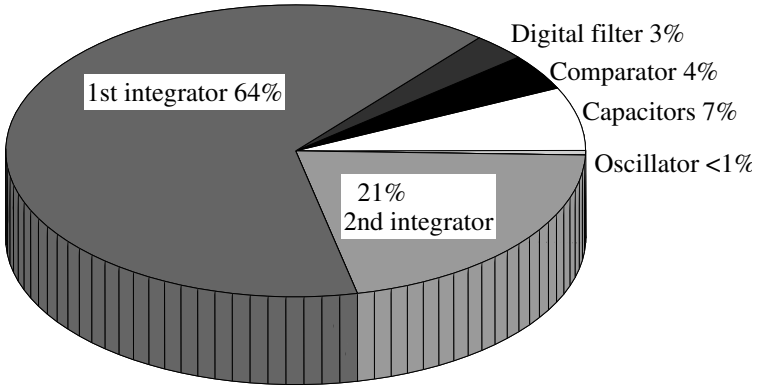

Figure 4.19: Distribution of power in a second order DT converter

ding to this model, the second order modulator consumes slightly less power than the third order modulator, but due to the gain and tonal problems mentioned above the third order modulator might be considered in some applications.

4.5 The continuous time ΣΔ modulator

Often the g_mC topology is used in CT modulators mainly due to the compatibility with CMOS processes. The disadvantage of the g_mC topology is the limited linear region. Normally the region with linear transconductance is much lower than 50 % of the supply voltage (recently <40 % [43] and [60] <30 % [25]).

In modern processes high quality resistors are available and because of the lin-

Table 4.2: Impact of 1/f noise in higher-order converters

Order	f_{min}	SNR_{max}
4	1 kHz	95 dB
5	4 kHz	91 dB
6	8 kHz	89 dB

earity of a resistor an RC integrator can easily reach a linear range of 80 % of the supply voltage ($K_r = 0.8$). In the CT modulator the sampling is performed after the integrators as shown in Fig. 4.20. For simplicity the modulator in the figure is shown single ended, even though the calculations are made for a differential modulator.

As for the DT modulator a power consumption model is built in this section. The calculations include noise, and ensure that a given SNR is obtained. The advantage of the CT modulator is that the integrators bandwidths are lower than in DT. This is of course included in the model as well as the fact that the CT modulator is more sensitive to jitter noise.

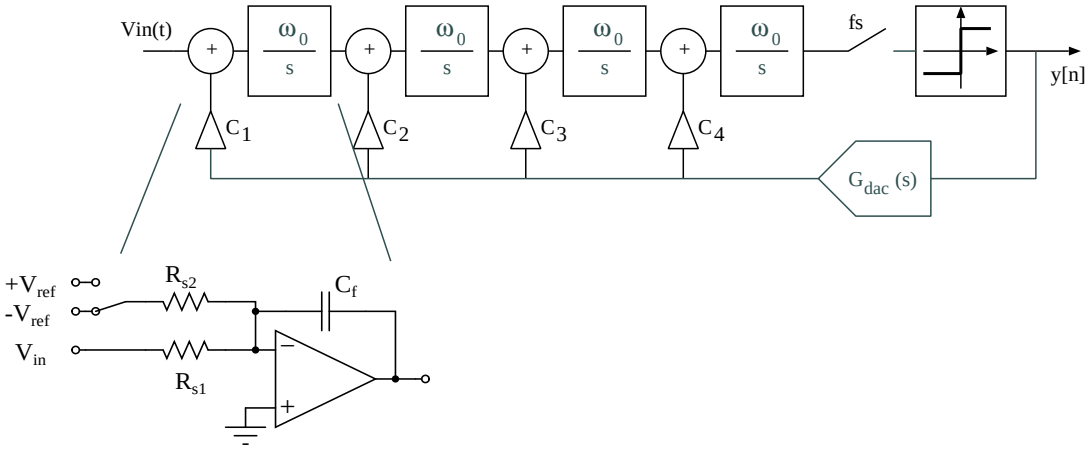

Figure 4.20: Block diagram of a 4^{th} order CT ΣΔ modulator and a single ended RC integrator

Stability calculations were seen to be independent of operation time mode (discrete or continuous). Thus the same assumptions can be made as for the DT modulator, and the signal power is still given as (4.17). The total noise budget in the modulator still consists of quantization noise (4.20), internal noise from the integrators and a jitter noise contribution as shown in (4.21).

4.5.1 Internal noise

The internal noise is produced by the amplifiers and the input components, which in this case are resistors as seen in Fig. 4.20. The resistors are noisy components (see also (B.2)) with a noise spectral density of:

$$N_r(f) = 4kTR \tag{4.61}$$

The integrated noise in a fully differential integrator is given as:

$$N_r(f) = 8kT(R_{s1} + R_{s2})f_b \tag{4.62}$$

The modulator can be scaled [28] with $C_1 = 1$ giving $R_{s1} = R_{s2} = R_s$. The total noise from the input resistors integrated over the conversion band from 0 to f_b is:

$$N_{rs} = 16kTR_sf_b \tag{4.63}$$

As in DT the noise or power consumption produced in the later integrator stages can be scaled. As for the stability the scaling is independent of operation time mode, and thus the power can be scaled according to (4.24) when the same amount of noise is allowed from all stages.

The amplifier is assumed to be the same as in the DT model, and the input referred noise from the amplifier is still given from equation (3.10) and (3.11). The white noise contribution (3.10) is controlled by the bias current and therefore the power consumption of the modulators. The noise from the amplifier is also used in a feedback configuration and the noise is amplified according to (4.29).

4.5.2 Jitter noise contribution

The third noise contribution in (4.21) is jitter noise, which is known to be more severe in CT than in DT modulators. The oscillator noise was discussed in section 3.2.1 and it was shown how the jitter is converted to input referred voltage noise. The oscillator jitter is converted to voltage noise in the sampler which is inside the loop, and jitter on the clock introduces two problems. First the input of the quantizer is sampled slightly too late or early, which however is a minor problem since this noise is shaped, and since errors occur very seldom due to the single-bit quantization. Secondly the length of the pulse which is feed back will be wrong which is a more severe error. This is illustrated in Fig. 4.21 for a no return to zero (NRZ) [7],[39].

From the figure it is seen, that the feedback signal can be seen as an error free feedback signal added with a error pulse train consisting of narrow pulses. The

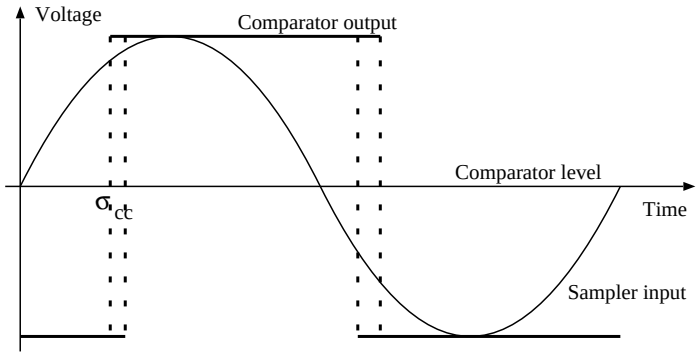

Figure 4.21: Time domain jitter noise to voltage noise conversion

feedback signal (and thus also the error pulses) is integrated by the first integrator in the modulator. All the error pulses have an amplitude of V_{ref}, and their effect in the integration is equivalent to pulses with the length $1/f_s$ and a noise amplitude given from:

$$V_{jit}^2 = \left(\frac{V_{ref}\sigma_{cc}}{T_s}\right)^2 = \left(V_{ref}\sigma_{cc}f_s\right)^2. \tag{4.64}$$

It is assumed that this noise is white [7], and distributed in the frequency spectrum from 0 to $f_s/2$. Integration of the noise power in the conversion band results in:

$$N_{jit} = \frac{16\gamma}{3\eta} \cdot \frac{kT}{P_{jit}} \cdot V_{ref}^2 \cdot 2f_b \tag{4.65}$$

or if the numbers from section 3.2.1 are used, the jitter is:

$$N_{jit} = \left(1.2 \cdot 10^{-10}\right)^2 \frac{2f_b}{P_{jit}} \cdot V_{ref}^2. \tag{4.66}$$

4.6 Power consumption in the continuous time ΣΔ modulator

The power consumption of the modulator in CT almost consists of the same contribution as in the DT modulator (4.33). Only the power consumption in the capacitors are exchanged by a power consumption of the resistors (P_{res}) in the integrators:

$$P_{tot} = P_{amp} + P_{comp} + P_{res} + P_{jit} + P_{filter}. \tag{4.67}$$

Since the power consumption of the comparator (P_{comp}) and the decimation filter (P_{filter}) are the same as in DT, they will not be discussed further.

4.6.1 Power consumption in integrator amplifiers

The power consumption of the amplifier includes power consumed by the CMFB since a differential solution is assumed. With a bias current of I_B in the folded

cascode amplifier P_{amp} is:

$$P_{amp} = m(4+1)I_B V_{dd} \tag{4.68}$$

The bias current can be limited either by slew-rate defined from the loading of the amplifier which in this case is resistive or by GBW of the amplifier.

When the amplifier is slewing, it delivers I_B to the load. The load on the amplifier consists of the input and feedback resistors at the input of the integrator in which it is placed and by the input resistor in the following integrator stage. Slewing occurs when the maximum voltage (and thus maximum charging current) is applied to the resistors. This worst case voltage is $V_{ref}/2$ resulting in an I_B of:

$$I_{slew} = \frac{3K_r V_{dd}}{2R_s} \tag{4.69}$$

The minimum GBW required in a CT modulator has been studied in [14]. This study is based on harmonic distortion, and the result is a minimum GBW of:

$$GBW = \frac{g_m}{C_f} = \frac{f_s}{\sqrt[2m]{2}-1} \tag{4.70}$$

It is expected that GBW in CT should be much lower than in DT. This is indeed seen to be true for high resolution modulators if (4.70) is compared to (4.39). As an example the GBW in the DT modulator in a 16 bit third order modulator is required to be 2.9 times the GBW in the CT equivalence. Since g_m is now known, the required bias current can be found according to (3.1):

$$I_{GBW} = GBW C_f n V_T \tag{4.71}$$

As in the previous case it is seen that I_{slew} and I_{GBW} is not related to the same component, and it is thus necessary to link them together. If it is assumed that the f_{co} is at the unity gain bandwidth of the integrator, the link between C_f and R_s is:

$$C_f = \frac{1}{\pi R_s f_n f_s}. \tag{4.72}$$

An interesting fact is that if I_{slew} in both cases is referred to C_f, it is seen that the current in DT is twice the current of its CT equivalence for the same value of C_f. This is however not a surprise since the amplifier delivers the same charge in both cases, but within half the time in the DT case.

4.6.2 Other power consumptions in the modulator

The comparator as well as the decimation filter is not dependent of whether it is used in DT or CT, and the discussions from the previous section can be used directly in the calculation of P_{comp} and P_{filter}.

In CT a high resolution requiring low integrator noise results in rather small values for R_s, and thus a considerable power consumption in the feedback resistors and in the input resistors of the first integrator. In the worst case, the voltage across a resistor is $V_{ref}/2$, and the current is thus given as:

$$I_{res} = \frac{K_r V_{dd}}{2R_s}. \tag{4.73}$$

In the differential solution, there are $2(m+1)$ resistors resulting in a power consumption of:

$$P_{res} = \frac{K_r V_{dd}^2}{2R_s} 2(m+1). \tag{4.74}$$

The last power contribution included in the model is the power consumed by the oscillator. This power consumption is dependent on the allowed jitter noise in the oscillator, and it can be found by rearranging (4.65) or (4.66). From the latter equation the result is:

$$P_{jit} = \left(1.2 \cdot 10^{-10}\right)^2 \frac{2f_b}{N_{jit}} \cdot V_{ref}^2. \tag{4.75}$$

4.7 Using the continuous time model

The results from the CT case should be compared to the results found for the DT case. This is done by calculating power consumption using the parameters mentioned in section 4.4 since these parameters are independent on the time mode.

4.7.1 Simulation set up

As in the DT case, an iterative method is used to find the optimal amount of the power budget that is used for the jitter noise N_{jit} and for the internal electrical noise N_{int}, and the oscillator power consumption is found from (4.75).

The trade-off is in the CT case that reducing R_s reduces the N_{rs} (4.63), and reduces thus the noise requirements to the amplifier, which decreases the necessary bias current. On the other hand a reduced R_s results in an increased I_{slew} (4.69) and I_{GBW} (4.71). Therefore the highest possible R_s value where the noise budget is just met, is calculated. Two different values for R_s are found for slew-rate limitation and GBW limitation. If the slew-rate is limiting the power consumption, R_s is calculated from:

$$\begin{aligned} N_{int} &= m \cdot ln\left(\frac{f_b}{f_{min}}\right) \frac{2K_{fp} + 2K_{fn}}{W_1 L_1 C_{ox}^2 \mu_p} \left(1 + \frac{1}{2f_n}\right)^2 + \\ & \quad m \cdot R_s \left(16kTf_b + \left(1 + \frac{1}{2f_n}\right)^2 \frac{32\gamma kTf_b n V_T 2}{3K_r V_{dd}}\right) \end{aligned} \tag{4.76}$$

and in the case of GBW limitation:

$$N_{int} = m \cdot ln\left(\frac{f_b}{f_{min}}\right)\frac{2K_{fp}+2K_{fn}}{W_1 L_1 C_{ox}^2 \mu_p}\left(1+\frac{1}{2f_n}\right)^2 + m \cdot R_s\left(16kTf_b + \left(1+\frac{1}{2f_n}\right)^2 32\gamma kTf_b(\sqrt[2m]{2}-1)f_n\pi\right). \quad (4.77)$$

From these values of R_s the power consumption of the complete modulator can be calculated. When the internal noise budget N_{int} is larger than the 1/f noise alone, the result is a positive and realizable value for R_s. Naturally the same process as well as the same parameters (see table 4.1) as in the DT case is used to make a fair comparison.

4.7.2 Results from CT simulations

The model is used as described for the DT modulator. This means that the modulator examined is a 1 V audio band (20 Hz to 20 kHz) for hearing aids. Also in this case the first order modulator is disregarded due to idle tones as well as a possible problematically low gain in the amplifiers. Simulations are carried out on the second order modulator. The solution range will be similar to the DT case, and in Fig. 4.22 simulated inverted power consumption as a function of the f_s and f_n when jitter and decimation filter are not included, is plotted.

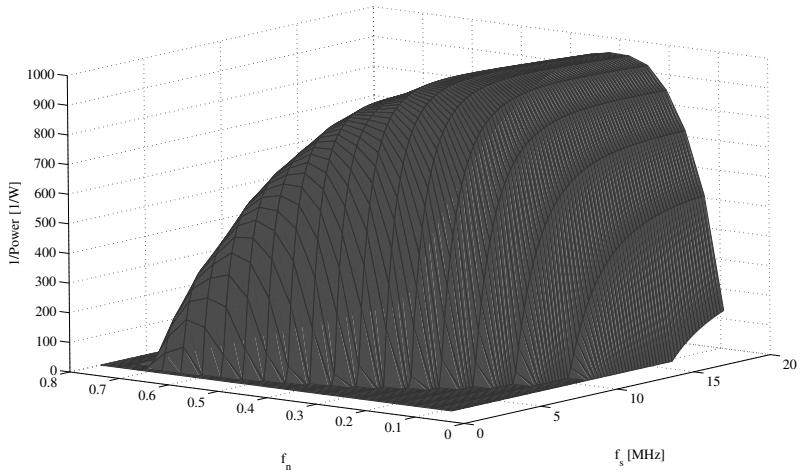

Figure 4.22: Power simulation result for a 1 V second order CT modulator where the f_s is in MHz, and the cut-off frequency is normalized as $(2f_{co})/f_s$

If this simulation result is compared to the second order DT modulator in Fig. 4.16 it is seen, that the area giving possible solutions for f_s and f_n is the

same for the two types since stability and 1/f noise is the same in both cases. In the simulation without oscillator and decimation filter included the optimal solution is a power consumption of 1.02 mW obtained at $f_s = 12$ MHz and $f_n = 0.3$. As expected this power consumption is much lower than in the DT simulation

The power consumption in Fig. 4.23 includes power consumed by the oscillator. Again an increased power consumption is expected, not only due to the power consumed by the oscillator, but also due to an increased power consumption in the amplifiers since N_{int} is reduced.

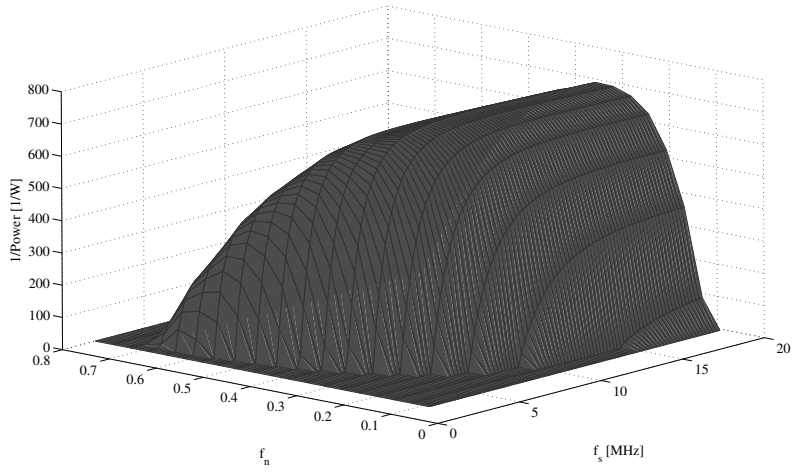

Figure 4.23: Power simulation result for a second order CT modulator including the oscillator power consumption and jitter

The power consumption in this simulation has increased to 1.41 mW. This is as expected a considerable increase (40%) compared to the increase in power in DT. It is however not enough to make the DT solution the better choice. Due to the relatively high resolution, the decimation filter included in Fig. 4.24 does not increase the power consumption much and thus the total power consumption is 1.46 mW.

The distribution of power in the converter is seen in Fig. 4.25. The result is much like in the DT case with a major power consumption in the first integrator. The only significant difference is the power consumed by the oscillator which has now increased to 8%. With the settings used in this simulation, the system is limited by slew-rate. The model might however be slightly pessimistic when it comes to slewing, since the situation designed for is quite unlikely to happen and thus some power might be saved with only slightly more distortion as a consequence.

The second order modulator consumes less power, but if less tones are needed a third order modulator can be used. For modulators with orders higher than three,

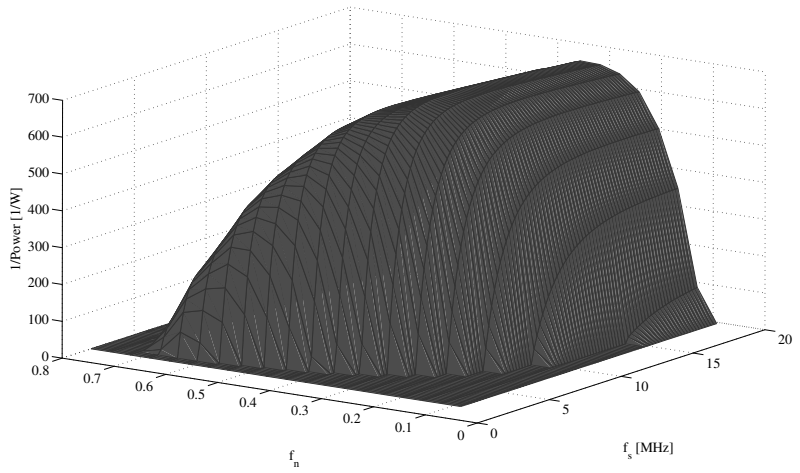

Figure 4.24: Power simulation result for a second order CT modulator with the oscillator and decimation filter included

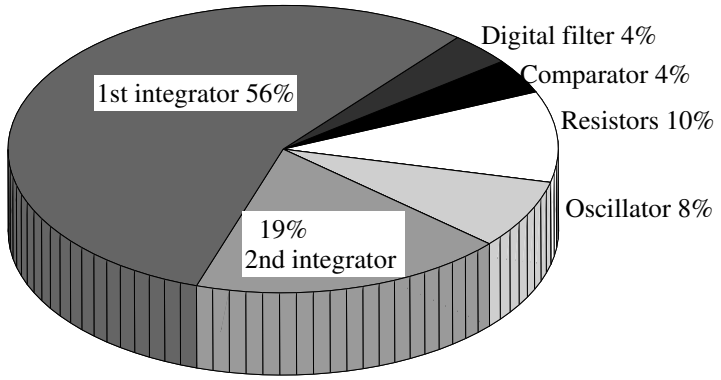

Figure 4.25: Distribution of power in the second order CT converter

the 1/f noise problem described for the DT case remains for this case as well.

4.8 State of the art comparison

Throughout the years a lot of implementations have been presented in the literature, and therefore state of the art only improves marginally for the well studied topologies like the single-bit single-loop topology. Results found in the newest literature should be comparable to the results predicted by the model, and thus model results are calculated for the parameters given in a few papers to evaluate results given by the model.

It is problematic to find recent publications usable with the assumptions made

Table 4.3: Comparison of power consumption predicted by the model and power consumption measured on fabricated converters

Cite	SNR	f_b	Supply	Power	Model pred.
[47]	81-dB	25 kHz	0.5 V	300 μW	200 μW
[15]	73-dB	25 kHz	1.5 V	135 μW	41 μW
[44]	76-dB	16 kHz	0.9 V	40 μW	29 μW
[59]	85-dB	20 kHz	1.0 V	130 μW	127 μW

in the model, not least because most implementations are multi-bit, but in table 4.3 simulations are compared to results from two CT converters published in [47] and [15] and two DT converters published in [44] and [59].

In all four simulations, the measured results are higher than the simulated result. This is also expected since the model does not include all phenomena such as matching and coupling found in a real implementation, even though the model is slightly pessimistic in the slew-rate limitation. On the other hand all four results are reasonably close to the measured results supporting the robustness of the simulations. The results might also fit even better if all parameters such as process parameters were known from the four publications, this was however not the case.

4.9 Summing up results on modulators with feedback

In this chapter power consumption in the single-bit single-loop modulator was modeled to find out which one between DT and CT modulators that are the optimal solution in terms of power consumption. It is well known and also demonstrated above, that the CT modulator is optimal when oscillator jitter is not included. But the simulations indicated that the CT implementation is still optimal, even if jitter and decimation filter are included.

In the DT case the total consumption was 2.25 mW and in the CT case it was 1.46 mW or only 65 % of the power needed by the DT solution. This is a noticeable difference, but the picture changes somewhat when the evaluations are made for other settings as shown in table 4.4. From these results it is evident, that the CT case might be the optimal choice but only marginal in some cases. This is also reasonable since none of the topologies have been able to outdo the other through numerous implementations.

Even though the difference might be small, the CT solution can be considered optimal, since it has less requirements for the anti-aliasing filter compared to the

Table 4.4: Power consumption of three different second order modulators

Frq. band	CT power	DT power	resolution	Difference in power consumption
20-20kHz	1.58μW	2.32μW	8bits	68%
10k-1MHz	37μW	64μW	6bits	58%
10k-1MHz	875μW	1069μW	12bits	82%

DT solution, which again can be seen as an advantage. The reason is, that since the sampling occurs after the integrators, it will inherently work as an anti-aliasing filter before the signal is sampled, while the DT solution only has the advantage of the oversampling compared to Nyquist converters.

4.9.1 Figure of merit for modulator with feedback

The figure of merit (FoM) is a measure allowing power comparison of different converters even if they are designed for different frequency bands or different resolutions. The FoM presented here is also found in other publications such as [45]:

$$FoM = \frac{P}{2 \cdot BW \cdot 2^B}. \tag{4.78}$$

In this equation P is the power consumption of the converter, BW is the conversion bandwidth, and B is the effective number of bits which is calculated from the SNR according to (2.2). It is noticed that the lower the FoM is, the better the converter performs.

From the theoretical derivations above the FoM for the feedback single-loop topology can be calculated. If should however be remembered that an implementation with the same topology usually results in a higher FoM, and therefore one should be careful when comparing FoM calculated for topologies and for implementations. The topology is not necessarily bad just because a designer has made a bad implementation.

The investigation of the DT and CT modulators above are all made for the same bandwidth and resolution, which was 20 kHz and 16 bits. The FoM in respectively DT and CT are:

$$FoM_{DT} = \frac{2.25\ mW}{40000 \cdot 2^{16}} = 858\ fJ/conv \tag{4.79}$$

$$FoM_{CT} = \frac{1.46\ mW}{40000 \cdot 2^{16}} = 557\ fJ/conv \tag{4.80}$$

Chapter 5

Frequency to digital ΣΔ modulator

A different approach compared to the single-bit single-loop topology just described is the modulator without feedback. In this chapter the frequency to digital ΣΔ modulator (FDSM) which is a modulator without feedback, is described. In this work the FDSM topology is based on integration in a voltage controlled oscillator (VCO) and digital differentiation, whereas other publications have been PLL based [3] [12] [49]. The advantage of the FDSM is its capability of extremely low supply voltages operation (even much below the threshold of a MOS transistor) and low power consumption. This means a competitive FoM. The theory of the modulator is described, and the principles are proved through implementations with measurements.

5.1 The first order FDSM

The ΣΔ modulator without feedback was presented in section 2.3.2. It was seen that the input signal should be integrated. There are no restrictions to what type of integrator which can be used, but because the modulator is designed for supply voltages below the threshold voltage, active circuits such as amplifiers cannot be used. The integrator type used in the FDSM is a VCO, and thus the intermediate signals in the modulator are converted into the frequency domain. By doing so the SNR of the modulator is not limited by supply voltage as in a modulator operating in voltage domain. The output frequency of a VCO is given from the input voltage x_i as:

$$f_{VCO}(t) = f_c + K_s x_i(t) \tag{5.1}$$

where f_c is the carrier frequency of the free running VCO, and K_s is the sensitivity of the VCO. The output phase is a perfect integration of the output frequency:

$$\theta(t) = 2\pi \int_{-\infty}^{t} f_c + K_s x_i(\tau) d\tau. \tag{5.2}$$

Thus if the phase is detected, a CT integration of the input signal is obtained. It is however also seen, that the output signal after differentiation will contain a DC signal not found in the input originating from f_c. This means that meaningful conversions at DC are problematic in the FDSM. Due to the cyclic behavior of the phase a DC component will not result in overflow in the integrator, as if a traditional active integrator was used. It is also seen, that the VCO sensitivity is defining the gain of the complete converter, and it is crucial that K_s is constant for all input values. If this is not the case, signals applied at the input will be distorted, and harmonic distortion is seen at the output.

The integration is in CT and thus it is followed by a sampler. This sampler detects phase, and divides the result by 2π. The sampled result is then passed to quantizer and differentiator. In general Fig. 2.6 changes into Fig. 5.1 in the first order FDSM.

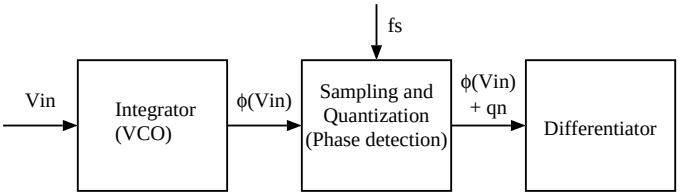

Figure 5.1: General structure of a first order FDSM

5.1.1 The D flip-flop FDSM

Implementation of the phase detection, sampling, quantization and differentiation can be carried out in various ways [22]. The straight forward implementation is to apply a resettable counter counting complete periods after the VCO. $\theta(t)$ is sampled when the counter is reset and started, and the phase is easily detected single-bit from the zero crossings of $\theta(t)$, and thus the VCO signal. Quantization and division by 2π are obtained automatically since the counter counts integers, and at the following sampling where the counter stops the result is already differentiated since the counter was reset at the previous sampling. The counter output for an increasing input voltage will be as shown in Fig. 5.2

In a practical implementation the resettable counter is however unpractical especially because it takes time to reset. An extension to this simple counter principle is

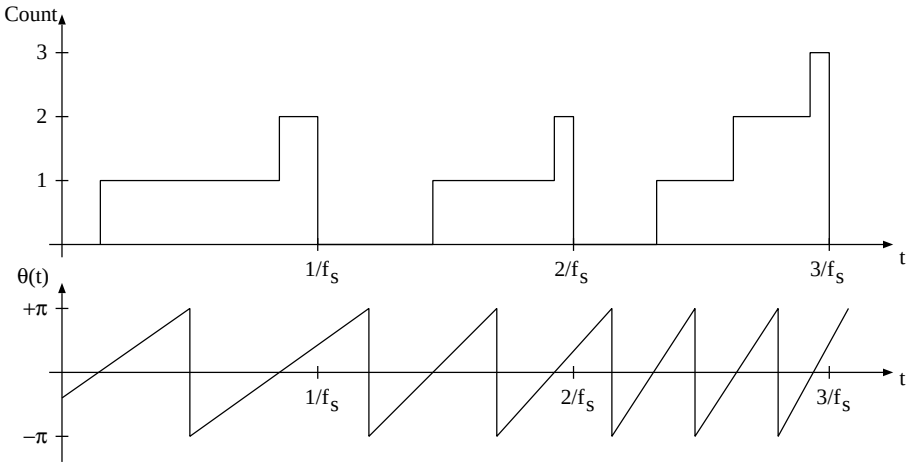

Figure 5.2: FDSM output with resettable counter

to use modulo-2^n arithmetic by using a free running counter with 2^n steps and sample the counted result. The difference between one sample and the previous sample is found in a 2^n bit subtracter, where the borrow bit is thrown away. The result is seen in Fig. 5.3 with the same input as in Fig. 5.2. It is seen, that the results using the two counter types are the same.

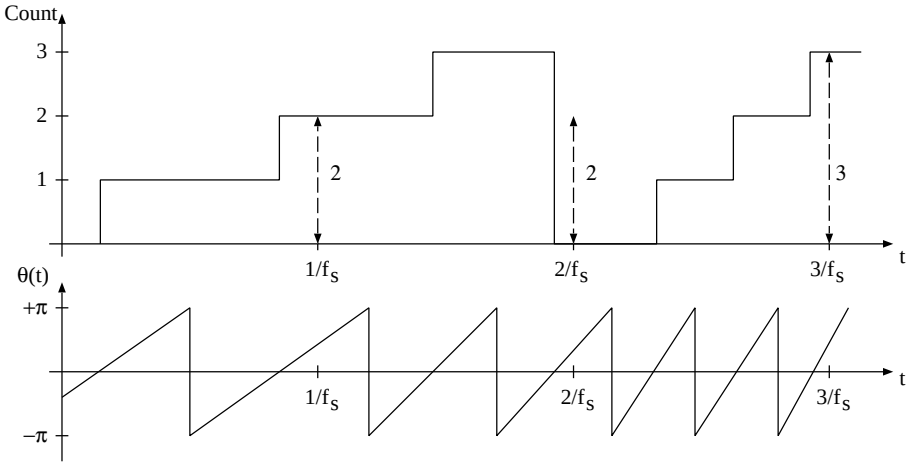

Figure 5.3: FDSM output using modulo-2^n counter

The modulo-2^n counter is not only advantageous when it comes to speed but also in terms of required steps in the counter. When using the resettable counter, the numbers of steps should be higher than than the maximum VCO periods which can occur during one sampling period with the highest possible input amplitude x_{imax}:

$$CNT_{res} \geq \frac{f_c + K_s \cdot x_{imax}}{f_s}. \tag{5.3}$$

The DC part coming from f_c/f_s is not interesting, and thus it is not needed to count that part in the modulo-2^n counter. If a maximum signal swing at the input is within $\pm x_{imax}$ the number of steps necessary is given from:

$$CNT_{m2} \geq int\left[\frac{2K_s x_{imax}}{f_s}\right] + 2. \tag{5.4}$$

The last 2 are added to ensure enough range, since $K_s \cdot x_{imax}/f_s$ is probable not an integer. Even though CNT_{m2} should be rounded to the nearest value of 2^n higher than CNT_{m2}, it will usually be somewhat lower than CNT_{res}.

Now imagine the simplest modulo-2^n counter with $n = 0$. Such a counter with only two steps will be a legal option in some designs. This means, that the internal word length will be a single bit. The delay in the differentiator is only a D flip-flop, and the subtracter throwing away the borrower bit reduces to a single XOR gate. if the counter now counts half VCO periods, the output will be as shown in Fig. 5.4.

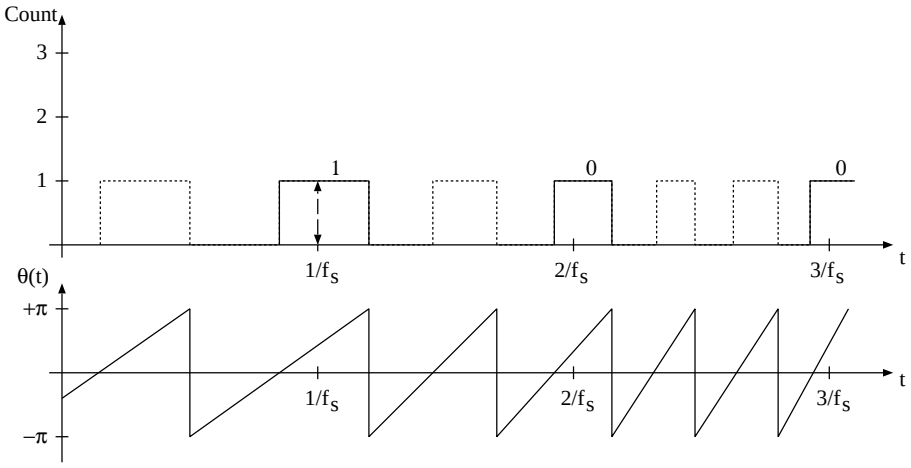

Figure 5.4: FDSM output using 2 stage counter

It is seen, that the shaded counts will not influence the result. It is also seen, that the output of the counter follows the sign of the wrapped phase, which is the same as the sign of amplitude of the VCO output signal, assuming an amplitude of $\pm V_{ref}$. If the VCO has a sinusoidal output, this simple counter reduces to a clocked comparator, and if the VCO output is a square signal it reduces even further to a D flip-flop. In the latter case, the first order FDSM is named a D flip-flop FDSM, and it is seen in Fig. 5.5. As seen in Fig. 5.4 the D flip-flop FDSM counts both rising and falling edges, meaning phase change of π. The result is, that the signal is doubled compared to the ordinary counter FDSM.

This is a nice and simple solution, but since the "counter" in this solution is only single-bit it will not work with all combinations of f_s and input amplitudes

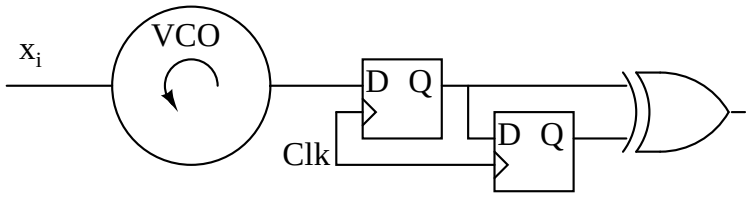

Figure 5.5: The D flip-flop FDSM

due to overflow in the counter. It is clear, that if the output signal from the VCO is oversampled, either none or a single zero crossings will occur. In this case even the strict case for CNT_{res} is fulfilled, and the single-bit counter will provide enough dynamic range.

It is assumed that the free running VCO frequency is much higher than the highest input frequency modulating the VCO. Thus f_s can easily be high enough to oversample the input frequency heavily, but still undersample the VCO output. What combinations of f_s and f_c that can be used, can be examined in both frequency and time domain [22]. In this case a time domain analysis will be presented. It should be remembered, that since only one bit is available, the number of half VCO periods are not allowed to differ with more than at most one period in two adjacent samples. This means, that if P is an integer, only counts of P and $P + 1$ are allowed. Two different examples of sampling frequencies are compared to a VCO output signal in Fig. 5.6.

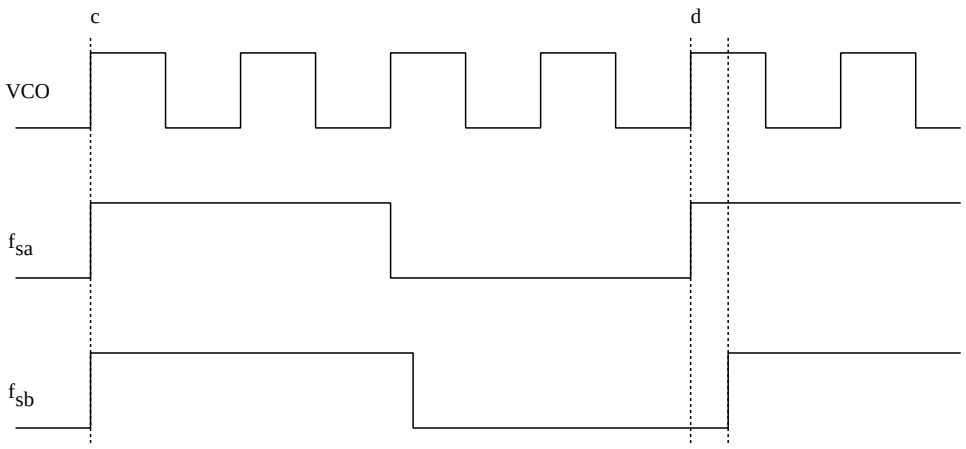

Figure 5.6: VCO signal compared to two different sampling signals

From the figure it is seen, that the period of f_{sa} is an integer of half VCO periods whereas the period of f_{sb} is a quarter of a VCO period longer. If f_{sa} is considered, it is seen, that just a slight phase change controls if the VCO transition (c) is counted

or not at the first sample point (first dashed line). At the next sample point (next dashed line), just a slight change in the VCO frequency will control if transition (d) is counted or not. This means, that with extremely small changes of the frequency (input voltage) the counting can include or exclude the two transitions. Therefore the counter should include three values, which is not allowed in the D flip-flop FDSM. However when using f_{sb}, it is seen, that small variations in phase and frequency will only cause a difference in the count from transition (c). This means, that selecting f_{sb} as the sampling frequency will result in a stable D flip-flop FDSM, even if a small signal is applied to the input of the VCO.

To summarize, the sampling period T_s is not allowed to equal an integer number of half VCO periods T_{VCO}. If P is still an integer this can be written:

$$\frac{2T_s}{T_{VCO}} \neq P \tag{5.5}$$

or if written with frequencies:

$$\frac{2f_{VCO}}{f_s} \neq P. \tag{5.6}$$

f_{VCO} was given in (5.1). If a sinusoidal signal is applied to the input, all of the input values need to result in a legal count. When the minimum value x_{imin} of the sinusoid is applied, the lowest f_{VCO} is obtained and thus also the minimum count during one sampling period. This number needs to be higher than P:

$$\frac{2(f_c + K_s x_{imin})}{f_s} > P. \tag{5.7}$$

When the maximum value x_{imax} of the sinusoid ($x_{imin} = -x_{imax}$ if the mean value is zero) is applied, f_{VCO} is increased, and the number of period counts will be higher. The limitation is:

$$\frac{2(f_c + K_s x_{imax})}{f_s} < P + 1. \tag{5.8}$$

It is clearly seen, that if a sinusoidal input is assumed, an optimal sampling frequency allowing maximum input amplitude is given from the mean input x_{imean} (which could be 0) is given from:

$$\frac{2(f_c + K_s x_{imean})}{f_s} = P + 0.5. \tag{5.9}$$

If f_s is decreased, more noise is moved into the conversion band, and it is thus usually not interesting to operate with very low sampling frequencies. Still it can be mentioned, that if $f_c >> K_s \cdot (x_{imax} - x_{imin})/2$ is assumed, the minimum usable sampling frequency is given from [22]:

$$f_s^{min} \approx 2K_s(x_{imax} - x_{imin}). \tag{5.10}$$

5.1.2 SNR and SQNR in D flip-flop FDSM

Calculation of signal to quantization noise (SQNR) can be calculated directly from the knowledge of the modulator principle, whereas noise produced in the VCO is needed to calculate the complete SNR. In both calculations the signal amplitude at the output A_o is used, and if quantization noise power is N_q, SQNR is given as:

$$\text{SQNR} = 20log\left(\frac{A_o}{\sqrt{2}}\right) - 10logN_q. \tag{5.11}$$

The output signal is found from the time domain output stream. If a high OSR is assumed, the input signal can be seen as a constant within one sampling period. The D flip-flop FDSM equals a counter FDSM counting half VCO periods, and the output stream is given from [22]:

$$y_n = q\left[2T_s\sum_{i=-\infty}^{n}(f_c + K_s x_i)\right] - q\left[2T_s\sum_{i=-\infty}^{n-1}(f_c + K_s x_i)\right] \tag{5.12}$$

where $q[g]$ is quantization of g. During the quantization operation, a quantization error e is added to the value at the input to the quantizer. The result is an output bit stream of:

$$y_n = 2T_s(f_c + K_s x_n) + e_n - e_{n-1}. \tag{5.13}$$

From this equation it is clear that the output bit stream will contain a DC part of $(2T_s f_c)$ and a shaped quantization noise $(e_n - e_{n-1})$. The signal part of (5.13) is $(2T_s K_s x_n)$, and thus the equivalent maximum output signal amplitude is:

$$A_o = \frac{2K_s(x_{imax} - x_{imean})}{f_s}. \tag{5.14}$$

It was proved in section 2.3.2, that the quantization noise was high pass filtered with the same noise transfer function as in the ordinary feedback modulator. In the frequency domain this transfer function is given from [27]:

$$|N_{TF}(f)| = 2sin\left(\frac{\pi f}{f_s}\right). \tag{5.15}$$

It can be shown, that if the quantization noise is assumed to be white, the constant spectral noise density k_x is given as [27]:

$$k_x = \left(\frac{\Delta}{\sqrt{12}}\right)\sqrt{\frac{1}{f_s}}. \tag{5.16}$$

If it is assumed that OSR is high, the $sin((\pi f)/f_s)$ function in (5.15) can be approximated as $((\pi f)/f_s)$, and with a conversion band limited at f_b quantization noise at the output of a first order modulator can then be found as:

$$N_q = \int_{-f_b}^{f_b} k_x^2 |N_{TF}(f)|^2 df \approx \frac{\Delta^2\pi^2}{36}\left(\frac{2f_b}{f_s}\right)^3. \tag{5.17}$$

When (5.14) and (5.17) are used, the SQNR for the D flip-flop is given as:

$$\text{SQNR} = 20 \cdot log\left(\frac{\sqrt{2}K_s(x_{imax} - x_{imean})}{f_s}\right) - 10 \cdot log\left(\frac{\pi^2}{36}\left(\frac{2f_b}{f_s}\right)^3\right). \quad (5.18)$$

It is seen, that Δ is not included in the SQNR. The reason is, that the D flip-flop is always single-bit, and since both signal and noise are normalized with the supply voltage, Δ always equals unity in the D flip-flop FDSM. It is interesting to notice from the equation, that the noise is reduced by 9 dB/octave as usual for a first order modulator. At the same time the signal is reduced with 6 dB/octave, and thus the net profit is only 3 dB/octave. The system should however be seen in a bigger perspective, since other optimizations through f_c and K_s can be made to overcome the signal degradation.

Calculation of SNR requires knowledge of noise power injected by the circuits in the FDSM (N_{int}). Measured noise will of course also include external noise applied from the input source, supply, coupling etc. If this is not included, and if it is assumed, that internal noise and quantization noise is uncorrelated, SNR is given as:

$$\text{SNR} = 20 \cdot log\left(\frac{A_o}{\sqrt{2}}\right) - 10 \cdot log(N_q + N_{int}) \quad (5.19)$$

In section 3.2.2 the phase noise in an oscillator was shown. Since the signal is converted into phase after the VCO, this phase jitter (3.23) is directly added to the signal. Clock oscillator jitter is not included in this section, and since the differentiator is digital, it can be assumed noiseless. To ease up calculations and since $f_s >> f_{1/f}$, white noise is assumed. The noise will be distributed in the band up to $f_s/2$, and the noise in the conversion band up to f_b is:

$$N_{int} = (\sigma_{\Delta\phi})^2 \frac{2f_b}{f_s}. \quad (5.20)$$

ω_0 in (3.23) is the frequency with x_{imean} at the input, and the reference period ΔT in $\sigma_{\Delta T}$ is the sampling period, resulting in an internal noise given from:

$$N_{int} = \left(2\pi(f_c + K_s x_{imean})\kappa\sqrt{\frac{1}{f_s}}\right)^2 \cdot \frac{2f_b}{f_s} \quad (5.21)$$

The internally produced noise is differentiated as the quantization noise. This means that output referred phase noise is converted back into 1/f noise and white noise.

5.2 Other features of the implemented FDSM

This type of converter has potentially a low power consumption depending on the VCO used. Digital circuits and thus also flip-flops can easily be operated far below

the threshold voltage of a transistor, and the complete FDSM is capable of low supply voltage operation depending on the VCO type. Thus the selection and optimization of the VCO is crucial for the converter, and it is commented in this section. Also discussed are noise problems not included above, as well as multi-bit and differential solutions.

5.2.1 VCO optimization for the FDSM

Here only the most important considerations are presented since this topic is thoroughly discussed in paper 3 and paper 4. In principle all types of VCOs can be used in the FDSM, but in the D flip-flop a VCO based on the nonlinear square signal oscillator type is advantageous since a D flip-flop can have problems detecting signals near the zero crossings correctly.

The inverter ring oscillator Fig. 3.4 is a square output oscillator. Another feature of this oscillator type, is that no bias currents are needed and thus no active transistors are needed. The oscillator only includes digital inverters, which as the other digital circuits can be operated at very low supply voltages, and thus there are no blocks in the FDSM requiring supply voltages above the threshold voltage. The complete single-bit FDSM is seen in Fig. 5.7.

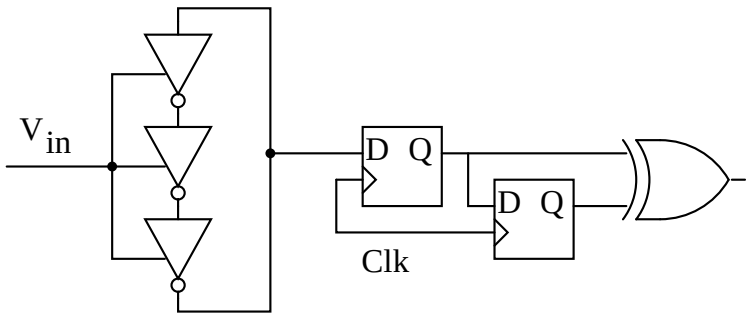

Figure 5.7: Complete FDSM with a three stage oscillator included

The frequency of the oscillator can be controlled in various ways, but through a discussion in paper 4 the optimal solution is found to be to control either the p or the n-MOS transistor bulk terminal. This will modulate the threshold voltage of the transistor, and thus also the maximum drain current I_D. In weak inversion operation this current is proportional to:

$$I_D \propto e^{-\gamma\sqrt{2\phi_f - x_i}/nV_T} \tag{5.22}$$

where γ is a process constant, ϕ_f is surface potential in the MOS transistor, n is a fitting parameter and $V_T \approx 26\ mV$ is the thermal voltage.

The frequency is linearly dependent of I_D, but as it is seen in (5.22), I_D is not linearly proportional to the input signal. The sensitivity of the VCO K_s is the first derivative of the frequency as a function of input voltage. Using the bulk controlled inverter ring VCO directly results in a sensitivity which is increasing with the input signal. A non constant sensitivity will introduce a nonlinearity in the signal path seen as harmonic distortion at the output. This is a problem often not addressed in publications, since the VCO signal is expected to be supplied from an external radio FM signal [12] [49] [57].

The linearity is improved according to the so-called soft rail principle by adding a bias transistor at the supply of the VCO (Fig. 5.8). This transistor reduces the supply voltage to the VCO when I_D (and frequency) is increased through x_i, which results in a negative feedback, reducing the sensitivity of the VCO when the input signal is increased.

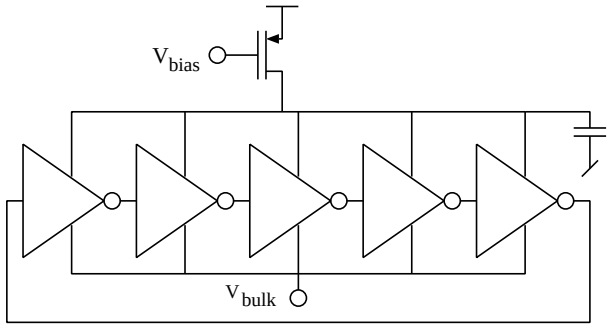

Figure 5.8: Bulk controlled VCO with soft rail bias transistor

The principle was proved through SpectreRF simulations of a 5 stage VCO supplied with 0.2 V, and in Fig. 5.9 it is seen, that the linearity is indeed improved with a correctly adjusted soft rail bias transistor. The trade-off is that K_s is reduced which in some systems is disadvantageous. The simulation is made for a full scale sweep of the input voltage. Due to the monotonic K_s curve, the linearity improves for a reduced input signal swing.

5.2.2 Noise sources in the FDSM

The VCO phase noise, which is the primary noise source in the FDSM, has already been discussed in the previous section. Other secondary noise sources are pattern noise, clock jitter, flip-flop metastability, substrate coupling, cross coupling, supply- and bias noise.

Since the FDSM has the same behavior as the modulator with feedback, it will

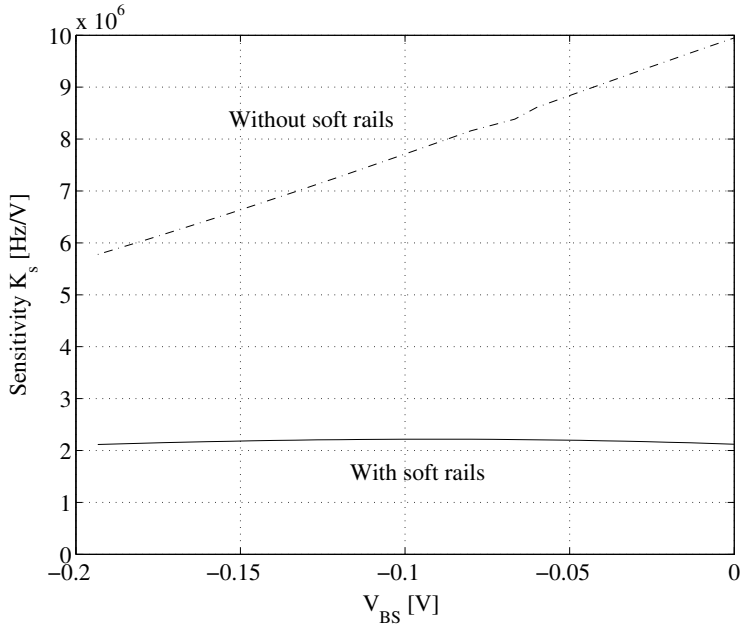

Figure 5.9: VCO sensitivity simulation illustrating impact from the soft rail bias transistor

also create tones at the output, when the input amplitude is low. When these tones come into the conversion band, it is named pattern noise which indeed is a problem since the implemented FDSMs are first order. Since this is a fundamental property even in an ideal modulator, it will always be there. The idle tone pattern is however changed when the DC signal at the input is changed or if f_c is changed up or down. This means that with a carefully designed f_c or an adjusted DC input, most tones will be outside the conversion band, and the total in band pattern noise will be low as shown in [5].

Clock jitter noise is not included in SNR, since the clock generator is not included in the implementations, and thus high power laboratory clock generators with low jitter is used. If this was not the case, the sampling time would be slightly wrong. With the cycle-to-cycle jitter of σ_{cc}, this can be seen as an additional phase at the sampling instance of:

$$\theta_{jit} = 2\pi(f_c + K_s x_i)\sigma_{cc}. \tag{5.23}$$

It is clear, that the clock related noise increases with the VCO frequency. It is however important to notice that due to the location of the sampler, the jitter noise is differentiated and thus shaped as the quantization noise.

The implementations are based on D flip-flops. There are two problems related to the flip-flops, race problems and metastability. The D flip-flop consists of two D latches, and in the first implementation they were connected as illustrated in

Fig. 5.10. The flip-flop shown will sample at falling Clk edges, but the problem is

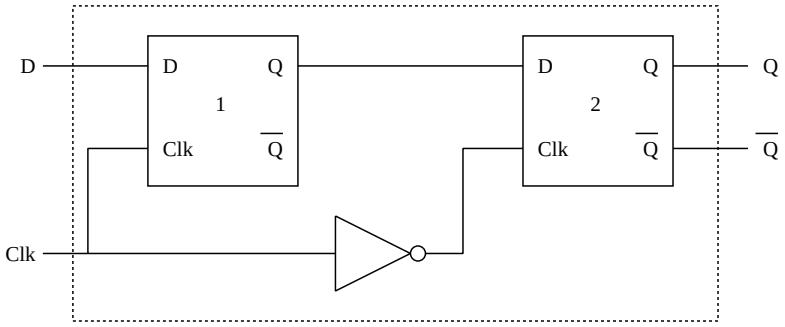

Figure 5.10: The D flip-flop consisting of two D latches

that when Clk is going from low to high, the second latch will close a bit late due to the delay in the inverter, and therefore an extra sampling at the falling Clk edge might occur. This problem is increasing with sampling frequency since the inverter delay is constant, and thus it will limit the speed of the flip-flop. The problem is solved in the second implementation with backwards clocking of the flip-flop by turning the inverter and connect the Clk to the second latch first. In this case the second latch is ensured time to close when the a falling Clk flank occurs, and thus sampling can only occur at rising edges.

Metastability can also cause problems [26]. The flip-flop is a bistable device (stable at 0 and 1), but it has a metastable point in between these two stable points. This means, that the output cannot remain in this state forever, but it might take a while until a stable output is obtained. The metastable point is reached in situations where the input D is close to the metastable point when the sampling occurs. Since the output voltage of the square signal VCO is passing the metastable point fast compared to the sinusoidal VCO, it will be advantageous. To reduce the metastability problem the transition time is also shortened in the second implementation by adding buffers on the VCO output. Each of the D latches in Fig. 5.10 is made with NOR gates as shown in Fig. 5.11. One more attempt has been made to reduce the metastability problem by scaling the NOR gates in the second stage in Fig. 5.11 slightly down compared to first stage. The result is, that the kip-voltage and thus the metastability points of the first and second stages are different. Therefore even if the first D Latch in Fig. 5.10 is at the metastable point, the second D Latch will settle to a stable point, and the complete D flip-flop is stable.

Coupling is a problem in these implementations, since the chip includes both analog inputs, more oscillators at the same time and clocked digital circuits. More initiatives have been made to minimize coupling. First tracks carrying digital and

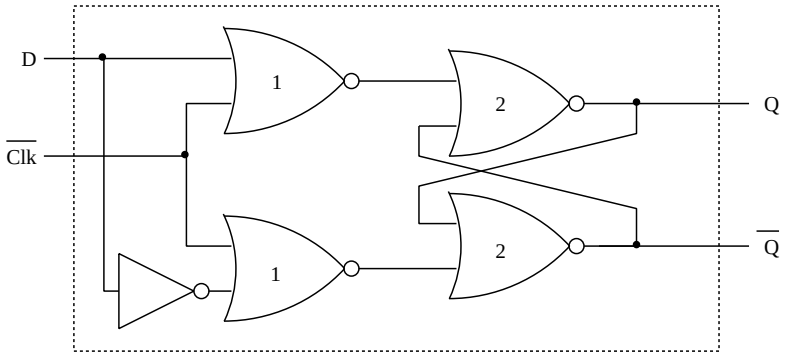

Figure 5.11: D latch consisting of four NOR gates

analog signals are kept separated and the digital and analog blocks have each their decoupling capacitances, power and ground pins. Ground connections can be separated since local isolated p-wells are used for each VCO and each digital block. This also rejects a major part of the substrate injected noise.

Supply noise is problematic since it will modulate the output frequency of the VCO, and thus it is seen as a signal with a gain comparable to K_s. To reduce this noise the decoupling on the test PCB is obviously important, but it is also reduced if the FDSM is made differential as proposed later. It is seen in paper 4 that the soft rail bias transistor greatly reduces the supply noise sensitivity of the VCO. Unfortunately the bias transistor also adds an additional noise input, but paper 4 indicates that the total noise is still reduced when the bias transistor is used, even when both noise inputs are considered. Since the same bias voltage is used in all VCOs, a differential solution is advantageous in this case.

5.2.3 Differential and multi-bit implementation of the FDSM

To improve performance of the FDSM, differential and multi-bit solutions are implemented in the chips designed. The advantage of the differential converter is that harmonics with an equal order as well as common mode signals will disappear. The principle of any differential circuit is, that the input is differential (two inputs x_+ and x_-), and it is assumed that the input signal applied is fully differential as well e.g.:

$$x_+ = A \cdot cos(\omega t) \tag{5.24}$$

$$x_- = A \cdot cos(\omega t - \pi). \tag{5.25}$$

It is clear that the differential signal is $x_{dif} = 2cos(\omega t)$. Nonlinearities introduces terms including $x_+^2, x_-^2, x_+^3, x_-^3$ ....Since $cos^2(\omega t)$ among other terms creates $cos(2\omega t)$

which is the 2nd harmonic, and since $cos^3(\omega t)$ creates $cos(3\omega t)$ which is the 3rd harmonic, the positive output of the differential circuit will include the terms $cos(2\omega t)$ and $cos(3\omega t)$, while the negative output will include terms with $cos(2\omega t - 2\pi)$ and $cos(3\omega t - 3\pi)$. Due to symmetry reasons, the amplitudes will be the same for all harmonics, and thus it is seen that the 2nd harmonic disappears while the 3rd is doubled in the differential result. The signal is also doubled and thus the result is, that all equal order harmonics disappears.

It was seen, that the harmonics disappeared since they were converted into common mode signals. Therefore also common mode noise such as supply noise (including 50 Hz hum) and noise injected at the bias input will be effectively rejected. The noise floor originating from VCO phase noise and quantization noise is however uncorrelated, and thus the noise floor is increased.

In the implementation it is chosen to have two identical converter channels as in Fig. 5.12. One will then be the positive channel and the other is the negative channel. The two results are measured separately. Post processing can then be used to find the differential solution. This is a difficult circuit to implement, since the

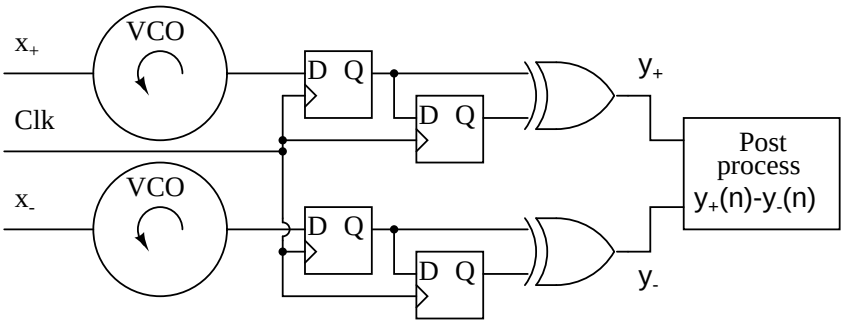

Figure 5.12: The differential implementation of the FDSM

two FDSMs should be completely identical and both cores and connections are thus layed out as mirrored versions of each other, with dummies placed around them to get an effective suppression.

Also a multi-bit solution has been implemented. The principle is to quantize the phase with a multi-bit quantizer. With the usual single-bit approach, the SQNR was given as (5.18). It is however clear, that when a multi-bit quantizer is used, the steps between the adjacent quantization levels are reduced. In (5.18) the quantization noise (5.17) was found using a difference between the quantization levels (Δ) of 1. Using an N level quantizer, Δ is reduced from 1 to $1/N$ and the quantization noise changes

to:

$$N_q = \int_{-f_b}^{f_b} k_x^2 |N_{TF}(f)|^2 df \approx \frac{\pi^2}{N^2 \cdot 36} \left(\frac{2f_b}{f_s}\right)^3 \tag{5.26}$$

leading to a SQNR for the multi-bit FDSM of:

$$\text{SQNR} = 20 \cdot log\left(\frac{\sqrt{2}K_s(x_{imax} - x_{imean})}{f_s}\right) - 10 \cdot log\left(\frac{\pi^2}{N^2 \cdot 36}\left(\frac{2f_b}{f_s}\right)^3\right). \tag{5.27}$$

It is clear, that for each extra bit (doubling of N) in the quantizer, SQNR is increased 6 dB. The analysis concerning sampling frequencies versus input voltage range in the undersampling region remains unchanged from the single-bit solution.

With the single tap used in the D flip-flop, it is difficult to quantize multi-bit since the phase of the square output signal from the VCO can only be detected during the transitions already used in the single-bit solution. When using the inverter ring VCO, it is however quite easy to detect the phase with multi-bit precision if more of the inverters in the ring are tapped. To ensure that all quantization steps are equal, the taps need to be equally spaced in the ring as the example in Fig. 5.13 for a 9 stage inverter ring.

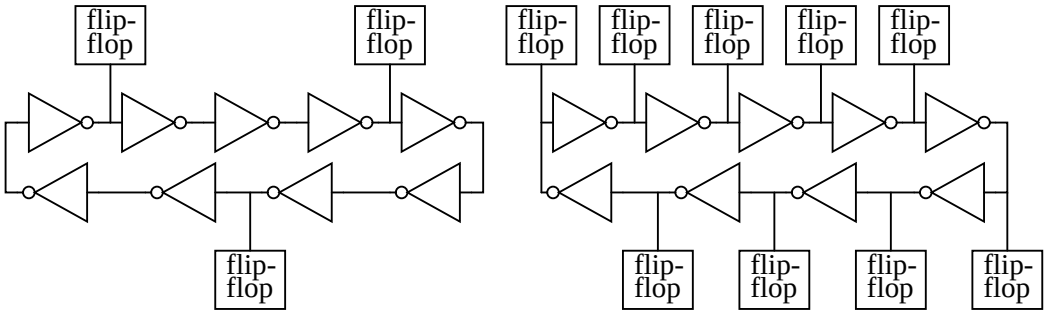

Figure 5.13: Two different solutions on correct tapping of a 9 stage inverter ring

The output from such a multi-bit quantizer is thermometer code like, and thus a binary encoder is encoding the quantizer result before the differentiation. Since the number of inverters in the oscillator is always odd, it is seen, that the allowed number of taps will be odd as well. Therefore the modulo-2^n subtraction cannot be used. This problem is solved with an additional subtraction of the borrow bit as shown for the general multi-bit FDSM in Fig. 5.14. This solution requires however that the number of taps is given as $2^X - 1$ where X is an integer number of bits. This means, that only the 3 tap solution in Fig. 5.13 is working with the solution in Fig. 5.14, and the next usable ring inverter is the 15 stage ring, where 3 and 15 taps will fulfill the requirements. With a multiplication of the borrow bit the circuit in Fig. 5.14 can be extended to operate with a number of taps different from $2^X - 1$.

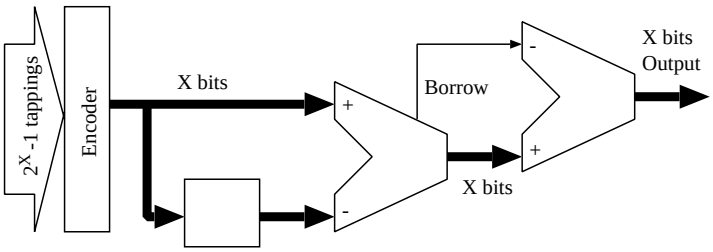

Figure 5.14: General multi-bit FDSM

The above solution is a general solution. In the implementation a VCO with three taps is used, and a customized digital block is made instead of the subtracters. It is seen, that the digital circuit should be able to detect how many taps the transition has moved in the inverter ring since the last sampling, and thus the output with three taps is either 0, 1 or 2 (two bits output in total). The transition edge is found between the two taps both producing either zeros or ones at the same time. Which flank it is, is not important, and thus XNOR gates are added as in Fig. 5.15. After the XNOR gates, the tap last passed by the transition flank will give 1 while the two other will give 0 leaving only three possible $\{A, B, C\}$ outputs $\{0, 0, 1\}$, $\{0, 1, 0\}$ or $\{1, 0, 0\}$. If $\{A_1, B_1, C_1\}$ denotes the present sample, and $\{A_0, B_0, C_0\}$ denotes the

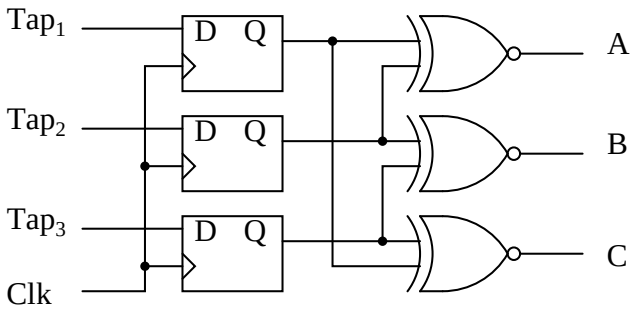

Figure 5.15: XNOR decoding of flank position

previous sample, it is clear that the two outputs $\{D, E\}$ of the complete FDSM, should fulfill the truth table 5.1.

This can be rewritten in a Karnaugh map as in Fig. 5.16, revealing the expressions for D and E is easily found as:

$$D = (B_0 \cdot C_1) + (A_0 \cdot B_1) + (C_0 \cdot A_1) \quad (5.28)$$

$$E = (A_0 \cdot C_1) + (C_0 \cdot B_1) + (B_0 \cdot A_1). \quad (5.29)$$

Table 5.1: Truth table for multi-bit digital block

A_0	0	0	1	0	0	1	0	0	1
B_0	0	1	0	0	1	0	0	1	0
C_0	1	0	0	1	0	0	1	0	0
A_1	0	0	0	0	0	0	1	1	1
B_1	0	0	0	1	1	1	0	0	0
C_1	1	1	1	0	0	0	0	0	0
D	0	1	0	0	0	1	1	0	0
E	0	0	1	1	0	0	0	1	0

Using DeMorgan's theorem [26], this can be rewritten into:

$$D = \left((B_0 \cdot C_1)' \cdot (A_0 \cdot B_1)' \cdot (C_0 \cdot A_1)\right)' \tag{5.30}$$

$$E = \left((A_0 \cdot C_1)' \cdot (C_0 \cdot B_1)' \cdot (B_0 \cdot A_1)\right)' \tag{5.31}$$

and thus D and E can be realized with one three input NAND gate and three two input NAND gates each, and the total multi-bit quantizer and differentiator is implemented as in Fig. 5.17. Using this implementation the multi-bit solution will be as fast as the single-bit solution, since the limitation is still the speed of the flip-flop.

5.3 FDSM implementations

In this section layout and measurements on two different chips with FDSM circuits will be presented, and the properties discussed above will be demonstrated.

		$\{A_0 B_0 C_0\}$					
		001		010		100	
$\{A_1 B_1 C_1\}$	001	0	0	1	0	0	1
	010	0	1	0	0	1	0
	100	1	0	0	1	0	0

Figure 5.16: Karnaugh map for the multi-bit digital block including $\{D, E\}$

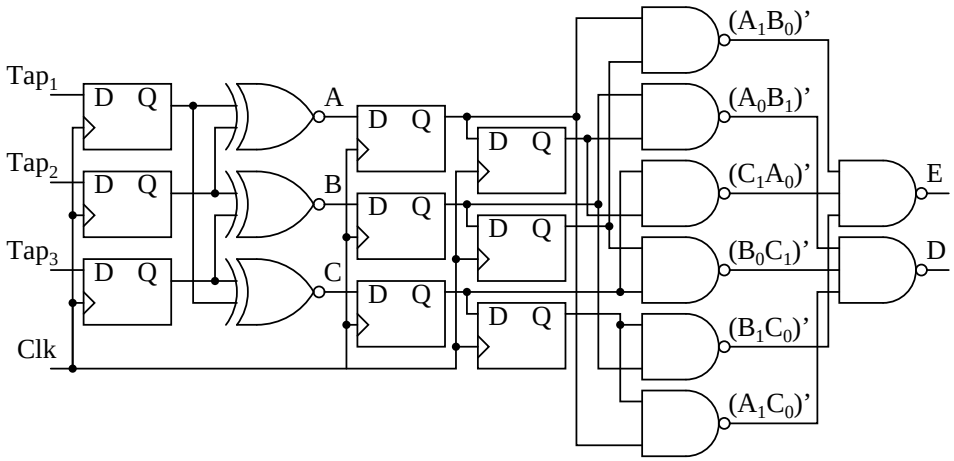

Figure 5.17: Quantizer and differentiator in the multi-bit FDSM

5.3.1 Layout

The two chips are implemented in a 90 nm triple-well process. The following FDSM circuits based on bulk controlled ring inverter VCOs with soft rail bias are on the chips:

Chip 1 Includes two single-bit and one multi-bit D flip-flop FDSM with down-sampled output.

Chip 2 Includes three single-bit (two were intented for differential use) and one multi-bit D flip-flop FDSM.

Increasing transistor lengths of the VCO inverters will increase the loading on inverter nodes and decrease the charging capabilities of the inverters, and thus the length of the transistors control f_c and K_s. The width of the transistors will also change the load, but depending on operation region, the charging capabilities of the transistors will compensate for the change in load, and thus the influence on oscillation frequency from changes to the width is very limited. On the other hand total power consumption of the VCO will increase with increased transistor widths, and according to (3.21) this will reduce the noise. Performance of chip 2 is improved by having wider transistors than in chip 1 as shown in table 5.2. It is seen that all three VCOs in chip 1 have equal dimensions, whereas one of the single-bit oscillators in chip 2 is scaled down compared to the remaining three VCOs in the chip.

Dimensions of the bias transistors are based on simulations. The length of the bias transistor will change the feedback, and a too short transistor might not be able to provide enough feedback to linearize the VCO, whereas a too long transistor

Table 5.2: VCO transistor dimensions for chip 1 and chip 2 in μm (width/length)

Implementation	P-MOS	N-MOS	Bias
Chip 1	6/0.1	3/0.1	10/0.35
Chip 2 (Differential and multi-bit)	60/0.25	35/0.25	100/0.25
Chip 2 (single-bit)	10/0.25	5.83/0.25	16.7/0.25

will narrow the linear operation range. The width of the bias transistor can be compensated after fabrication by the bias voltage, and thus it is not that crucial in the design phase. Bias transistor dimensions are also presented in table 5.2.

In chip 1 the single-bit outputs were split out into two parallel bits coming out with half of the sampling frequency, and the two bits output was split out into four bits. This was done to relax the demands on the output buffers. It turned out not to be necessary, and due to difficulties to acquire the multi-bit results, these output stages were not included in chip 2.

Other improvements in chip 2 were an improved differential design, faster D flip-flops, buffers between VCO and sampler (D flip-flop) and an improved substrate noise immunity since no transistors were placed directly in the substrate. Results from chip 1 indicated same performance from n- or p-MOS bulk input, and thus only p-MOS bulks were accessible in chip 2 to reduce the pin count.

Since the manufacturer of the chips covered them completely with dummy metal, micro photographs do not show any structures and thus the core layout of chip 2 is shown instead in Fig. 5.18. Total dimensions of the core are 270x240μm^2. The layout is not optimized for area, and much of the area is used on decoupling capacitance. It is marked with the rows and columns where soft rail transistors, VCOs, VCO buffers, digital circuits and output buffers are placed in the layout.

5.3.2 Measurements on VCO output

It was seen that f_c is not directly interesting since the FDSM can operate with both under- and oversampling of f_c. Indirectly f_c has some importance, since sensitivity K_s is usually scaled with f_c. K_s controls the complete gain in the system, and the desired value for K_s is thus dependent on the specific application. Since these implementations are only prototypes and thus not designed for a given application (and full scale input), the absolute K_s is of secondary importance, whereas the linearity is extremely important. All measurements in this section are made with 0.2 V supply.

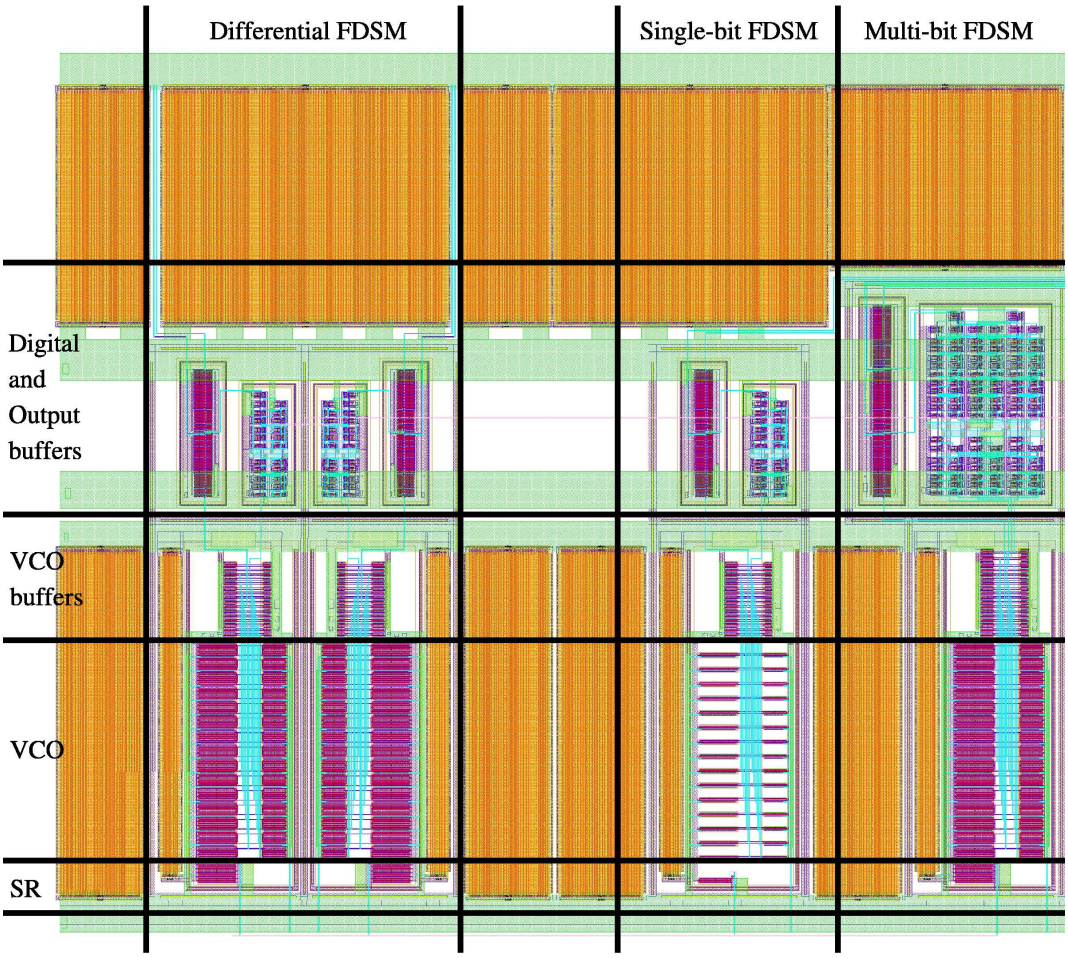

Figure 5.18: Layout of chip 2 core with total dimensions are 270x240μm^2

In the implementations one of the taps from the VCO has been buffered to an output pin. In paper 5 measured results are seen from chip 1. It is clearly seen that the soft rail biasing improved linearity. When the VCO has optimal linearity it is found that $f_c = 14$ MHz and $K_s = 8.7$ MHz/V.

VCO linearity has also been measured for the VCO used in chip 2. Results for output frequency vs. input voltage as a function of the bias voltage is presented in Fig. 5.19.

It is seen, that also in chip 2 the linearity is improved with the soft rail bias. It is also seen, that f_c in chip 2 is reduced compared to measurements on chip 1 due to the increased length of the VCO transistors. The sensitivity derived from Fig. 5.19 is seen in Fig. 5.20. These results indicate that K_s is reduced compared to chip 1 however not as much as f_c reduction. Since the low distortion input source used in SNR measurements does not have DC offset, it is seen from Fig. 5.20 that the FDSM

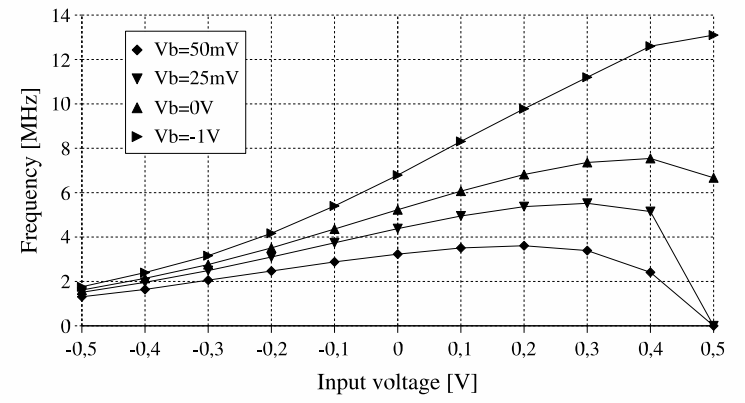

Figure 5.19: VCO output frequency vs. input voltage as a function of bias voltage

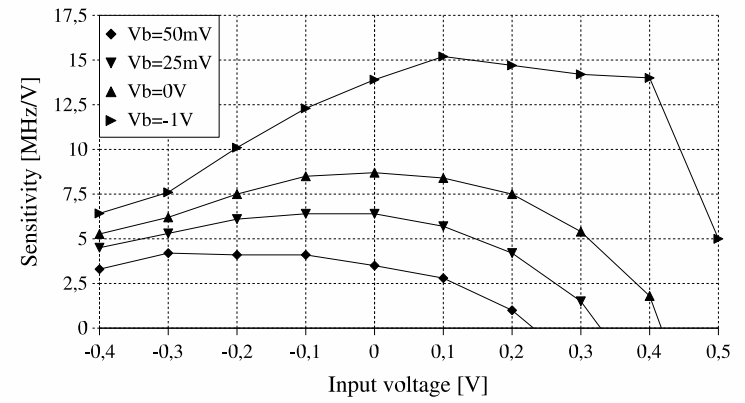

Figure 5.20: VCO sensitivity derived from Fig. 5.19

will provide best linearity with a bias voltage of approximately 0 V.

5.3.3 SNR and SNDR in basic FDSM

Due to the extremely low supply voltage, acquisition of the digital output stream from the FDSM requires either voltage conversion into standard logic levels such as CMOS or TTL, or specialized acquisition equipment with user defined threshold levels. In these measurements a digital acquisition PC card from National Instruments with user defined thresholds was used. To reduce the load on the chip, unity gain buffers were added on the test PCB. Results shown are mean results of at least ten 524288 points spectra acquired with LabView.

It was previously theoretically proved, that the FDSM can operate with both under- and oversampling of f_c. In chip 1 only undersampling was possible since the maximum possible f_s was approximately 5 MHz. This was improved in chip 2 to approximately 20 MHz due to improved flip-flop clocking, and since f_c was reduced

as well, oversampling was possible in chip 2.

SNR and SNDR is calculated with a conversion band from 20 Hz to 20 kHz, and the maximum SNR and SNDR obtained for chip 1 were respectively 47,4 dB and 44,2 dB with a 4 kHz input tone. The spectrum providing the maximum SNDR is presented in Fig. 5.21. This spectrum is obtained with f_s=3.4 MHz and 200 mV supply voltage.

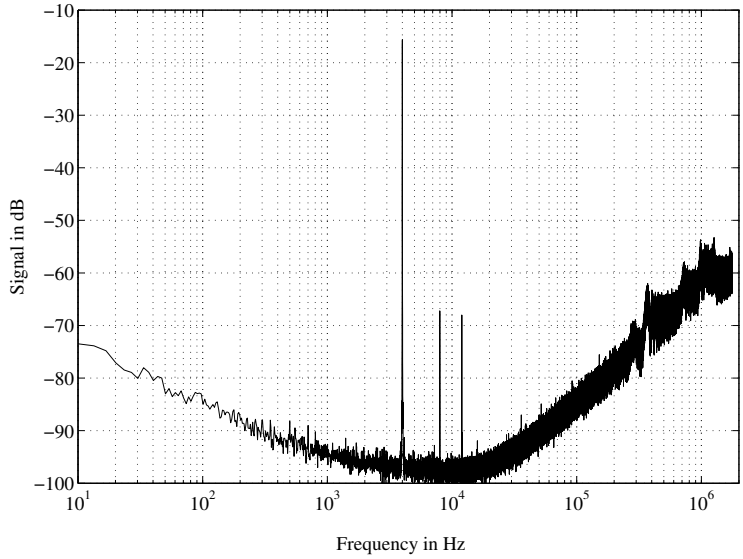

Figure 5.21: Output spectrum measured on single-bit solution in chip 1

It was seen during the measurements, that the amount of harmonic distortion could be controlled with the bias voltage as expected. It is also seen, that the conversion band is dominated by 1/f and white noise which according to theory originates from VCO phase noise. Quantization noise starts to dominate at approximately 20 kHz.

SNR and SNDR for the same chip as a function of applied input signal is presented in Fig. 5.22. The dynamic range (DR) is the range from the maximum allowed input signal to the minimum input signal detectable at the output. DR can be found from Fig. 5.22 to 52 dB.

The power consumption is extremely low, since there are no active biased transistors in the circuits. The VCOs have their own supply, but unfortunately the digital circuits share supply pin with the output buffers, and thus power is measured for both digital circuits and buffers. Usually power consumed by output buffers is not considered, since they are not needed if the circuit is used in a larger system, and thus this power consumption is removed based on a simulation result which gave

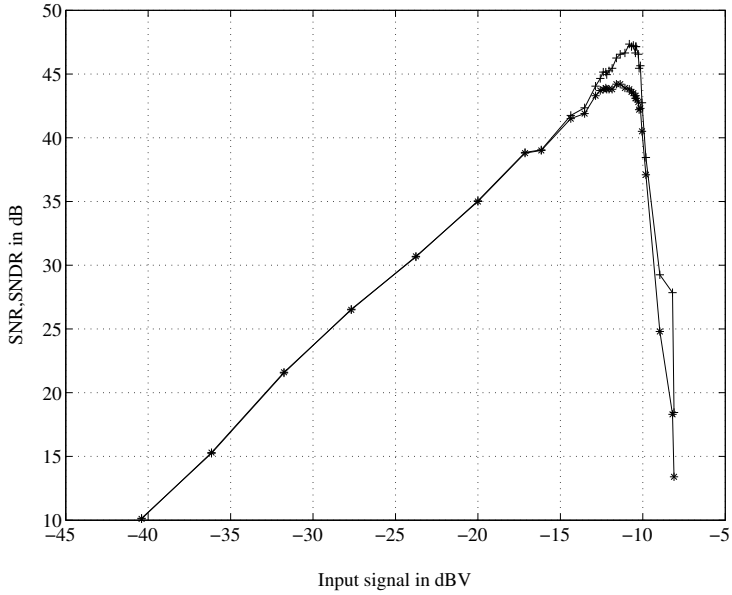

Figure 5.22: SNR and SNDR as a function of input amplitude

a total power consumption very close to the measured result. The total measured power for all three FDSM circuits is 3.5 μW, but when buffer power consumption has been removed, the power of a single FDSM can be found to 0.44 μW.

In chip 2 the power consumption of the VCOs is increased by increasing the widths of the transistors in the VCO. It is thus expected that the SNR is increased accordingly. The linearization principle has not been changed, and thus the SNDR is not expected to increase equally much. The SNDR is however still increased somewhat when the noise floor is lowered since a higher SNDR can be obtained with a lower signal and thus with less distortion. Therefore the SNDR curve is expected to peak at a lower signal level than the SNR, an effect which was not as pronounced for chip 1 in Fig. 5.22. Transistor lengths were also increased slightly (from 0.1 μm to 0.25 μm) since simulations indicated better linearity with this transistor length.

A spectrum measured with an f_s of 6.5 MHz as for chip 2 is seen in Fig. 5.23. It is seen that the noise floor has lowered as expected. The maximum signal at the output is approximately the same as for chip 1. From Fig. 5.24 the SNR is found to 61.5 dB while the SNDR is 54.5 dB. This means an SNR increase of approximately 14 dB. The measured power consumption in chip 2 is dominated by the VCOs, and power share consumed by buffers is reduced to approximately 20 %. After subtraction of the buffer power consumption, the total consumption is 3 μW. This is a factor of 6 higher than in chip 1, and since phase noise depends on $\sqrt{1/P}$, the difference between noise floor in chip 1 and chip 2 should be approximately 8 dB. The increase

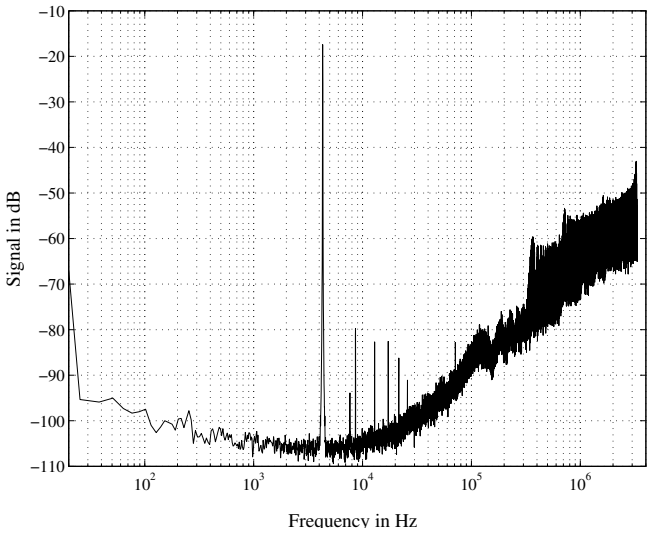

Figure 5.23: Output spectrum measured on single-bit solution in chip 2

of 14 dB is measured at a higher f_s than the results for chip 1, but measurements of chip 2 with f_s=3.4 MHz actually showed a 6 dB increase in SNR compared to chip 1 result. The quantization noise is moved with the increased f_s, but it is still limiting SNR.

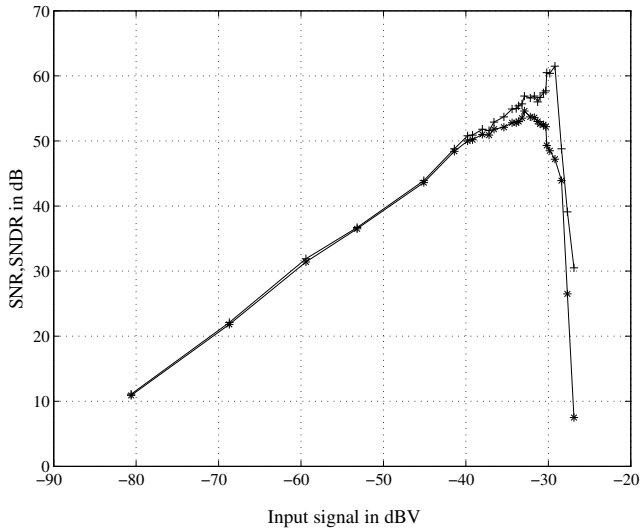

Figure 5.24: SNR and SNDR as a function of input amplitude in chip 2

It should be mentioned that the measurements presented for chip 2 are made with a bias of -20 mV and that a trade-off exists. If the bias is increased, the SNR increases while SNDR is reduced. The fact that SNR increases with the bias voltage

is explored later.

5.3.4 Measurements on the differential FDSM

The measurements on the differential FDSM are made with the same test setup as the basic FDSM above. The only difference is, that two channels are used at the same time. The success of this circuit depends on how well the two channels match. This matching is examined by applying a common mode sinusoidal signal to the two channels. With perfect matching the applied tone should be completely removed in the differential result. Both the single channel result and the differential result is seen in Fig. 5.25. The applied common mode signal is seen to be suppressed

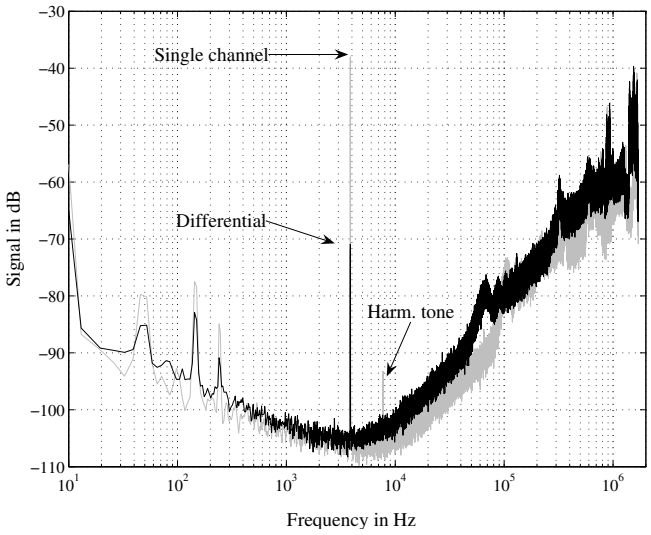

Figure 5.25: Result with common mode signal on the differential FDSM

35 dB which is a good result when based on pure matching between two independent channels. The second harmonic has also disappeared in the differential result. It was also expected that the 50 Hz noise would disappear, but it is only suppressed about 5 dB. This indicates, that the 50 Hz is not coupling as a common mode signal. However in another measurement without common mode signal applied, the 50 Hz tones was the only signal found in the spectrum from each of the channels, and in this measurement, they were completely removed in the differential result.

The 1/f noise and the white noise from the two channels are uncorrelated noise and thus the differential noise floor will be 3 dB higher than in a single channel. This also fits measurements at low frequencies. At frequencies where quantization noise starts to dominate, the difference is increased, which might indicate that the

quantization noise is not completely uncorrelated. At higher frequencies, the slight unmatch between the two channels results in quite different tonal behaviors, and thus the differential result will be dominated by only one of the channels at a time.

Fig. 5.23 indicated that the second harmonic is dominating SNDR in chip 2, and thus improved SNDR is expected when adding a differential input signal. Since the differential signal at the output will be 6 dB higher while the noise floor increases only 3 dB, the SNR is also assumed to increase 3 dB.

Measurements also indicate, that the noise floor from the VCO actually decreases when the supply voltage is decreased, which might be due to the decreased f_c. On the other hand the digital circuits becomes slower with decreased supply voltage which is a disadvantage. If the bias voltage is increased slightly, the supply voltage to the VCO is decreased while the digital supply is constant. That this changes the noise floor is seen in Fig. 5.26, where the oversampled (f_s=7.4 MHz) differential FDSM is applied a small constant differential input signal and three different bias voltages.

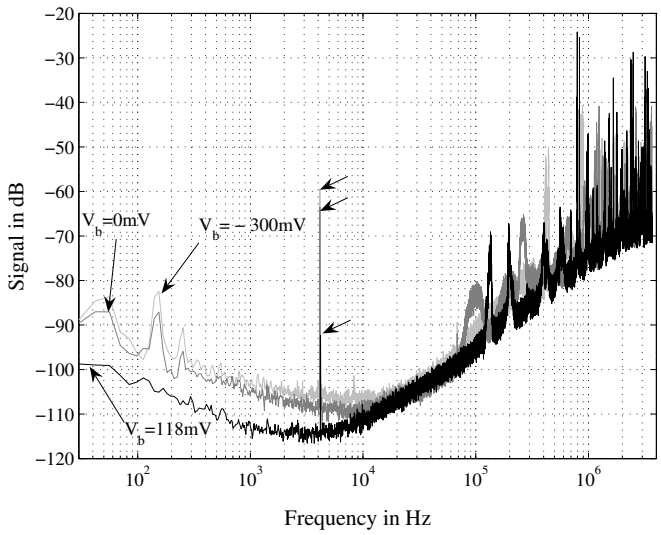

Figure 5.26: Measurements on differential FDSM with bias voltages of -300 mV, 0mV and 118 mV

As expected K_s and thus the overall gain is (seen from signal amplitudes indicated with arrows) reduced when V_b is increased. It should be noticed that the 50 Hz noise assumingly coming from the supply is reduced with higher V_b as well. This indicates that the bias transistor shields the circuit from supply noise as described in paper 4. Except from the tones which are high due to the low input signal, the quantization noise are at the same level in all three measurements, since f_s and the quantizer are the same in all three measurements.

The performance of the differential FDSM with a fully differential signal at the input and with the same f_s as used for the single ended solution gave an SNR and SNDR increase of 3 to 5 dB depending on bias voltage. Maximum SNDR is found from the spectrum in Fig. 5.27 where it is seen that the third harmonic is now dominating.

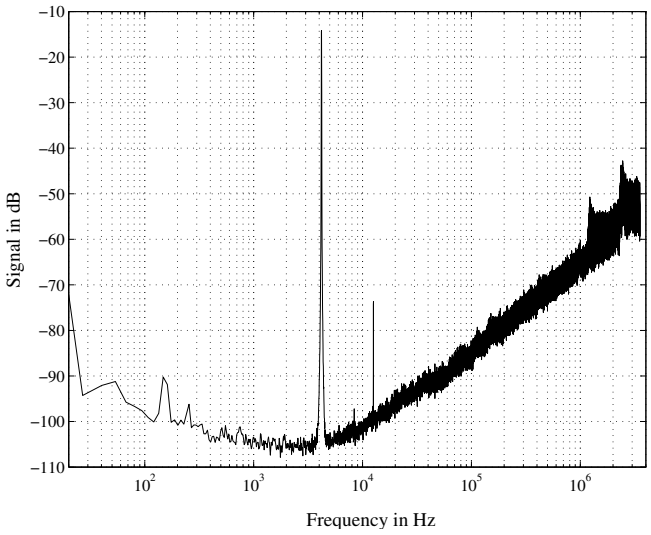

Figure 5.27: Output spectrum measured on differential FDSM

When f_s is increased to 12.2 MHz, measurements give a SNDR of 60.3 dB (9.7 bit). The maximum SNR of the differential FDSM with f_s=12 MHz is 68.9 dB, and in Fig. 5.28 SNDR and SNR are seen as a function of differential input signal.

Usual differential circuits comes at almost no power costs, but in the FDSM two identical circuits are needed, and power consumption of this solution with the same f_s consumes twice the power (6 μW) compared to the single ended solution. Since only 3 dB noise reduction are gained, the differential solution is theoretically not advantageous when considering power consumption. On the other hand if linearity is considered or if other environments with more common mode noise are considered, it is indeed advantageous. Increasing the sampling frequency to 12.2 MHz increases measured power consumption to approximately 7.5 μW.

5.3.5 Measurements on the multi-bit FDSM

Unfortunately only a single ended multi-bit solution was implemented, and thus the same set up as for the basic FDSM was used. Due to the smaller quantization steps, the quantization noise is assumed to be lower than in the single ended solution. This

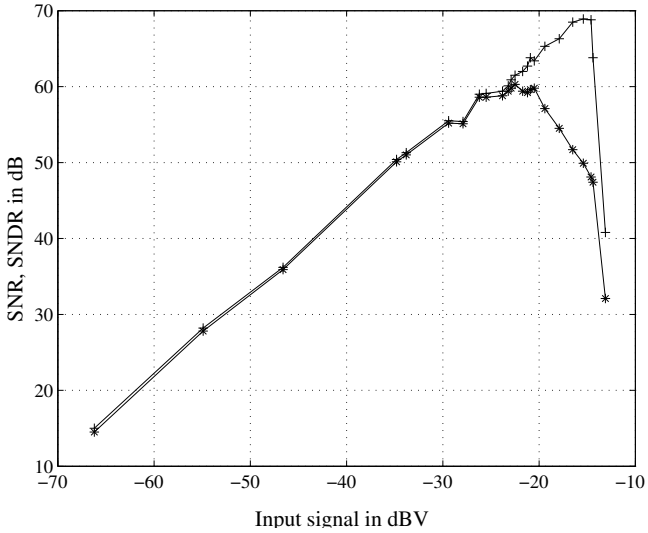

Figure 5.28: SNR and SNDR as a function of input amplitude in the differential FDSM with f_s=12 MHz

is however not what is seen at the output spectrum, since the output stream from the FDSM is detected as the values {0,1,2} and not as assumed in the theory {0,0.5,1}. This means Δ is still 1, but the maximum signal has instead increased 9.5 dB while the quantization noise remains at the same level.

All three taps used includes signal and thus the signal is increased, but unfortunately they also include noise from the oscillator. This means that 1/f noise and white noise are increased as much as the signal and thus only SQNR is improved. This is illustrated in Fig. 5.29 where input signals with equal amplitudes but slightly different frequencies are passed through both a single-bit FDSM and a multi-bit FDSM, and the results are compared.

The measured spectrum for maximum SNDR with f_s=6.3 MHz is presented in Fig. 5.30. From the results on SNR and SNDR which are 60.9 dB and 54.8 dB respectively, it is seen that the system is not limited by quantization noise, since the results are approximately the same as for the single-bit solution.

This implementation uses the same VCO as the single tap solution, and since the digital power consumption is very limited compared to the analog consumption, this solution only requires 10 % increase in power consumption (3.3 μW). It is however only a power efficient implementation in systems limited by quantization noise, and where an increased sampling frequency is not an option. It could also be used in systems where idle tones should be limited, since the amplitudes of the idle tones scales with Δ.

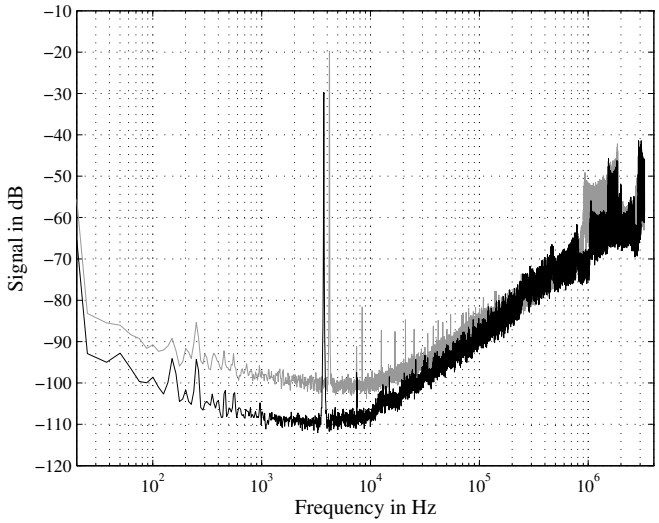

Figure 5.29: Comparison of single-bit and multi-bit FDSM

5.3.6 Figure of merit for FDSM

It is interesting to compare the performance of the FDSM to that of the $\Sigma\Delta$ with feedback, and thus the FoM is calculated according to (4.78). In the previous sections, both measured SNR and power consumption for the different implementations of the FDSM are found, and the corresponding FoM results are calculated in table 5.3.

Table 5.3: Measured FoM for different FDSM implementations

Implementation	SNR [dB]	Bits	Power [μW]	FoM [fJ/conv]
Chip 1 (Single-bit)	47.4	7.6	0.44	57
Chip 2 (Single-bit)	61.5	9.9	3.0	78
Chip 2 (Differential)	68.9	11.2	7.5	82
Chip 2 (Multi-bit)	60.9	9.8	3.3	93

It is clearly seen, that in terms of performance chip 2 is preferable, while chip 1 provides the best FoM. It should however be mentioned, that power consumption measurements are somewhat inaccurate, since only total power consumptions can be measured, while the distribution inside the chip relies on simulations. To the defense of chip 2 it should also be mentioned that if a high SNDR is sacrificed, the SNR can be slightly increased which will bring down the FoM.

The overall conclusion from chip 2 is that the performance of the FDSM can be increased with increased power consumption, and that the FoM of approximately

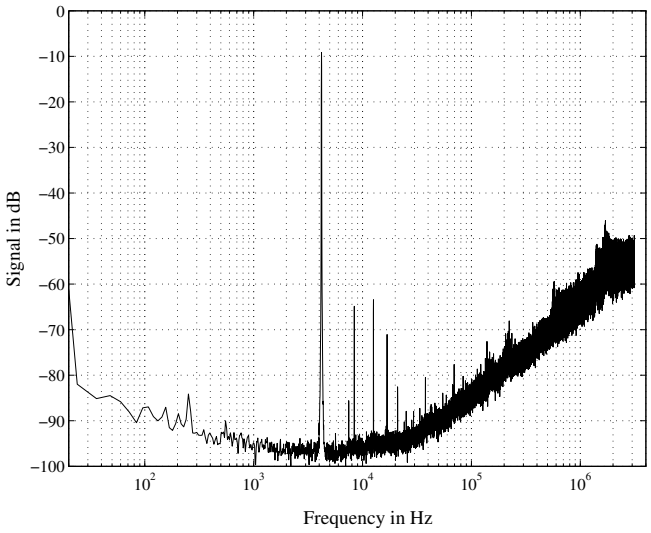

Figure 5.30: Output spectrum measured on the multi-bit FDSM

100 fJ/conv can be expected. Compared to the results in section 4.9.1, FoM for the modulator with feedback is seen to be approximately 5 times the FoM of the FDSM.

Calculated from a FoM of 100 fJ/conv, it is seen that the 16 bit converter theoretically requires only 262 μW, and it might thus be concluded that the FDSM is the optimal solution when discussing converters for hearing aids. Only one basic (but extremely important) problem remains: The FDSM is first order, which (discussed previously) is inappropriate in a hearing aid due to idle tones.

Chapter 6

Conclusion

The starting point for the discussions of this thesis was analog to digital converters for hearing aids. The first priority in these converters is low power consumption. Other parameters that should be fulfilled by the hearing aid converter are sub 1 V supply voltage operation, complete audio conversion band from 20 Hz to 20 kHz and an average conversion precision of 12-16 bits.

The first converter type discussed was the Nyquist converter. This converter type can easily provide a sufficiently high precision, and sub 1 V operation can be obtained in modern CMOS processes with low threshold voltages. Power consumption of the converter itself can be kept at a fair level, but the requirements to the anti-aliasing filter are high. The power consumption of the filter was calculated based on published state of the art filters, and it was shown that if this power consumption was included as well, the total power consumption of this converter type was not competitive any longer.

In oversampling converters the anti-aliasing filter requirements are more relaxed, and thus the well known single-loop, single-bit $\Sigma\Delta$ converter was discussed in two different variants. A variant where the integration is carried out in discrete time (DT) and a variant where integration is carried out in continuous time (CT). The DT topology discussed was a switched capacitor circuit and the CT topology an active RC circuit. The target was to predict how much power a 16 bit (SNR) implementation of these converter types would require and to predict which of the two variants that was most power efficient. This topic was treated theoretically through Matlab simulations. Models of the noise as function of power consumption were obtained. They required the use of an advanced stability model for the converter, since this modulator type has a tendency to become unstable when the modulator order is increased. The models also included power consumed in the clock oscillators, since

the CT modulator is much more sensitive to clock jitter than the DT modulator. On the other hand the bandwidth requirements are lower in the CT modulator than in the DT equivalent. The results indicated that the power consumption in both cases was limited by the slew-rate of the amplifiers used in the integrators, and that the CT implementation was the most power efficient of the two. The total power consumption of the 16 bit converter was 1.46 mW which was slightly too much for the hearing aid application, since the total power budget for all circuits in the application was approximately 1 mW. A figure of merit (FoM) was calculated from the simulated results, and it was 557 fJ/conv.

Using the FoM it was possible to compare the performance of the single-loop, single-bit $\Sigma\Delta$ converter to the last converter type discussed. This was a converter producing $\Sigma\Delta$ noise shaping but without feedback. It was based on integration in a VCO converting the signal into the frequency domain, and thus the converter was named frequency to digital $\Sigma\Delta$ converter (FDSM). The FDSM was able to operate on extremely low supply voltages even below the threshold of a transistor and extremely low power consumptions, since it could be implemented without active circuits. The VCO selected for the implementations presented was the bulk controlled inverter ring VCO, and one of the main topics was to linearize its modulation. This linearization was obtained with the so-called soft rail principle, where a bias transistor created a feedback through a reduction of the supply voltage of the VCO. Various implementations including multi-bit, differential and single ended solutions with different power consumptions were made, and even through measurements they proved extremely efficient operated at only 200 mV supply. 16 bit was not obtained, but measurements on converters up to 11.2 bit (SNR) proved FoM values ranging from 57 to 93 fJ/conv. It was also proved that both differential and multi-bit implementation was feasible. It was also found, that if a FoM of 100 fJ/conv was assumed, the 16 bit converter could be obtained from only 262 μW which was more in the range of a hearing aid. The modulator was, however, only first order, and thus idle tones in the output spectrum might limit the use of the presented FDSM in the hearing aid.

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Appendix A

High resolution Nyquist converter topologies

In this appendix different types of Nyquist converters and the applicability in hearing devices are examined. In converter applications the important parameters to evaluate are conversion speed, resolution and linearity [20] often at the lowest possible power consumption. Three types of converters known to provide possibilities of high resolution A/D conversion are commented [45] [27].

A.1 Integrating converter

Different types of integrating converters are widely used in high resolution and low speed applications. The simplest type is the single slope converter which integrates a reference voltage on the capacitor C while the clock edge triggered binary counter is counting. The count is terminated by a comparator signal when the integrator voltage V_R exceeds the input voltage also giving the name time-division conversion.

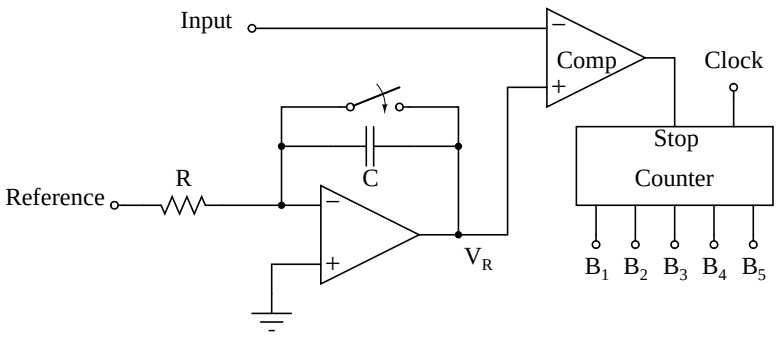

Figure A.1: Schematic of the single slope A/D converter

However the resolution of this type of converter is extremely sensible to process variations in the RC term, reference voltage noise and to the input offset error of the amplifiers. The RC term problem and the amplifier offset error problem can be overcome by using the dual slope converter [45]. An implementation of this example is presented in the paper 1. The possibility of obtaining 16-bit of resolution with this type of converter has been reported [4] and is therefore interesting. In this type of converter the two slopes are obtained by integrating the input voltage for half a sampling period (2^B clock cycles) [10]. Then the reference voltage is integrated and the binary counter is counting until the comparing level has been reached.

Since the same RC components are used in both integrations, the dependency of the RC term is eliminated. Also input offset error is eliminated since it is included in the beginning of the first integration, where the integrator output is reset to the offset voltage of the integrator amplifier [27].

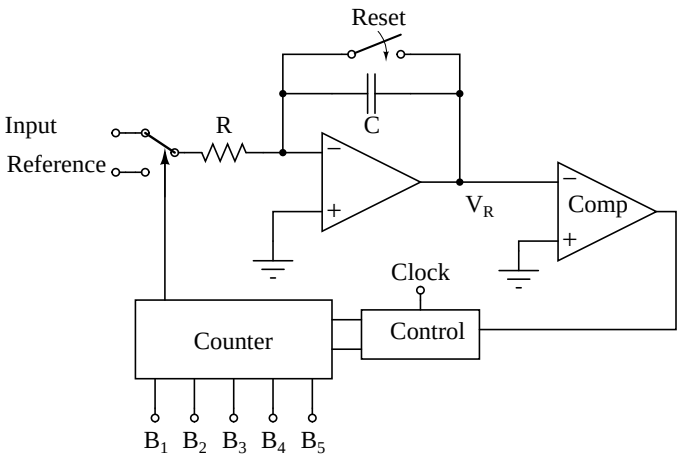

Figure A.2: Schematic of the dual slope A/D converter

In a 16-bit converter the input voltage is integrated for a full clock period counts of 2^{16} followed by the integration of the reference voltage in a partial count giving the digital converted result according to:

$$\text{Partial count} = \frac{V_{in}}{V_{ref}}\text{full count} \tag{A.1}$$

According to this a converter with full scale input voltage of V_{ref} has a worst case counting time of two full counts. For a 16-bit converter the clock frequency supplied should be at least 5.8 GHz to obtain 44 kHz sampling. Even though the speed can be improved by using multi-slope implementations [55], this fact reveals that the integrating converter is to slow for this application.

A.2 Successive approximation converter

The successive approximation converter has faster conversion times than the integrating converters although it still obtains a relatively high resolution [46] even at low voltage supplies [38]. At relatively high sample frequencies of a few MS/s 4-6 bit, are still easily obtainable, and pipelining can result in high resolution converters at medium frequencies. With this approach a 12 bit converter at 5 MS/s using only 0.19 pJ/conversion has been reported [34]

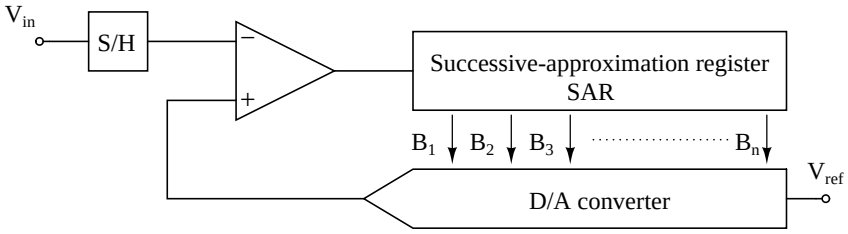

Figure A.3: Schematic of the successive approximation A/D converter

The principle of the converter is to guess the result. First all of the bits are 0 except for the most significant bit (MSB) which is 1. This result is converted in the D/A converter giving half of the reference voltage applied to the D/A converter, which is compared to the input voltage. If the input voltage is larger than half of the reference voltage the output from the comparator is 0 with the sign conventions from figure A.3 and the MSB is known to be one. Then the next bit is changed to 1, and the bit combination is converted in the D/A converter and compared to the input voltage. This process is continued until all of the bits have been determined. This means, that only a number of clock cycles corresponding to the number of output bits are needed. For a 16-bit converter sampling at 44 kHz the clock frequency should be at least 700 kHz.

In this type of converter, the quality of the conversion is depending on the type of D/A conversion used. Often used D/A converter types are the R-2R based converters, the charge-redistribution capacitor converter, the thermometer based converter, the charge-redistribution switched-capacitor converter or hybrid converters formed from a combination of the different converter types [27].

In Fig. A.4 the R-2R approach to the D/A conversion is illustrated with a 4 bit converter. The digital bit combination is applied to the switches B_1 to B_4. Because of the R-2R ladder the currents switched in or out are binary scaled, and the converted output is obtained by the current to voltage conversion formed by the amplifier and the resistor R_F.

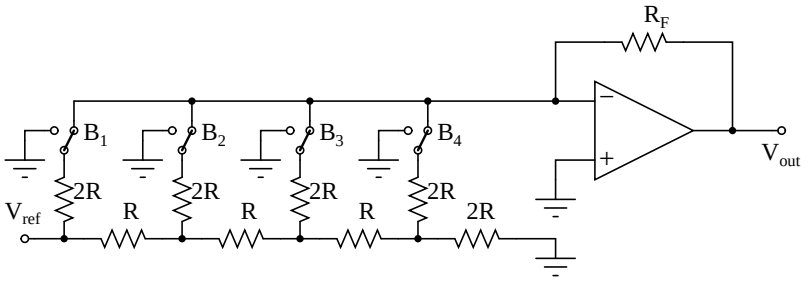

Figure A.4: The R-2R approach to D/A conversion in a successive approximation A/D converter

This type of converter uses as few current paths as possible, and it can be extended to a large number of bits since the component values do not scale with the number of bits. This also means, that common centroid layouts increasing the linearity is easily implemented. The drawbacks of the R-2R approach are that monotonicity is not ensured because of the binary weighting, and the power consumption is high because of the current giving a continuous power consumption.

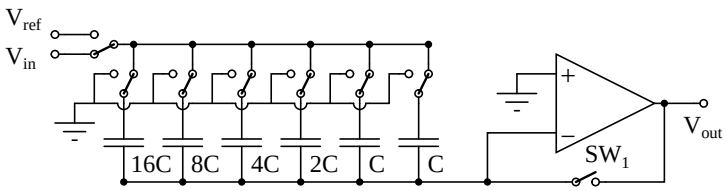

Figure A.5: The charge redistribution approach to D/A conversion in a successive approximation A/D converter

The charge redistribution approach is seen in Fig. A.5. In this case the comparator seen in figure A.3 is also included in the D/A conversion, and the output is connected directly to the SAR. In this topology the signal carrier is charge, and the amount of charge transfered for each bit is binary scaled by scaling the size of the capacitors switched in or out. The conversion is obtained by applying V_{in} to all of capacitors while the comparator are reset through the switch SW_1. By switching in the capacitors in the successive approximation method, the converted digital bit combination is compared to the analog input voltage.

This type of converter has a low power consumption since there is no static current running in the circuit, and because an amplifier can be spared compared to the other solutions. The drawbacks are, that monotonicity is still not ensured, and that the capacitor areas are growing exponentially with the number of bits, reducing the number of bits possible. Because of the capacitor scaling the common centroid

layout is not as easily implemented as in the other converter types.

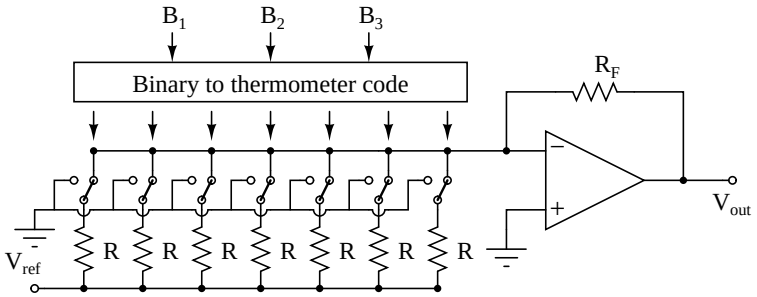

Figure A.6: A resistive thermometer approach to D/A conversion in a successive approximation A/D converter

The thermometer approach illustrated in Fig. A.6 can be implemented both as a resistive and a capacitive implementation. In this case the Bit combination coming from the SAR is thermometer decoded, and each switch applies the same current to the resistor R_F which is converting the current into a voltage.

The important advantage with the thermometer approach is that it is always monotone. Also in this case the components have the same value giving the possibility of obtaining a high number of bits and effective common centroid layouts. The drawbacks are the relatively high power consumption because of the continuous current consumption and the high number of current path components needed. The current path component count is $2^B - 1$ compared to B in the R-2R converter.

The hybrid converter type is used to combine the different advantage from other types of converters. An example is to combine a thermometer array at the MSBs to obtain monotonicity and an R-2R ladder at the LSBs to reduce the overall number of current paths [38]. Another example is to combine the charge redistribution converter with a resistor string to obtain a higher number of output bits [46].

A.3 Algorithmic converter

The algorithmic A/D converter or the cyclic A/D converter also in principle uses one clock cycle to produce one output bit. It is based on the same dividing principles as the successive approximation converters, but in this case it is the input voltage that is multiplied by 2 for every bit produced as illustrated in Fig. A.7

In this type of converter the circuit multiplying by two are crucial for the overall performance of the converter because of the cyclic behavior of the converter. The circuit seen in Fig. A.8 are multiplying the input voltage by two without introducing

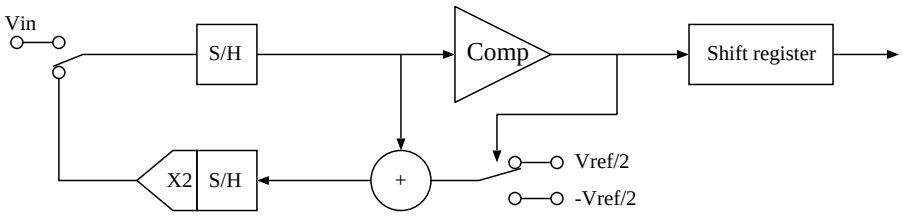

Figure A.7: Block diagram showing the signal flow in the algorithmic converter

errors due to input offset voltage in the amplifier, and it is independent of process variations in the capacitances [27] [35].

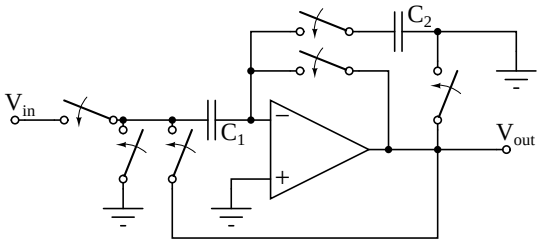

Figure A.8: Matching independent circuit multiplying input signal by two

To operate the switches correctly four cycles are needed. The complete converter proposed by Li [35] produces one output bit for every six clock cycles with this type of multiplier. A speed improvement to three clock cycles for a matching independent converter has been proposed in [42]. In both cases charge injected from the switches are an important performance reducing parameter since the multiplication is depending on charge transfered between the capacitances in the circuit. By using a precise switching timing and a differential version of the circuit shown in Fig. A.8, the charge injection problems can be reduced significantly [35].

Appendix B

Basic component noise sources

Noise produced in components is distributed with a given spectral density for a given component type, where spectral density is the noise voltage produced in the component squared per Hz (V_n^2). The two most common types of noise are white noise where the density is a constant independent of frequency and 1/f noise where the spectral density is proportional to 1/f. The two types of noise are illustrated in Fig. B.1. It is seen, that the 1/f noise are most pronounced at low frequencies, and since 1/f noise theoretically is ∞ at DC, a 1/f noise corner is always present.

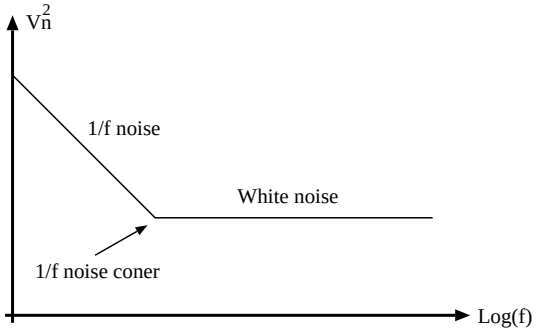

Figure B.1: Noise spectral density for white noise and 1/f noise. 1/f noise corner is shown

Since spectral density is the noise per Hz, the total RMS noise power can be found by integrating the complete frequency spectrum as:

$$V_{n(RMS)}^2 = \int_0^\infty V_n^2(f)df \tag{B.1}$$

It is obvious, that a white noise source has a RMS noise going to ∞. This is however only the case for the noise source alone, when the component producing the noise is used in a circuit, the noise source will be band limited and (B.1) reveals a finite value.

B.1 Passive components

Of the passive components only the resistors are noisy components. The noise in resistors is thermal noise, and it can be modeled as a white noise voltage source in series with a resistor or a white noise current source in parallel with the resistor. The noise is named thermal, since it originates from thermal excitation of the charge carriers in the material, and it is therefore proportional to the absolute temperature [27]. The noise in a resistor is illustrated in Fig. B.2 and the spectral density is given in (B.2) where k is Boltzmann's constant, T is the absolute temperature and R is the resistance.

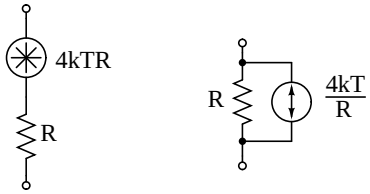

Figure B.2: Noise models for a resistor

$$V_{nr}^2(f) = 4kTR \tag{B.2}$$

The capacitor do not introduce noise, but when it is charged it is normally through some resistive elements introducing noise, and in this case an RC term band limits the noise is obtained as shown in Fig. B.3.

$$V_{nc}^2 = 4kTR\left(\frac{\pi}{2}\frac{1}{2\pi RC}\right) = \frac{kT}{C} \tag{B.3}$$

It is seen, that the capacitor can be seen as having a noise source independent only dependent of the capacitance C [32]. This noise also has to be included in switched capacitor circuits, since the capacitor is charged through a resistive MOS transistor.

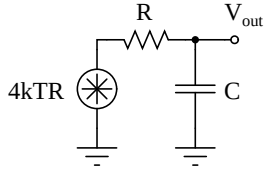

Figure B.3: RC noise bandwidth limitation

B.2 Active components

Of the active components only the MOS transistor is important to discuss to fulfill the noise study of this work. This type of component generally has three types of noise when it is operating in the active region. The first noise type included is a white noise introduced in the component due to the resistive channel in the transistor. The input referred white noise spectral density is given in (3.8). The factor γ is a process and transistor size dependent constant. For long devices γ approximates 2/3. g_{d0} is the transconductance for zero drain source voltage.

The MOS transistor also includes 1/f noise. In (3.9) the spectral noise density is shown as an input referred noise voltage density. K_f is a process constant used in SPICE2 simulations. C_{ox} is the oxide capacitance, W is the width of the transistor, L is the length of the transistor, μ is the charge carrier mobility and f is the frequency.

$$V_{wnm}^2 = 4kT\gamma\frac{g_{d0}}{g_m^2} \approx 4kT\gamma\frac{1}{g_m} \tag{B.4}$$

$$V_{fnm}^2 = \frac{K_f}{2C_{ox}^2\mu WLf} \tag{B.5}$$

The third type of noise in the transistor, not included in this model, is the gate noise. This is a white noise due to the resistance present in the gate of the transistor. This noise is not included in the model due to the relatively low frequencies used meaning that the impedance of the gate source capacitance is extremely large resulting in an extremely small gate current [32]. In Fig. B.4 the noise model of the MOS transistor is shown. The white noise contribution is coming from the channel in the MOS transistor and is thus intuitively a noise current in the drain path, but can as well be transfered to the input as shown in the figure.

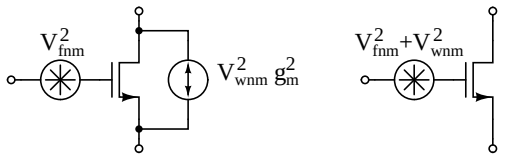

Figure B.4: Noise model for a n-MOS transistor

Appendix C

Publications

The following publications were presented during the study:

Paper 1 Ulrik S. Wismar, Arda D. Yalcinkaya, Ole Hansen, "A Low-Power CMOS Interface Chip for Data Logging Applications". *Proc.* 17^{th} *EUROSENSORS Conference*, pp. 494-495, Portugal, Sept. 2003.

Paper 2 Ulrik Wismar, Jannik Nielsen, Pietro Andreani, "Impact of oscillator Power in Discrete and Continiuous time $\Sigma\Delta$ Converters". *Proc.* 22^{nd} *IEEE NORCHIP Conference*, pp. 127-130, Norway, Nov. 2004.

Paper 3 Ulrik Wismar, Dag Wisland, Pietro Andreani, "Linearity of Bulk-Controlled Inverter Ring VCO in Weak and Strong Inversion". *Proc.* 23^{nd} *IEEE NORCHIP Conference*, pp. 145-148, Finland, Nov. 2005.

Paper 4 Ulrik Wismar, Dag Wisland, Pietro Andreani, "Linearity of Bulk-Controlled Inverter Ring VCO in Weak and Strong Inversion". *Springer Analog Integrated Circuits and Signal Processing*, Vol. 50(1), p.59-67, 2007.

Paper 5 Ulrik Wismar, Dag Wisland, Pietro Andreani, "A 0.2 V 0.44 μW 20 kHz Analog to Digital $\Sigma\Delta$ Modulator with 57 fJ/conversion FoM". *Proc. IEEE* 32^{nd} *European Solid-State Circuits Conference*, pp. 187-190, Switzerland, Sept. 2006.

Paper 6 Ulrik S. Wismar, Jannik H. Nielsen, Pietro Andreani, "Power Consumption Optimization in $\Sigma\Delta$ A/D Converters with Oscillator Co-Design". Under review in *Springer Analog Integrated Circuits and Signal Processing*, 11 pages.

One additional publication on unpublished measurements has been planed. The papers (except Paper 6) are reproduced with permission of their respective copyright holdes on the following pages.

Paper 1

A Low-Power CMOS Interface Chip for Data Logging Applications

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Summary. *The interface chip presented in this paper is a dedicated system designed for fish data loggers, that converts signals from 7 sensors into an 11 bit digital signal. A full-custom prototype chip was fabricated in a 0.6 μm Complementary Metal Oxide Semiconductor (CMOS) process. Designed for a 5V battery supply, the chip has a power consumption less than 1.5 mW. The chip can be used to interface a large variety of sensors such as pressure, acceleration, temperature and light sensors. In order to demonstrate the functionality, two hybrid systems containing a sensor and the interface chip was tested. A measurement with a pressure sensor showed a fine separation of different pressure levels and a linearity over a pressure range from 0 to 12 bar, and with a photo diode applied the result was a logarithmic dependency to light power.*

Keywords: Interfacing, multi sensor, ADC
Category: 9 (System architecture, electronic interfaces, wireless interfaces)

1 Introduction

Current demands on the data loggers for fisheries research have made it necessary to integrate multiple functionalities without sacrificing low power consumption, small size and portability. The original application of the present chip is to interface sensors placed on a fish to be used as a data logger, consisting of sensors, interface circuit, memory and a very simple processing unit [1]. Some important physical parameters to be gauged in this task are pressure, temperature, acceleration/tilt, light intensity and conductivity. These parameters, for instance, can supply information about swimming depth, tail movement frequency, water salinity, hunting and escape behavior of the fish. Specifically the pressure tells about swimming depth, differential pressure measurements on the tail of the fish tells about tail movements, temperature and resistivity tells about the salinity of the water, light and acceleration reveals the hunting and escape behavior. The operation range of the complete data logger is accelerations of 0 g to 2 g with a resolution of 1 mg. The temperature range should be $-2\,^{\circ}\mathrm{C}$ to $20\,^{\circ}\mathrm{C}$ with intervals of $0.05\,^{\circ}\mathrm{C}$ and the depth measurement requirement is from 0 m to 200 m in intervals of 10 cm. The requirements specify a digital resolution of 11 bit. The physical parameters on a fish are slowly changing parameters, and the highest required sample rate is 10 Hz. The data acquisition should be possible either as intensive data collection with the highest sampling rate until the memory is full, or as a rare data collection for a long period of time like one year. The data logger is a battery driven system, and the interface is therefore optimized for battery supply and low power consumption. The chip could also be used in other applications, where a general sensor interface is needed [2].

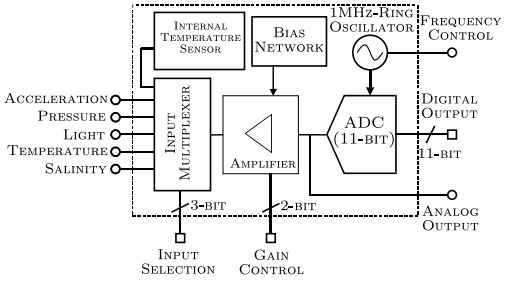

Fig. 1: Block diagram showing the contents of the interface chip. Chip border is represented with dashed line.

2 Description of the Design

The chip can process seven external sensor signals and one internal temperature sensor signal, all of which are interfaced to high-impedance inputs. A block diagram of the interface chip is seen in Figure 1. The inputs are connected to an input multiplexer, which allows one of the inputs to pass to an instrumentation amplifier according to three input selection bits giving eight combination possibilities. The multiplexer is made with eight transmission gates having a large W:L ratio. They are controlled by a tree bit decoding circuit. The first input is connected to the internal temperature sensor, and the following seven inputs are connected to external pins. In order to be able to communicate with a broad range of sensors, regardless their transduction styles and signal levels, the gain in the instrumentation amplifier can be set to 1, 10 or 100 times through two gain control bits. The instrumentation amplifier is realized using a difference amplifier with two voltage buffers on the input as shown in Figure 2. The amplification is con-

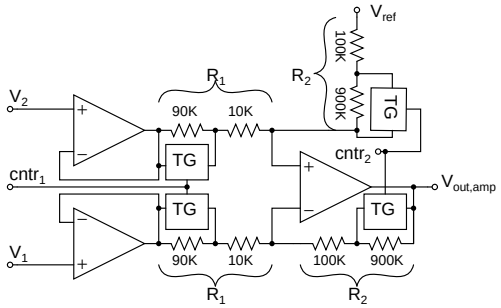

Fig. 2: Electrical diagram showing the instrumentation amplifier. The two control signals controlling the transmission gates changes the amplification.

trolled by changing the resistive feedback on the difference amplifier with transmission gates. The output voltage from the amplifier is related to an internal reference voltage of 2.50 V below the supply voltage, which normally is in the range from 4.5 V to 5.5 V. The amplified differential signal is then applied to the input of an 11-bit dual-slope integrating Analog Digital Converter (ADC) [3]. Due to the 10 Hz sampling frequency the conversion speed is not an issue, and the obvious choice was a dual-slope ADC thanks to its precision and low-power consumption. This type of converter consists of a resetable integrator connected to a comparator with a digital 11 bit counter applied to its output, as it is seen in Figure 3. The integrator starts by integrating

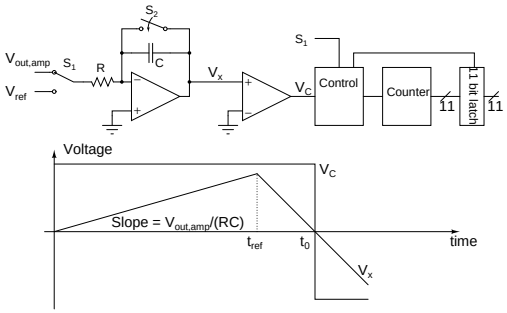

Fig. 3: Block diagram showing the dual-slope integrating converter and signal diagram for the output from the integrator V_x and the output from the comparator V_C

the input voltage for a fixed time period controlled by a 12 bit counter. In the following time period it integrates a reference voltage. While the reference voltage is integrated, the 11 bit counter is counting until the integrator voltage reaches ground level, and the comparator sends a stop signal to the counter. The value obtained is the converted result [3]. The output voltage from the integrator is given by:

$$V_x = -\int \frac{V_{out,amp}}{RC} dt$$

It is seen, that the counter result is given as $T = t_0 - t_{ref} = \frac{V_{out,amp} \cdot t_{ref}}{V_{ref}}$ (See Figure 3 for definitions). The ADC uses the same reference voltage as the amplifier, meaning that the precision of the conversion is independent of changes in the supply voltage. Since the converter is the integrating type, an oscillator is needed to control the internal counter of the ADC. In order to make the interface easy to use in a large variety of applications, an internal ring oscillator with a free-running frequency of 1 MHz is included in the chip. This type of oscillator is based on an odd number of inverters placed in a loop giving a negative feedback at all other frequencies than the oscillation frequency. Between the five inverters used in this circuit, RC delay lines are placed to lower the oscillation frequency. An external port connected to one of these delay lines allows a reduction in the oscillation frequency, thereby increasing the resolution of the ADC because of the increased integration voltage change per clock period. A disadvantage of the lower clock frequency is the reduced input voltage capability of the converter because of saturation in the integrator. The two peripheral blocks temperature sensor and reference circuit are both based on the bandgap reference circuit [4]. This circuit contains two unequally sized bipolar transistors biased with the same current. Because of their unequal size, their base emitter voltages are not the same, and the difference in base emitter voltage turns out to be linearly dependent on the temperature [5]. By making some small modifications to the resistors in the circuit, the base voltage can be made independent to supply voltage changes and temperature changes in a limited temperature range. Since the data logger is a battery operated portable system, the interface circuit has to consume low-power. Using a supply voltage of 5 V, the system is designed to consume 1.5 mW (drawing 300 μA of current) in the worst case. With this power consumption, the interface chip can fill 16 MB of data with a standard 5 mAh battery, corresponding to 16.7 hours of operation time.

In order to eliminate mismatch of the components, a common-centroid layout was designed for analog parts. Figure 4 shows a micrograph of the fabricated prototype using 0.6 μm double poly, triple metal CMOS process from Austria Micro Systems. The layout is divided into two blocks containing analog and digital circuits respectively. This is done to avoid coupling and interference of digital signals to the analog circuits. Separation of the supply voltages for the digital and the analog blocks helps to reduce the coupling of noise between these blocks. The chip die has an area of 0.7 mm^2 and the chip uses 43 bonding pads.

3 Electrical Characterization

The chip is characterized electrically without sensors to reveal the functionality and the linearity of the chip, before sensors are applied to the circuit. The reference circuit was stable at 2.500 V within the uncertainty of the measuring equipment with supply voltages rang-

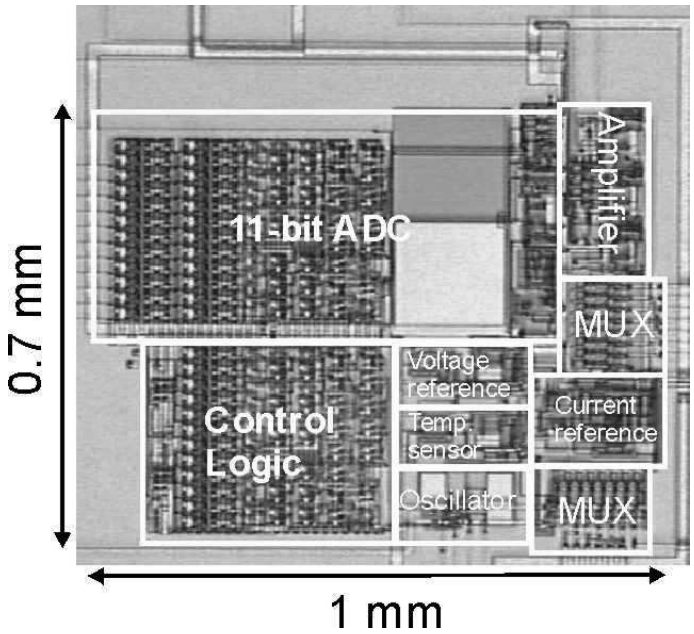

Fig. 4: Die micrograph of the fabricated prototype. Active chip area measures 1 mm×0.7 mm.

ing from 4.5 V to 5.5 V. The oscillator frequency was changeable from 200 kHz to 1.3 MHz. The instrumentation amplifier characteristic was linear, and the values for the gain was 1.0, 10.0 and 92.6. For all three gains, the input offset voltage was 4 mV. An external capacitor controls the frequency range, and it is kept low to increase the signal to noise ratio. The frequency response is seen in Figure 5. The complete characteristic of the

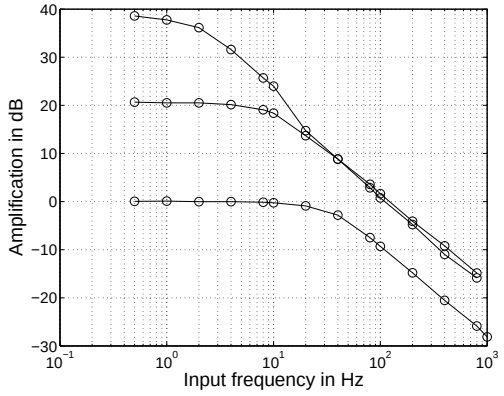

Fig. 5: Frequency response for the instrumentation amplifier at 1, 10 and 100 times of amplification.

circuit is found from measurements, where an analog voltage is applied to a sensor input, passing trough the amplifier and converted in the 11 bit converter. The digital result is plotted against the input voltage by calculating the output voltage corresponding to the digital result from:

$$V_{out} = \frac{d_{10}2^{10} + d_9 2^9 + \ldots + d_1 2 + d_0}{2^{11}} V_{ref} \quad (1)$$

where d_i (i=0,1,..,10) are the digital output bits, and V_{ref} is the reference voltage used in the integrator. The measurement results shown in Figure 6 are the output result together with the differential input voltage in the top figure, and the error result shown in the bottom figure is the difference between the measurement points and the expected ideal line where output equals input. To reveal the noise error in the conversion, four data points are made for each input voltage. The clock signal used in the conversion is a 400 kHz signal produced from the internal clock generator giving a input range of 1 V. From the results in Figure 6 it is seen, that the

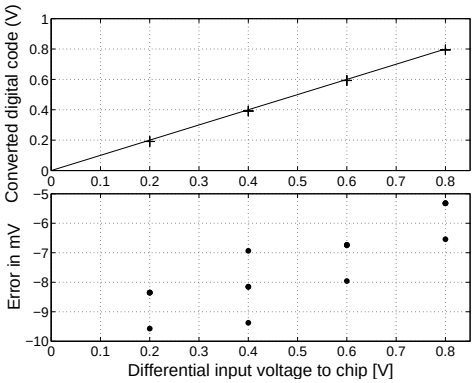

Fig. 6: ADC conversion and error results for four different input voltages. The conversions are made with an internal 400 kHz clock signal.

random noise error is maximum 2.4 mV corresponding to two bits. An error of this size could be due to noise in the chip, or it could be due to drift in the input source especially if the input voltage supplied is close to a threshold voltage. The measurement also included the output voltage from the amplifier. This measurement showed, that the offset error seen in Figure 6 originates from the offset error in the amplifier.

4 Hybrid System Measurements

In order to demonstrate that the circuit is capable of interfacing different types of sensors, the chip was interfaced to a pressure sensor and a light power sensor. The pressure sensor was a differential pressure sensor with a piezoresistive Wheatstone bridge giving an analog output voltage in the range from 0 mV to 50 mV for pressure levels from 0 bar to 12 bar. The digital output from the interface as a function of the pressure applied to the sensor is shown in Figure 7. The digital words are converted into voltages according to equation 1, where the 11 bit full scale value equals 2.500 V. The pressure applied to the sensor was measured in bar with three decimals of precision, and the digital result was found for pressures in the range from 0.5 bar to 12 bar, emulating a fish swimming at water depths from 5 m to 120 m. Taking the sensor signal level into account, an amplification of 10 and a clock frequency of 200 kHz were chosen for the best resolution. Three conversions were made at each pressure to find the maximum repetition error which was found to be 1 bit. Extrapolation over the experimental data reveals possibilities of separating pressures down to 0.05 bar in a pressure range from 0 bar to 93.4 bar.

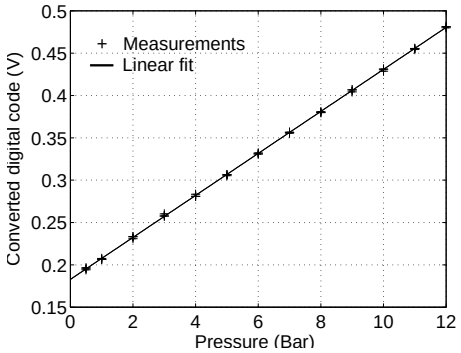

Fig. 7: Results from measurements with a pressure sensor applied to the interface chip.

The light power measurement was made with a photo diode connected to one of the differential inputs. The measurement is made in an open circuit configuration, where the diode is connected directly to the input of the interface circuit. Because of the extremely high input impedance of the interface, no current will be running from the photo diode resulting in an output voltage from the diode that has a logarithmic light power dependency. The reference light power is found from a reference photo diode connected to an amp meter measuring the photo current from the reference diode. The digital output result is calculated into a voltage according to equation 1 with a full scale value of 2.500 V. The result is seen in Figure 8.

It is seen, that the output result has a logarithmic dependency on the light power, meaning that the resolution in the light measurement is changing with the light

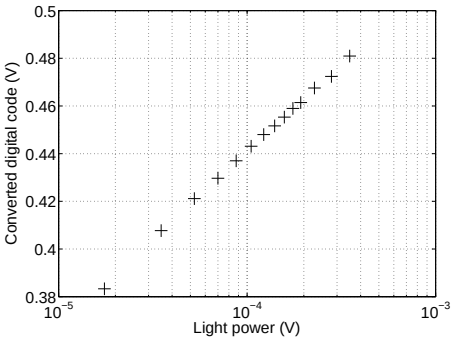

Fig. 8: Results from measurements with a photo diode applied to the interface chip.

power. This can be avoided by using the diode in a closed circuit configuration, where the photo current in the diode is supplied to a resistor, converting the current to a voltage that can be supplied to the interface. The photo current is linearly dependent on the light power, meaning that the resolution of the complete system is independent of the light power.

5 Conclusion

A low-power, battery driven, portable sensor interface circuit was successfully designed and tested. Operating with a battery supply of 5 V and consuming 1.5 mW, the chip has shown to satisfy the requirements set by the fisheries research applications. An experimental characterization of the chip was performed showing a noise error below 2 bits. The electrical characterization showed, that the chip was able to convert a differential analog input signal with a small offset error of approximately 8 mV. Measurements with a hybrid system were also made to examine the circuits capability to interface a sensor. These measurements showed an easy interfacing of a pressure sensor and a photo diode.

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Paper 2

Impact of Oscillator Power in Discrete and Continuous Time ΣΔ Converters

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Abstract

This paper presents theory and simulations of clock oscillator jitter in continuous time and discrete time modulators with single bit feedback. The theory yields the output noise power of both discrete and continuous time modulators as a function of the power consumption of a ring oscillator producing the clock signal. Simulink simulations of 3^{rd} order modulators have been included for comparison with the theoretical results, indicating that an oscillator power consumption 5 orders of magnitude higher in the continuous time case than in the discrete time case is needed, assuming a 98 dB signal to noise ratio is required.

1. Introduction

ΣΔ converters are today a commonly used topology for audio band converters, and the portable equipment requires as low power consumption as possible. Because of a lower gain bandwidth (GBW) requirement [1] in continuous time modulators this modulator type is gaining popularity, but the disadvantage is a high clock jitter sensitivity. In portable equipment the oscillator producing the clock is powered from the same battery as the modulator, and it is therefore important to include the power consumption of the oscillator when the two different modulator types are compared. The power consumption of the oscillator is seldom considered in the published literature.

This paper deals with the size of this difference in jitter sensitivity. In continuous time, the system samples internally in the modulator before the quantizer, and the jitter modulates the full scale feedback pulse [2]. In discrete time, the sampling occurs at the input of the modulator, where the jitter is modulated on the input signal which is a slowly changing signal compared to the sampling signal. If the GBW, which is controlled by the power consumption of the integrators, is too low, sampling with jitter will also introduce noise in the feedback path in the modulator. It is in this paper assumed, that the GBW is high enough to eliminate this noise. The jitter sensitivity is illustrated in figure Fig. 1 (A) and (B).

Reference circuit noise and power consumption could also be considered but it has the same effect in both the continuous time modulator and the discrete time modulator, and is not important to include in the comparison to find the optimal solution for a given converter specification.

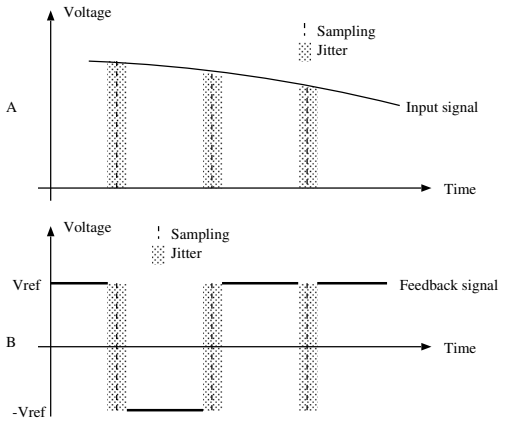

Figure 1. In discrete time (A) jitter is modulated on the input signal and in continuous time (B) jitter is modulated on the feedback signal

In this paper only the jitter noise is considered together with the quantization noise. In an real implementation other limiting noise contributions, especially from the first integrator, should be considered. In the modulators this noise is controlled by the kT/C (switched capacitor integrators) or 4kTR (active RC integrators) noise, and the power consumption of the amplifiers in the integrators.

Where power consumption is mentioned, it is the power consumption of the oscillator. The power consumption of the modulator itself is not included. The paper is meant as a tool to examine if the power consumption of the oscillator is of relevance in a specific modulator. The modulators are assumed to be single loop, and the feedback pulses are assumed to be square waves with no return to zero.

2. Oscillator model

A detailed model of the oscillator producing the clock is necessary. The most common oscillator implementation in ordinary CMOS process is the inverter ring oscilla-

tor because of the compatibility with all CMOS processes and the low area consumption because inductors are not needed. The power consumption and noise in the ring oscillator has been examined in [3], and the standard deviation of the jitter from the oscillator is given from:

$$\sigma_{\Delta T} = \kappa\sqrt{\Delta T} \tag{1}$$

Here $\sigma_{\Delta T}$ is the standard deviation of the oscillator signal after the time ΔT, where ΔT is much larger than or a multiple of the clock period. Cycle-to-cycle jitter occurs if $\Delta T = 1/f_s$, where f_s is the sample frequency.

The constant κ is found using the impulse sensitivity function for a ring oscillator. If there is perfect waveform symmetry and no extra disturbances such as substrate or supply noise, the minimum value is according to [3] given as:

$$\kappa_{min} = \sqrt{\frac{16\gamma}{3\eta}} \cdot \sqrt{\frac{kT}{P}} \tag{2}$$

Here γ and η are process and device constants; k is Boltzmann's constant, T is temperature, and P is the power consumed by the oscillator.

From (2) it is is seen that κ is proportional to $\sqrt{1/P}$ with a proportionality constant of $1.21 \cdot 10^{-10}$. The constant is found with numbers for a long channel approximation, and the method use approximated triangular waveforms. A better approximation to proportionality constant for the 0.13 μm CMOS process available to us is found through phase noise simulations on several oscillators in Cadence, giving $\kappa \approx 3.6 \cdot 10^{-11}/\sqrt{P}$. The total cycle-to-cycle jitter is therefore calculated from:

$$\sigma_{cc} = 3.6 \cdot 10^{-11}\sqrt{\frac{1}{Pf_s}} \tag{3}$$

3. Time jitter in discrete time modulator

The clock jitter is in the discrete time modulator converted into a noise voltage at the input of the modulator when the input signal is sampled, as illustrated with the simulink model in Fig. 2

In the model the modulator is placed in a subsystem triggered by the rising edges of the clock signal. Jitter is applied to the clock by delaying an ideal clock with a random number generator. The variance of the random number produced is given from the deviation in (3) squared.

If the input to the modulator is assumed to be a sinusoidal signal, the noise power originating from the jitter is given from [4]:

$$V_{jit}^2 = \sigma_{cc}^2\left(\frac{dV_{in}}{dt}\right)^2 = \sigma_{cc}^2\omega_{in}^2A^2\left(\cos\left(\omega t\right)\right)^2 \tag{4}$$

In (4) ω_{in} is the input frequency and A is the input amplitude. It is seen, that the worst case noise power is when the input frequency is high and the cosine term is unity.

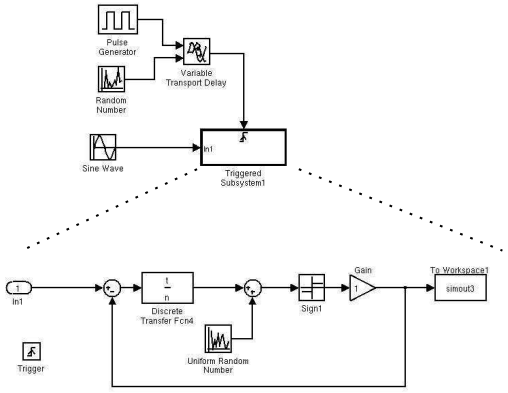

Figure 2. Simulink model of a discrete time $\Sigma\Delta$ modulator with jitter on the clock signal

The noise is assumed to be white [5], and because of folding placed in the band from 0 to $f_s/2$. The worst case noise in the conversion band from 0 to f_b is given by:

$$P_n = \left(3.6 \cdot 10^{-11}\right)^2 \frac{1}{P} A^2 \frac{\left(2\pi f_{in}\right)^2}{f_s} \frac{2f_b}{f_s} \tag{5}$$

It is seen, that the in-band noise power is inversely proportional to the power consumption of the oscillator, and proportional to the input frequency squared. To illustrate these dependencies, simulations in simulink has been carried out with the model from Fig. 2. The input amplitude dependency is illustrated in Fig. 3, and the input frequency dependency is illustrated in Fig. 4. The modulator simulated is a 3^{rd} order modulator oversampling 256 times, and the result is averaged 25 times.In both simulations the parameter is changed a factor of 10 and the result is that the noise floor moves in steps of 20 dB as expected from (5).

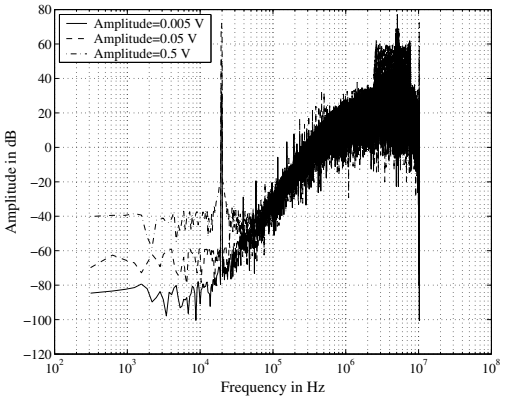

Figure 3. Simulated output spectrum from the discrete time modulator with different input signal amplitudes

From (5) it can be calculated, that to obtain a signal to noise ratio (SNR) of 16 bits with an input amplitude of 0.5 V, a conversion bandwidth of 20 kHz and an oversampling ratio (OSR) of 256 a power consumption of 16 pW is needed in the oscillator if jitter noise is considered as the dominant noise source. It is not realistic to built an oscillator with such a low power consumption, and the result is that the jitter noise is not important in this discrete time case.

Several SNRs have been simulated for a 3^{rd} order modulator. The input frequency is 19375 Hz, which is close to the maximum input frequency of 20 kHz to get the worst case jitter noise. The result is averaged 25 times, and in Fig. 5 (A) it is seen, that at high power consumptions the quantization noise reduce the SNR to around 125 dB, and at power consumptions lower than 10^{-7} W, the jitter noise starts to dominate, ending with a SNR of approximately 16 bit (98 dB) at a power consumption of 10^{-11} W.

The power dependency of jitter noise is also seen in Fig. 6 where the frequency spectrum from the output of the modulator is shown.

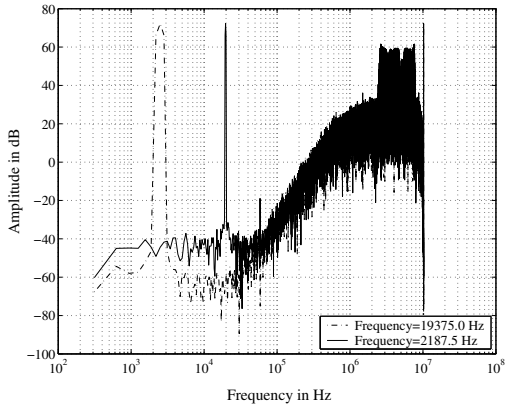

Figure 4. Simulated output spectrum from the discrete time modulator with different input signal frequencies

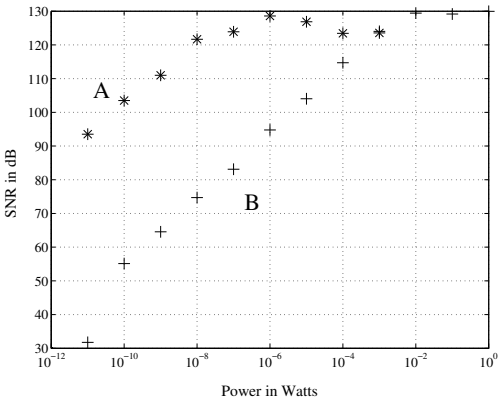

Figure 5. SNR for different power consumptions in the discrete time modulator (A) and for the continuous time modulator (B)

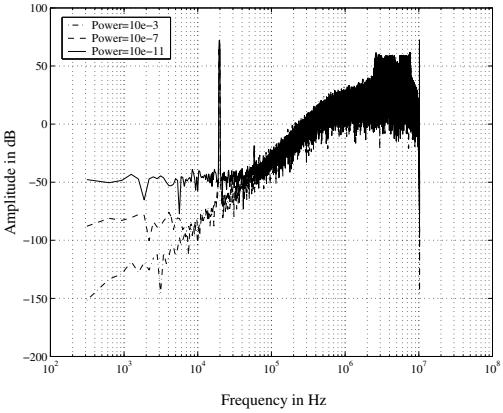

Figure 6. Output frequency spectrum from the modulator in the discrete time simulation with power consumptions of 10^{-3}, 10^{-7} and 10^{-11} W in the oscillator

4. Time jitter in continuous time modulator

In the continuous time modulator the jitter conversion into voltage noise in the middle of the modulator as illustrated in Fig. 7 [6].

In this model the subsystem is a connection passing the signal at a rising edge on the clock signal. According to analysis of Fig. 1 the noise power is given by:

$$V_{jit}^2 = (2V_{ref}\sigma_{cc}f_s)^2 \tag{6}$$

Here V_{ref} is the amplitude of the feedback pulses. It is fair to assume that this noise is white and distributed from 0 to $f_s/2$ [2]. The noise in the conversion band is therefore given by:

$$P_n = 8V_{ref}^2\left(3.6\cdot 10^{-11}\right)^2\frac{1}{P}f_b \tag{7}$$

It is seen that the noise is independent of the sampling frequency, and the dependency of the reference voltage is illustrated in Fig. 8; the reference of 10 V is not realistic, but is chosen to have a noticeable (20 dB) change in noise floor. According to (7) the 16 bit SNR with an (OSR) of 256 and a reference voltage of 1 V discussed in the previous section, requires a power consumption of 1.7 μW, or 5 orders of magnitude more than in the discrete case.

Also simulations with the model from Fig. 7 supports this result. The result from the simulation is shown in Fig. 5 (B), and it is seen, that 1 μW gives approximately 95 dB as expected, and the jitter noise starts to dominate around 1 mW. This is also seen in Fig. 9, where the noise

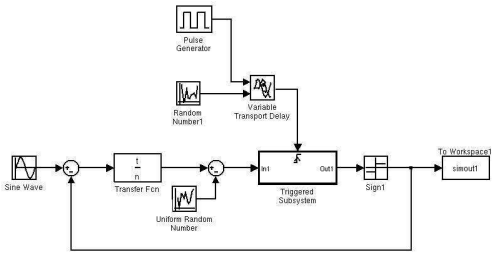

Figure 7. Simulink model of a continuous time $\Sigma\Delta$ modulator with jitter on the clock signal

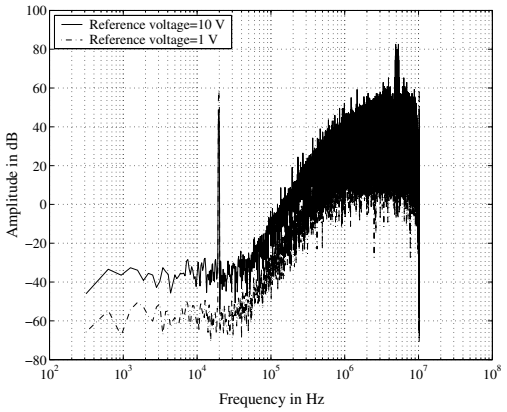

Figure 8. Simulated output spectrum from the continuous time modulator with different internal reference voltages

floor in the output frequency spectrum of the modulator is seen to decrease with power according to (7).

5. Conclusion

Theoretical equations based on oscillator power consumption giving the noise power originating from clock jitter in discrete time $\Sigma\Delta$ modulators and in continuous time $\Sigma\Delta$ modulators were presented. The models were based on power consumption in ring oscillators, and simulation models with clock jitter implemented were made. The models can be used to predict the jitter sensitivity in a given implementation.

In the 3^{rd} order example with 98 dB SNR given in the paper, the power consumption in the oscillator was 5 orders of magnitude higher in the continuous time simulation than in the discrete time case, but it is important to notice that the result in the discrete time case was a theoretical value of 16 pW. This is not a value that can be implemented, and in a practical situation it means, that the the power gained will possibly be much less than 5 orders of magnitude.

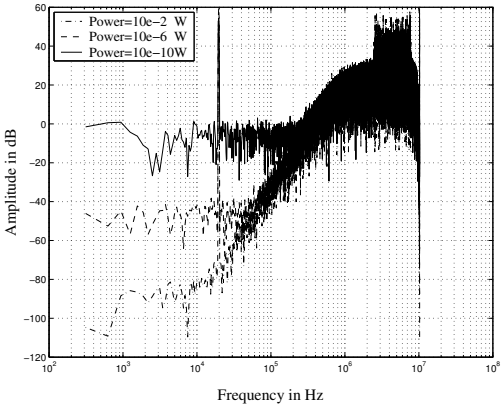

Figure 9. Output frequency spectrum from the modulator in the above simulation with power consumptions of 10^{-3}, 10^{-7} and 10^{-11} W in the oscillator

According to the analysis, jitter sensitivity in the continuous time modulator is extreme, compared to the discrete time case, while the impact of jitter can be completely disregarded in discrete time modulators. However, a reasonably low oscillator power consumption can still fulfill a wide specification range for continuous time modulators.

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Paper 3

Linearity of Bulk-Controlled Inverter Ring VCO in Weak and Strong Inversion

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Abstract

Frequency modulation in ring VCOs is investigated. Primarily, the linearity of conversion from input voltage to output frequency is considered. Bulk-voltage control of the threshold voltage of the VCO transistors is found to be a very promising approach for applications in frequency $\Delta\Sigma$ converters. Different approaches apply in presence of high supply voltages, when transistors work in strong inversion, compared to low supply voltages, when transistors are in weak inversion. In strong inversion, second-order effects controlled by the supply voltage linearize the VCO modulation, while in weak inversion an improved linearity can be obtained using soft rails, at the expense of a reduced sensitivity.

1. Introduction

A frequency $\Delta\Sigma$ converter (FDSM) is a $\Delta\Sigma$ converter without feedback [1]. The feedback in a $\Delta\Sigma$ converter can be eliminated by building a system consisting of an integrator and a differentiator. The signal is integrated, after which it is sampled and differentiated. Assuming that the output of the sampling consists of the input signal and some added quantization noise, it can be seen that the signal is passing unchanged through the converter, while the quantization noise is differentiated or high-pass filtered. The output phase of a VCO is the input voltage integrated, and thus a complete FDSM is obtained by sampling the phase and differentiating the result, as illustrated in Fig. 1.

If the VCO is nonlinear, it will introduce a harmonic distortion to the signal, and the signal to noise and distortion ratio will possibly be limited by the nonlinearity. We believe that an attractive VCO architecture for use in a FDSM is a voltage-controlled inverter-ring oscillator (RVCO), due to the two following reasons: the possibility of a rather high linearity when frequency tuning is performed from the bulk terminal of the MOS transistors

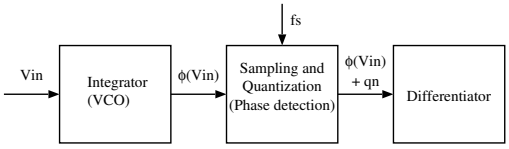

Figure 1. Block diagram of FDSM. The integrator is implemented as a VCO

(as shown later), and the low supply voltage and power consumption capabilities of this VCO type [2].

According to the literature on RVCOs, the primary consideration is often wide tuning range and low phase noise [3] [4], and current starvation is commonly used to control the oscillation frequency. These topics are of secondary importance to the FDSM, and they will not be treated in this paper. Controlling the frequency with the bulk voltage has some similarities to the current-starvation principle, but it has linearity advantages at the expense of a smaller tuning range, compared to current starvation. This is discussed in section 2.

The linearity of the bulk-controlled RVCO is discussed when transistors are operating in strong inversion and weak inversion, respectively. In both cases, the validity of the approaches is supported by spectreRF simulations.

2. Voltage to frequency relations in the RVCO

The RVCO consists of an odd number (N) of inverters connected in a ring. In each of the inverters the signal will be delayed by the time t_d, thus the output frequency of the oscillator is given from:

$$f = \frac{1}{2Nt_d}. \tag{1}$$

Each node in the inverter chain is loaded by a capacitance C_L consisting of the total gate capacitance from two transistors, the total drain capacitance from two transistors, routing capacitance, and a possible additional capacitance or varactor. The delay in the inverter exists due to the time it takes the transistors in the inverter to charge C_L. If N is large enough, all nodes will be completely charged and discharged during one period, and each inverter delivers the charge $C_L V_{dd}$. The transistor charging the capacitance will initially charge it with a maximum current I_D. The current decreases during the transition, and if ηI_D is the mean current (disregarding leak currents), the frequency of the RVCO is given by

$$f = \eta \frac{I_D}{2NC_L V_{dd}} \tag{2}$$

N and η are fixed parameters for a given RVCO, but from (2) it is clear that f can be controlled through C_L, V_{dd} and I_D.

C_L can be controlled by a varactor, such as a biased pn junction. This is simple and effective, but also highly nonlinear [5]. A linear conversion can be obtained by switching on and off fixed capacitors, according to the magnitude of the input voltage. However, this requires large capacitor arrays at each node, and, more importantly, an A/D converter to control the switches, making it unsuitable in an A/D converter design.

Controlling V_{dd} will also influence I_D, as it is seen in the following sections. This principle has been shown to produce a reasonably good linearity. However, it requires high input voltages and the input signal is loaded with pulses and a generally low impedance. This solution is not suitable in a low supply voltage and low power circuit.

I_D can be controlled through different current starving techniques. This approach results in a wide tuning range, but is also very nonlinear. Controlling I_D with the threshold voltage of the transistors through the bulk voltage yields a better linearity. Furthermore, this solution implies a high and stable input impedance, and if V_{dd} is lower than one diode voltage, it is possible to have rail to rail inputs, or even input voltages exceeding the supply voltage.

3. Bulk-controlled RVCO in strong inversion

The behavior of the RVCO depends on the operation region of the transistors. It can be assumed that all nodes are completely charged or discharged during an oscillation period. This means that the drain-source voltage across the transistor that is about to be turned on is V_{dd}, while the gate-source voltage will be lower than the drain-source voltage. Assuming that the supply voltage is high, the transistor will saturate when the gate-source voltage passes the threshold voltage (V_{th}). To a crude approximation the saturation drain current is given by

$$I = \frac{W}{2L}\mu_{eff}C_{ox}(V_{gs} - V_{th})^2 \qquad (3)$$

where W and L are transistor dimensions, μ_{eff} is the effective carrier mobility, and C_{ox} is the oxide capacitance. The maximum current used in (2) is obtained from (3) when the gate-source voltage equals V_{dd}. It is seen that V_{th} is in the equation for the drain current thus a model of the bulk dependency of V_{th} is needed. When the bulk source voltage V_{BS} is increased, the depletion area and thus the space charge is reduced. Due to charge neutrality through the MOS structure, the threshold voltage will be reduced according to:

$$V_{th} = V_{t0} + \gamma(\sqrt{2\Phi_f - V_{BS}} - \sqrt{2\Phi_f}) - K_B V_{BS} \quad (4)$$

where V_{t0} is V_{th} when $V_{BS} = 0$, γ is a process constant and Φ_f is the surface potential of the MOS transistor. The last term is a secondary short-channel effect. It is seen from the equations that if V_{BS} is increased, V_{th} is reduced. This results in an increased current in the transistor and thus an increased oscillation frequency. Now (3) is rewritten as:

$$I_D = \frac{W}{2L}\mu_{eff}C_{ox}(V_{dd}^2 + V_{th}^2 - 2V_{dd}V_{th}). \qquad (5)$$

To operate in strong inversion, $V_{dd} > V_{th}$ is required, and the term with linear dependency to V_{th} will dominate. If the constant part of (4) is replaced with $K_\Phi = V_{t0} - \gamma\sqrt{2\Phi_f}$ and the bulk-voltage dependent part is replaced with $y = \gamma\sqrt{2\Phi_f - V_{BS}}$, a first-order approximation of the current can be written as

$$\begin{aligned} I_D = \; & \tfrac{W}{2L}\mu_{eff}C_{ox}(V_{dd}^2 + K_\Phi^2 - 2V_{dd}K_\Phi \\ & +\gamma^2 y^2 - 2\gamma(V_{dd} - K_\Phi)y). \end{aligned} \qquad (6)$$

When V_{dd} is high, the linear dependency on y is dominating, and the current will grow with a power to V_{BS} larger than one. When V_{dd} is reduced, the linear second-order effect in (4) becomes more important, making the dependency more linear.

In a real RVCO the load capacitance as well as μ_{eff} [7] will also be dependent on the bulk voltage. Reducing V_{dd}, and thus the primary effects, increases the influence of the secondary effects. These, in turn, reduce the oscillation frequency when V_{BS} is increased, and will increase the linearity in a limited V_{BS} range for low supply voltages in the strong inversion region. This is illustrated by the spectreRF simulation of a 5-stage RVCO implemented in a 0.13 μm CMOS process. In Fig. 2 the increased influence of second-order effects at low supply voltages is illustrated by the sensitivity K_s of the output frequency f versus the tuning voltage V_{BS} (i.e., $K_s = \partial f/\partial V_{BS}$), for supply voltages of 1.2 V and 600 mV. Both plots are normalized the value of the sensitivity for V_{BS}=0.6 V. It should be added that only the bulk voltage of the n-mos transistors is controlled. Both n-mos and p-mos bulk could be controlled, but it would require two different voltage levels dependent on each other, which is difficult to accomplish.

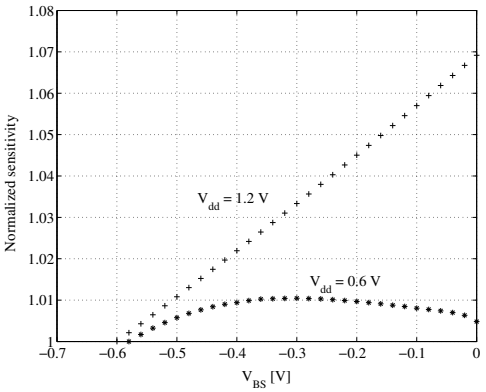

Figure 2. Sensitivity of 5 stage RVCO normalized to their minimum value with supply voltages of 1.2 V and 0.6 V

The plot of the oscillation frequency versus the tuning voltage V_{BS}, for $V_{dd} = 600$ mV, is shown in Fig. 3, with the corresponding sensitivity (without normalization) in Fig. 4.

A measure of the nonlinearity of the transfer function of the VCO is given by

$$NL = \frac{\Delta K_s}{2K_{s-mean}}100\% \qquad (7)$$

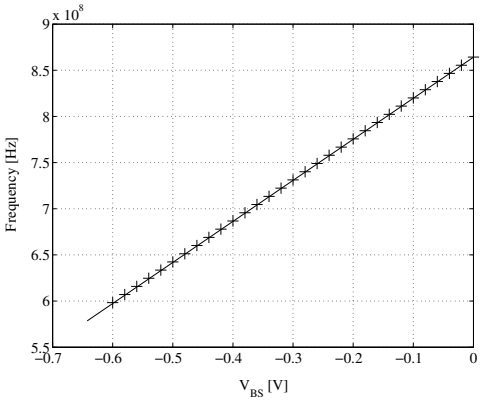

Figure 3. RVCO transfer function for a 5 stage RVCO simulated in Cadence

(see Fig. 4). The nonlinearity is 0.5% over an input range of 0.6 V with a supply of 600 mV. However, if the supply voltage is higher, the nonlinearity increases, and e.g. at V_{dd}=0.9 V the nonlinearity is 6.0% and the sensitivity curve is monotonically increasing.

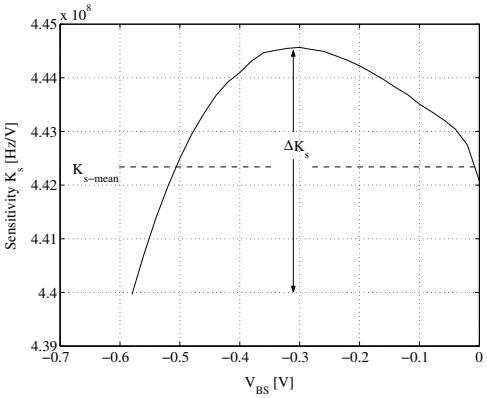

Figure 4. Sensitivity of the RVCO illustrates a nonlinearity of 0.5%

4. Bulk-controlled RVCO in weak inversion

In many applications low supply voltages are desired. In these applications the RVCO is advantageous, and it has been reported to function down to 80 mV [2]. When V_{dd} decreases below V_{th} the channel in the transistors can no longer exist, and they are working in the weak inversion region. This means that the current expression is not given by (3), but depends exponentially on V_{gs} as in a bipolar transistor. V_{th} influences the drain current according to [6]

$$I = I_0 e^{(V_{gs}-V_{th})/nV_T}\left(1 - e^{-\delta\frac{V_{DS}}{V_T}}\right) \qquad (8)$$

where I_0 is a proportionality constant, V_T is the thermal voltage, δ and n are fitting parameters, and V_{DS} is the drain-source voltage. The maximum current is found, as a function of V_{th}, when $V_{gs} = V_{dd}$. The last term in (8) can be a part of I_0.

The threshold voltage V_{th} is, according to the approximation given by (4), independent of the operation region of the transistor. This means that the maximum current, and thus the frequency in weak inversion, is proportional to

$$I_D \propto e^{-\gamma\sqrt{2\phi_f - V_{BS}}/nV_T}. \qquad (9)$$

This implies that I_D is a function of V_{BS} to a power higher than one, and the sensitivity of the RVCO will be increasing with V_{BS}. To obtain linearity, this effect should be compensated. When V_{gs} is replaced with V_{dd}, it is seen from (8) that a reduction of V_{dd} will decrease I_D, and this effect can be used as a feedback mechanism on I_D. The feedback can be obtained with so-called soft rails by providing the supply voltage in the inverters through a biased transistor, as shown in Fig. 5.

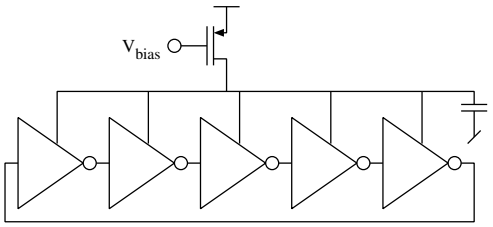

Figure 5. RVCO with soft rails

When V_{BS} is increased, V_{th} is reduced, and the average current in the bias transistor ηI_D is increased. This will cause an increased drain-source voltage across the bias transistor, and the negative feedback is obtained. The bias transistor will also be operating in weak inversion with a constant V_{gs} and V_{th}. According to (8) the drain source voltage of the bias transistor is given from the average current I_{D-B} as

$$V_{DS-B} = -\frac{V_T}{\delta} ln\left(1 - \frac{I_{D-B}}{I_{0-B}}\right) \qquad (10)$$

where $I_{0-B} = I_0 e^{(V_{bias}-V_{th})/nV_T}$. The length of the bias transistor changes the curvature of the (I,V) characteristic. To maximize the linear tuning range, it should be short. However, if it becomes too short it will not be able to provide sufficient feedback. Cadence simulations of two (I,V) characteristics for bias transistors with different lengths can be seen in Fig. 6.

The width of the bias transistor and the gate bias voltage V_{bias} adjust the work point to a portion of the (I,V) characteristic where the curvature provides the desired feedback. The principle is illustrated with a Cadence simulation of the frequency and sensitivity in Fig. 7 and Fig. 8. The same process as in the strong inversion simulation is used, and the supply voltage is 200 mV. It is seen that the nonlinearity is improved from 27% to 2.4% when soft rails are used, at the expense of a lower sensitivity. It should be mentioned that simulations in weak inversion are often not very reliable, and good performances for the circuit just described are likely to be obtained only after some prototyping.

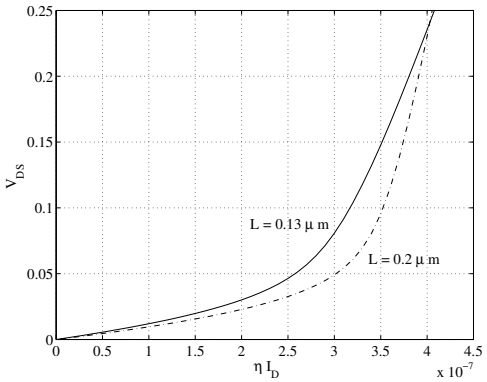

Figure 6. Cadence simulation of (I,V) characteristic of two bias transistors with lengths of 0.13 μm and 0.2 μm

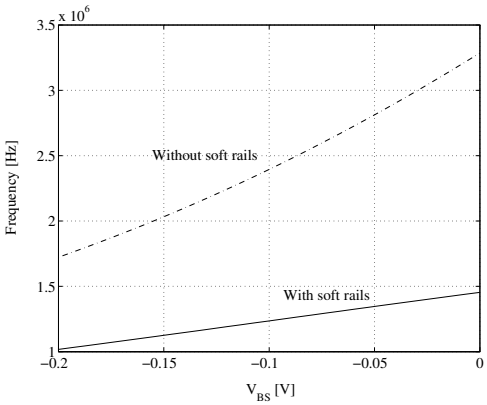

Figure 7. RVCO output frequency in weak inversion supplied with 0.2 V with and without soft rails

5. Conclusion

Modulation linearity was discussed for inverter-ring voltage-controlled oscillators (RVCOs). This type of VCO was found to be a good realization for the integrator in an FDSM, where linearity in the conversion between input voltage and output frequency is important.

The RVCO was studied in two situations: when the supply voltage is high enough to bring the transistors in strong inversion, and when the supply voltage is low, forcing the transistors in weak inversion.

In strong inversion the influence from second-order effects was seen to be controlled by the supply voltage, where a lowering of the supply voltage increased the influence of these effects. Through simulations it was shown that, when the optimal supply voltage (0.6 V in this simulation) was found, the nonlinearity could be reduced to 0.5% for a full scale input signal.

In weak inversion it was seen that the modulation is generally nonlinear. The linearity was shown to be greatly improved by using soft rails for the supply voltage to the RVCO inverters. Through simulations on a RVCO supplied with 0.2 V this principle was shown to improve the nonlinearity from 27% to 2.4% for a full scale input.

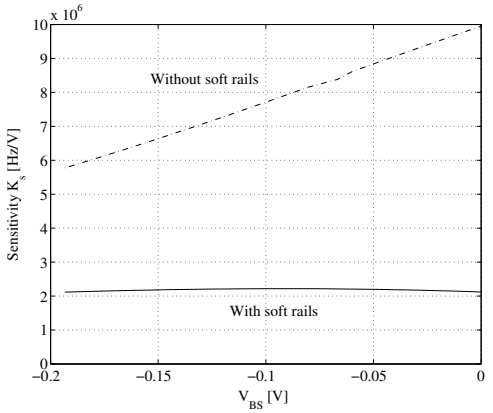

Figure 8. Sensitivity of the RVCO in weak inversion supplied with 0.2 V with and without soft rails

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Paper 4

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Linearity of bulk-controlled inverter ring VCO in weak and strong inversion

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Abstract In this paper linearity of frequency modulation in voltage controlled inverter ring oscillators for non feedback sigma delta converter applications is studied. The linearity is studied through theoretical models of the oscillator operating at supply voltages above and below the threshold voltage of a transistor, bringing the transistors in respectively strong and weak inversion. The theoretical results are tested with more advanced models through spectreRF simulations. A soft rail approach implemented to improve linearity in weak inversion is proposed and demonstrated. The influence from voltage noise, process variations and temperature variations have also been simulated to indicate the advantages of having the soft rail bias transistor in the VCO.

Keywords Inverter ring · Linear modulation · Weak inversion · VCO · FDSM

1 Introduction

The supply voltage and power consumption of A/D converters have been decreasing due to demands from technology scaling and battery driven applications. Directly reducing the supply voltage reduces also the power consumption, but introduces a number of disadvantages. Two disadvantage that active analog circuits are influenced by, are the reduced overdrive voltage, even though the threshold voltage of a transistor scales somewhat with the technology, and the increased requirements to the noise in the circuits. Usually an internal voltage signal scales with the supply voltage. To keep the same signal to noise ratio the noise is reduced by increasing the bias current and the power consumption is thus not scaled.

Another approach is to have an internal signal which is not scaled with the supply voltage. By keeping a constant signal swing when the supply voltage is reduced, the power is scaled at the same time. Different signal carriers have been used such as charge signals in switched capacitors, current signals in current mode circuits, and frequency signals in FM circuits. A frequency $\Delta\Sigma$ converter (FDSM) is a $\Delta\Sigma$ converter with a frequency intermediate signal carrier and therefore it opens possibility of both low supply voltages and low power consumptions.

The FDSM is a $\Delta\Sigma$ converter without feedback [1]. The feedback in a $\Delta\Sigma$ converter can be eliminated by building a system consisting of an integrator and a differentiator. The signal is integrated, after which it is sampled and differentiated. Assuming that the output of the sampling consists of the input signal and some added quantization noise, it can be seen that the signal is passing unchanged through the converter, while the quantization noise is differentiated or high-pass filtered. The output frequency and phase of a VCO is given from:

$$f_{out}(t) = f_c + K_s V_{in}(t) \tag{1}$$

$$\theta(t) = 2\pi \int_{-\infty}^{t} (f_c + K_s V_{in}(\tau)) d\tau \tag{2}$$

where f_c is the oscillator carrier frequency, K_s is the sensitivity of the modulation and $V_{in}(t)$ is the input voltage. It is

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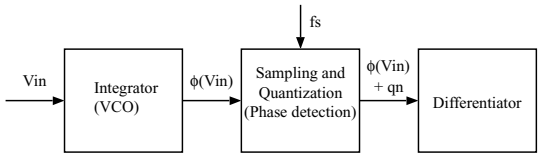

Fig. 1 Block diagram of FDSM. The integrator is implemented as a VCO

seen, that the integration of the input signal and conversion from voltage signal carrier to frequency signal carrier is directly obtained in the VCO using the phase output, and thus a complete FDSM is obtained by sampling the phase and differentiating the result, as illustrated in Fig. 1.

The differentiation is a digital differentiation which in a single bit solution is simple to carry out with two flipflops and a XOR gate. More complicated differentiations using parallelization and multibit logic can be used to improve the performance of the modulator.

According to the literature on RVCOs, the primary consideration is often wide tuning range and low phase noise [2, 3]. From (2) it is seen that the carrier frequency f_c introduces only a DC value and the absolute value of the sensitivity K_s is a gain, neither of them is limiting factors for the signal to noise and distortion ratio (SNDR). But if the VCO is nonlinear, having a sensitivity K_s which is signal dependent, it will introduce harmonic distortion to the signal, and the SNDR will possibly be limited by the nonlinearity. The linearity is thus treated as the primary topic when dealing with the VCOs in this paper. Regarding carrier frequency, the FDSM can operate with both over and under sampling of the RVCO frequency, meaning that there is no upper or lower limit on f_c. There are however some frequency ranges which are not allowed when the RVCO is under sampled, and the result is, that the most robust FDSM is obtained, when f_c is low enough to allow oversampling. On the other hand when f_c is reduced, K_s usually scales together with it. With fixed linearity, a reduced K_s will decrease SNDR, and thus the optimal f_c is the highest frequency still allowing oversampling for the given supply voltage.

A good VCO for the FDSM implementation is found to be a bulk voltage-controlled inverter-ring oscillator (RVCO) through a discussion in this paper. The theoretical equations for linearity of the RVCO is derived for transistors operating in strong inversion and weak inversion, respectively. In both cases the validity of the approaches is supported by spectreRF simulations with the BSIM3v3 parameters for a 0.13 μm CMOS process. To improve the linearity when operating with the transistors in weak inversion, an approach improving the linearity of the VCO by using soft supply rails is proposed.

The application for the FDSM is as low-pass $\Delta\Sigma$ modulator. The fact that the modulator discussed is first order and thus does requires a high oversampling ratio, together with the fact the the input should be kept somewhat lower than the carrier frequency, makes it very suitable in low frequency applications such as very low power audio applications.

2 The optimal VCO type in FDSM

Different types of VCOs can be considered for the FDSM. Basically the VCO is an oscillator where an element capable of changing the oscillation frequency is added. The oscillators can be separated in two different types: tuned oscillators with sinusoidal output and oscillators with square output. The tuned oscillators are based on a positive feedback around a tuning block such as a crystal or a LC tank. They can provide a very low phase noise, and a low harmonic distortion. They are however very bulky, complicated and expensive in terms of chip area due to the size of inductors, and might require external components. This is especially true when low carrier frequencies are desired.

Because the phase detection in the FDSM is single bit, it just detects whether when the sign on the phase is positive or negative, and thus the system is not disturbed by harmonics, opening possibility of using the square output oscillators. In this category the inverter-ring oscillator is the most simple type and it is easily implemented in a standard CMOS process.

The digital parts of the FDSM is capable of operation at supply voltages much lower than the threshold voltage of a transistor [4] and the VCO will be the block limiting the supply voltage. The ring oscillator consists of inverter gates and thus by using this type of oscillator the complete FDSM is capable of operation at extremely low supply voltages.

The RVCO consists of an odd number (N) of inverters connected in a ring. Assuming balanced inverters with equally powerful n and p-MOS transistors, the signal will be delayed by the time t_d in each inverter, and the output frequency of the oscillator is given from:

$$f = \frac{1}{2Nt_d}. \tag{3}$$

Each node in the inverter chain is loaded by a capacitance C_L consisting of the total gate capacitance from two transistors, the total drain capacitance from two transistors, routing capacitance, and a possible additional capacitance or varactor. The delay in the inverter exists due to the time it takes the transistors in the inverter to charge C_L. If N is large enough, all nodes will be completely charged and discharged during one period, and each inverter delivers the charge $C_L V_{dd}$.

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The transistor charging the capacitance will initially charge it with a maximum current I_D. The current decreases during the transition, and if ηI_D is the mean current (disregarding leak currents), the frequency of the RVCO is given by

$$f = \eta \frac{I_D}{2NC_L V_{dd}} \tag{4}$$

N and η are fixed parameters for a given RVCO, but from (4) it is clear that f can be controlled through C_L, V_{dd} and I_D.

If the inverters are not balanced, the n and p-MOS transistors will not charge C_L with the same maximum current I_D resulting in a RVCO frequency of:

$$f = \eta \left(\frac{I_{Dp}}{NC_L V_{dd}} + \frac{I_{Dn}}{NC_L V_{dd}} \right). \tag{5}$$

The unbalanced inverters will result in unequal rise and fall times at the output nodes of the RVCO. If rise and fall times are significantly different, this will according to [6] result in increased phase noise. This is however the only performance degradation related to unequal rise and fall times in the FDSM, as long as both times are small enough not to provoke metastability in the flipflops in the digital differentiation.

C_L can be controlled by a varactor, such as a biased pn junction. This is simple and effective, but also highly nonlinear [7]. A linear conversion can be obtained by switching on and off fixed capacitors, according to the magnitude of the input voltage. However, this requires large capacitor arrays at each node, and, more importantly, an A/D converter to control the switches, making it unsuitable in an A/D converter design.

Controlling V_{dd} will also influence I_D, as it is seen in the following sections. This principle has been shown to provide a reasonably good linearity for bipolar oscillators [5] which behaves much like MOS circuits in weak inversion. However, it requires high input voltages and the input signal is loaded with pulses and a generally low impedance. This solution is not suitable in a low supply voltage and low power circuit.

I_D can be controlled through different current starving techniques often implemented with a tail transistor on the inverters reducing the charging current. This approach results in a wide tuning range, but is also highly nonlinear when controlling the tail transistor with a voltage input. Another principle of controlling I_D which have some similarities to the current starving technique is to modulate the threshold voltage of the transistors through the bulk voltage. This principle yields a better linearity than the basic current starving technique. Furthermore, this solution implies a high and stable input impedance, and if V_{dd} is lower than one diode voltage, it is possible to have rail to rail inputs, or even input voltages exceeding the supply voltage. This solution has been shown to have very low supply voltage and low power consumption capabilities [8]. And the result is that bulk voltage-controlled RVCO is an advantageous VCO in the FDSM.

Different types of inverters can be incorporated in the oscillator core. The following derivations are made for simple standard CMOS inverters. This type of inverter is selected because of its simplicity which eases the modeling, and because this inverter includes the minimum number of stacked devices, which is an advantage in low supply voltage circuits. The 0.13 μm process used for simulations is a p-subtrate process which includes isolated p-wells and thus both n and p-MOS transistors are placed in isolated wells. The inputs controlling the RVCO are therefore connected directly in the wells of n and p-MOS transistors. This will not cause problems, as long as the pn junction between the well and the global substrate is not forward biased, which will not happen, if the input voltage is concealed within the supply voltages.

3 Bulk-controlled RVCO in strong inversion

The behavior of the RVCO depends on the operation region of the transistors. It can be assumed that all nodes are completely charged or discharged during an oscillation period. This means that the drain-source voltage across the transistor that is about to be turned on is V_{dd}, while the gate-source voltage will be lower than the drain-source voltage. Assuming that the supply voltage is high, the transistor will saturate when the gate-source voltage passes the threshold voltage (V_{th}). To a crude approximation the saturation drain current is given by

$$I = \frac{W}{2L} \mu_{eff} C_{ox} (V_{gs} - V_{th})^2 \tag{6}$$

where W and L are transistor dimensions, μ_{eff} is the effective carrier mobility, and C_{ox} is the oxide capacitance. The maximum current used in (4) is obtained from (6) when the gate-source voltage equals V_{dd}. It is seen that V_{th} is in the equation for the drain current thus a model of the bulk dependency of V_{th} is needed. When the bulk source voltage V_{BS} is increased, the depletion area and thus the space charge is reduced. Due to charge neutrality through the MOS structure, the threshold voltage will be reduced according to [9]:

$$V_{th} = V_{t0} + \gamma(\sqrt{2\Phi_f - V_{BS}} - \sqrt{2\Phi_f}) + K_B V_{BS} \tag{7}$$

where V_{t0} is V_{th} when $V_{BS} = 0$, γ is a process constant and Φ_f is the surface potential of the MOS transistor. The last term is a secondary short-channel effect. It is seen from the equations that if V_{BS} is increased, V_{th} is reduced. This results

in an increased current in the transistor and thus an increased oscillation frequency. Now (6) is rewritten as:

$$I_D = \frac{W}{2L}\mu_{eff}C_{ox}\left(V_{dd}^2 + V_{th}^2 - 2V_{dd}V_{th}\right). \tag{8}$$

To operate in strong inversion, $V_{dd} > V_{th}$ is required, and the term with linear dependency to V_{th} will dominate. If the constant part of (7) is replaced with $K_\Phi = V_{t0} - \gamma\sqrt{2\Phi_f}$ and the bulk-voltage dependent part is replaced with $y = \sqrt{2\Phi_f - V_{BS}}$, a first-order approximation of the current can be written as:

$$I_D = \frac{W}{2L}\mu_{eff}C_{ox}\left(V_{dd}^2 + K_\Phi^2 - 2V_{dd}K_\Phi + \gamma^2 y^2 - 2\gamma(V_{dd} - K_\Phi)y\right). \tag{9}$$

When V_{dd} is high, the linear dependency on y is dominating, and the current will grow with a power to V_{BS} larger than one. When V_{dd} is reduced, the linear second-order effect in (7) becomes more important, making the dependency more linear.

In a real RVCO the load capacitance as well as μ_{eff} [11] will also be dependent on the bulk voltage. Reducing V_{dd}, and thus the primary effects, increases the influence of the secondary effects. These, in turn, reduce the oscillation frequency when V_{BS} is increased, and will increase the linearity in a limited V_{BS} range for low supply voltages in the strong inversion region. This is illustrated by a spectreRF simulation of a 5-stage RVCO based on BSIM3v3 parameters from a 0.13 μm CMOS process.

A plot of the oscillation frequency versus the tuning voltage V_{BS}, for $V_{dd} = 600$ mV, is shown in Fig. 2.

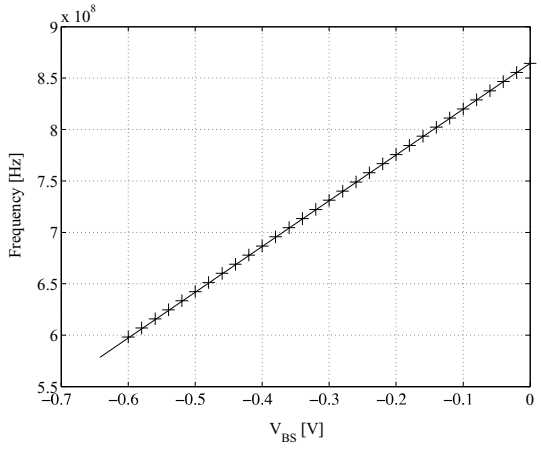

Fig. 2 RVCO transfer function for a 5 stage RVCO simulated in SpectreRF

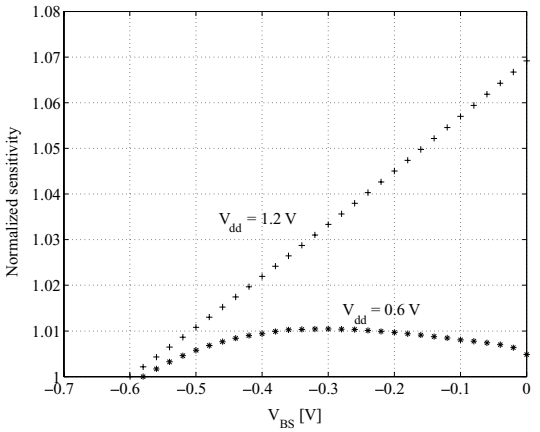

Fig. 3 Sensitivity of 5 stage RVCO normalized to their minimum value with supply voltages of 1.2 V and 0.6 V

Linearity is however difficult to detect from the frequency output, but high linearity means a constant sensitivity K_s and thus nonlinearities is easily detectable from the sensitivity. According to (1) K_s is found as the first derivative of the output frequency with respect to input voltage (i.e., $K_s = \partial f/\partial V_{BS}$). In Fig. 3 the increased influence of second-order effects at low supply voltages is illustrated by the sensitivity, for supply voltages of 1.2 V and 600 mV. Both plots are normalized to the value of the sensitivity for $V_{BS} = 0.6$ V. It should be added that only the bulk voltage of the n-MOS transistors is controlled which according to (5) reduces the sensitivity compared to the case where both transistors are controlled in (4). Both n-MOS and p-MOS bulk could be controlled, but it would require two different voltage levels dependent on each other, which is difficult to accomplish.

The sensitivity corresponding to the frequency plot in Fig. 2 is seen (without normalization) in Fig. 4. A measure of the nonlinearity of the transfer function of the VCO is given by

$$NL = \frac{\Delta K_s}{2K_{s-mean}}100\% \tag{10}$$

(see Fig. 4). The nonlinearity is 0.5% over an input range of 0.6 V with a supply of 600 mV. However, if the supply voltage is higher, the nonlinearity increases, and e.g. at $V_{dd} = 0.9$ V the nonlinearity is 6.0% over an input range of 0.6 V and the sensitivity curve is monotonically increasing.

4 Bulk-controlled RVCO in weak inversion

In many applications low supply voltages are desired. In these applications the RVCO is advantageous, and it has been

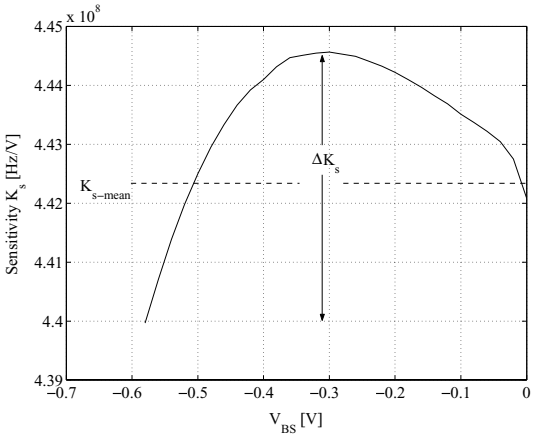

Fig. 4 Sensitivity of the RVCO illustrates a nonlinearity of 0.5%

reported to function down to 80 mV [8]. When V_{dd} decreases below V_{th} the channel in the transistors can no longer exist, and they are working in the weak inversion region. This means that the current expression is not given by (6), but depends exponentially on V_{gs} as in a bipolar transistor. V_{th} influences the drain current according to [10]

$$I = I_0 e^{(V_{gs}-V_{th})/nV_T}\left(1 - e^{-\delta\frac{V_{DS}}{V_T}}\right) \tag{11}$$

where I_0 is a proportionality constant, V_T is the thermal voltage, δ and n are fitting parameters, and V_{DS} is the drain-source voltage. The maximum current is found, as a function of V_{th}, when $V_{gs} = V_{dd}$. The last term in (11) can be included in I_0.

The threshold voltage V_{th} is, according to the approximation given by (7), independent of the operation region of the transistor. This means that the maximum current, and thus the frequency in weak inversion, is proportional to

$$I_D \propto e^{-\gamma\sqrt{2\phi_f - V_{BS}}/nV_T}. \tag{12}$$

This implies that I_D is a function of V_{BS} to a power higher than one, and the sensitivity of the RVCO will be increasing with V_{BS}. To obtain linearity, this effect should be compensated. When V_{gs} is replaced with V_{dd}, it is seen from (11) that a reduction of V_{dd} will decrease I_D, and this effect can be used as a feedback mechanism on I_D. The feedback can be obtained with so-called soft rails by providing the supply voltage in the inverters through a biased transistor, as shown in Fig. 5.

When V_{BS} is increased, V_{th} is reduced, and the average current in the bias transistor ηI_D is increased. This will cause an increased drain-source voltage across the bias transistor, and the negative feedback is obtained. The bias transistor

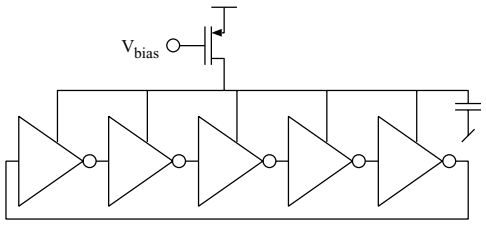

Fig. 5 RVCO with soft rails

will also be operating in weak inversion with a constant V_{gs} and V_{th}. According to (11) the drain source voltage of the bias transistor is given from the average current I_{D-B} as

$$V_{DS-B} = -\frac{V_T}{\delta} ln\left(1 - \frac{I_{D-B}}{I_{0-B}}\right) \tag{13}$$

where $I_{0-B} = I_0 e^{(V_{bias}-V_{th})/nV_T}$. The length of the bias transistor changes the curvature of the (I,V) characteristic. To maximize the linear tuning range, it should be short. However, if it becomes too short it will not be able to provide sufficient feedback. SpectreRF simulations with BSIM3v3 parameters from the 0.13 μm process of two (I,V) characteristics for bias transistors with different lengths can be seen in Fig. 6.

The width of the bias transistor and the gate bias voltage V_{bias} adjust the work point to a portion of the (I,V) characteristic where the curvature provides the desired feedback. The principle is illustrated with a SpectreRF simulation of the frequency and sensitivity in Figs. 7 and 8. The same process as in the strong inversion simulation is used, and the supply voltage is 200 mV. It is seen that the nonlinearity is improved from 27 to 2.4% when soft rails are used, at the expense of

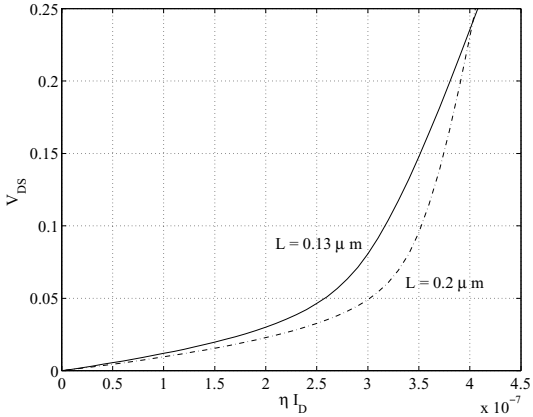

Fig. 6 SpectreRF simulation of (I,V) characteristic of two bias transistors with lengths of 0.13 μm and 0.2 μm

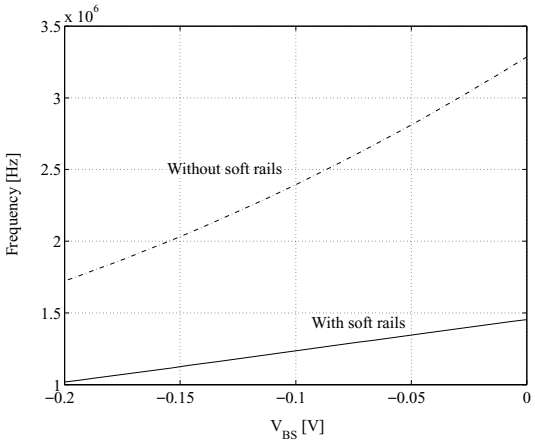

Fig. 7 RVCO output frequency in weak inversion supplied with 0.2 V with and without soft rails

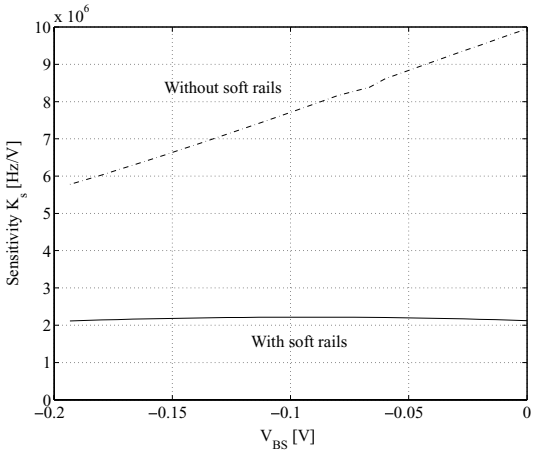

Fig. 8 Sensitivity of the RVCO in weak inversion supplied with 0.2 V with and without soft rails

a lower sensitivity. It should be mentioned that simulations in weak inversion are often not very reliable. This should not affect the principle, but good performances for the circuit just described are likely to be obtained only after some prototyping.

5 Fabrication and noise immunity considerations

The above derivations are made from crude approximations, where as in the simulations much more advanced BSIM3v3 models are implemented and this result should be closer to the measurement on a real chip. To know the worst case result in a fabricated circuit, it is however important to consider process variations, noise rejection and stability to temperature variations. The main focus will be on improvements or deteriorations when the soft rail biasing is implemented.

Impact from process variations, is studied through corner and Monte Carlo simulations. In corner simulations the worst case situations is simulated and the slow/fast and fast/slow transistor corners are compared to the typical situation.

In a ring oscillator the oscillation frequency is directly affected by the speed of the transistor through the time delay t_d (3). This is however not directly important because a different oscillation is only changing the DC value at the output of the FDSM (2). The absolute size of the sensitivity is more important, because it is controlling the gain in the FDSM. On the other hand, because the limiting factor for the SNDR in the FDSM is linearity, a gain error, depending on the application, can be considered secondary. The most important impact from the process variation is deterioration of the linearity.

In these simulations only the *n*-MOS bulk is controlled resulting in major changes to sensitivity in a corner simulation because the transistor in the slow corner will be dominating the overall time delay of the inverter. When the *n*-MOS is in the slow corner, the output frequency is much more sensitive to input voltage changes than when the *p*-MOS is in the slow corner. This is a disadvantage when using only *n*-MOS input, but an advantage is, that the linearity is much less sensitive than when both *n* and *p*-MOS inputs are used.

In the strong inversion operation, where the nonlinearity was 0.5% without process spreading and mismatch, corner simulations showed that the worst case nonlinearity is 3.3%, which is acceptable as a worst case. A more reasonable result can be found through the 200 sample Monte Carlo simulation including both process variation and mismatch in Fig. 9. It is seen, that the nonlinearity will normally be limited to a value below 1%. In this case the oscillation frequency is

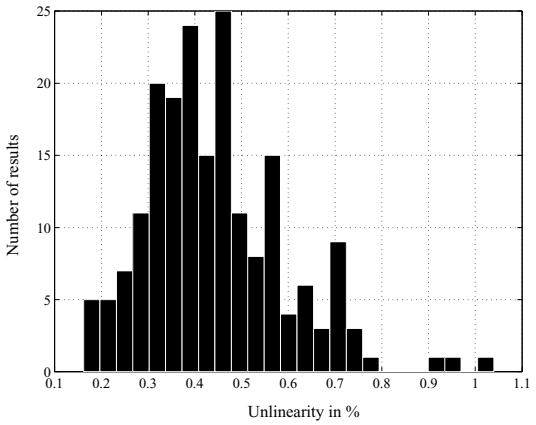

Fig. 9 Monte Carlo simulation on the nonlinearity including 200 samples supplied with 0.6 V

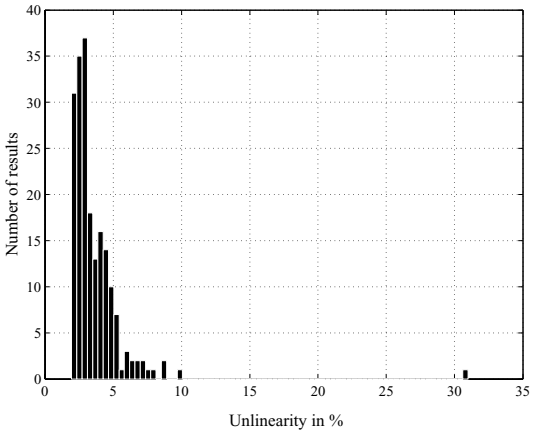

Fig. 10 Monte Carlo simulation on the nonlinearity including 200 samples supplied with 0.2 V

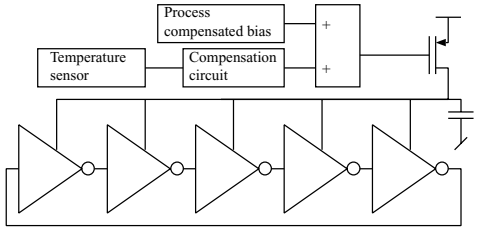

Fig. 11 Oscillator with soft rail transistor, process and temperature compensation

roughly independent of the corners, because a slow transistor is compensated by a fast transitor.

This is different in weak inversion where the soft rail is implemented as a p-MOS transistor. Due to this bias transistor, the oscillation frequency is changed quite much. If the bias voltage is fixed, the biasing in the corner simulation is changed, and the nonlinearity increases to an unacceptable level of 40%. The 200 sample Monte Carlo simulation in Fig. 10 indicates, that the nonlinearity will usually be smaller than what was found in the corner simulation, even though it often increases above 5% without tuning. A major advantage of the soft rail transistor is however, that if the bias voltage is tuned after fabrication, the influence from process variations on the linearity can be removed.

The influence from temperature changes are simulated at 0 and 70°C. In this temperature range, the nonlinearity increases to approximately 50% in the worst case for strong-inversion operations. In this case the strong-inversion simulations revealed a linearity slightly more dependent on temperature than weak-inversion simulations. Another important advantage in the weak-inversion soft-rail approach is again that a temperature dependent bias input should be able to compensate the temperature dependency. Dependent on the compensation circuit shown as a blackbox in Fig. 11, this system can reduce the temperature dependency much.

The noise found in the spectrum at the output of the FDSM can arise internally or externally. Assuming the clock signal has low enough jitter, the digital circuit can be assumed noiseless. This is a reasonable assumption, because clock jitter noise will be first-order shaped together with the quantization noise. The internal noise is produced in the RVCO, and is seen as phase noise at the output of the RVCO. At this point the signal is converted into phase, and the RVCO noise is thus directly added to the signal. The phase noise is dominated by $1/f^2$ and $1/f^3$ noise around the carrier. This is noise power, and it can be referred to the output if multiplied by f^2 due to the digital differentiation. It is therefore seen as white noise and $1/f$ noise at the output. At low frequencies where quantization noise is negligible, it is optimal, in terms of total power consumption to have a noise at the output limited by the power consumption of the RVCO, and because the phase noise is proportional to the power consumption of the RVCO, it is necessary to have a good noise rejection to the external sources.

When discussing noise rejection, the noise in the signal band at the input has the same transfer function as the signal, and will not be discussed. In the strong inversion there is thus only the supply voltage that works as a noise input. The output has a high sensitivity to the supply voltage, and thus a stable and low-noise supply voltage is needed.

When simulating the noise rejection originating from the supply voltage, phase noise is added to the supply voltage, and phase noise on the output is studied. From this result the phase noise gain (PNG) from supply to output is found.

When the soft rail approach is applied, an extra input which can inject noise is introduced. On the other hand the bias transistor is changing the PNG, and it is relevant to compare PNG for the four cases shown in Fig. 12. In circuit A there is no soft rail bias transistor, and the supply is thus the only noise input. When the soft rail transistor is included, noise is injected both in the bias terminal as in circuit B, where the noise is modulated on the bias current through g_m or through the supply voltage as in circuit C or D. The difference between these two circuits is, that in C the bias voltage is referred to the source of the transistor and in D the bias voltage is referred to ground. In C the gate source voltage is unaffected by the noise, and the noise is absorbed in the drain source voltage which is only modulating the bias current slightly. Contrary in D the noise is directly modulated on the bias through g_m of the transistor. It should be remembered that if the noise is injected on the supply voltage inside the chip, the noise is injected as in circuit D even with

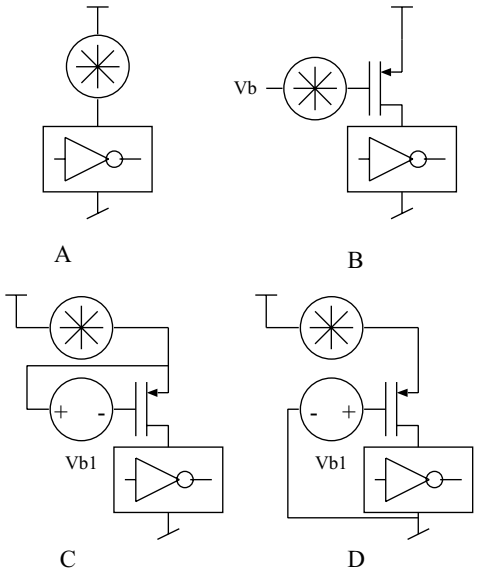

Fig. 12 Four cases of noise injection in the oscillator (A) Supply noise without soft rail (B) Noise injected in the bias input (C) Supply noise when bias voltage is referred to chip supply with soft rail and (D) Supply noise when bias is referred to ground with soft rail

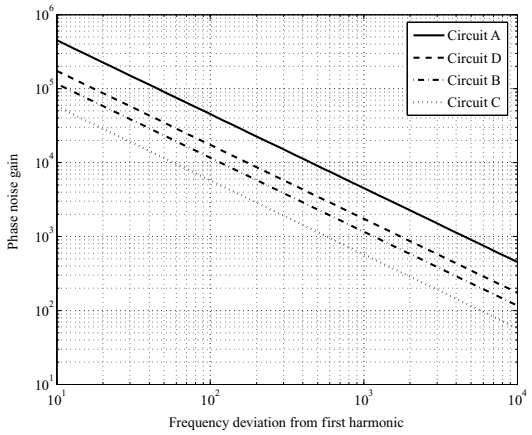

Fig. 13 Phase noise gain simulations for the four circuits illustrated in Fig. 12

the bias voltage referred to the supply voltage on the outside of the chip.

PNG simulation results for the four circuits can be seen in Fig. 13. The PNG simulations is a small signal periodic steady state simulation. White voltage noise is modulating the charging current and thus the output frequency. For low noise frequencies it is expected that the first order harmonic output frequency is directly modulated by the input frequency. This is also seen to be the case as the PNG shows a straight line in a log-log plot indicating an integration (2).

It is also seen, that the standard ring oscillator topology without soft rails results in a high PNG. When soft rails are included, the PNG is reduced by a factor of 3 when the bias is referred to ground. As expected the PNG is reduced even more when the bias voltage is referred to the supply voltage. When the soft rails are included, the noise on the bias is also important. As expected the PNG in circuit B is comparable to circuit D. Even when both supply and bias noise are included, it is seen, that the simulations indicates that less noise is transferred to the output when the soft rail approach is used.

6 Conclusion

Modulation linearity was discussed for inverter-ring voltage-controlled oscillators (RVCOs). This type of VCO was found to be a good realization for the integrator in an FDSM, where linearity in the conversion between input voltage and output frequency is important.

The RVCO was studied in two situations: when the supply voltage is high enough to bring the transistors in strong inversion, and when the supply voltage is low, forcing the transistors in weak inversion.

In strong inversion the influence from second-order effects was seen to be controlled by the supply voltage, where a lowering of the supply voltage increased the influence of these effects. Through simulations it was shown that, when the optimal supply voltage (0.6 V in this simulation) was found, the nonlinearity could be reduced to 0.5% for a full scale input signal. Corner and Monte Carlo simulations indicated, that if process variations and mismatch are included, the nonlinearity could increase up to 3.3% but will normally be within 1%.

In weak inversion it was seen that the modulation is generally nonlinear. The linearity was shown to be greatly improved by using soft rails for the supply voltage to the RVCO inverters. Through simulations on a RVCO supplied with 0.2 V this principle was shown to improve the nonlinearity from 27 to 2.4% for a full scale input.

Corner and Monte Carlo simulations indicated in this case that the nonlinearity often would be between 5 and 10% and could reach unacceptable values as high as 40% when process variations and mismatch was considered.

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Paper 5

A 0.2 V 0.44 μW 20 kHz Analog to Digital $\Sigma\Delta$ Modulator with 57 fJ/conversion FoM

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***Abstract*— This paper presents a 90 nm CMOS $\Sigma\Delta$ A/D modulator operating with a supply voltage of 0.2 V, well below the threshold voltage of the transistors. The modulator is an open-loop first-order architecture based on a frequency-modulated intermediate signal, generated in a ring voltage-controlled oscillator. The linearity of the modulator is greatly improved by the adoption of a so-called soft-rail in the oscillator. Measurements show a dynamic range of 52 dB over a 20 kHz signal bandwidth with a sampling frequency of 3.4 MHz, for a total power consumption as low as 0.44 μW. The corresponding peak SNDR is 44.2 dB, while the peak SNR is 47.4 dB.**

I. Introduction

A consumer market demanding ever smaller portable devices is, together with technology scaling, increasing the requirements on low voltage supply and low power consumption. Even though the MOS threshold voltage in future technologies can be assumed to continue decreasing, circuits containing transistors operating in strong inversion will very likely become even more problematic to design than they already are.

Traditional $\Sigma\Delta$ converters, both continuous- and discrete-time, make use of operational amplifiers, and are thus dependent on a supply voltage sufficiently higher than the MOS threshold voltage. In these converters, the feedback signal needs to be higher than the input signal, which reduces the input signal to a fraction of the supply voltage. Thus, if high resolution is required, the noise in the amplifiers needs to be very low, at the expense of power consumption.

The system presented in this paper is a frequency-to-digital $\Sigma\Delta$ modulator (FDSM) [1], where the input signal undergoes frequency modulation. An advantage of using frequency modulation is that the noise requirements in the internal circuits are not directly related to the available supply voltage. Furthermore, the FDSM does not make use of feedback, so that the maximum amplitude of the input signal is not constrained as in feedback-based $\Sigma\Delta$ converters.

This type of modulator includes a voltage-controlled oscillator (VCO) providing an integration of the input signal, a technique that has been previously demonstrated with an inverter-ring VCO (RVCO) controlled from the supply voltage [1]. In the present work, the VCO is an RVCO where the control terminal is the bulk contact of the transistors, which, thanks to a dual-well process, is possible for both nMOS and pMOS devices. This RVCO topology enables operations at extremely low supply voltages, provides a high impedance to the input signal, and even opens up the possibility of having input voltages exceeding the supply voltage in both the positive and the negative direction.

Since the modulator operates in an open-loop fashion, the intrinsic linearity of its blocks becomes extremely important, to avoid introducing distortion in the output signal. For this reason, linearity is the main concern in the design of the RVCO, since the RVCO itself does not provide a linear frequency modulation. However, the RVCO linearity is greatly improved by the adoption of a soft-rail, where the supply voltage to the RVCO is delivered through a voltage-biased transistor. The feedback provided by the soft rail enhances the linearity of the system by some 20 dB.

II. $\Sigma\Delta$ conversion with intermediate frequency modulation

The FDSM is, unlike the traditional $\Sigma\Delta$ converter, a $\Sigma\Delta$ modulator without feedback. The major advantage of feedback is that nonlinearities in the forward path of the modulator are suppressed by a high loop gain. This means that low-order single-bit modulators are simple to design. When a higher quantization noise suppression is needed, though, the single-loop higher-order modulators tend to become unstable, and when a multi-bit quantizer is used, nonlinearities are introduced by the D/A conversion in the feedback path.

Modulators without feedback, on the other hand, are always stable. However, since their nonlinearities are not mitigated by feedback, they must exhibit a sufficiently high intrinsic linearity. It may be worth noticing that digital correction of the nonlinearity is possible, to the extent that the nonlinearity itself is known.

The block diagram in Fig. 1 shows the implemented FDSM, where the input signal is first integrated, and subsequently applied to the quantizer, which can be single-bit or multi-bit. The output of the quantizer is a digital bit stream containing the integrated input signal with the additional quantization noise. A digital differentiator follows the quantizer, which means that the digital representation of the analog input signal

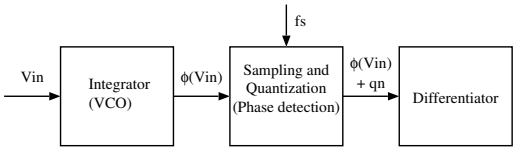

Fig. 1. Block diagram of the FDSM.

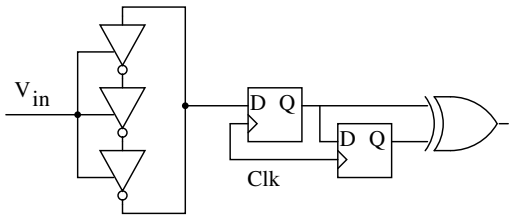

Fig. 2. First-order single-bit FDSM.

is found at the output of the modulator. The quantization noise, however, is subjected to differentiation only, which is equivalent to high pass filtering. Thus, the signal transfer function and noise transfer function in the FDSM are the same as in a traditional first-order $\Sigma\Delta$ modulator.

A digital differentiation $D(z)$ is given by

$$D(z) = (1 - z^{-1})$$

which, in a standard single-bit architecture, is easily accomplished with one flip-flop implementing the delay, and a XOR gate performing the modulo-2 subtraction.

The integrator could theoretically be a traditional operational-amplifier-based voltage integrator, but this solution would require a high supply voltage, and would therefore be inferior to the standard $\Sigma\Delta$ converter employing feedback. In the FDSM, the integration is obtained inside an RVCO, where the free-running oscillation frequency f_c is modulated by the control (input) signal $v_{in}(t)$ via the RVCO gain constant K_o. The phase $\theta(t)$ of the oscillation waveform is therefore written as

$$\theta(t) = 2\pi \int_{-\infty}^{t} (f_c + K_o\, v_{in}(\tau))d\tau \qquad (1)$$

which shows that the desired integration of the input signal has indeed been obtained. At the same time, the integration of f_c gives, after the following digital differentiation, an easily removed DC offset. The key advantage afforded by the RVCO integrator is that inverters are capable of operating in weak inversion, where they have been shown to be functional at supply voltages as low as 93 mV in a 0.6 μm process [2]. Signal quantization must be performed in combination with a phase detector; however, only zero-crossings need to be detected in a single-bit quantizer; in this case, phase detector and quantizer together turn out to be embodied by a single flip-flop.

A complete first-order single-bit FDSM is shown in Fig. 2, where the RVCO is made of an odd number of bulk-controlled inverters. One RVCO node is tapped into a flip-flop quantizing the phase signal, followed by a second flip-flop and a XOR gate implementing the signal differentiation. The XOR output is the desired $\Sigma\Delta$ bit stream.

In a first-order single-bit modulator, the signal to quantization noise ratio (SQNR) is given by [1]:

$$SQNR = 20\log\left(\frac{\sqrt{2}\Delta f}{f_s}\right) - 10\log\left(\frac{\pi^2}{36}\left(\frac{2f_{max}}{f_s}\right)^3\right) \qquad (2)$$

where Δf is the maximum frequency deviation from f_c (corresponding to the maximum amplitude excursion of the input signal), f_s is the sampling frequency, and f_{max} is the maximum frequency of the input signal. The SQNR can be improved by adopting a multi-bit quantizer, which, however, increases the complexity of the circuit in Fig. 2. A simpler way to increase the SQNR is to take advantage of the multiple output nodes in the RVCO; in fact, it can be shown [1] that the SQNR increases by $20\log(m)$, when m RVCO nodes are utilized.

From (2), it would seem that the SQNR does not depend on f_c; however, considering that Δf is proportional to f_c itself, it is clear that a way of improving the SQNR is to increase f_c.

III. VCO DESIGN

It has been mentioned that the fundamental advantage of the RVCO-based FDSM is the capability of deep subthreshold operations, thereby allowing the use of unprecedentedly low supply voltages in the $\Sigma\Delta$ modulator. Associated with this, however, is the important drawback that nonlinearities in the RVCO gain K_o are not suppressed by feedback on the input signal.

The oscillator frequency in the RVCO is [3]

$$f_c = \eta\frac{I_{ds,max}}{2NC_LV_{dd}} \qquad (3)$$

where N is the number of inverters in the ring, C_L is the load capacitance seen by each inverter, V_{dd} is the supply voltage, $I_{ds,max}$ is the maximum drain current charging C_L during a transition, and η is a scaling parameter, where $\eta I_{ds,max}$ is the mean current consumed by the oscillator. In principle, f_c can be controlled through one or more of the parameters C_L, V_{dd} and $I_{ds,max}$ in (3). Control of C_L can be obtained with different types of varactors, resulting in a possibly wide tuning range, but a very limited linearity. Using V_{dd} as control terminal results in a good linearity, but also in a quite limited input range, and a low and time-variant input impedance, which is undesirable. Controlling $I_{ds,max}$ through the bulk terminal of the transistors (i.e., by modulating the transistor threshold voltage V_{th}) yields a much more optimal input impedance. In weak inversion, the drain current I_{ds} in the MOS transistor depends exponentially on the gate-source

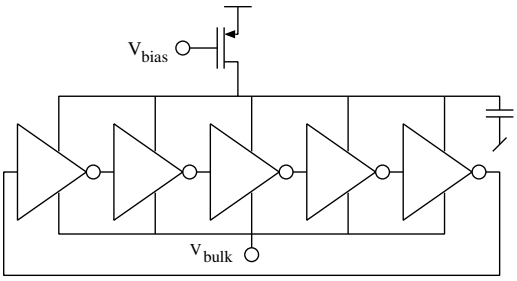

Fig. 3. RVCO with soft V_{dd} rail.

voltage V_{gs} as in a bipolar transistor, according to [4]

$$I_{ds} = I_0 e^{(V_{gs}-V_{th})/nV_T}\left(1 - e^{-\delta\frac{V_{ds}}{V_T}}\right) \quad (4)$$

where I_0 is a process-dependent current, V_{ds} is the drain-source voltage, δ and n are fitting parameters, and V_T is the thermal voltage, amounting to approximately 26 mV at room temperature. From (4), it can be shown that the maximum drain current $I_{ds,max}$ has the following proportionality [5]:

$$I_{ds,max} \propto e^{-\gamma\sqrt{2\phi_f - V_{bs}}/nV_T} \quad (5)$$

where γ is a process constant, ϕ_f is the surface potential of the MOS transistor, and V_{bs} is the bulk-source voltage. Clearly, $I_{ds,max}$ is a function of V_{bs} to a power higher than unity, and this will inevitably introduce distortion.

It can be noticed that, since the second-order derivative of $I_{ds,max}$ with respect to V_{bs} is always positive, the first-order derivative of the RVCO gain K_o is positive as well, and thus a negative feedback reducing the oscillation frequency when V_{bs} is increased is highly desirable, as this results in a more linear K_o. Since the maximum value of V_{gs} in (4) is equal to V_{dd}, it is clear that $I_{ds,max}$ is exponentially dependent on V_{dd}, which results in a strongly reduced current when V_{dd} is decreased. This can be used to improve the linearity of the RVCO by using a soft-rail technique, where V_{dd} is delivered to the RVCO through a pMOS bias transistor, as shown in Fig. 3.

The principle is that, when V_{bs} is increased, I_{ds} increases as well, resulting in an increased mean total current consumption in the RVCO, which flows through the soft-rail transistor. This, in turn, has a fixed gate-source voltage, and thus its drain-source voltage will increase with an increased drain current. Seen from the RVCO, this is equivalent to a reduction in the supply voltage, and the desired negative feedback on I_{ds} and K_o is thus obtained. Seen from another point of view, this approach trades modulation depth (since both V_{dd} and I_{ds} are reduced in (3)) for an improved linearity.

The amount of linearization obtained can be controlled through the dimensions and the bias voltage of the soft-rail transistor.

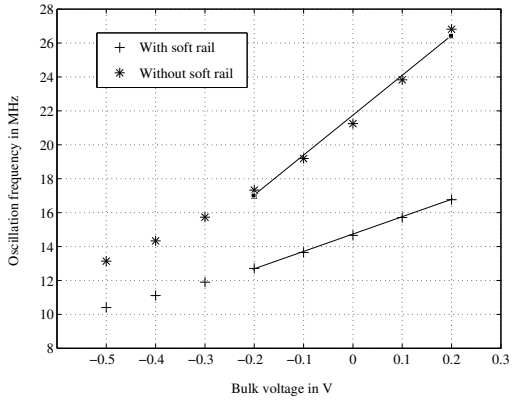

Fig. 4. Modulation linearity improvement with the soft rail technique.

IV. Measurement results

A complete single-bit FDSM has been implemented in a standard 90 nm CMOS process. The core of the modulator includes a 15 stage RVCO, where both nMOS and pMOS bulk terminals are controllable. The flip-flops are standard master-slave realizations, and the XOR gate is built with NOR logic cells. The design includes also a readout circuit consisting of five additional flip-flops and output buffers. The active die area is 100μm$\times 200\mu$m; a chip photograph is not included, since all details are hidden behind dummy metal patterns added by the foundry.

The FDSM was found to be operational with a power supply down to 0.18 V, while all measurements presented here are obtained with $V_{dd} = 0.20$ V. With the pMOS bulk tied to the supply and the nMOS bulk tied to ground, f_c is approximately 14 MHz, with a sensitivity of 10 MHz/V. This result is obtained with a soft-rail transistor bias voltage of approximately 0 V, which is also the bias voltage providing maximum linearity. Such a value of f_c is too high to allow oversampling in the quantizer and in the differentiator; this is not, however, a severe limitation, since undersampling is allowed [1], trading a reduced SNR for a reduced power consumption. The power consumed by the oscillator is $0.18\,\mu$W (0.2 V$\times 0.9\,\mu$A). The total core power consumption is $0.44\,\mu$W (0.2 V$\times 2.2\,\mu$A) at the sampling frequency of 3.4 MHz.

The influence of the soft-rail transistor is illustrated in Fig. 4, where the oscillation frequency of the RVCO is plotted as a function of the input voltage. The bias voltage of the soft-rail transistor was adjusted to linearize K_o for values of the input (control) signal in the vicinity of 0 V. The soft-rail transistor can not be bypassed, but by applying a large negative voltage (e.g., -1 V) to its gate, it was effectively turned into a short circuit. The linearity of the curves in Fig. 4 is clearly improved when the soft-rail is active, at the expense of a reduced modulation depth. The increased linearity results in a 20 dB higher spurious-free dynamic range (SFDR) in the output spectrum, when the input signal is 10 dB below its

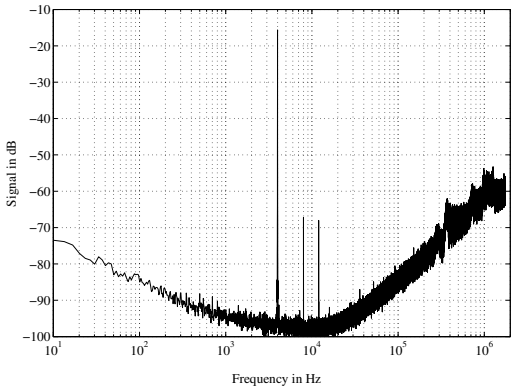

Fig. 5. Output spectrum providing maximum SNDR over a band from 20 Hz to 20 kHz.

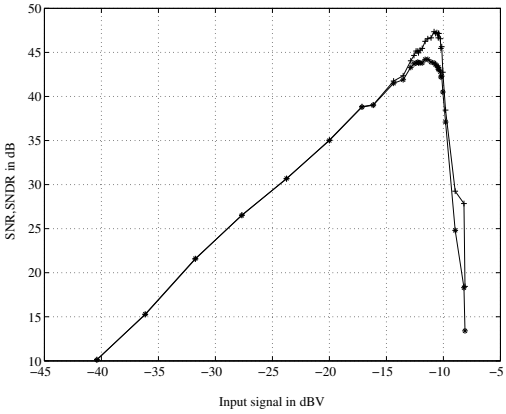

Fig. 6. Measured SNR and SNDR versus peak to peak input signal amplitude.

maximum level.

The output spectrum corresponding to maximum SNDR is shown in Fig. 5. The SNR is limited by white noise up to the audio band limit of 20 kHz. Fig. 6 shows both SNR and SNDR as functions of the amplitude of the input signal. The maximum SNDR is 44.2 dB, and the maximum SNR is 47.4 dB, both measured with a 4 kHz input tone over the full audio band from 20 Hz to 20 kHz. The dynamic range (DR) is approximately 52 dB.

No previously demonstrated modulators have been operating on supply voltages as low as 0.2 V. Therefore, the performance of the modulator is compared to the state-of-the-art through the well-known figure-of-merit (FoM) [6]

$$\text{FoM} = \frac{P}{2BW \cdot 2^N} \tag{6}$$

TABLE I
SUMMARY OF MEASURED PERFORMANCE.

Clock frequency	3.4 MHz
Signal bandwidth	20 kHz
DR	52 dB
Peak SNR	47.4 dB
Peak SNDR	44.2 dB
Supply voltage	200 mV
Power consumption	0.44 μW
Active chip dimensions	100x200μm^2
FoM	57fJ/conversion
Technology	90 nm triple well CMOS

where P is the power consumption, BW is the signal bandwidth, and N is the effective number of bits of the converter, which is here calculated to 7.6 from the SNR data. This results in the very low FoM of 57 fJ/conversion. Compared to other state-of-the-art audio converters (see e.g. [7] [8]), the achieved result is very competitive. The performance of the modulator is summarized in Table I.

V. CONCLUSIONS

A complete analog-to-digital modulator providing first-order $\Sigma\Delta$ noise shaping has been presented. The modulator, which adopts an open-loop architecture, is based on a VCO integrating the input signal, followed by a digital differentiation. The 90 nm CMOS prototype allows operations at a 200 mV supply voltage, for a power consumption of only 0.44 μW. To improve the linearity of the frequency modulation performed in the VCO, a soft-rail bias transistor is used in the VCO, which results in a 20 dB linearity improvement. The SNDR, SNR and DR performances of the modulator were measured to 44.2 dB, 47.4 dB and 52 dB, respectively, over a full 20 kHz audio signal band.

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