A Miniature Recording Cardiotachometer

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host of any changes in its own status. No matter what the error, the EAR task maintains a System Error Log in a non-volatile memory so that maintenance personnel at a later date may have a record of all system failures and their known causes.

Maintenance Port

The Maintenance Port (MP) is a standard serial interface on the LMG bus which allows either a CRT or a maintenance computer to communicate with the MGP. Communicating through this port, a Maintenance Support task provides a wide range of capabilities for controlling and monitoring the entire RLU operation. All commands available through service messages can be issued through the MP, in addition to standard debug functions such as reading from any memory location. Thus local processing tasks can be loaded and initiated, and data transfers through SM can be performed without using the LCU or BIU; or the Maintenance Support task can simply monitor specific actions taking place while on-line to the host computer.

V. CONCLUSIONS

An architecture has been proposed for the RLU, an advanced remote terminal system for data acquisition and control applications. The distributed architecture involves the use of separate, specialized processors with a careful partitioning of functions among the processors. Communication between the processors is through a combination of direct memory access and true shared memory. Since each processor is programmable, it is possible to vary through software the communications protocol (LCU), the RLU supervisory functions and backup processing (MGP), and the signal processing interface to the subsystems (LMP). Although there is an increase in hardware (CPU's and memory) over conventional remote terminal designs, these costs are rapidly diminishing as a design factors. Indeed, these costs will be more than offset by savings realized from the increased functionality, flexibility, and maintainability of the RLU.

ACKNOWLEDGMENT

The authors wish to acknowledge the contributions of G. W. Batten who participated in this project.

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A Miniature Recording Cardiotachometer

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***Abstract*—The design of a miniature, recording cardiotachometer is described. It is simple and can store digital data. Bench and field tests, using a hand-held display, are presented. Construction and principles of operation are discussed. Applications, with performing athlete subjects, are outlined.**

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INTRODUCTION

CARDIOMETRIC instruments have been peculiar to medical diagnosis. Conventional cardiographs [1], [2] are large instruments, usually multichannel. Even "portable" single-channel devices are about the size of a small suitcase.

Cardiographs detect, amplify, and record the potential changes due to the motor neuron activity responsible for the stimulation of the contractions of the involuntary muscles of the circulatory system. Cardiotachometers, on the other hand, only provide a measure of the heart rate or the interval time between successive heart beats.

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Conventional tachometers generate a dc signal proportional to heart rate or beat interval and display this on an analog meter or digital readout [3]. Adapting these devices for recording requires peripheral equipment. The need for a very small recording cardiotachometer for the training of athletes led to the development of the instrument described herein.

This instrument which has a TTL compatible parallel interface was developed in collaboration with the McGill Biomechanics of Sports Medicine Laboratory which combines the disciplines of mechanical engineering, physical education, and orthopaedics. Some MBMSML projects involve the acquisition of vital function data from "free" (rather than "captive") athlete subjects. The concept of "freedom" versus "captivity" may be illustrated by considering that subjects who are instrumented with electromyographic electrodes may swing a golf club, baseball bat, or hockey stick or may even practice sprint starts while cabled to a stationary data acquisition system. These subjects are "captive" as is, even a skater with radiotelemetric instrumentation who cannot be monitored beyond the range of his miniature transmitter. The cardiotachometer design requirements are peculiar to an orienteering[1] subject who runs four hours over rugged, often wooded terrain, where he is crested or out of range to a stationary receiver and inaccessible to a vehicle based one.

The specifications may be summed up as follows:

1) cigarette-pack size and less than 500 g with battery,
2) low power and no moving parts,
3) convenient data retrieval,
4) 1024 data words of 8-bits, taken at 10-s intervals and covering the range of feasible heart rate extremes,
5) mass produced cost under $100.00.

Design features include:

1) amplification and filtering of the EKG signal,
2) "QRS complex" detection with rejection of occasional large amplitude "T waves,"
3) successive "QRS" events gate a reference frequency into a negative offset preloaded counter,
4) 1K by 8-bit ultra-low-power RAM memory,
5) data retrieval via a simple parallel interface.

GENERAL DESCRIPTION–FIG. 1

The cardiotachometer is composed of:

1) The Analog Input Module which conditions and digitizes the incoming EKG signal.

2) The Beat Period Accumulator in which the heart beat is counted.

3) The Clock Module which synchronizes the operating sequence.

4) The auto-incrementing Data Address Register.

5) The Memory Module to store the beat period data.

6) The State Controller which defines the operating sequence.

The State Controller logic can be conveniently decomposed into four functional submodules:

[1] Orienteering involves cross-country racing where the participants navigate with map and compass. Constraints such as checkpoints and timed legs, similar to those of automobile rallying, are included.

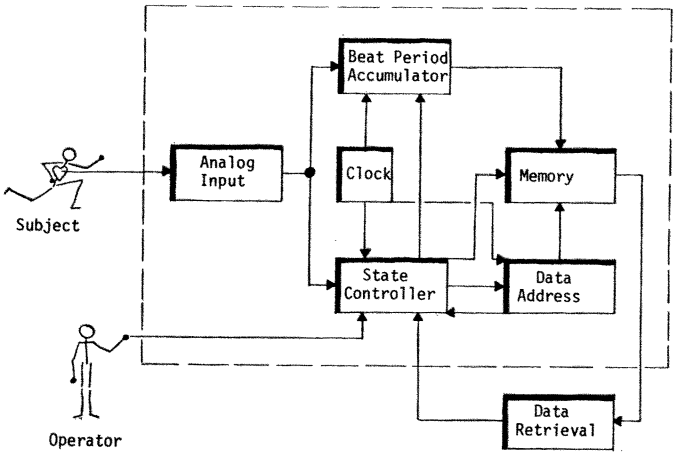


Fig. 1. Cardiotachometer block diagram.

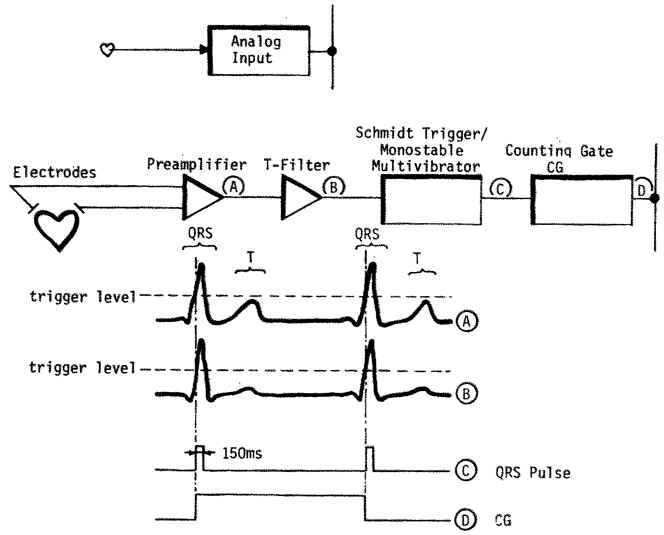


Fig. 2. Analog input and digital conversion.

a) The Flag Generator which indicates when acquired data are to be stored.

b) The Reset Generator which clears the memory when the tachometer is started, then starts the data acquisition sequence.

c) The Write Controller which controls data transfer to memory during both clearing and data acquisition sequences.

d) The Transition Controller which is the master control that responds to external signals and clock transitions by activating other submodular functions.

An operating synopsis is provided by two timing diagrams and a state transition diagram which follow the detailed module descriptions below.

ANALOG INPUT MODULE–FIG. 2

A pair of silver/silverchloride chest electrodes, with potassiumchloride gel to minimize contact resistance and electrode/skin potential, provides analog input to the tachometer. This EKG signal is conditioned by a differential input instrumentation amplifier (AD521) and a second stage (μA741) active bandpass filter. The "QRS complex" of the EKG has a shorter rise time than the secondary "T wave." The filter thus tends to reduce the relative "T wave" amplitude thereby preventing a second counting gate transition during any given beat period.

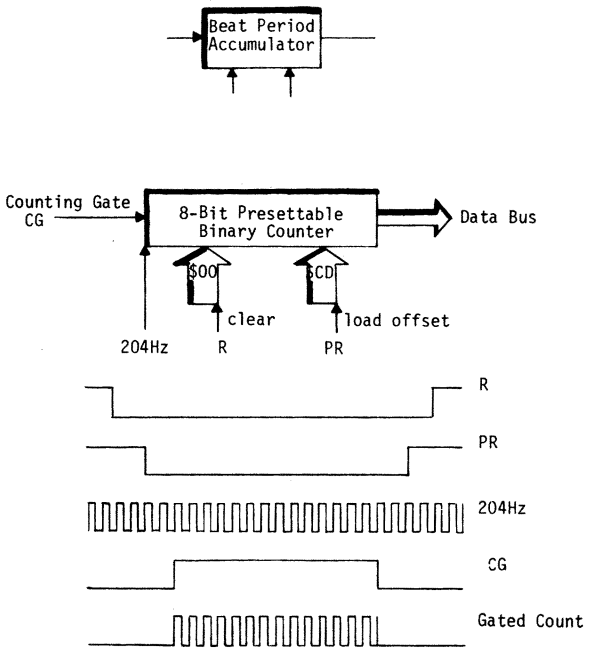


Fig. 3. Heart beat period measurement.

The rising edge of the "QRS complex" Schmitt triggers a single shot which produces 150 ms long, logic level pulses at heart rate frequency. A toggle flip-flop produces a true counting gate signal, CG, during every second heart beat interval.

BEAT PERIOD ACCUMULATOR–FIG. 3

This 8-bit counter acquires and holds data to be stored in memory. During initialization, the true R (Reset) signal maintains a null count so that $00 (hexadecimal) is written into all memory locations in the first second after EXT RST (External Reset) was pressed.

During data acquisition, after initialization, the high going PR (Preset) signal loads an offset of −51 or rather the 8 least significant bits of its 9-bit 2's complement ≡ $CD. This offset, together with gated frequency of 204 Hz, was chosen so that an 8-bit count represents the beat period range $00 ≡ 0.25 s to $FF ≡ 1.5 s. This is equivalent to heart rates of 240 beats/min ≡ 4 Hz to 40 beats/min ≡ 2/3 Hz. The 204-Hz clock is gated into the counter while CG (Counting Gate) is true, yielding a completed beat period measurement when CG falls. The period during which CG is false provides time for data storage to take place.

CLOCK MODULE–FIG. 4

This is a 5-MHz crystal oscillator with frequency division to furnish:

1) 156 kHz to strobe the State Controller and memory,
2) 1 kHz to clear memory during initialization,
3) 204 Hz to manufacture data in the Beat Period accumulator,
4) 0.1 Hz to set the storage request flag which initiates a data storage sequence.

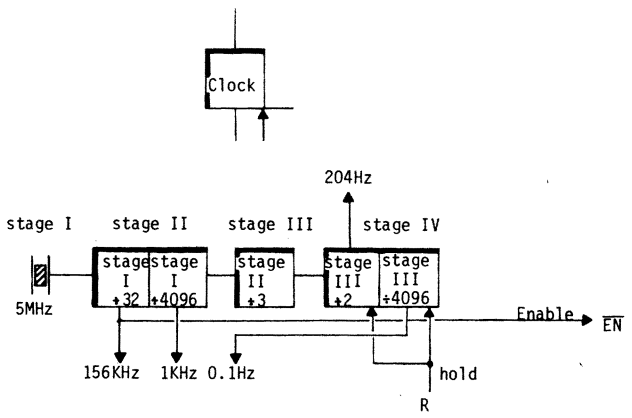
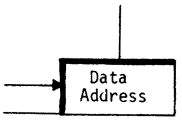


Fig. 4. Synchronous timing signals.



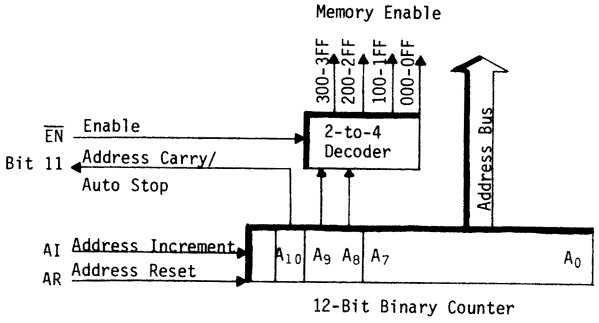


Fig. 5. Data Storage Address generation.

DATA ADDRESS GENERATOR–FIG. 5

This is a 12-bit binary counter which is cleared by the signal AR (Address Reset) on the rising edge of R, before the memory is cleared, and again when R falls, when clearing is complete. Thus the first measurement will be stored at address $000. The address is incremented after data storage by the signal AI (Address Increment). The signal EN (Enable) strobes data into the currently addressed memory location. The signal Bit 11 (Carry) becomes true after "address wraparound" and terminates the memory clearing procedure. It also stops the acquisition of data after memory has been filled.

MEMORY MODULE–FIG. 6

During a Write cycle, data in the Beat Period Accumulator is transferred to the memory byte addressed by the eight low-order address bits, applied to every 256 X 4-bit RAM chip (HM6562-D5), and the four "Enable" lines which represent the decoded high-order bit pair. Each line enables a pair of chips since two chips are required to hold a data byte. The selected "Enable" line is strobed by the 156-kHz clock. This

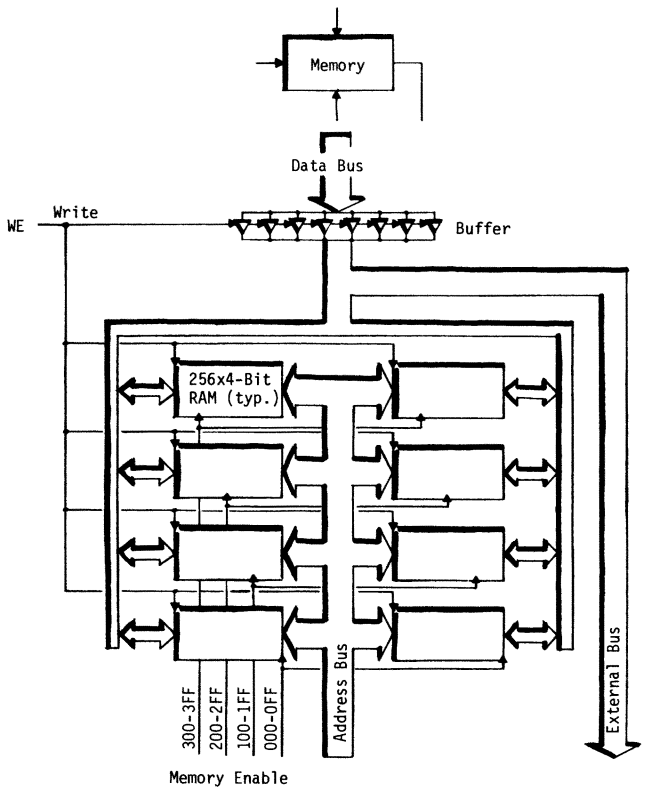


Fig. 6. Memory access and control.

strobe overlaps the signal WE (Write Enable) aperture, generated by the State Controller, which enables the tri-state buffers on the data bus and holds the memory in the "Write" mode.

The data bus is accessible at an external connector as are the three external control lines, AR, EN, and AI, which are *ORed*, respectively, with their internal counterparts. Thus stored data may be read, in sequence beginning at \$000, by any 8-bit parallel input device with three control lines that can

1) toggle AR to reset memory address to \$000,
2) toggle $\overline{\text{EN}}$ to access the addressed data byte,
3) toggle AI to advance the memory address.

No read/write control is required since the memory is normally held in its safe "Read" state when the tachometer is stopped.

STATE CONTROLLER–FIG. 7

The State Controller generates asynchronous timing signals, as opposed to clocks, which invoke various tachometer operating cycle functions. These signals include the following expressed as functions of other signals:

1) $SRF_{n+1}(SRF_n$, 0.1 Hz, AI)
2) $Q1_{n+1}(Q1_n, Q2_n$, CG, SRF, Bit 11)
3) $Q2_{n+1}(Q1_n$, Bit 11)
4) $R(Q_1, Q2)$
5) WE(1 kHz, R, CG, Q_1)
6) AI(WE)
7) PR(1 kHz, R, CG).

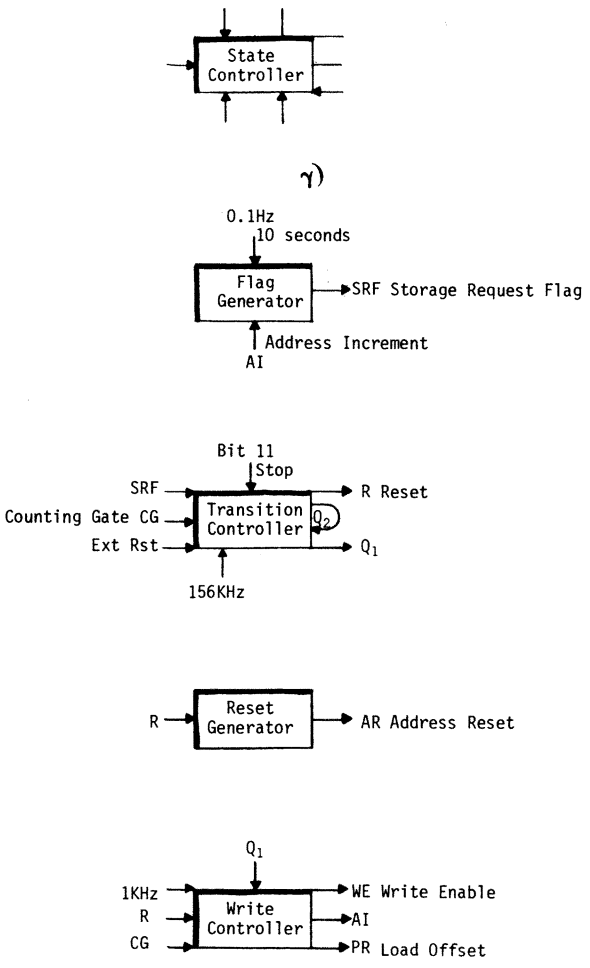


Fig. 7. Asynchronous timing signals.

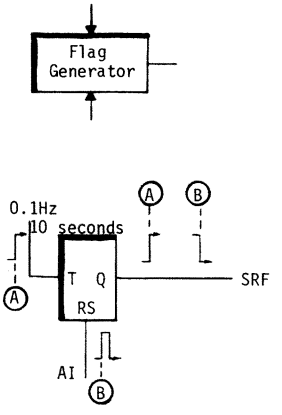


Fig. 8. Storage request flag generator.

FLAG GENERATOR–FIG. 8

This is a toggle flip-flop which changes state on the rising edge of the 0.1 Hz/10 s clock; the storage request signal. When AI increments the memory address after data storage it also clears the flip-flop output signal SRF (Storage Request Flag) via the direct clear input.

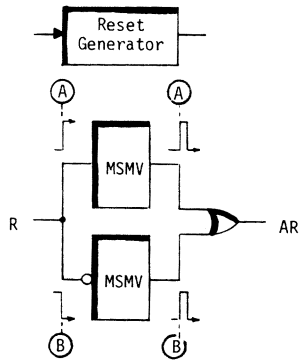


Fig. 9. Address reset pulse generator.

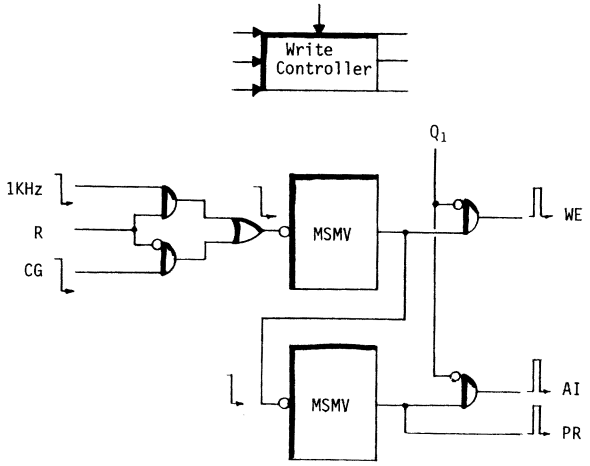


Fig. 10. Write enable, address increment, and load offset signal generation.

RESET GENERATOR–FIG. 9

The signal pulse AR (Address Reset) is the *ORed* output of a pair of monostable multivibrators (MSMV). One triggers on the rising edge, the other on the falling edge, of the signal R (Reset).

WRITE CONTROLLER–FIG. 10

The Write Controller is a tandem pair of MSMV's. The second one unconditionally generates an output pulse on the falling edge of the output pulse emitted by the first. This "two shot" sequence occurs a) on the falling edge of the 1-kHz clock during initialization when R is high or b) on the falling edge of CG when the tachometer is in the data acquisition mode. Notice that the signal PR is generated every time CG falls, however, the signals WE and AI occur only during initialization and during a Write cycle; when Q_1 is low.

TRANSITION DIAGRAM AND STATE CONTROLLER–FIGS. 11 AND 12

The function of the Transition Controller is described by its two control signal outputs, Q_1 and Q_2, which define the operating states of the tachometer. These are

1) *Start* $(0,0) = (\bar{Q}_1, \bar{Q}_2)$,
2) *Write* $(0,1) = (\bar{Q}_1, Q_2)$,
3) *Halt* $(1,0) = (Q_1, \bar{Q}_2)$,
4) *Write* $(1,1) = (Q_1, Q_2)$.

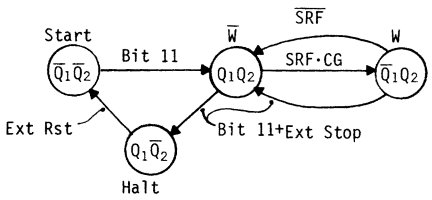
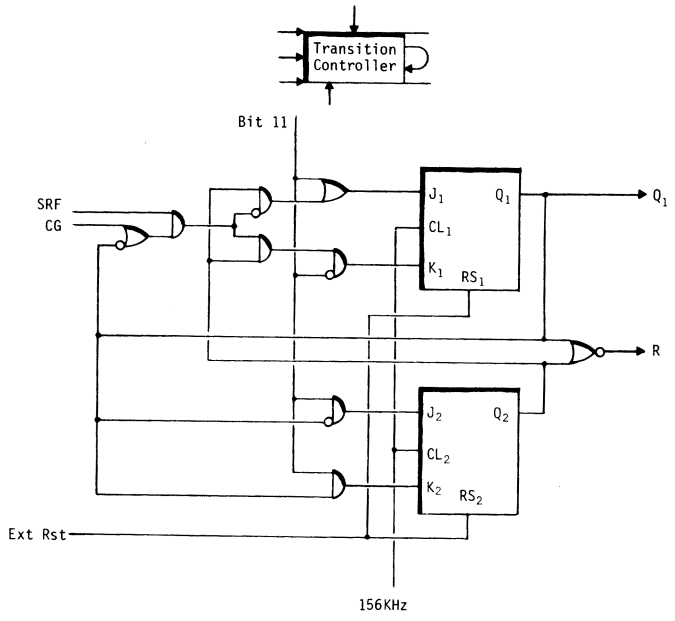


Fig. 11. State transition diagram.



$J_1 = ((\overline{CG+\bar{Q}_1})\cdot SRF\cdot Q_2)+Bit\ 11$

$K_1 = (CG+\bar{Q}_1)\cdot SRF\cdot Q_2\cdot \overline{Bit\ 11}$

$J_2 = \bar{Q}_1\cdot Bit\ 11$

$K_2 = Q_1\cdot Bit\ 11$

$R = \overline{Q_1+Q_2}$

Fig. 12. Transition controller logic.

In the *Halt* state R is held low and WE and AI are blocked by Q_1; no data storage can take place. Furthermore, $Q_1\bar{Q}_2$ feedback combination prevents the Transition Controller from changing state under the influence of any combination whatsoever of SRF, CG, Bit 11, or 156-kHz signals. *Halt* is a blocked state from which there is no exit except by an operator initiated EXT RST signal which unconditionally forces a *Start* state. After initialization, the Bit 11/Carry signal, which indicates that memory has been zeroed, forces a *Write* state on this occasion only because the low going signal R causes an AR pulse to clear Bit 11 before a *Halt* state is established. A *Write* state exists when SRF · CG = 1. This state reverts to *Write* after data has been stored and the signal AI clears SRF. When memory is full or if the operator presses EXT STOP, the Transition Controller blocks into the *Halt* state.

CLEARING OF MEMORY/INITIALIZATION–FIG. 13

The transitions between *Halt* and *Start* and between *Start* and *Write* are detailed in this timing diagram. Note that the falling edge of Q_1, in concert with a prevailing $Q_2 = 0$, generates the rising edge of R on entry to the *Start* state. This renders an Address Reset pulse, AR. The prevailing R = 1 during *Start* gates the 1-kHz clock to the two MSMV's of the write control-

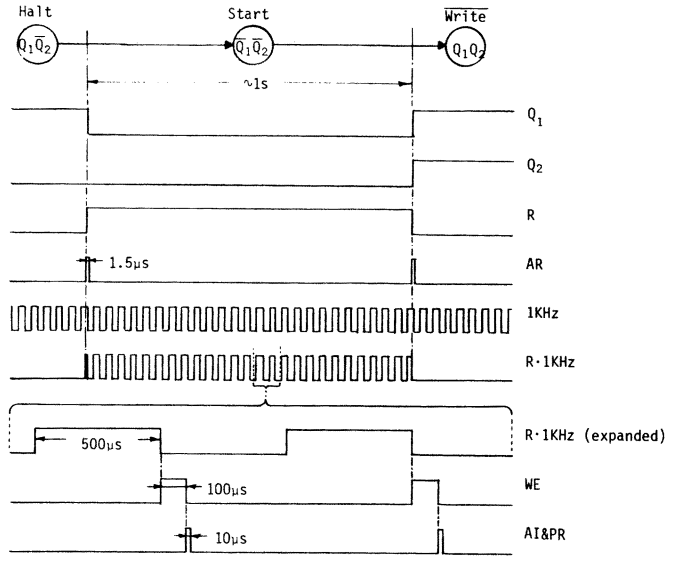


Fig. 13. Memory clear during start ($\bar{Q}_1\bar{Q}_2$) state.

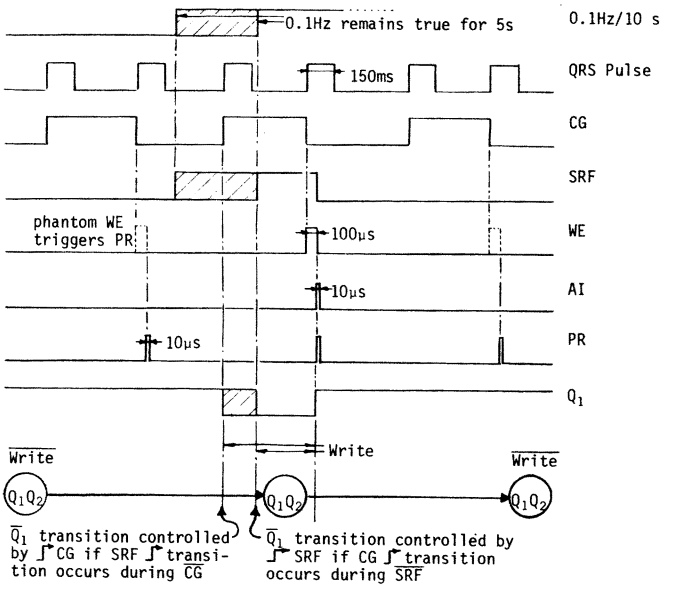


Fig. 14. Memory storage cycle timing sequence.

ler. Each falling edge of this clock stimulates a WE→AI/PR sequence until all memory has been zeroed and Bit 11 arrives. A second AR pulse resets the memory address to $000, once again, this time on the falling edge or R and the Transition Controller establishes the data acquisition posture of the tachometer in the *Write* state.

DATA STORAGE/MEMORY WRITE CYCLE–FIG. 14

The Beat Period Accumulator contains valid data at every falling edge of CG. If the Transition Controller is in a *Write* state and SRF has been set by the 0.1 Hz/10 s Storage Request clock, a write cycle will be initiated. The *Write* state is entered when CG rises if a rising edge of SRF occurred during a low CG. Conversely, *Write* begins with a rising SRF if this transition occurs while CG is high. In either event, the *Write* state prevails during some finite portion of a high CG interval. When CG falls during a *Write* state, a WE pulse is emitted. Simultaneous AI and PR pulses arise as WE falls. The falling edge of WE also restores $Q_1 = 1$ and the attendant *Write* state. Notice that WE and AI emerge only when the gating of the Write Controller outputs are enabled by $\bar{Q}_1$. Since PR is not so gated, the preset signal loads the offset count into the Beat Period Accumulator on the falling edge of the frustrated or "phantom" WE pulse, upstream of its gate, after every low-going CG transition.

BENCH TESTS AND RESULTS–FIG. 15

The attenuated square-wave output of an HP-3300 Function Generator was used to provide a calibration signal of stable but adjustable amplitude and frequency. Fig. 15 shows this differential signal input to the AD521 preamplifier. It was established that this amplifier, equipped with a 10-kΩ adjusting resistor, could be trimmed to produce a stable, noise-free, logic level pulse at the "T wave" filter output B down to a low limit input of ~5 µV. Since EKG electrode output is typically ~100 µV, the cardiotachometer's input sensitivity is quite adequate. Simulated heart rates between 0.7 and 3.5 Hz (45 to 210 beats/min) were reliably measured and stored to within ±1 count resolution. It can be seen that the heart rate R is

$$R = \frac{60C}{M+F}$$

where

- R heart rate, beats/min,
- M 8-bit count stored in memory,
- C 204-Hz clock output from Stage IVa ≡ (Stage III)/2,
- F = 205, the initial count, $CD ≡ −51, preset into the Beat Period Accumulator before each measurement cycle.

MANUAL READOUT AND CONTROL UNIT–FIG. 17

It is intended to develop a hand-held microprocessor based readout and statistics calculator module as well as to completely repackage the prototype tachometer for minimum size. Currently, however, the unit is mounted as shown in Fig. 16. The operator controls, EXT RST, and EXT STOP, are the two microswitches seen between the terminal strips. Although the 8-bit data bus, power connections, and external controls, EXT AR, EXT AI, and EXT EN are brought out here, only the EKG electrode inputs (EKG1 and EKG2), battery connections (±9 V, +5 V, and Ground), and Analog Input monitoring points (Ⓐ and Ⓑ) were used during bench and field tests.

In order to monitor address incrementation during data acquisition and to examine the data recorded in memory afterwards, a hand-held address control and address and data readout unit was constructed. The unit is shown in Fig. 17 and it is connected to the tachometer with a flexible cable and plug assembly which conveys:

1) logic power and ground,
2) control signals EXT AI, EXT AR, and EXT EN,
3) the 8-bit data and 10-bit address buses.

The address and data are displayed in binary on separate rows of light-emitting diodes (LED's). By using a large 4.5-V dry cell (rather than a miniature battery pack, required when the tachometer is worn by a subject), sufficient power is available for the eighteen LED's and attendant buffers and

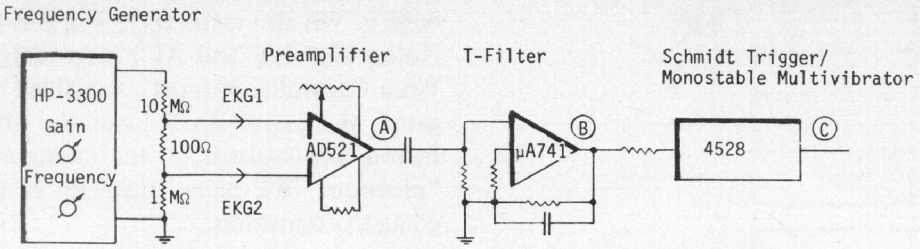


Fig. 15. Analog input calibration circuit.

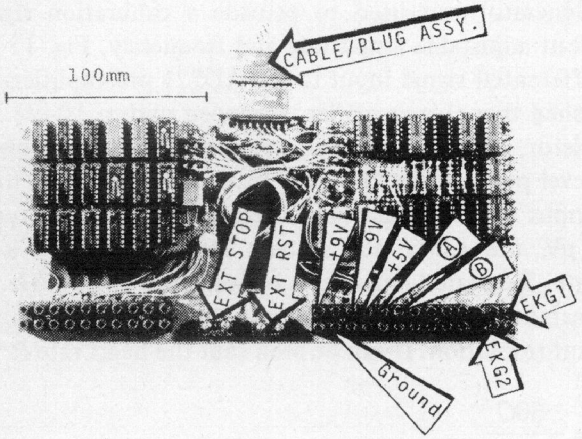


Fig. 16. Prototype cardiotachometer.

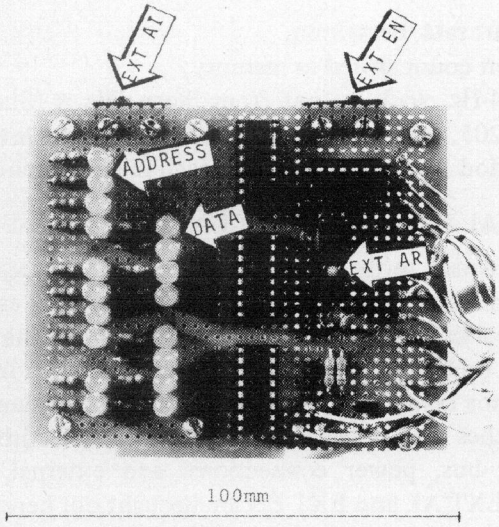


Fig. 17. Readout unit.

logic as well as to power the tachometer. The CMOS memory and the Data Address Generator drive the display via 8T96 tristate buffers. Only the EXT AI switch requires debouncing so as to prevent multiple increment pulses. Multiple triggering of EXT AR or EXT EN causes no problem.

FIELD TESTS AND RESULTS—FIG. 18

A subject was instrumented with EKG electrodes attached on the sternum and under the left nipple, respectively. The leads were connected to EKG1 and EKG2. Heart rates, in the range 60 to 90 beats/min, peculiar to subject sitting or standing at rest, were measured and recorded. The recorded beat periods compared favorably with intervals measured from EKG signal oscillograms shown in Fig. 18. Fig. 18(a) shows a raw EKG,

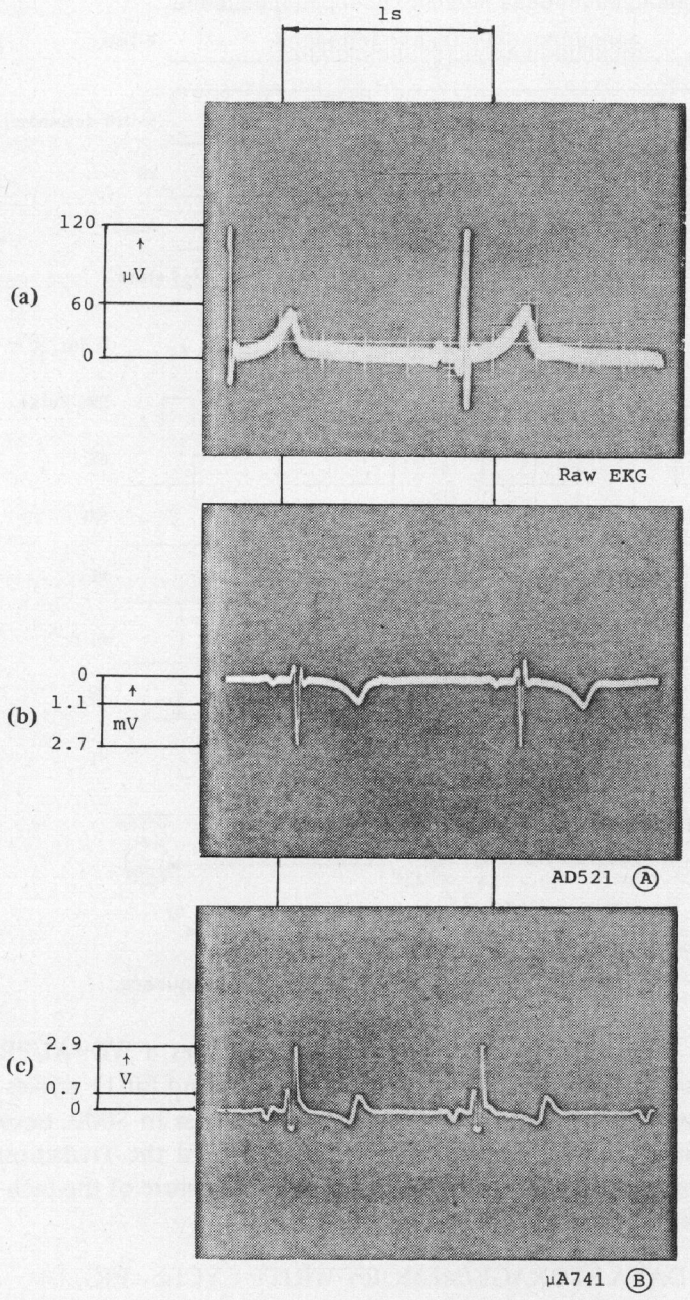


Fig. 18. EKG signal oscillograms. (These are *not* simultaneous traces; they are, however, typical of the waveforms obtained at the three respective test points from a normal human subject at rest with a heart rate of about 60 beats/min.)

obtained directly from the chest electrodes with a storage oscilloscope using a high-gain differential plug-in (1A7). This signal has a ~120-μV "R" peak, measured from base line, and a ~60-μV "T" peak. Output of the preamplifier (AD521) at Ⓐ is shown in Fig. 18(b) where 2.7-mV "R" and 1.1-mV

"T" spikes can be seen. Fig. 18(c) is the output of the T-filter (μA741) measured at Ⓑ . The analog amplifiers have boosted the "R" peak, used to trigger CG, to a comfortable 2.9-V, TTL compatible pulse. While the "R" signal has been amplified by a factor of $\sim 2 \times 10^4$ the T-filter has reduced the T/R amplitude ratio from ~0.5 to less than 0.25. The "T wave" has sufficient margin so as to avoid spurious triggering of the MSMV output, Ⓒ.

The cardiotachometer, which consumes only 75 mW, is easily powered by miniature batteries. In contrast, the 18 LED's, resistors, and 4 TTL packages of the readout unit require 20 times as much. This additional load, absent during data acquisition, is mentioned only as a comparison to emphasize the tachometer's ultra-low power feature.

PLANS AND APPLICATIONS

Development plans include the following:

1) Substantial reduction in size which can be accomplished by using a multilayer PC board and by substituting 512 X 4-bit memory for the current 256 X 4-bit RAM, thereby saving four chips.

2) The evolution of a hand-held readout and statistics computation unit, possibly including a miniature printer.

3) The development of a single-channel EKG data acquisition and storage unit with low power/high density memory; this would use a conventional 8-bit ADC and would have a 64K byte memory and a 500-Hz sampling rate.

Although the proposed electrocardiograph appears to seriously compromise the small size and power consumption achieved by the tachometer design, consider that at current memory packing density only an additional 800 cm^2 of board space would be required. A 64K 512 X 4-bit memory would fit on only 400 cm^2. The power consumption of a 64K 256 X 8-bit memory would be just over 28 mW and it is believed that the entire EKG unit would consume no more than 150 mW.

The tachometer will initially be used to monitor and to help train orienteers. These athletes constitute an excellent example of subjects who are unsuited to telemetric instrumentation. Another application involves the monitoring of military parachutists during actual jumps. In this regard, it is intended to check what appear to be unbelieveably high heart rates (up to 280 beats/min!) reported in [4]. It is suspected that the tape recorders used in these experiments were strongly affected by inertial shock, an effect to which a solid-state instrument would be immune.

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