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Kamel, Ayadi; Danielsen, Per Lander

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A 100 MHz Synchronized OEIC Photoreceiver in N-well, CMOS Technology

Kamel Ayadi and Per Danielsen

Technical University of Denmark, COM center, Building 348, DK-2800 Lyngby, Denmark
tel: +45-45 253876, fax: +45-45 871866, e-mail: ka@com.dtu.dk

Abstract— **We analyze and demonstrate a synchronized CMOS photoreceiver for the conversion of optical inputs of pulse-light to electronic digital signals. Small-signal and photonic analysis of the proposed circuit are detailed. The photoreceiver was operated at 100 MHz with only 13.3 fJ/pulse of 830-nm input light. Its effective area is 100 × 60 μm² which makes this monolithic photoreceiver extremely important for use in data storage and optical interconnection applications.**

I. INTRODUCTION

It is reported in [1] that by 2001, the integration density for silicon CMOS field-effect transistor logic is expected to be up to 13 million transistors and the projected on-chip clock rate to be 600 MHz. The enormous bandwidth that will be available for computation and switching on a silicon IC will create an increasing demand for high-bandwidth input and output (I/O) to a VLSI circuit. The optical interconnection should overcome this need of I/O. This will encourage the development of high-density, high-speed CMOS photoreceivers for the evolution of optoelectronic very-large-scale integrated circuits (OE-VLSI).

In this paper we report about a monolithic photoreceiver, in full CMOS technology, for conversion of optical pulses to electronic digital signals.

II. OPERATIONAL PRINCIPLE AND ANALYSIS

II.a. Photoreceiver circuit

The schematic of the synchronized photoreceiver [2] is shown in Fig. 1. The load capacitance C_L is the capacitance of the external pad and package. It is estimated at 5 pF. The post-amplifier of M1-M7 is therefore buffered by two levels of complementary CMOS inverters. The input capacitance of the buffer stage is typically between 50 fF and 100 fF. The local p-n junctions available in CMOS technology are exploited to build vertical p-n-p BJT transistors [2].

Since the base of Q2 is exposed to the light, photo-Darlington current I_D is induced and given by $I_D = (\beta+1)^2 I_{ph}$, where β is the BJT current-gain. This current I_D is reflected back from the photoDarlington and it is mirrored and amplified by M2 in I_{amp}. The current I_{amp} will be compared with a reference bias current by M3-M7 [3]. This results in a return-to-zero (RZ) format. The gate of M7 is connected to the diode-connected M6 to replicate I_{amp} by M7 in I_{rep}. A reference current is established by M3 and M5, and it is mirrored by M4 to establish the threshold current I_{th} and the bias voltage V_{bias}.

The output current is defined as the difference of the two drain currents I_{rep} and I_{th}. The current-mirror comparator provides the two logical output voltages V_{out}: a logical high output voltage for I_{rep} less than I_{th}, and a logical low output voltage for I_{rep} higher than I_{th}. So the stable state of V_{pad} is at 5-V, the injection of pulse of light changes the state of V_{pad} to a digital pulse of 0-V.

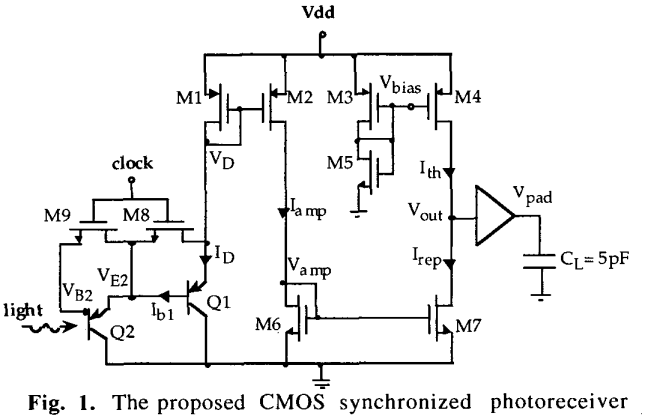

Fig. 1. The proposed CMOS synchronized photoreceiver circuit.

In this 0.7-μm 5-V n-well CMOS technology, $\beta = 22.5$ and the generated photocurrent is rearranged to be reflected in this design by $I_{rep} = 177509\, I_{ph}$.

During measurement, the light pulse delay should take a few ns from the corresponding half-cycle, when clock is at its low state, in case to leave the maximum of time to the photocarrier diffusion current generated in the n-well/substrate photodiode.

The proposed photoreceiver has two new features in its clocked photoDarlington configuration. The first feature is that Q1 and Q2 are controlled by M8 and M9 rather than a classic Darlington structure. This clocked photoDarlington synchronizes the photoreceiver circuit. The second is the pull-up of the base voltage of the phototransistor Q2 junction to auto-reverse its base-collector when the clock is high, instead of the conventionally used phototransistor in [4].

The auto-reverse voltage modulates the n-well/substrate depletion layer [2, 5] and removes the excess charge at the base of Q2 during the first half-cycle, to just reduce the diffusion delay of the generated photocarriers to reach the junction.

II.b. Small-signal analysis

The small signal behavior of the post-amplifier M1-M7 of Fig. 1 is very important to compare the performance of the post-amplifier M1-M7 in the two following cases: (1) when it is loaded by an ideal current source; and (2) when it is loaded by the preamplifier Q1 and Q2.

The small-signal transconductances of M1-M7, and their output conductances are noted g_{mi} and g_{dsi}, respectively, with $i = 1,\ldots 7$. C_{gs}, C_{gd}, and C_{bd} are, respectively, the gate-to-source, -to-drain and substrate-to-drain device capacitances. $g_{m(Qi)}$, $g_{\pi(Qi)}$ and $g_{o(Qi)}$ are, respectively, the small-signal transconductances, input conductances and output conductances, and are indexed by their appropriate bipolar transistors Q1 and Q2.

The use of a symbolic small-signal simulator like ISAAC [6] yields a quite complicated open-loop transfer function

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Table I. The equivalent expression of the simplified parameters of Fig. 2(b) as a function of the device transconductances g_m and conductances g_{ds} of M1-M7, and the capacitance coupling gate-to-source C_{gs}, gate-to-drain C_{gd}, and bulk-to-drain C_{bd} of the output stage M4 and M7.

$$R_{out} = \frac{1}{g_{ds4} + g_{ds7}}, \quad R_0 = \frac{1}{g_{m6} + g_{ds6} + g_{ds2}} \cong \frac{1}{g_{m6}}$$

$$C_0 \cong C_{gs7}, \quad C_{out} = C_{bd7} + C_{bd4} + C_{gd7} + C_L$$

$$\frac{V_0}{V_{in}} = -\frac{g_{m2}}{g_{m6}}, \quad \frac{I_0}{I_{in}} = -\frac{g_{m2}}{g_{m1} + g_{ds1}} \cong -\frac{g_{m2}}{g_{m1}}$$

$$\frac{V_{in}}{I_{in}} \cong \frac{1}{g_{m1}}$$

Table II. Analytical expression of the transfer function characteristics of Fig. 2(b) as a function of g_m, g_{ds} of M1-M7 and C_{gs}, C_{gd}, and C_{bd} of the output stage M4 and M7.

$$\Re_0 = \frac{g_{m2}\, g_{m7}}{g_{m1}\, g_{m6}\,(g_{ds4} + g_{ds7})}$$

$$A = \frac{C_{gs7} + C_{gd7}}{g_{m6}} + \frac{C_{gd7} + C_{gd4} + C_{bd7} + C_{bd4}}{g_{ds4} + g_{ds7}} + \frac{g_{m7}\, C_{gd7}}{g_{m6}\,(g_{ds4} + g_{ds7})}$$

$$B = \frac{C_{gs7}\, C_{gd7} + (C_{gs7} + C_{gd7})(C_{gd4} + C_{bd7} + C_{bd4})}{g_{m6}\,(g_{ds4} + g_{ds7})}$$

$\Re(s) = V_{out}/I_{in}$, with a second-order numerator and a third-order denominator which are too lengthy to be usefully reproduced here. However the complete numerical small-signal analysis and curves generated by ISAAC give a good insight.

II.b.1. Ideal analysis

To achieve analytical relationships between the pole-zeros and the small-signal device parameters: the post-amplifier M1-M7 is presented by a simplified circuit and its small-signal model [7] circuit is shown in Fig. 2. Furthermore, some simplifications introduced in the generated expressions overcome the complexity of the full small-signal equations. The relationship between the parameters shown in Fig. 2(b) and the parameters of the circuit is reveled in table I.

The transimpedance gain $\Re(s)$ can be expressed as follows

$$\Re(s) = \frac{V_{out}}{I_{in}} \cong -\Re_0 \frac{1 - s/z_1}{1 + A\,s + B\,s^2} \tag{1}$$

where $\Re_0$, z_1, A, and B are given in table II as functions of the small-signal device parameters.

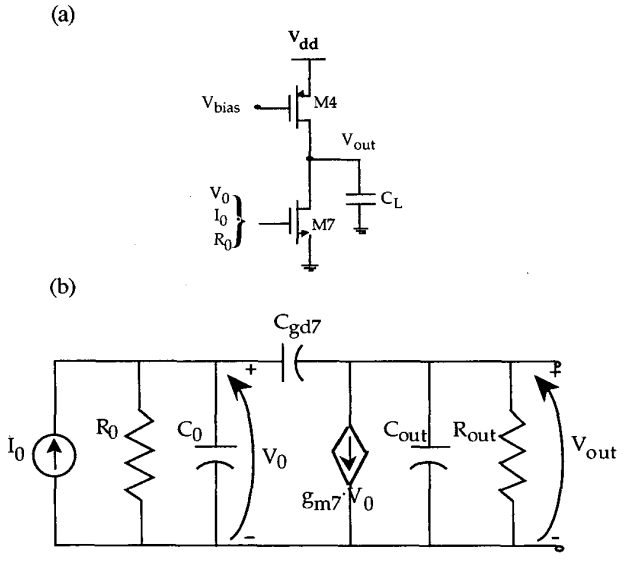

Fig. 2. (a): simplified post-amplifier circuit for small signal analysis. (b): simplified small signal model of the post-amplifier.

The open-loop transfer function $\Re(s)$ allows an easy expressions of the zero z_1 and the two poles p_1 and p_2 of the post-amplifier in these following expressions

$$z_1 = \frac{g_{m7}}{C_{gd7}} \tag{2}$$

$$p_1 = \frac{-1}{A} \cong \frac{-g_{m6}\,(g_{ds4} + g_{ds7})}{g_{m6}\,(C_{gd7} + C_{gd4} + C_{bd7} + C_{bd4} + C_L) + g_{m7}\, C_{gd7}} \tag{3}$$

$$p_2 = \frac{-A}{B} \cong -\frac{g_{m6}\,(C_{gd7} + C_{gd4} + C_{bd7} + C_{bd4} + C_L) + g_{m7}\, C_{gd7}}{C_{gs7}\, C_{gd7} + (C_{gs7} + C_{gd7})(C_{gd4} + C_{bd7} + C_{bd4} + C_L)} \tag{4}$$

The zero z_1 occurs in the right half-plane due to the feed-forward path through C_{gd7}. The pole p_1 is more dominant than p_2 as they are expressed as the typical ratio of g_{ds}/C and g_m/C, respectively, and g_m is always larger than of g_{ds}. The numerical analysis of the comparator in 0.7-µm 5-V n-well CMOS technology is done by ISAAC and is depicted in Fig. 3.

The transimpedance gain at low frequency $\Re_0$ is about 162 dBΩ. The first pole of the post-amplifier with a capacitive load $C_L = 1$ pF is located at 1 KHz, the second pole is located at 2 MHz. The phase of the open-loop transimpedance gain of the post-amplifier amounts to 42° at the cut off frequency of 100 MHz.

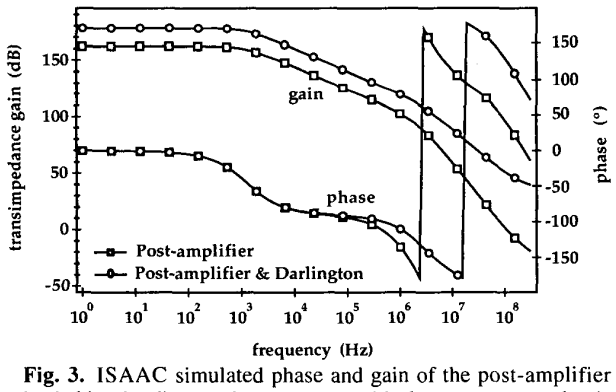

Fig. 3. ISAAC simulated phase and gain of the post-amplifier leaded by the discussed two cases: an ideal current source that is presented by the square marks; and (Q1, Q2) Darlington that is presented by the circle marks.

II.b.2. Entire analysis

The post-amplifier M1-M7 is loaded by a p-n-p Common-Collector-Common-Collector cascade (Q1, Q2) Darlington configuration by replacing V_{in} and I_{in} by V_D and I_D, respectively. Since the characteristics of the circuit change due to the input impedance of the post-amplifier is now the equivalent output impedance of the (Q1, Q2) Darlington. This output impedance can be approximated by $1/g_{m(Q1)}$ which is in parallel with $1/g_{m1}$. The approximation is done by assuming that the small-signal output resistance of the common collector configuration goes to infinity and then $g_{o(Q1)}$ and $g_{o(Q2)}$ are kept to zero [8].

The output stage M4 and M7 is driven from a lower equivalent resistance at the gate of M7 but does not have any effect on the performance of the circuit. Hence M7 is driven from the low resistance source of about $1/g_{m6}$. Consequently, there is no change in the location of the pole-zeros of the circuit. The voltage gain of (Q1, Q2) is close to unity by the low load impedance, $1/g_{m1}$. Hence the post-amplifier is driven by the emitter current of Q1 which is $(\beta+1)^2 I_{b2}$, where I_{b2} is the input base current of Q2.

The ratio I_0/I_{in} expressed in table I, becomes the ratio of I_0 by I_{b2} and is expressed by

$$\frac{I_0}{I_{b2}} = -g_{m2}\left(\frac{g_{m(Q2)}}{g_{\pi(Q1)}\, g_{\pi(Q2)}}\right) \tag{5}$$

Consequently, $\Re_0$ raises and is given by

$$\Re_0 \cong \frac{g_{m(Q1)}\, g_{m2}\, g_{m7}}{g_{\pi(Q1)}\, g_{\pi(Q2)}\, g_{m6}\left(g_{ds4} + g_{ds7}\right)} \tag{6}$$

The numerical analysis of the comparator loaded by the (Q1, Q2) Darlington in 0.7-µm 5-V n-well CMOS technology is also done by ISAAC and depicted in Fig. 3. The transimpedance gain at low frequency is increased up to 178 dBΩ. The locations of p_1 and p_2 are kept without change. At 100 MHz, the phase of the open-loop transimpedance gain of this circuit amounts to 129° with gain of 51 dB as shown in Fig. 3. Thus the performance of the proposed post-amplifier is not degraded when it is loaded by the (Q1, Q2) Darlington.

Since the gates of M8 and M9 are connected to an external large signal clock, the addition of these transistors to the previous circuit does not make any significant change as M8 and M9 contribute solely with their drain-source impedances r_{ds8} and r_{ds9}, respectively. These are seen in parallel with smaller $r_{\pi(Q1)}$ and $r_{\pi(Q2)}$ of Q1 and Q2, respectively. Hence, the small-signal analysis performed earlier of the post-amplifier loaded by (Q1, Q2) Darlington does not change by adding M8 and M9 to the circuit. This is confirmed by ISAAC.

II.c. Noise switching circuit effects

As demonstrated in the previous description, a switching circuit (M8, M9) is needed to connect V_{B2} to a reverse voltage for refreshing after injection phase. It increases the maximum operation frequency significantly. This electrical switching circuit however causes electrical noise and large parasitic capacitance effects. The electrical noise degrades the photoreceiver performances in sensitivity and operating frequency.

Since there is no gain in the refresh circuit (M8, M9), thermal noise will play a very important role in the stability of the base signals. When a clock is applied to the base-collector capacitors C_{bc1} and C_{bc2} of Q1 and Q2, respectively, they are seen in parallel. Their top plates are charged to the base voltage and their bottom plates are connected to the collector voltage. These capacitances introduce a KT/C thermal noise which limits the bandwidth of the circuit.

The sampled switched-gate noise contributes $\sqrt{KT/C_{//}} \cong 64.4$ µV rms at room temperature and a noise density of 6.44 nV/$\sqrt{\text{Hz}}$ for a bandwidth above 100 MHz, where $C_{//}$ is the equivalent capacitance of the parallel connection of C_{bc1} and C_{bc2}.

As a consequence to the noise discussed above and the clock feedthrough in [2], a switched-current circuit [9] seems to be a good candidate for the reduction of the switching noise and will replace M1 in the next version of this photoreceiver circuit in the future.

III. EXPERIMENTAL RESULTS

The circuit proposed in Fig. 1 was designed and fabricated in a 0.7-µm 5-V n-well CMOS technology. Fig. 4 shows the photograph of the synchronized photoreceiver under test. Measurement with well area A_{B2} of 60×60 µm^2 and under a dark laboratory environment result in a dark-current of about 154 pA, using an *hp*_4145B semiconductor parameter analyzer.

The photoreceiver occupies an effective area of only 100×60 µm^2 (the output buffer and pads are not included). During the experiments, V_{bias} is held at 0-V, the clock swings from 0 to 5-V, and the light input was given as 5-ns pulses of 830-nm laser diodes.

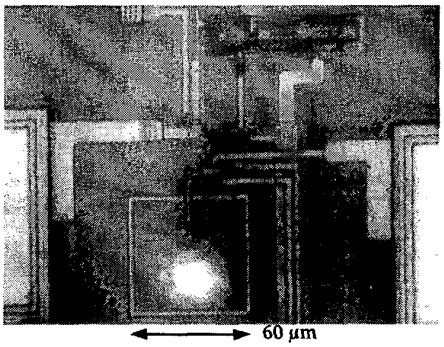

Fig. 4. Photograph of the dynamic photoreceiver under test. The white spot in the bottom of the figure defines the injected input light into the enlarged base area $A_{B2} = 60\times60\,\mu m^2$ of Q2.

The photoreceiver's dynamic range of optical power is as wide as 40 dB at a bit-rate of 100 Kb/s. The minimum detectable external optical energy level was 135 aJ (-45.7 dBm/beam) at this frequency, as shown in Fig. 5. We assume a detector responsivity of 0.5 A/W by considering that 25 % of the given 830-nm laser is reflected [10], which means that only 423 electrons generated in the diode n-well-substrate of Q2 are required for changing the output state. This corresponds to $I_{ph} = 13.6$ nA minimum photocurrent generated and $I_{rep} = 1.696$ mA reflected current. The fall time of the generated signal V_{amp} is $\Delta t = 0.56$ ns which is derived from $i = C(dV/dt)$ calculations.

The photoreceiver performances in input-light dynamic range and maximum operating frequency are measured and

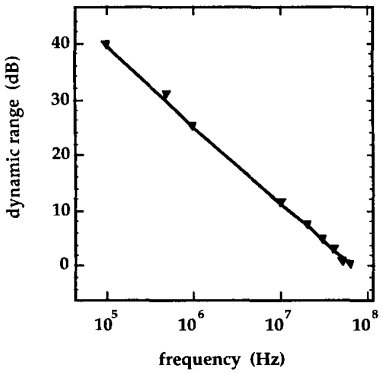

Fig. 5. Measured dynamic range of the photoreceiver with the injection of 830-nm laser diodes.

plotted in Fig. 5 and Fig. 6, respectively, using a package of a large cavity and 40-pins.

The decrease in dynamic range at high frequencies is due to the accumulation of the photoelectrons in the substrate, which escape the refreshing phase when the clock is high [2]: the large absorption length of about $L_n = 10\,\mu m$ [11] for the given wavelength of 830-nm input laser and the total depth of the affected silicon by light $L_D = 4.6\,L_n$ [5] result in a considerable sweep-out time. So the use of 460-nm blue laser diodes [12, 13] should reduce the penetration depth by one order of magnitude and decrease the photocarrier density in the substrate [14]. Thus the dynamic range should be held at about 40 dB as it is the case at low frequencies.

High operating frequency was measured for this first version of CMOS photoreceiver at 100 MHz. The optical input was given, repetitively, to the base of Q2 in the order '000101011111'. '0' means that no light was injected during the appropriate half clock period, and '1' means that an optical input pulse of light was injected during the appropriate half clock period. The output V_{pad} in its R Z format is shown in Fig. 6. An optical input of 1-ns pulses, 830-nm laser diode is used. These short laser pulses are able to generate photocurrent pulses of 5-ns [2]. Hence the photoreceiver is improved in a higher operating frequency. We measured 13.3 fJ external pulse energy at 100 MHz, or -18.8 dBm/beam external power. The output pattern shown in Fig. 6 matches perfectly the repetitive string of the optical input pulses described previously.

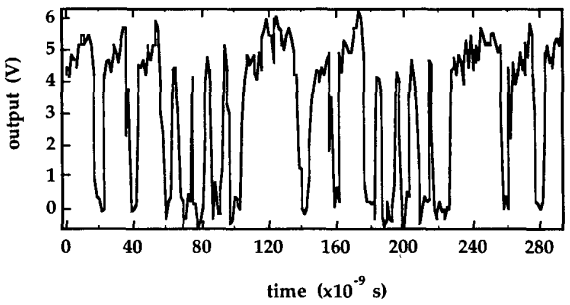

Fig. 6. Improvement of 100 MHz maximum frequency of the photoreceiver by injecting 1-ns pulses of 830-nm laser diodes.

IV. CONCLUSION

We have established a strategy for the conception of an original monolithic CMOS photoreceiver. This strategy is based on the use of the inexpensive CMOS technology for sensing and digitizing optical input pulses. The CMOS photoreceiver is refreshed after each injection of light to avoid the accumulation of the deeply generated photoelectrons in the substrate. Our photoreceiver is designed in standard 0.7-μm 5-V n-well CMOS technology with an effective area of $100 \times 60\,\mu m^2$. The maximum frequency achieved for the demonstrated photoreceiver is 100 MHz with only 13.3 fJ/pulse external light energy of 830-nm wavelength.

The detailed conception of CMOS photoreceiver should play a significant role in the evolution of the state-of-the-art monolithic lightwave receiver, because the realization of a high-speed photoreceiver in CMOS technology offers the possibility to incorporate the sensor and the processing circuitry in a single IC.

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