# Conduction Losses and Common Mode EMI Analysis on Bridgeless Power Factor Correction

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# Conduction Losses and Common Mode EMI Analysis on Bridgeless Power Factor Correction

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***Abstract*—In this paper, a review of Bridgeless Boost power factor correction (PFC) converters is presented at first. Performance comparison on conduction losses and common mode electromagnetic interference (EMI) are analyzed between conventional Boost PFC converter and members of Bridgeless PFC family. Experiment results are given to validate the efficiency analysis and EMI model building.**

***Keywords-conduction losses; EMI; bridgeless; power factor correction (PFC)***

## I. INTRODUCTION

With demands on improving electromagnetic compatibility and reducing loss in power supplies in industrial applications, research on maximizing power transmission turns out to have significant impact. Innovation and optimization of power factor correction (PFC) technology would be an important method to achieve higher efficiency and low electromagnetic interference (EMI) power supplies.

Traditional Boost PFC in Fig. 1 cannot avoid some natural power loss because of the drawbacks of their structures with full-wave rectifier in the input. Recently, a new PFC family called Bridgeless PFC (BLPFC) family has been proposed to realize high efficiency PFC converters by more or less eliminating the ac rectifier of traditional Boost PFC [1~3]. However, whether all the members belonging to BLPFC family have high efficiency is doubtful, besides many researchers have shown that some of the BLPFC topologies have bad EMI performance due to their circuit structures [4~5].

In this paper, a systematic review of BLPFC family is presented; conduction losses and common mode (CM) EMI performances are analyzed comparing with conventional Boost PFC. Simulation and experiment results shows that low EMI and high efficiency PFC can be realized by a certain BLPFC topology.

## II. REVIEW OF BRIDGELESS BOOST PFC CONVERTERS

### *A. Five Bridgeless Boost PFC Topologies for Comparison*

Five different type of BLPFC topologies are discussed in this section. The basic one in Fig. 2, called Dual Boost PFC, which has been shown to have higher efficiency than conventional Boost PFC in Fig. 1, because of the reduced semiconductor numbers in line current path [6]. However, this

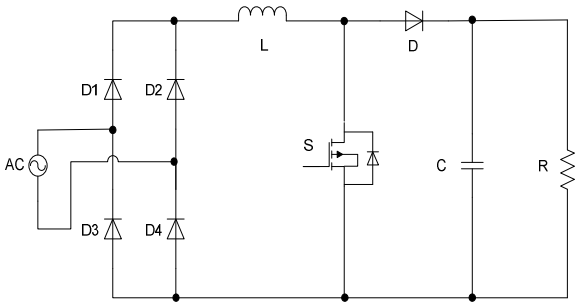



Figure 1. Conventional Boost PFC

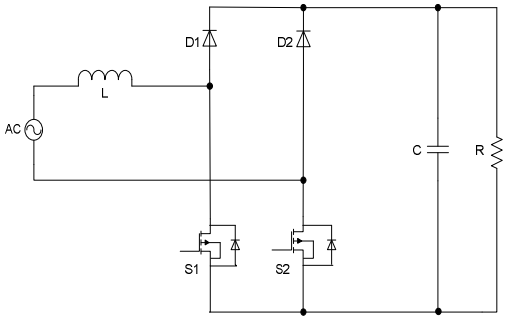



Figure 2. Dual Boost PFC

PFC rectifier has significantly larger CM noise than the conventional Boost PFC. The reason is that: in the conventional boost PFC, the output ground is always connected to the ac source through full-bridge rectifier, whereas, in the Dual Boost PFC, the output ground is connected to the ac source only during positive half-line cycle through the body diode of switches. So large pulse current from high frequency switches will flow through parasitic capacitors and brings EMI problems.

Fig. 3 is a Bidirectional Switches BLPFC [7] using two additional fast diodes. This leads to increase conduction losses of the circuit. Because in the negative half-line period, in traditional Boost PFC, there is only one high frequency diode and two low frequency diodes conducting, but in Fig. 3, there are two high frequency diodes conducting together.

In Fig. 4, there are two Boost circuits in the BLPFC [8~9]. One can expect higher efficiency than Boost PFC with the same reason as Dual Boost PFC. And its EMI will be lower than Boost PFC, because not only the low frequency diodes D3 and D4 connect the output ground to the ac source but the symmetric Boost inductors operate as a CM filter which can be expected to achieve higher CM EMI reduction.

Fig. 5 is called Pseudo Totem-pole BLPFC, because of the position of switches [10]. This topology also has only 2 semiconductors in series on its current path no matter the MOSFET is on or off. So it has the same benefit in conduction losses reduction as which in Fig. 2 and Fig. 4.

Finally, Fig. 6 shows a modification of the basic BLPFC Boost rectifier from Fig. 2, which is obtained by exchanging the position of the diode and switch in Fig. 2.

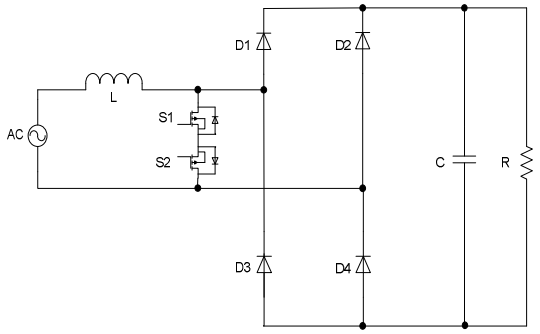



Figure 3. Bidirectional Switches Boost PFC

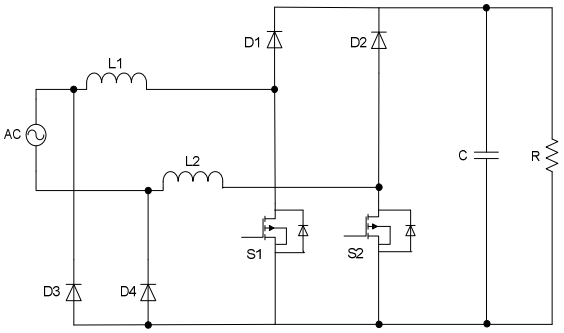



Figure 4. Two-boost-circuit PFC

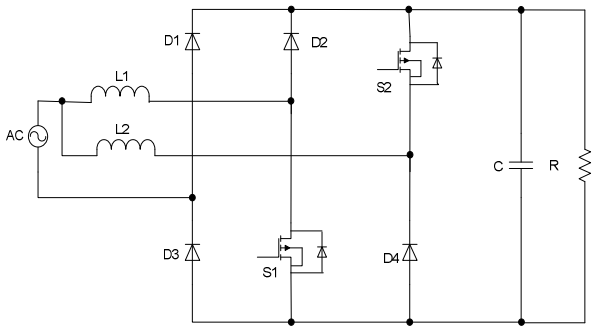



Figure 5. Pseudo Totem-pole PFC

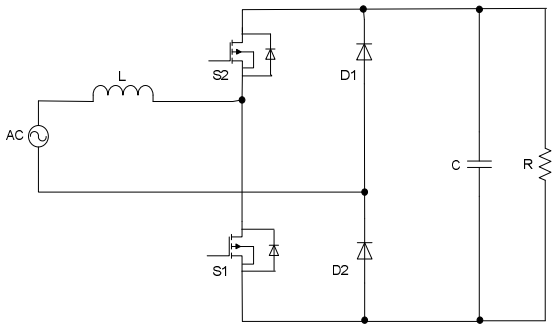



Figure 6. Totem-pole PFC

## B. *Conduction Losses Calculation*

It is well known that what dominate the power loss in PFC converters are semiconductor losses. Table 1 gives the semiconductor numbers in current flow path of each PFC topology during line positive ac period. Where, On/Off means on time and off time of MOSFET; $D_F$ symbolizes fast diode; $D_L$ symbolizes line frequency diode; M is for MOSFET and $D_M$ is the body diode of MOSFET. It shows that the BLPFCs respectively have lower semiconductor numbers comparing with conventional Boost PFC, which will bring benefits on decreasing conduction losses of the whole systems.

For making a fair comparison, all the MOSFETs of different PFC topologies operated in hard switching condition.

The simulation parameters are choosing as below:

$P_o = 3.5\,kW$ ; $V_o = 400\ V_{dc}$ ; $V_{in} = 85 \sim 265\ V_{ac}$ ; the

TABLE I. SEMICONDUCTOR NUMBERS IN CURRENT FLOW PATH IN THE SIX PFC TOPOLOGIES

| PFC topology | On/Off | $D_F$ | $D_L$ | M | $D_M$ | Total Number |
|---|---|---|---|---|---|---|
| Boost PFC | On | 0 | 2 | 1 | 0 | 3 |
| | Off | 1 | | 0 | | |
| Dual Boost PFC | On | 0 | 0 | 1 | 1 | 2 |
| | Off | 1 | | 0 | | |
| Bidirectional Switches PFC | On | 0 | 0 | 1 | 1 | 2 |
| | Off | 2 | | 0 | 0 | |
| Two-boost–circuit PFC | On | 0 | 1 | 1 | 0 | 2 |
| | Off | 1 | | 0 | | |
| Pseudo Totem-pole PFC | On | 0 | 1 | 1 | 0 | 2 |
| | Off | 1 | | 0 | | |
| Totem-pole | On | 0 | 1 | 1 | 0 | 2 |
| | Off | | | 0 | 1 | |

Boost inductor $L = 3mH$ ; MOSFET: STW45NM50; Fast Diodes: RHRP-3060.

Fig. 7 shows the efficiency columns of six PFC topologies based on simulation results when only the conduction losses are taken into account. Totem-pole PFC in Fig. 6, Two-boost-circuit PFC in Fig. 4 and Pseudo Totem-pole in Fig. 5 has better efficiency comparing with other topologies. These are according with what has been discussed theoretically in part A and which are shown in Table 1. It should be noticed that Fig. 3 may not be a high efficient topology without choosing circuit components carefully, because it has two fast diodes working together when the MOS is off.

Fig. 8 shows the voltage waveforms between power ground and the neutral of ac source from Fig. 1 to 6 during one ac period. Since the CM noise is induced by the internal noise voltage between the ground reference point and the cable connection, which mostly comes from the high frequency switch operation of the PFC converter [11]. Therefore, this figure shows the possible CM EMI problems in the six PFC topologies, because in this way, we consider the neutral as a ground reference and take the power ground as the cable connection point. And it is not only easy to find out that traditional Boost PFC in Fig. 1 and the BLPFC topologies in Fig. 4 and 5 all have lower EMI comparing with other PFC topologies, because of there is no pulse voltage in their waveforms during line negative period; but also easy to get that BLPFC in Fig. 5 has worse EMI than Boost PFC in Fig. 1 and BLPFC in Fig. 4, since its quasi-square wave will bring lots of high frequency noise components, which may decrease its EMI performance. It should be noticed that although there is no pulse voltage show in Fig. 8(f), this does not mean the Totem-pole Bridgeless PFC has better EMI performance. That's because during the line negative period, the boost inductor will bring lots of switching frequency pulses between power ground and the line, which will cause serious EMI problem, too.

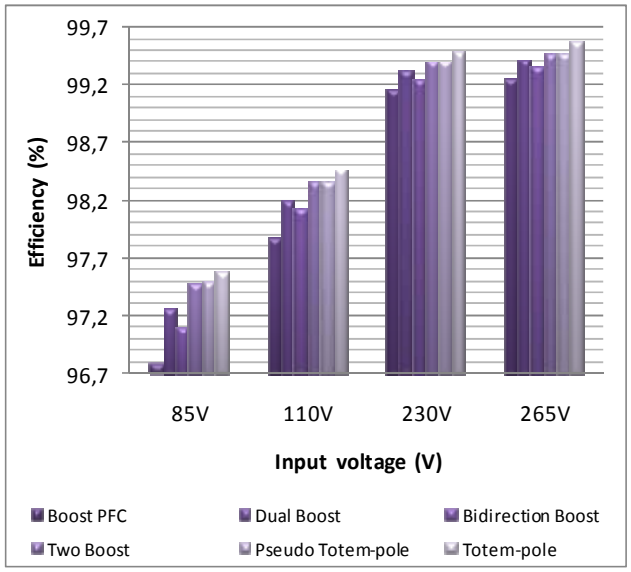


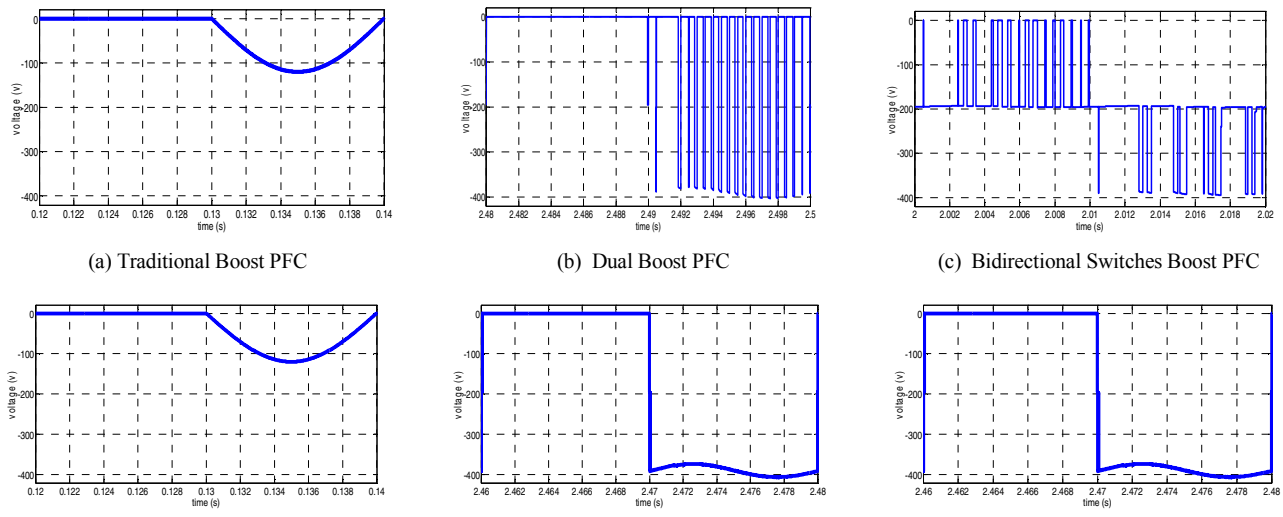

Figure 7. Efficiency comparison only for conduction losses among six PFC topologies based on simulation.

Through Fig. 7 and 8, in order to remain the same CM EMI performance as traditional Boost PFC, it can be concluded that only BLPFCs in Figs. 4 and 5 are needed to be further considered. In next sections, Two-boost-circuit BLPFC in Fig.4 is selected for EMI model building and further discussion, for its high efficiency and low EMI comparing with other BLPFCs. Furthermore, its gate drives are referenced to ground and easier to realize for industrial application.

## III. EMI Model Building and CM Noise Analysis

### *A. EMI Model Building*

If we take the Boost PFC as a noise source and consider the ac source as a load, it was proved that the EMI model of the Boost PFC converter equals to a high frequency pulse source [12]. In order to make a precise EMI analysis of BLPFC family, the EMI model is needed to be built. Take Two-boost-




(a) Traditional Boost PFC (b) Dual Boost PFC (c) Bidirectional Switches Boost PFC

(d) Two-boost-circuit PFC (e) Pseudo totem-pole PFC (f) Totem-pole PFC

Figure 8. CM voltage waveforms between power ground and the neutral of ac source showing the EMI comparison among the six PFC topologies

circuit PFC as an example; since it's a symmetrical circuit for both positive and negative part of ac source, we only consider the positive ac period. Ignore the limited noise current flows through the body diode of S2 and L2 [13], analysis of generate the EMI model of the topology is showed in Fig. 9.

- Step 1: Using the symmetrical operation structure to simplify the topology.
- Step 2: Because the output filter capacitor can be considered as a short circuit in high frequency, and the boost inductor can be considered as an open circuit, these two components can be ignored.
- Step 3: Simplify the semiconductor components. In high frequency domain, the fast diode can be simplified as a capacitor and the MOSFET can be considered as a pulse source.
- Step 4: Deduction of circuit using Thevenin's Theory.

As the result, the Two-boost-circuit BLPFC in the positive ac source can be equal to a pulse voltage source Veq in series with a capacitor Ceq.

$$Veq = -Vds \times C_{S1} \times C_{eq}^{-1} \tag{1}$$

$$C_{eq} = C_{S1} + C_{S2} + C_b \tag{2}$$

Where, $C_{S1}$ and $C_{S2}$ are the parasitic capacitances of MOSFETs, $C_b$ is the capacitance between output ground and the power earth. Normally, $C_b$ is 10 to 20 times bigger than $C_{S1}$ and $C_{S2}$ [14], so if there is any pulses voltage across it, it will bring a significant extra CM current flow through it and lead to CM EMI problems. However, from (1) and Fig. 9(c), one can find that $C_b$ is connected directly between the source of the MOS (which connected to the neutral) and the earth. This will cause no pulses voltage draw on $C_b$, therefore the CM current of the circuit will be reduced.

EMI model of this topology in the negative period of ac source is the almost the same as the former one in (1), but:

$$Veq = -Vds \times C_{S2} \times C_{eq}^{-1} \tag{3}$$

Assuming $C_{S1} = C_{S2} = C_S$, the EMI model for the whole ac period can be written as:

$$Veq = -Vds \times C_S \times C_{eq}^{-1} \tag{4}$$

$$Ieq = -Vds \times \omega C_S \tag{5}$$

Equation (4) shows that although the switching operation generates high frequency pulses inside the Two-boost-circuit PFC, they will not impact the voltage waveform between power ground and neutral. Because of the line frequency return diodes D3 and D4 in Fig. 4, the power ground is connected to the neutral for the whole ac period and all the pluses voltages go into the earth through the parasitic capacitances $C_S$ of the MOS, which gives a continuous and smooth waveform between power ground and the neutral, just like what has been shown in Fig. 8(d). Equation (5) shows that the CM current will only flow through the parasitic capacitance of MOS.

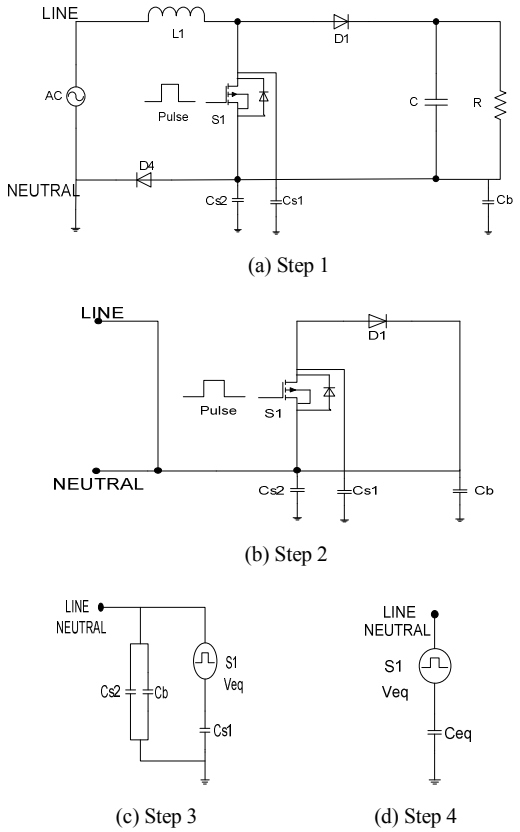



Figure 9. EMI model building for two-boost-circuit PFC

Using the same way to analysis, all the EMI models among Figs. 1 to 6 can be calculated mathematically.

### *B. CM Noise Analysis*

CM noise is a very important issue, which not only affects the design of EMI filter but also influences the stability of the circuit. Fig. 8 shows that traditional Boost PFC, Tow-boost-circuit PFC and Pseudo totem-pole PFC have lower EMI comparing with other PFC topologies. Dual Boost PFC and Totem-pole PFC have higher EMI in line negative period because the neutral is separated from output ground by the

TABLE II. EMC AND EFFICIENCY COMPARISON AMONG SIX PFC TOPOLOGIES

| PFC topology | Efficiency Rank | CM Voltage Rank | CM Current Rank |
|---|---|---|---|
| Boost PFC | 6 | 1 | 1 |
| Dual Boost PFC | 4 | 5 | 5 |
| Bidirectional Switches PFC | 5 | 5 | 5 |
| Two-boost–circuit PFC | 2 | 1 | 1 |
| Pseudo Totem-pole PFC | | 3 | 3 |
| Totem-pole | 1 | 3 | 3 |

boost inductor, which will require larger EMI filter to meet the EMC standard. Obviously, Dual boost PFC and Totem-pole PFC are not suitable for industrial application without improvement. Especially in Dual boost and Totem-pole PFC, because $C_b$ is connected between the drain of the MOS and the earth and its impedance is too small, it will increase the CM current and a part of it will flow through control circuit by stray capacitor connected between MOSFET and control loop. This will lead an unstable factor to the whole system and bring problems in converter design [15].

Table 2 gives the CM EMC and efficiency comparison among conventional Boost PFC and five BLPFCs. From this table, it comes to a conclusion that the Two-boost-circuit PFC shows higher efficiency and lower EMI performances, which is worth for industrial application and further improvement.

## IV. EXPERIMENT RESULTS

The performance comparison of the Boost PFC and Two-boost-circuit PFC shown in Fig. 1 and 4, was evaluated on the same prototype hardware, which is a 65kHz switching frequency, 350W output power circuit operating from a universal ac-line input (85~260Vrms ) and delivering up to 0.9A at 390V output. The schematics of both PFCs are shown in Fig. 10 and 11. Since the drain voltage of boost switches is clamped to bulk capacitor, the peak voltage stress on each boost switch is approximately 390V. The peak current stress on boost switches, which occurs at full-load and low line, is approximately 5.4A. Therefore, SPW47N60C3 MOSEFET from Infineon was used for each PFC converter. Boost diodes were implemented with IDT04S60C SiC diode from Infineon, and two diodes of bridge rectifier in traditional PFC, 1N5406 from Multicomp, were used as the return diodes D3 and D4 in two-boost-circuit PFC. The cores of the boost inductors $L$ are 77083-A7 (high flux Kool-Mμ core from Magnetics. A magnet wire (AWG#19) was used for each winding. Finally, two high voltage aluminum capacitors (270$\mu$F, 400VDC) were used for bulk capacitor.

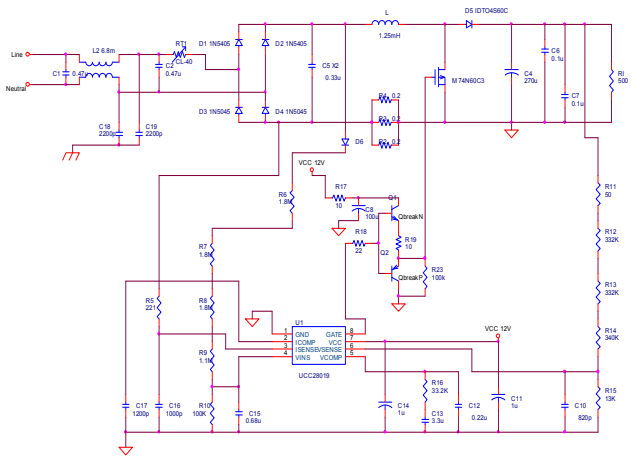


Figure 10. Schematic of conventional Boost PFC

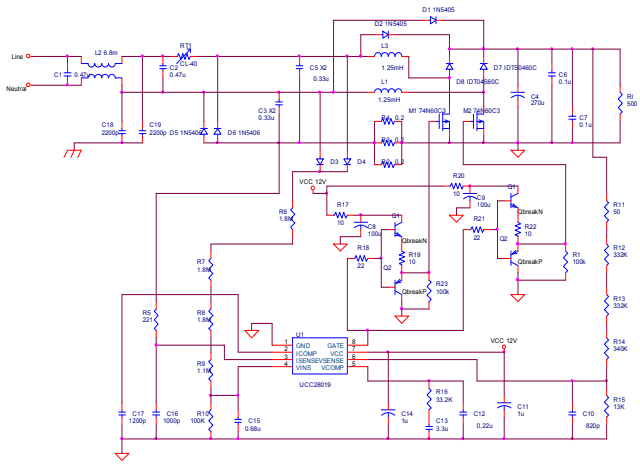


Figure 11. Schematic of Two-boost-circuit PFC

UCC28019 (an eight-pin continuous-conduction-mode PFC controller) from Texas Instrument was used in the experimental prototype circuit because it does not require line voltage sensing. It should be noted that switches S1 and S2 in both Dual Boost and Two-circuit-boost PFC are operated simultaneously by the same gate signal from the controller. Although both switches are always gated, only one switch, on which the positive input voltage is induced, carries positive current and delivers the power to the output. The other switch, on which the negative input voltage is induced, does not influence the operation since its body diode conducts.

To compare the efficiency of the two PFC converters fairly, two SPW47N60C3 MOSEFETs connected in parallel were used as boost switch, while two IDT04S60C SiC diodes connected in parallel were used as boost diode in conventional Boost PFC. A full-bridge rectifier built with four 1N5406 from Multicomp was used as an input-bridge rectifier.

Fig. 12 shows the measured efficiency of the traditional Boost PFC (dashed line) and the Two-boost-circuit PFC (solid line) as functions of the output power, when the ac input is 85V. As can be seen in Fig. 10, the bridgeless rectifiers have higher conversion efficiency than the conventional Boost PFC rectifier over the entire measured power range. Fig. 13 shows the simulation results of conduction losses and percent of output power comparison between Boost PFC and Two-boost-circuit PFC at 85 Vac input and 350W power level. The simulation result shows one can gain 1.22% efficiency improvement with Two-boost-circuit PFC, which is almost according with the measurement results 1.58% in Fig. 12. The small difference may come from the switching losses (since we use two MOSs

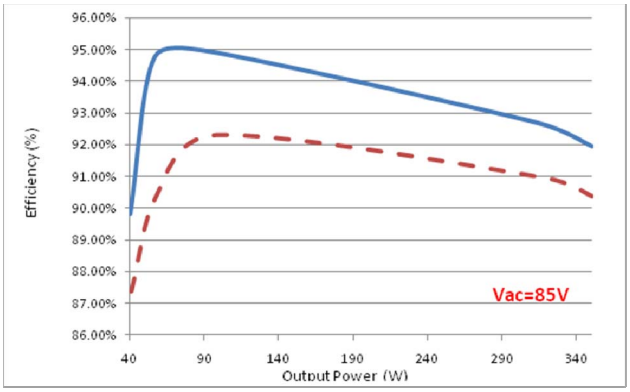



Figure 12. Efficiencies measurement at 85Vac input of conventional Boost PFC (dashed line) and Two-boost-circuit PFC rectifier (solid line) as functions of output power.

parallel in Boost PFC） and the inductor loss.

Fig. 14 and 15 show the measured peak and average EMI of the conventional Boost PFC and the Two-boost-circuit PFC with the same EMI input filter respectively. As it can be seen from Fig. 14 the measured EMI value of the Boost PFC cannot satisfy the EN55022 requirements over the frequency range from 436kHz to 1.2MHz in low frequency domain. But can be seen from Fig. 15, the Two-boost-circuit PFC exhibits EMI reduction over the entire measured frequency range. Specifically, the measured peak EMI shows more than 10dB≤ V margin from the requirements over the entire frequency range below 3MHz. This is because the two boost inductors in Two-boost-circuit PFC operate as a CM filter and reduce the CM noise.

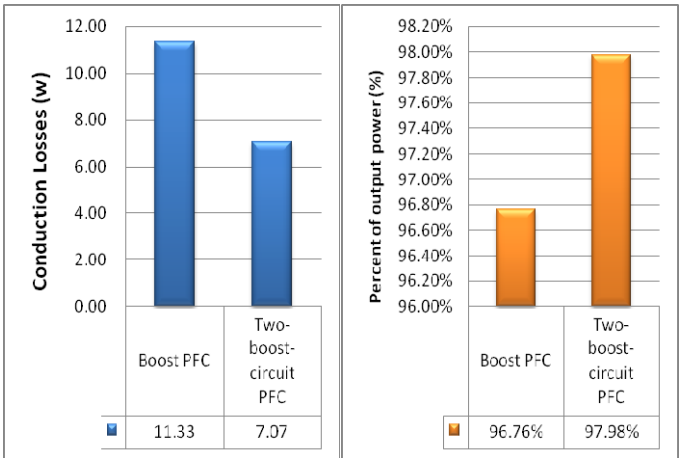



Figure 13. Simulation results of conduction losses and percent of output power at 85Vac input and 350W. Conduction losses (blue), percent of output power (orange).

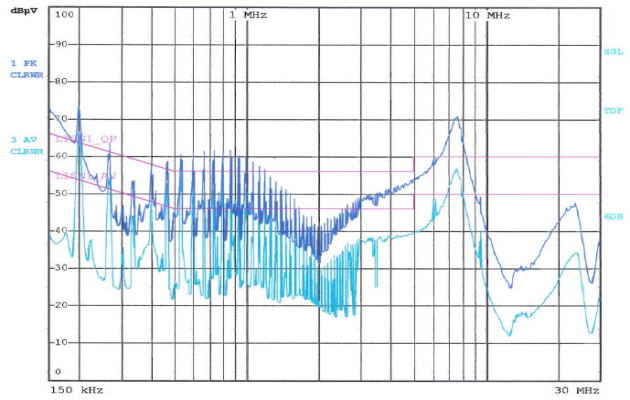



Figure 14. EMI measurement of conventional Boost PFC.

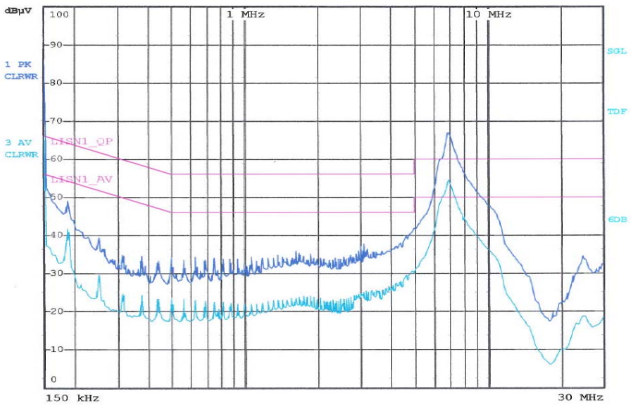



Figure 15. EMI measurement of Two-boost-circuit PFC.

## V. CONCLSION

In this paper, a review of Bridgeless Boost power factor correction (BLPFC) converters is presented. Performance comparison, including conduction losses analysis and common mode electromagnetic interference (EMI) argumentation, is analyzed between traditional Boost PFC converter and six members of Bridgeless PFC family. The simulation and experiment results show the advantages and disadvantages of all the Bridgeless PFC topologies clearly. It also shows the valid Bridgeless PFC topologies for industrial application.

## REFERENCES

[1] Jee-Woo Lim and Bong Hwart-Kwon, "A power-factor controller for Single-Stage PWM rectifiers," *IEEE* Trans. *Ind. Electron.,* vol. 46, pp. 1035-1037, Oct. 1999.

[2] Alexandre Ferrari de Souza and IYO Barbi,"'A new ZVS semiresonant high power factor rectifier with reduced conduction losses," *IEEE Tram. Ind. Electron.,* vol. 46. pp. 82-91), Feb. 1999.

[3] Ugo Monconi, I' A bridgeless PFC configuration based on L4981 PFC controller," *STMicroelecrronics Applicarion Noles,* AN1606, Nov. 2002.

[4] P. Kong, S.Wang, and F. C. Lee, "Common mode EMI noise suppression in bridgeless boost PFC converter," in *Proc. CPES Power Electronics Conf.*, Apr. 2006, pp. 65–70.

[5] H. Ye, Z. Yang, J. Dai, C. Yan, X. Xin, and J. Ying, "Common mode noise modeling and analysis of dual boost PFC circuit," in *Proc. Int. Telecommunication Energy Conf.*, Sep. 2004, pp. 575–582.

[6] P. N. Enjeti and R. Martinez, "A high performance single phase AC to DC rectifier with input power factor correction," in *Proc. IEEE Applied Power Electronics Conf.*, Mar. 1993, pp. 190–195.

[7] J. C. Salmon, "Circuit topologies for PWM boost rectifiers operated from 1-phase and 3-phase ac supplies and using either single or split dc rail voltage outputs," in *Proc. IEEE Applied Power Electronics Conf.*, Mar. 1995, pp. 473–479.

[8] A. F. Souza and I. Barbi, "High power factor rectifier with reduced conduction and commutation losses," in *Proc. Int. Telecommunication Energy Conf.*, Jun. 1999, pp. 8.1.1–8.1.5.

[9] T. Ernö and M. Frisch, "Second generation of PFC solutions," in *Proc. Power Electronics Europe*, 2004, no. 7, pp. 33–35.

[10] J. Liu, W. Chen, J. Zhang, D. Xu, and F. C. Lee, "Evaluation of power losses in different CCM mode single-phase boost PFC converters via simulation tool," in *Rec. IEEE Industry Applications Conf.*, Sep. 2001, pp. 2455–2459.

[11] Tim. Williams, "EMC for product designers," in press. Newnes, 2001.

[12] H. Ye, Z. Yang, J. Dai, C. Yan, X. Xin, and J. Ying, "Common mode noise modeling and analysis of dual boost PFC circuit," in Proc. Int. Telecommunication Energy Conf., Sep. 2004, pp. 575-582.

[13] Huber L, Yungtaek Jang, etc. "Performance evaluation of Bridgeless PFC Boost rectifiers" in: *IEEE Transactions on Power Electronics*, 2008, 23(3), pp. 1381-1390.

[14] Pengju Kong, Shuo Wang, etc. "Common mode EMI noise suppression for bridgeless PFC converters" in*: IEEE Transactions on Power Electronics*, 2008, 23(1), pp. 291-297.

[15] Yungtaek Jang, Milan M. Jovanovic. "A bridgeless PFC boost rectifier with optimized Magnetic Utilization" in: *IEEE Transactions on Power Electronics*, 2009, 24(1), pp. 85-93.