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Wireless and Photonic High-Speed Communication Technologies, Circuits and Design Tools

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***Abstract* — Wireless and Ethernet communications aim at millimeter-wave frequency operation and gigabit-per-second data transmission. Increased data rates in wireless systems can only be achieved at frequencies beyond 60 GHz or 80 GHz and in 100 Gbit/s (100-G) data transmission over fibre. Both systems are fundamental to emerging consumer and professional applications. These systems start to emerge as near future applications and are subject of ongoing research activities in Europe, for example within the EU FP6 GIBON project. Wireless systems with over 100 GHz carriers as well as first over 100-G fibre systems were reported. These communication systems present new challenges for circuit designers. The presentation will be devoted to technologies and various aspects of circuit design for 100 G applications. We will present overview on wired and wireless systems demonstrating the challenges of this research including design challenges, relevant trade-offs and the present bottlenecks. Different system architectures will be presented with their impact on component requirements. Similarities and differences of wired and wireless applications will be pointed out. Design methodologies, necessary tools and circuit performances obtained in various technologies (Si, SiGe, GaAs and InP) will be presented and discussed. Finally, modeling, measurements and packaging problems at such high frequencies/speeds will be also addressed.**

Keywords -

I. INTRODUCTION

The demand for high data rate has triggered major research and development efforts in the area of high speed components and systems. It has been predicted by Cisco & Gardner that the global Internet traffic will reach 11200 Gbit/s in the year 2011/2012. It is also believed that the best candidate to support this high data volume will be IP over Ethernet.

The technology envisaged to support this development is based either on optoelectronic data transmission over fiber or electronic wireless transmission. In both cases, spectral efficiency at a high-speed data rate is of outmost importance. The envisaged spectral efficiency is 2 bit/s/Hz, which would result in a 10 Gbit/s data transfer over a 5 GHz bandwidth channel. Such wide spectral windows are attainable only at millimeter-wave (mm-wave) frequencies or with optical fibre systems. One can show that the Shannon channel capacity for wireless data transmission over < 5 km increases at mm-waves from 2 Gbit/s around 24 GHz, to 10 Gbit/s at E-band and reaches a maximum of 20 Gbit/s in the 200 GHz to 300 GHz band. On the other hand, next generation optical system standard is considered to operate at 100 Gbit/s [1],[2], as depicted in Fig. 1.

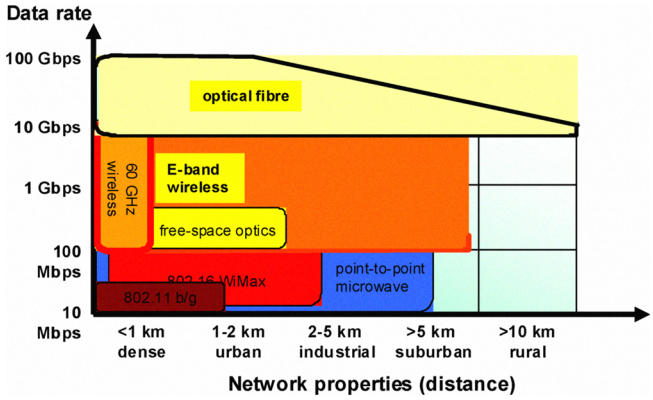

Fig. 1. Schematic representation of data rate in various communications technologies as a function of the achievable link distance.

Transmitters and receivers based on optoelectronic and fully electronic components operating at 100 Gbit/s and 10 Gbit/s data rates, respectively, are realized using multi-chip module packaging technology and microwave monolithic integrated circuits (MMIC). At the data rates envisioned, signal integrity and accurate modeling of interconnects, passives, and on-chip matching circuits demand full-wave 3D electromagnetic (EM) simulation tools. The paper discusses the EM co-simulation and optimization approach for high speed devices and includes many results from the recently completed EU FP6 research project GIBON: Opto-electronic Integration for 100 Gigabit Ethernet Optical Networks.

II. COMPONENT TECHNOLOGIES FOR HIGH-SPEED SYSTEMS

High-speed high voltage swing operation with high current capabilities is one of the requirements for MMIC technology. Potential candidates for the analog front-end of wireless systems and drivers for OEIC systems are SiGe HBT, InP HBT, GaAs mHEMT, InP HEMT technologies and recently also GaN HEMTs. High breakdown voltage is necessary for high linearity and high efficiency power amplifier operation using higher order modulation schemes. The same argument applies to drivers for OE components such as modulators. In addition to high breakdown voltage, high current capabilities

are necessary for high efficiency high linearity power amplifier operation with linear output powers > 100 mW at E-band, linearity C/I > 25 dB, and a power-added efficiency > 20%. In case of OEIC drivers an output swing of > 2 V is required to drive modulators.

From the perspective of transistor performance it seems that InP HBT are best suited. However, they are not as compact as SiGe HBT device, which at E-band frequencies becomes an important aspect. It should also be noted that the digital baseband circuits represent a serious bottleneck, which favors SiGe BiCMOS technology solutions.

Again the same argument applies to drivers for OE components, such as modulators. Modulators with bandwidths into the millimeter-wave range require high voltage switching into low impedance loads of the order of $Z_L \approx 30\ \Omega$, resulting in high dynamic currents. Photodetectors (PD) are the main active components in photonic receivers, while modulators are the main active devices in photonic transmitters.

PD modules are typically packaged using conductor-backed coplanar waveguides (CBCPWs) to connect the PD chip to an output coaxial connector or to an integrated transimpedance amplifier (TA). An illustration of a 100 GHz bandwidth PD packaging structure with a 1mm coax connector is shown in Fig. 3 [3]. The pin of the connector is directly soldered onto the centre conductor of the CBCPW. The upper ground planes are soldered to the outer conductor of the connector. This contact is important to obtain good transmission characteristic in the low frequency range and also shorts the gap between the CBCPW and the connector to reduce unexpected coupling effects.

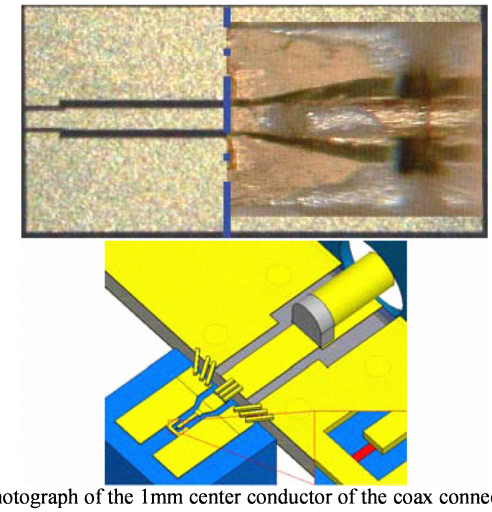

Fig. 3. Photograph of the 1mm center conductor of the coax connector and the CBCPW substrate (top) and a schematic representation of the full package (bottom). Top left: test substrate for CBCPW interconnect structure.

Integrated high-speed modulators are widely realized as electro-absorption modulator (EAM) in transmitters for 40Gbit/s and 100Gbit/s optical communication systems [3],[5]. They offer monolithic integration capabilities, are compact and exhibit modulation efficiency. Monolithic integration of an EAM with a laser forms an electro-absorption modulated laser (EML) structure [6]. Schematic drawing of a 100 Gbit/s EML structure is illustrated in Fig. 4 together with a photograph of the realized EML, the packaging geometry and the setup used in EM simulations. A 100 Gbit/s operation demands for an electrical to optical transmission bandwidth of $B_{eo} > 70$ GHz, resulting in a strong dependence on the load impedance [6] and EML time-constant $\tau_{EML} \sim 1/C_s(Z_L||Z_d+R_s)$, where Z_d is the driver impedance, Z_L the load impedance, C_s the EAM junction capacitance, and R_s the EAM series resistance [7]. Further details in the fabrication process can be found in [9].

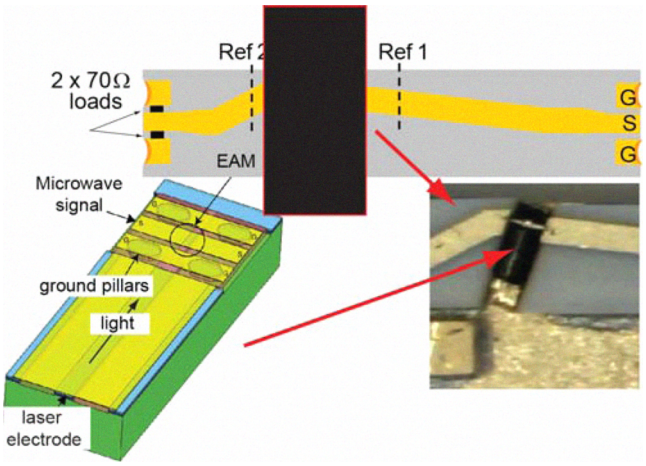

Fig. 4. Schematic drawing of the EML package structure and the EML internal structure employed in EM simulations. Insert shows photograph of wirebonded EML. Reference planes for simulation by parts are also shown.

The packaging examples for high-speed components demonstrate that it is necessary to accurately design interconnect structures, such as wire bonding or flip-chip, as well as monolithic interconnects between different contact structures. The design must further be capable to accurately predict chip to chip and chip to substrate transitions. Such a design requires 3D EM simulation tools, because of the essential 3D geometry of the package structures. 3D EM simulation tools are not sufficiently efficient direct co-simulation in the component design process, which partially requires large-signal operation analysis. In the following section we will discuss a possible solution methodology employing EM based circuit co-simulation with accurate excitation schemes.

III. Interconnect and Packaging Modeling

The 3D character of the packaging with transitions to planar transmission lines, such as conductor backed coplanar waveguides (CBCPW) and CPW to microstrip and wire bond transitions requires accurate modeling of signal transmission including radiation losses, losses due to modal transitions and metallic as well as dielectric losses of typically multi-mode structures. The complex simulation environment demands improved excitation schemes for planar structures, which should allow to excite the actual signal propagation modes with the correct field pattern. This can not be easily accomplished with structures such as wave ports or discrete lumped ports in EM simulations.

We therefore suggest to employ 3D EM simulation tools using a novel excitation scheme as described in the next section. Circuit co-simulation schemes will be discussed in the subsequent section.

A. *Electromagnetic excitation tools*

Excitation schemes in EM simulations determine the accuracy of the simulation results. Standard schemes such as wave ports are very efficient in closed waveguide geometries, but may lead to inaccurate results in planar structures, especially CPW type structures. Another disadvantage of this excitation scheme is that it is difficult to simulate situations where the actual excitation is within the simulation domain. We have recently developed an excitation scheme, which overcomes these problems and is well suited for complex inhomogeneous EM simulation environments. The basic idea is to employ a discrete port in a structure shown in Fig. 5, which is then deembedded from the simulation results in a similar way as in the measurements.

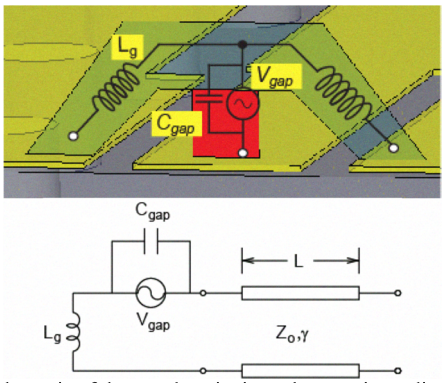

Fig. 5. Schematic of the novel excitation scheme using a discrete port.

The equivalent circuit for this excitation scheme can be represented by only two parameters. It is possible to resemble the situation often encountered during measurements, when the probe tips are placed away from the edge of the substrate on some pad structures. Typical values for the equivalent circuit elements of the excitation port are $L_g = 25 - 40$ pH and $C_{gap} = 5 - 7$ fF. The de-embedding procedure for this port resembles standard calibration procedures [11]. In the simplest case one can employ the L – 2 L calibration method, where the unknown equivalent elements of the excitation scheme have been lumped into an error network T_A and T_B for two-port measurements, respectively.

Two simulations at two different lengths result in

$$\begin{aligned} T_{L,sim} &= T_A T_L T_B \\ T_{2L,sim} &= T_A T_L T_L T_B \end{aligned}, \qquad (1)$$

which can be solved for a thru connection of the two unknown error boxes

$$T_{thru} = T_A T_B = T_{L,sim} T_{2L,sim}^{-1} T_{L,sim} \qquad (2)$$

and finally the unknown elements are determined as

$$\begin{aligned} L_g &= \Im\left\{\frac{T_{thru,12}}{2}\right\}/\omega \\ C_{gap} &= \Im\left\{\frac{T_{thru,21}}{1+T_{thru,11}}\right\}/\omega \end{aligned}. \qquad (3)$$

In some cases higher accuracy or non-symmetrical excitation ports are desired where the short-open calibration (SOC) can be used [15]-[18].

This technique has been employed for a short CPW transmission line on isolating semiconductor substrate with pad structure for on-wafer measurements, shown in Fig. 6. It can be seen that the calculated transmission coefficient is able to represent the magnitude and the phase with a fair agreement, with slight changes in the predicted resonance frequency. All small details from measurements can be replicated in the EM simulations.

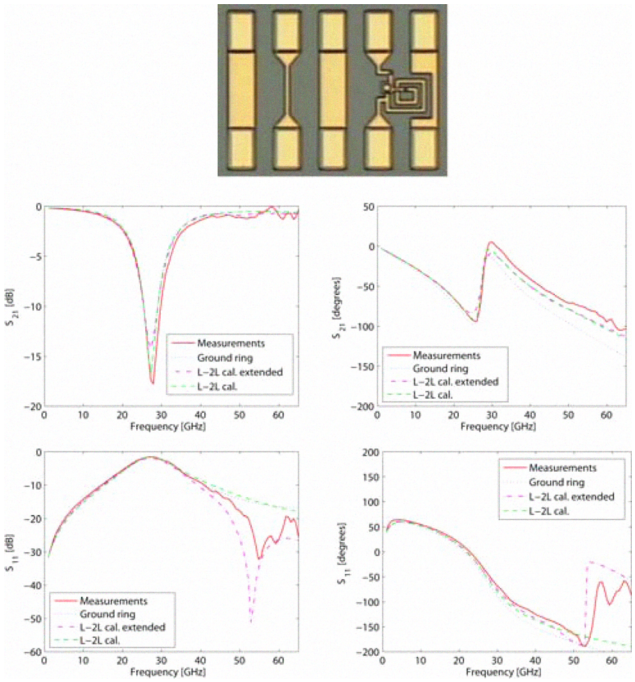

Fig. 6. Planar structure for verification of the de-embedding technique with on-wafer measurements. Comparison of measured and simulate S11 and S21 versus frequency for different excitation schemes.

IV. DEVICE EM CIRCUIT CO-SIMULATION

In this section we describe the EM circuit co-simulation and design using the above methodologies. The EM simulation is exemplified on an EML and a PD device.

A. *EML equivalent circuit modeling*

The EML structure together with the excitation and its equivalent circuit is illustrated in Fig. 7. An orthogonal microwave and lightwave propagation direction scheme is employed to avoid any curvature in the RF path. Further details in the fabrication process can be found in [9].

To estimate the E/O response of the integrated EML structures an EM/circuit co-simulation approach was proposed [8], [9]. The EAM part is modelled using a series resistance R_s and capacitance C_s, and a dynamic photocurrent-resistance R_{ph} [10]. The dynamic photocurrent resistance is essential to predict the effect of the optical power on the E/O response. An external shunt capacitor C_p is also included. This represents partly the capacitance of the iron doped InP buried layer in the region outside the EAM multi-quantum well (MQW) stack and partly the pad capacitance. The isolation resistance R_{iso} represents the coupling to the laser part. The laser part itself is modelled here with a single capacitor C_{laser}. The E/O response is determined by the voltage V_o across the EAM diode junction.

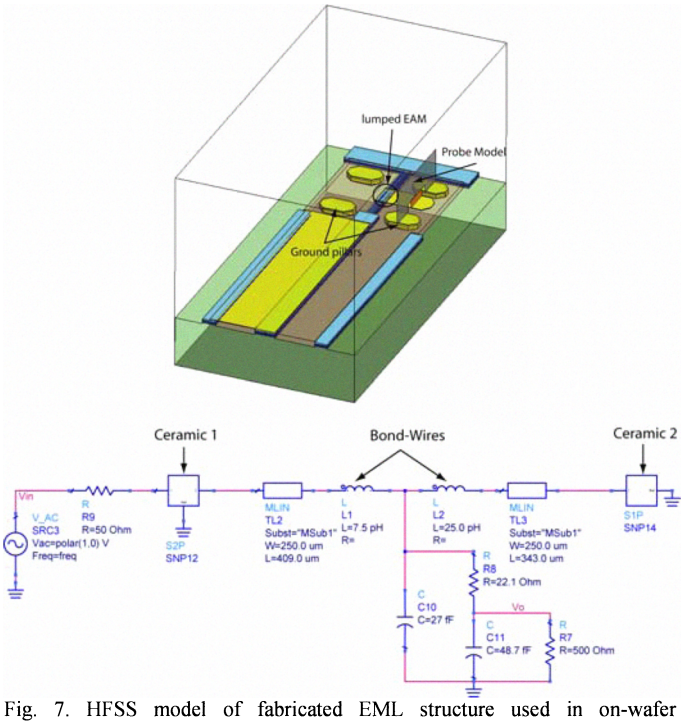

Fig. 7. HFSS model of fabricated EML structure used in on-wafer measurements. The probe GSG excitation is resembled using the bridge configuration shown.Integrated EML Structure

The extraction procedure employs the imaginary part of the admittance parameters measured at several bias points in order to separate the total extracted capacitance between the bias dependent MQW junction capacitance C_s from the bias independent pad capacitance C_p external to the MQW junction. The series resistance R_s was extracted from the real part of the impedance parameter at high forward bias currents The dynamic photocurrent resistance R_{ph} can be determined from the real part of the impedance parameter once R_s is known. A simple estimate of the network describing the coupling between the EAM and laser parts and consisting of R_{iso} and C_{laser} can be obtained from the observed increase in the imaginary part of the admittance parameters at low frequencies. From the equivalent circuit model of the integrated EML structure illustrated in Fig. 7 it is observed that the laser capacitance shunts the junction capacitance at frequencies in the MHz rangeThe element values of the equivalent circuit model for the integrated EML structure at the bias point of V_d=-2.0V are given in table 1.

TABLE I
ELEMENTS OF EQUIVALENT CIRCUIT MODEL FOR V_D=-2.0V
(*Ilaser<Ith)

Element	C_s [fF]	C_p [fF]	R_s [Ω]	R_{ph} [Ω]	L_p [pH]	R_{iso} [MΩ]	C_{laser} [pF]
Value	48.7	27.1	22.1	500/ 25k*	15.0	0.5	2.0

Previously, EM simulations of EAMs have been performed by substitution of the MQW stack in the EAM diode junction with a dielectric material having an average permittivity [12]. In this work a different approach is followed in that a lumped small-signal equivalent circuit model for the MQW stack in the EAM and the laser junction parts are included into the HFSS EM simulation.

The integrated EML structure has been wire-bonded onto 50Ω microstrip lines on an alumina ceramic substrate as shown in Fig. 4. The experimental results of the assembled EML structure, as indicated in Fig. 8 and Fig. 9, demonstrate impressive 3dB bandwidth capabilities of approximately 45 GHz and 60 GHz for the microstrip assembly using 50Ω and 35Ω loads, respectively [9]. The intrinsic time-constant limiting the bandwidth is approximately given by $C_s \cdot (Z_o \| Z_d + R_s)$. With the element values given in table 1 one obtains bandwidths of 69GHz and 76GHz for the 50Ω and 35Ω loads, respectively.

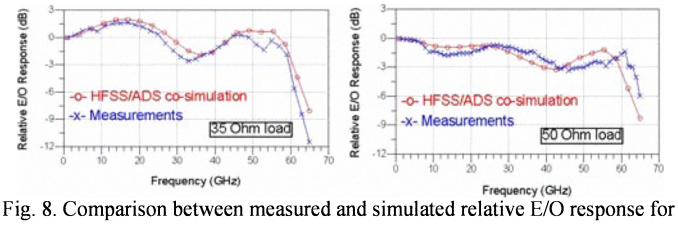

Fig. 8. Comparison between measured and simulated relative E/O response for EML microstrip assembly. Left: Z_0=35Ω; Right: Z_0=50Ω.

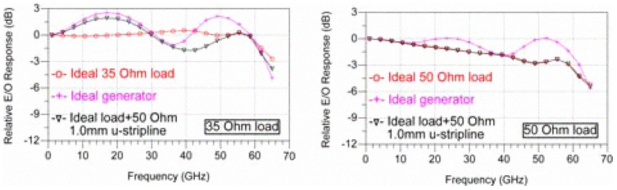

Fig. 9. Investigation of relative E/O transmission response for EML u-strip assembly variations. Left: Z_0=35Ω; Z_0=50Ω.

B. Modeling of the photodiode assembly

EM models usually refer to passive structures in microwave and millimeter-wave application, here we will demonstrate that PDs as active devices can be modelled at behavioral level in EM simulations. Since PDs are opto-electronic (O/E) devices, the behavioral model accurately describes the O/E response of the devices given by $R_{PD} = P_{el}/P_{opt}$. The EM behavioral model S21 can be used to characterize the O/E response of the PDs if the port impedances are appropriately assigned, as S21 is equivalent to the power gain of a two-port network. Such a model intrinsically include the RC and transit time limitation in device performance. The major advantage of this approach is the capability of the model to naturally include all parasitic effects without the necessity for their extraction. The simulation model and its results are presented in Fig. 10.

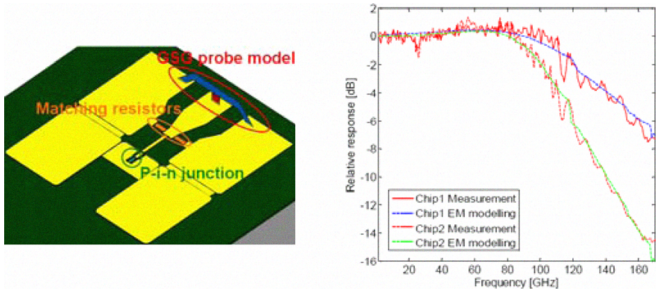

Fig. 10. The EM model of a PD and comparison between the simulated and measured relative response of the high-speed PD.

The EM model includes the active part (junction capacitance and resistance, transit time effects etc) as lumped elements and otherwise is built on a precise layer structure of the actual diode. One can deduce from the results that an excellent agreement between measured and simulated values can be achieved using this approach.

This approach can also be used to optimize PD devices for very high frequency operation, as indicated in Fig. 11. One can depict in the figure that a sample PD device incorporated into a CPW structure for measurements can suffer contact resistance problems, which can be clearly seen in the simulated characteristics presented in Fig. 11. The target frequency of operation is 1000 GHz.

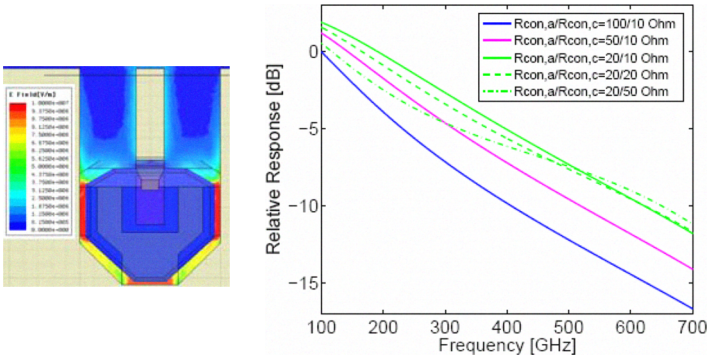

Fig. 11. The simulated relative responses of the PD with varied contact resistance combination and E-field pattern at 400 GHz, where Rcon;a/Rcon;c=10/50. Rcon;a is the anode and Rcon;c the cathode contact resistance, respectively.

A high anode contact resistance can substantially reduce the frequency response and hence the bandwidth of the device. On the other hand if the cathode contact resistance is large compared to the anode resistance, one depicts from Fig. 11 that high frequency performance can be enhanced. This is due to the capacitive short circuiting effect in the cathode CPW structure for this device.

V. CONCLUSION

The present paper shows an improved EM approach for the optimization of the electrical and optical device performance. The EM based analysis allows for a realistic prediction of the device performance and does not require the extraction of the parasitic elements of typical equivalent circuits. This approach has been verified against electrical and E/O measurements up to 110 GHz for various fabricated structures. As a second majore results we report on the utilization of the EM model and co-simulation for packaging problems and identification of potential embedding and mode conversion issues. The EM/circuit co-simulation environment established here provides a path for an improved design of high-speed packaged assemblies with multi-chip modules.

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