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Three dimensional electrochemical system for neurobiological studies

Patricia Vazquez, Maria Dimaki, Winnie E. Svendsen

Abstract— ***In this work we report a novel three dimensional electrode array for electrochemical measurements in neuronal studies. The main advantage of working with these out-of-plane structures is the enhanced sensitivity of the system in terms of measuring electrochemical changes in the environment of a cell culture in real time. In addition, the system is devised to offer a compact solution that helps to obtain a homogeneous distribution of current density among the active electrodes.***

I. INTRODUCTION

SENSORS for measurements of neurobiological events need to be fast and small, with a lower limit being a 1μm disk shaped electrode [1]. A fast response in the subsecond time scale is essential when trying to detect neurotransmitters, since the lifetime of these chemicals in the extracellular space is short [2].

The time response of an electrode is equal to the time required to charge its double layer. This is the shortest time that ensures a decoupling between faradic effects and capacitive ones, the former being the effects that contain the kinetic information of the chemical processes going on in the solution. The time response is in the order of R_sC_{DL}, (R_s being the solution resistance and C_{DL} the double layer capacitance of the electrode) [1], and thus by minimizing both R_s and C_{DL} fast responses of the system can be achieved. This fact leads us to the starting point of using small and three dimensional electrodes: small, because that will minimize the capacitance, and three dimensional for obtaining high surface area ratios that would decrease R_s.

Additionally, in mammalian neurons the amount of neurotransmitters released from each vesicle is in the range of 30000 molecules [3], so high-sensitivity recordings are required. The major source of noise in the electrodes is the thermal noise, which is directly depending on their resistance [4]. Since this value is inversely proportional to the surface area, using three dimensional electrodes provides higher signal-to noise ratios.

It is for this reason and for the known fact that three dimensional structures promote cells to spread over similarly to their natural settings that we have devised a design where out of plane electrodes are active sensors for electrochemical measurements. The problem of integration of a larger counter electrode with the active electrodes (which is necessary to provide the active electrode with current) in a compact way is resolved by surrounding its structure with the smaller working electrodes Figure 1; this design helps to obtain a homogeneous distribution of current density among them and thus make the sensor system more reliable against disturbances such as bubbles in the microfluidic system for cell culturing or inhomogeneous directionality of the input signal.

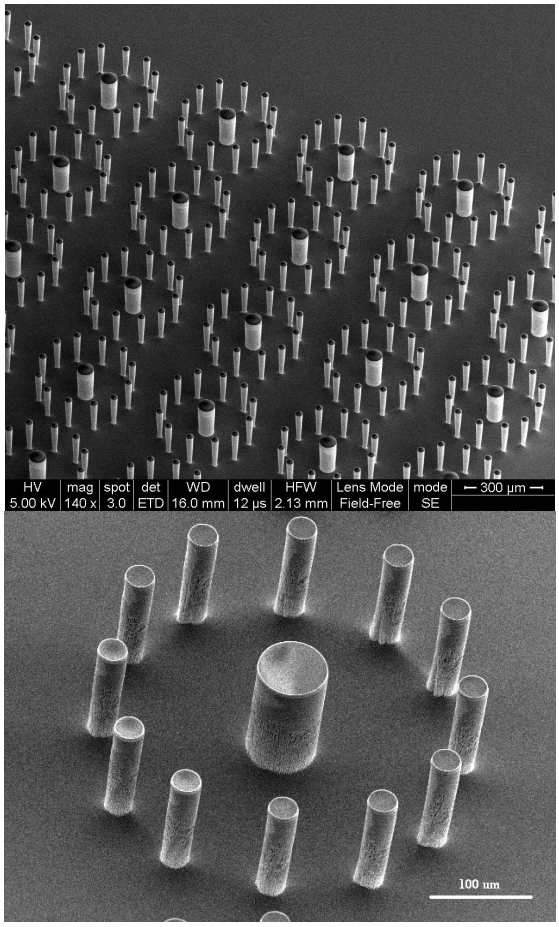

Figure 1: SEM image of an array of electrodes (top) and (bottom) detail showing the main pillar (center, counter electrode) surrounded by the smaller active electrodes.

The system is also intended to be used in brain tissue slice studies, since the electrode height (in the order of 100 μm) is big enough to penetrate the dead cell layers at the surface of

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acute brain slices, thus reducing the distance to the active cells and increasing the signal.

In this article we will show the fabrication process followed to obtain the first electrode system and what the prospects are for future applications of these structures. In the first results, arrays of electrodes with an active area of around 100 μm in height were obtained.

The electrodes are fabricated in silicon and their walls are completely covered by a thin metal layer that acts as the conductor element.

A major drawback in the fabrication of out-of plane structures as tall as in our system is the metallization step, where they become active electrodes. The technical challenge resides into covering the almost vertical walls of the pillars.

II. Fabrication process

The main steps followed in the fabrication process are described in Figure 2. The first step is to define by photolithography the areas of the silicon that will be etched; this is done by spinning a thick resist of 4 μm on the wafer and then expose and develop it to obtain the mask features to define the top of what will be the electrodes. The wafer is then etched to obtain the pillar structures. Since all structures are made on the same surface of silicon, and therefore connected electrically, it is necessary to use an isolation layer and a posterior metallization to target only specific areas as electrically active. For this purpose we used a Low Pressure Chemical Vapor Deposition (LPCVD) furnace that deposited 200 nm of stoichiometric silicon nitride on top of the wafer. It is a process that allows for a good step coverage; this feature is key to the vertical walls in our electrodes. The pillars become active electrodes by the following metallization of their surface, and lastly the desired active sites of their surface will be uncovered from a second insulation layer of silicon nitride.

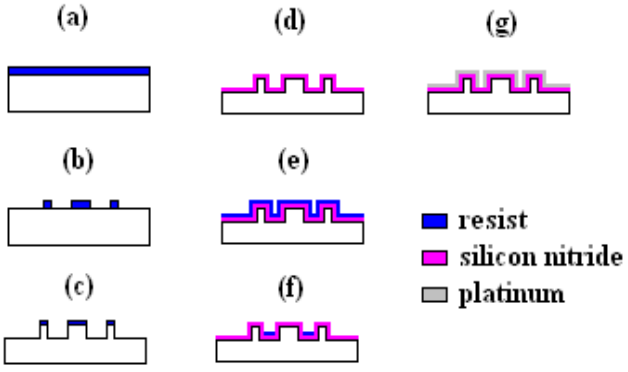

Figure 2: Fabrication procedure for out of plane electrodes made of Si. (a) and (b) are typical steps to define by photolithography a pattern on a silicon wafer; (c), creation of the pillars after etching; (d) isolation of electrode structures by growth of a silicon nitride; (e) and (f) show a second photolithography step to define wiring and electrodes areas for the final (g) metallization of electrodes with a lift off step. A final step of insulation of the array is done by deposition of silicon nitride and etch of the active sites of the electrodes to uncover them.

A. Plasma etching

There are several etching methods to achieve high aspect ratio structures in silicon and they have been all profusely explained in the literature [5-7]. The one chosen for our experiment is plasma etching, due to the high etch directionality of the process independent of the crystal orientation of the silicon. Applying the Bosch technique [8] with plasma etching it is possible to obtain very high out-of-plane structures with almost vertical walls. In our labs, an Inductively Coupled Plasma Etcher (ICP) provided by the company STS was used for the process.

Determining the optimal values of the parameters that influence the shape of the etched structures is not a trivial task, though. Ayon *et al.* [7] give very useful guidelines for understanding the effects of power, pressure and gas concentrations. However, application of these rules for our particularly tall structures (in the range of 100 μm), caused the appearance of a non desired side effect that needed to be tackled: the molding of the plasma sheath to the bottom of the surface. This effect starts to appear when the dimensions of the structures are comparable to the thickness of the sheath [9, 10], and it translates into a faster etch at the bottom of the pillars. Few reports mention this effect. It is responsible for etching at a faster rate at the base of the electrode-pillars than their top. This trend is noticeable in Figure 3.

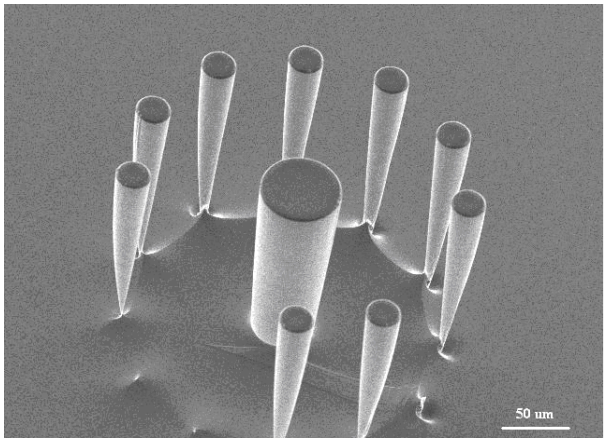

Figure 3: SEM image of silicon pillar etched during a Bosch process that shows the inward deviation of the walls at its base (this effect is most prominent in the outer pillars as they are more exposed to the plasma)

In order to avoid it, Hanein *et al.* [11] proposed the idea of protecting a main pillar with surrounding sacrificial structures, in a way that they would obstruct the plasma coupling to the bottom of the main electrode and thus avoid

the underetch. They also used a second etching step to sharpen the main pillars and get rid of the sacrificial structures; the latter happens naturally as a consequence of the etching process.

We have used this idea with the intention of keeping the sacrificial surrounding pillars as working electrodes and the main pillar as a counter electrode for an electrochemical measurement setting. This solution has helped to fabricate arrays of electrodes with heights in the range of 100 to 120 µm and diameters in between 10 and 70 µm. Figure 1 shows an example of the design.

B. Metallization

A difficult step in the process is the metallization of the electrodes and the wiring to the outer pads for external connections. This is maybe why it is not so frequently described in the scientific literature reports, although it remains a challenge in the fabrication of out-of-plane structures that are meant to be electrically active. The major concern is the quality of step coverage at the electrode sites.

There is also an issue with the preparation step that consists of a negative photolithography step in order to transfer on the wafer the pattern of the wiring and electrode sites that need to be metalized. The existence of structures of different heights in the design make the spinning of the resist a difficult task; the proximity to the UV light source when the process of exposure takes place differs for these structures, and therefore so does the optimal exposure time. This effect is translated into under or overexposure at different sites of the design. Moreover, the proximity of the structures to each other affects the spinning of the resist in between them; the results are poor uniformity in the thickness of the resist and consequently more problems in the development phase, as it is shown in Figure 4.

Several attempts were made in order to achieve an optimal spread of the resist, with three different thicknesses: 1.5, 2.2 and 4.2 µm; all of them were also spun at different velocities, with no seemingly improved results.

As it seems, for a proper spreading of the resist around the electrodes the minimum pitch of those need be not less than 250 µm, and although the process needs further optimization some first results with wire definition could be obtained. Those were done with a final resist thickness of 1.5 µm.

For the metallization step itself, Pt was the material of choice; the reasons behind this decision lie on the fact that it is biocompatible and durable in electrochemical environments, and thus it is a suitable candidate for our chip. The metal was deposited on the wafer with a Physical Vapor Deposition (PVD) process carried out in a magnetron sputtering machine for 299 seconds. This process usually provides structures with an excellent step coverage, which is critical for reliability of electrical conductivity in the pillar-electrodes.

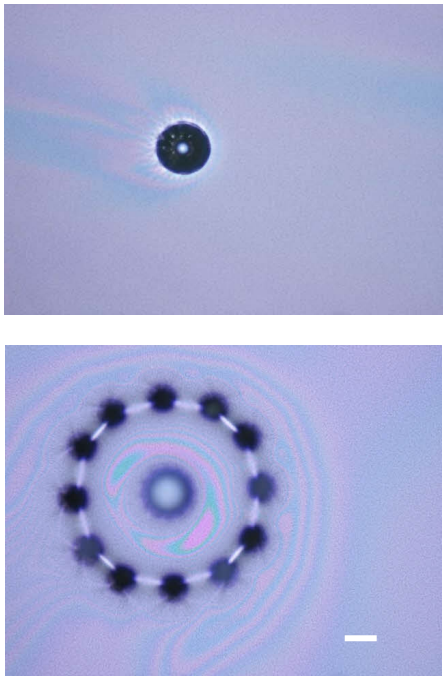

Figure 4: Spun resist (1.5 µm) on (top) the site of a 30 µm electrode surrounded by sacrificial pillars at a pitch of 100 µm and (bottom) a 50 µm electrode with sacrificial pillars at a pitch of 250 µm. Scale bar is 30 µm.

Even so, for high aspect ratio structures such as the focus of this article, such step coverage is not enough to reach all areas of the lateral walls. Figure 5 shows clearly how only the top and part of the lateral walls (encircled areas) have been covered by the metal.

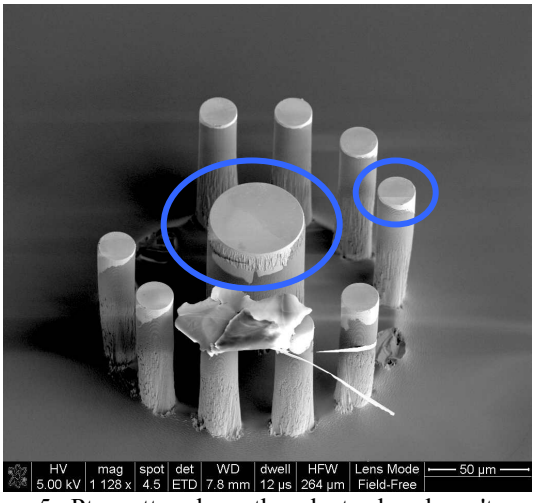

Figure 5: Pt sputtered on the electrodes doesn't cover the side walls. The picture also shows some debris after lift-off

In contrast, Figure 6 offers a view of the electrodes covered by a thin layer of Pt down to the bottom (see detail encircled). The improvement in the coverage of walls was achieved by tilting the wafer inside the vacuum chamber with a home-made holder.

The electrodes should be connected to the outside by the wires shown in Figure 7; technical difficulties due to poor lithography, as commented before, impede the full wiring, but several solutions are under investigation to conclude the array fabrication.

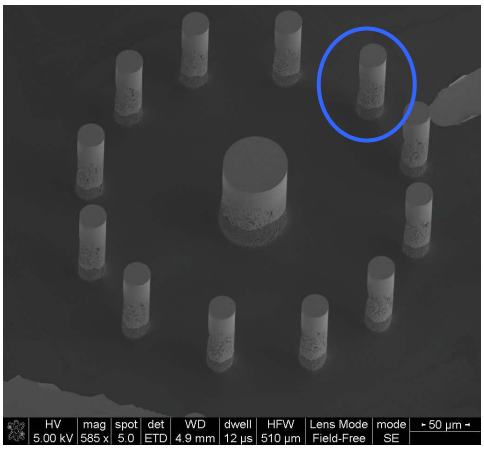

Figure 6: detail of electrode metallization. The blue circle line highlights one of the active electrodes covered by a layer of Pt

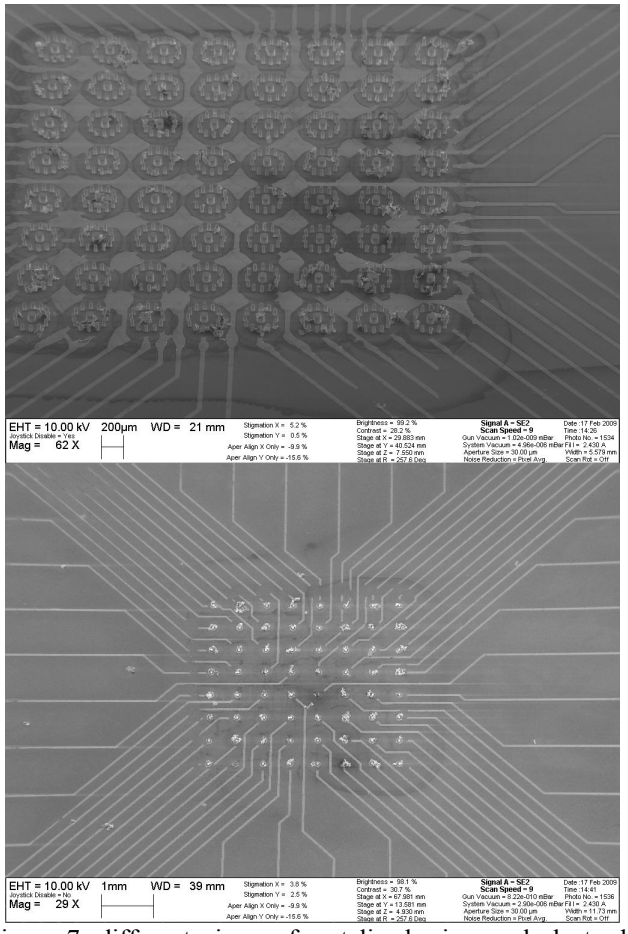

Figure 7: different views of metalized wires and electrode sites

III. SHADOW MASK

One potential solution to avoid the problems generated from the negative photolithography commented in section II is to use a shadow mask for the patterning and metallization of the electrode array. With this process the desired wire pattern is transferred onto the wafer by applying a wafer on top with the wiring already etched on the surface and through the wafer.

For this experiment, a shadow mask was fabricated with a silicon wafer, etched in the ASE to obtain the desired pattern. Figure 8 shows the thus obtained shadow mask. The mask wafer is then attached to the wafer with the electrode array already etched on its surface. Both wafers are sputtered, with the metal only depositing in the uncovered areas. Those uncovered areas are the wires that link the electrodes to the outside pads for electrical connections Figure 9

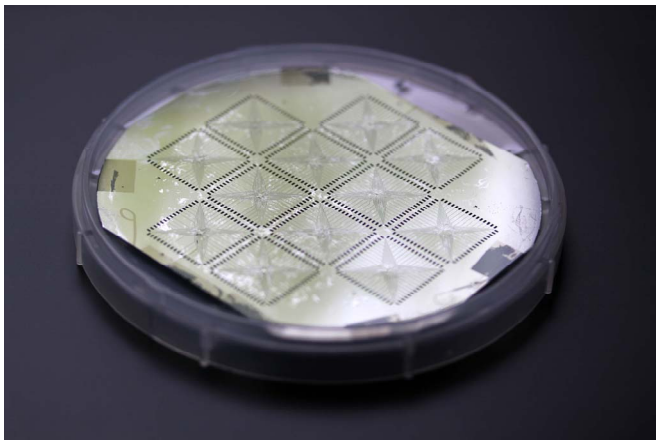

Figure 8: the shadow mask

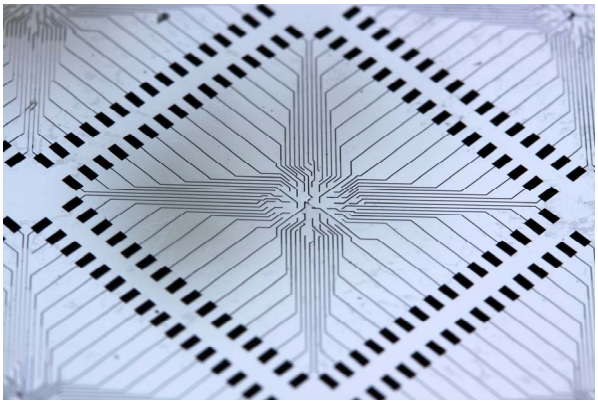

Figure 9: Detail of shadow mask showing the wiring between the electrode array and the external pads

Until now this process has been only tested to check that the patterning of all the details of the wiring is achieved. The next step will be to apply this mask to the electrode array to make the wiring.

IV. RESULTS AND CONCLUSIONS

We have designed and fabricated a system with counter and working electrodes arranged in such a way as to provide

a uniform distribution of current density for optimal electrochemical measurements. The use of the surrounding working electrodes as protective structures for the etching process of the bigger main electrode in the center helped in controlling the height and profile of the structures.

Several technical issues have arisen in the presence of different planes when it comes to photolithographic processes. The different height between the top of the electrodes and the surface of the wafer, together with the density of the electrodes interfere with a perfect transfer of the desired pattern onto the wafer. We have found that with a pitch of 250 μm it is possible to obtain reasonably good wafer coverage. Nevertheless, we have been able to metalize electrodes with vertical walls with height in the range of 100 μm. Some preliminary results are shown in Figure 7.

Although the metallization process requires some optimization (see Figure 7 top, showing poor wire definition at some areas), it has allowed us to obtain the array of electrodes in a novel configuration for electrochemical measurements. The wiring fabrication will be improved with the use of a shadow mask during the metallization.

The next step will be to test our system with cells in order to study the limitations in the speed of the response of the electrodes and the signal to noise ratio obtained. This will be achieved with a full integration into a microfluidic system for cell culturing on top of the electrode array.

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