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Ølgaard, Christian; Sassene, Haoues; Perch-Nielsen, Ivan R.

Published in:

Proceedings of the IEEE International Symposium on Circuits and Systems

Link to article, DOI:

[10.1109/ISCAS.1996.539883](https://doi.org/10.1109/ISCAS.1996.539883)

Publication date:

1996

Document Version

Publisher's PDF, also known as Version of record

[Link back to DTU Orbit](#)

Citation (APA):

Ølgaard, C., Sassene, H., & Perch-Nielsen, I. R. (1996). An area efficient low noise 100 Hz low-pass filter. In Proceedings of the IEEE International Symposium on Circuits and Systems (Vol. Volume 1). IEEE. DOI: [10.1109/ISCAS.1996.539883](https://doi.org/10.1109/ISCAS.1996.539883)

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AN AREA EFFICIENT LOW NOISE 100 HZ LOW-PASS FILTER

Christian Ølgaard¹, D. Haoues Sassene² and Ivan R. Nielsen³
 Center for Integrated Electronics, Technical University of Denmark, Denmark

¹CIE, Presently with National Semiconductor Corp.
 coe@marconi.nsc.com

²CIE, Presently with GN-Danavox A/S, Denmark
 dhs@it.dtu.dk

³CIE, Presently with NOKIA Mobile A/S, Denmark
 Ivan.Riis@nmp.nokia.com

ABSTRACT

A technique [1] based on scaling a filter's capacitor currents to improve the noise performance of low frequency continuous-time filters is presented. Two 100 Hz low-pass filters have been implemented: a traditional low pass filter (as reference), and a filter utilizing the above mentioned current scaling technique. The two filters utilize approximately the same silicon area. The scaled filter implements the scaling by use of a MOS based current conveyor type CCII- [2]. Measurements indicate that the current scaled filter results in a noise improvement of approximately 5.5dB over the reference filter when a class A/B biasing scheme is used in the current divider. Obtaining identical noise performance from the reference filter would require a 3.6 times larger filter capacitor. This would increase the reference filter's die area by 100%. Therefore, the current scaling technique allows filters with improved noise performance/dynamic range, given a fixed silicon area and a fixed power supply.

1. INTRODUCTION

Fully integrated continuous-time (C-T) low-pass filter design has always been a non-trivial task to the designer. Problems like variation of the passive components' absolute value and a limited silicon area makes it a challenge for any designer to perform a smooth silicon implementation. Presently, many techniques to solve the problems of component variation have been presented [3].

However, given the current trend of lowering the supply voltages, new problems may arise. A lowering of the supply voltage reduces the maximum obtainable dynamic range (signal to noise ratio). It is well known that for a large number of filter topologies, the dynamic range is limited by the kT/C factor [4] - thus, the dynamic range is limited by the silicon area being allowed for capacitors in the given filter implementation.

This paper presents a technique to improve the noise performance of a filter given a fixed silicon area. The technique is based on down-scaling the current flowing into the filter's capacitor. By down-scaling the capacitor's current, the capacitor will appear bigger when seen from the outside. This allows smaller resistor values to be used, thus, less noise.

To illustrate the possibilities of the current scaling technique, two 100 Hz first order low-pass filters have been implemented. A reference filter utilizing a traditional topology, and a filter topology utilizing current scaling. The two filter topologies are shown in fig. 1. Both filters utilize about the same silicon area. The current-scaler is implemented as a Current Conveyor type II (CCII) operated in class AB

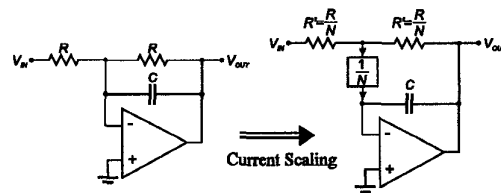


Figure 1. LP-Filter: Reference (left), Current-scaled (right)

mode. Measurements indicate that the current scaled filter offers a significant improvement in the dynamic range, while maintaining a silicon area identical to the reference filter.

First the noise impact of the current scaled filter is discussed, followed by design considerations on how to implement the highest possible dynamic range. This is followed by details of the actual implementation and presentation of simulated results. Measurement results from the fabricated chips are then presented and compared to the simulated results. Finally, some concluding remarks are presented.

2. NOISE IMPROVEMENT BY CURRENT DOWN-SCALING

The transfer function of the filters shown in Fig. 1 is given by

$$H(s) = \frac{-1}{sRC + 1} \quad (1)$$

Assuming a noiseless operational amplifier, the total output noise can be determined by

$$\overline{v_{n,out}^2} = \int_0^\infty \frac{4kT \cdot 2R}{(2\pi fRC)^2 + 1} df = 2 \cdot \frac{kT}{C} \quad (2)$$

Equation(2) indicates the kT/C relationship - the factor of two originates from the fact that two resistors are used. As already concluded a large capacitor value is required to obtain low noise. However the chip area limits the capacitor's value. To overcome the problem of limited on-chip capacitor values, current-scaling can be utilized. If the current flowing into a capacitor is down-scaled by a factor N, then the capacitor will appear N times bigger. Current scaling can be implemented in the lowpass filter as shown in fig. 1. Note that the block performing the current-scaling must have a virtual ground input in order for the filter topology to work. The introduction of the current scaler (N:1) reduces the filter resistors by a factor N ($R' = \frac{R}{N}$), thus re-

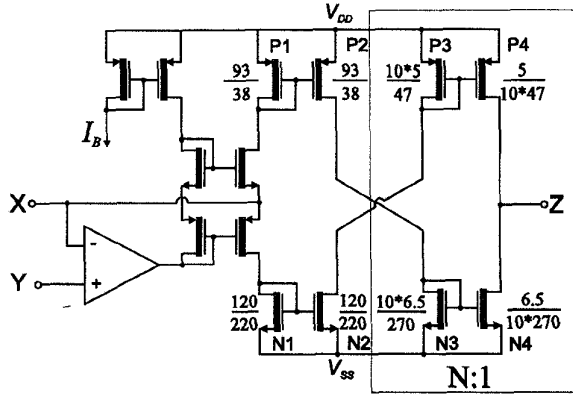


Figure 2. MOS based CCII- Cell

ducing the noise from the passive components by the same factor N , see (2).

Including the noise of the current scaler, the total input referred noise density of the topology is given by

$$\widehat{v_{n,in}^2} = 4kT \cdot 2R' + v_{n,in,1/N}^2 = 4kT \cdot \frac{2R}{N} + v_{n,in,1/N}^2 \quad (3)$$

where $v_{n,in,1/N}^2$ is the noise density of the block implementing the current-scaling (referred to the filter input). Equation(3) indicates that the noise of the current scaler must be lower than the improvement from the smaller resistor values if a total noise improvement is to be achieved.

3. IMPLEMENTATION, LAYOUT & SIMULATION

The actual implementation of the current scaler is shown in fig. 2. The "Y" terminal being connected to virtual ground ensures the virtual ground input property of the current scaler. The major noise contributors in the given topology are the two output current mirrors [1]. In [1, 5] it is concluded that to implement a low noise current mirror, the transconductance G_m of the output mirror's output transistor branches must be as small as possible (the transconductance of P4, N4 on fig. 2). To obtain a low output transconductance, the saturation voltage (V_{mirr}) of the output transistors should be as large as possible.

The maximum capacitor current I_{cmax} occurs for a rail to rail step response, and it is given by (see fig. 1).

$$I_{cmax} = \frac{\Delta V_{in}}{R} \geq \frac{K_P \frac{W}{L}}{2N} V_{mir}^2 \quad (4)$$

The output current mirrors of the current-scaler drives a virtual ground node, so they will have half the supply across their output branches at all times. Therefore, V_{mir} can be chosen close to half the supply voltage for the maximum output current. Similar conclusions are valid for the remaining current mirrors in the current divider topology.

Analysis shows that if the current scaler is operated in class A ($I_B > \frac{N I_{cmax}}{2}$), no noise improvement is obtainable [1]. However, by choosing a lower biasing current (I_B), the scaler will operate in class A/B and consequently, a lower noise in the quiescent state is achieved. The class A/B biasing scheme makes it possible to obtain a noise improvement while ensuring that the filter's large signal behavior is preserved.

The output referred noise density of one of the output current mirrors is given by

$$\begin{aligned} \widehat{i_{n,out}^2} &= \widehat{i_{n,out,w}^2} + \widehat{i_{n,out,f}^2} \\ &= \frac{2}{3} \left(\frac{1}{N} + 1 \right) \cdot 4kT G_m + \left(\frac{1}{A_L} + \frac{1}{A_R} \right) \frac{K'_F G_m^2}{f \cdot C_{ox}} \end{aligned} \quad (5)$$

where $\widehat{i_{n,out,w}^2}$ is the white noise component, $\widehat{i_{n,out,f}^2}$ is the flicker noise component, A_L and A_R are the gate areas of the left (input) and right (output) branches of the output mirrors, and $K'_F \equiv KF(spice)/2\mu_0 C_{ox}$ is a flicker noise coefficient. The two output current mirrors are sized for equal (low) transconductance.

The value of the flicker noise highly depends on transistor sizes. The flicker noise is minimized by distributing a total area optimally among the CCII-'s 8 mirror transistors using the formula presented in [1]. The shown W/L ratios in fig. 2 are based on a total gate area of $100000 \mu m^2$.

4. LAYOUT & SIMULATION

The current-scaling filters were designed using the topology shown in fig. 1 (right) with a feedback capacitance of 100pF and a current-scaling factor of 100 ($R'=159K\Omega$). The 100 Hz reference filter was implemented with a feedback capacitance of 100pF and resistors of 15.9M Ω . Both filters use the same low noise two-stage Miller compensated BiCMOS opamp. The opamp is also used in the MOS CCII- current scaler. The process used is the HBiCMOS from Mietec (3 μ) offered through Eurochip (now EuroPractice)

The layout of both filters is shown in fig. 3. It is observed that the two filters have approximately the same size. The resistors are implemented using high ohmic poly (2k Ω/\square), and the capacitors are of the poly/diffusion type.

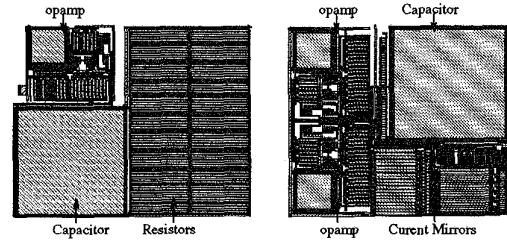


Figure 3. Reference- (left) and Scaled- (right) Filters

4.1. Simulation

Fig. 4 shows the simulated amplitude response and noise spectra of the two filters. The scaled filter shows a clear improvement in thermal (white) noise but it shows a slight increased flicker noise level. The latter originates from the flicker noise of the current mirrors. The opamp and the current mirrors were designed to have approximately the same flicker noise contribution. The current scaler is biased at 0.1% of the max. current. The obtained noise performance is summarized in table 1. Note, that the current scaled filter has a noise performance which is significantly better than the $2kT/C$ "limit" of the reference filter - it is even better than the kT/C "limit" of a purely passive implementation.

Filter Topology	$\frac{Total\ Noise}{(1mHz-10kHz)}$	$\frac{Total\ Noise}{\sqrt{\frac{2kT}{C}}}$
Reference Filter	9.2424 μV_{rms}	+0.1879 dB
Scaled Filter	4.7810 μV_{rms}	-5.5374 dB

Table 1. Noise performance of the filters versus the noise of the passive components $\frac{2kT}{C}$

A slight deviation from the reference filter's close to ideal amplitude response is observed for the current scaled filter. This deviation originates from poles generated in the current divider's large mirror transistors (large parasitic capacitances) combined with its extremely low bias current.

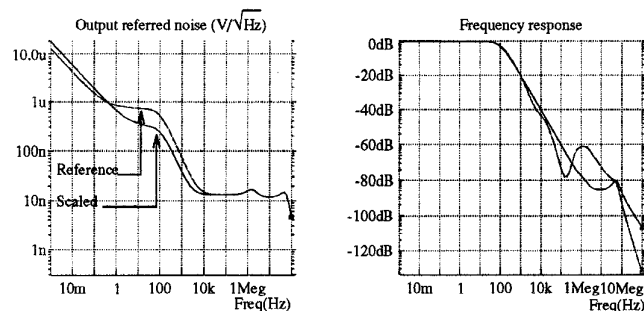


Figure 4. LP-filter Normal/Scaled:Noise spectral Density, Transfer Function

5. MEASUREMENTS

After fabrication the two filter topologies were measured using a +/- 5V supply. Two low noise operational amplifiers (Philips NE5533AN) and a simple output stage were included to allow the filters to drive the 50Ω load of the instruments. Further, for the noise measurements the opamps were used to amplify the noise signal. The operational amplifiers' noise is significantly lower than that of both filters, and the used resistor values were chosen, so they would not contribute significantly to the overall noise of the test setup. Therefore, the noise contribution from the amplifiers and output stage have been ignored. Furthermore, the operational amplifiers and output stage used a voltage supply of +/- 7.5V to be able to verify the large signal behavior of the filters.

Figure 5 shows the measured frequency response of the two filters. As can be seen the two filters have identical cut-off frequency, and the measured performance is close to the simulated response.

Figure 6 shows the two filters' measured noise performance. Unfortunately, the spectrum analyzer used (HP4195A) only allows measurement from 10Hz and up, so the flicker noise performance of the filters has not been verified yet. However, it is clear from the measurements that the current scaled filter has a significantly better noise performance than the reference filter. Furthermore, as can be seen from the figure, the superimposed simulation results¹ indicate that the simulated noise performance is in accordance with actual measurements, and that the noise improvement of about 5.5dB also holds for the measurements. The noise floor observed in the measurements originates from the used spectrum analyzer.

¹ compensated for the amplification in the measurement setup.

To verify the large signal behavior, distortion measurements were performed on the current scaled filter when using a +/- 4V input signal. The measured total harmonic distortion @ 100Hz is less than 0.1%. This indicates that the current scaled topology preserves the large signal behavior, thus the topology allows an increased dynamic range.

6. CONCLUSIONS

A technique to improve the dynamic range in low frequency, low-noise, continuous-time filters is presented. The technique makes it possible to integrate a filter with a higher dynamic range/lower noise without using extra silicon area. The technique relies on down scaling the currents flowing into the filter's capacitors. This allows the filter's resistor values to be reduced, thus less noise will be generated by the passive components. To obtain an overall noise improvement, a class A/B biasing scheme is required, combined with a careful sizing and layout of the transistors in the current-scaler.

Two prototype 100Hz first order low-pass filters were designed and fabricated. The two filters occupy about the same silicon area. Measurements confirm that the current scaled filter has an improved noise performance. The filter shows a noise improvement of about 5.5 dB over the reference filter without affecting the dynamic range. If a similar noise performance were to be obtained using the reference filter topology, then the capacitor had to be 3.6 times larger. Therefore, the current scaled filter topology demonstrates an area improvement of approximately 50% over the reference filter. Finally, it should be noted that the current scaled filter's noise performance extends the kT/C "limit" many filter topologies exhibit (see table 1).

7. REFERENCES

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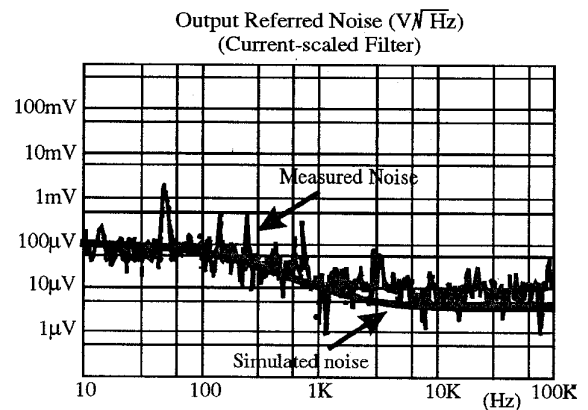
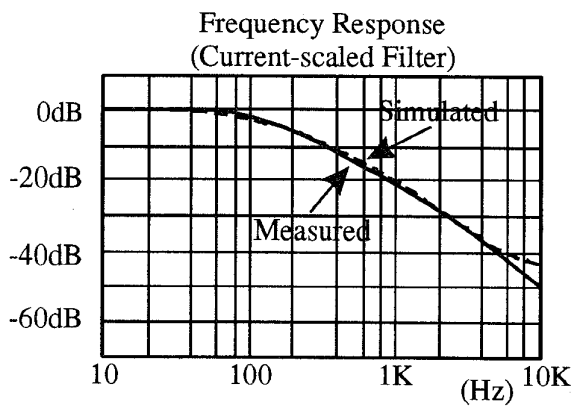
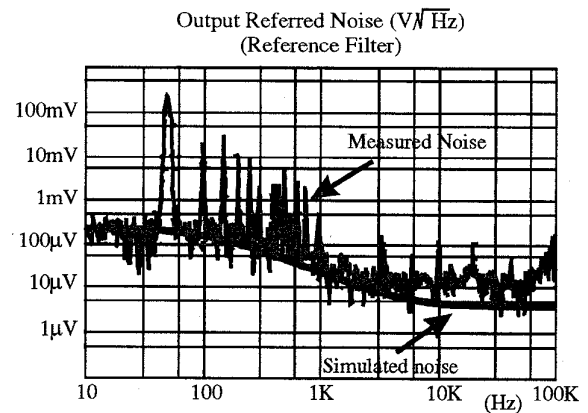
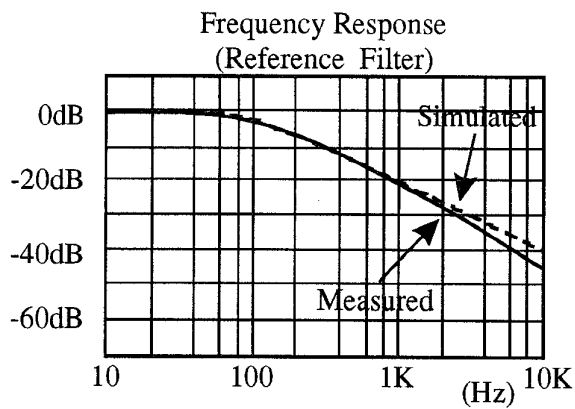


Figure 5. Transfer function: Reference- and Scaled-Filters

Figure 6. Noise spectrum: Reference- and Scaled-Filters