Downloaded from orbit.dtu.dk on: Dec 17, 2017

Technical University of Denmark

Noise Properties of CMOS Current Conveyors

Bruun, Erik

Published in:
Proceedings of the 1996 IEEE International Symposium on Circuits and Systems

Link to article, DOI:
10.1109/ISCAS.1996.539829

Publication date:
1996

Document Version
Publisher's PDF, also known as Version of record

Link back to DTU Orbit

Citation (APA):
Bruun, E. (1996). Noise Properties of CMOS Current Conveyors. In Proceedings of the 1996 IEEE International Symposium on Circuits and Systems (Vol. Volume 1, pp. 144-147). IEEE. DOI: 10.1109/ISCAS.1996.539829

DTU Library
Technical Information Center of Denmark

General rights
Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal

If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.

NOISE PROPERTIES OF CMOS CURRENT CONVEYORS

Erik Bruun
Department of Information Technology, Bldg. 344
Technical University of Denmark
DK–2800 Lyngby
Denmark
E–mail: bruun@it.dtu.dk

ABSTRACT

The definition of the current conveyor is presented and it is shown how different generations of current conveyors can all be combined into a single definition of a multiple-output second generation current conveyor (CCII). Next, noise sources are introduced into the model, and a general noise model for the current conveyor is established. This model is used for the analysis of selected examples of current conveyor based operational amplifier configurations and the relative merits with respect to the noise performance of these configurations are discussed. Finally, the noise model is developed for a CMOS current conveyor implementation, and optimization strategies for noise reduction are discussed. It is concluded that a class AB implementation provides more flexibility than does a class A configuration. In both cases it is essential to design low noise current mirrors and current sources, and with the class AB design the current mirror and current source noise can be reduced by using small values of bias current without compromising the maximum available output current.

1. INTRODUCTION

Although the current conveyor has been around for more than 25 years [1, 2] and current mode signal processing has been investigated thoroughly in recent years [3] only a few reports on the noise performance of current mode devices are found in the literature [4, 5, 6]. In this paper we present a noise model for current conveyors and show how the model can be used to calculate the noise performance of current mode signal processing functions. Further, we analyze the noise characteristics of a CMOS implementation of a current conveyor and discuss design strategies for optimum noise performance of the conveyor.

2. CURRENT CONVEYOR DEFINITIONS

Several generations of current conveyors have been defined over the years [1, 2, 7]. Undoubtedly, the second generation conveyor (CCII) is the more well known of the devices and it is defined by the following relation between the terminal currents and voltages:

$$\begin{Bmatrix} I_y \\ V_x \\ I_z \end{Bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{Bmatrix} V_y \\ I_x \\ V_z \end{Bmatrix} \qquad (1)$$

where the subscripts x, y, and z refer to the terminals labeled X, Y and Z in fig. 1. The CCII is defined in both a positive and a negative version where the +sign in the matrix is used for the CCII+ type conveyor and the −sign is used for the CCII− type conveyor.

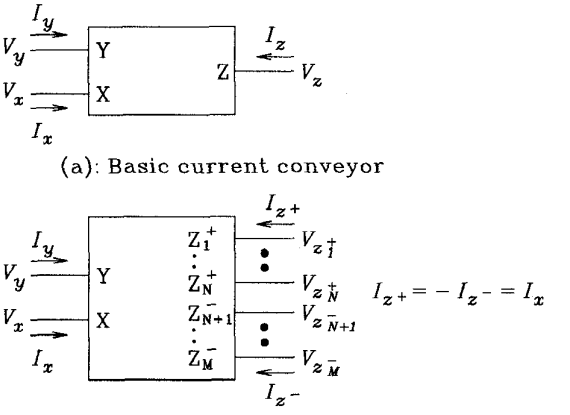

Figure 1. Current conveyor terminal definition.

A first generation conveyor or a third generation conveyor may be realized from a multiple output second generation conveyor simply by feeding back an appropriate Z-output to the Y-input to establish the input relation $I_y = I_x$ (first generation) or $I_y = -I_x$ (third generation) [8]. Hence, we shall concentrate on the multiple output second generation conveyor.

3. NOISE SOURCES

The noise in a conventional amplifier is often described by an equivalent noise input voltage and an equivalent noise input current. However, with a multiple output device such as the current conveyor shown in fig. 1b this is not an adequate noise representation because the outputs may contain both correlated noise contributions and uncorrelated noise contributions. The correlated contributions are conveniently described by an equivalent input noise whereas the uncorrelated contributions must be described by independent output sources. This leads to the noise model shown in fig. 2. Note that a noise voltage is only associated with the Y-input as any noise voltage in series with the X-input can be directly transferred to the Y-input.

Assuming an ideal conveyor, this model leads to the noise output signals given below with the source resistances R_{SX} and R_{SY} connected to the X and Y terminals, respectively.

$$\overline{dv_x^2} = \overline{dv_{yeq}^2} + \overline{di_{yeq}^2} R_{SY}^2 + 4kTR_{SY}\,df \qquad (2)$$

0-7803-3073-0/96/$5.00 ©1996 IEEE

Authorized licensed use limited to: Danmarks Tekniske Informationscenter. Downloaded on March 02,2010 at 07:33:13 EST from IEEE Xplore. Restrictions apply.

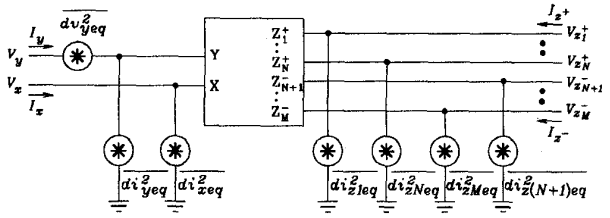

Figure 2. Current conveyor with added equivalent terminal noise generators.

$$\begin{aligned}\overline{di_{zn}^2} &= \overline{di_{xeq}^2} + \overline{di_{zneq}^2} + \overline{dv_x^2}/R_{SX}^2 + \frac{4kT}{R_{SX}}df \\ &= \overline{di_{xeq}^2} + \overline{di_{zneq}^2} + \overline{dv_{yeq}^2}/R_{SX}^2 + \overline{di_{yeq}^2}(\frac{R_{SY}}{R_{SX}})^2 \\ &\quad +(1+\frac{R_{SY}}{R_{SX}})\frac{4kT}{R_{SX}}df \qquad (3)\end{aligned}$$

where k is Boltzmann's constant, T is the absolute temperature, df is the frequency bandwidth considered, and n is the Z-output number. For an ideal conveyor with a single Z-output, the output noise source can obviously be transformed to the X-terminal, so this conveyor structure is described by two independent noise current sources and one noise voltage. With a voltage drive to the Y-input and a current drive to the X-terminal we have $R_{SX} \gg R_{SY}$, and (3) simplifies to

$$\overline{di_{zn}^2} = \overline{di_{xeq}^2} + \overline{di_{zneq}^2} + \overline{dv_{yeq}^2}/R_{SX}^2 + \frac{4kT}{R_{SX}}df \qquad (4)$$

Using the noise model of fig. 2 we can develop noise models for first and third generation conveyors. The first generation conveyor (CCI) is obtained from the CCII by feeding back a positive Z-output to the Y-input. This implies, that the equivalent input noise current of the first generation Y-input is the sum of the second generation Y-input noise current and the Z-output noise, i.e. $\overline{di_{yIeq}^2} = \overline{di_{yIIeq}^2} + \overline{di_{z1eq}^2}$. Similarly, the third generation conveyor is obtained by feeding back a negative Z-output to the (second generation) Y-input, resulting in an equivalent third generation Y-input noise current of $\overline{di_{yIIIeq}^2} = \overline{di_{yIIeq}^2} + \overline{di_{z(N+1)}^2}$.

4. NOISE MODELING OF CURRENT CONVEYOR BASED OPERATIONAL AMPLIFIERS

The current conveyor is a useful tool for describing opamp structures. In doing so, we must take into account the non-idealities of practical realisations of current conveyors. The most important deviations from the ideal conveyor model given by (1) are finite values of input and output impedances. A small signal model with finite values of input and output impedances is shown in fig. 3.

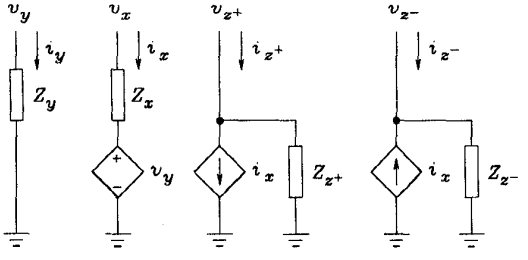

Figure 3. Small signal current conveyor model.

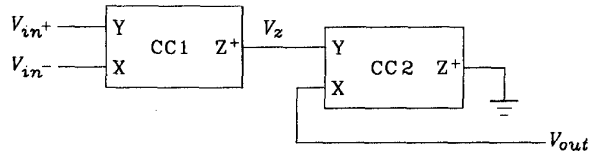

Figure 4. Current feedback opamp described by second generation current conveyors.

This model is very useful in opamp descriptions. As an example, fig. 4 shows a conveyor description of a current feedback opamp (CFOA) [9]. From the conveyor model shown in fig. 3 one can easily find the transresistance of the CFOA as $R_T = R_{z1} \parallel R_{y2}$ and the inverting input resistance as $R_{IN-} = R_{x1}$. Inserting the noise model of fig. 2 and transferring the noise sources to the inputs of the CFOA we find the opamp equivalent input noise sources

$$\overline{dv_{in,eq}^2} \simeq \overline{dv_{y1eq}^2} \qquad (5)$$

$$\overline{di_{in+,eq}^2} = \overline{di_{y1eq}^2} \qquad (6)$$

$$\overline{di_{in-,eq}^2} \simeq \overline{di_{x1eq}^2} + \overline{di_{z1eq}^2} + \overline{di_{y2eq}^2} \qquad (7)$$

Another example is a standard voltage mode opamp (VOA) as shown in fig. 5. The opamp low frequency open loop gain A_o is found by insertion of the model shown in fig. 3. We obtain $A_o = (R_{z1} \parallel R_{y3})/(R_{x1} + R_{x2})$. Referring the conveyor noise sources to the opamp inputs, we find (with $R_{x1} = R_{x2}$)

$$\begin{aligned}\overline{dv_{in,eq}^2} &\simeq \overline{dv_{y1eq}^2} + \overline{dv_{y2eq}^2} \\ &\quad +(\overline{di_{x1eq}^2} + \overline{di_{x2eq}^2} + 4\overline{di_{z1eq}^2} + 4\overline{di_{y3eq}^2})R_{x1}^2 \qquad (8)\end{aligned}$$

$$\overline{di_{in+,eq}^2} = \overline{di_{y1eq}^2} \qquad (9)$$

$$\overline{di_{in-,eq}^2} = \overline{di_{y2eq}^2} \qquad (10)$$

When comparing equations (5)-(7) with (8)-(10) we note that with the same current conveyors used for the two amplifiers the current feedback opamp has a lower equivalent input noise voltage than the voltage mode opamp. Because of the symmetric structure of the voltage mode opamp it has similar input noise currents at the inverting and non-inverting input. The asymmetry in the current feedback opamp leads to different input noise currents for this configuration. The non-inverting input is similar to the voltage mode opamp input, but the inverting input is a low impedance input which is often realized by a common gate or common base configuration. The input noise current of such a stage depends strongly on the bias current sources for the stage and on the subsequent current mirror stages.

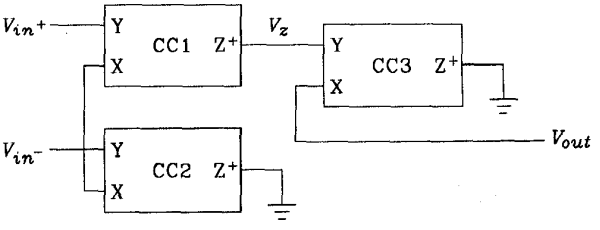

Figure 5. Voltage mode opamp described by second generation current conveyors.

Authorized licensed use limited to: Danmarks Tekniske Informationscenter. Downloaded on March 02,2010 at 07:33:13 EST from IEEE Xplore. Restrictions apply.

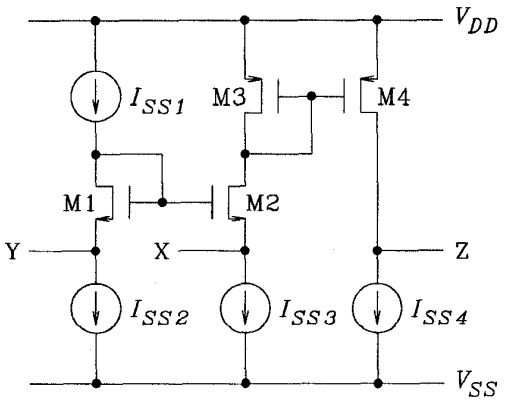

Figure 6. Class A CMOS current conveyor.

5. NOISE MODELING OF CMOS CURRENT CONVEYOR

As an example of a current conveyor implementation we can take the class A CMOS current conveyor shown in fig. 6, [10]. In order to simplify the analysis, we use simple MOS transistor (i.e. without cascoding transistors, etc.), and the bias current generators are assumed to be noiseless ideal current sources of identical magnitude in parallel with noise current sources, $\overline{di^2_{SSn}}$ for current source I_{SSn}. In this way, only four MOS transistor are required to implement the current conveyor, and they are pairwise matched (M1 to M2 and M3 to M4). The noise contributed by each of these transistors can be described by a noise current source $\overline{di^2_{DSl}}$ for transistor Ml between the drain and source. Considering only the thermal noise we have

$$\overline{di^2_{DSl}} = \frac{8kT}{3} g_{ml} df \tag{11}$$

where g_{ml} is the transconductance of transistor Ml. With this transistor noise model and the bias current noise sources we find the equivalent noise generators for the conveyor:

$$\begin{aligned}
\overline{dv^2_{yeq}} &= \frac{\overline{di^2_{DS2}}}{g^2_{m2}} + \frac{\overline{di^2_{DS1}}}{g^2_{m1}} + \frac{\overline{di^2_{SS1}}}{g^2_{m1}} \\
&= \frac{8kT}{3g_{m2}} df + \frac{8kT}{3g_{m1}} df + \frac{\overline{di^2_{SS1}}}{g^2_{m1}} && (12) \\
\overline{di^2_{yeq}} &= \overline{di^2_{SS1}} + \overline{di^2_{SS2}} && (13) \\
\overline{di^2_{xeq}} &= \overline{di^2_{DS3}} + \overline{di^2_{SS3}} = \frac{8kT}{3} g_{m3} df + \overline{di^2_{SS3}} && (14) \\
\overline{di^2_{zeq}} &= \overline{di^2_{DS4}} + \overline{di^2_{SS4}} = \frac{8kT}{3} g_{m4} df + \overline{di^2_{SS4}} && (15)
\end{aligned}$$

It should be noted that the Y-terminal equivalent noise input voltage and noise input current contain a common element ($\overline{di^2_{SS1}}$), so they are not completely uncorrelated. This must be taken into account when calculating the noise in a system using the current conveyor.

Fig. 6 shows a single-output conveyor. For multiple-output conveyors implemented by adding more outputs or cross-coupled current mirrors to the current mirror M3-M4, the separation in X-terminal and Z-terminal noise sources is achieved by considering the input side and the output side of the current mirrors separately.

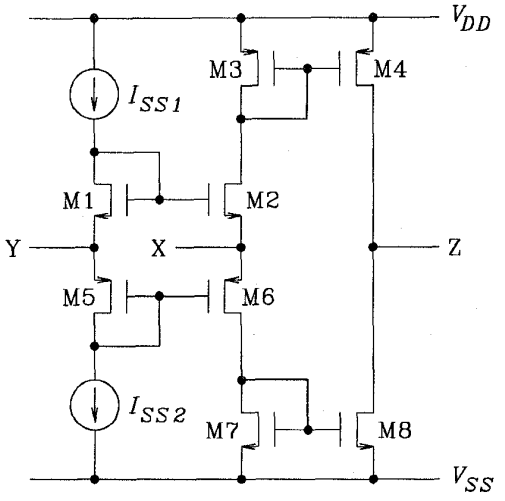

Figure 7. Class AB CMOS current conveyor.

6. NOISE OPTIMIZATION OF CMOS CURRENT CONVEYORS

From (12) it is evident that the equivalent input noise voltage is minimized by selecting a large value of g_{m1} and g_{m2} and minimizing the noise from the bias source I_{SS1}. For the transistor transconductance we may use the expression

$$g_m = \frac{2I_D}{V_{GS} - V_T} \tag{16}$$

where V_T is the transistor threshold voltage. Thus, in order to obtain a large value of g_m, we should select a rather small value of the effective gate voltage $V_{GS} - V_T$. This is achieved by using a wide transistor for M1 and M2. In order to minimize the Y-input equivalent noise current we must design low noise bias current sources. The X-terminal and Z-terminal equivalent noise currents are caused by the noise from the current mirror M3-M4 and the bias current sources I_{SS3} and I_{SS4}. Thus, low noise bias current sources are essential, and for the current mirror transistors, low values of g_m should be used, i.e. either the bias current should be small or the effective gate voltage should be large. The bias current is determined by the required dynamic range at the conveyor Z-output. With a class A current conveyor configuration the current swing at the Z-output cannot exceed the bias current. Assuming a required current swing of $i_{z,max}$, a voltage drive to the Y-input, and a current drive to the X-terminal, we find the Z-output noise current

$$\overline{di^2_z} = \frac{8kT}{3}(g_{m3} + g_{m4}) df + \overline{di^2_{SS3}} + \overline{di^2_{SS4}} \tag{17}$$

In a CMOS technology the bias current sources are implemented with MOS transistor, so the noise currents $\overline{di^2_{SS3}}$ and $\overline{di^2_{SS3}}$ can be assumed to be of the form

$$\overline{di^2_{SS}} = \frac{8kT}{3} g_{mSS} df \tag{18}$$

with g_{mSS} being proportional to the transistor transconductance of the current source transistor. Combining (17) and (18) with (16) we find that the noise output power is proportional to the bias current, i.e. proportional to $i_{z,max}$. The available output signal power is proportional to $i^2_{z,max}$.

Authorized licensed use limited to: Danmarks Tekniske Informationscenter. Downloaded on March 02,2010 at 07:33:13 EST from IEEE Xplore. Restrictions apply.

Transistor	M1	M2	M3	M4
W/L	80/2.4	80/2.4	24/2.4	24/2.4
g_m	$660\mu S$	$660\mu S$	$200\mu S$	$200\mu S$
Transistor	MSS1	MSS2	MSS3	MSS4
W/L	12/2.4	4/2.4	4/2.4	4/2.4
g_m	$100\mu S$	$140\mu S$	$140\mu S$	$140\mu S$

Table 1. Transistor parameters for class A conveyor. Transistor channel width W and channel length L are given in μm.

Transistor	M1	M2	M3	M4	M5
W/L	80/2.4	80/2.4	12/2.4	12/2.4	240/2.4
g_m	$160\mu S$	$160\mu S$	$35\mu S$	$35\mu S$	$160\mu S$
Transistor	M6	M7	M8	MSS1	MSS2
W/L	240/2.4	4/2.4	4/2.4	12/12	4/12
g_m	$160\mu S$	$35\mu S$	$35\mu S$	$12\mu S$	$12\mu S$

Table 2. Transistor parameters for class AB conveyor. Transistor channel width W and channel length L are given in μm.

Thus, the achievable signal to noise ratio is proportional to $i_{z,max}$.

With a class AB design as shown in fig. 7 we have an expression similar to (17) for the noise output. With this design, however, the maximum output current may exceed the bias current, so the maximum signal output swing is no longer limited by the bias current but rather by the maximum current available from the current mirrors within the limitations of the supply voltage. Thus, the class AB design provides an increased degree of freedom in the optimization of the noise performance.

To illustrate this, both a class A conveyor and a class AB conveyor corresponding to figs. 6 and 7, respectively, have been designed and simulated in an industry standard $2.4\mu m$ CMOS technology. The conveyors have been designed for a supply voltage of $V_{DD} = -V_{SS} = 2.5V$ and have been designed for a maximum output current of $|i_{z,max}| = 100\mu A$. For the class A design, the bias current is selected to $100\mu A$ and for the class AB design, the bias current is selected to $5\mu A$. The transistor geometries are listed in Tables 1 and 2. With these designs, the simulated output noise currents (with a voltage drive to the Y-input and a current drive to the X-terminal) were $2.8pA/\sqrt{Hz}$ and $1.2pA/\sqrt{Hz}$, respectively. These values correspond closely to the values calculated from (17) and (18) and the similar set of equations for the class AB design and confirm the analytical results.

7. CONCLUSION

We have established a general current conveyor noise model and applied this model to opamp configurations based on current conveyors. This analysis shows that a current feedback opamp has the potential for a very low equivalent input noise voltage but that the inverting input noise current will exceed that of a voltage opamp built from similar conveyor structures.

We have also in detail studied the noise sources in a CMOS implementation of a current conveyor, and we have found that an essential consideration in the noise minimization of such a conveyor is the design of low noise bias current sources and current mirrors, i.e. low-g_m structures in combination with a high-g_m structure for the X-input stage and the Y to X level shifter stage. Also, the choice of a class AB configuration has been shown to alleviate some of the design compromises which cannot be avoided in a class A configuration.

REFERENCES

[1] K. C. Smith and A. S. Sedra, "The current conveyor – a new circuit building block," *Proc. IEEE*, vol. 56, pp. 1368-1369, Aug. 1968.

[2] A. S. Sedra and K. C. Smith, "A second generation current conveyor and its applications," *IEEE Trans. Circuit Theory*, vol. CT-17, pp. 132-134, Feb. 1970.

[3] C. Toumazou, F. J. Lidgey, and D. G. Haigh (Ed.), *Analogue IC design: the current mode approach*, Peter Peregrinus Ltd. on behalf of IEE: London, UK, 1990.

[4] M. Steffes, "Noise analysis for Comlinear's op amps," Comlinear Application Note OA-12, 1990 (in Comlinear Corporation 1991 Data Book).

[5] K. R. Laker and W. M. C. Sansen, *Design of analog integrated circuits and systems*, pp. 591-595, McGraw-Hill Inc.: New York, USA, 1994.

[6] A. F. Arbel, "Comparison between the noise performance of current-mode and voltage-mode amplifiers," *Analog Integrated Circuits and Signal Processing*, vol. 7, pp. 221-242, May 1995.

[7] A. Fabre, "Third generation current conveyor: a new helpful active element," *Electron. Lett.*, vol. 31, pp. 338-339, March 1995.

[8] E. Bruun, "A combined first- and second-generation current conveyor structure," *Int. J. Electron.*, vol. 78, pp. 911-923, May 1995.

[9] E. Bruun and O. H. Olesen, "Conveyor implementations of generic current mode circuits', *Int. J. Electron.*, vol. 73, pp. 129–140, July 1992.

[10] E. Bruun, "CMOS Current Conveyors," pp. 632-641 (Chapter 11.5) in: C. Toumazou, N. Battersby and S. Porta (Ed.), *Circuits & Systems Tutorials*, LTP Electronics on behalf of IEEE ISCAS'94: London, UK, 1994.

Authorized licensed use limited to: Danmarks Tekniske Informationscenter. Downloaded on March 02,2010 at 07:33:13 EST from IEEE Xplore. Restrictions apply.