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Published in:
Proceedings of the IEEE International Symposium on Circuits and Systems

Link to article, DOI:
10.1109/ISCAS.1996.539988

Publication date:
1996

Document Version
Publisher's PDF, also known as Version of record

A LOW-NOISE/LOW-POWER PREAMPLIFIER FOR CAPACITIVE MICROPHONES

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ABSTRACT

A design for a microphone preamplifier for application in hearing aids is presented. The amplifier operates at a supply of 1-1.5V, the current drain is 40μA. The maximum sound level allowed is more than 120 dB SPL (Sound Pressure Level), with a typical noise level of 25 dB(A) SPL (A-weighted). The amplifier is optimized for a capacitive microphone with a capacitance of 1.2pF. The amplifier is fully integrated in a 0.7μm n-well CMOS technology . Design details concerning noise performance are analytically described.

1. INTRODUCTION

Current capacitive microphones for hearing aids use an electret design for the microphone.An electret microphone represent a capa-citive source for the preamplifier. Due to the low frequencies involved, the fact that microphones is miniaturized and source capacitance is diminishing, a need for preamplifiers with a very low noise current is needed. Thus achieving acceptable signal to noise ratios. In traditional designs, a junction FET in a source follower configuration is used to buffer the signal from the microphone. Due to gate leakage current and the relatively low value of the bias resistor (1-10GΩ) the noise from a junction FET source follower can not be decreased. The value of the bias resistor can not be enlarged, because the leakage current imposes an upper bound. Other disadvantages of a junction FET source follower are, poor PSRR (Power Supply Rejection Ratio) and low output swing. In order to lower the noise current of the preamplifier, MOSFETS which show a negligible gate leakage current, can be used. Two zero biased diodes can then be used as bias resistors, obtaining very large equivalent bias resistance and at the same time serve as protection diodes. Based on this, a fully integrated preamplifier can then be designed to obtain a superior PSRR and full output swing. Traditional design obtain noise level of 27 dB SPL and maximum sound level of 110 dB SPL. PSRR in traditional design is no more than 30dB.

Others have designed integrated preamplifiers for electret microphones [6,8]. So far no solution has been presented that could compete with the ordinary junction FET source follower addressing SNR (Signal to Noise Ratio).

2. AMPLIFIER TOPOLOGY

An electret microphone (Fig.1) consists of a capacitor which is charged by a permanent electric field. One off the capacitors plates acts as a diaphragm. The microphone can be represented as a voltage generator V_{mic} and a capacitor C_{mic} in series. The amplitude of the voltage generator is proportional to the incoming sound pressure. The proportionality constant, normally denoted the sensitivity, is usually in the range 5mV/Pa-20mV/Pa. The sensitivity used everyvere in this paper is 15.8mV/Pa.

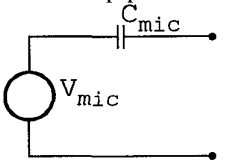

Fig. 1. Equivalent circuit for an electret microphone.

The amplifier topology used is a Differential Difference Amplifier (DDA) [5,9]. The amplifier topology is showed in Fig. 2 where C_{mic} is the capacitance of the microphone, C_p is the parasitic bonding capacitance and C_f is the feedback capacitance. The small signal resistance of the parallel diodes is denoted R_{diodes}. And last the V_{ref} is used to set the DC voltage level at the output. A block diagram of the DDA is showed in Fig. 3.

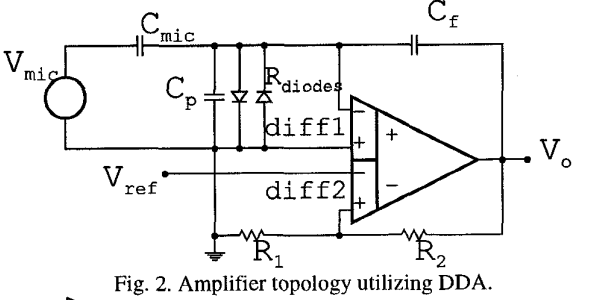

Fig. 2. Amplifier topology utilizing DDA.

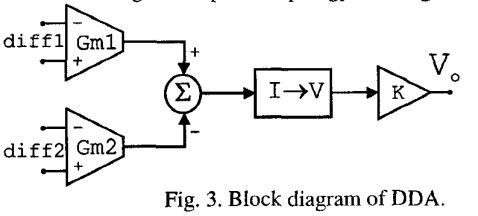

Fig. 3. Block diagram of DDA.

The DDA consist of two V→I converters (diff1 and diff2), a I→V converter and a gain k. Transconductances of diff1 an diff2 is denoted Gm1 and Gm2. Below the unity gain frequency of the DDA the transfer function from V_{mic} to V_o can be calculated to :

$$A_{in}(s) = \frac{V_o}{V_{in}} = -\frac{C_{mic}}{C_f}\frac{1}{1+\eta}\frac{s}{s+\omega_o\frac{\eta}{1+\eta}} \qquad (1)$$

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And from V_{ref} to V_o :

$$A_{ref}(s) = \frac{V_o}{V_{ref}} = (1+\frac{R_2}{R_1})\frac{\eta}{1+\eta}\frac{s+\omega_o}{s+\omega_o\frac{\eta}{1+\eta}} \qquad (2)$$

Where

$$\omega_o = \frac{1}{R_{diodes}(C_{mic}+C_f+C_p)} \quad \text{and} \quad \eta = \frac{1+\frac{C_{mic}}{C_f}}{1+\frac{R_2}{R_1}}\cdot\frac{Gm2}{Gm1}$$

We see that it is desirable if $\eta \ll 1$. Then $A_{in}(s)$ equals the gain of a charge amplifier. And the gain $A_{ref}(s)$, will be very small above ω_o. $\eta \ll 1$ can be obtained by $C_{mic}/C_f \ll R_2/R_1$ and Gm2 « Gm1.

3. LOW-NOISE DESIGN OF INPUT STAGE

3.1. Configuration

The input stage chosen is a standard differential stage. The input stage corresponds to diff1 in the DDA. A differential stage is not the optimum choice for a low-noise design [2] but in this case it is convenient because the DC common mode voltage value, at the input diff1, can be set arbitrarily. In our case it is grounded. This would not have been possible with any other type of input stage.

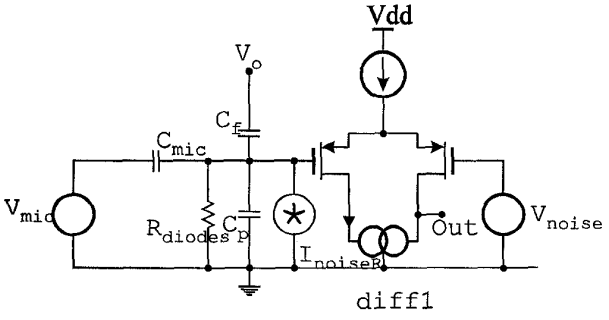

Fig. 4. Input stage configuration.

The noise from the input stage is represented by the noise voltage V_{noise} . This represents thermal noise and 1/f noise from the input stage. The bias resistor generated noise is represented by I_{noiseR}. We will in the following only consider frequencies above $1/2\pi C_{mic}$. In order to calculate the SNR we will refer the noise to the input. this can be calculated to :

$$V_{neqi}^2 = I_{noiseR}^2\frac{1}{(\omega\cdot C_{mic})^2} + V_{noise}^2\left(\frac{C_{mic}+C_p+C_f}{C_{mic}}\right)^2 \qquad (3)$$

In our case this noise voltage should be weighted by the A weighting function in order to obtain the SNR(A). The A weighting function is showed in Fig. 5. Input transistors are assumed to operate in weak inversion, possibly moderate inversion as resent measurements show that noise in PMOS transistors is due to mobility fluctuations and not carrier number fluctuations [1,7]. Therefore they should preferably be biased in strong inversion. If possible.

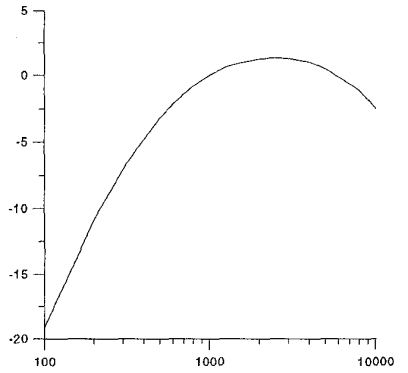

Fig. 5. A-Weighting Curve (-20dBre20μPa to +5dBre20μPa and 100Hz to 10kHz).

3.2. Minimisation of Input Transistor Noise

The noise from the input stage can be divided into three noise sources. Bias resistor white noise, white noise of input transistors and 1/f noise of input transistors. We will refer these to the input. First we define the following :

C_{ox} : Thin oxide capacitance pr. square.
I_d : MOST (MOS transistor) drain current.
K : Boltzmans constant $1.38\cdot10^{-23}$.
K_f : MOST 1/f noise parameter.
K_p : Transconductance parameter MOST.
L : MOST channel length.
L_d : Underdiffusion length.
T : Temperature in Kelvin.
V_t : KT/q = 26mV @ T=300°K.
W : MOST channel length.

3.2.1. Bias resistor generated noise

$$V_{neqiBiasres}^2 = \frac{4KT}{R_{diodes}}\frac{1}{(\omega\cdot C_{mic}))^2} \qquad (4)$$

As we see the noise from the bias resistor is moved to lower frequencies as the resistor gets larger. So it is advantageous that the bias resistor is as large as possible. The best way of implementing very large resistors onchip is to implement them as junction diodes. Two zero biased diodes will be as noisy as resistor with the Value of :

$$R_{diodes} = V_t/(2I_{leak}) \qquad (5)$$

Where I_{leak} = 10fA for a minimum diode. This gives us at theoretically value of $R_{bias} = 1.3T\Omega$.

3.2.2. Transistor generated thermal noise

For the input referred transistor generated thermal noise, there exist an optimal gate area. This gate area gives minimal transistor generated thermal noise.

It is located at :

$$WL = \frac{C_p + C_{mic} + C_f}{C_{ox}\alpha} \text{ , Where } \alpha = 1 + 9L_d/2L. \quad (6)$$

And the minimal input referred transistor generated thermal noise is :

$$V^2_{neqitherm\,\min} = 4KT\frac{4}{3}\frac{L}{\sqrt{2I_dK_p}} \cdot \sqrt{\frac{C_{ox}\alpha}{C_p + C_{mic} + C_f}}\left(\frac{4}{3}\frac{C_{mic} + C_p + C_f}{C_{mic}}\right)^2 \quad (7)$$

3.2.3. Transistor generated 1/f noise

Again there exists a minimum. This is located at :

$$WL = 3\frac{C_p + C_{source} + C_f}{C_{ox}\alpha} \quad (8)$$

And the value associated with this minimum is :

$$V^2_{neqi1/f} = \frac{4}{3}\frac{1}{f}\frac{K_f\alpha}{K_p}\frac{(C_{mic} + C_p + C_f)}{C^2_{mic}} \quad (9)$$

3.3. Optimizing for lowest noise

As we see from equation 6 and 8, there exists two different optimal gate areas, where the thermal respectively the 1/f noise is minimal. The gate area for minimal 1/f noise is three times larger than the gate area for minimal thermal noise. The noise corner frequency of the input transistors determines which gate area should be chosen. In this design, the noise corner is placed at a fairly low frequency. So I have chosen gate area for minimal thermal noise. Normally one would have to use numerically optimization using SPICE. But as SPICE MOST models underestimates thermal noise in moderate inversion this solution is not accurate. One solution is to use the EKV (Enz- Krummenacher- Vitoz) MOST model [3].

3.4. Minimisation of Total Noise

The total noise from the amplifier consist of contributions from the input transistors and from all other transistors. Having minimized noise from input transistor one should assure that contributions from all other transistors are negligible to those of the input transistors. This is easily done, keeping in mind, that the transconductance g_m of the input transistors should be larger than all other transistors. Input transistors gatelengths should be shorter than all other transistors.

4. OVERALL DESIGN

The schematic of the amplifier is showed in Fig. 6. It consists of 5 sections. A current reference [4], input stage (Diff1), bias input stage (Diff2), folded cascode and last a single transistor output stage. This configuration has been chosen because of its ability to operate at very low voltages. The current reference is a standard current reference with the two PMOS transistors operating in weak inversion [4]. Input stage Diff1 is operated at a larger current than Diff2. This is to reduce noise and assure a total gain close to C_f/C_{mic}. The cascodes are operated close to V_{ss}. This is to assure that Diff1 can handle voltages as low as V_{ss} on its input. Output stage is a single transistor biased by a current generator and millercompensated by a capacitor. Bias input stage (Diff2) is connected to V_{dd} and Out. Resistors are chosen in such a way that the bias voltage at the output always is $V_{dd}/2$. Last the input is biased by two diodes of minimum size. This is two assure the best SNR possible. These diodes serve as ESD protection diodes also.

5. EXPERIMENTAL RESULTS

The amplifier has been integrated with a 1.2pF capacitance simulating the microphone capacitance. Another version without the 1.2pF capacitance is being fabricated unbonded. This version is supposed to be bonded to a commercial electret microphone. At the moment only measurements on the version with a capacitance of 1.2pF has been performed.

5.1. Static Measurements

It has been verified that the amplifier can operate at a supply voltage of 1V-1.5V. The current drain was simulated to 30µA and measured to 36µA -40µA. The measured outputsving is approx. $0.5V_P$ at a supply voltage of 1.5V. This corresponds to a maximum input sound level of more than 120 dB SPL.

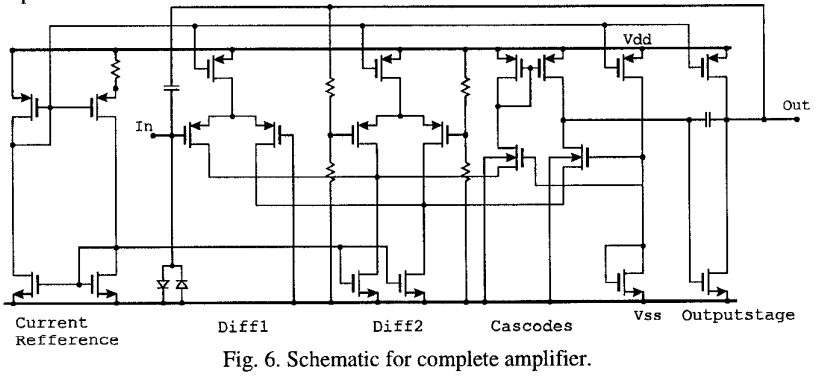

Fig. 6. Schematic for complete amplifier.

5.2. Dynamic Measurements

During the test of the amplifier it was noticed that when the amplifier was overloaded it saturated and returned to normal operation very slowly. This saturated state may last for several minutes. This can be explained as follows. When the amplifier is saturated, then the high impedant node at the input is charged. The only current discharging the node, is the leakage current of the bias diodes. As this current is very small, the discharging may take some time. Furthermore the dc gain from the high impedant node to the output is very large (approx. 300 times). This worsens the saturation problem. A solution is to enlarge the biasing diode leakage current a little, and to decrease the DC gain from the high impedant node to the output.

Gain has been measured to 2.96 ~ 9.42dB @ 1kHz.. This was simulated to 3.03 ~ 9.63dB @ 1kHz. Fig. 8 shows the measured gain A_{mic} as a function of the frequency. The peak located at 300kHz is due to capacitive loading of 100pF(cables).

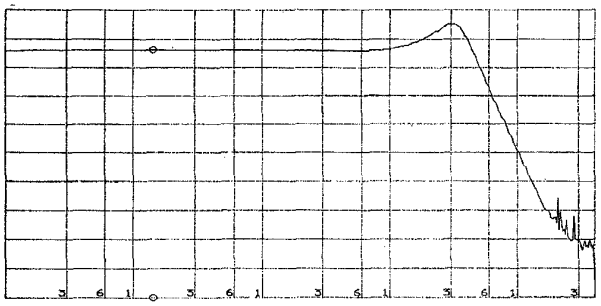

Fig. 8. Measured gain A_{mic} (dB) as a function of frequency. Frequency : 100Hz to 4MegHz. 5dB/div. Gain = 9.42dB @ 1khz.

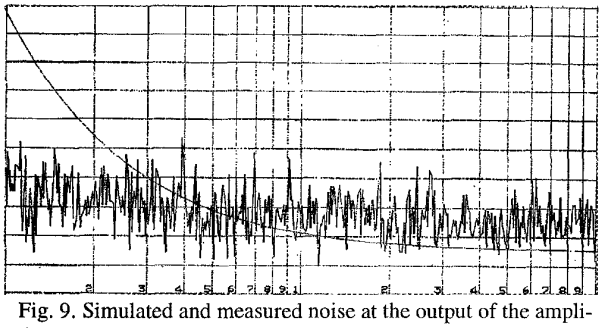

Fig. 9. Simulated and measured noise at the output of the amplifier. Frequency: 100Hz to 10kHz. Scale : 0nv to 800nv(Rms).

The noise at the output of the amplifier has been measured and simulated (fig. 9). This is worth a notice. The white noise level is approx. 6dB higher than simulated. It is at the moment not clarified why this disproportion exists. Some of the transistors are biased in moderate inversion and as SPICE overestimates the transconductance in this area, this might explain some of the difference between measurements and simulation. Simulation has to be done using the EKV MOST model [3]. This has not yet been done as this model level not is an integrated feature of SPICE.

The low frequency noise is much lower than expected. This is quite surprising. The noise corner is situated at a very low frequency (approx. 40Hz). This is though, only based on measurements from 10 samples of a single run. So while white noise is larger than expected the low frequency noise is smaller. The total noise level was simulated to 24B(A) SPL. And it was measured to 25dB(A).The frequency range was 100Hz to 10Khz.

6. CONCLUSION

A preamplifier optimized for capacitive microphones with a very low source capacitance has been presented. It utilizes a new design. A DDA is used to amplify the signal from the microphone. Expressions for optimal gatearea concerning noise are given. The preamplifier is implemented in a CMOS 0.7μm technology. Noise measurements differs from the simulations. White noise is larger and low frequency noise is smaller. This has not yet been explained. The total measured noise level is equivalent to 25dB(A) SPL. This compared with the maximum sound level allowed of more than 120 dB SPL gives us a dynamic range of 95dB at a supply voltage of 1.5V.

7. ACKNOWLEDGEMENTS

Claus Erdmann Fürst acknowledges the Ph.D. scholarship granted by the Danish Technical Research Council. The work described was supported by a contract with Microtronic A/S, Denmark.

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