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A 2.5 Gb/s GaAs ATM Mux Demux ASIC

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Abstract — This paper describes the design and implementation of a high speed GaAs ATM Mux Demux ASIC (AMDA) which is the key element in a high speed ATM Add-Drop unit. This unit is used in a new distributed ATM multiplexing-demultiplexing architecture for broadband switching systems. The Add-Drop unit provides a cell based interface between networks/systems operating at different data rates, the high speed interface being 2.5 Gb/s and the low speed interface being 155/622 Mb/s. Self timed FIFOs are used for handling the speed gaps between domains operating at different clock rates, and a Self Timed At Receiver's Input (STARI) interface is used at all high speed chip-to-chip links to eliminate timing skews. The AMDA demonstrated operation above 4 Gb/s (500 MHz clock frequency) with an associated power dissipation of 5 W.

I. Introduction

Asynchronous Transfer Mode (ATM) is selected as the technology for future integrated broadband switching networks. Today, ATM networks operating at 155 Mb/s are commercially available, and in the near future 622 Mb/s and 2.5 Gb/s networks will appear [1]. This evolution scenario requests new interface techniques in order to link the lower speed ATM networks (155/622 Mb/s) to the high speed ones.

This paper describes the design and implementation of a high speed GaAs ATM Mux Demux ASIC (AMDA) which is the central component in a proposed high speed distributed ATM add-drop architecture for broadband switching networks [2]. The primary objective of the add-drop unit is to provide access to a high speed network/system (2.5 Gb/s) from lower speed ones (up to 622 Mb/s), e.g. as illustrated in Fig. 1. The first add-drop unit in a string of add-drop units generates a slotted cell stream, which is transmitted along the string, while succeeding add-drop units either regenerate or modify the individual cell slots. High speed local area networks and switches can be realised using this add-drop unit as well.

The distributed nature of the add-drop unit provides for easy scalability, i.e. additional nodes can be added without the need for changes in the rest of the system. Only in case the total bandwidth of the lower speed interfaces exceed the bandwidth of the high speed link (2.5 Gb/s), a Media Access Control (MAC) protocol must be applied.

The high speed interface is 2.5 Gb/s, while the lower speed interface is 155/622 Mb/s. The add-drop unit is therefore naturally separated into two different clocking domains - a high speed domain operating at 311.04 MHz used for processing the 2.5 Gb/s data rates (8 bit parallel), and a lower speed domain operating at 19.44/77.76 MHz used at the 155/622 Mb/s. The actual implementation of the add-drop unit reflects this separation between clocking domains as shown in Fig. 2.

The AMDA constitutes the high speed domain and implements all the very high speed transmission related functions, while the Auxiliary component(s) provides the high complexity functions and buffering required in the low speed domain. The AMDA is implemented in GaAs DCFL technology, while the Auxiliary component(s) is most appropriately implemented using CMOS technology. The following description only concerns the AMDA.

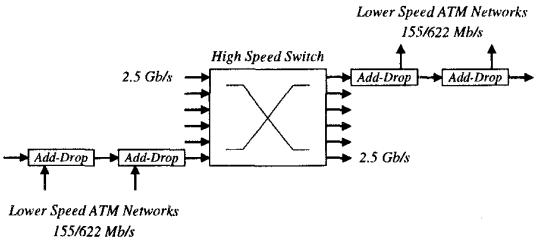

Fig. 1. Distributed ATM multiplexer-demultiplexer architecture.

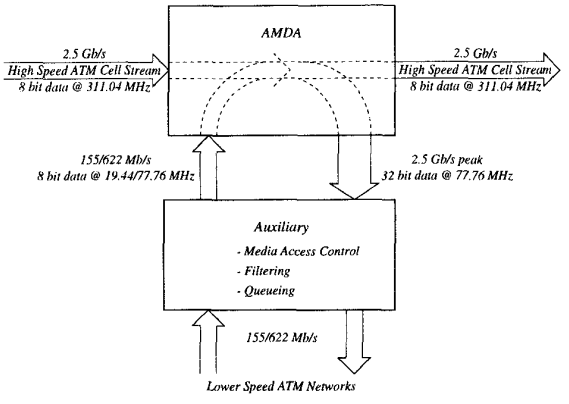

Fig. 2. Functional block diagram of add-drop unit.

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II. Architecture

The overall architecture of the AMDA chip is shown in Fig. 3, illustrating the five main modules: Input, Mux, Demux, Output, and Internal Access module.

A. Input module

The Input module provides a phase independent interface between the incoming high speed data stream (including associated clock) operating at 2.5 Gb/s, i.e. 8x311.04 Mb/s, and the internal high speed system clock. This type of interface is an important feature of the AMDA, since problems associated with chip-to-chip timing skew are completely eliminated. In a typical application such as the multiplexer-demultiplexer architecture, a large number of AMDA chips will have to be interconnected across one or more PCBs. In such applications considerable timing skew is inevitable, since signal propagation is comparable to the clock cycle time (3.2 ns).

The input module also features some primitive Operation and Maintenance (OAM) capabilities. It checks that the incoming data stream represents a continuos flow of ATM cell slots each being 53 bytes long. Furthermore, the ATM cell flow is divided into frames separated by OAM cells carrying information about the number of cells in the frame, and the parity calculated over the entire frame whereby cell loss and bit errors can be monitored. This monitoring is also handled by the Input module.

B. Mux module

The Mux module manages the actual interface between the lower speed (155/622 Mb/s) upstream data path, and the high speed (2.5 Gb/s) data path. In order to handle the speed gab between the upstream path and the high speed path, a self-timed one cell FIFO buffer is used. Due to the self-timed nature of such a buffer, writing and reading from the buffer can be performed at different speeds, and at high speed as well. The latter because only local control/communication is required between neighbouring storage elements, providing very small internal loads and compact and regular layout.

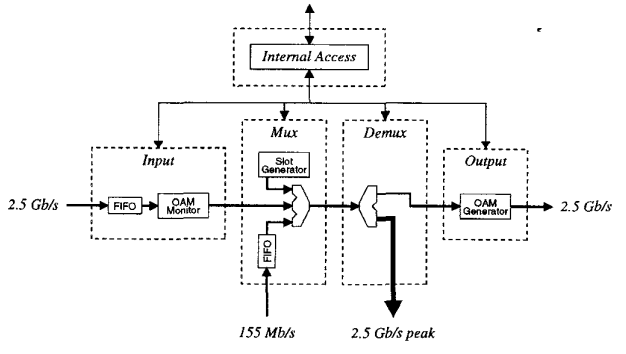

Fig. 3. Architecture of AMDA.

The Mux module also contains a slot generator, which generates a continuos flow of empty ATM cell slots (including OAM slots). This feature is required for string topologies such as the multiplexer-demultiplexer architecture. The first AMDA in a string of add-drop units generates a slotted cell stream, which is transmitted along the string.

C. Demux module

The Demux module implements the drop function, thus interfacing between the high speed data path and the low speed downstream data path. An 8 bit address with optional masking is used for filtering out the ATM cells to be dropped (more refined filtering is performed in the Auxiliary component(s)). Extracted cells are replaced by empty cell slots on the high speed data path, unless the cell is a multicast or broadcast cell.

The peak data rate on the downstream data path is 2.5 Gb/s (in case all cells on the high speed data path are destined for this add-drop node). In order to reduce the electrical bandwidth of this interface, a 32 bit interface is used in the downstream data path.

D. Output module

The Output module is in principle equivalent to the OAM block in the Input module, i.e. it calculates the parity and cell count over the transmission frame, and insert the information in the dedicated OAM cells. This information is used by the Input module of the succeeding AMDA for monitoring the transmission on the high speed data path.

E. Internal Access module

The Internal Access module provides a low speed (e.g. 2 MHz) serial interface between the internal control registers of the AMDA and an external control entity (e.g. a PC). This interface is used for initialising the AMDA, e.g. programming the address filter, and for conveying OAM information between the Input module and the external control entity.

III. Implementation

The AMDA chip is implemented using GaAs DCFL technology, because of its favourable speed-power figures compared to other high-speed technologies (e.g. ECL). Since ECL/TTL interfaces are required, a minus 2 V power supply is used for the internal logic and the ECL I/O buffers, and a positive 5 V power supply for the TTL I/O buffers.

Most of the blocks in the AMDA is implemented using traditional synchronous pipelined design style except for two key blocks; the input FIFO buffer in the high speed data path, and the FIFO cell buffer in the low speed upstream data path.

In order to avoid problems associated with timing skew, the high speed data path (including an associated clock) is retimed at the input of each AMDA using a technique called Self-Timed At Receiver's Input (STARI) [3]. Fig. 4 shows a STARI interface. STARI assumes that the transmitter and receiver operates at the same clock frequency while the clock phases can be arbitrary and independent in time. The key component of STARI is a self-timed FIFO (in this implementation based on a high speed self timed FIFO [4]) placed at the receiver's input. During one clock cycle, the transmitter inserts one datum in the FIFO, which ripples to the end of the FIFO asynchronously. Likewise, the receiver reads one datum from the FIFO. Thus in steady state, one datum is inserted and one datum is removed from the FIFO in each cycle assuming that the FIFO can complete each insert and remove operation within one clock cycle. Once properly initialised (FIFO app. half-filled), this prevents the FIFO from overflowing or underflowing, and the data path is retimed.

The speed gap between the upstream low speed data path and the high speed data path is managed by a self timed FIFO buffer including write and read control logic as illustrated in Fig. 5. In principle writing and reading from the FIFO can be performed completely asynchronously, but in this implementation, the write clock operates at one fourth (622 Mb/s) or one sixteenth (155 Mb/s) the system clock.

The multiplexing cycle is as follows. The auxiliary component (see Fig. 2) writes an ATM cell into the self timed buffer via the upstream data path. The AMDA then waits for permission from the MAC (located in the auxiliary component) to insert the cell into the high speed cell flow. Once this permission is granted, the ATM cell contained in the FIFO is inserted in the first empty cell slot on the high speed data path. The AMDA then informs the auxiliary components, that the Mux module is ready to receive a new ATM cell, which completes the multiplexing cycle.

Since the data exchange between neighbouring storage elements in the FIFO buffer is characterised by local control/communication, the internal loads are very small and the layout very compact and regular, thus feasible for high speed operation contrary to a static RAM implementation.

IV. Fabrication

The AMDA is fabricated in a standard 0.8 µm E/D MESFET process [5] at Vitesse Semiconductor Corp. A full-custom approach was applied to fully exploit the speed and power potential of the technology, and in order to save area. Basic gates, flip-flops and I/O circuitry was optimised using HSPICE, and the chip was layed out manually using MAGIC.

The AMDA contains app. 30k transistors on a 3.5x5.5 mm^2 die, and is packaged in a 132 pin LDCC with 89 signal pins and 43 power pins. A plot of the chip is shown in Fig. 6.

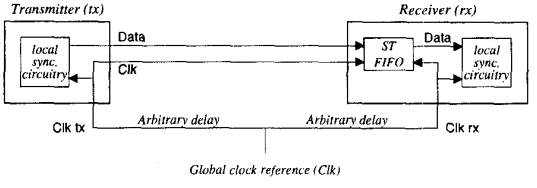

Fig. 4. STARI interface.

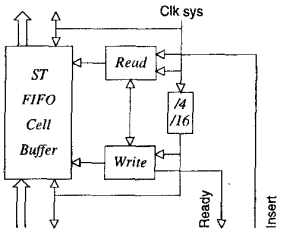

Fig. 5. Self timed FIFO cell buffer.

V. Performance

In order to evaluate the performance of the AMDA, a test PCB with two add-drop units in a distributed multiplexing-demultiplexing architecture was developed. The auxiliary functions of the add-drop unit, i.e. enhanced buffering, media access control and refined filtering were implemented using standard components and FPGA technology. The 155 Mb/s interfaces were prepared for ITU and ATM forum standards as well as for in-house ATM test equipment. An RS-232 PC interface was used for accessing the Internal Access module of the AMDA. A schematic block diagram of the testbed is shown in Fig. 7. The testbed can be extended to include more add-drop units by connecting several PCBs via high speed connectors and coaxial cables.

A 155 Mb/s ATM cell flow was connected to the upstream (add) port of the first add-drop unit, and extracted on the downstream (drop) port of the second add-drop unit. Error free transmission of ATM traffic across the distributed

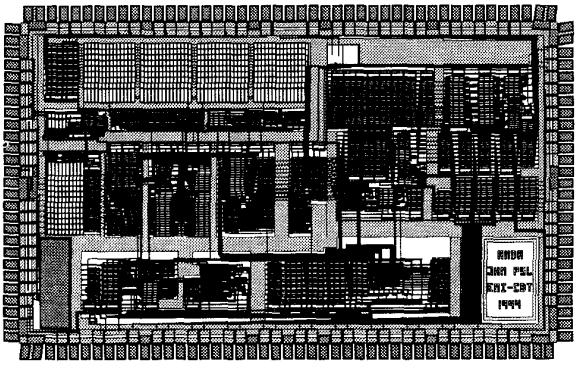

Fig. 6. Plot of the AMDA chip.

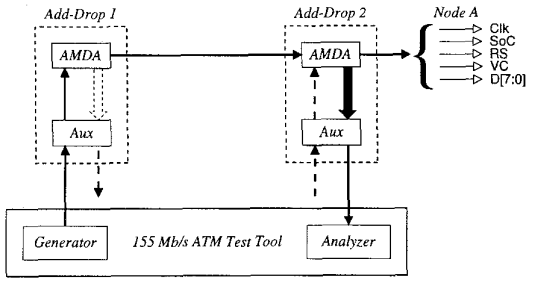

Fig. 7. Block diagram of testbed.

multiplexer-demultiplexer was verified at data rates up to 2.7 Gb/s on the high speed ATM data path, corresponding to a system clock frequency of 340 MHz. However, the maximum frequency of operation of the add-drop unit was limited by the auxiliary circuitry in the downstream data path which operates at one fourth the system clock frequency. The AMDA itself demonstrated operation above 500 MHz (4 Gb/s) with an associated power dissipation of 5 W.

A sample of signals on the high speed data path (node A) during transmission of ATM cells at the target transmission rate (2.5 Gb/s) is shown in Fig. 8. The top trace is the Start of Cell signal (SoC) indicating the start of each cell slot on the high speed data path. A continuos flow of slots is generates by the first add-drop unit and transmitted through the second unit. The slot period is 170 ns (i.e. 2.5 Gb/s). The second trace is the Reserved Cell signal (RS, active low) which indicates slots that are occupied by OAM cells. OAM cells are transmitted periodically with a period determined by the head-end add-drop unit, i.e. the first add-drop unit. The periodicity is programmable through the Internal Access module, and ranges from 1 to 255 empty slots between each OAM slot. The third trace is the Valid Cell signal (VC, active low), which indicates slots containing ATM cells that

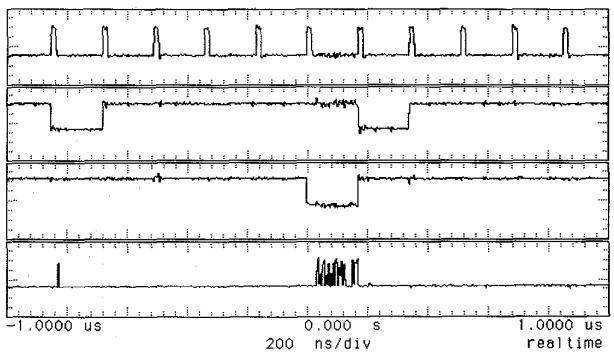

Fig. 8. Sample signals on high speed data path (node A). Traces from top to bottom: SoC, RS, VC, D0.

TABLE I
CHIP SUMMARY

Technology	0.8 µm E/D MESFET
Basic gate topology	DCFL
Chip size	3.5x5.5 mm^2
Transistor count	30k
Power supplies	-2/+5 V
Power consumption	5 W
Max. clock frequency	> 500 MHz (4 Gb/s)

have been multiplexed (added) onto the high speed data path by previous add-drop units, and not yet demultiplexed (dropped) or are multicast/broadcast cells. The last signal (D0) represents one of the eight data bit of the high speed data path. This signal carries data during reserved and valid cells. Table I summarises key figures of the AMDA chip.

VI. CONCLUSIONS

In this paper we have presented the design of a high speed GaAs ATM Mux Demux ASIC (AMDA), which constitutes the key element of an ATM add-drop unit to be used in a distributed multiplexing-demultiplexing architecture. The AMDA provides an easy way of interfacing between 2.5 Gb/s and lower speed ATM networks. The AMDA uses self timed FIFOs to handle the speed gap across interfaces operating at different clock frequencies, and a self timed protocol at all high speed chip-to-chip data links to eliminate problems associated with timing skew. The maximum frequency of operation was above 500 MHz in a standard 0.8 µm GaAs E/D MESFET process supporting a data rate in excess of 4 Gb/s, and with an associated power dissipation of 5 W.

ACKNOWLEDGMENT

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