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5.8 Gb/s 16:1 multiplexer and 1:16 demultiplexer using 1.2 m BiCMOS

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ABSTRACT

High speed time-division multiplexers and demultiplexers are important components of modern optical communication systems. They are needed to parallelize the data to allow most of the system to operate at much lower speeds. This paper describes a 16:1 multiplexer and a 1:16 demultiplexer implemented on one IC in a 1.2μm BiCMOS process. The IC combines fast ECL circuits with CMOS circuits, demonstrating that by utilizing the combination of bipolar and MOS transistors, a VLSI circuit with very high speed interface is feasible.

INTRODUCTION

In high speed optical communication systems multiplexers and demultiplexers are used to reduce the part of the system which must operate at the very high speed of the serial link. Most of the system will process the data several bits in parallel. With the increasing requirements for complex real time processing of the transmitted data that comes with the advanced low level communication protocols, such as ATM (Asynchronous Transfer Mode), the size of the hardware part of the communication system that works directly with the transmitted data increases.

The bipolar and GaAs processes that offer the speed needed in the multiplexers and demultiplexers do not offer the very high levels of integration needed to handle the communication protocol. On the other hand CMOS, which offers the high integration, is capable of operating at the speed (100–400MHz) needed for handling the protocols on parallel data [1], [2], but does not offer the speed needed in the multiplexers and demultiplexers. From this viewpoint an obvious choice would be BiCMOS, which offers both the high speed of bipolar circuits and the high level integration of CMOS circuits.

The choice of a BiCMOS process is not without penalty. The performance of the bipolar transistors in presently available BiCMOS processes is not comparable to that of advanced

R_b	C_{jc}	C_{js}	f_T	β
105Ω	67fF	78fF	7.8GHz	80

Table 1: Typical BJT parameters at $V_{CB} = 1.6V$ and $V_{CS} = 4V$.

bipolar processes. BiCMOS processes with transition frequencies up to 15GHz have been reported [3], [4], while advanced bipolar processes reach transition frequencies of more than 45GHz [5]. But even with these BiCMOS processes both all currently used communication speeds and the next generation (10Gb/s) are reachable.

The process used in the design presented here is not advanced, with an f_T of only 7.8GHz. Table 1 summarizes some of the data for the bipolar transistors with two base contacts and a 1.2μm$\times$10μm emitter. The maximum speed of both the multiplexer (5.8Gb/s) and the demultiplexer (6.9Gb/s), relative to the f_T of the transistors, compares very closely with other published results [5].

MULTIPLEXER ARCHITECTURE

The multiplexer output is not retimed and therefore the clock frequency need only be half the output bit rate, limiting the frequencies that need to be handled when packaging. Figure 1 shows a simplified block diagram of the multiplexer. The stippled line represents the approximate borderline between CMOS and ECL circuits. Inserted in figure 1 the topology of the 2:1 multiplexers is shown. The 2:1 multiplexing is performed by first retiming the two signals from the previous multiplexer, then skewing one of them half a clock cycle, and finally selecting each in turn with the clock signal.

The first column of 2:1 multiplexers contain extra layers of latches to obtain a flip-flop like function for all inputs. These inputs are first latched in CMOS, and then converted to ECL levels in the selector of the first stage. This selector is an
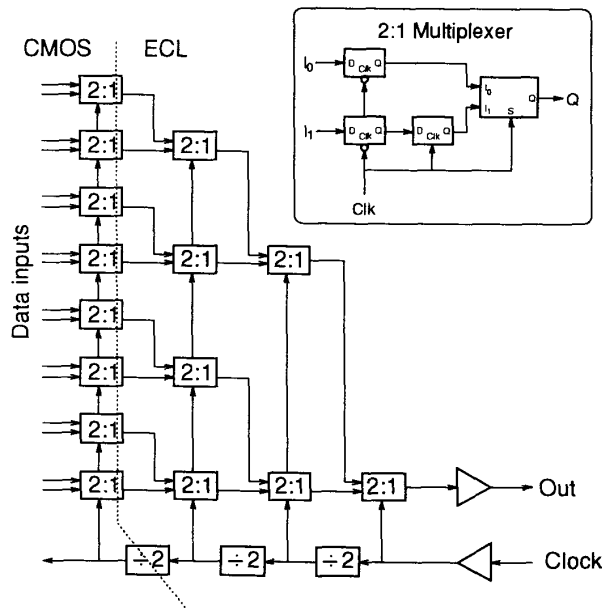
Figure 1: Multiplexer architecture.

MCSL gate (Merged Current Switch Logic) providing both CMOS and ECL inputs, and ECL outputs. The clock divider generating clock signals for this stage has outputs for both CMOS and ECL levels, as the MCSL selector needs ECL levels on the clock inputs. All following stages are implemented fully in ECL.

The maximum speed of the complete multiplexer is determined by the selector in the last 2:1 multiplexer. This selector, the output driver, and the clock input buffer, are the only parts switching at the full clock frequency. 50Ω on-chip termination was used for all high speed inputs and outputs. This has been shown to efficiently reduce reflections and the importance of packaging parasitics as compared to off-chip termination [6].

DEMULTIPLEXER ARCHITECTURE

The demultiplexer consists of a tree of 1:2 demultiplexer blocks with 4 levels as shown in figure 2. The stippled line indicates the borderline between ECL and CMOS circuits. The 1:2 demultiplexers all have the topology shown inserted in figure 2.

The actual demultiplexing is done by leading the input to two latches clocked on opposite edges. An extra latch in one half aligns the signals to have the same phase at the outputs. As both edges of the clock signal are used, a clock frequency of only half the bit rate is needed, as was the case for the multiplexer.

Both the latches in the first 1:2 demultiplexer and in the first clock divider are clocked at the full clock frequency. All other parts of the demultiplexer are clocked at a lower frequency. The maximum input data rate is therefore set by the highest clock frequency that can be applied to a chain of latches. Delaying the clock signal between each level of latches in the input demultiplexer would not improve the speed, as the clock divider still sets the same limit. As for the multiplexer, on-chip termination was used for both data and clock inputs.

GATE DESIGN

Several different logic types are used in the design. For all logic types automatic optimization was used to guide the gate design. To shorten the design time a limited number of speed/power classes of the gates was used. This has of course resulted in excessive power consumption and area.

For the fastest stages of both multiplexer and demultiplexer ECL gates with double emitter followers were used. This allows a reduction of the load on the internal nodes where the conversion from current to voltage signal occurs, and increase the collector–base voltage of following stages. Figure 3 shows a schematic for the fastest selector used in the multiplexer. To reduce the delay in this critical gate, a signal swing of only 300mV was used, compared to the minimum of 400mV used for all other ECL gates. Two weak current sources were added to draw a small current through each of the two top-most current switches, reducing the swing on the common emitter nodes. Where the highest speed was not needed simpler gates
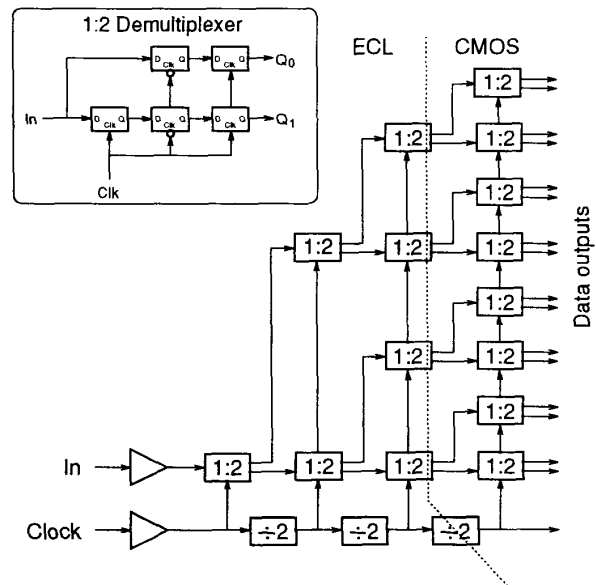

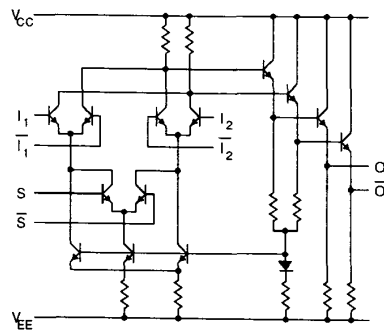Figure 2: Demultiplexer architecture.
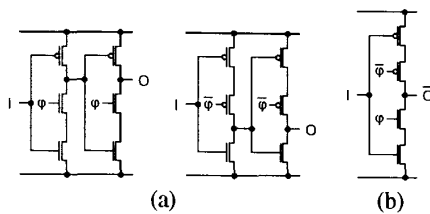
Figure 3: Fast ECL selector

Figure 4: CMOS latches; (a) TSPC latches, (b) two phase latch.

with only one emitter follower was used. Differential signals were used in all the ECL gates.

For most of the CMOS parts the TSPC latches (True Single Phase Clock) shown in figure 4(a) were used. These are examples of a family of CMOS circuits that can work at high speeds using only one clock phase (in this case 360MHz) [7]. Because of the large delay in converting the clock signal from ECL to CMOS signal levels, a latch with a smaller delay and a lower load on the clock signal was needed for the latches just before the conversion to ECL in the multiplexer. This latch, shown in figure 4(b), needs to clock phases. These are easily generated in parallel when converting from ECL to CMOS clock signals, and are only distributed locally with very good control over the setup and hold times of the input signals to these latches.

The conversion from CMOS to ECL signal levels is the fastest and least power consuming of the two conversions involved in the ECL/CMOS interface. It is performed by using an MCSL gate. Figure 5(a) shows the schematic for the MCSL selector · used in this design. It is a simple replacement of some of the bipolar transistors in an ECL gate, with MOS transistors. The speed of this gate is very close to that of the fully bipolar gate.

The conversion from ECL to CMOS signal levels is the weakest part of the ECL/CMOS interface. It is both slow and power consuming. Figure 5(b) shows the schematic for the converter
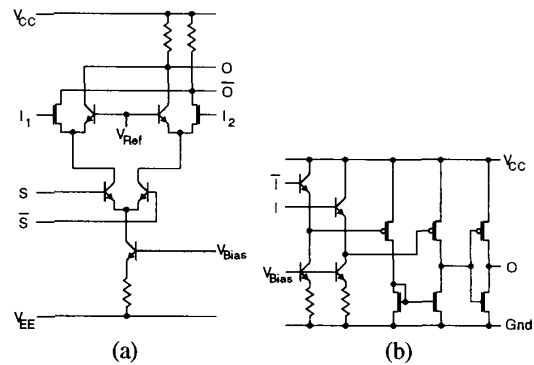

Figure 5: ECL–CMOS interface circuits; (a) MCSL selector, (b) ECL–CMOS converter

used in this design. It is not the fastest configuration, but it is also not the most power consuming. The input comes from an ECL latch with a large output swing of 1.6V. As used in the last clock divider of the multiplexer, it directly drives the last CMOS latch of every input, plus a driver, which in turn drives the rest of the CMOS latches. This approach is only feasible for very small circuits. For large circuits an efficient approach could be to buffer the converted signal heavily, then reconvert to ECL and use a phase lock to adjust the phase of the buffered CMOS signal to be very close to the ECL clock signal.

SIMULATED PERFORMANCE

For simulations a single ended clock signal with a sinus waveform and a peak to peak amplitude of 800mV was use for both multiplexer and demultiplexer. When fabricated, the IC's will be packaged in multilayer ceramic packages with 50Ω transmission lines from the package bond pad to the package lead. To take into account mounting parasitics, a die bond pad capacitance of 50fF, a bonding wire inductance of 2n, and a package bond pad capacitance of 1p were added to all inputs and outputs.

Spice simulations under typical conditions predict that at 5.8Gb/s the minimum output amplitude of the multiplexer is only reduced by 15%. The demultiplexer is simulated to work up to 6.9Gb/s with a 400mV swing and 140pS rise time on the data inputs.

Table 2 lists the power consumption in various parts of the design. The clock dividers are included in the stage they drive.

CONCLUSIONS

The design presented here combines very high speed bipolar circuits with high speed CMOS circuits, demonstrating that very high speed on-chip bipolar interfaces to CMOS circuits

	Multiplexer	Demultiplexer
Fast	970mW	370mW
•	320mW	270mW
•	250mW	490mW
Slow	370mW (240mW)	230mW (140mW)
Total	1.91W	1.36W

Table 2: Power consumption. Numbers in parenthesis are without ECL I/O buffers.

may be constructed using present BiCMOS technologies. The power consumption is comparable to other bipolar designs designed for the highest possible speed. To really utilize the high integration capability of the CMOS, an IC might need several high speed inputs and outputs. This puts some constraints on the available power for each high speed interface. But as the power consumption can be reduced drastically when just reducing the speed slightly, a single IC with several 2.5Gb/s inputs and outputs is possible even in the process used in this design. With the more advanced $0.8\mu m$ and $0.5\mu m$ BiCMOS processes, IC's with several inputs and outputs a 5Gb/s or more would be possible with reasonable power consumption. With the present technologies BiCMOS circuits can not replace pure bipolar circuits at the speeds of the future generations of optical communication systems. But BiCMOS circuits could have an important place in communication systems at speeds from 500Mb/s to 10Gb/s.

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