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SWITCHED CURRENT MICROPOWER 4th ORDER LOWPASS / HIGHPASS FILTER

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Abstract

This paper describes a 4th order lowpass / highpass Butterworth filter implemented in switched current technique. The filter has been designed for low power operation. A prototype implementation has been made and it operates with supply voltages down to 2V and with a total supply current of 211μA at a sampling rate of 50kHz. The chip includes a clock-generator, three current-followers, sample-and-hold and two 4th order filters. The sampling frequency is restricted to approximately 50kHz and the ratio between sampling frequency and cutoff frequency is 12.5. The dynamic-range was found to be 49dB for the highpass section and 58dB for the lowpass section, with a peak signal current of 750nA. The area of the chip core is 1.33mm^2.

I. Introduction

Traditionally, analog sampled data systems have been implemented in switched capacitor technology [1]. Switched capacitor circuits require operational amplifiers and floating linear capacitors, for implementing most of the basic building blocks such as integrators, differentiators, amplifiers etc. This makes it difficult to implement switched capacitor circuits in standard digital CMOS processes. Capacitor ratios are used to determine gain and time constants. The accuracy is therefore limited by matching of capacitors, which can be made as tight as 0.1%. Very low power operation is possible by operating the operational-amplifiers in weak inversion.

By the use of switched current technique [2,3,4] it is now possible to implement analog sampled data systems without the need for operational amplifiers and linear floating capacitors. Therefore, switched current circuits may be implemented in traditional digital CMOS-processes without the need for special process steps. Furthermore, switched current circuits normally occupy less chip area than switched capacitor circuits, because they don't need operational amplifiers. Gain and time constants are determined by transconductance ratios, and the accuracy depends on matching of MOS transistors.

A 4th order lowpass / highpass Butterworth filter, intended for use in a low voltage and low power application (hearing aid), has been realized in switched current technique by applying bilinear Z-transform to an analog prototype filter. The circuit was implemented in an industry standard analog 2.4μm CMOS process.

The filter described in this paper includes an on-chip clock-generator, three current-followers, a sample-and-hold, and a 4th order lowpass and highpass filter. Current copier cells [3, chap.11] are used as storage elements. This results in high accuracy because there is no need for matching of components. Current mirrors are used to perform current scaling, for realizing filter coefficients. Because the filter coefficients are realized by transconductance ratios (current mirrors), the accuracy of these coefficients is limited to approximately 1%. Therefore, it is necessary to have a reasonably low filter sensitivity.

In section II, we describe the filter structure. Details of the implementation of the circuits are given in section III. Experimental results from a prototype implementation of the filter are given in section IV.

II. Filter structure

The filter described in this paper contains the following circuitry, as shown in figure 1: three current-followers, to perform buffering at the input and outputs of the filter, a sample-and-hold, to perform quantization in time, a 4th order lowpass and highpass filter, and a two phase non-overlapping clock-generator. The filter is intended for use in a hearing aid. It is therefore important that the passband gain and the crossover frequencies of the lowpass and highpass filter sections are accurate, to avoid the need for external adjustments. This implies low filter sensitivity, which is achieved by realizing each filter section by cascading of two biquads, where each biquad is based upon differentiator elements (D) and current amplifiers (A1,A2, ... ,A5), as shown in figure 2. By using differentiator elements for realizing each biquad, very low filter sensitivity is achieved as long as the sampling frequency is much higher than the cutoff frequency of the filter [5]. Each differentiator element implements a Backward Euler transfer function, given by:

$$D = (Z^{-1}-1) \tag{1}$$

Each current amplifier (A1, ... ,A5) has multiple outputs, where each output is a scaled version of the input current Iin, by the assigned coefficient. The assigned scaling values represent the filter coefficients. The filter is intended for use in the frequency range from 10Hz to 10kHz. The frequency of the input signal is limited to 10kHz. Therefore, to avoid aliasing the minim sampling frequency is set at 20kHz. The cutoff frequency was set to 1.59kHz at a sampling frequency of 20kHz. This gives a ratio between sampling frequency and cutoff frequency of 12.58. By performing a bilinear Z-transform to an analog Butterworth prototype filter we get the transfer functions given by (2) and (3).

$$H_{LP}(Z) = \frac{1+(Z^{-1}-1)+0.25(Z^{-1}-1)^2}{1-2.621(Z^{-1}-1)+2.280(Z^{-1}-1)^2} \cdot \frac{1+(Z^{-1}-1)+0.25(Z^{-1}-1)^2}{1-0.500(Z^{-1}-1)+3.341(Z^{-1}-1)^2} \tag{2}$$

$$H_{HP}(Z) = \frac{3.841(Z^{-1}-1)^2}{1-2.621(Z^{-1}-1)+2.280(Z^{-1}-1)^2} \cdot \frac{3.841(Z^{-1}-1)^2}{1-0.500(Z^{-1}-1)+3.341(Z^{-1}-1)^2} \tag{3}$$

Because of the low filter sensitivity we are able to truncate the filter coefficients to the nearest multiple of 0.25, (4) and (5), without significant influence on the overall frequency response, as shown in figure 4.

$$H_{LP}(Z) = \frac{1+(Z^{-1}-1)+0.25(Z^{-1}-1)^2}{1-2.50(Z^{-1}-1)+2.25(Z^{-1}-1)^2} \cdot \frac{1+(Z^{-1}-1)+0.25(Z^{-1}-1)^2}{1-0.50(Z^{-1}-1)+3.25(Z^{-1}-1)^2} \tag{4}$$

$$H_{HP}(Z) = \frac{3.75(Z^{-1}-1)^2}{1-2.50(Z^{-1}-1)+2.25(Z^{-1}-1)^2} \cdot \frac{3.75(Z^{-1}-1)^2}{1-0.50(Z^{-1}-1)+3.25(Z^{-1}-1)^2} \tag{5}$$

III. Circuit description

Low voltage and low power operation is achieved by using a single ended design and by using low bias and signal currents. The peak input-signal current was set to 750nA. The choice of the signal current is based upon a compromise between speed (sampling frequency), power consumption (low current) and compactness of the layout.

Because the filter is intended for use in a hearing aid, it is of great importance to have a low power consumption. When aiming for low power one would normally use a class AB design instead of a class A design. But in this case we found that a class A design [4, chap. 5.3] resulted in the lowest power consumption. This is because the class A circuits operate at half the supply voltage of the class AB circuits [4, chap. 5.5.3]. Also, the quiescent current of the class AB circuits could not be reduced below the quiescent current of the class A circuits because of severe settling problems caused by the differentiators.

Because of the differentiator elements, the signal currents have to settle throughout the whole filter in each clock phase. The time constant for a simple current copier cell is given by (6), where L is the channel length and ΔV is the saturation voltage of the current copier transistor. The time to settle within 0.01 %, through the longest signal path, is 17.75 time constants. This places a severe restriction on the maxim allowable sampling frequency. It also places an upper limit on Cgs, which implies a lower limit on kT/C noise.

$$\tau = \frac{Cgs}{g_m} = \frac{2}{3}\frac{CoxL^2}{K'\Delta V} \tag{6}$$

The schematic of a single differentiator element is shown in figure 3(a). The differentiator is built from two current copier transistors M1 & M3 [3, chap. 11.5]. To achieve high accuracy, it is necessary to cascode the current copiers and the current sources [3, chap. 11]. The cascoding of the current copiers reduces the channel length modulation, which improves the current transfer, and it also reduces coupling of the output voltage to the gate voltage of the current copier transistors. A special cascoding arrangement has been used [6],

which minimizes the voltage drops at the inputs and outputs of the cascoding transistors so that the circuit can operate with low supply voltages. The sample-and-hold is built from a differentiator, by placing a switch in series with the input. The effect of this is that the differentiator now operates as two current copiers in cascade with a hold function. In order to reduce the effect of charge-injection, and to lower noise, the saturation voltage of the current copiers has been set to a rather high value. Also, their gate-source capacitance has been made as large as possible, while still allowing sufficiently fast settling.

The schematic of current amplifier A2 is shown in figure 3(b). It shows that the current amplifiers are realized by current mirrors only. To achieve high accuracy and linearity, the current mirrors were realized using unity transistors and cascoding. The smallest current mirror scaling factor was set to 0.25. This implies that the desired filter coefficients (2),(3) cannot be realized exactly, but only in multiples of 0.25 (4),(5). Because of the low filter sensitivity this has no significant influence on the overall transfer function.

IV. Experimental Results

Figure 4 and 5 show the calculated and the measured frequency response of the filter at a sampling rate of 25kHz. From figure 5 it appears that the crossover frequencies of the lowpass and highpass filters are at 2kHz. This implies that the ratio between sampling frequency and cut off frequency is 12.5. The maxim sampling frequency where the filter still operated correctly was about 50kHz. The reason for this limit on the sampling frequency is, as previously discussed, that the settling time in the filter is high because of the differentiators. The circuit operated correctly for supply voltages down to 2V as expected, with a total supply current of 211μA, at a sampling rate of 50kHz. From figure 5 we observe that the dynamic-range is about 49dB for the higpass filter and about 58dB for the lowpass filter. The reason for this rather poor dynamic-range is mainly the low signal levels compared to the noise generated in the current copiers and in the current mirrors. One way to improve the dynamic-range would be to increase the signal current and at the same time make Cgs of the current copier transistor larger. This would reduce the kT/C noise and thereby increase the dynamic-range. Another possibility is to use class AB circuits which allows processing of signal currents much larger than the quiescent current. Figure 6 shows the chip photo. The area occupied by the chip core is 1.33mm^2 of which the lowpass filter occupies 0.57mm^2 and the highpass filter 0.46mm^2.

V. Conclusion

This paper has described the use of the switched current technique for implementing a sampled analog filter. The design demonstrates that differentiator based filters achieve very low sensitivity. The filter has been optimized for low power operation and measurements show that the filter operated correctly down to 2V, with a total supply current of 211μA. In the CMOS process used for this design, the threshold voltage was 0.9V. The area of the chip core is approximately 1.33mm^2 and the sampling frequency was limited to 50kHz .

Acknowledgement

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References

[1] Roubik Gregorian and Gabor C. Temes:
"Analog MOS Integrated Circuits for Signal Processing"
Published by:John Wiley & Sons, USA, 1986

[2] J.B. Hughes, N.C. Bird, and I.C. Macbeth:
"Switched Currents - A New Technique For Analog Sampled-Data Signal Processing"
IEEE International Symposium On Circuits And Systems, 1989, pp. 1584-1587

[3] C. Toumazou, F.J. Lidgey and D.G. Haigh:
"Analog IC-design: the current-mode approach"
Published by: Peter Peregrinus Ltd., London, United Kingdom, 1990

[4] R.S. Soin, F. Maloberti and J. Franca:
"Analog-Digital ASICs"
Published by: Peter Peregrinus Ltd., London, United Kingdom, 1991

[5] Shen-Iuan Liu, Chih-Hsien Chen, Hen-Wai Tsao and Jingshown Wu:
"Switched-Current Differentiator-Based IIR And FIR Filters"
Int. J. Electronics, 1991, Vol. 71, No 1, pp. 81-91

[6] P.J. Crawlay and G.W. Roberts:
"High-Swing MOS Current Mirror With Arbitrarily High Output Resistance"
Electronics Letters, 13th February 1992, Vol. 28, No. 4, pp. 361-363

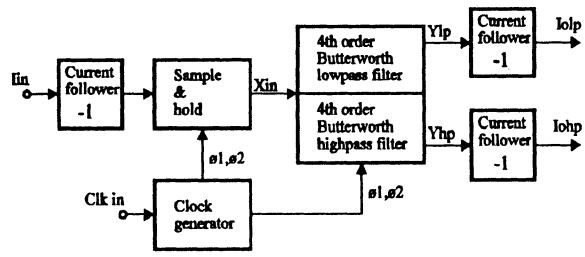


Figure 1: Block diagram of the filter-chip

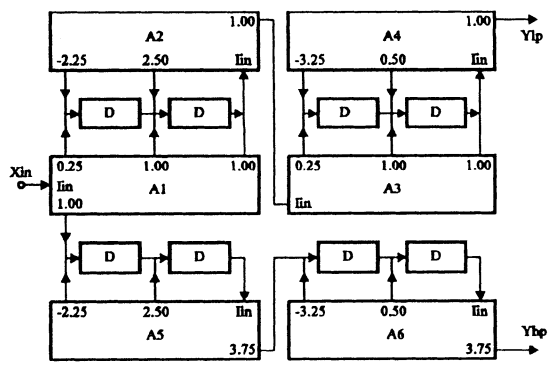


Figure 2: Filter structure

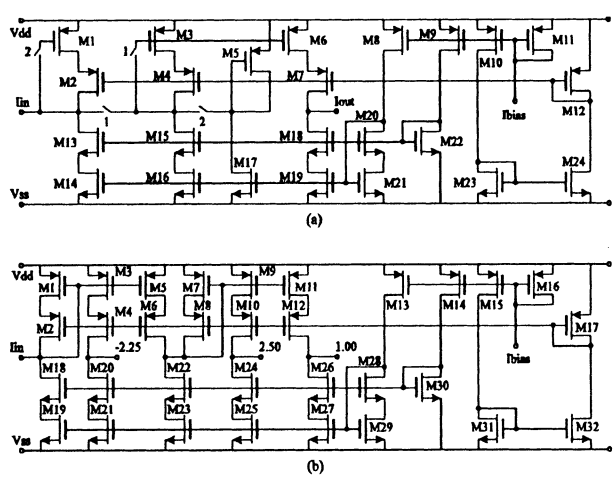


Figure 3: Switched current cells
(a): Differentiator.
(b): Current amplifier A2.

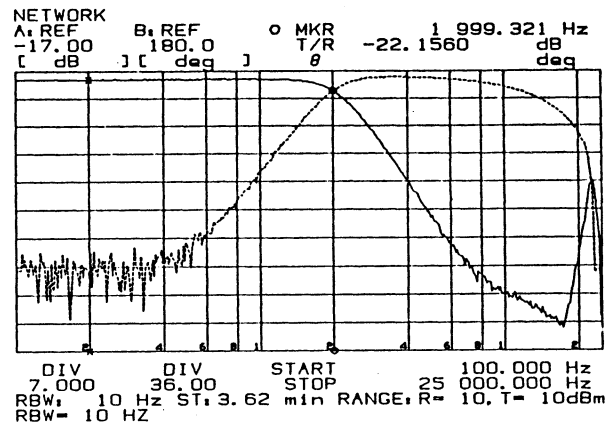
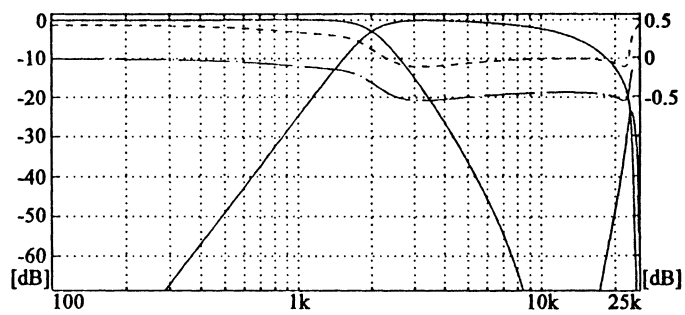


Figure 5: Measured frequency response



Solid: Coefficients truncated to nearest multiple of 0.25
Dashed: Error between exact and truncated highpassfilter
Dashdot: Error between exact and truncated lowpassfilter

Figure 4: Calculated frequency response

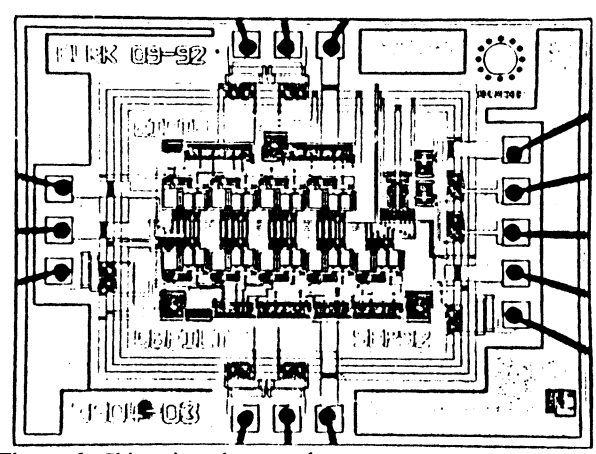


Figure 6: Chip microphotograph