Performance Aspects of Gate Matrix Layout

Hald, Bjarne; Madsen, Jan

Published in:
International Conference on V L S I Design. Proceedings

Publication date:
1993

Document Version
Publisher's PDF, also known as Version of record

Performance Aspects of Gate Matrix Layout

Bjarne Hald and Jan Madsen

Center for Integrated Electronics
Department of Computer Science
Technical University of Denmark
DK-2800 Lyngby, Denmark
Email: bh@id.dth.dk, jm@id.dth.dk

Abstract

This paper introduces performance aspects as a new optimization criteria when generating Gate Matrix Layouts. A new layout model is presented that limits the amount of parasitic capacitance in signal paths and the resistance in power supply lines. The performance considerations are combined with a new layout strategy that improves circuit performance with little or no area penalty. An Automatic Transistor Layout Synthesizer (ATLAS) implements the proposed changes to the Gate Matrix Layout style.

1 Introduction

The Gate Matrix Layout style was introduced by Lopez and Law in 1980 [4] as a general strategy for manual CMOS layout generation, where transistors are laid out on rows in a matrix and vertically running polysilicon wires form gate terminals for the transistors. The regular structure allows for easy technology updates involving only a change in the inter-row and inter-column distances.

Much research effort has been spent on automating the layout generation, and the key topics have been optimization of gate sequence and transistor net placement. The first problem is to find a sequence of gate lines that minimizes the problem of connecting transistors to each other. The problem is known to be NP-complete and therefore much effort has gone into finding a good heuristic algorithm with a low time-complexity. The second problem is to find the optimal placement of transistors onto rows in order to minimize the total area.

Previous research ([2], [3], [1], [5]) has resulted in a number of good algorithms for optimizing the area of *symbolic* layouts, but almost no real layouts have been presented. Performance aspects have not been considered when generating symbolic layouts thus leading to real layouts with unnecessary amounts of parasitic capacitance in signal paths. Furthermore, the symbolic layouts have not included power connections, although Huang et al. [1] have presented a power connection strategy. This power connection strategy limits the length of power supply lines to a fixed number of rows, but does not consider the load on the supply lines.

This paper introduces a new layout model that changes the usual Gate Matrix style of making vertical connections and gives a set of rules to be obeyed when placing and connecting transistor nets. The use of these rules and the new connection style will limit the amount of parasitic capacitance in signal paths. The power connection strategy is improved by limiting the length of power supply lines dynamically as a function of the load.

The new layout model minimizes area by decreasing the distance between polysilicon lines. Previously, only the number of rows have been optimized in the attempt to minimize area, but experimental results from exhaustive tests on gate sequence show that this is not a good optimization criteria.

The proposed Gate Matrix Layout Model has been implemented in the ATLAS (Automatic Transistor LAyout Synthesizer) program that inputs a transistor netlist and outputs a real layout in e.g. CIF format.

2 Analysis of previous gate matrix layouts

The Gate Matrix Layout style can be improved with respect to performance and area by taking a closer look at the inherent layout model, i.e. the model describing how the final layout should be created from internal symbolic representations.

0-8186-3180-5/92 $3.00 © 1992 IEEE

Parasitic capacitance

The most important contributor to parasitic capacitances in a layout is the diffusion layer, which contributes significantly both from the bottom (area dependent) and the side-wall (perimeter dependent). Furthermore, the sheet resistance of diffusion is very high, and the combination of large capacitance and sheet resistance thus leads to large *rc*-delays when the layer is used for routing.

In previous approaches, diffusion is used for vertical connections as well as for connections between abutting transistors that are far apart, thereby inducing extra capacitance and perhaps significant *rc*-delays in the signal path.

Power connections

The power connection strategy by Huang et al. [1] prescribes that power connections should be made with metal wires running horizontally from the left and righthand sides of the matrix. If some transistors cannot be supplied this way, extra power rows must be inserted in the matrix from which vertical diffusion wires can supply the transistors with power. There will be a voltage drop in the diffusion wires due to the large resistance in the diffusion layer. This voltage drop depends on the current in the wire which in turn depends on the load that is driven, i.e. the width of the supplied transistors. A long vertical diffusion wire supplying several transistors may therefore slow down performance considerably. Huang et al. proposed to put a fixed limit on the length of these diffusion wires, i.e. with no consideration to the load driven by the wire.

Placement rules

The placement of transistors and connections in a Gate Matrix has previously been made without consideration to neighbouring transistors or connections thus enabling more transistors to fit in one row and thereby decrease the row count. This is desirable in a symbolic layout where the area is considered proportional to the number of rows, because columns are assumed to be equally spaced. However, in a real layout, two non-connected transistors with terminals in the space between adjacent gates (the *channel*) will push the columns apart because of design rule spacings. The same happens if a gate contact extends into the same piece of channel as a transistor terminal or diffusion wire. This has the twofold impact of increasing both matrix area and the diffusion area of abutting transistors anywhere in that channel.

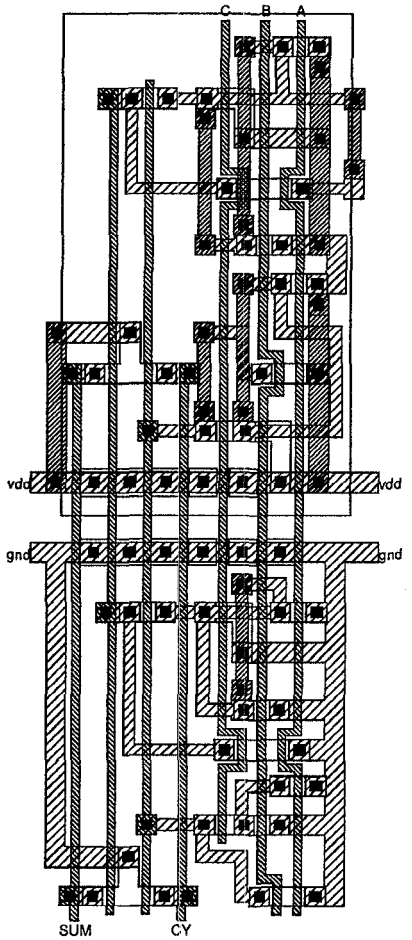

Figure 1: Layout of fulladder produced by ATLAS

3 ATLAS

The ATLAS (Automatic Transistor Layout Synthesizer) tool implements a new layout model, which takes into account performance and area aspects. The min-net-cut algorithm presented by Hwang et al. [2] is used to find the gate sequence, and a left-edge algorithm is used to place transistors and connections onto rows. This section describes the characteristics of the new layout model, which is further illustrated in the layout of a fulladder produced by ATLAS (see fig. 1).

Connection style

ATLAS uses a combination of Metal-1 and Metal-2 for routing vertical connections, thereby avoiding diffusion as a routing layer. The Metal-1 layer is used where possible, otherwise Metal-2. Horizontal connections in diffusion between abutting series-connected

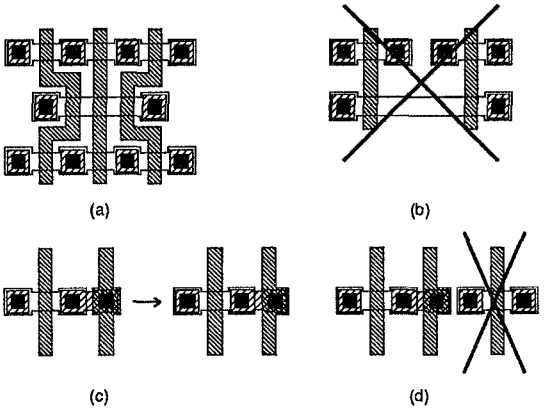

Figure 2: (a) Transistor Squeezing. (b) Rule 1. (c) Rule 2. (d) Rule 3.

transistors are shortened by *squeezing* transistors together as shown in figure 2a. Series-connections with less than 4 transistors can be squeezed with very little or no area-penalty.

Power connections

Power connections follow the same general strategy as previously, but a limit is posed onto the length of power diffusion wires depending on the load driven by the wire. As stated before, the voltage drop in a power supply line depends on resistance (a function of length and width) and current. The maximum current in a power supply line is reached when the transistor is in the saturation region, and the maximum current is then proportional to the transistor width. N transistors driven by the same power supply line is made equivalent to one wide transistor in order to find an upper bound on the resulting voltage drop. This gives the following equation:

$$\lceil \Delta V \rceil = rlI = rl\frac{\sum_{j=1}^{N} W_j}{W_0} i_0$$

where r is the resistance per length of the diffusion wire, l is the length of the wire, I is the total maximum current drawn by all transistors, W_j is the width of the j'th transistor and W_0 is the width of a transistor in which the maximum current is i_0. If the maximum voltage drop, ΔV_{max}, at peak current, i_0 is known for a transistor, then the maximum length, l_{max}, of the diffusion wire that feeds power to it can be computed. This leads to the bounding equation for diffusion length and load:

$$l\sum_{j=1}^{N} W_j < l_{max} W_0$$

The above equation enables ATLAS to limit the length of diffusion wires depending on the load, if the maximum length is known of a diffusion wire feeding a single transistor of width W_0. This maximum length can either be estimated or computed via circuit simulations. The product of length and width, the *LW-product*, can then be passed to ATLAS, which will insert extra rows in the layout if the *LW-product* of a particular power line exceeds the prescribed value.

Placement rules

The area of a Gate Matrix Layout is a function of the number of columns and rows as well as the width and height of individual columns and rows. In a realistic layout the width of columns and the height of rows will vary because of design rules. This has not been considered by previous research, where the only optimization goal has been to minimize the number of rows, thereby assuming that the width and height is the same for all columns and rows respectively.

ATLAS uses a set of placement rules in order to minimize the distance between gates to one that exactly allows room for a diffusion contact to be placed. The placement rules are to be observed every time a new transistor net is placed in the matrix. When for instance a transistor is placed and connected to an adjacent gate it is necessary to shift the gate contact away. The placement ruleset is given below:

Rule 1 Two transistors on adjacent gates but with non-abutting diffusion regions must not be placed on the same row (see figure 2b).

Rule 2 If a transistor drain connects to the immediately adjacent gate then the gate contact must be shifted away from the drain (see figure 2c).

Rule 3 A transistor must not be placed in a position adjacent to a shifted gate contact (see figure 2d).

4 The influence on area of power connections

ATLAS is capable of performing exhaustive tests on the sequence of gate lines. For each possible gate sequence the real layout is produced and various statistical data recorded so that the smallest layout can be found. Exhaustive tests were made on three benchmark circuits, a fulladder, a halfadder and a multiplexer. Two sets of statistics were gathered for each circuit; a set containing data from all possible sequences (the full set) and a set containing data from all sequences resulting in a minimum row count (power rows excluded). Results from the literature have all

Circuit		Row Count (N)	Area μ^2	Power Area (%)
fulladder	Min.	13	20330	6
	Max.	21	55076	25
halfadder	Min.	8	12432	9
	Max.	15	22470	31
mux	Min.	7	9898	11
	Max.	11	20501	31

Table 1: Results from Exhaustive Test

Circuit		Row Count (N)	Area μ^2	Power Area (%)
fulladder	Opt.	16	20330	8
	Min.	13	24557	19
	Max.	13	30573	22
halfadder	Opt.	10	12432	14
	Min.	8	13301	23
	Max.	8	15471	29
mux	Opt.	7	9898	17
	Min.	7	9898	17
	Max.	7	17709	31

Table 2: Minimum rowcount results compared with minimum area results

been measured by the minimum number of rows obtained excluding the power connections. The exhaustive test was done in order to evaluate the influence of power connections on area with the theory that a minimum number of rows doesn't necessarily lead to minimum area. Table 1 shows the maximum and minimum data from the full exhaustive test. Table 2 shows the optimal result with corresponding row count and power area percentage compared with the maximum and minimum data obtained from layouts with minimum row count.

For all benchmarks the exhaustive test shows that using the minimum number of non-power rows as an area estimate may lead to layouts that are more than 75 % larger than the minimum layout. Furthermore, in both the *fulladder* and *halfadder* examples, minimum area was obtained using a non-minimal number of non-power rows. This effect can be explained by studying the area percentage occupied by power connections. Minimum area was in all examples obtained for solutions with small power area percentages, with minimum row count solutions leading to larger percentages. This is reasonable, because when a small number of rows is used for transistors and connections the layout is very dense, thus making it more difficult to connect transistors to power. In very dense layouts it will therefore be necessary to insert more power connection rows and hence increase the area. Consequently, the previously used optimization criteria (i.e. number of rows excluding power connections) does not guarantee minimum area. It is therefore necessary to include power connection considerations in the algorithms used for gate line sequencing and to include the impact on area of these connections in the measure used for comparing algorithms.

5 Conclusion

A new layout model for Gate Matrix Layout has been introduced that improves performance by decreasing the amount of parasitic capacitance in signal paths and limiting the voltage drop in power supply lines. By paying attention to design rule effects when placing transistors and connection nets, the distance between gate lines and hence matrix width is minimized.

The layout model has been implemented in a Gate Matrix tool (ATLAS) capable of producing real Gate Matrix Layouts from transistor netlists. Exhaustive tests on the sequence of gate lines have been made using this tool, showing a significant impact on area of power connections. Gate Matrix algorithms must therefore be adjusted so as to consider power connections.

References

[1] Shuo Huang and Omar Wing. Improved Gate Matrix Layout. *IEEE Transactions on Computer-Aided Design*, 8(8):875–889, August 1989.

[2] D.K. Hwang, W.K. Fuchs, and S.M. Kang. An Efficient Approach to Gate Matrix Layout. In *International Conference on Computer-Aided Design*, pages 312–315, November 1986.

[3] H.W. Leong. A New Algorithm for Gate Matrix Layout. In *International Conference on Computer-Aided Design*, pages 316–319, November 1986.

[4] Alexander D. Lopez and Hung-Fai S. Law. A Dense Gate Matrix Layout Method for MOS VLSI. *IEEE Journal of Solid-state circuits*, SC-15(4):736–740, August 1980.

[5] Uminder Singh and C.Y. Roger Chen. From Logic to Symbolic Layout for Gate Matrix. *IEEE Transactions on Computer-Aided Design*, 2(2):216–227, February 1992.