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CMOS Technology and Current–Feedback Op–Amps

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Abstract — **The implementation of current–feedback op–amps (CFB op–amps) relies on the use of a semiconductor process with complementary device structures for class AB operation of the input and output stages. Thus, CMOS technology is an obvious candidate. However, commercial CFB op–amps are all realized in bipolar processes.**

In this paper we identify some of the problems related to the application of CMOS technology to CFB op–amps. Problems caused by the low device transconductance and by the absence of matching between P–channel and N–channel transistors are examined, and circuit solutions providing improved input characteristics are presented. Also, problems related to the achievable output voltage swing are examined and circuits which may be used to achieve a near rail to rail output swing are proposed.

It is concluded that mere translations of bipolar circuit designs yield a rather poor performance compared to the bipolar designs, but CMOS has a potential for CFB op–amp design if more ingenious circuit configurations are applied.

I. Introduction

Almost all current–feedback operational amplifiers (CFB op–amps) presented in the literature or as commercial products have been realized in bipolar technology. However, with the preference for CMOS in mixed analog/digital systems the question arises whether CMOS is a viable technology for the implementation of CFB op–amps. When investigating this question a number of specific problems are raised. The problems are related to the relatively high threshold voltage of MOS transistors compared to the normal level of supply voltage, the mismatch between N–channel and P–channel transistors, and the low value of gate transconductance. In this paper we shall review some of these problems and indicate design directions which may provide useful solutions to the problems.

II. Basic CMOS implementations

The first natural approach taken to implement a CMOS CFB op–amp is to translate well known bipolar configurations [1, 2] into CMOS [3]. This leads to the two CMOS circuits shown in fig. 1. The circuit of fig. 1(a) uses a single stage complementary source follower as the input stage. Transistors M3 and M4 provide a biasing for the complementary source follower stage M1 and M2. The transimpedance stage is composed of the current mirrors M9, M11 and M10, M12, and M13–M16 form the output buffer. The basic characteristics obtained from this structure are the transresistance R_T and the inverting input resistance R_x given by

$$R_T = (g_{ds11} + g_{ds12})^{-1} \tag{1}$$

and

$$R_x = (g_{m1} + g_{m2} + g_{mbs1} + g_{mbs2})^{-1} \tag{2}$$

where g_{dsN}, g_{mN}, and g_{mbsN} denote the drain–source output conductance, the gate transconductance, and the bulk transconductance, respectively, of MOS transistor number N.

Obviously, the use of single transistors as shown in fig. 1 leads to an unacceptably low value of R_T. This problem can be solved by the use of cascoded current mirrors. The value of R_x is fairly high, about one order of magnitude higher than for bipolar implementations operating at a

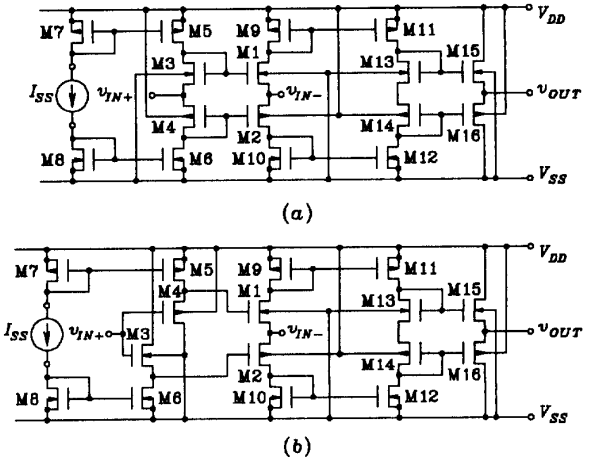

Fig. 1. Basic CMOS current–feedback op–amps. (a) Single stage complementary source follower input. (b) Source follower cascade input.

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comparable level of quiescent current. This is unfortunate because the bandwidth of the CFB op–amp in a non–inverting feedback configuration with a feedback resistor R_F from the output to the inverting input is given by

$$2\pi BW = \frac{1}{C_T(R_F + A_{cl}R_x)} \tag{3}$$

where A_{cl} is the closed loop gain and C_T is the compensation capacitor placed at the transimpedance node. With high values of closed loop gain, R_x provides a serious limitation to the bandwidth. This problem is considered in more detail in section III. Another problem with the input stage of fig. 1(a) is a dc input error current to the non–inverting input. This is caused by a mismatch of the bias currents to transistors M3 and M4. These two bias currents are derived from a single current source through the current mirrors M7, M5 and M8, M6. With a matching accuracy of about 1%, input error currents in the microampere range can be expected for a bias current of some hundreds of microamperes.

Finally, the configuration of fig. 1(a) has a rather limited common mode range because of the source follower structures. The maximum output voltage swing achievable is from $V_{SS}+V_{TN}$ to $V_{DD}+V_{TP}$ where the threshold voltages V_{TN} and V_{TP} for the N–channel and P–channel transistors, respectively, are subjected to the maximum bulk effect, implying that they assume values in the range of $\pm 1V$ to $\pm 2V$. This must be compared to the supply voltage $V_{DD} - V_{SS}$, normally in the range of $3V$ to $10V$. Especially for circuits designed to operate off standard digital supply voltage levels, this presents a significant problem. In section IV we consider alternatives providing a larger output voltage swing.

The circuit of fig. 1(b) utilizes a complementary source follower cascade as the input stage. It has the same properties as the circuit of fig. 1(a) with respect to R_T and R_x. Compared to the circuit of fig. 1(a) two major differences are noted: (*i*) The use of a complementary source follower cascade eliminates the dc input error currents to the non–inverting input, and (*ii*) both a gain error and an offset error between the non–inverting and the inverting input is introduced. The gain error is due to the bulk effect on the source follower transistors, causing the gain of each of the source followers to be less than 1, typically in the range of 0.50 to 0.95. The offset error is caused by different threshold voltages for N–channel and P–channel transistors, respectively. It is typically some hundreds of mV. As the gain of the voltage follower input stage enters directly as a factor into the closed loop gain equations for the CFB op–amp, a gain different from 1 is clearly unacceptable for a general purpose CFB op–amp. Also, a large offset voltage between the non–inverting and the inverting input is unacceptable. Therefore, the configuration of fig. 1(b) is not directly applicable but as we show in the next section, elements of the implementation may be employed in an improved input stage configuration.

III. Input Stage Design

An input stage with a lower inverting input impedance can be obtained by using an op–amp with feedback to obtain the unity–gain operation from the non–inverting input to the inverting input. Assuming an idealized op–amp model with an open loop output resistance of R_{ol} and an open loop gain of $A_{ol} = 2\pi GBW/s$ where GBW is the unity–gain bandwidth of the op–amp we find an inverting input impedance of

$$Z_x = s\frac{R_{ol}}{2\pi GBW}\,\frac{1}{1+s/(2\pi GBW)}. \tag{4}$$

It is noted that the input impedance is inductive at moderate frequencies with an equivalent inductance of $L_x = R_{ol}/(2\pi GBW)$. This may cause stability problems if the feedback impedance Z_F from output to inverting input is small compared to $L_x s$. With a feedback impedance Z_F from output to inverting input and an impedance Z_S from inverting input to ground we find a loop gain of

$$T(s) = \frac{R_T}{Z_F + A_{cl}Z_x}\,\frac{1}{1+sR_TC_T} \simeq \frac{1}{sC_T(Z_F + A_{cl}Z_x)} \tag{5}$$

where $A_{cl} = 1 + Z_F/Z_S$. This gives the phase margin

$$\phi_m = 90^\circ - \angle(Z_F(j\omega_m) + A_{cl}(j\omega_m)Z_x(j\omega_m)) \tag{6}$$

with ω_m given by

$$|\omega_m C_T(Z_F(j\omega_m) + A_{cl}(j\omega_m)Z_x(j\omega_m))| = 1. \tag{7}$$

Even with a purely resistive feedback network ($Z_F = R_F$, $Z_S = R_S$), we see that the term $A_{cl}Z_x(j\omega_m)$ causes a reduction of the phase margin.

Another problem with the use of a feedback input buffer is the slew rate. One of the advantages of the CFB op–amp over standard voltage mode op–amps is its non–slew rate limited transient response. However, this requires a non–slew rate limited input buffer. This leaves only a few

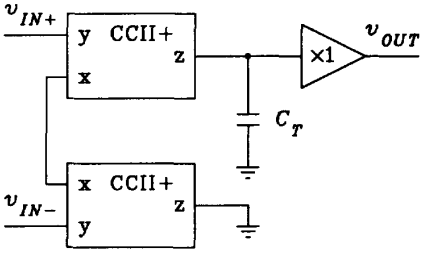

Fig. 2. Conveyor based voltage mode op–amp.

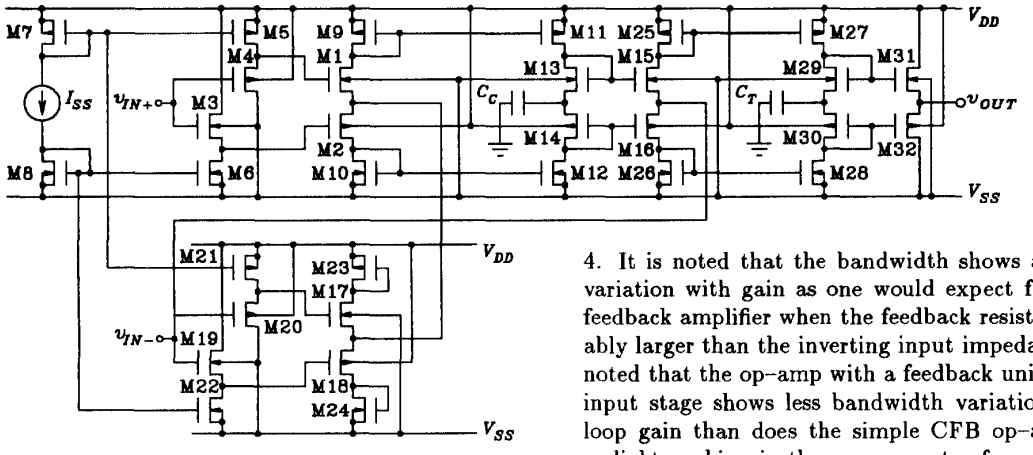

Fig. 3. Improved CMOS current-feedback op-amp design with op-amp based unity-gain input buffer.

implementation principles for an input buffer with feedback. One is to use another CFB op-amp with feedback as a unity-gain buffer [4]. Another is to utilize the current conveyor-based non-slew rate limited op-amp design shown in fig. 2 [5]. The latter approach has some advantages: As the current conveyor gain from y to x may be different from 1, and as there may be an offset from y to x (provided the two conveyors are identical), the conveyor shown in fig. 1(b) may be employed in the implementation of the op-amp of fig. 2. This provides the advantage of eliminating the non-inverting input error current. There is another advantage of using the op-amp structure shown in fig. 2 instead of a CFB op-amp for the input buffer design: The circuit of fig. 2 has a feedback loop encompassing both of the conveyor y to x buffers, whereas the y to x buffer in a unity-gain amplifier based on a CFB op-amp is outside the feedback loop. Hence, the design based on the op-amp of fig. 2 can be expected to have better properties with respect to linearity, distortion, sensitivity to component tolerances, etc.

An experimental version of both the CFB op-amp shown in fig. 1(a) and an improved structure with a simplified transistor diagram as shown in fig. 3 has been designed and fabricated in an industry standard $2.4\mu m$ analog CMOS process. Both of the test op-amps have been designed with minimum channel lengths. In order to increase the output resistance of the MOS transistors, regulated cascodes [6] have been used for each of the transistors in the circuit.

The frequency response of the op-amps has been measured as the response of a non-inverting current-feedback amplifier with a feedback resistance of $5k\Omega$ (compared to an inverting input resistance of about 250Ω for the simple op-amp of fig. 1(a)). The measurements are shown in fig. 4. It is noted that the bandwidth shows a rather small variation with gain as one would expect from a current feedback amplifier when the feedback resistor is considerably larger than the inverting input impedance. It is also noted that the op-amp with a feedback unity-gain buffer input stage shows less bandwidth variation with closed loop gain than does the simple CFB op-amp. Finally, a slight peaking in the response at a frequency of about $40MHz$ is noted for the op-amp with a feedback unity-gain buffer input stage. This is attributed to the feedback loop of the input buffer.

IV. Output Stage Design

The output buffer shown in figs. 1 and 3 is essentially a complementary source follower. This means that it provides a reasonably low open loop output impedance but a

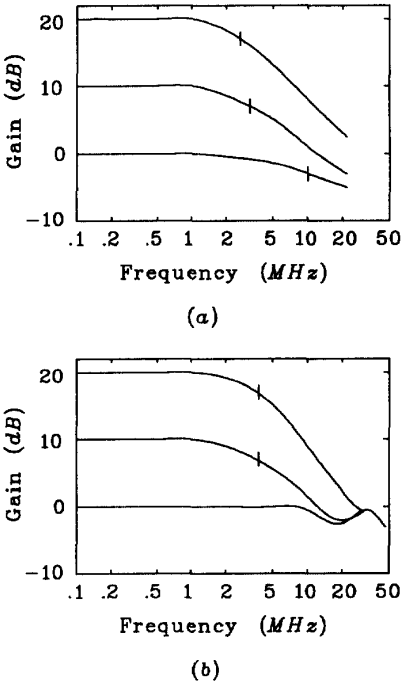

Fig. 4. Frequency response of experimental CFB op-amps. (a) Single stage source follower input. (b) Op-amp based unity-gain buffer input.

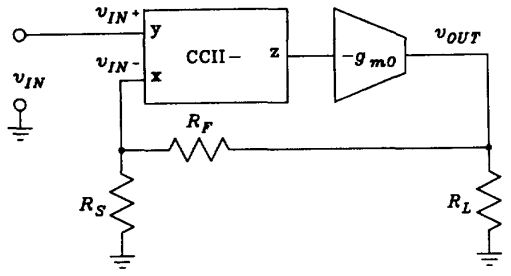

Fig. 5. CFB op–amp with a transconductance output stage.

limited output voltage range. In order to achieve a larger output voltage range, a common source output stage is required. When using a pure common source stage, the output stage is inverting, and to a first approximation it is described by a transconductance g_{mO}. This implies that the sign of the current mirror to the transimpedance stage has to be changed. The resulting op–amp configuration may be described by a CCII– conveyor and a transconductance output stage as shown in fig. 5. With the assumption that the CCII– provides a perfect mirroring of i_X to $-i_Z$, we find a loop gain of

$$T(s) = \frac{R_T g_{mO}}{1 + sR_T C_T} \frac{R_L}{R_L + R_F + R_S \parallel R_x} \frac{R_S}{R_x + R_S}. \quad (8)$$

From (8) we find the bandwidth BW

$$2\pi BW = \frac{g_{mO}}{C_T} \frac{1}{\left(1 + \frac{R_x}{R_S}\right)\left(1 + \frac{R_F}{R_L}\right) + \frac{R_x}{R_L}}. \quad (9)$$

With the simplifying assumptions that $R_x \ll R_S$ and $R_x \ll R_L$, we find

$$2\pi BW = \frac{g_{mO}}{(1 + R_F/R_L)C_T} \quad (10)$$

which expresses a constant bandwidth (independent of closed loop gain A_{cl}).

An important problem with this configuration is the high output impedance of the output stage which can lead to stability problems with capacitive loading. Thus, the time constant $C_L \times (R_L \parallel R_F)$ must be smaller than $(2\pi BW)^{-1}$ in order to ensure a reasonable phase margin. One way of solving this problem would be to introduce an output buffer with a small input capacitance. With this buffer kept outside the feedback loop, the bandwidth relations given above remain valid, but the problem of designing a non–slew rate limited output buffer with rail to rail voltage swing also remains unsolved. Another approach would be to use a combination of a source follower output stage and a common source output stage [7] with separate signal paths to the output source follower through single current mirrors and to the common source output drivers through cross–coupled current mirrors. This method results in a small output resistance and frequency characteristics comparable to those found in a conventional CFB op–amp. Work is presently in progress with an implementation using this approach.

V. Conclusion

It has been shown that translations of bipolar current–feedback op–amps into CMOS have some weak points in terms of inverting input resistance, input error currents, and signal range. Circuit solutions are pointed out which may provide solutions to the problems. The inverting input resistance can be lowered by using an input buffer with feedback. The error current to the non–inverting input can be eliminated through the use of an input stage with only transistor gates (and protective devices) connected to the input terminal. The output signal range may be expanded through the use of a common source output stage. One problem not dealt with is the common mode input signal range. In the proposed designs this is limited by the limited swing of the source follower stages used for the input buffers. An expansion of the input signal range would require a re–design of the input buffer such that it can accomodate larger signal swings, i.e. the incorporation of a common source stage driving the inverting input, but this has not been considered in the present work.

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