Above 8GHz Static T-Flip-Flop Operation using FT=22.9GHz GaAs MESFETs

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ABOVE 8GHZ STATIC T-FLIP-FLOP OPERATION USING F_T=22.9GHZ GAAS MESFETS

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ABSTRACT

Abstract: A static SCFL Toggle Flip-Flop GaAs IC having maximum operating frequency of F_{div}=8.25GHz has been designed using a commercially available GaAs MESFET foundry service. The average F_t for the present wafer is F_t=22.9GHz giving a very high F_{div}/F_t-ratio of F_{div}/F_t=0.36. In addition output voltage transition times of T_t(20%-80%)=35ps are obtained by implementation of a novel output driver design.

MOTIVATION

Recently there has been a dramatic progress in the development of ultrahigh-speed frequency dividers, thus maximum frequencies of operation of above 20GHz have been reported. These high performance devices are based on very advanced transistors, such as very short gate SAINT MESFETs (1), HEMTs (2) or HBTs (3). There has hence been a rather intense publishing activity regarding high divider speed obtained through new or refinement of existing processes. We do not have access to such advanced transistors mentioned above but are restricted to use commercially available foundry services. Therefore our approach has been to get maximum performance from the given MESFET process through circuit design. In order to compare with elsewhere reported divider performance we use the F_{div}/F_t-ratio as a figure of merit of, how well a process is utilized. In Table 1 is shown a list of reported performance of static MESFET frequency dividers covering different authors (processes) over the past 14 years, and a grouping in the F_{div}/F_t-ratio of $0.30<F_{div}/F_t<0.33$ seems to be the case.

F_t	F_{div}	F_{div}/F_t	Year	L_g	Author
15GHz	4.5GHz	0.30	1977	1.00µm	HP
15GHz	5.0GHz	0.33	1982	1.00µm	HP
23GHz	7.5GHz	0.33	1985	0.55µm	NTT
60GHz	17.9GHz	0.30	1986	0.20µm	HRL
35GHz	11.0GHz	0.31	1986	0.50µm	NTT
32GHz	10.2GHz	0.32	1988	0.40µm	NTT
49GHz	16.0GHz	0.33	1989	0.50µm	OKI
74.3GHz	26.8GHz	0.36	1989	0.15µm	NTT
22.9GHz	8.25GHz	0.36	1991	0.50µm	CBT

Table 1: Reported performance of static dividers based on GaAs MESFETs.

DEVICE CHARACTERISTICS

We have used Anadigics GaAs foundry service. They offer a 0.5µm gate length MESFET process. According to the PCM data for our wafer the MESFETs have a pinch-off voltage of V_p=-0.8V, an ac transconductance of G_m=189mS/mm, a saturation current of I_{dss}=140mA/mm and an average unity current gain frequency of F_t=22.9GHz. F_t is calculated as $F_t=G_m/2\pi C_{gs}$ at V_{ds}=2.5V and V_{gs}=0V.

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4-PHASE GENERATOR

Designers of e.g. high-speed multiplexers and demultiplexers may need 4 timing signals at half the clock rate shifted 0,90,180 and 270 degrees, respectively, instead of just a single signal at half the clock rate (4)(5). This lead to the divider configuration shown in Fig.1, where we use a Master-Slave D-Flip-Flop (MS D-FF) with the usual feed-back connections and take M,S and the corresponding complementary signals as output signals thus generating the desired 4 timing signals.

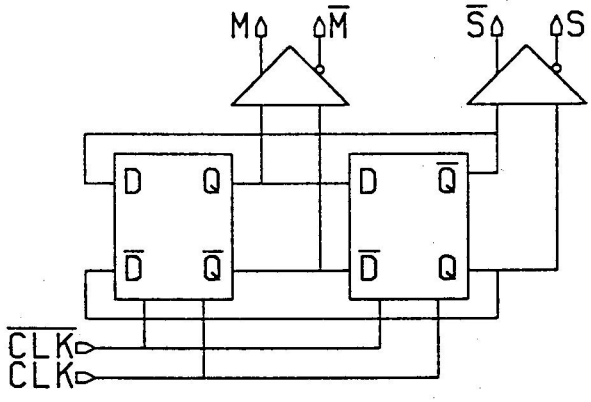

Fig 1: 1/2 frequency divider configuration

SCFL 1/2 FREQUENCY DIVIDER

Both the master and the slave latch are realized using the well known SCFL two-level logic structure shown in Fig.2. Gate width scaling factors are chosen in such a manner, that all FETs are kept in good biasing conditions during the full logic swing, that is, switching FETs are operating near the peaking in the unity current gain frequency F_t during switching, and the source follower input FETs are operating near the peaking in the transconductance G_m.

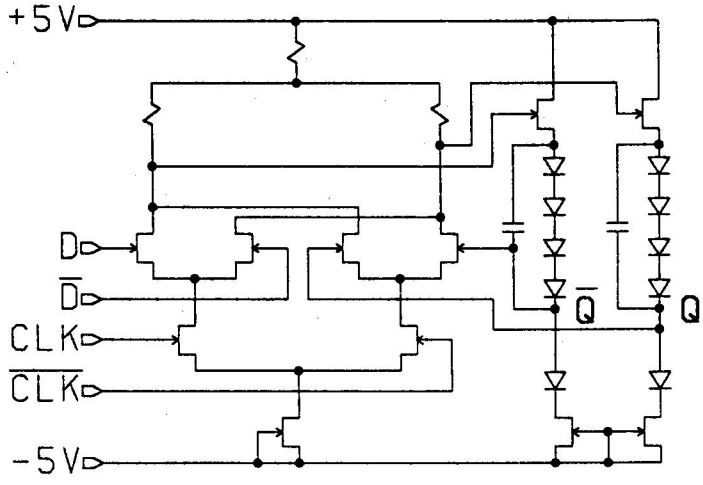

Fig 2: SCFL latch configuration used for both master and slave.

NOVEL OUTPUT DRIVER DESIGN

In order to achieve short rise and fall times at the output ports we have applied open drain outputs, which is commonly seen for devices operating at or above 5Gbit/s (6)(7). In addition we suggest this differential output stage to be driven by the *differential push-pull buffer/amplifier* shown in Fig.3. By using this output stage we have achieved very short transition times.

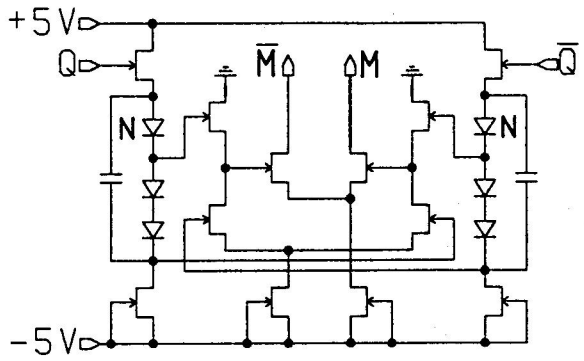

Fig 3: Differential push-pull output driver. Q and M represent input and output signals, respectively.

MEASURED CIRCUIT PERFORMANCE

Circuit performance was measured using a Cascade Microtech probe station. The dual phase input clock signals were generated using an HP microwave generator, a power splitter and a variable delay line. Output signals were monitored on a HP 4 channel sampling oscilloscope and a spectrum analyzer. A maximum toggle frequency of 8.25GHz was obtained at a power dissipation of 740mW and an output voltage swing of 480mV. The corresponding response monitored by a spectrum analyzer is shown in Fig.4 At toggle frequencies above 7.5 GHz the output signal duty cycle drifts rapidly away from 50%, and the output voltage swing and input sensitivity are decreasing, Fig.5, thus adding the requirement for filtering and amplification at clock frequencies above 7.5GHz for most digital applications. However, at clock frequencies below 7.5GHz, e.g. at 5GHz as shown in Fig.6, square-wave like outputs are generated having near 50% duty cycle, app. 800mV amplitude (V_{OH}=0V) and very short transition times, Table 2.

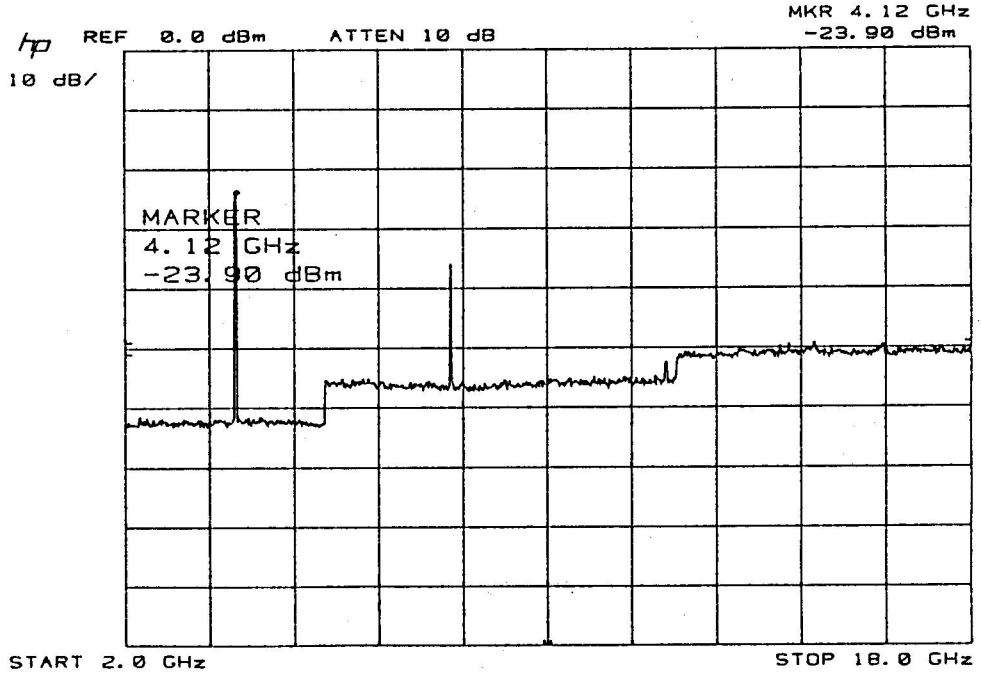

Fig 4: MS-TFF output measured by spectrum analyzer when operating at the maximum input frequency of 8.25GHz.

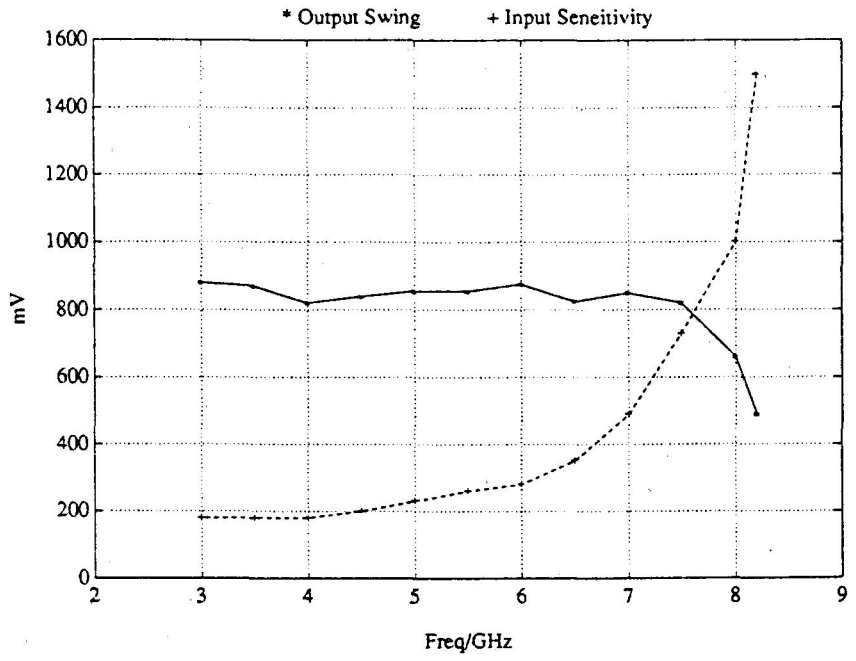

Fig 5: Input sensitivity (dashed line) and output voltage swing (solid line) as function of input clock frequency.

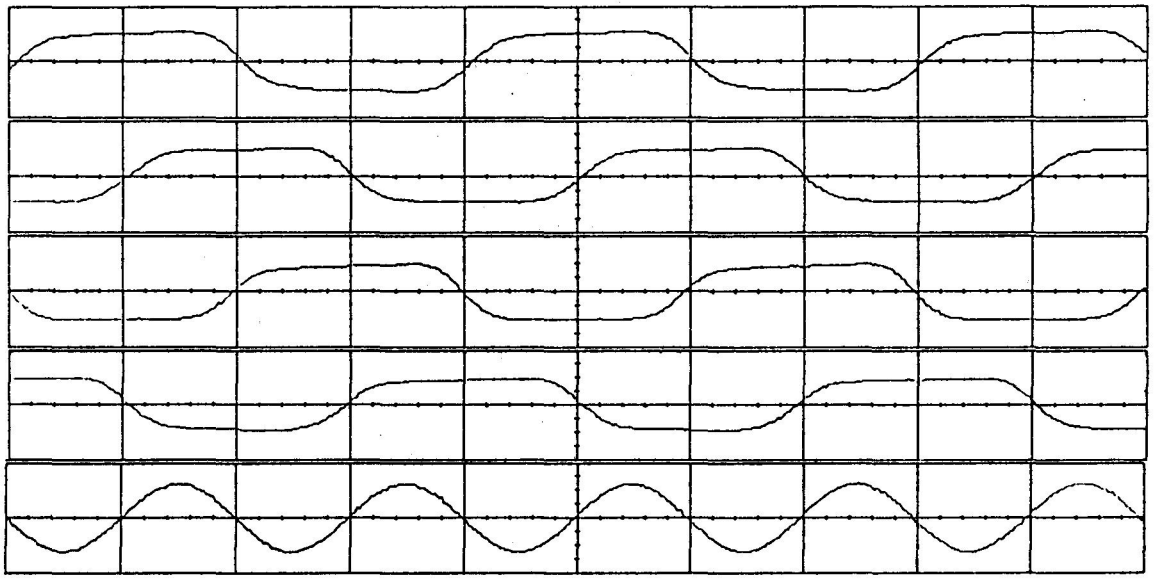

Fig 6: Measured Output signals M,S,NM,NS and corresponding input clock wave-forms when operating on a 5GHz clock. Vertical: 1V/div and Horizontal: 20ps/div.

	10-90%	20-80%
T_r	54ps	35ps
T_f	51ps	33ps

Table 2: Measured transition times at 5GHz clock frequency.

CONCLUSION

A 8.25GHz static 1/2 frequency divider IC has been designed using a commercially available 0.5µm gate length GaAs MESFET process with an average F_t across the wafer of F_t =22.9GHz. Thus a high F_{div}/F_t-ratio of F_{div}/F_t=0.36 is obtained, which we ascribe to the utilization of the peaking in F_t and G_m. Also very short transition times of T_t(20%-80%)=35ps are obtained by applying a novel output-driver design, where we use a differential push-pull buffer/amplifier to drive an open drain differential output stage. Power dissipation is 740mW, and the output voltage swing is just above 800mV below toggle frequencies of 7.5GHz decreasing to 480mV at the maximum toggle frequency of 8.25GHz.

REFERENCES

1 Enoki T., Sugitani S. and Yamane Y.:'0.15µm GaAs MESFETs applied to Ultrahigh-Speed Static Frequency Dividers', Electronic Lett.,1989,Vol.25, No.8,pp.512-513.

2 Mishra U.K., Jensen J.F. et al.:'Ultra-High-Speed Digital Circuit Performance in 0.2µm Gate-Length AlInAs/GaInAs HEMT Technology', IEEE Electronic Device Letters,1988, Vol.9, No.9, pp.482-484.

3 Yamauchi Y. et al.:'A 34.8 GHz Static Divider using AlGaAs/GaAs HBTs', Technical Digest, GaAs IC Symposium, San Diego CA.,October 1989, pp.121-124.

4 Rein H.M.:'Multi-Gigabit-Per-Second silicon bipolar IC's for future optical-fiber transmission systems', IEEE Journal of Solid-State Circuits, Vol.23, No.3, June 1988, pp.664-675.

5 Tanaka K. et al.:'High Speed 8:1 Multiplexer and 1:8 Demultiplexer ICs using GaAs DCFL Circuit', Technical Digest, GaAs IC Symposium, Monterey CA, October 20-23 1991, pp.229-232.

6 Ohhata M. et al.:'13 Gb/s D-Type Flip-Flop IC using GaAs MESFETs', Electronic Letters, Vol.26, No.14, July 1990, pp.1039-1040.

7 Ohhata M. et al.:'Above 8-Gb/s GaAs Monolithic Flip-Flop ICs for very high-speed optical transmission systems', Technical Digest, GaAs IC Symposium, October 1988, pp.23-26.