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NONLINEARITIES IN SC DELTA-SIGMA A/D CONVERTERS

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ABSTRACT

The effects of using nonlinear low-gain opamps in switched-capacitor delta-sigma modulators are analyzed. Using unconventional topologies, the state variables are made essentially uncorrelated with the input signal, hence opamp nonlinearity will cause very little harmonic distortion. Nonlinearity errors, which are uncorrelated with the input, are called non-harmonic distortion. Using a correlated-double-sampling integrator, the non-harmonic distortion can be reduced to a level where other errors dominate.

1. INTRODUCTION

Nearly all low-distortion A/D converters (ADCs) make use of a highly-linear D/A converter (DAC) in a feedback loop. Due to their inherent linearity, single-bit DACs have found their use in analog delta-sigma modulators. The output from a single-bit delta-sigma modulator is a bitstream at a rate which typically is orders of magnitude higher than the Nyquist rate. By means of oversampling, noise shaping, low-pass filtering, and down sampling, high-resolution and low-distortion A/D conversion can be obtained at the Nyquist rate [1]. If a high oversampling ratio can be accepted, delta-sigma ADCs can yield signal-to-noise-and-distortion ratios which are limited only by thermal noise or clock jitter.

The technologies are continuously being scaled down and the supply voltage lowered. As a tradeoff for the high speed the technologies can offer and as a consequence of the low supply voltage, the achievable opamp gain may be quite low and nonlinear.

Low and nonlinear opamp gain will cause errors which can dominate both the THD and the SNR performance. The performance of the ADC will therefore not necessarily be determined by the linearity of the DAC in the feedback loop nor by thermal noise.

This paper will discuss how delta-sigma modulators can be designed to be robust to low and nonlinear opamp gain.

2. TOPOLOGY VERSUS THD

Figure 1 shows a model of a delta-sigma modulator. When stability is considered, all delta-sigma modulators with a linear loop filter can be modeled in this way. In the Figures, the quantizer performs both the single-bit A/D and D/A conversion.
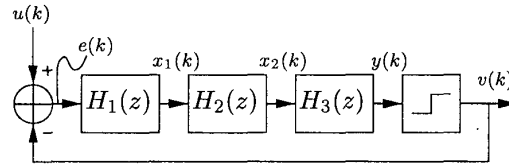
Figure 1: General model of a delta-sigma modulator.

2.1. Delta-Sigma ADC Operation

The signal $e(k)$ expresses the difference between the input $u(k)$ and the one-bit output $v(k)$. If the output $y(k)$ from the loop filter $H(z) = H_1(z)H_2(z)H_3(z)$ is kept bounded, the spectral components of $e(k)$ will be bounded inversely proportional to the gain of the loop filter.

The loop filter is designed to have a very high gain in the signal band and a small gain outside the signal band. A well-designed modulator can make $e(k)$ very small in the signal band; the output $v(k)$ will then equal the input $u(k)$. The problem is to keep $y(k)$ bounded, i.e., to keep the modulator stable. Good solutions are known and can easily be obtained using a toolbox [2].

2.2. The Sensitive Nodes in the Circuit

Analog circuits cannot be implemented without introducing errors. It is therefore important to know where the circuit is most sensitive to errors.

The aim in delta-sigma modulation is to keep $e(k)$ as small as possible in the signal band. The node where $e(k)$ appears is the circuit's most sensitive; any error in $e(k)$ can be referred directly back to $u(k)$ as either noise or distortion. The node where $x_1(k)$ appears is significantly less sensitive; when referred to the input, errors in $x_1(k)$ are suppressed by the large gain of $H_1(z)$. By continuing this argumentation, it follows that $x_2(k)$ and $y(k)$ are even less sensitive. Consequently, it is primarily imperfections in the first filter section $H_1(z)$ which can limit the modulator's performance.

2.3. Harmonic Distortion

Harmonic distortion is a consequence of applying a nonlinear operation to the input signal $u(k)$. That implies the following:

A modulator implemented according to Figure 1 will produce very little harmonic distortion.

The reason is simple: the loop filter's high signal-band gain assures that $x_2(k)$, $x_1(k)$, and $e(k)$ (in that order) will have less and less energy in the signal band. The signals of primary concern, $e(k)$ and $x_1(k)$, will therefore be essentially uncorrelated with the input $u(k)$. Hence, errors caused by imperfections in $H_1(z)$, including those caused by opamp nonlinearity, will be uncorrelated with $u(k)$. Ultimately, this implies that the modulator will not produce harmonic distortion.

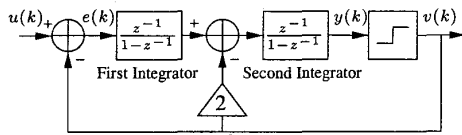## 2.4. A Popular Topology Which Generates Harmonic Distortion

Figure 2: Frequently used topology.

Figure 2 shows a topology which has often been used for analog delta-sigma modulators. A high loop gain in the baseband is obtained by cascading a number of integrators (here two). To stabilize the modulator, it is necessary to include zeros in the loop filter. This is obtained by making loops in the topology which do not include all integrator stages. The topology is often called "Cascaded Integrators with Feedback" because the smaller loops are realized as feedback branches to intermediate integrator stages.

The topology is not equivalent to Figure 1. It will next be explained why this modulator will produce harmonic distortion.

2.4.1. How The Modulator Produces Harmonic Distortion

In the modulator shown in Figure 2, spectral components representing $2u(k)$ will be part of the output from the first integrator. The first integrator will therefore have to be extremely well-performing to obtain a -100dB THD performance.

The contents of $2u(k)$ in the output from the first integrator can be verified by simulation. The explanation is however simple: The input to the second integrator cannot have significant power in the signal band; the high gain of the second integrator prevents that. The output from the first integrator must therefore balance the signal band contents of $2v(k)$. Because $e(k) = u(k) - v(k)$ is small in the signal band, the output from the first integrator will include spectral components representing $2u(k)$.

2.5. Robust Modulators

It is easy to design a modulator which does not produce significant amounts of harmonic distortion: simply use a topology which is equivalent to the topology shown in Figure 1.

Figure 3 shows two ways to redesign the modulator shown in Figure 2 to make it equivalent to the modulator shown in Figure 1. The modulator shown at the top makes use of the same feedback path to secure the modulator's stability. To compensate for the signal injected in this way, an extra signal path is included. Notice that the input to the second integrator is the output from the first integrator plus $2e(k)$. When modeled as in Figure 1, the first filter stage is described as
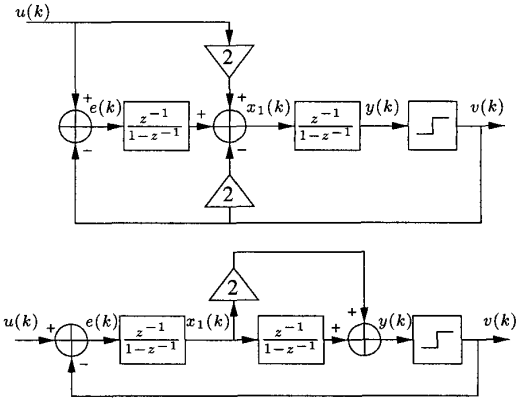

Figure 3: Low-THD equivalents of the modulator shown in Figure 2.

$H_1(z) = \frac{z^{-1}}{1-z^{-1}} + 2$, while the second filter stage is a simple delaying integrator. By switching the two filter stages, the topology shown at the bottom of Figure 3 arises. This alternative topology is often called "Cascaded-Integrators with Feed-forward (CIFF)."

It is an additional advantage that the signal swing of $x_1(k)$ is reduced significantly. That will save chip area and reduce the system's sensitivity to non-harmonic distortion.

3. NON-HARMONIC DISTORTION IN SC DELTA-SIGMA MODULATORS

By changing the modulator's topology, the input $u(k)$ can be decorrelated with the state variables $x_1(k)$, $x_2(k)$, ..., $y(k)$, however, this cannot remove the signals and thereby the errors which are caused by nonlinearities.

The effects of using nonlinear filter stages will be analyzed next. As discussed previously, it is only the first filter stage which has to be considered. For baseband modulators, this stage is an integrator. Some SC integrators and their non-idealities' impact on the modulator's performance will be analyzed.

3.1. The Basic SC Integrator

Figure 4: Basic switched-capacitors integrator.

Figure 4 shows a simple SC integrator which has been used to implement delta-sigma modulators [7]. It has the useful feature that it performs the subtraction of $u(k)$ and $v(k)$ with a single capacitor C_i. The chip area and the sampling noise is thereby kept at its minimum.

The voltage across C_f will represent an ideal integration of the charges $q_i(k)$ transferred during clock phases Φ_2. Due to imperfections in the opamp, the voltage across C_f will not

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be equal to V_{out}. However, when referred to the input, the difference is a non-accumulative error in $x_1(k)$ which will be suppressed by the gain of $H_1(z)$. Unless otherwise stated, it is assumed that the voltage across C_f equals V_{out}.

Let $g(V_{out})$ describe the opamp's input voltage as a function of V_{out}. The charge transfer $q_i(k)$ in the clock period k will then be proportional to the voltage change across the sampling capacitor C_i as described by the following Equation:

$$\frac{q_i(k)}{C_i} = [u(k) - v(k)] - g[x_1(k)] \qquad (1)$$

This Equation shows that, independent of the capacitance of capacitors C_i and C_f, the input referred voltage error is given by:

$$e_{error}(k) = -g[x_1(k)] \qquad (2)$$

3.1.1. Error Evaluation

The inverse opamp gain $g(V_{out})$ can be separated into an offset V_{offset}, a linear term μV_{out}, and a nonlinear term $n(V_{out})$:

$$g(V_{out}) = V_{offset} + \mu V_{out} + n(V_{out}) \qquad (3)$$

It is assumed that the modulator is designed to prevent harmonic distortion; i.e., such that $x_1(k) \simeq V_{out}(\Phi_2)$ contains very little energy in the signal band.

If the opamp is linear then $n(V_{out}) = 0$. The error $e_{error}(k)$ will be the offset V_{offset} and a small fraction μ of $x_1(k)$. Since $x_1(k)$ has very little energy in the signal band, the error $\mu x_1(k)$ will have even less energy in the signal band. Thus, the respective zero in the modulator's noise transfer function is moved slightly from $z = 1$ towards $z = 0$. That will in general not cause problems.

If the opamp is nonlinear the performance may get degraded significantly. The nonlinear term $n[x_1(k)]$ will fold energy from high frequencies back into the signal band. For all practical purposes, $n[x_1(k)]$ can be assumed to be white noise. If the opamp gain is low, this error may very well dominate the sampling noise.

In a low-gain environment, the error $n[x_1(k)]$ can be reduced by reducing the signal swing of $x_1(k)$. That will require a quite large C_f. In general, it will be a better choice to design the system as a multibit structure. In that case, a highly linear DAC in the feedback path is required. New research results show that this is feasible [3] [4] [5] [6].

Alternatively, the error $n[x_1(k)]$ can be made smaller by increasing the gain of the opamp. Correlated-double-sampling techniques can increase the effective gain of a low-gain opamp.

3.2. Correlated-Double-Sampling (CDS) Integrators

The fundamental property of any CDS scheme is that it will try to generate an improved virtual ground. Simple schemes can cancel offset and 1/f noise. More advanced schemes incorporate information about the previous or subsequent V_{out} to increase the effective gain of the opamp.
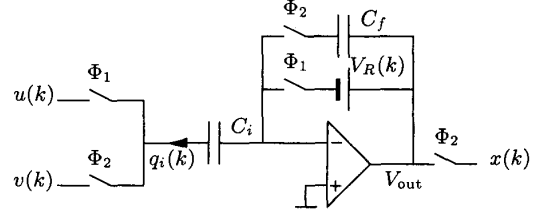

Figure 5: General model for a CDS integrator.

3.2.1. Modeling CDS

The model shown in Figure 5 can model most CDS schemes. At least, it is sufficiently general for the following discussion.

The voltage source $V_R(k)$ used in the feedback is typically implemented as a appropriately precharged dummy capacitor which can absorb the charge during the reset clock phase Φ_1. Details can be found in the literature [8].

3.2.2. Holding CDS

A holding CDS integrator will in the ideal case make $V_R(k)$ equal to the voltage across C_f. Usually $V_{out}(\Phi_2)$ is used as a substitute. Some schemes also depend on capacitor matching in which case some inaccuracy is to be expected. Neglecting such small errors at this point, the input $q_i(k)$ can be derived from:

$$\frac{q_i(k)}{C_i} = [u(k) - v(k)] + [g(x_1(k)) - g(x_1(k-1))] \qquad (4)$$

The input referred error is therefore given by:

$$e_{error,primary}(k) = [g(x_1(k)) - g(x_1(k-1))] \qquad (5)$$

This error is both small and first-order shaped. Consequently, in a highly oversampled environment, it will be very small in the signal band.

3.2.3. Predictive CDS

In clock phase Φ_1, a predicting CDS integrator attempts to predict what V_{out} will be in the following clock phase Φ_2. All known predicting CDS integrators rely on capacitor matching. Some inaccuracy is therefore to be expected. Neglecting such small errors at this point, the input $q_i(k)$ can be derived from:

$$\frac{q_i(k)}{C_i} = [u(k) - v(k)] + [g(x_1(k)) - g(x_1(k))] \qquad (6)$$

Accordingly, given the assumptions, the operation will be ideal.

3.2.4. Secondary Errors

The inaccuracy of $V_R(k)$ was neglected in the analysis of both the holding and the predicting CDS integrators. That is not a justifiable simplification. The errors discussed above will be called the primary errors. An additional input-referred error, called the secondary error, must be taken into account. For both the holding and the predicting integrators, the secondary error can be derived from:

$$e_{error,secondary}(k) = g'[x_1(k)] \Delta V_R(k) \qquad (7)$$

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The uncertainty $\Delta V_R(k)$ of the held or predicted voltage $V_R(k)$ is expected to be quite random. Since $x_1(k)$ is wide-spectered and since $g'(V_{out})$ is nonlinear, the first term $g'[x_1(k)]$ is wide-spectered as well. The secondary error, being the product of two wide-spectered signals, will have an approximately uniform spectral distribution (white noise).

Because the primary error (equations 5 and 6) is either first-order shaped or zero, the secondary error (equation 7) is expected to dominate if the oversampling ratio is high. Simulation results support this point of view.

3.2.5. Holding Versus Predictive CDS

If there is any difference, it is the author's belief that a holding CDS integrator will be the better choice. It is simpler to hold the old value than it is to predict the next. The uncertainty $\Delta V_R(k)$, and thereby the secondary error, is likely to be smaller for the holding CDS integrator. Furthermore, a holding CDS integrator is simpler to implement than a predicting CDS integrator.

4. SIMULATION RESULTS

To verify the derivations, a 4th order delta-sigma modulator, implemented in the CIFF topology shown in Figure 3 and with a quadruple zero at $z = 1$, was simulated with HSPICE using ideal switches and capacitors. The only incorporated non-ideality was the gain of each of the 4 opamps. It was described as a hyperbolic tangent with a maximum gain of 50dB. Each stage was driven to 85% of full scale which means that the opamp gain varied from about 38dB to 50dB. A holding CDS integrator, as shown in Figure 41 in [8], was used as the input stage.
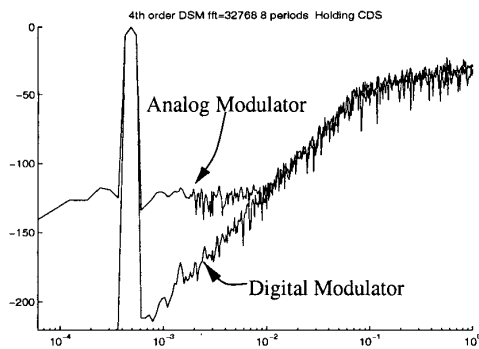

Figure 6: The effect of using opamps with finite and nonlinear gain. The Figure shows a 32768 point FFT. The frequency axis is normalized with respect to the Nyquist frequency.

Figure 6 shows the FFT of the output $v(k)$ of the analog modulator compared to the FFT of the output of a supposedly identical digital modulator. As expected, the modulator does not produce detectable harmonic distortion.

Figure 7 shows the FFTs of the output $v(k)$ and the primary and secondary errors as defined by equations 5 and 7. As expected, the primary error is first-order shaped and it does not limit the performance for any oversampling ratio. Had this error not been shaped, as for the integrator shown in Figure 1,

it would have limited the SNR performance at around 70dB SNR @ 100 times oversampling.

The secondary error is also shown. As expected, it is an unshaped error. The Figure clearly shows that this is the limiting factor in the modulator. The SNR performance is around 110dB @ 100 times oversampling. The sampling capacitor C_i has to be 16.5pF to bring the sampling noise to the same low level (assuming a 2Vpp signal swing).
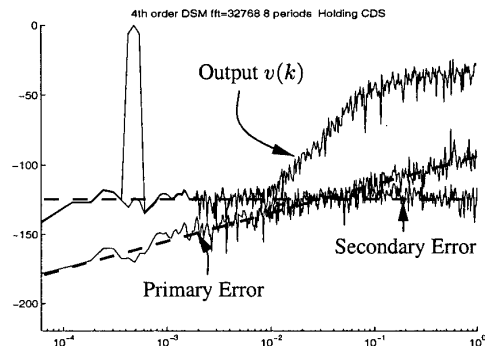

Figure 7: The FFTs of output $v(k)$ and the primary and secondary errors. Notice the match of $v(k)$ and the secondary error for low frequencies.

5. SUMMARY

The topology in which an analog delta-sigma modulator is implemented will affect its THD performance. The input to the quantizer should be the only node in the modulator which is significantly correlated with the input signal.

If a technology only offers low-gain nonlinear opamps, CDS techniques can improve the performance significantly. Simulations show that a 16bit ADC can be implemented with quite poor opamps. The concept of primary and secondary CDS errors has been introduced. The secondary error is typically neglected in the analysis, but it is nevertheless often the dominating error source. When used in delta-sigma modulators, holding CDS seems more promising than predictive CDS.

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